4ESS™ Switch With 1B Processor Master Control Complex (MCC) Description

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1. Overview

1.01 This practice describes the new Master Control Complex (MCC) control and display interface used in the *4ESS*™ Switch with a 1B Processor. The MCC interface provides one of the primary human interfaces for the *4ESS* switching system. This practice supports the 1B Processor master control complex equipment.

1.02 This practice is being reissued for general updates and to provide support for the *4ESS* Switch 4E24 Generic.

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1.06 Every effort has been made to ensure that the information in this practice is complete and accurate at the time of printing; however, information is subject to change.

1.07 This practice was developed by the Lucent Technologies Customer Training and Information Products Organization.

2. Introduction

2.01 This practice describes the MCC terminal interface that is provided with the AT&T 1B Processor in the *4ESS* Switch. This practice includes information about the MCC interfaces for both on-site and remote MCC terminals.

2.02 The MCC interfaces support all the control and display capabilities required to perform switch maintenance. This is with the exception of the Attached Processor System (APS) which provides its own maintenance interface.

2.03 Figure 1 provides a high-level architectural view of the MCC on-site and remote interfaces.

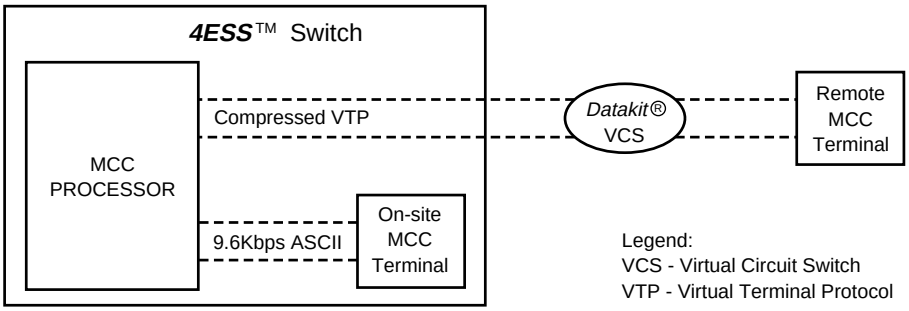

Figure 1. MCC High-Level Architecture

2.04 Although not explicitly shown in Figure 1, the 1B Processor provides four Control and Display (C&D) ports which are designated as the MCC interface.

NOTE:
The MCC interface is separate and should not be confused with the *4ESS* Switch maintenance terminal interface.

2.05 Typically, two of the four MCC ports provide on-site MCC terminal interfaces for the local *4ESS* Switch maintenance personnel while the other two ports provide remote maintenance interfaces to the 1B Processor.

2.06 As shown in Figure 1, the remote MCC interface connects the remote MCC terminals to the MCC Processor via the *Datakit*® Virtual Circuit Switch. This interface can be routed to a different operating system and/or work center depending on the customer's remote maintenance configuration.

2.07 For example, a possible configuration for Network Service Division (NSD) would be to route the remote MCC interface via the *Datakit* VCS to the Total Network Management (TNM) system. In turn, the TNM system could provide access to various remote work centers such as the Network Control Center (NCC).

2.08 The intent of the remote interface is to provide personnel at the remote maintenance site with the same control and display capabilities as available to on-site personnel.

NOTE:
Throughout this practice, the term "control" refers to the ability to effect changes in the state of the 1B Processor or *4ESS* Switch. This control may range from releasing alarms to forcing a processor reconfiguration. The term "display" refers to the functions involved in providing status indications to the maintenance personnel. This is achieved through the use of various display features at the user's workstation.

3. MCC Interfaces

3.01 Figure 2 provides a basic block diagram of the MCC interfaces at the *4ESS* Switch with a 1B Processor. The MCC interfaces consist of a dual processor configuration referred to as the MCC and Utility Processors (MUPs). The two MUPs are designated MUP 0 and MUP 1.

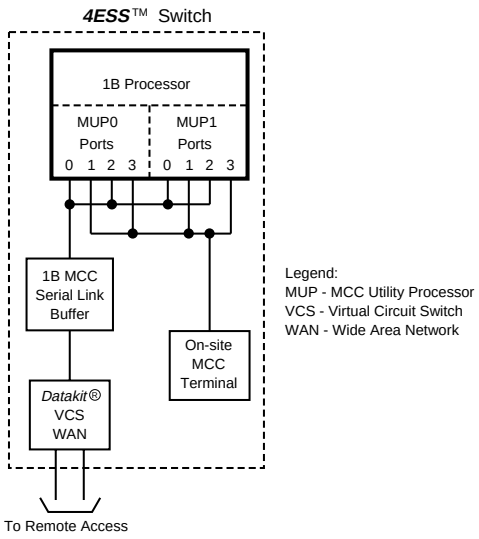

Figure 2. *4ESS* Switch MCC Interface

3.02 Only one MUP is active at a time. The second MUP will operate in a warm standby, non-matching mode. A standby MUP may be taken out-of-service for diagnostics, testing and/or repair.

3.03 During 1B Processor recovery, the MUP will perform all data display functions. The MUP power supply is separate from the 1B Processor power supply. This includes separate power converters, power switches, fusing, etc. This configuration ensures that the MUP will maintain all Emergency Action Interface (EAI) functionalities should a 1B Processor power failure occur.

3.04 The *4ESS* Switch MCC interface must support control and display terminals at both the on-site and remote locations. Each location (on-site and remote) will have access to two MCC ports. The two ports will ensure that both sites have a backup terminal.

3.05 Switch reliability requirements dictate that all terminals at *4ESS* Switch sites must conform to National Equipment and Building Standards (NEBS) requirements, especially in the areas of office power, holdover and interference.

NOTE:
If a non-NEBS compliant terminal is used in an emergency situation, it is imperative that the terminal be replaced with a NEBS compliant terminal as quickly as possible.

NOTE:
Since each MCC terminal is driven by an MCC port, the terms "terminal" and "port" will refer to the same throughout the remainder of this practice.

3.06 Each MUP supports four MCC compatible ports, numbered 0, 1, 2 and 3. Each port will be fully operational as long as one MUP is active. All four MCC ports will operate at 9600 bps in full-duplex.

3.07 The four MCC ports operate independently. This means the MCC will be able to transmit/receive messages from all four ports simultaneously. The MUP will synchronize the information displayed to all four ports (for example, if the same data is displayed to two or more ports, the MUP will keep the data at the ports synchronized).

3.08 MCC ports 0 and 2 are mated as are ports 1 and 3. Mated ports are physically positioned on separate hardware devices for greater reliability. A user at a terminal connected to port 0 or 2 will have the ability to inhibit ports 1 and 3.

NOTE:
When a port is inhibited, the MCC display information will continue to be accessible at that terminal and the user will be able to request and observe the different MCC display pages. However, all other MCC functions associated with the MCC interface will be inhibited.

3.09 The MCC ports can terminate at either on-site or remote locations as dictated by the switch maintenance needs. Ports 0 and 2 should terminate at the location which is to have primary maintenance responsibility for the switch. As shown in Figure 2, customers who perform switch maintenance remotely will assign Ports 0 and 2 to a remote maintenance site (such as, the NCC work center for NSD users). Ports 1 and 3 may be used for local connections. For customers who perform switch maintenance locally (such as the Local Exchange Carriers (LECs)), ports 0 and 2 will connect to the on-site MCC terminals and ports 1 and 3 may either be connected to a remote location or unused.

3.10 The MUP will code the MCC display pages in two output formats:

- American Standard Code for Information Interchange (ASCII) for local, on-site applications
- Compressed Virtual Terminal Protocol (VTP) interface for remote applications.

The *4ESS* Switch will automatically determine the appropriate output format to use on each port without user intervention.

3.11 An inhibit on Ports 1 and 3 will be automatically removed if one of the following conditions occur:

(1) If Ports 0 and 2 are both timed out by the *4ESS* Switch while they are in the VTP mode

NOTE:
If Ports 0 and 2 resume the VTP mode, the inhibit will not be automatically reactivated on Ports 1 and 3.

(2) If Data Terminal Ready (DTR) is lost on both Ports 0 and 2 while they are in the ASCII mode.

3.12 The MUP will permit ports which are mated to transmit in different formats. This means that either port may transmit in compressed VTP or ASCII format regardless of what the other port is doing. The MUP will perform character echo and command line editing for non-VTP formatted ports.

NOTE:
Command line editing includes line erase and single-stroke, single-character erase.

3.13 Character echo and command line editing on VTP formatted ports will be performed by the remote MCC interface system (for example, TNM) rather than by the MUP. When the MUP receives VTP control characters that are not printable on an ASCII formatted port, these characters will not be echoed to the terminal. Echoing nonprintable characters can have unpredictable results on some terminals.

On-Site MCC Interface

3.14 The local on-site MCC terminal interface (Figure 2) is directly driven from the MUP in a 9600 bps ASCII format. This interface is capable of operating with either MUP (0 or 1) from port pairs 0 and 2 or 1 and 3. The local MCC interface has the same control and display capabilities as the remote MCC interface.

Remote MCC Interface

The remote MCC terminal interface (Figure 2) is indirectly driven from the MUP in a 9600 bps compressed Virtual Terminal Protocol (VTP) format. As shown in Figure 2, the remote MCC interface consists of the following components:

- MUP interface port
- 1B MCC Serial Link Buffer
- *Datakit* VCS Wide Area Network (WAN).

3.15 The MUP interface port is capable of operating with either MUP (0 or 1) from port pairs 0 and 2 or 1 and 3. The remote MCC interface has the same control and display capabilities as the local on-site MCC interface.

3.16 The 1B MCC Serial Link Buffer (sometimes referred to as MUP PUP) is an in-line buffering device used to buffer data between the compressed VTP interface and the MUP.

3.17 The *Datakit* VCS WAN provides sufficient connectivity to interface all customer-designated MCC remote ports to the desired remote work center. *Datakit* VCS is capable of supporting either 9600 bps or 56K bps synchronous channels between each *4ESS* Switch site and the remote work center.

4. MCC Interface Display Pages — General Descriptions

4.01 The primary function of the MCC interface is to provide the control and display functionalities of the 4ESS Switch in a Video Display Terminal (VDT) format. The MCC's VDT format is presented in the form of "display pages."

Display Pages

4.02 Table A describes the different MCC terminal display pages. As shown in Table A, each display page is assigned a unique page access poke command. All display page access poke commands and titles are identified on the MCC page index (Page 100). When the display page access poke command is entered at the MCC terminal, the MUP will paint the corresponding display page onto the MCC terminal screen.

4.03 The EAI Page is assigned a special programmed function key on the MCC terminal keyboard. The EAI Page function key is labeled **EA DISP**. When the **EA DISP** key is depressed, the MUP will paint the EAI Page onto the MCC terminal screen.

4.04 An additional programmed function key is available on the MCC terminal keyboard whenever the EAI Page is displayed. This function key is labeled **NORM DISP**. When the EAI Page is actively displayed on the MCC terminal screen and the **NORM DISP** key is depressed, the MUP will erase the displayed EAI Page and repaint the screen with the last "normal" (non-EAI) page previously displayed. If there is no previous normal page to be displayed (for example, after power-up) when the **NORM DISP** key is depressed, the MUP will erase and repaint the screen with the Page Index (Page 100).

Table A. MCC Terminal Display Pages

Page Access Poke Command	Page Name	Page Description
EAI	Emergency Action Interface (EAI)	The EAI Page provides access to critical controls and functions required to perform system recovery actions. The EAI page will be the default page displayed whenever communication is first initialized at the MCC terminal. The EAI page is accessed by depressing the **EA DISP** function key.
100	Page Index	The Page Index lists all MCC pages and identifies the page access poke command for each applicable MCC page. The Page Index is accessed by entering Poke Command **100**.
101-105	Reserved	Not assigned.
106	MUP Status and Control	The MUP Status and Control page provides specific status and control information about the MCC and Utility Processors (MUPs). The MUP Status and Control page is accessed by entering Poke Command **106**.
107	Reserved	Not assigned.
108	System Status	The System Status page provides overall switching status, alarm information and hardware equipment status for the *4ESS* Switch. The System Status page is accessed by entering Poke Command **108**.
109	Program Store Status and Control	The Program Store Status and Control page provides 1B Processor program store information such as the current program store configuration and program store M-code configuration in addition to program store bus status. The Program Store Status and Control page is accessed by entering Poke Command **109**.
110	Call Store Status and Control	The Call Store Status and Control page provides 1B Processor call store information such as the current call store configuration and call store M-code configuration in addition to call store bus status. The Call Store Status and Control page is accessed by entering Poke Command **110**.

Table A. MCC Terminal Display Pages (Contd)

Page Access Poke Command	Page Name	Page Description
111	IFB Clients Status and Control	The IFB Clients Status and Control page provides the status of all IFB clients. Existing IFB clients and new IFB clients are reflected on this page. The IFB Clients Status and Control page is accessed by entering Poke Command **111**.
112-117	Reserved	Not assigned.
118	1B Processor Status	The 1B Processor Status page provides 1B Processor configuration data for the central control, program store bus, call store bus, peripheral unit bus, interface bus, interface bus clients, auxiliary unit bus and auxiliary unit bus units. The 1B Processor Status page is accessed by entering Poke Command **118**.
119	Direct Data Insert (DDI) Key Options	The DDI Key Options page consists of a two-page format identifying the Modified Recovery Actions DDI key assignments and the Inhibit Interrupts DDI key assignments. The user can toggle between the two pages by using Poke Command **499**. The Direct Data Insert (DDI) Key Options page is accessed by entering Poke Command **119**.
120	Data Display	The Data Display page provides memory displays, data insert keys and utility functions used to read, write and control 1B Processor functionality. The Data Display page requires special maintenance capabilities and is intended to aid experienced personnel who are familiar with 1B Processor hardware and software. The Data Display page is accessed by entering Poke Command **120**.

Table A. MCC Terminal Display Pages (Contd)

Page Access Poke Command	Page Name	Page Description
1990	Dead Start	The Dead Start page provides the functionality to restore an insane 1B Processor's sanity when automatic and manual efforts to restore sanity via the EAI Page have not been successful. The Dead Start page requires special maintenance capabilities and is intended to aid experienced personnel who are extremely familiar with 1B Processor hardware and software. The Dead Start page is accessed by entering Poke Command **1990**.

A. Display Page Layout

4.05 Figure 3 illustrates the layout of an MCC display page using the Page Index (Page 100) as an example with callouts identifying the display page common areas.

4.06 All MCC display pages conform to the same basic layout as shown in Figure 3. Each display page consists of 24 vertical lines. The page layout for all display pages is divided into the following common areas:

- System Identification Area (Line 1)
- Summary Status Area (Lines 2 and 3)
- Command Line Area (Line 4)
- Application Page Display Area (Lines 5-23)
- Error/Status Message Area (Line 24).

4.07 In Figure 3, note the small squares (□) beside the MUP and PORT fields in the System Identification Area (Line 1). These squares indicate fields that will contain specific data when the actual MCC page is displayed.

NOTE 1:
Throughout this practice, the small squares will be used in the example display pages to indicate specific data fields.

NOTE 2:
The column of line numbers to the left of Figure 3 will not appear on the actual MCC displays. The line numbers are included in this practice to provide a convenient way of referring to the different areas of the display pages.

B. Display Colors

4.08 In addition to text on the MCC terminal display pages, different colors are used to convey information to the user. The color scheme is used to indicate the following:

- Normal operating conditions
- Trouble/alarm/error conditions
- Indicator status.

4.09 A two-color background/foreground scheme is used to convey indicator status information. The "foreground" is defined as the colored letters or numbers that make up the indicator and the "background" is defined as the color that surrounds the letters or numbers. All foreground and background colors have specific meanings when used in different combinations. Table B identifies each foreground and background color and their specific meaning when used in the various color combinations on the MCC terminal display pages.

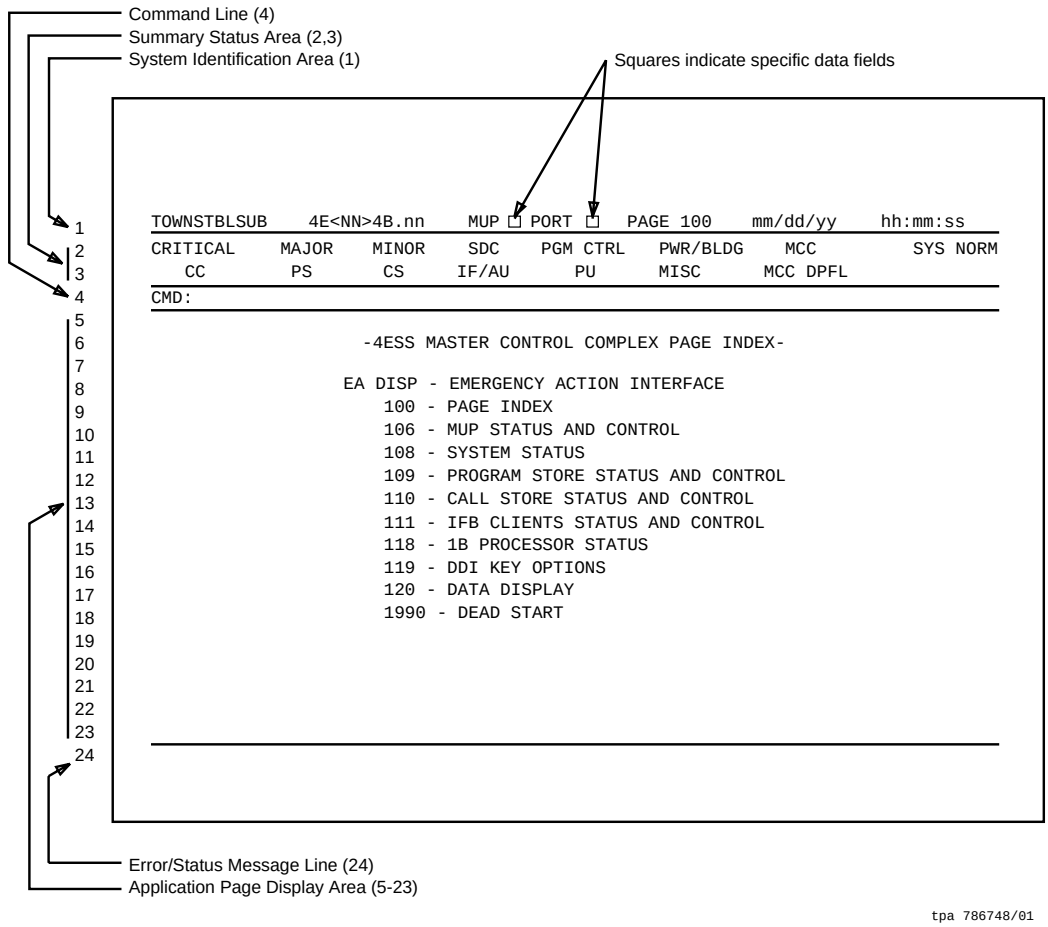

Figure 3. Display Page Example

Table B. Display Page Indicator Background and Foreground Color Definitions

Background	Foreground	Meaning
Black	-	Identifies normal information or text
Black	White	Information - Normal Conditions
Black	Yellow	Instruction - Normal Conditions
White	-	Identifies a selected state
White	Black	Selected for non-force indicators
White	Purple	Selected for force indicators
Purple	-	An option that has been forced in hardware registers
Purple	Black	Force has been activated in hardware
Purple	Light Blue	Forced but hardware error present
Yellow	-	Identifies a minor problem
Yellow	Black	Minor problem - Status verified
Yellow	Red	Minor problem - No status available
Red	-	Identifies a major problem, critical problem or out-of-service state
Red	White	Major problem
Red	White (Flashing)	Critical problem
Red	Black	Out-of-Service (OOS) unit
Red	Yellow	Forced but hardware error present
Red	Light Blue	Forced but hardware error present
Green	-	Identifies an active unit or system normal condition
Green	Black	Active unit or status normal
Blue	-	Identifies a standby unit
Blue	White	Standby unit
Light Blue	-	Off-normal unalarmed condition
Light Blue	Black	Situation-specific meaning

Command Entry

4.10 All MCC display pages except the Emeregency Action Interface (EAI) page are displayed on the MCC terminal by entering a page access poke command followed by a carriage return. The EAI Page is displayed by depressing the MCC terminal **EA DISP** key. Table C identifies the page access poke commands assigned to the different MCC display pages.

Table C. MCC Page Access Poke Commands

Poke Command	MCC Display Page
100	Page Index
106	MUP Status and Control
108	System Status
109	Program Store Status and Control
110	Call Store Status And Control
111	IFB Clients Status And Control
118	1B Processor Status
119	DDI Key Options
120	Data Display
1990	Dead Start
EA DISP Key	Emergency Action Interface

4.11 The following general guidelines must be used when entering MCC poke commands:

- Only one command may be entered at a time.
- Commands that require options/arguments will be rejected if the proper options/arguments are not included.
- Commands that require options/arguments will be rejected if commas are not used to separate the command and each option/argument.
- Intervening blanks will be permitted within commands.

NOTE:
Some "special" MCC functions are activated by entering a control/escape sequence or by depressing a specific programmed function key on the MCC terminal keyboard. These special functions are described later in the "Special Command Functions" section of this practice.

There are two types of MCC poke commands, local and global. The meaning of local poke commands depends on the current display page while the meaning of global poke commands is independent of the current display page. However, the global poke command and current display page independency does not mean that global poke commands will be accepted on every display page. Table D identifies the various poke command identifiers and types.

Table D. MCC Poke Command Identifiers and Types

MCC Poke Command			
Identifier	**Type**	**Identifier**	**Type**
0-99	Local	100-199	Global
200-299	Local	300-399	Local
400-499	Local	500-599	Local
600-699	Global	700-799	Global
800-899	Global	900-999	Global
1000-1999	Global		

A. MCC Command Acknowledgments

4.12 All MCC commands will receive an appropriate acknowledgment (accepted or rejected) on the display page command line. Commands that can be performed will be acknowledged as accepted, and commands that cannot be performed will be acknowledged as rejected supported with an appropriate explanation.

4.13 All acknowledgments conform to the Program Documentation Standards as specified in the ***4ESS*** *Switch Input Message Manual*, IM-4A000-01, Volume 1.

4.14 A valid command will be acknowledged with one of the following acknowledgments:

IP In Progress — The request was received and initiated. An output at the 1B Processor Maintenance (MTC) terminal and MCC display page changes will follow.

OK Confirmed — The request was accepted and completed.

PF Printout Follows — An output at the 1B Processor MTC terminal will follow.

RL Repeat Later — The request cannot be executed currently due to unavailable system resources.

4.15 An invalid command will be rejected with one of the following acknowledgments:

NA No Acknowledgment — Normally, the system acknowledges a command within 2 to 5 seconds. If control of message processing has been lost, the No Acknowledgment (NA) response is output to indicate an acknowledgment failure.

NG No Good — The command syntax is valid, but the request conflicts with current system or equipment status.

?A The command action field contains an error.

?D The command data field contains an error.

?E A command syntax error exists (for example, there are missing parameters, too many parameters, missing commas, too many commas, etc.).

?I The command identification field contains an error.

?R Resources are not available.

4.16 Unless otherwise stated, the following general acknowledgment rules apply to all commands:

- Every accepted poke command will be acknowledged with an "OK" acknowledgment and every rejected poke command will be acknowledged with an "NG" acknowledgement.
- If an unknown poke command is entered or if an unknown escape/shift sequence is entered, the action will be rejected and acknowledged with a "?A" acknowledgment.
- If a poke command is entered with an invalid parameter, the action will be rejected and acknowledged with a "?D" acknowledgment.
- If a poke command is entered with an incorrect number of parameters, missing parameters, missing commas, or too many commas, the action will be rejected and acknowledged with a "?E" acknowledgement.

B. Special Command Functions

4.17 The following special command functions will be accepted regardless of the MCC page currently displayed.

NOTE:
Throughout this practice, functions that are activated by an escape/control sequence are shown in the format "<ESC>, <CNTL>, <x>." This means the MCC keyboard keys should be depressed in the order of Escape, Control and x.

EA DISP When the **EA DISP** key is depressed or when the sequence "<ESC>, <SHIFT>, <o>, <p>" is entered, the MCC terminal screen will be cleared and the EAI Page will be displayed. The EAI Page provides access to critical controls and functions required to perform system recovery actions. The EAI Page is the default page displayed whenever communications at the MCC terminal are disrupted or first initialized.

NORM DISP When the **NORM DISP** key is depressed or when the sequence "<ESC>, <SHIFT>, <o>, <q>" is entered, the MCC terminal screen will be cleared and the current page will be repainted in its entirety (refreshed).

When the EAI Page is currently displayed and the **NORM DISP** key is depressed, the page displayed before the EAI Page will be repainted. In some cases such as after a MUP switch via an "<ESC>, <CNTL>, <x>" command sequence, a page prior to the EAI Page will not exist. Under these circumstances when the **NORM DISP** key is depressed, the Page Index (Page 100) will be displayed.

RETIRE ALARM

When the **RETIRE ALARM** key is depressed or when the command sequence "<ESC>, <SHIFT>, <o>, <s>" is entered, all *4ESS* Switch alarms currently active will be retired and the CRITICAL indicator in the summary status area of all MCC display pages will be reset to normal (white on black).

If an alarm is cleared and the conditions causing the alarm still exist, the alarm will be reactivated.

C. Escape/Control Sequences

CAUTION:
The escape/control sequences described in this section should only be used in emergency situations when all other obvious solutions have been exhausted.

NOTE:
When commands involving escape sequences are discussed, the syntax in this document refers to the character stream actually input at the on-site MCC terminal and received by the *4ESS* Switch. This is an important distinction because the No. 2B SCCS and TNM operating systems do not transmit the first escape <ESC> entered by the user. Consequently, a user at the remote work center (for example, NCC) wishing to force an unconditional MUP switch ("<ESC>, <CNTL>, <x>") would need to enter "<ESC>, <ESC>, <CTRL>, <x>" to initiate the switch.

<ESC>, <CNTL>, <x>

CAUTION:
All Utility System UCD matcher and monitor store information will be lost.

The command sequence "<ESC>, <CNTL>, <x>" will cause the following action regardless of where (MCC port or display page) the sequence is entered:

- An unconditional switch of the active MUP.
- All control and display screens to be cleared and the EAI Page displayed.
- The status of all 1B Processor indicators to be rebuilt.
- All MUP indicators to be reset to default values.
- The MCC indicator in the Summary Status Area of the EAI Page to indicate a major problem
- The RLS MCC FORCE indicator on the MUP Status And Control Page (Page 106) to indicate that the MCC has been forced.

- A 1B Processor interject to occur.
- Ports 1 and 3 to be allowed if they were previously inhibited.

The "<ESC>, <CNTL>, <x>" command sequence will be recognized and acted upon even if entered from an inhibited port.

<ESC>, <CNTL>, <r>

CAUTION:
All Utility System UCD matcher and monitor store information will be lost.

The "<ESC>, <CNTL>, <r>" command sequence will cause the following action regardless of where (MCC port or display page) the sequence is entered:

- All control and display screens to be cleared and the EAI Page displayed.
- The status of all 1B Processor indicators to be rebuilt.
- All MUP indicators to be reset to default values.
- A 1B Processor interject to occur.
- Ports 1 and 3 to be allowed if they were previously inhibited.

The "<ESC>, <CNTL>, <r>" command sequence will be recognized and acted upon even if entered from an inhibited port.

5. MCC Terminal Display Page — Common Areas

5.01 As illustrated in Figure 3, all MCC terminal display pages have the following display areas in common:

- System Identification Area (Line 1)
- Summary Status Area (Lines 2 and 3)
- Command Line Area (Line 4)
- Application Page Display Area (Lines 5-23)
- Error/Status Message Area (Line 24).

Details describing the MCC terminal display page common areas are provided in the following paragraphs.

System Identification Area

5.02 The System Identification Area (Figure 4) will appear as the first line of each MCC terminal display page. All indicators in this area will appear white on black.

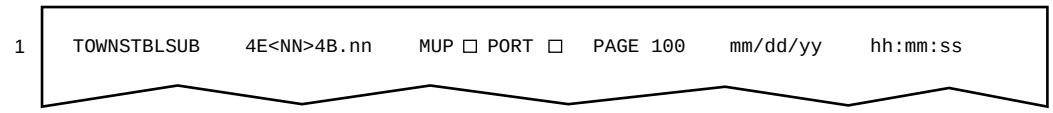

Figure 4. Display Page System Identification Area

NOTE:
The small squares shown in the examples throughout this practice indicate specific data fields that will be filled with appropriate data on the actual MCC display page.

Indicators displayed in the System Identification Area (Line 1) are as follows:

CLLI Code The CLLI* code is an 11-character field that identifies the *4ESS* Switch office that is associated with the MCC display page.

NOTE:
If the MUP has never established communication with the 1B Processor since power up or a software reset (such as, "<ESC>, <CNTL>, <r>"), the characters **??????????** will be displayed in place of the CLLI code.

Generic Identifier The generic indicator identifies the name of the current *4ESS* Switch software release (generic program) in the form **4E<*NN*>4B.*nn***. The "NN" identifies the software release issue and "nn" identifies the point issue.

MUP The MUP indicator identifies the active MUP in the form **MUP *n***. The "n" identifies the active MUP member number (0 or 1). The MUP indicator will be updated whenever a MUP configuration change occurs. The default MUP member number is zero (0).

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PORT The PORT indicator identifies the active port connection for the MCC terminal in the form **PORT *n***. The "n" identifies the port (0, 1, 2 or 3) where the MCC terminal data link is connected. The PORT indicator will be updated whenever a port configuration change occurs. The default PORT connection is zero (0).

PAGE The PAGE indicator identifies the MCC terminal display page currently being displayed in the form **PAGE *cccc***. The "cccc" identifies the current MCC page number. The PAGE indicator will be updated whenever an MCC terminal display page change occurs. The default MCC display page is the EAI page.

Date Identifier

The date indicator identifies the current date in the form ***mm/dd/yy*** (month/day/year). The date indicator is updated daily. The default value is 99/99/99. The date default value will be displayed if the MCC loses communication with the 1B Processor for more than 10 seconds. The date indicator will appear white on black when the indicator is in the normal state displaying a month, day and year. However, the date indicator will appear white on red when in the default state (99/99/99).

Time Identifier

The time indicator identifies the current time in a 24-hour format as ***hh:mm:ss*** (hour:minutes:seconds). The time is updated every 3 seconds. The default value is 00:00:00. If the correct time is unavailable to the MUP, the date indicator will be reset to its default value (99/99/99) and the time will be updated by the MCC every 3 seconds. The time indicator will alternate between white on black and black on green every 3 seconds as the time is updated by the MUP. The color alternating sequence verifies normal MUP operations.

Summary Status Area

5.03 The Summary Status Area (Figure 5) will appear as the second and third line of each MCC terminal display page. The summary status area provides status indicators for the *4ESS* Switch.

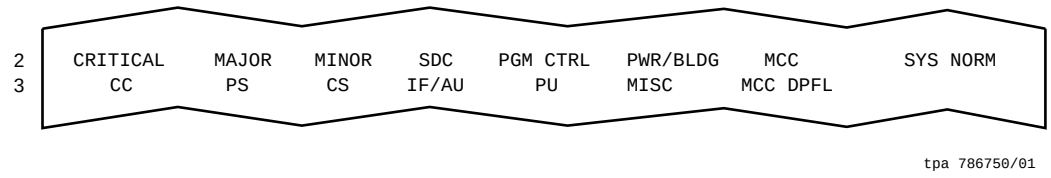


Figure 5. Display Page Summary Status Area

5.04 Indicators displayed in the Summary Status Area (Line 2) are as follows:

CRITICAL The CRITICAL indicator normally appears white on black indicating that there are no critical alarms. If a critical alarm occurs, the CRITICAL indicator will flash white on red. The indicator will continue to flash white on red until the **RETIRE ALARM** key on the MCC terminal keyboard is depressed (even if the condition that caused the alarm has been cleared). If the **RETIRE ALARM** key is depressed before the alarm condition is cleared, the MUP will return the CRITICAL indicator to its normal state but the indicator will activate again as soon as the central control reports the alarm condition.

MAJOR The MAJOR indicator normally appears white on black indicating there are no major alarms. If a major alarm occurs, the MAJOR indicator will appear white on red. The alarm will continue to appear white on red until the **RETIRE ALARM** key on the MCC terminal keyboard is depressed (even if the condition that caused the alarm has been cleared). If the **RETIRE ALARM** key is depressed before the alarm condition is cleared, the MUP will return the MAJOR indicator to its normal state but the indicator will activate again as soon as the central control reports the alarm condition.

MINOR The MINOR indicator normally appears white on black indicating that there are no minor alarms. If a minor alarm occurs, the MINOR indicator will appear black on yellow. The alarm will continue to appear black on yellow until the **RETIRE ALARM** key on the MCC terminal keyboard is depressed (even if the condition that caused the alarm has been cleared). If the **RETIRE ALARM** key is depressed before the alarm condition is cleared, the MUP will return the MINOR indicator to its normal state but the indicator will activate again as soon as the central control reports the alarm condition.

SDC The SDC indicator normally appears white on black indicating that there is no Service Degrading Condition (SDC) in effect. If such a condition occurs, the SDC indicator will appear white on red. The SDC indicator provides status for the 1B Processor, the Attached Processor System (APS), and the Common Network Interface (CNI) ring.

PGM CTRL The PGM CTRL indicator normally appears white on black indicating that there are no Program Controls (PGM CTRL) in effect. If any interrupts or audits are inhibited, any recent changes restricted or any other defined "off-normal" conditions are in effect, the PGM CTRL indicator will appear black on yellow.

PWR/BLDG The PWR/BLDG indicator normally appears white on black indicating that there are no power or building (PWR/BLDG) faulty conditions in effect. If a power fault or environmental fault is detected by the *4ESS* Switch, the PWR/BLDG indicator will appear black on yellow. The PWR/BLDG indicator will continue to appear black on yellow until the faulty condition is corrected.

MCC The MCC indicator normally appears white on black indicating that there are no MCC alarms. If either MUP is in an off-normal condition, the MCC indicator will appear black on yellow. If there is a major problem with the MCC or the Utility Interface switch is in the "enabled" position, the MCC indicator will appear white on red. If a MUP force is active, the MCC indicator will appear black on purple.

SYS NORM The SYS NORM indicator normally appears black on green indicating that there are no abnormal conditions in the *4ESS* Switch. If one or more of the other status indicators go off-normal, the SYS NORM indicator will appear white on black. The SYS NORM indicator serves as a check against the operation of all other indicators and will provide maintenance personnel with a visual indication of the overall switch operation.

5.05 Indicators displayed in the Summary Status Area (Line 3) are as follows:

CC The CC indicator normally appears white on black indicating that there are no Central Control (CC) alarm conditions. If a 1B Processor CC unit is out-of-service or if the CC displays a "trouble", "power" or "stopped" indicator, the CC indicator will appear white on red. If a CC force is active, or the Disable Auto PC function is activated, the CC indicator will appear black on purple.

PS The PS indicator normally appears white on black indicating there are no program store (PS) alarms. If one or more, but not all, of the spare program stores go out-of-service, the PS indicator will appear black on yellow. If all spare program stores go out-of-service or if a Program Store Bus (PSB) goes out-of-service, the PS indicator will appear white on red.

CS The CS indicator normally appears white on black indicating there are no Call Store (CS) alarms. If one or more, but not all, of the spare call stores go out-of-service, the CS indicator will appear black on yellow. If all spare call stores go out-of-service or if a Call Store Bus (CSB) goes out-of-service, the CS indicator will appear white on red.

IF/AU The IF/AU indicator normally appears white on black indicating that there are no interface alarms. Table E identifies the IF/AU indicator colors for each alarmed condition.

Table E. IF/AU Indicator

IF/AU Client Out-of-Service	IF/AU Indicator NORMAL	IF/AU Indicator ALARM
AUB	White on Black	Black on Yellow
MUP	White on Black	Black on Yellow
SSD	White on Black	Black on Yellow
API	White on Black	Black on Yellow
DUS (See Note)	White on Black	Black on Yellow
IFB	White on Black	White on Red
AUI	White on Black	White on Red

NOTE:
The DUS units are not functional in 4E22 and later generics. The IF/AU indicator may detect a DUS unit Out-of-Service if the DUS units remain "equipped" in translations.

PU The PU indicator normally appears white on black indicating that there are no Peripheral Unit (PU) alarms. If any peripheral unit in the peripheral equipment status area of MCC Page 108 is in an alarmed state, the PU indicator will appear the same color as the highest alarmed unit. A minor alarmed unit will produce black on yellow, a major alarmed unit will produce white on red and a critical alarmed unit will produce flashing white on red.

MISC The MISC indicator normally appears white on black indicating that there are no Fan System (FNS), Input/Output Unit Selector (IOUS), Input/Output Unit Controller (IOUC), Power Conversion and Distribution (PCD) or Miscellaneous Power (XPWR) alarms. If either of the FNS, IOUS, IOUC, PCD or XPWR indicators in the processor equipment status area of MCC Page 108 is in an alarmed state, the MISC indicator will appear the same color as the highest alarmed unit. A minor alarmed unit will produce black on yellow, a major alarmed unit will produce white on red and a critical alarmed unit will produce flashing white on red.

MCC DPFL The MCC DPFL indicator normally does not appear when the MCC is communicating properly with the 1B Processor. If the MUP is duplex failed from the 1B Processor's perspective, the MCC DPFL indicator will appear flashing white on red.

Command Line Area

5.06 The Command Line Area (Figure 6) will appear as the fourth line of each MCC terminal display page. All commands will be entered at the command line. The command line is an 80-character field that consists of a prompt area, command area and response area.

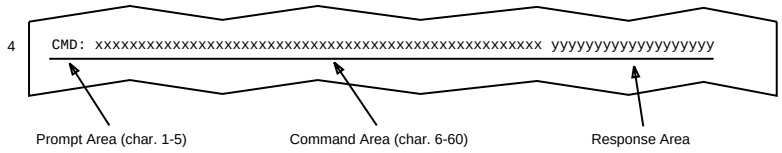


Figure 6. Display Page Command Line Area

5.07 The prompt area of the command line contains the prompt **CMD:** in the first five character positions.

5.08 The command area of the command line is to the right of the prompt area. The command area will accept an input command up to 55 characters long entered by the user. If the user tries to enter more than 55 printable characters, the *4ESS* Switch will cause the MCC terminal to beep (indicating a problem) and will only retain the first 55 characters.

5.09 The response area of the command line is one character position to the right of the **used** command area. This area is used to display system responses to commands entered. The response area is variable and can range from 19 to 55 characters depending upon the portion of the command area used to enter the command.

Application Page Display Area

5.10 The Application Page Display Area (Lines 5-23) of each MCC terminal display page is used to display the various poke commands and indicators associated with each specific display page. Indicators are simply areas of text that change color and/or text content to indicate different switch conditions or events. Poke commands are defined command entries that are initiated by entering a specific code. In addition, the text associated with most of the various poke commands also serves as an indicator by changing colors. **The information contained in the Application Page Display Area is different for each of the MCC terminal display pages**. Therefore, the data contained in this area for the different MCC display pages is described in the "MCC Terminal Display Page — Unique Areas" section of this practice.

Error/Status Message Area

5.11 The Error/Status Message Area (Figure 7) will appear as the last line (Line 24) of each MCC display page. All error and status messages from the remote maintenance system will be received on this single 80-character line. Multi-line output from the remote maintenance system to the MCC display page error/status message area will not cause the message area to scroll upward. Instead, each new line will simply overwrite the previous line.

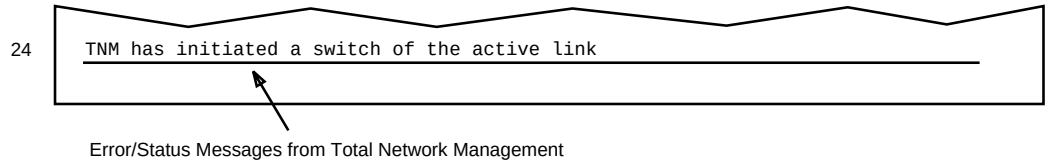


Figure 7. Display Page Error/Status Message Area

6. MCC Terminal Display Page — Unique Areas

6.01 As described in the previous section, each MCC terminal display page has an Application Page Display Area which displays the various poke commands and indicators that are unique to that page. This section provides a detailed description of the poke commands and indicators that are specific to each display page. The following display pages are described:

- Page Index (Page 100)
- Emergency Action Interface (Page EAI)
- MUP Status and Control (Page 106)
- System Status (Page 108)
- Program Store Status and Control (Page 109)
- Call Store Status and Control (Page 110)
- IFB Clients Status and Control (Page 111)
- 1B Processor Status (Page 118)
- DDI Key Options (Page 119)
- Data Display (Page 120)
- Dead Start (Page 1990).

Page Index (Page 100)

6.02 The Page Index (Page 100) lists all accessible pages and identifies the associated poke commands/**EA DISP** key required to select the applicable page. The page index (Figure 8) is invoked by entering Poke Command 100.

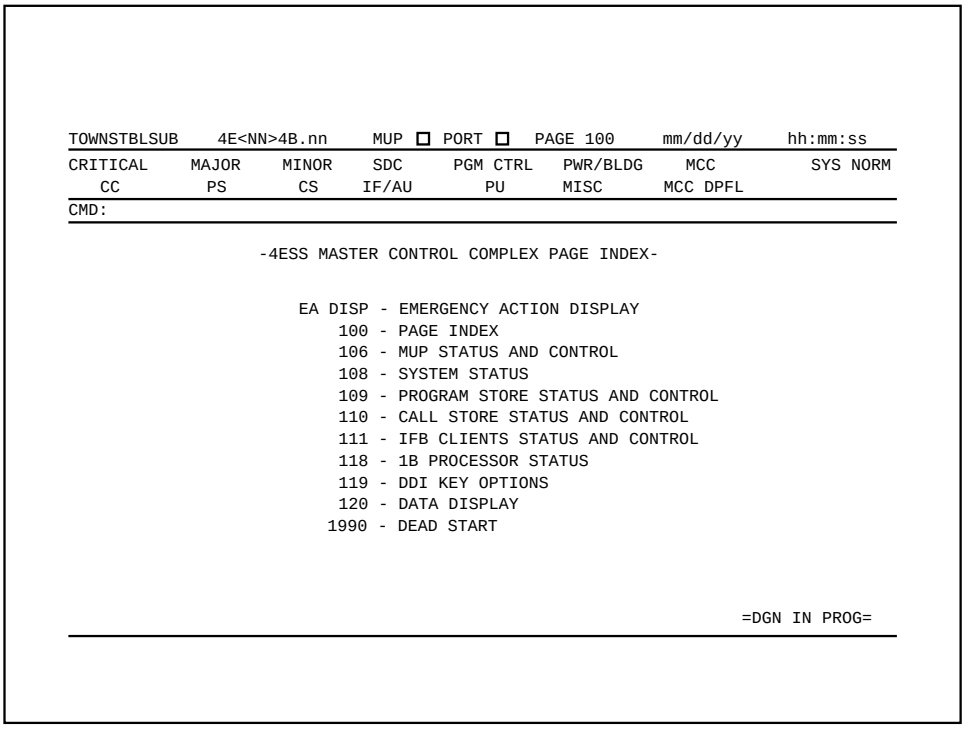


Figure 8. Page Index (Page 100)

6.03 The Page Index (Page 100) lists all MCC display page names and associated poke commands used to access the pages.

A. Page 100 — Indicators

6.04 Table F identifies the indicators associated with Page 100. All Page 100 indicators, except the DGN IN PROG indicator, will appear white on black when there are no alarms on the referenced page. All page 100 indicators will display the highest level alarm if there are alarms on the referenced page. Normally, the DGN IN PROG indicator will not appear. However, when any system unit is under diagnostic control and diagnostics are in progress, the DGN IN PROG indicator will appear yellow on black.

Table F. Page Index (Page 100) Indicators

4ESS SWITCH MASTER CONTROL COMPLEX PAGE INDEX
EA DISP - EMERGENCY ACTION INTERFACE
100 - PAGE INDEX
106 - MUP STATUS AND CONTROL
108 - SYSTEM STATUS
109 - PROGRAM STORE STATUS AND CONTROL
110 - CALL STORE STATUS AND CONTROL
111 - IFB CLIENTS STATUS AND CONTROL
118 - 1B PROCESSOR STATUS
119 - DDI KEY OPTIONS
120 - DATA DISPLAY
1990 - DEAD START
DGN IN PROG

B. Page 100 — Poke Commands

6.05 The following information describes the function of each Page 100 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels. All Page 100 poke commands are accepted by the *4ESS* Switch even if the Page Index is not displayed.

EA DISP When the **EA DISP** key is depressed or when the control sequence "<ESC>, <SHIFT>, <o>, <p>" is entered, the MCC terminal screen will be cleared and the EAI Page will be displayed.

If the EAI Page is already displayed when the **EA DISP** key is depressed, the screen will be cleared and the EAI Page data will be re-transmitted in its entirety.

NORM DISP When the EAI Page is actively displayed on the MCC terminal screen and the **NORM DISP** key is depressed, the MUP will erase the displayed EAI Page and repaint the screen with the last "normal" (non-EAI) page previously displayed. If there is no previous normal page to be displayed (for example, after power-up) when the **NORM DISP** key is depressed, the MUP will erase and repaint the screen with the Page Index (Page 100).

100 When Poke Command 100 is entered, the screen will be cleared and Page 100 will be displayed.

106 When Poke Command 106 is entered, the screen will be cleared and Page 106 will be displayed.

108 When Poke Command 108 is entered, the screen will be cleared and Page 108 will be displayed.

109 When Poke Command 109 is entered, the screen will be cleared and Page 109 will be displayed.

110 When Poke Command 110 is entered, the screen will be cleared and Page 110 will be displayed.

111 When Poke Command 111 is entered, the screen will be cleared and Page 111 will be displayed.

118 When Poke Command 118 is entered, the screen will be cleared and Page 118 will be displayed.

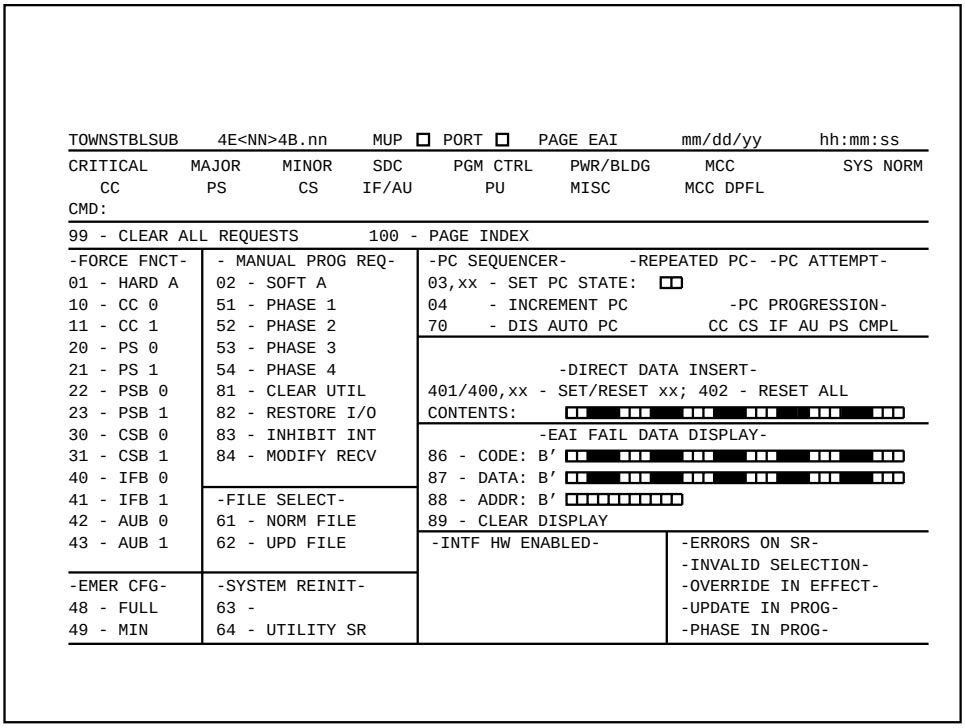
119 When Poke Command 119 is entered, the screen will be cleared and Page 119 will be displayed.

120 When Poke Command 120 is entered, the screen will be cleared and Page 120 will be displayed.

1990 When Poke Command 1990 is entered, the screen will be cleared and Page 1990 will be displayed.

Emergency Action Interface (EAI Page)

6.06 The EAI Page provides access to critical control functions required to perform system recovery actions. The EAI page (Figure 9) is invoked by depressing the **EA DISP** key on the MCC terminal keyboard. The EAI Page is the default page displayed when communication between the MUP and MCC display terminal is initialized.



tpa 786422/01

Figure 9. EAI Page (Page EAI)

6.07 The EAI Page includes the following functional areas:

- FORCE FNCT — Force Functions
- EMER CFG — Emergency Configuration
- MANUAL PROG REQ — Manual Program Request
- FILE SELECT — File Selection
- SYSTEM REINIT — System Reinitialization
- PC SEQUENCER — Processor Configuration Sequencer
- DIRECT DATA INSERT — Direct Data Insert
- EAI FAIL DATA DISPLAY — EAI Failure Data Display
- Various status and alarm indicators.

A. EAI Page — Indicators

6.08 The following information describes the indicators associated with the EAI Page. The text, colors and specific circumstances under which the indicators will change are specified.

HARD A The HARD A indicator is informational text used to identify when hardware A-level interrupt processing is in progress. Normally, the indicator will appear white on black. When selected, the indicator will appear black on purple. The HARD A indicator is affected by Poke Commands 01 and 10 through 43.

SOFT A The SOFT A indicator is informational text associated with Poke Command 02 and will appear white on black.

SET PC STATE
The SET PC STATE indicator is informational text associated with Poke Command 03 and will appear white on black.

PC State Display
The PC State Display is a 2-digit octal display that identifies the Processor Configuration (PC) state count. When the Processor Configuration (PC) state count is zero, no digits will be displayed. When the PC state count is greater than zero, digits will be displayed and the indicator will appear white on red.

INCREMENT PC
The INCREMENT PC indicator is informational text associated with Poke Command 04 and will appear white on black.

FORCE FNCT
The FORCE FNCT indicator is informational text identifying the EAI Page force function area. The indicator will appear yellow on black.

CC 0 The CC 0 indicator is informational text associated with Poke Command 10 and will normally appear white on black. The indicator has eight states. Table G identifies the eight states and their associated colors. The meaning of the columns in Table G are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register
- Active = Force in effect
- Foreground = Foreground color
- Background = Background color.

Table G. CC 0 Indicator States

State	Selected	Set	Active	Foreground	Background
1	No	No	No	White	Black
2	No	Yes	No	Yellow	Red
3	Yes	No	No	Yellow	Red
4	Yes	Yes	No	Purple	White
5	No	No	Yes	Light Blue	Red
6	No	Yes	Yes	Light Blue	Red
7	Yes	No	Yes	Light Blue	Red
8	Yes	Yes	Yes	Black	Purple

When CC 0 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the CC 0 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The CC 0 indicator is affected by Poke Commands 01, 10 and 99.

CC 1

The CC 1 indicator is informational text associated with Poke Command 11 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When CC 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 1 indicator has been selected and Poke Command 01 has been entered and accepted, the CC 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The CC 1 indicator is affected by Poke Commands 01, 11 and 99.

PS 0

The PS 0 indicator is informational text associated with Poke Command 20 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When PS 0 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After PS 0 indicator has been selected and Poke Command 01 has been entered and accepted, the PS 0 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PS 0 indicator is affected by Poke Commands 01, 20 and 99.

PS 1

The PS 1 indicator is informational text associated with Poke Command 21 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When PS 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After PS 1 indicator has been selected and Poke Command 01 has been entered and accepted, the PS 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PS 1 indicator is affected by Poke Commands 01, 21 and 99.

PSB 0

The PSB 0 indicator is informational text associated with Poke Command 22 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When PSB 0 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After PSB 0 indicator has been selected and Poke Command 01 has been entered and accepted, the PSB 0 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PSB 0 indicator is affected by Poke Commands 01, 22 and 99.

PSB 1

The PSB 1 indicator is informational text associated with Poke Command 23 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When PSB 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After PSB 1 indicator has been selected and Poke Command 01 has been entered and accepted, the PSB 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PSB 1 indicator is affected by Poke Commands 01, 23 and 99.

CSB 0

The CSB 0 indicator is informational text associated with Poke Command 30 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When CSB 0 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CSB 0 indicator has been selected and Poke Command 01 has been entered and accepted, the CSB 0 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The CSB 0 indicator is affected by Poke Commands 01, 30 and 99.

CSB 1 The CSB 1 indicator is informational text associated with Poke Command 31 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When CSB 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CSB 1 indicator has been selected and Poke Command 01 has been entered and accepted, the CSB 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The CSB 1 indicator is affected by Poke Commands 01, 31 and 99.

IFB 0 The IFB 0 indicator is informational text associated with Poke Command 40 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When IFB 0 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After IFB 0 indicator has been selected and Poke Command 01 has been entered and accepted, the IFB 0 indicator will transition through the states and remain in state 8 if no hardware problems exist.

If Poke Command 40 (IFB 0) is entered and the forced MUP is not on the selected IFB, the message **FORCED MUP IS NOT ON SELECTED IFB** will be displayed.

The IFB 0 indicator is affected by Poke Commands 01, 40 and 99.

IFB 1 The IFB 1 indicator is informational text associated with Poke Command 41 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When IFB 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After IFB 1 indicator has been selected and Poke Command 01 has been entered and accepted, the IFB 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

If Poke Command 41 (IFB 1) is entered and the forced MUP is not on the selected IFB, the message **FORCED MUP IS NOT ON SELECTED IFB** will be displayed.

The IFB 1 indicator is affected by Poke Commands 01, 41 and 99.

AUB 0 The AUB 0 indicator is informational text associated with Poke Command 42 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When AUB 0 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After AUB 0 indicator has been selected and Poke Command 01 has been entered and accepted, the AUB 0 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The AUB 0 indicator is affected by Poke Commands 01, 42 and 99.

AUB 1 The AUB 1 indicator is informational text associated with Poke Command 43 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator CC 0 (Table G).

When AUB 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After AUB 1 indicator has been selected and Poke Command 01 has been entered and accepted, the AUB 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The AUB 1 indicator is affected by Poke Commands 01, 43 and 99.

EMER CFG The EMER CFG indicator is informational text identifying the EAI Page emergency configuration area. The indicator will appear yellow on black.

FULL The FULL indicator is informational text associated with Poke Command 48 and will normally appear white on black. The indicator has eight states. Table H identifies the eight states and their associated colors. The meanings of the columns in Table H are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register
- Active = Force in effect
- Foreground = Foreground color
- Background = Background color.

Table H. FULL Indicator States

State	Selected	Set	Active	Foreground	Background
1	No	No	No	White	Black
2	No	Yes	No	Yellow	Red
3	Yes	No	No	Yellow	Red
4	Yes	Yes	No	Purple	White
5	No	No	Yes	Black	Green
6	No	Yes	Yes	Light Blue	Red
7	Yes	No	Yes	Light Blue	Red
8	Yes	Yes	Yes	Black	Purple

When FULL indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the FULL indicator will transition through the states and remain in state 8 if no hardware problems exist.

The FULL indicator is affected by Poke Commands 01 and 48.

49 - MIN

The MIN indicator is informational text associated with Poke Command 49 and will normally appear white on black. The indicator has eight states. Table I identifies the eight states and their associated colors. The meanings of the columns in Table I are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register
- Active = Force in effect
- Foreground = Foreground color
- Background = Background color.

Table I. MIN Indicator States

State	Selected	Set	Active	Foreground	Background
1	No	No	No	White	Black
2	No	Yes	No	Yellow	Red
3	Yes	No	No	Yellow	Red
4	Yes	Yes	No	Purple	White
5	No	No	Yes	Black	Green
6	No	Yes	Yes	Light Blue	Red
7	Yes	No	Yes	Light Blue	Red
8	Yes	Yes	Yes	Black	Purple

When MIN indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the MIN indicator will transition through the states and remain in state 8 if no hardware problems exist.

The MIN indicator is affected by Poke Commands 01 and 49.

MANUAL PROG REQ

The MANUAL PROG REQ indicator is informational text identifying the EAI Page manual program request area. The indicator will appear yellow on black.

PHASE 1

The PHASE 1 indicator is informational text associated with Poke Command 51 and will normally appear white on black. The indicator has 8 states. Table J identifies the eight states and their associated colors. The meaning of the columns in Table J are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register
- Active = Force in effect
- Foreground = Foreground color
- Background = Background color.

Table J. PHASE 1 Indicator States

State	Selected	Set	Active	Foreground	Background
1	No	No	No	White	Black
2	No	Yes	No	Yellow	Red
3	Yes	No	No	Yellow	Red
4	Yes	Yes	No	Purple	White
5	No	No	Yes	Black	Purple
6	No	Yes	Yes	Light Blue	Red
7	Yes	No	Yes	Light Blue	Red
8	Yes	Yes	Yes	Black	Purple

When PHASE 1 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the PHASE 1 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PHASE 1 indicator is affected by Poke Commands 01 and 51.

PHASE 2 The PHASE 2 indicator is informational text associated with Poke Command 52 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator PHASE 1 (Table J).

When PHASE 2 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the PHASE 2 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PHASE 2 indicator is affected by Poke Commands 01 and 52.

PHASE 3 The PHASE 3 indicator is informational text associated with Poke Command 53 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator PHASE 1 (Table J).

When PHASE 3 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the PHASE 3 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PHASE 3 indicator is affected by Poke Commands 01 and 53.

PHASE 4 The PHASE 4 indicator is informational text associated with Poke Command 54 and will normally appear white on black. The indicator has eight states. The eight states and their associated colors are identical to indicator PHASE 1 (Table J).

When PHASE 4 indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. After CC 0 indicator has been selected and Poke Command 01 has been entered and accepted, the PHASE 4 indicator will transition through the states and remain in state 8 if no hardware problems exist.

The PHASE 4 indicator is affected by Poke Commands 01 and 52.

FILE SELECT

The FILE SELECT indicator is informational text identifying the EAI Page file selection area. The indicator will appear yellow on black.

NORM FILE The NORM FILE indicator is informational text associated with Poke Command 61 and will normally appear white on black. The indicator has four states. Table K identifies the four states and their associated colors. The meanings of the columns in Table K are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register
- Foreground = Foreground color
- Background = Background color.

Table K. NORM FILE Indicator States

State	Selected	Set	Foreground	Background
1	No	No	White	Black
2	No	Yes	Yellow	Red
3	Yes	No	Yellow	Red
4	Yes	Yes	Purple	White

When NORM FILE indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist.

When NORM FILE indicator is accepted, the indicator specifies that the generic and Office Data Assembler (ODA) are to be read from the normal 1BFILE on the 3B disk.

The NORM FILE indicator is affected by Poke Command 61 and 99.

UPD FILE The UPD FILE indicator is informational text associated with Poke Command 62 and will normally appear white on black. The indicator has four states. The four states and their associated colors are identical to the NORM FILE indicator (Table K).

When UPD FILE indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist.

When UPD FILE indicator is accepted, the indicator specifies that the generic and Office Data Assembler (ODA) are to be read from the update 1BFILE on the 3B disk.

The UPD FILE indicator is affected by Poke Commands 62 and 99.

SYSTEM REINIT

The SYSTEM REINIT indicator is informational text identifying the EAI Page system reinitialization area. The indicator will appear yellow on black.

NORMAL SR The NORMAL SR indicator is not valid with 4E22 and later generics due to the DUS/TUC removal. The NORMAL SR indicator will appear as blank for 4E23 and later generics.

UTILITY SR The UTILITY SR indicator is informational text associated with Poke Command 64 and will normally appear white on black. The indicator has eight states. Table L identifies the eight states and their associated colors. The meanings of the columns in Table L are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Ready = SR source has been enabled.
- Set = Choice selected and acknowledged in CC register
- Foreground = Foreground color
- Background = Background color.

Table L. UTILITY SR Indicator States

State	Selected	Ready	Set	Foreground	Background
1	No	No	No	White	Black
2	No	Yes	No	Black	Green
3	Yes	No	No	Purple	White
4	Yes	Yes	No	Black	Purple
5	No	No	Yes	White	Black
6	No	Yes	Yes	Black	Green
7	Yes	No	Yes	Purple	White
8	Yes	Yes	Yes	Black	Purple

When only the UTILITY SR indicator is selected, the indicator will transition through the first three states and remain in state 3 if no hardware problems exist. When ready, the indicator will remain in state 2. When selected and enabled, the indicator will transition through the states and remain in state 8 if no hardware problems exist.

The UTILITY SR indicator is affected by Poke Commands 64 and 99.

DIS AUTO PC

The DIS AUTO PC indicator is informational text associated with Poke Command 70 and will normally appear white on black. The indicator has four states. Table M identifies the four states and their associated colors. The meanings of the columns in Table M are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register
- Foreground = Foreground color
- Background = Background color.

Table M. DIS AUTO PC Indicator States

State	Selected	Set	Foreground	Background
1	No	No	White	Black
2	No	Yes	Yellow	Red
3	Yes	No	Yellow	Red
4	Yes	Yes	Black	Purple

When DIS AUTO PC is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. If the indicator is selected but not set in hardware, the indicator will reside in state 3. When the indicator is set in hardware but not selected, the indicator will reside in state 2. The DIS AUTO PC indicator is driven by a hardware status bit that is read by the MUP and set via Poke Command 70.

PC SEQUENCER

The PC SEQUENCER indicator is informational text and will normally appear yellow on black.

PC PROGRESSION

The PC PROGRESSION indicator is informational text identifying the EAI Page processor configuration progression area. The indicator will appear white on black.

CC

The CC indicator is informational text identifying the central control status during processor configuration. Normally, the CC indicator will appear white on black. When processor configuration begins and if CC related processor configuration actions are expected to occur, the CC indicator will appear white on red. When CC-related processor configuration actions are completed, the CC indicator will appear white on black.

The CC indicator is affected by Poke Commands 01, 03 and 04.

CS

The CS indicator is informational text identifying the call store status during processor configuration. Normally, the CS indicator will appear white on black. When processor configuration begins and if CS related processor configuration actions are expected to occur, the CS indicator will appear white on red. When CS related processor configuration actions are completed, the CS indicator will appear white on black.

The CS indicator is affected by Poke Commands 01, 03 and 04.

IF

The IF indicator is informational text identifying the Interface Bus (IFB) status during processor configuration. Normally, the IF indicator will appear white on black. When processor configuration begins and if IFB-related processor configuration actions are expected to occur, the IF indicator will appear white on red. When IFB-related processor configuration actions are completed, the IF indicator will appear white on black.

The IF indicator is affected by Poke Commands 01, 03 and 04.

AU The AU indicator is informational text identifying the Auxiliary Unit Bus (AUB) status during processor configuration. Normally, the AU indicator will appear white on black. When processor configuration begins and if AUB related processor configuration actions are expected to occur, the AU indicator will appear white on red. When AUB related processor configuration actions are completed, the AU indicator will appear white on black.

The AU indicator is affected by Poke Commands 01, 03 and 04.

PS The PS indicator is informational text identifying the program store status during processor configuration. Normally, the PS indicator will appear white on black. When processor configuration begins and if PS related processor configuration actions are expected to occur, the PS indicator will appear white on red. When PS related processor configuration actions are completed, the PS indicator will appear white on black.

The PS indicator is affected by Poke Commands 01, 03 and 04.

CMPL The CMPL indicator is informational text identifying the processor configuration completion status. Normally, the CMPL indicator will appear black on green. When processor configuration actions begin, the CMPL indicator will appear white on red. When processor configuration actions are completed, the CMPL indicator will appear black on green.

The CMPL indicator is affected by Poke Commands 01, 03 and 04.

REPEATED PC

The REPEATED PC indicator is informational text identifying a repeating processor configuration condition. Normally, the REPEATED PC indicator will not appear. However, when repeated processor configuration attempts are in progress, the REPEATED PC indicator will appear white on red. The indicator is displayed under hardware control and removed under 1B Processor software control.

PC ATTEMPT

The PC ATTEMPT indicator is informational text identifying a processor configuration attempt. Normally, the PC ATTEMPT indicator does not appear. However, when a processor configuration attempt is in progress, the PC ATTEMPT indicator will appear white on red. The indicator is displayed under hardware control and removed under MUP software control.

DIRECT DATA INSERT

The DIRECT DATA INSERT indicator is informational text identifying the EAI Page direct data insert area. The indicator will appear yellow on black.

SET/RESET The SET/RESET indicator is informational text associated with Poke Command 401/400. The indicator will appear white on black.

RESET ALL The RESET ALL indicator is informational text associated with Poke Command 402. The indicator will appear white on black.

CONTENTS: The CONTENTS: indicator is informational text associated with the direct data insert (DDI) 32-digit display. The indicator will appear white on black.

DDI Display The DDI Display indicator is a 32-digit display. The indicator will appear as triplets of digits, alternating between white on black and yellow on black, with the three rightmost digits appearing white on black. Individual digits in this indicator will change from 0 to 1 when Poke Command 401 is entered or from 1 to 0 when either Poke Command 400 or 402 is entered. If all digits are 0, no digits will be displayed.

CLEAR UTIL The CLEAR UTIL indicator is informational text associated with Poke Command 81 and will normally appear white on black. The indicator has four states. Table N identifies the four states and their associated colors. The meanings of the columns in Table N are as follows:

- State = State number (for reference)
- Selected = User choice accepted by MCC software
- Set = Choice selected and acknowledged in CC register.
- Foreground = Foreground color
- Background = Background color.

Table N. CLEAR UTIL Indicator States

State	Selected	Set	Foreground	Background
1	No	No	White	Black
2	No	Yes	Yellow	Red
3	Yes	No	Yellow	Red
4	Yes	Yes	Purple	White

When CLEAR UTIL indicator is selected, the indicator will transition through the states and remain in state 4 if no hardware problems exist. State 4 will cause the utility function to be cleared when Poke Command 02 is entered. The CLEAR UTIL indicator is affected by Poke Commands 02, 81 and 99.

RESTORE I/O

The RESTORE I/O indicator is informational text associated with Poke Command 82 and will normally appear white on black. The indicator has four states. The four states and their associated colors are identical to the CLEAR UTIL indicator (Table N). When RESTORE I/O indicator is selected, the indicator will appear purple on white indicating that the input/output system is to be restored during A-level processing.

INHIBIT INT The INHIBIT INT indicator is informational text associated with Poke Command 83 and will normally appear white on black. The indicator has four states. The four states and their associated colors are identical to the CLEAR UTIL indicator (Table N). When INHIBIT INT indicator is selected, the indicator will appear purple on white indicating that interrupts during A-level processing are to be inhibited per selected DDI key settings.

MODIFY RECV

The MODIFY RECV indicator is informational text associated with Poke Command 84 and will normally appear white on black. The indicator has four states. The four states and their associated colors are identical to the CLEAR UTIL indicator (Table N). When MODIFY RECV indicator is selected, the indicator will appear purple on white indicating that recovery actions during A-level processing are to be modified per selected DDI key settings.

EAI FAIL DATA DISPLAY

The EAI FAIL DATA DISPLAY indicator is informational text identifying the EAI Page failure data display area. The indicator will appear yellow on black.

CODE: The CODE: indicator is informational text associated with the program code 32-digit display. The CODE: indicator will appear white on black.

A word of program code under processor control during recovery actions will be displayed following the CODE: indicator. No digits will be displayed when any one of the following conditions exist:

(1) Word of program code is all zeroes

(2) CMPL indicator returns to normal

(3) There is no phase in progress.

Entering poke command 89 "CLEAR DISPLAY" will clear the program code information following the CODE: indicator.

There are two parts to the displayed word of program code: a two-character prefix (B', O', D, X' or Blank) followed by a number. The prefix B' indicates that the number will be expressed in binary, O' (octal), D' (decimal), X' (hexadecimal) or blank (ASCII). The indicator will have 10 states, 2 states corresponding to each of the 5 prefixes — states 1 and 2 for binary, 3 and 4 for octal, 5 and 6 for decimal, 7 and 8 for hexadecimal and 9 and 10 for ASCII. The second part of the indicator will be a left-adjusted number identifying the instruction code at the point of failure. In state 1 (binary), the number will be displayed in alternating triplets of white on black and yellow on black digits with the rightmost 3 digits appearing white on black. In state 2 (also binary), the number will be displayed in alternating triplets of yellow on black and white on black digits (the reverse of state 1). In states 3, 5, 7 and 9, the entire indicator will appear white on black and in states 4, 6, 8 and 10, the indicator will appear yellow on black.

The displayed number will be updated as change occurs in the underlying data, but will not be updated more frequently than once every 2 seconds.

Every time the displayed number is changed, the indicator will alternate states. For example, if the indicator is in state 1, it will go to state 2; if in state 2, it will go to state 1; if in state 3, it will go to state 4; if in state 4, it will go to state 3, etc.

This relationship is illustrated as follows:

Old State:	1	2	3	4	5	6	7	8	9	10
New State After Update:	2	1	4	3	6	5	8	7	10	9

DATA: The DATA: indicator is informational text associated with the data word 32-digit display. The DATA: indicator will appear white on black.

A word of data under processor control during recovery actions will be displayed following the DATA: indicator. No digits will be displayed when any one of the following conditions exist:

(1) Word of data is all zeroes

(2) CMPL indicator returns to normal

(3) There is no phase in progress.

Entering poke command 89 "CLEAR DISPLAY" will clear the recovery action data following the DATA: indicator.

There will be two parts to the displayed word of data: a two-character prefix (B', O', D or X') followed by a number. The prefix B' indicates that the number will be expressed in binary, O' (octal), D' (decimal) or X' (hexadecimal). The indicator will have eight states, two states corresponding to each of the four prefixes — states 1 and 2 for binary, 3 and 4 for octal, 5 and 6 for decimal and 7 and 8 for hexadecimal.

The second part of the indicator will be a left-adjusted number identifying the data word. In state 1 (binary), the number will be displayed in alternating triplets of white on black and yellow on black digits with the rightmost three digits appearing white on black. In state 2 (also binary), the number will be displayed in alternating triplets of yellow on black and white on black digits (the reverse of state 1). In states 3, 5 and 7, the entire indicator will appear white on black and in states 4, 6 and 8, the indicator will appear yellow on black.

The displayed number will be updated as change occurs in the underlying data, but will not be updated more frequently than once every 2 seconds.

Every time the displayed number is changed, it will alternate states. For example, if the indicator is in state 1, it will go to state 2; if in state 2, it will go to state 1; if in state 3, it will go to state 4; if in state 4, it will go to state 3, etc.

This relationship is illustrated as follows:

Old State:	1	2	3	4	5	6	7	8
New State After Update:	2	1	4	3	6	5	8	7

ADDR: The ADDR: indicator is informational text associated with the program store word address 32-digit display. The ADDR: indicator will appear white on black.

A program store word address under processor control during recovery actions will be displayed following the ADDR: indicator. No digits will be displayed when any one of the following conditions exist:

(1) Address is all zeroes

(2) CMPL indicator returns to normal

(3) There is no phase in progress.

Entering poke command 89 "CLEAR DISPLAY" will clear the program store word address following the ADDRESS: indicator.

There will be two parts to the displayed address: a two-character prefix (B', O', D or X') followed by a number. The prefix B' indicates that the number will be expressed in binary, O' (octal), D' (decimal) or X' (hexadecimal). The indicator will have eight states, two states corresponding to each of the four prefixes — states 1 and 2 for binary, 3 and 4 for octal, 5 and 6 for decimal and 7 and 8 for hexadecimal.

The second part of the indicator will be a left-adjusted number identifying the program store word address. In state 1 (binary), the number will be displayed in alternating triplets of white on black and yellow on black digits with the rightmost 3 digits appearing white on black. In state 2 (also binary), the number will be displayed in alternating triplets of yellow on black and white on black digits (the reverse of state 1). In states 3, 5 and 7, the entire indicator will appear white on black and in states 4, 6 and 8 the indicator will appear yellow on black.

The number will be updated as change occurs in the underlying data, but will not be updated more frequently than once very two seconds.

Every time the number is changed, it will alternate states. For example, if the indicator is in state 1, it will go to state 2; if in state 2, it will go to state 1; if in state 3, it will go to state 4; if in state 4, it will go to state 3, etc.

This relationship is illustrated as follows:

Old State:	1	2	3	4	5	6	7	8
New State After Update:	2	1	4	3	6	5	8	7

CLEAR DISPLAY

The CLEAR DISPLAY indicator is informational text associated with Poke Command 89 and will normally appear white on black.

INTF HW ENABLED

The INTF HW ENABLED indicator is informational text identifying when the hardware utility interference switch on the 1B Processor has been moved to the enable position. Normally, the indicator will not appear. However, when present, the indicator will appear white on red.

99 - CLEAR ALL REQUESTS

The CLEAR ALL REQUESTS indicator is informational text associated with Poke Command 99 and will normally appear white on black.

ERRORS ON SR

The ERRORS ON SR indicator is informational text identifying when there are errors during system reinitialization. Normally, the indicator will not appear. However, when present, the indicator will appear white on red. The indicator changes state under program control.

INVALID SELECTION

The INVALID SELECTION indicator is informational text identifying when any of the following conditions exist:

- Either Poke Command 01 or Poke Command 02 is entered but a valid processor configuration has not been selected.
- An attempt is made to select both mates of a processor component (for example, both Program Store Buses) when specifying a forced processor configuration.
- An attempt is made to select more than one request from the range of Poke Commands 51 through 54.

Normally, the INVALID SELECTION indicator will not appear. However, when present, the indicator will appear white on red. The indicator will disappear upon entry of the next valid force function (FORCE FNCT) or manual program request (MANUAL PROG REQ) poke command.

OVERRIDE IN EFFECT

The OVERRIDE IN EFFECT indicator is informational text identifying when an override is in effect. The indicator has three states:

(1) State 1 where no text appears

(2) State 2 where the text NO OVERRIDE will appear purple on white

(3) State 3 where the text OVERRIDE IN EFFECT will appear black on purple.

The state of this indicator is related to the state of the force function (FORCE FNCT) indicators.

UPDATE IN PROG

The UPDATE IN PROG indicator is informational text identifying when an update of disk records is in progress. Normally, the UPDATE IN PROG indicator will not appear. However, when present, the indicator will appear black on yellow.

PHASE IN PROG

The PHASE IN PROG indicator is informational text identifying when any software initialization phase is in progress. Normally, the PHASE IN PROG indicator will not appear. However, when present, the

indicator will appear white on red. The indicator will be removed when either the software initialization phase completes or a hardware A-level is entered.

PAGE INDEX The PAGE INDEX indicator is informational text associated with Poke Command 100 and will appear white on black.

B. EAI Page — Poke Commands

6.09 The following information describes the function of each EAI Page poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels.

NOTE:
Poke Commands in the 00 - 99 and 400 series are specific to the EAI page (local commands). Poke Command 100 is a global poke command and can be executed from any page.

01 - HARD A Poke Command 01 will cause a hardware activated A-level interrupt to occur. Poke Command 01 functions as a toggle command, meaning that the configuration will remain in force until Poke Command 01 is entered again to release the force.

If the HARD A indicator is selected and Poke Command 01 is entered to release the force, the HARD A indicator will be retired but A-level interrupt processing will continue.

If the HARD A indicator is not selected, Poke Command 01 will be accepted only if one of the following occurs:

(1) One of the two CCs is selected with no other processor element selected.

(2) A complete processor configuration is selected, consisting of:

- One CC
- One Base Program Store
- One Program Store Bus
- One Call Store Bus
- One Interface Bus
- One Auxiliary Unit Bus.

If the HARD A indicator is not selected, Poke Command 01 is entered and one of the two conditions above is not met, the INVALID SELECTION indicator will appear white on red.

If Poke Command 01 is accepted, the following actions will occur:

(1) The IP (In Progress) acknowledgment will be displayed in the response part of the command line.

(2) The HARD A indicator will appear black on purple identifying the indicator as being selected.

(3) All selected Force Function (FORCE FNCT) indicators (CC, PS, PSB, CSB, IFB and AUB) will be activated.

(4) If processor configuration occurs, the SET PC STATE indicator display will identify the current Processor Configuration (PC) state. If automatic processor configuration is enabled (DIS AUTO PC indicator not selected), the processor configuration state count will be updated every half second.

(5) If processor configuration occurs or if the processor configuration state count exceeds 07, all the PC PROGRESSION indicators (CC, CS, IF, AU, PS and CMPL) will appear white on red. As the activity to which each indicator corresponds is completed, that specific indicator will change back to its normal color.

NOTE:
The first 7 processor configuration states do not involve pump activity that is related to the PC PROGRESSION indicators. Therefore, the PC PROGRESSION indicators will not appear white on red during those 7 states.

(6) All EAI FAIL DATA DISPLAY indicators (CODE:, DATA: and ADDR:) will be cleared.

(7) The OVERRIDE IN EFFECT indicator will appear black on purple.

(8) The PHASE IN PROG indicator will be retired (if present).

(9) If a phase has been selected when the phase activity begins, the corresponding indicator (PHASE 1, PHASE 2, PHASE 3 or PHASE 4) will progress from the selected state (purple on white) to the active state (black on purple). When the phase activity completes, the corresponding phase indicator will return to the normal state (white on black).

(10) If a phase has been selected, any of the following indicators that are also selected will be activated:

— FULL

— MIN

— MODIFY RECV

(11) As recovery actions progress, the CC will read the status of each Force Function (FORCE FNCT) indicator, each Manual Program Request (MANUAL PROG REQ) indicator and each DDI key at the time the status of the indicator or key is required. The CC will not "latch" all indicators or keys at the beginning of the recovery process.

02 - SOFT A Poke Command 02 activates a previously requested Manual Program Request (MANUAL PROG REQ) software action. Poke Command 02 will cause the IP (In Progress) acknowledgment to be displayed in the response part of the command line.

03 - SET PC STATE

Poke Command 03 will be rejected when either of the following conditions are true:

(1) If no parameter is provided or if the parameter is an invalid processor configuration state

(2) If automatic processor configuration is enabled.

Poke Command 03 will cause the following actions to occur:

(1) The IP (In Progress) acknowledgment will be displayed in the response part of the command line.

(2) The processor configuration counter will be set to the state specified by the parameter.

(3) The SET PC STATE indicator display will identify the state specified by the parameter.

(4) One of two messages or no message will appear in the Summary Status Area of the MCC page currently displayed:

(1) The =IN PROGRESS= message will appear yellow on black when a processor configuration request is in progress.

(2) The =PC FAILED= message will appear white on red when a processor configuration request has failed to achieve the target PC state.

(3) If no message appears, one of the following has occurred:

(a) Poke Command 03 has completed successfully and there is currently no activity

(b) Poke Command 03 has failed and another poke command has subsequently been entered.

(5) If the SET PC STATE indicator display count is greater than 07, the following actions will occur:

(a) All EAI FAIL DATA DISPLAY indicators (CODE:, DATA: and ADDR:) will be cleared. If the processor configuration fails, the EAI FAIL DATA DISPLAY indicators will be displayed as necessary.

(b) The PHASE IN PROG indicator will be retired (if present)

(c) Any one of the phase indicators (PHASE 1, PHASE 2, PHASE 3 or PHASE 4) which is active will be retired.

(d) The PC PROGRESSION indicators (CC, CS, IF, AU, PS and CMPL) that are affected by the specified state will appear white on red. As the activity to which each indicator corresponds is completed, the indicator will change back to its normal color.

(6) The OVERRIDE indicator will not change.

04 - INCREMENT PC

Poke Command 04 will increment the processor configuration state counter by one during manual sequencing. The poke command will be rejected if the DIS AUTO PC indicator does not appear black on purple (automatic processor configuration enabled).

Poke Command 04 will cause the same actions to occur as Poke Command 03 except the processor configuration counter will be incremented by one.

Each subsequent entry of Poke Command 04 will increment the processor configuration counter by one.

10 - CC 0 Poke Command 10 will select CC 0 for inclusion in a forced configuration or release it if it has already been selected.

If neither CC 0 nor CC 1 has been selected, Poke Command 10 will be accepted and the following actions will occur:

- CC 0 will be selected.
- The INVALID SELECTION indicator will be removed (if present).
- The NO OVERRIDE indicator will be displayed.

If CC 0 is already active, Poke Command 10 will cause the following actions to occur:

- All active force function (FORCE FNCT) indicators (CC, PS, PSB, CSB, IFB and AUB) will return to the selected state.
- The HARD A indicator will return to the normal state.
- A-level processing will continue.

  If A-level processing has proceeded far enough to force CC 0, CC 0 will be configured by force. If A-level processing has not proceeded far enough to force CC 0, the default CC will be configured.

If A-level processing has proceeded far enough to force any other selected processor elements, that element will be configured by force. If A-level processing has not gone far enough to force any other selected processor elements, the default processor elements will be configured.

- The INVALID SELECTION indicator will be removed (if present).
- The NO OVERRIDE indicator will be displayed.

If CC 1 has already been selected (or is now active), Poke Command 10 will be rejected and the INVALID SELECTION indicator will appear.

NOTE:
A selected indicator goes "active" when Poke Command 01 is entered. Force functions are acted upon relatively early in the boot process, so it is virtually impossible to "release" a force and actually cause a default configuration.

11 - CC 1 Poke Command 11 will perform the same functions for CC 1 that Poke Command 10 performs for CC 0. The same criteria for accepting and rejecting Poke Command 10 will apply to Poke Command 11.

20... Unit 0 The title 20...Unit 0 is intended to cover all even-numbered force function (FORCE FNCT) poke commands greater than 10.

Poke Commands 20, 22, 30, 40 and 42 will perform the same functions for PS 0, PSB 0, CSB 0, IFB 0 and AUB 0, respectively, as Poke Command 10 performs for CC 0. The same criteria for accepting and rejecting Poke Command 10 will apply to these poke commands with two exceptions:

(1) Unit 0 of the corresponding PS, PSB, CSB, IFB and AUB indicator will replace the role of the CC 0 indicator.

(2) If A-level activity is in progress with only a CC forced, the following actions will occur:

— Poke commands will be rejected
— Corresponding indicators will remain normal
— The INVALID SELECTION indicator will appear
— The OVERRIDE IN EFFECT indicator will remain lighted.

21... Unit 1 The title 21...Unit 1 is intended to cover all odd-numbered force function (FORCE FNCT) poke commands greater than 11.

Poke Commands 21, 23, 31, 41 and 43 will perform the same functions for PS 1, PSB 1, CSB 1, IFB 1 and AUB 1, respectively, as Poke Command 11 performs for CC 1. The same criteria for accepting and rejecting Poke Command 11 will apply to these poke commands with two exceptions:

(1) Unit 1 of the corresponding PS, PSB, CSB, IFB and AUB indicator will replace the role of the CC 1 indicator.

(2) If A-level activity is in progress with only a CC forced, the following actions will occur:

- Poke commands will be rejected
- Corresponding indicators will remain normal
- The INVALID SELECTION indicator will appear
- The OVERRIDE IN EFFECT indicator will remain lighted.

48 - FULL Poke Command 48 selects the full configuration option during emergency mode recovery. If the minimum configuration option has already been selected, Poke Command 48 will be rejected. Otherwise, Poke Command 48 will be accepted. If the full configuration option is already selected, Poke Command 48 will cause the full configuration option to be released. If the full configuration option is not already selected, Poke Command 48 will cause the full configuration option to be selected.

49 - MIN Poke Command 49 selects the minimum configuration option during emergency mode recovery. If the full configuration option has already been selected, Poke Command 49 will be rejected. Otherwise, Poke Command 49 will be accepted. If the minimum configuration option is already selected, Poke Command 49 will cause the minimum configuration option to be released. If the minimum configuration option is not already selected, Poke Command 49 will cause the minimum configuration option to be selected.

51 - PHASE 1 If no phase indicator (PHASE 1, PHASE 2, PHASE 3 or PHASE 4) is selected, Poke Command 51 will be accepted and the PHASE 1 indicator will be selected. If PHASE 1 has been selected, Poke Command 51 will be accepted and the PHASE 1 indicator will be retired. When Poke Command 51 is accepted, the INVALID SELECTION indicator will be removed (if present).

If any other phase indicator has been selected, Poke Command 51 will be rejected and the INVALID SELECTION indicator will be displayed.

52 - PHASE 2, 53 - PHASE 3, 54 - PHASE 4

Poke Commands 52 (Phase 2), 53 (Phase 3) and 54 (Phase 4) requests the indicated phase and will have the same effect on their respective indicators and other associated indicators as Poke Command 51 has on its indicators.

61 - NORM FILE

Poke Command 61 specifies that memory be pumped from the normal 1BFILE during recovery. If neither the UPD FILE or NORM FILE indicator has been selected, Poke Command 61 will be accepted and the INVALID SELECTION indicator will be removed (if present). If the NORM FILE indicator has been selected, Poke Command 61 will cause the indicator to retire. If the UPD FILE indicator has been selected, Poke Command 61 will be rejected and the INVALID SELECTION indicator will appear.

62 - UPD FILE

Poke Command 62 specifies that memory be pumped from the update 1BFILE during recovery. If neither the NORM FILE or UPD FILE indicator has been selected, Poke Command 62 will be accepted and the INVALID SELECTION indicator will be removed (if present). If the UPD FILE indicator has been selected, Poke Command 62 will cause the indicator to retire. If the NORM FILE indicator has been selected, Poke Command 62 will be rejected and the INVALID SELECTION indicator will appear.

63 - Poke Command 63 is not a valid poke command in 4E22 and later generics due to the DUS/TUC removal. A response of "NG" is given if poke command 63 is entered. A blank will replace the NORMAL SR indicator associated with poke command 63 under normal conditions. The NORMAL SR indicator may reappear during recovery or booting.

64 - UTILITY SR

Poke Command 64 causes system reinitialization to use the generic and ODA read. If UTILITY SR indicator has not been selected, Poke Command 64 will be accepted and the INVALID SELECTION indicator will be removed (if present). If the UTILITY SR indicator has been selected, Poke Command 64 will cause the indicator to retire.

70 - DIS AUTO PC

Poke Command 70 enables and disables automatic processor configuration during system recovery. If the DIS AUTO PC indicator is white on black, Poke Command 70 will cause the indicator to appear black on purple indicating that automatic processor configuration is disabled. If the DIS AUTO PC indicator is black on purple, Poke Command 70 will cause the indicator to appear white on black indicating that automatic processor configuration is enabled.

When Poke Command 70 is accepted, the PC-ATTEMPT indicator will be removed (if present).

81 - CLEAR UTIL

Poke Command 81 requests that active utility functions be cleared during A-level activity. If the CLEAR UTIL indicator has not been selected, Poke Command 81 will cause the indicator to be selected. If the CLEAR UTIL indicator has been selected, Poke Command 81 will cause the indicator to retire.

82 - RESTORE I/O

Poke Command 82 requests the unconditional restoration of maintenance related input/output channels during A-level activity. If the RESTORE I/O indicator has not been selected, Poke Command 82 will cause the indicator to be selected. If RESTORE I/O indicator has been selected, Poke Command 82 will cause the indicator to retire.

83 - INHIBIT INT

Poke Command 83, in conjunction with the DDI key options selected on MCC Page 119, causes specific maintenance interrupts to be inhibited during recovery actions. If the INHIBIT INT and MODIFY RECV indicators have not been selected, Poke Command 83 will cause the indicator to be selected. If the MODIFY RECV indicator is selected, Poke Command 83 should not be selected. If the INHIBIT INT indicator has been selected, Poke Command 83 will cause the indicator to retire.

84 - MODIFY RECV

Poke Command 84, in conjunction with the DDI key options selected on MCC Page 119, causes modified recovery action during all software initialization phases, during manual processor configuration or during System Reinitialization.

If the MODIFY RECV and INHIBIT INT indicators have not been selected, Poke Command 84 will cause the indicators to be selected. If the INHIBIT INT indicator is selected, Poke Command 84 should not be selected. If the MODIFY RECV indicator has been selected, Poke Command 84 will cause the indicator to retire.

86 - CODE Poke Command 86 causes the number base of the CODE: indicator to cycle between binary, octal, decimal, hexadecimal and ASCII. The default setting will be octal.

87 - DATA Poke Command 87 causes the number base of the DATA: indicator to cycle between binary, octal, decimal and hexadecimal. The default setting will be octal.

88 - ADDR Poke Command 88 causes the number base of the ADDR: indicator to cycle between binary, octal, decimal and hexadecimal. The default setting will be octal.

89 - CLEAR Poke Command 89 causes the EAI FAIL DATA DISPLAY indicator displays (CODE:, DATA: and ADDR:) to be cleared.

99 - CLEAR ALL REQUESTS

Poke Command 99 clears all selected requests associated with the force function (FORCE FNCT) and manual program request (MANUAL PROG REQ) functional areas. Poke Command 99 will not clear activated overrides (forces). Only selected indicators associated with the identified functional areas will be cleared. Clearing a request means setting the indicator to its default state.

The processor "reads" selected force function (FORCE FNCT) indicators and selected manual program request (MANUAL PROG REQ) indicators in the midst of recovery rather than at the beginning of recovery. As a result, poke commands that are entered during recovery actions *may* affect recovery. Therefore, the wisest course of action may be to avoid any MCC activity until recovery either fails or succeeds.

Requests will be cleared without reference to whether they have been acted upon. For example, if Poke Command 81 (CLEAR UTIL) is entered before Poke Command 01 (HARD A) and Poke Command 99 (CLEAR ALL REQUESTS) is entered immediately *after* Poke Command 01, the utility system may or may not get cleared (Poke Command 81 action) but the CLEAR UTIL indicator will return to normal.

100 - PAGE INDEX

Poke Command 100 causes the screen to be cleared and the Page Index to be displayed.

401,xx,xx,... SET xx

Poke Command 401 sets one or more bits in the DDI register associated with specified DDI keys. Optional inputs to Poke Command 401 must conform to the following:

- Up to 16 two-digit option values can be entered as long as each option value is followed by a comma, for example, **401,10,03,14**.
- All options must be two digits. Otherwise, the command will be rejected.
- All options must be in the range 00 through 31. Otherwise, the command will be rejected.

If Poke Command 401 is rejected for any reason, no DDI keys will be set.

400,xx,xx,... RESET xx

Poke Command 400 clears one or more bits in the DDI register associated with specified DDI keys. The criteria for accepting or rejecting Poke Command 400 is the same as previously described for Poke Command 401.

If Poke Command 401 is rejected, no DDI keys will be reset.

402 - RESET ALL

Poke Command 402 causes all 32 bits in the DDI register to be reset.

MUP Status and Control (Page 106)

6.10 The MUP Status and Control Page (Page 106) provides specific control and status information associated with the MUP. Page 106 (Figure 10) is invoked by entering Poke Command 106.

6.11 The MUP Status and Control Page includes the following functional areas:

- Common Control
- Unique Control
- Utility Access System Mode (UAS MODE)
- Various MUP status and control indicators/alarms.

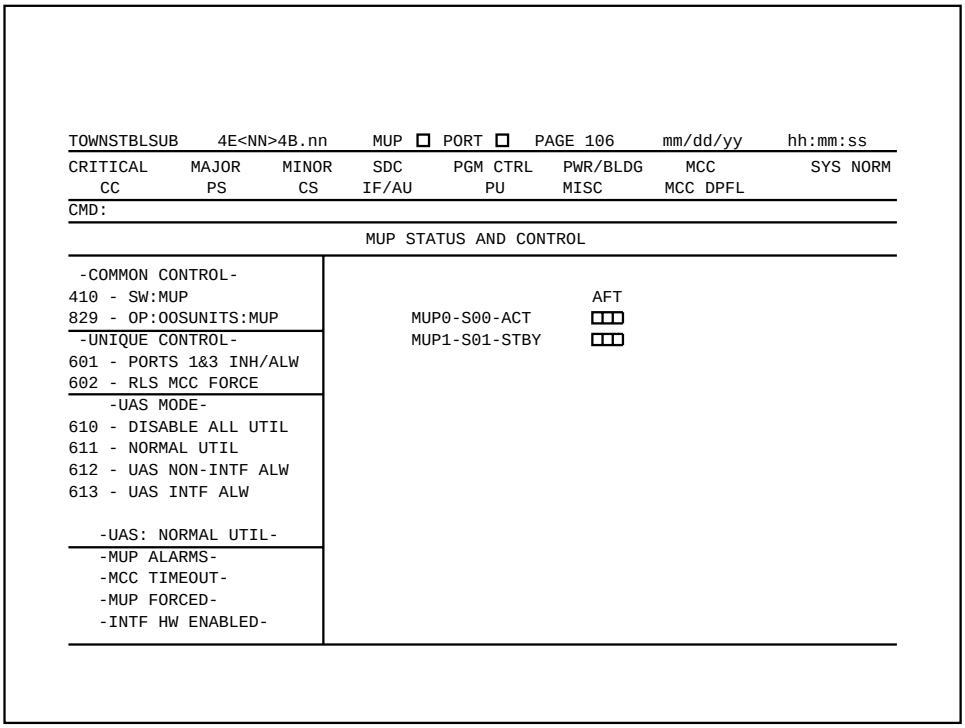


Figure 10. MUP Status and Control Page (Page 106)

NOTE:
The digits of a numerical variable on the MCC display pages are represented by a square (□).

A. Page 106 — Indicators

6.12 The following information describes the indicators associated with Page 106. The text, colors and specific circumstances under which the indicators will change are specified.

MUP STATUS AND CONTROL
The MUP STATUS AND CONTROL indicator is informational text identifying Page 106 and will appear white on black.

COMMON CONTROL
The COMMON CONTROL indicator is informational text identifying the common control area of Page 106 and will appear white on black.

AFT The AFT indicator is informational text identifying MUP status. The indicator that will appear white on black. The characters AFT stand for the following:

A = Active
F = Force
T = Trouble.

MUP0-S00-status and **MUP1-S01-status**
These indicators identify the status of MCC Utility Processors 0 and 1. The MUP0/MUP1 designations identify the associated MUP and the S00/S01 designations identify the IFB slot number associated with MUP 0 and MUP 1, respectively. The MUP status is identified using test phrases and colors. The text phrases and associated colors are as follows:

- ACT (Active) - Black on green
- STBY (Standby) - White on blue
- OOS (Out-of-service) - Black on red
- UNK (Unknown) - Red on yellow.

AFT The AFT indicator is informational text identifying the Active (A), Forced (F) and Trouble bits associated with MUP 0 and MUP 1. The indicator will appear white on black.

AFT Bit Display
The MUP 0 and MUP 1 AFT bit display is a 3-character display that identifies the AFT bits. The A (Active), F (Force) and T (Trouble) bits are single-digit values which are set under 1B Processor hardware control. When a MUP is OOS or STBY, the F and T bits are not displayed.

A bit value of 1 indicates that the function is selected and a value of 0 indicates that the function is not selected. Therefore:

- If A is equal to 1, the associated MUP (0/1) is active.
- If T is equal to 1, the associated MUP (0/1) has trouble.
- If F is equal to 1, the associated MUP (0/1) is forced.

The colors associated with the AFT display bits are identical to the MUP0-S00-*status* and MUP1-S01-*status* indicators.

SW:MUP The SW:MUP indicator is informational text associated with Poke Command 410 and will appear white on black.

OP:OOSUNITS;MUP

The OP:OOSUNITS;MUP indicator is informational text associated with Poke Command 829. Normally, the indicator will appear white on black. However, the indicator will appear white on red if either of the following conditions exist:

— A MUP is out-of-service

— An MCC timeout has occurred.

UNIQUE CONTROL

The UNIQUE CONTROL indicator is informational text identifying the unique control area of Page 106. The indicator will appear white on black.

PORTS 1&3 INH/ALW

The PORTS 1&3 INH/ALW indicator is informational text associated with Poke Command 601 used to identify the state of Ports 1 and 3 (released/inhibited). Normally, the indicator will appear white on black indicating Ports 1 and 3 are released. However, when Ports 1 and 3 are inhibited, the indicator will appear white on red.

RLS MCC FORCE

The RLS MCC FORCE indicator is informational text associated with Poke Command 602 used to identify if an MCC force is in effect. If the MUP is not forced, the indicator will appear white on black. If the MUP is forced, the indicator will appear black on purple.

The RLS MCC FORCE indicator is also affected by the "<ESC>, <CNTL>, <x>" sequence which causes an unconditional MUP switch.

UAS MODE The UAS MODE indicator is informational text identifying the utility access system mode area of Page 106. The indicator will appear white on black.

DISABLE ALL UTIL

The DISABLE ALL UTIL indicator is informational text associated with Poke Command 610 used to disable all utilities. The indicator will appear white on black.

NORMAL UTIL

The NORMAL UTIL indicator is informational text associated with Poke Command 611 used to specify normal utilities. The indicator will appear white on black.

UAS NON-INTF ALW

The UAS NON-INTF ALW indicator is informational text associated with Poke Command 612. The indicator will appear white on black.

UAS INTF ALW

The UAS INTF ALW indicator is informational text associated with Poke Command 613. The indicator will appear white on black.

MUP ALARMS

The MUP ALARMS indicator is informational text identifying the MUP alarm area of Page 106. The indicator will appear white on black.

MCC TIMEOUT

The MCC TIMEOUT indicator identifies that an MCC timeout has occurred while waiting for input from the central control. Normally, the indicator will not appear. However, when an MCC timeout has occurred, the indicator will appear white on red. The indicator is identical to the MCC TIMEOUT indicator on Page 108.

MUP FORCED

The MUP FORCED indicator identifies when a MUP force is in effect. Normally, the indicator will not appear. However, when a MUP is forced, the indicator will appear black on purple.

INTF HW ENABLED

The INTF HW ENABLED indicator identifies when the 1B Processor utility interference switch has been moved to the enable position. Normally, the indicator will not appear. However, when the utility interference switch has been moved to the enable position (a major alarm condition), the indicator will appear white on red. The MCC indicator in the Summary Status Area of any MCC page will also appear white on red when the 1B Processor utility interference switch is in the enable position.

B. Page 106 — Poke Commands

6.13 The following information describes the function of each Page 106 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels.

NOTE:
Poke Commands in the 400 series are specific to Page 106 (local commands). Poke Commands in the 600 and 800 series are global poke commands and can be executed from any page.

410 SW:MUP Poke Command 410 will cause a software switch of the active and standby MCCs. The poke command will be rejected if an MCC force is in effect (RLS MCC FORCE indicator appears black on purple). When Poke Command 410 is accepted, the following actions will occur:

(1) A PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

(2) All active MCC options and configurations are transferred to the standby MCC. However, inhibited ports will not be released.

(3) The active MCC will be made standby and the original standby MCC will be made active.

(4) The current screen being displayed will be cleared and repainted on MCC associated with the port where Poke Command 410 was entered. No change will be made to the MCC screens associated with other ports.

(5) An output message is sent to the MTC I/O channel indicating the following:

— Status of software MCC switch (passed or failed)
— Time and date of MCC switch
— When applicable, text indicating that the switch will not complete due to some problem. Consult the *4ESS* Switch I/O message manuals for explanation of problem.

829 - OP:OOSUNITS;MUP
Poke Command 829 causes an output listing of all out-of-service MUPs to be printed at the MTC channel. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line when a successful request has been completed.

601 - PORTS 1&3 INHIBIT/ALLOW
Poke Command 601 toggles the inhibit/allow mode for MCC Ports 1 and 3. Poke Command 601 will be rejected if the command is entered from either Port 1 or Port 3.

If Ports 1 and 3 are inhibited as a result of Poke Command 601, all poke commands received over Ports 1 and 3 will be rejected with the exception of the global Poke Commands 100, 106, 108, 118, 119, 120, 1990, EA DISP and NORM DISP. Escape/control sequences "<ESC>, <CTRL>, <x>" (Force MUP Switch) and "<ESC>, <CTRL>, <r>" (MUP Software Reset) will also be accepted.

The inhibition of Ports 1 and 3 will be released automatically when one of the following occurs:

- Ports 0 and 2 time out while operating in the Virtual Terminal Protocol (VTP) mode.
- Data Terminal Ready (DTR) is lost on Ports 0 and 2.
- A MUP software reset control sequence "<ESC>, <CNTL>, <r>" is issued.

602 - RLS MCC FORCE

Poke Command 602 will release an MCC force. If there is no MCC force, Poke Command 602 will be rejected. If an MCC force *is* in effect, Poke Command 602 will cause the following actions to occur:

(1) A PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

(2) The MCC force will be released.

(3) The RLS MCC FORCE indicator will appear white on black.

Poke Command 602 will *not* cause a switch of the active MCC. Poke Command 602 will only release the MCC force thus allowing a subsequent software switch to be made.

610-613 *UAS Pokes*

The Poke Commands 610-613 allow the user to choose among four manually selectable Utility Access System (UAS) modes. Poke Commands 610-613 are described in Table O.

Table O. UAS Mode Poke Commands

Poke	Text	Function
610	**610 - DISABLE ALL UTIL**	Disable all utility functions
611	**611 - NORMAL UTIL**	Return to normal utilities (release craft override)
612	**612 - UAS NON-INTF ALW**	Allow all non-interfering functions
613	**613 - UAS INTF ALW**	Allow interfering functions

It is not possible to successfully enter Poke Commands 610-612 while the 1B Processor is performing interfering actions. Interfering actions include:

(1) Suspending the processor (Poke Command 701)

(2) Automatic Hard A generation

(3) BOL/BOR Lock

(4) Executing test Poke Command 740 or 741.

If Poke Commands 610-612 are entered while interfering actions are in progress, the poke command will be rejected with the following messages:

(1) NG, CC IS HALTED

(2) NG, HARD-A IN PROG

(3) NG, BOL/BOR LOCKED

(4) NG, BOOT ROM TEST IP.

Poke Command 613 allows entry into modes where UAS operation could interfere with the operation of the 1B Processor. Poke Command 613 will not be accepted unless the 1B Processor utility interference switch has been moved from the "inhibit" to the "allow" position. In addition, if the utility interference switch is moved to "inhibit" while the MUP is in the UAS interfering mode (Poke Command 613 active), the MUP will revert to the UAS non-interfering mode.

Poke Commands 610-613 allow the MCC user to select the level of utilities to be allowed. Poke Commands 610-613 text appears white on black. After Poke Commands 610, 611 and 612 are successfully entered, an OK acknowledgment will be displayed in the response part of the the command line. In order for Poke Command 613 to be entered successfully, the 1B Processor utility interference switch must be moved from the "inhibit" to the "allow" position. If Poke Command 613 is entered while the utility interference switch is in the "inhibit" position, the poke commands will be rejected and an NG (No Good) acknowledgment will be displayed in the response part of the command line. If Poke Command 613 is successfully entered while the utility interference switch is in the "allow" position, an OK acknowledgment will be displayed in the response part of the command line.

System Status (Page 108)

6.14 The System Status Page (Page 108) provides *4ESS* Switch status, alarm and hardware equipment status information. Page 108 is invoked by entering Poke Command 108.

6.15 The System Status Page (Figure 11) includes the following functional sections:

- System Activity
- System Status
- System Controls
- Processor Equipment Status
- Peripheral Equipment Status
- Various system status indicators/alarms.

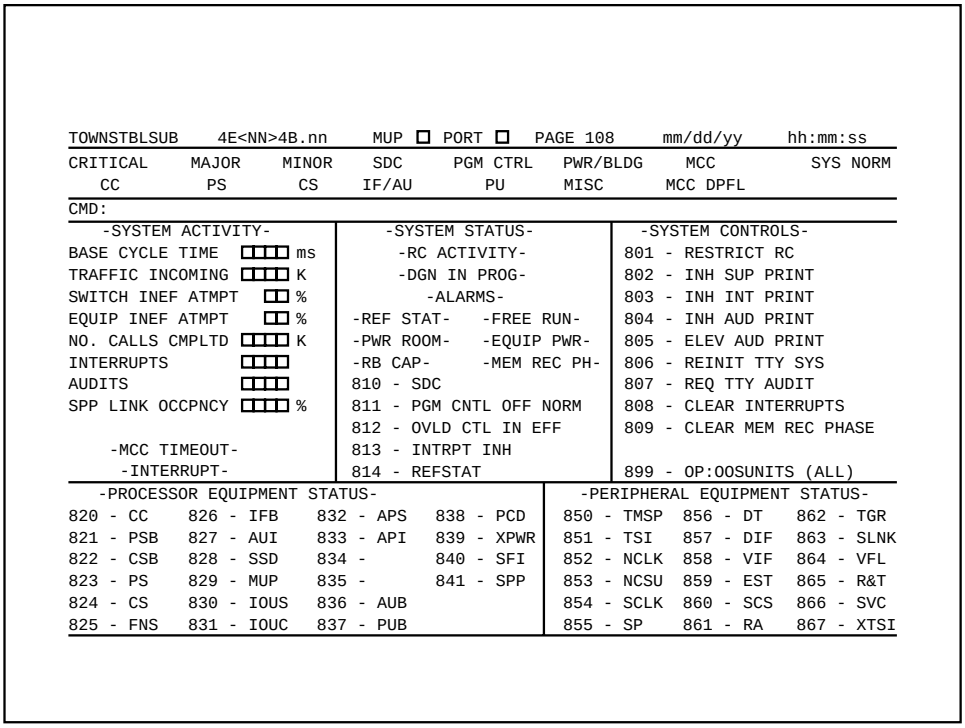


Figure 11. System Status Page (Page 108)

NOTE:
The digits of a numerical variable on the MCC display pages are represented by a square (□).

A. Page 108 — Indicators

6.16 The following information describes the indicators associated with Page 108. The text, colors and specific circumstances under which the indicators will change are specified. Page 108 indicators are updated via CC software.

SYSTEM ACTIVITY

The SYSTEM ACTIVITY indicator is informational text identifying the system activity area of Page 108. The indicator will appear white on black.

BASE CYCLE TIME

The BASE CYCLE TIME indicator is informational text identifying the base cycle time display and will appear white on black.

BASE CYCLE TIME digits

The base cycle time display consists of 4 digits and will appear white on black. The four digits indicate the average duration of the base level cycle in milliseconds (ms). The indicator is updated every 10 seconds.

TRAFFIC INCOMING

The TRAFFIC INCOMING indicator is informational text identifying the incoming traffic display and will appear white on black.

TRAFFIC INCOMING digits

The incoming traffic display consists of 4 digits and will appear white on black. The four digits indicate the total number of 1,000 (K) call attempts on all trunks, regardless of signaling characteristics including CCIS CR queue abandons and overflows. The display is updated every minute and indicates a normalized hourly figure (that is, the last minute multiplied by 60).

SWITCH INEF ATMPT

The SWITCH INEF ATMPT indicator is informational text identifying the switch ineffective attempts display and will appear white on black.

SWITCH INEF ATMPT digits

The switch ineffective attempts display consists of 2 digits and will appear white on black. The two digits provide a visual indication of switching ineffectiveness. It shows the ratio (%) of nonswitched calls to the number of call attempts during the past 60 seconds. The display is updated every minute.

NOTE:

Nonswitched is defined as the sum of nonequipment and equipment-related failed call attempts, excluding Centralized Automatic Message Accounting (CAMA) automatic office and automatic identification failures.

EQUIP INEF ATMPT

The EQUIP INEF ATMPT indicator is informational text identifying the equipment ineffective attempts display and will appear white on black.

EQUIP INEF ATMPT digits

The equipment ineffective attempts display consists of two digits and will appear white on black. The display shows the ratio (%) of equipment-related ineffective attempts to traffic-related ineffective attempts during the past 60 seconds. The display will be updated every minute.

NO. CALLS CMPLTD

The NO. CALLS CMPLTD indicator is informational text identifying the number of calls completed display and will appear white on black.

NO. CALLS CMPLTD digits
The number of calls completed display consists of four digits and will appear white on black. The display is based on the total number of 1,000 (K) calls for which answer supervision has been received. The display will be updated every minute and indicates a normalized hourly figure (last minute multiplied by 60).

INTERRUPTS The INTERRUPTS indicator is informational text identifying the interrupts display and will appear white on black.

INTERRUPTS digits
The interrupts display consists of four digits and will appear white on black. The display identifies the total number of interrupts generated during the 10 seconds prior to the last update. The display is updated every 10 seconds.

AUDITS The AUDITS indicator is informational text identifying the audits display and will appear white on black.

AUDITS display The audits display consists of four digits and will appear white on black. The display identifies the total number of audits generated (including those not printed) during the 10 seconds prior to the last update. The display is updated every 10 seconds.

SPP LINK OCCPNCY
The SPP LINK OCCPNCY indicator is not operational at this time.

SPP LINK OCCPNCY display
The SPP LINK OCCPNCY display is not operational at this time.

MCC TIMEOUT The MCC TIMEOUT indicator identifies when an MCC timeout has occurred while waiting for input from the central control. This is a major alarm condition. Normally, the indicator will not appear. When a timeout occurs, the indicator will appear white on red.

INTERRUPT The INTERRUPT indicator identifies when a maintenance interrupt (A thru F) has occurred. This is a major alarm condition. Normally, the indicator will not appear. However, when an interrupt occurs, the indicator will appear white on red. The indicator is affected by Poke Command 808.

SYSTEM STATUS
The SYSTEM STATUS indicator is informational text identifying the system status area of Page 108. The indicator will appear white on black.

RC ACTIVITY The RC ACTIVITY indicator is informational text identifying when recent change activity is in effect. Normally, the indicator will not appear. However, when recent change activity is in effect, the indicator will appear yellow on black.

DGN IN PROG The DGN IN PROG indicator is informational text identifying when any system unit is under diagnostic control. Normally, the indicator will not appear. However, when diagnostics are in progress, the indicator will appear yellow on black.

ALARMS The ALARMS indicator is informational text identifying the alarm area of Page 108. The indicator will appear white on black.

REF STAT The REF STAT indicator is informational text identifying when there is an outage on either Network Clock Synchronization Unit (NCSU) reference signal (DS1A or DS1B) or when the alternate reference

signal is being used as the active reference. Normally, the indicator will not appear. However, when either of the above stated conditions exist, the indicator will appear black on yellow.

FREE RUN The FREE RUN indicator is informational text identifying when the NCSU is operational but not in service or when there is no active reference signal. Normally, the indicator will not appear. However, when either of the above stated conditions exist, the indicator will appear black on yellow.

POWER ROOM The POWER ROOM indicator is informational text identifying when a failure occurs in the power room. Normally, the indicator will not appear. However, when a power room failure occurs, the indicator will appear black on yellow.

EQUIP POWER The EQUIP POWER indicator is informational text identifying when a failure is detected in the alarm grid. Normally, the indicator will not appear. However, when a failure is detected in the alarm grid, the indicator will appear black on yellow.

RB CAP The RB CAP indicator is informational text identifying when the Recent Change Rollback area is fifty percent of capacity or greater. Normally, the indicator will not appear. However, when 50 percent of capacity or greater is reached in the Recent Change Rollback area, the indicator will appear black on yellow. This indicator will remain black on yellow until the Tape Write/Read Process (TWRP) is performed or buffer usage goes below 50 percent. This indicator will only be displayed for LEC offices.

MEM REC PH The MEM REC PH indicator is informational text identifying when a Memory Recovery Phase occurs. Normally, the indicator will not appear. However, when a Memory Recovery Phase occurs, the indicator will appear black on yellow. This indicator will remain black on yellow until the indicator is turned off by Poke **809**. This indicator will only be displayed for LEC offices.

SDC The SDC indicator is informational text identifying when any system degrading condition occurs. In the normal state (non-degraded), the indicator will appear white on black. When a service degraded condition exists, the indicator will appear white on red.

PGM CNTL OFFNRM The PGM CNTL OFFNRM indicator is informational text identifying when any program control off-normal condition occurs. Normally, the indicator will appear white on black (no program controls). When a program control exists, the indicator will appear black on yellow.

OVLD CTL IN EFF The OVLD CTL IN EFF indicator is informational text identifying when any overload control goes into effect. Normally, the indicator will appear white on black (no overload control). When an overload control exists, the indicator will appear black on yellow.

INTRPT INH The INTRPT INH indicator is informational text identifying when any interrupt inhibit exists. Normally, the indicator will appear white on black (no interrupt inhibits). When an interrupt inhibit exists, the indicator will appear black on yellow.

REFSTAT The REFSTAT indicator is informational text identifying when any off-normal condition exists in the external reference signal. Normally, the indicator will appear white on black (no off-normal condition). When an off-normal condition exists, the indicator will appear black on yellow.

SYSTEM CONTROLS
The SYSTEM CONTROLS indicator is informational text identifying the system control area of Page 108 and will appear white on black.

RESTRICT RC The RESTRICT RC indicator is informational text identifying when Recent Change (RC) restrictions are in effect. When RC restrictions are not in effect, the indicator will appear white on black. When RC restrictions are in effect, the indicator will appear black on white.

INH SUP PRINT The INH SUP PRINT indicator is informational text identifying when supplementary interrupt printouts are inhibited. Normally, the indicator will appear white on black. However, when supplementary interrupt printouts are inhibited, the indicator will appear black on white.

INH INT PRINT The INH INT PRINT indicator is informational text identifying when interrupt printouts are inhibited. Normally, the indicator will appear white on black (not inhibited). However, when interrupt printouts are inhibited, the indicator will appear black on white.

INH AUD PRINT The INH AUD PRINT indicator is informational text identifying when audit printouts are inhibited. Normally, the indicator will appear white on black (not inhibited). However, when audit printouts are inhibited, the indicator will appear black on white.

ELEV AUD PRINT The ELEV AUD PRINT indicator is informational text identifying when the message priority of audit printouts has been elevated to a higher level of output. Normally, the indicator will appear white on black. However, when the priority level has been elevated, the indicator will appear black on white.

REINIT TTY The REINIT TTY indicator is informational text identifying when the TTY I/O system has been reinitialized. The indicator will appear white on black.

REQ TTY AUDITS The REQ TTY AUDITS indicator is informational text identifying when the TTY audit request is being processed. Normally, the indicator will appear white on black. When selected, the indicator will appear black on white.

CLEAR INTERRUPTS
The CLEAR INTERRUPTS indicator is informational text identifying when interrupts are being cleared. The indicator will appear white on black.

CLEAR MEM REC PHASE
The CLEAR MEM REC PHASE indicator is informational text identifying how to Clear the Memory Recovery Phase indicator. The indicator will appear white on black. This indicator will only be displayed for LEC offices.

OP:OOSUNITS (ALL)

The OP:OOSUNITS (ALL) indicator is informational text associated with Poke Command 899. The indicator will appear white on black.

PROCESSOR EQUIPMENT STATUS

The PROCESSOR EQUIPMENT STATUS indicator is informational text identifying the processor equipment status area of Page 108. The indicator will appear white on black.

The following describes the two basic color schemes used for indicators in the processor equipment status area of Page 108:

(1) Duplexed equipment or equipment that has only one spare will have the following states/colors:

- Normal — White on black
- Major Alarm or problem — White on red
- Critical Alarm or problem — *Flashing* white on red.

Examples of this equipment type are:

— Central Control (CC)
— System Buses
— Auxiliary Unit Interface (AUI)
— MCC and Utility Processor (MUP)
— Attached Processor System (APS)
— Auxiliary Unit Bus (AUB)
— Attached Processor Interface (API).

Equipment that has multiple elements, equipment that uses the N + K sparing strategy or equipment that is not critical to call processing will have the following states/colors:

- Normal — White on black
- Minor Alarm or problem — Black on yellow
- Major Alarm or problem — White on red.

Examples of this equipment type are:

- Program Stores (PSs)
- Call Stores (CSs)
- Fan System (FNS)
- Scan and Signal Distribution (SSD) Matrices
- Input/Output Unit Controller (IOUC)
- Input/Output Unit Selector (IOUS)

NOTE:
With some equipment types (TUCs for example) there are *no* major alarm conditions since the equipment is not service affecting.

CC The CC indicator is informational text identifying the state of the central controls. Normally, the indicator will appear white on black. When either CC is out-of-service, the indicator will appear white on red.

PSB The PSB indicator is informational text identifying the state of the program store buses (PSBs). Normally, the indicator will appear white on black. When either PSB is out-of-service, the indicator will appear white on red.

CSB The CSB indicator is informational text identifying the state of the Call Store Buses (CSBs). Normally, the indicator will appear white on black. When either CSB is out-of-service, the indicator will appear white on red.

PS The PS indicator is informational text identifying the state of the Program Stores (PSs). Normally, the indicator will appear white on black. When one or more, but not all, spare program stores are out-of-service, the indicator will appear black on yellow. When there are no spare program stores, the indicator will appear white on red.

CS The CS indicator is informational text identifying the state of the Call Stores (CSs). Normally, the indicator will appear white on black. When one or more, but not all, spare call stores are out-of-service, the indicator will appear black on yellow. When there are no spare call stores, the indicator will appear white on red.

FNS The FNS indicator is informational text identifying the state of the fan system. Normally, the indicator will appear white on black. When there is a minor alarm associated with the fan system, the indicator will appear black on yellow. When there is a major alarm associated with the fan system, the indicator will appear white on red.

IFB The IFB indicator is informational text identifying the state of the Interface Buses (IFBs). Normally, the indicator will appear white on black. When either IFB is out-of-service, the indicator will appear white on red.

AUI The AUI indicator is informational text identifying the state of the Auxiliary Unit Interfaces (AUIs). Normally, the indicator will appear white on black. When either AUI is out-of-service, the indicator will appear white on red. When both AUIs are out-of-service, the indicator will appear flashing white on red.

SSD The SSD indicator is informational text identifying the state of the Scan and Signal Distributor (SSD) matrix. Normally, the indicator will appear white on black. When either SSD matrix unit is out-of-service, the indicator will appear black on yellow.

MUP The MUP indicator is informational text identifying the state of the MCC and Utility Processors (MUPs). Normally, the indicator will appear white on black. When either MUP is out-of-service or if a MCC timeout occurs, the indicator will appear white on red.

IOUS The IOUS indicator is informational text identifying the state of the Input/Output Unit Selectors (IOUSs). Normally, the indicator will appear white on black. When the number of out-of-service IOUSs causes a serious threat to service, the indicator will appear white on red. If there is not a serious threat to service, the indicator will appear black on yellow.

NOTE:
The strategy used with IOUSs to determine a "serious threat to service" is the same as was used in the 1A Processor.

IOUC The IOUC indicator is informational text identifying the state of the Input/Output Unit Controllers (IOUCs). Normally, the indicator will appear white on black. When the number of out-of-service IOUCs causes a serious threat to service, the indicator will appear white on red. If there is not a serious threat to service, the indicator will appear black on yellow.

NOTE:
The strategy used with IOUCs to determine a "serious threat to service" is the same as was used in the 1A Processor.

APS The APS indicator is informational text identifying the state of the Attached Processor System (APS). Normally, the indicator will appear white on black. When the APS hardware is out-of-service, the indicator will appear white on red. If one or more of the following conditions exist, the indicator will appear flashing white on red:

(a) The APS is duplex failed.

(b) The 1BFILE is duplex failed.

(c) The CNI traffic stream has stopped.

If either of the above conditions exist, the APS can only be taken to its normal state via program control.

API The API indicator is informational text identifying the state of the Attached Processor Interfaces (APIs). Normally, the indicator will appear white on black. When either API is out-of-service, the indicator will appear white on red. When both APIs are out-of-service, the indicator will appear flashing white on red.

DUS The DUS indicator is informational text identifying the state of the data unit selector (DUSs). The DUS units are not functional for 4E22 and later generics. The DUS indicator will appear white on black for DUSs that remain "equipped" in translations. The DUS indicator will appear as blank for DUSs shown as "unequipped" in translations.

TUC The TUC indicator is informational text identifying the state of the tape unit controllers (TUCs). The TUC units are not functional for 4E22 and later generics. The TUC indicator will appear white on black for TUCs that remain "equipped" in translations. The TUC indicator will appear as blank for TUCs shown as "unequipped" in translations.

AUB The AUB indicator is informational text identifying the state of the Auxiliary Unit Buses (AUBs). Normally, the indicator will appear white on black. When either AUB is out-of-service, the indicator will appear white on red. When both AUBs are out-of-service, the indicator will appear flashing white on red.

PUB The PUB indicator is informational text identifying the state of the Peripheral Unit Buses (PUBs). Normally, the indicator will appear white on black. When either PUB is out-of-service, the indicator will appear white on red. When both PUBs are out-of-service, the indicator will appear flashing white on red.

PCD The PCD indicator is informational text identifying the state of the Power Conversion and Distribution (PCD) system. Normally, the indicator will appear white on black. When there is a minor alarm associated with the PCD system, the indicator will appear black on yellow. When there is a major alarm associated with the PCD system, the indicator will appear white on red.

XPWR The XPWR indicator is informational text identifying the state of the Miscellaneous Power (XPWR) system. Normally, the indicator will appear white on black. When there is a minor alarm associated with the XPWR system, the indicator will appear black on yellow. When there is a major alarm associated with the XPWR system, the indicator will appear white on red.

SFI The SFI indicator is not operational at this time.

SPP The SPP indicator is not operational at this time.

PERIPHERAL EQUIPMENT STATUS

The PERIPHERAL EQUIPMENT STATUS indicator is informational text identifying the peripheral equipment status area of Page 108. The indicator will appear white on black. The following describes the two basic color schemes used for indicators in the peripheral equipment status area of Page 108:

(1) Duplexed equipment or equipment that has only one spare will have the following states/colors:

- Normal — White on black
- Major Alarm or problem — White on red
- Critical Alarm or problem — *Flashing* white on red.

Equipment types that have multiple elements, equipment that use the N + K sparing strategy or equipment that is not critical to call processing will have the following states/colors:

- Normal — White on black
- Minor Alarm or problem — Black on yellow
- Major Alarm or problem — White on red.

The 1B Processor MUP will support three indicator states for peripheral equipment indicators. When employed, these states will be normal, warning and critical.

NOTE:
Unlike the processor equipment indicators, the peripheral equipment indicators are controlled by the PUCNAUDS program (pident) system. The PUCNAUDS pident will only set the primary lamp bit. Consequently, the secondary lamp state will not be used for most peripheral equipment.

TMSP The TMSP indicator is informational text identifying the state of the Time Multiplexed Switch Peripherals (TMSPs). Normally, the indicator will appear white on black. When any TMSP is out-of-service, the indicator will appear white on red.

TSI The TSI indicator is informational text identifying the state of the Time Slot Interchanges (TSIs). Normally, the indicator will appear white on black. When any TSI subunit is out-of-service, the indicator will appear white on red.

NCLK The NCLK indicator is informational text identifying the state of the Network Clock (NCLK). Normally, the indicator will appear white on black. When the network clock is out-of-service, the indicator will appear white on red.

NCSU The NCSU indicator is informational text identifying the state of the Network Clock Synchronization Unit (NCSU). Normally, the indicator will appear white on black. When the NCSU external reference is removed from service via either a hardware fault or a TTY input message, when the NCSU is removed from service or when the System Clock (SCLK) is duplex failed, the indicator will appear white on red.

SCLK The SCLK indicator is informational text identifying the state of the System Clock (SCLK). Normally, the indicator will appear white on black. When either of the system clock controllers is out-of-service, the indicator will appear white on red. If both controllers are out-of-service, the indicator will appear white on red.

SP The SP indicator is informational text identifying the state of the Signal Processors (SPs). Normally, the indicator will appear white on black. When any SP is out-of-service, the indicator will appear white on red.

DT The DT indicator is informational text identifying the state of the Digroup Terminals (DTs). Normally, the indicator will appear white on black. When any digroup terminal is out-of-service, the indicator will appear white on red.

DIF The DIF indicator is informational text identifying the state of the Digital Interface Frames (DIFs). Normally, the indicator will appear white on black. When any DIF subunit (including DIUs) is out-of-service, the indicator will appear white on red.

VIF The VIF indicator is informational text identifying the state of the Voice Interface Frames (VIFs). Normally, the indicator will appear white on black. When any VIF subunit is out-of-service, the indicator will appear white on red.

EST The EST indicator is informational text identifying the state of the Echo Suppressor Terminals (ESTs). Normally, the indicator will appear white on black. When any EST is out-of-service, the indicator will appear white on red.

SCS The SCS indicator is informational text identifying the state of the Service Circuit System (SCS). Normally, the indicator will appear white on black. When an SCS is out-of-service, the indicator will appear white on red.

RA The RA indicator is informational text identifying the state of the Recorded Announcement (RA) frame. Normally, the indicator will appear white on black. When any recorded announcement frame unit is out-of-service, the indicator will appear white on red.

TGR The TGR indicator is informational text identifying the state of the Terminal Group (TGR) frame. Normally, the indicator will appear white on black. When any TGR is out-of-service, the indicator will appear white on red.

SLNK The SLNK indicator is informational text identifying the state of the CCIS Signaling Links (SLKs). Normally, the indicator will appear white on black. When any CCIS signaling link is out-of-service, the indicator will appear black on yellow.

VFL The VFL indicator is informational text identifying the state of the CCIS Voice Frequency Links (VFLs). Normally, the indicator will appear white on black. When any of the CCIS voice frequency links are out-of-service, the indicator will appear white on red.

R&T The R&T indicator is informational text identifying the state of the Ringing and Tone (R&T) plant. Normally, the indicator will appear white on black. When either ringing and tone plant side (0 or 1) is out-of-service, the indicator will appear white on red.

SVC The SVC indicator is informational text identifying the state of the Service Circuits (SVCs). Normally, the indicator will appear white on black.

When service circuits are set to the "Maintenance Disabled" state and the number of maintenance disabled circuits ***has not*** exceeded the allowable maintenance busy threshold, the indicator will appear black on yellow.

When service circuits are set to "Maintenance Disabled" state and the number of maintenance disabled circuits ***has*** exceeded the allowable maintenance busy threshold, but not exceeded the critical threshold, the indicator will appear white on red.

When service circuits are set to "Maintenance Disabled" state and the number of maintenance disabled circuits ***has*** exceeded the critical threshold, the indicator will appear flashing white on red.

XTSI The XTSI indicator is informational text identifying the state of the Expanded Time Slot Interchanges (XTSIs). Normally the indicator will appear white on black. When XTSI(s) have a minor alarm, the indicator will appear black on yellow. When XTSI(s) have a major alarm, the indicator will appear white on red. When XTSI(s) have a critical alarm, the indicator will appear flashing white on red.

B. Page 108 — Poke Commands

6.17 The following information describes the function of each Page 108 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels.

NOTE:
Poke Commands in the 800 series are global poke commands and can be executed from any page.

801 - RESTRICT RC

Poke Command 801 will toggle the restriction function that controls (enables and restricts) recent change activity. Its corresponding indicator will change accordingly.

802 - INH SUP PRINT

Poke Command 802 will toggle the restriction function that controls the output of supplementary interrupt printouts to the MTC channel. Its corresponding indicator will change accordingly.

803 - INH INT PRINT

Poke Command 803 will toggle the restriction function that controls the output of interrupt printouts. Its corresponding indicator will change accordingly.

804 - INH AUD PRINT

Poke Command 804 will toggle the restriction function that controls the output of audit printouts. Its corresponding indicator will change accordingly.

805 - ELEV AUD PRINT

Poke Command 805 controls the function for changing the priority of audit messages between a higher output priority and the original priority. Its corresponding indicator will change accordingly.

806 - REINIT TTY SYS

Poke Command 806 will cause all TTY buffers to be flushed and the TTY input/output system to be reinitialized. Its corresponding indicator will change accordingly.

NOTE:
All messages in the TTY input/output queue will be lost when Poke Command 806 is entered.

807 - REQ TTY AUDIT

Poke Command 807 will cause an audit of the TTY system to be run once. Output will be directed to the MTC channel and a PF (Printout Follows) acknowledgment will be displayed in the response part of the command line. Its corresponding indicator will change accordingly.

808 - CLEAR INTERRUPTS

Poke Command 808 will cause the INTERRUPT indicator to be removed. However, subsequent interrupts will cause the INTERRUPT indicator to reappear.

809 - CLEAR MEM REC PHASE

Poke Command 809 will cause the MEM REC PH indicator to be removed. Poke Command 809 will only be allowed for LEC offices.

810 - SDC Poke Command 810 will cause a system output identifying all service degrading conditions in effect to be directed to the MTC channel. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line. Poke Command 810 corresponds to the OP:SDC! TTY input message.

811 - PGM CNTL OFFNRM

Poke Command 811 will cause a system output identifying all software controls in effect to be directed to the MTC channel. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

812 - OVLD CTL IN EFF

Poke Command 812 will cause an output message to be printed identifying the status of office overload controls. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

813 - INTRPT INH

Poke Command 813 will cause an output listing of all inhibited interrupts to be printed at the MTC channel. Poke Command 813 corresponds to the OP:INHINT and OP:PERIFINH TTY input messages. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

814 - REFSTAT

Poke Command 814 will cause an output of one or more OP:NCSU messages depending on the status of the network clock synchronization unit. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

820 - 841 **850-867**" Poke Commands 820 through 841 and 850 through 867 will correspond to the OP:OOSUNITS [*utype*]! TTY input messages where [*utype*] is the equipment type associated with each individual poke command. These poke commands will cause an output listing of all out-of-service units of the selected equipment type to be printed at the MTC channel. The PF (Printout Follows) acknowledgment will be displayed in the response part of the command line.

834-835 Poke Commands 834 and 835 will still be active for 4E22 and later generics if the DUS and TUC units remain "equipped" in translations. These poke commands will cause an output listing of all out-of-service DUSs and TUCs.

Poke Commands 834 and 835 will respond with an "NG" for 4E22 and later generics if the DUS and TUC units are "unequipped" in translations.

840 - SFI Poke Command 840 is not operational and will respond with an "NG".

841 - SPP Poke Command 841 is not operational and will respond with an "NG".

867 - XTSI Poke Command 867 is a new poke command that will correspond to OP:OOSUNITS:XTSI! TTY input message. Poke Command 867 follows the process of Poke Commands 820-841 and 850-867, above.

899 - OP:OOSUNITS (ALL)

Poke Command 899 will cause a complete listing of all out-of-service processor and peripheral equipment to be output. Poke Command 899 corresponds to the OP:OOSUNITS! TTY input message.

Program Store Status and Control (Page 109)

6.18 The Program Store Status and Control Page provides the status for all program stores and program store buses in addition to store and bus control. The Program Store Status and Control Page (Page 109) is invoked by entering Poke Command 109.

6.19 The Program Store Status and Control Page contains the following functional sections:

- Program Store Bus Status (BUS STATUS)
- Program Store Status (STORE STATUS)
- Program Store and Bus Control (STORE CONTROL)

6.20 The Program Store Bus Status area contains indicators identifying the status of the Program Store Buses (PSBs). The Program Store Status area contains indicators showing the status of each program store in addition to store maintenance bits. The status is indicated with a text phrase such as ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNEQ (Unequipped), etc. The Program Store Control area contains poke commands to be used to Remove (RMV), Restore (RST) and Diagnose (DGN) program stores in addition to commands used to obtain program store and bus status information.

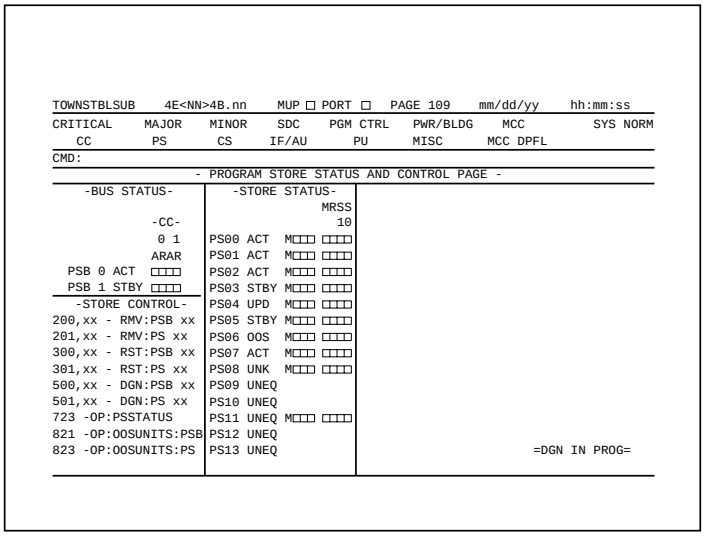


Figure 12. Program Store Status and Control Page (Page 109)

A. Page 109 — Indicators

6.21 The following information describes the indicators associated with Page 109. The text, colors and specific circumstances under which the indicators will change are specified.

BUS STATUS The BUS STATUS indicator is informational text identifying the program store bus status area of Page 109. The indicator will appear white on black.

CC The CC indicator is informational text identifying the central control and will appear white on black.

0 1 The 0 1 indicator is informational text identifying CC 0 and CC 1. The indicator will appear white on black.

ARAR The ARAR indicator is informational text identifying the Address (A) and Reply (R) bus-element connections to CC 0 and CC 1. The indicator will appear white on black.

PSB [0,1] The "PSB [0,1]" indicator is informational text identifying PSB 0 and PSB 1. The indicator will appear the same color as the PSB [0,1] state and status bits found below.

PSB [0,1] state & status bits

The PSB 0/1 state and status bit indicators identify the send/receive hardware status of the program store buses. However, this status may not be the correct software status for these buses since the MUP cannot accurately interpret the hardware states into corresponding software states. Therefore, these indicators **should not** be used to determine the software status of the program store buses.

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For program store bus status, use global Poke Command 821.

The program store bus state indicators are ACT (Active), STBY (Standby) and OOS (Out-Of-Service). The indicator text and associated colors are as follows:

— ACT *wxyz* — Black on green
— STBY *wxyz* — White on blue
— OOS *wxyz* (em Black on red.

The ARAR status bits "*wxyz*" identify program store bus-element connections to CC 0 and CC 1. For example:

- If "*w*"=1, CC 0 is sending on that bus.
- If "*x*"=1, CC 0 is receiving on that bus.
- If "*y*"=1, CC 1 is sending on that bus.
- If "*z*"=1, CC 1 is receiving on that bus.

STORE CONTROL

The STORE CONTROL indicator is informational text identifying the store control data area for Page 109. The indicator will appear white on black.

RMV:PSB xx The "RMV:PSB xx" indicator is informational test associated with Poke Command 200 used to remove a program store bus from service. The indicator will appear white on black.

RMV:PS xx The "RMV:PS xx" indicator is informational text associated with Poke Command 201 used to remove a program store from service. The indicator will appear white on black.

RST:PSB xx The "RST:PSB xx" indicator is informational text associated with Poke Command 300 used to restore a program store bus to service. The indicator will appear white on black.

RST:PS xx The "RST:PS xx" indicator is informational text associated with Poke Command 301 used to restore a program store to service. The indicator will appear white on black.

DGN:PSB xx The "DGN:PSB xx" indicator is informational text associated with Poke Command 500 used to diagnose a program store bus. The indicator will appear white on black.

DGN:PS xx The "DGN:PS xx" indicator is informational text associated with Poke Command 501 used to diagnose a program store. The indicator will appear white on black.

OP:PSSTATUS

The OP:PSSTATUS indicator is informational text associated with Poke Command 723 used to obtain program store status. The indicator will appear white on black.

OP:OOSUNITS:PSB

The OP:OOSUNITS:PSB indicator is informational text associated with Poke Command 821 used to obtain a list of out-of-service program store buses. The indicator will normally appear white on black. However, if either of the program store buses is Out-Of-Service (OOS) or the bus status is Unknown (UNK), the indicator will appear white on red.

OP:OOSUNITS:PS

The OP:OOSUNITS:PS indicator is informational text associated with Poke Command 823 used to obtain a list of out-of-service program stores. The indicator will normally appear white on black. When one or more, but not all, spare program stores are out-of-service, the indicator will appear black on yellow. When there are no spare program stores, the indicator will appear white on red.

STORE STATUS

The STORE STATUS indicator is informational text identifying the program store status area of Page 109. The indicator will appear white on black.

MRSS 10

The MRSS indicator is informational text identifying the Maintenance (M), Receive on (R), Send on bus 1 (S1) and Send on bus 0 (S0) maintenance bits. The indicator will appear white on black.

PS [00,13] state Mcde fghi

The "PS [00,13] state Mcde fghi" indicator is informational text identifying the state and status information for program stores 00 through 13. The program store state indicators are ACT (Active), STBY (Standby), UPD (Update), UNK (Unknown), OOS (Out-Of-Service) and UNEQ (Unequipped).

The UNEQ (Unequipped) state has two modes:

- Unequipped/bits normal
- Unequipped/bits abnormal.

The unequipped/bits normal mode will not include the program store M-code value (Mcde) and the maintenance & status bits (fghi). The unequipped/abnormal mode will include the program store M-code value (Mcde) and maintenance & status bits (fghi).

The program store state indicator text and associated colors are as follows:

- ACT *Mcde fghi* — Black on green
- STBY *Mcde fghi* — White on blue
- UPD *Mcde fghi* — White on blue
- UNK *Mcde fghi* — Red on yellow
- OOS *Mcde fghi* — Black on red
- UNEQ *Mcde fghi* — White on black.

The program store M-code value (Mcde) will be identified and displayed as the letter M followed by the numeric M-code value, for example, M000.

The program store maintenance and status bits (fghi) are single-digit values which are set under 1B Processor hardware control. However, the maintenance and status bit values for unequipped program stores will be determined by communication between the MCC and 1B Processor. The bit values will only be displayed for unequipped program stores when an abnormal bit value is identified ("Mcde fghi" data other than "M000 1000").

The program store maintenance and status bit (fghi) values and definitions are as follows:

- If "*f*"=0, Identified program store is NOT in the maintenance mode.
- If "*f*"=1, Identified program store is in the maintenance mode.
- If "*g*"=0, Identified program store is receiving on bus 0.
- If "*g*"=1, Identified program store is receiving on bus 1.
- If "*h*"=0, Identified program store is NOT sending on bus 1.
- If "*h*"=1, Identified program store is sending on bus 1.
- If "*i*"=0, Identified program store is NOT sending on bus 0.
- If "*i*"=1, Identified program store is sending on bus 0.

DGN IN PROG

The DGN IN PROG indicator is informational text identifying when any system unit is under diagnostic control. Normally, the indicator will not appear. However, when diagnostics are in progress, the indicator will appear yellow on black.

B. Page 109 — Poke Commands

6.22 The following information describes the function of each Page 109 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels. Poke commands that use a member number (xx) require that both digits be specified. Otherwise, an error message will be output.

NOTE:
Poke commands in the 200, 300 and 500 series are specific to Page 109 (local commands). Poke commands in the 700 and 800 series are global poke commands and can be executed from any page.

200,xx	Poke Command 200 corresponds to input message RMV:PSB xx! used to remove a specific program store bus (00 or 01).
201,xx	Poke Command 201 corresponds to input message RMV:PS xx! used to remove a specific program store (00-13).
300,xx	Poke Command 300 corresponds to input message RST:PSB xx! used to restore a specific program store bus (00 or 01).
301,xx	Poke Command 301 corresponds to input message RST:PS xx! used to restore a specific program store (00-13).
500,xx	Poke Command 500 corresponds to input message DGN:PSB xx! used to diagnose a specific program store bus (00 or 01).
501,xx	Poke Command 501 corresponds to input message DGN:PS xx! used to diagnose a specific program store (00-13).
723	Poke Command 723 corresponds to input message OP:PSSTATUS! used to obtain the status of program stores.
821	Poke Command 821 corresponds to input message OP:OOSUNITS:PSB! used to obtain a listing of all out-of-service program store buses.
823	Poke Command 823 corresponds to input message OP:OOSUNITS:PS! used to obtain a listing of all out-of-service program stores.

Call Store Status and Control (Page 110)

6.23 The Call Store Status and Control Page provides the status for all call stores and call store buses in addition to store and bus control. The Call Store Status and Control Page (Page 110) is invoked by entering Poke Command 110.

6.24 The Call Store Status and Control Page contains the following functional sections:

- Call Store Bus Status (BUS STATUS)
- Call Store Status (STORE STATUS)
- Call Store and Bus Control (STORE CONTROL)

6.25 The Call Store Bus Status area contains indicators identifying the status of the Call Store Buses (CSBs). The Call Store Status area contains indicators identifying the status of each call store in addition to store maintenance bits. The status is indicated with a text phrase such as ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNEQ (Unequipped), etc. The Call Store Control area contains poke commands to be used to Remove (RMV), Restore (RST) and Diagnose (DGN) call stores in addition to commands used to obtain call store and bus status information.

Figure 13 shows an example of the layout for Page 110.

A. Page 110 — Indicators

6.26 The following information describes the indicators associated with Page 110. The text, colors and specific circumstances under which the indicators will change are specified.

BUS STATUS The BUS STATUS indicator is informational text identifying the bus status area for Page 110. The indicator will appear white on black.

CC The CC indicator is informational text identifying the central control and will appear white on black.

0 1 The 0 1 indicator is informational text identifying CC 0 and CC 1. The indicator will appear white on black.

ARAR The ARAR indicator is informational text identifying the Address (A) and Reply (R) bus-element connections to CC 0 and CC 1. The indicator will appear white on black.

CSB [0,1] The CSB [0,1] indicator is informational text identifying CSB 0 and CSB 1. The indicator will appear the same color as the CSB [0,1] state and status bits found below.

CSB [0,1] state & status bits
The CSB 0/1 state and status bit indicators identify the send/receive hardware status of the call store buses. This status may not be the correct software status of the buses, since the MUP cannot accurately interpret the hardware states into corresponding software states. Therefore, these indicators **should not** be used to determine

the software status of the call store buses.

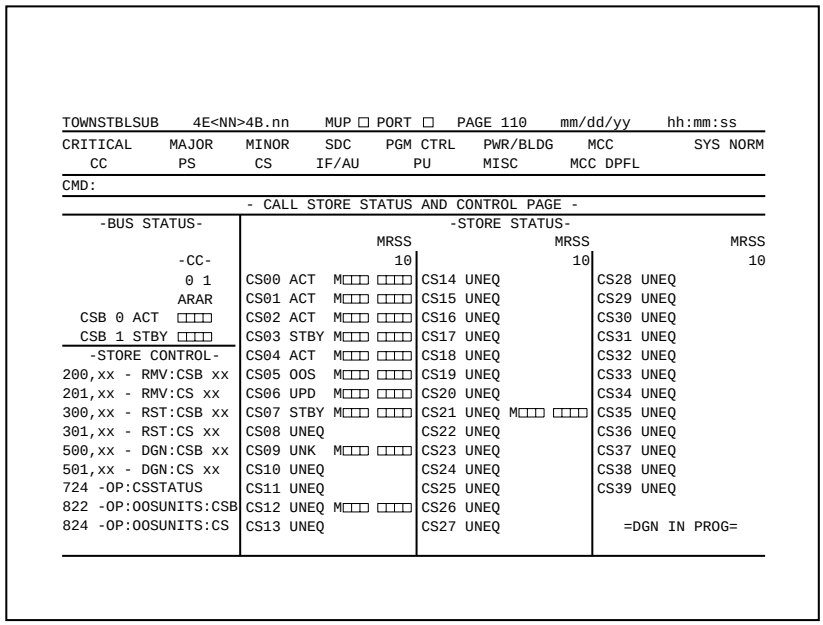


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Figure 13. Call Store Status and Control Page (Page 110)

6.27

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For call store bus status, use global Poke Command 822

The call store bus state indicators are ACT (Active), STBY (Standby) and OOS (Out-Of-Service). The indicator text and associated colors are as follows:

— ACT *wxyz* — Black on green
— STBY *wxyz* — White on blue
— OOS *wxyz* — Black on red.

The ARAR status bits "*wxyz*" identify call store bus-element connections to CC 0 and CC 1. For example:

- If "*w*"=1, CC 0 is sending on that bus.
- If "*x*"=1, CC 0 is receiving on that bus.
- If "*y*"=1, CC 1 is sending on that bus.
- If "*z*"=1, CC 1 is receiving on that bus.

STORE CONTROL

The STORE CONTROL indicator is informational text identifying the store control data area for Page 110. The indicator will appear white on black.

RMV:CSB xx The "RMV:CSB xx" indicator is informational text associated with Poke Command 200 used to remove a call store bus from service. The indicator will appear white on black.

RMV:CS xx The "RMV:CS xx" indicator is informational text associated with Poke Command 201 used to remove a call store from service. The indicator will appear white on black.

RST:CSB xx The "RST:CSB xx" indicator is informational text associated with Poke Command 300 used to restore a call store bus to service. The indicator will appear white on black.

RST:CS xx The "RST:CS xx" indicator is informational text associated with Poke Command 301 used to restore a call store to service. The indicator will appear white on black.

DGN:CSB xx The "DGN:CSB xx" indicator is informational text associated with Poke Command 500 used to diagnose a call store bus. The indicator will appear white on black.

DGN:CS xx The "DGN:CS xx" indicator is informational text associated with Poke Command 501 used to diagnose a call store. The indicator will appear white on black.

OP:CSSTATUS

The OP:CSSTATUS indicator is informational text associated with Poke Command 724 used to obtain call store status. The indicator will appear white on black.

OP:OOSUNITS:CSB

The OP:OOSUNITS:CSB indicator is informational text associated with Poke Command 822 used to obtain a listing of out-of-service call store buses. The indicator will normally appear white on black. However, if either of the call store buses is Out-Of-Service (OOS) or the bus status is Unknown (UNK), the indicator will appear white on red.

OP:OOSUNITS:CS

The OP:OOSUNITS:CS indicator is informational text associated with Poke Command 824 used to obtain a listing of out-of-service call stores. The indicator will normally appear white on black. When one or more, but not all, spare call stores are out-of-service, the indicator will appear black on yellow. When there are no spare call stores, the indicator will appear white on red.

STORE STATUS

The STORE STATUS indicator is informational text identifying the call store status area of Page 110. The indicator will appear white on black.

MRSS 10

The "MRSS" indicator is informational text identifying the Maintenance (M), Receive on (R), Send on bus 1 (S1) and Send on bus 0 (S0) maintenance bits. The indicator will appear white on black.

CS[00,39] state Mcde fghi

The "CS[00,39] state Mcde fghi" indicator is informational text identifying the state and status information for call stores 00 through 39. The call store state indicators are ACT (Active), STBY (Standby), UPD (Update), UNK (Unknown), OOS (Out-Of-Service) and UNEQ (Unequipped).

The UNEQ (Unequipped) state has two modes:

- Unequipped/bits normal
- Unequipped/bits abnormal.

The unequipped/bits normal mode will not include the call store M-code value (Mcde) and the maintenance & status bits (fghi). The unequipped/abnormal mode will include the call store M-code value (Mcde) and maintenance & status bits (fghi).

The call store state indicator text and associated colors are as follows:

— ACT *Mcde fghi* — Black on green
— STBY *Mcde fghi* — White on blue
— UPD *Mcde fghi* — White on blue
— UNK *Mcde fghi* — Red on yellow
— OOS *Mcde fghi* — Black on red
— UNEQ *Mcde fghi* — White on black.

The call store M-code value (Mcde) will be identified and displayed as the letter M followed by the numeric M-code value, for example, M000.

The call store maintenance and status bits (fghi) are single-digit values which are set under 1B Processor hardware control. However, the maintenance and status bit values for unequipped call stores will be determined by communication between the MCC and 1B Processor. The bit values will only be displayed for unequipped call stores when an abnormal bit value is identified ("Mcde fghi" data other than "M000 1000").

The call store maintenance and status bit (fghi) values and definitions are as follows:

- If "*f*"=0, Identified call store is NOT in the maintenance mode.
- If "*f*"=1, Identified call store is in the maintenance mode.
- If "*g*"=0, Identified call store is receiving on bus 0.
- If "*g*"=1, Identified call store is receiving on bus 1.
- If "*h*"=0, Identified call store is NOT sending on bus 1.
- If "*h*"=1, Identified call store is sending on bus 1.
- If "*i*"=0, Identified call store is NOT sending on bus 0.
- If "*i*"=1, Identified call store is sending on bus 0.

DGN IN PROG

The DGN IN PROG indicator is informational text identifying when any system unit is under diagnostic control. Normally, the indicator does not appear. However, when diagnostics are in progress, the indicator will appear yellow on black.

B. Page 110 — Poke Commands

6.28 The following information describes the function of each Page 110 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels. Poke commands that use a member number (xx) requires that both digits be specified. Otherwise, an error message will be output.

NOTE:
Poke Commands in the 200, 300 and 500 series are specific to Page 110 (local commands). Poke Commands in the 700 and 800 series are global poke commands and can be executed from any page.

200,xx Poke Command 200 corresponds to input message RMV:CSB xx! used to remove a specific call store bus (00 or 01).

201,xx Poke Command 201 corresponds to input message RMV:CS xx! used to remove a specific call store (00-39).

300,xx Poke Command 300 corresponds to input message RST:CSB xx! used to restore a specific call store bus (00 or 01).

301,xx Poke Command 301 corresponds to input message RST:CS xx! used to restore a specific call store (00-39).

500,xx Poke Command 500 corresponds to input message DGN:CSB xx! used to diagnose a specific call store bus (00 or 01).

501,xx Poke Command 501 corresponds to input message DGN:CS xx! used to diagnose a specific call store (00-39).

724 Poke Command 724 corresponds to input message OP:CSSTATUS! used to obtain the status of call stores.

822 Poke Command 822 corresponds to input message OP:OOSUNITS:CSB! used to obtain a listing of out-of-service call store buses.

824 Poke Command 824 corresponds to input message OP:OOSUNITS:CS! used to obtain a listing of out-of-service call stores.

IFB Clients Status and Control (Page 111)

6.29 The IFB Clients Status and Control Page provides the status for all IFB clients in addition to bus and client control. The IFB Clients Status and Control Page (Page 111) is invoked by entering Poke Command 111.

6.30 The IFB Clients Status and Control Page contains the following functional sections:

- IFB Bus Status (BUS STATUS)
- IFB Clients Status (CLIENT STATUS)
- IFB Clients Bus and Client Control (BUS AND CLIENT CONTROL)

6.31 The IFB Bus Status area contains indicators identifying the status of the IFB Buses (IFBs). The Client Status area contains indicators identifying the status of each IFB Client in addition to maintenance bits. The status is indicated with a text phrase such as ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNEQ (Unequipped), UNK (Unknown), etc. The Bus and Client Control area contains poke commands to be used to Remove (RMV), Restore (RST), Diagnose (DGN), Switch (SW), Out-Of-Service (OOS), and Status (STAT) IFB Bus and Clients.

Figure 14 is an example of the layout for Page 111.

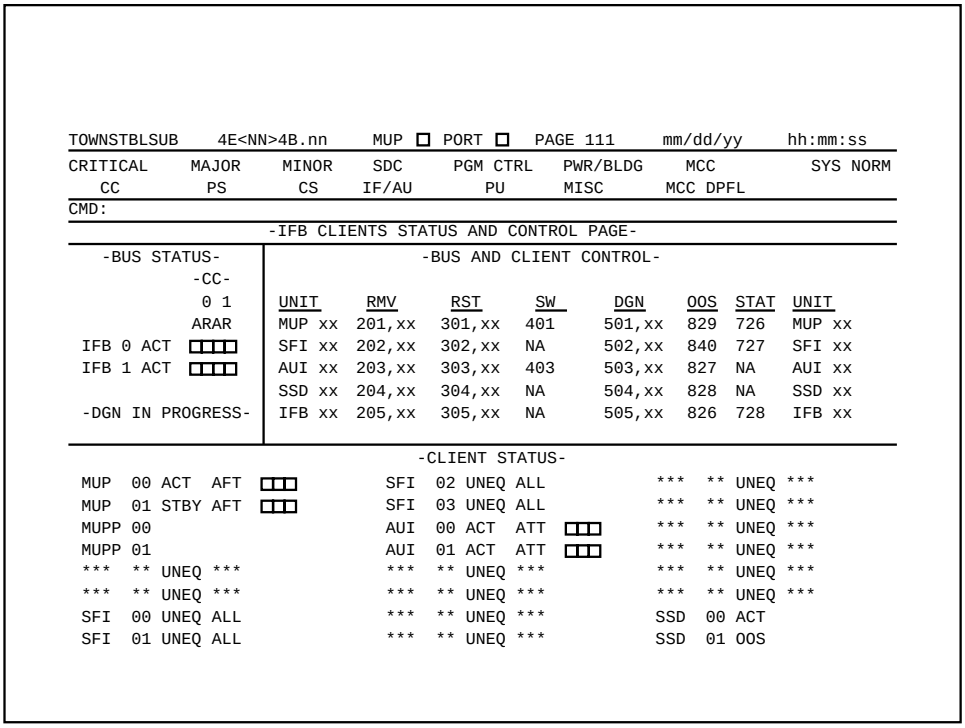


Figure 14. IFB Clients Status and Control Page (Page 111)

A. Page 111 — Indicators

6.32 The following information describes the indicators associated with Page 111. The text, colors and specific circumstances under which the indicators will change are specified.

BUS STATUS The BUS STATUS indicator is informational text identifying the bus status area for Page 111. The indicator will appear white on black.

CC The CC indicator is informational text identifying the central control and will appear white on black.

0 1 The 0 1 indicator is informational text identifying CC 0 and CC 1. The indicator will appear white on black.

ARAR The ARAR indicator is informational text identifying the Address (A) and Reply (R) bus-element connections to CC 0 and CC 1. The indicator will appear white on black.

IFB [0,1] The IFB [0,1] indicator is informational text identifying IFB 0 and IFB 1. The indicator will appear the same color as the corresponding IFB [0,1] state and status bits found below.

IFB [0,1] state & status bits

The IFB 0/1 state and status bit indicators are informational text identifying the send/receive hardware status of the interface buses. However, this status may not be the correct software status for these buses, since the MUP cannot accurately interpret the hardware states into corresponding software states. These indicators **should not** be used to determine the software status of the interface buses.

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For interface bus status, use global Poke Command 826

The interface bus state indicators are ACT (Active), STBY (Standby), and OOS (Out-Of-Service). The text and associated colors are as follows:

— ACT *wxyz* — Black on green
— STBY *wxyz* — White on blue
— OOS *wxyz* — Black on red

The ARAR status bits "*wxyz*" identify interface bus-element connections to CC 0 and CC 1. For example:

- If "*w*"=0, address bus to CC 0 is not active.
- If "*w*"=1, address bus to CC 0 is active.
- If "*x*"=0, reply bus to CC 0 is not active.
- If "*x*"=1, reply bus to CC 0 is active.
- If "*y*"=0, address bus to CC 1 is not active.
- If "*y*"=1, address bus to CC 1 is active.
- If "*z*"=0, reply bus to CC 1 is not active.
- If "*z*"=1, reply bus to CC 1 is active.

DGN IN PROG

The DGN IN PROG indicator is informational text identifying when any system unit is under diagnostic control. Normally, the indicator will not appear. However, when diagnostics are in progress, the indicator will appear yellow on black.

BUS AND CLIENT CONTROL

The BUS AND CLIENT CONTROL indicator is informational text identifying the Bus and Client Control data area for Page 111. The indicator will appear white on black.

UNIT The UNIT indicator is informational text identifying the client or bus name. The indicator will appear white on black.

RMV The RMV indicator is informational text associated with Poke Commands 201-205 used to remove a "Unit" from service. The indicator will appear white on black.

RST The RST indicator is informational text associated with Poke Commands 301-305 used to restore a "Unit" to service. The indicator will appear white on black.

SW The SW indicator is informational text associated with Poke Commands 401 and 403 used to switch a "Unit". The indicator will appear white on black.

DGN The DGN indicator is informational text associated with Poke Commands 501-505 used to diagnose a "Unit". The indicator will appear white on black.

OOS The OOS indicator is informational text associated with Poke Commands 826-829, and 840 used to obtain a listing of out-of-service "Units". The indicator will appear white on black.

STAT The STAT indicator is informational text associated with Poke Commands 726-728 used to obtain the status of a "Unit". The indicator will appear white on black.

UNIT The UNIT indicator is informational text identifying the bus or client name. The indicator will appear white on black.

xx The xx indicator is informational text identifying the client number. Both digits are required to be specified. The indicator will appear white on black.

NA The NA indicator is informational text identifying a poke command is not applicable for that input command associated with that client. The indicator will appear white on black.

MUP xx The MUP xx indicator is informational text identifying the MUP xx associated with Poke Commands 201,xx; 301,xx; 401, 501,xx; 829; and 726. The MUP xx indicator appears on both ends of line 9 for readability. The indicator will appear white on black.

SFI xx The SFI xx indicator is not operational at this time.

AUI xx The AUI xx indicator is informational text identifying the AUI xx associated with Poke Commands 203,xx; 303,xx; 403, 503,xx; and 827. The AUI xx indicator appears on both ends of line 11 for readability. The indicator will appear white on black.

SSD xx The SSD xx indicator is informational text identifying the SSD xx associated with Poke Commands 204,xx; 304,xx; 504,xx; and 828. The SSD xx indicator appears on both ends of line 12 for readability. The indicator will appear white on black.

IFB xx The IFB xx indicator is informational text identifying the IFB xx associated with Poke Commands 205,xx; 305,xx; 505,xx; 826; and 728. The IFB xx indicator appears on both ends of line 13 for

readability. The indicator will appear white on black.

CLIENT STATUS

The CLIENT STATUS indicator is informational text identifying the Client Status area of Page 111. The indicator will appear white on black.

MUP [00,01] The MUP [00,01] indicator is informational text identifying MUP 0 and MUP 1. The indicator will appear the same color as the corresponding MUP [00,01] status and maintenance bits found below.

MUP [00,01] status and maintenance bits

The "MUP 0/1 status and maintenance bit" indicators are informational text identifying the status of MUP 0 and MUP 1. The status indicator is a text phrase and the A (Active), F (Forced) and T (Trouble) maintenance bits are binary digits representing specific maintenance conditions.

The MUP status text phrases are ACT (Active), STBY (Standby), OOS (Out-Of-Service) and UNK (Unknown). The text and associated colors are as follows:

— ACT *aft* — Black on green
— STBY *aft* — White on blue
— OOS *aft* — Black on red
— UNK *aft* — Red on yellow.

The maintenance bits "*aft*" are single-digit values set under 1B Processor hardware control. For example:

- If "*a*"=1, associated MUP is active.
- If "*f*"=1, associated MUP is forced.
- If "*t*"=1, associated MUP trouble flag set.

The MCC design will not permit the F (Forced) or T (Trouble) bits to be known for the inactive MUP. Therefore, the force and trouble bits will be blank for the inactive MUP.

MUPP [00,01] The MUPP [00,01] indicator is informational text identifying MUP Power board (MUPP) 0 and MUP Power board (MUPP) 1. MUPP 0 is associated with MUP 0. The MUPP 0 indicator will appear the same color as the MUP 0 indicator found above. MUPP 1 is associated with MUP 1. The MUPP 1 indicator will appear the same color as the MUP 1 indicator found above.

UNEQ The UNEQ indicator is informational text identifying a line in the Client Status section of Page 111 as unequipped. The UNEQ indicator will be used for future IFB clients placed on Page 111. The indicator will appear white on black.

SFI [00,01] The SFI [00,01] indicator is not operational at this time.

SFI [02,03] The SFI [02,03] indicator is not operational at this time.

AUI [00,01] The "AUI [00,01]" indicator is informational text identifying AUI 0 and AUI 1. The indicator will appear the same color as the AUI [00,01] status and maintenance bits found below.

ATT The ATT indicator is informational text identifying the active (A), trouble - bus 0 (T) and trouble - bus 1 (T) maintenance bits. The indicator will appear the same color as the AUI [00,01] status and maintenance bits found below.

AUI [00,01] status and maintenance bits

The "AUI 0/1 status and maintenance bit" indicators are informational text identifying the status of AUI 0 and AUI 1. The status indicator is a text phrase and the A (active), T (trouble - bus 0) and T (trouble - bus 1) maintenance bits are binary digits representing specific maintenance conditions.

The AUI status text phrases are ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNK (Unknown), and UNAV (Unavailable). The text and associated colors are as follows:

— ACT *att* — Black on green
— STBY *att* — White on blue
— OOS *att* — Black on red
— UNK *att* — Red on yellow
— UNAV *att* — Black on yellow.

The maintenance bits "*att*" are single-digit values set under 1B Processor hardware control. For example:

- If "*a*"=1, associated AUI is active.
- If "first *t*"=1, associated AUI has trouble on bus 0.
- If "second *t*"=1, associated AUI has trouble on bus 1.

SSD [00,01] The SSD [00,01] indicator is informational text identifying SSD 0 and SSD 1. The indicator will appear the same color as the SSD [00,01] status indicator found below.

SSD [00,01] Status

The SSD 0/1 status indicators are informational text identifying the status of SSD 0 and SSD 1.

The SSD status text phrases are ACT (Active), OOS (Out-Of-Service), UNK (Unknown), and UNAV (Unavailable). The text and associated colors are as follows:

— ACT — Black on green
— OOS — Black on red
— UNK — Red on yellow
— UNAV — Black on yellow.

B. Page 111 — Poke Commands

6.33 The following information describes the function of each Page 111 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels. Poke commands that use a member number (xx) require that both digits be specified. Otherwise, an error message will be output.

NOTE:
Poke Commands in the 200, 300, 400 and 500 series are specific to Page 111 (local commands). Poke Commands in the 700 and 800 series are global poke commands and can be executed from any page.

201,xx	Poke Command 201 corresponds to input message RMV:MUP xx used to remove a specific MCC Utility Processor (00 or 01).
202,xx	Poke Command 202 is not operational and will respond with an "NG".
203,xx	Poke Command 203 corresponds to input message RMV:AUI xx used to remove a specific Auxiliary Unit Interface (00-01).
204,xx	Poke Command 204 corresponds to input message RMV:SSD xx used to remove a specific Scan and Signal Distributor (00-01).
205,xx	Poke Command 205 corresponds to input message RMV:IFB xx used to remove a specific Interface Bus (00-01).
301,xx	Poke Command 301 corresponds to input message RST:MUP xx used to restore a specific MCC Utility Processor (00 or 01).
302,xx	Poke Command 302 is not operational and will respond with an "NG".
303,xx	Poke Command 303 corresponds to input message RST:AUI xx used to restore a specific Auxiliary Unit Interface (00-01).
304,xx	Poke Command 304 corresponds to input message RST:SSD xx used to restore a specific Scan and Signal Distributor (00-01).
305,xx	Poke Command 305 corresponds to input message RST:IFB xx used to restore a specific Interface Bus (00-01).
401	Poke Command 401 corresponds to input message SW:MUP used to switch the active MCC Utility Processor (MUP) to the standby MUP, and switch the standby MUP to the active MUP.
403	Poke Command 403 corresponds to input message SW:AUI used to switch the active Auxiliary Unit Interface (AUI) to the standby AUI, and switch the standby AUI to the active AUI.
501,xx	Poke Command 501 corresponds to input message DGN:MUP xx used to diagnose a specific MCC Utility Processor (00 or 01).

502,xx	Poke Command 502 is not operational and will respond with an "NG".
503,xx	Poke Command 503 corresponds to input message DGN:AUI xx used to diagnose a specific Auxiliary Unit Interface (00-01).
504,xx	Poke Command 504 corresponds to input message DGN:SSD xx used to diagnose a specific Scan and Signal Distributor (00-01).
505,xx	Poke Command 505 corresponds to input message DGN:IFB xx used to diagnose a specific Interface Bus (00-01).
726	Poke Command 726 corresponds to input message OP:MUPSTAT used to obtain the status of the MCC Utility Processors (MUPs).
727	Poke Command 727 is not operational and will respond with an "NG".
728	Poke Command 728 corresponds to input message OP:IFBSTAT used to obtain the status of the Interface Buses (IFBs).
826	Poke Command 826 corresponds to input message OP:OOSUNITS:IFB used to obtain a listing of out-of-service Interface Buses.
827	Poke Command 827 corresponds to input message OP:OOSUNITS:AUI used to obtain a listing of out-of-service Auxiliary Unit Interfaces.
828	Poke Command 828 corresponds to input message OP:OOSUNITS:SSD used to obtain a listing of out-of-service Scan and Signal Distributors.
829	Poke Command 829 corresponds to input message OP:OOSUNITS:MUP used to obtain a listing of out-of-service MCC Utility Processors.
840	Poke Command 840 is not operational and will respond with an "NG".

1B Processor Status (Page 118)

6.34 The 1B Processor Status Page (Page 118) provides the status of all 1B Processor elements excluding the program stores and call stores.

6.35 The 1B Processor Status Page contains the following functional sections:

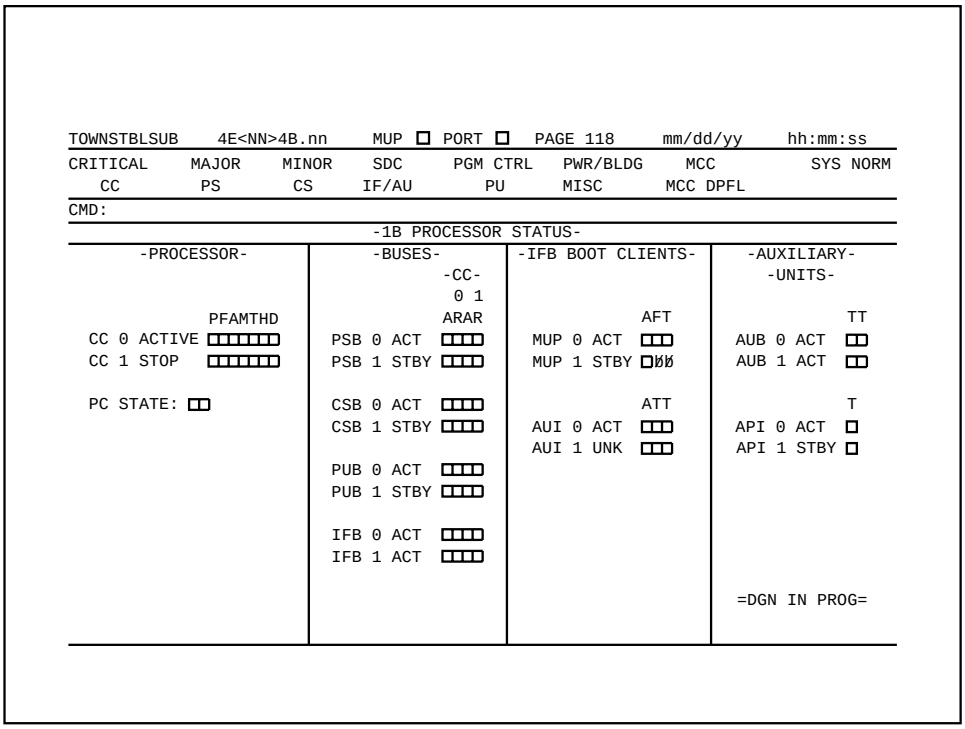
- Central Control Status (PROCESSOR)
- Processor Buses (BUSES)
  - — Program Store Bus (PSB)
  - — Call Store Bus (CSB)
  - — Peripheral Unit Bus (PUB)
  - — Interface Bus (IFB)
- IFB Client Status (IFB BOOT CLIENTS)
  - — MCC and Utility Processor (MUP)
  - — Auxiliary Unit Interface (AUI)
- Auxiliary Unit Status (AUXILIARY UNITS)
  - — Auxiliary Unit Bus (AUB)
  - — Attached Processor Interface (API)
  - — Data Unit Selector (DUS)

NOTE:
The DUS units are not functional in 4E22 and later generics. The DUS indicator will appear if the DUS units remain "equipped" in translations. The DUS indicator will not appear if the DUS units are "unequipped" in translations.

NOTE:
The digits of a numerical variable on Page 118 are represented by a square (□).

6.36 The status of each processor element is indicated with a text phrase such as ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNEQ (Unequipped), etc.

Figure 15 shows an example of the layout for Page 118.



tpa 786425/01

Figure 15. 1B Processor Status Page (Page 118)

A. Page 118 — Indicators

6.37 The following information describes the indicators associated with Page 118. The text, colors and specific circumstances under which the indicators will change are specified.

PROCESSOR

The PROCESSOR indicator is informational text identifying the processor central control area for Page 118. The indicator will appear white on black.

PFAMTHD The PFAMTHD indicator is informational text identifying the P (Power), F (Forced), A (Active), M (Match), T (Trouble), H (Halt) and D (Divorce) status and maintenance bits associated with CC 0 and CC 1. The indicator will appear white on black.

CC [0,1] The "CC [0,1]" indicator is informational text identifying CC 0 and CC 1. The indicator will appear the same color as the CC [0,1] status and maintenance bits found below.

CC [0,1] status & maintenance bits

The CC 0/1 status and maintenance bit indicators are informational text identifying the status and maintenance information for CC 0 and CC 1. The status indicator is a text phrase and the P (Power), F (Forced), A (Active), M (Match), T (Trouble), H (Halt) and D (Divorce) maintenance bits are binary digits representing specific maintenance conditions.

The text phrase and indicator color are determined by the applicable maintenance bits:

(1) When power is removed from CC 0 or CC 1, the text POWER will appear white on red.
(2) When CC 0 or CC 1 has been forced active (as part of a forced configuration), the text FORCED will appear black on purple.
(3) When CC 0 or CC 1 is the active CC, the text ACTIVE will appear black on green.
(4) When CC 0 or CC 1 is in routine matching mode, the text MATCH will appear white on blue.
(5) When the trouble CC flag in CC 0 or CC 1 is set, the text TROUBLE will appear black on red.
(6) When CC 0 or CC 1 is halted, the text STOP will appear black on red.
(7) When CC 0 or CC 1 is in an unknown state or divorced, the text UNKNOWN will appear red on yellow.

The maintenance bits (PFAMTHD) are set under 1B Processor hardware control. The value and meaning of these bits are as follows:

- If *P*=1, CC is powered on.
- If *P*=0, CC is powered off.
- If *F*=1, CC is forced.
- If *F*=0, CC is NOT forced.
- If *A*=1, CC is active.
- If *A*=0, CC is NOT active.
- If *M*=1, CC is matching.
- If *M*=0, CC is NOT matching.
- If *T*=1, TROUBLE is set for other CC.
- If *T*=0, TROUBLE is NOT set for other CC.
- If *H*=1, CC is halted.
- If *H*=0, CC is NOT halted.
- If *D*=1, CC is divorced.
- If *D*=0, CC is NOT divorced.

PC STATE digits

The PC STATE indicator is informational text identifying when Processor Configuration (PC) recovery actions are taking place. Normally, the indicator will not appear. However, when processor configuration recovery actions are being performed, the indicator will appear white on red.

The "PC STATE *digits*" 2-digit display identifies the PC state count. Normally, the PC state count is 0. When processor configuration recovery actions are being performed (PC state count greater than zero), the displayed digits will appear white on red.

BUSES The BUSES indicator is informational text identifying the bus status area for Page 118. The indicator will appear white on black.

CC The CC indicator is informational text identifying the central control. The indicator will appear white on black.

0 1 The 0 1 indicator is informational text identifying CC 0 and CC 1. The indicator will appear white on black.

ARAR The ARAR indicator is informational text identifying the Address (A) and Reply (R) bus-element connections to CC 0 and CC 1. The indicator will appear white on black.

PSB [0,1] The PSB [0,1] indicator is informational text identifying PSB 0 and PSB 1. The indicator will appear the same color as the PSB [0,1] state and status bits found below.

PSB [0,1] state & status bits

The PSB 0/1 state and status bit indicators are informational text identifying the send/receive hardware status of the program store buses. However, this status may not be the correct software status for these buses since the MUP cannot accurately interpret the hardware states into corresponding software states. Therefore, these indicators **should not** be used to determine the software status of the program store buses.

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For program store bus status, use global Poke Command 821

The program store bus state indicators are ACT (Active), STBY (Standby), and OOS (Out-Of-Service). The text and associated colors are as follows:

— ACT *wxyz* — Black on green
— STBY *wxyz* — White on blue
— OOS *wxyz* — Black on red

The ARAR status bits "*wxyz*" identify program store bus-element connections to CC 0 and CC 1, for example:

- If "*w*"=0, address bus to CC 0 is not active.
- If "*w*"=1, address bus to CC 0 is active.
- If "*x*"=0, reply bus to CC 0 is not active.
- If "*x*"=1, reply bus to CC 0 is active.
- If "*y*"=0, address bus to CC 1 is not active.
- If "*y*"=1, address bus to CC 1 is active.
- If "*z*"=0, reply bus to CC 1 is not active.
- If "*z*"=1, reply bus to CC 1 is active.

CSB [0,1] The "CSB [0,1]" indicator is informational text identifying CSB 0 and CSB 1. The indicator will appear the same color as the CSB [0,1] state and status bits found below

CSB [0,1] state & status bits

The CSB 0/1 state and status bit indicators are informational text identifying the send/receive hardware status of the call store buses. However, this status may not be the correct software status for these buses since the MUP cannot accurately interpret the hardware states into corresponding software states. Therefore, these indicators **should not** be used to determine the software status of the call store buses.

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For call store bus status, use global Poke Command 822

The call store bus state indicators are ACT (Active), STBY (Standby), and OOS (Out-Of-Service). The text and associated colors are as follows:

— ACT *wxyz* — Black on green
— STBY *wxyz* — White on blue
— OOS *wxyz* — Black on red

The ARAR status bits "*wxyz*" identify call store bus-element connections to CC 0 and CC 1. For example:

- If "*w*"=0, address bus to CC 0 is not active.
- If "*w*"=1, address bus to CC 0 is active.
- If "*x*"=0, reply bus to CC 0 is not active.
- If "*x*"=1, reply bus to CC 0 is active.
- If "*y*"=0, address bus to CC 1 is not active.
- If "*y*"=1, address bus to CC 1 is active.
- If "*z*"=0, reply bus to CC 1 is not active.
- If "*z*"=1, reply bus to CC 1 is active.

PUB [0,1] The "PUB [0,1]" indicator is informational text identifying PUB 0 and PUB 1. The indicator will appear the same color as the PUB [0,1] state and status bits found below.

PUB [0,1] state & status bits

The PUB 0/1 state and status bit indicators are informational text identifying the send/receive hardware status of the peripheral unit buses. However, this status may not be the correct software status for these buses since the MUP cannot accurately interpret the hardware states into corresponding software states. Therefore, these indicators **should not** be used to determine the software status of the peripheral unit buses.

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For pripheral unit bus status, use global Poke Command 837

The peripheral unit bus state indicators are ACT (Active), STBY (Standby), and OOS (Out-Of-Service). The text and associated colors are as follows:

— ACT *wxyz* — Black on green
— STBY *wxyz* — White on blue
— OOS *wxyz* — Black on red

The ARAR status bits "*wxyz*" identify peripheral unit bus-element connections to CC 0 and CC 1. For example:

- If "*w*"=0, address bus to CC 0 is not active.
- If "*w*"=1, address bus to CC 0 is active.
- If "*x*"=0, reply bus to CC 0 is not active.
- If "*x*"=1, reply bus to CC 0 is active.
- If "*y*"=0, address bus to CC 1 is not active.
- If "*y*"=1, address bus to CC 1 is active.
- If "*z*"=0, reply bus to CC 1 is not active.
- If "*z*"=1, reply bus to CC 1 is active.

IFB [0,1] The IFB [0,1] indicator is informational text identifying IFB 0 and IFB 1. The indicator will appear the same color as the IFB [0,1] state and status bits found below.

IFB [0,1] state & status bits

The IFB 0/1 state and status bit indicators are informational text identifying the send/receive hardware status of the interface buses. However, this status may not be the correct software status for these buses since the MUP cannot accurately interpret the hardware states into corresponding software states. Therefore, these indicators **should not** be used to determine the software status of the interface buses.

For the overall bus status, use global Poke Command 899 or TTY input message **OP:OSSUNITS**. For interface bus status, use global Poke Command 826

The interface bus state indicators are ACT (Active), STBY (Standby), and OOS (Out-Of-Service). The text and associated colors are as follows:

- ACT *wxyz* — Black on green
- STBY *wxyz* — White on blue
- OOS *wxyz* — Black on red.

The ARAR status bits "*wxyz*" identify interface bus-element connections to CC 0 and CC 1. For example:

- If "*w*"=0, address bus to CC 0 is not active.
- If "*w*"=1, address bus to CC 0 is active.
- If "*x*"=0, reply bus to CC 0 is not active.
- If "*x*"=1, reply bus to CC 0 is active.
- If "*y*"=0, address bus to CC 1 is not active.
- If "*y*"=1, address bus to CC 1 is active.
- If "*z*"=0, reply bus to CC 1 is not active.
- If "*z*"=1, reply bus to CC 1 is active.

IFB BOOT CLIENTS

The IFB BOOT CLIENTS indicator is informational text identifying the interface bus client area of Page 118. The indicator will appear white on black.

AFT

The AFT indicator is informational text identifying the Active (A), Forced (F) and Trouble (T) maintenance status bits. The indicator will appear white on black.

MUP [0,1] The MUP [0,1] indicator is informational text identifying MUP 0 and MUP 1. The indicator will appear the same color as the MUP [0,1] status and maintenance bits found below.

MUP [0,1] status and maintenance bits

The "MUP 0/1 status and maintenance bit" indicators are informational text identifying the status of MUP 0 and MUP 1. The status indicator is a text phrase and the A (Active), F (Forced) and T (Trouble) maintenance bits are binary digits representing specific maintenance conditions.

The MUP status text phrases are ACT (Active), STBY (Standby), OOS (Out-Of-Service) and UNK (Unknown). The text and associated colors are as follows:

— ACT *aft* — Black on green
— STBY *aft* — White on blue
— OOS *aft* — Black on red
— UNK *aft* — Red on yellow.

The maintenance bits "*aft*" are single-digit values set under 1B Processor hardware control. For example:

- If "*a*"=1, associated MUP is active.
- If "*f*"=1, associated MUP is forced.
- If "*t*"=1, associated MUP trouble flag set.

The MCC design will not permit the F (Forced) or T (Trouble) bits to be known for the inactive MUP. Therefore, the force and trouble bits will be blank for the inactive MUP.

ATT The ATT indicator is informational text identifying the active (A), trouble - bus 0 (T) and trouble - bus 1 (T) maintenance bits. The indicator will appear white on black.

AUI [0,1] The "AUI [0,1]" indicator is informational text identifying AUI 0 and AUI 1. The indicator will appear the same color as the AUI [0,1] status and maintenance bits found below.

AUI [0,1] status and maintenance bits

The "AUI 0/1 status and maintenance bit" indicators are informational text identifying the status of AUI 0 and AUI 1. The status indicator is a text phrase and the A (active), T (trouble - bus 0) and T (trouble - bus 1) maintenance bits are

binary digits representing specific maintenance conditions.

The AUI status text phrases are ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNK (Unknown), and UNAV (Unavailable). The text and associated colors are as follows:

— ACT *att* — Black on green
— STBY *att* — White on blue
— OOS *att* — Black on red
— UNK *att* — Red on yellow
— UNAV *att* — Black on yellow.

The maintenance bits "*att*" are single-digit values set under 1B Processor hardware control. For example:

- If "*a*"=1, associated AUI is active.
- If "first *t*"=1, associated AUI has trouble on bus 0.
- If "second *t*"=1, associated AUI has trouble on bus 1.

AUXILIARY UNITS

The AUXILIARY UNITS indicator is informational text identifying the auxiliary units area of Page 118. The indicator will appear white on black.

TT The TT indicator is informational text identifying the T (trouble - bus 0) and T (trouble - bus 1) maintenance bits. The indicator will appear white on black.

AUB [0,1] The AUB [0,1] indicator is informational text identifying AUB 0 and AUB 1. The indicator will appear the same color as the AUB [0,1] status and maintenance bits found below.

AUB [0,1] status and maintenance bits

The "AUB 0/1 status and maintenance bit" indicators identify the status of AUB 0 and AUB 1. The status indicator is a text phrase and the T (trouble - bus 0) and T (trouble - bus 1) maintenance bits are binary digits representing specific status and maintenance conditions.

The AUB status text phrases are ACT (Active), OOS (Out-Of-Service) and UNK (Unknown). The text and associated colors are as follows:

— ACT *tt* — Black on green
— OOS *tt* — Black on red
— UNK *tt* — Red on yellow.

The maintenance bits "*tt*" are single-digit values set under 1B Processor hardware control. For example:

- If "first *t*"=1, AUI 0 has trouble on associated AUB.
- If "second *t*"=1, AUI 1 has trouble on associated AUB.

T The "T" indicator is informational text identifying the T (trouble) maintenance status bits. The indicator will appear white on black.

API [0,1] The "API [0,1]" indicator is informational text identifying API 0 and API 1. The indicator will appear the same color as the API [0,1] status and maintenance bit found below.

API [0,1] status & maintenance bit

The API 0/1 status and maintenance bit indicators are informational text identifying the status of API 0 and API 1. The status indicator is a text phrase and the T (trouble) maintenance bit is a binary digit representing specific maintenance conditions.

The API status text phrases are ACT (Active), STBY (Standby), OOS (Out-Of-Service), UNK (Unknown), and UNAV (Unavailable). The text and associated colors are as follows:

— ACT *t* — Black on green
— STBY *t* — White on blue
— OOS *t* — Black on red
— UNK *t* — Red on yellow
— UNAV *t* — Black on yellow.

The maintenance bit "*t*" is a single-digit value set under 1B Processor program control. For example, if "*t*"=1, the associated API has trouble.

DUS [0,1] The DUS [0,1] indicator is informational text identifying DUS 0 and DUS 1. The DUS units are not functional in 4E22 and later generics. The DUS indicator will appear the same colors as the DUS [0,1] status indicator found below if the DUS units remain "equipped" in translations.

The DUS [0,1] indicator will not appear if the DUS units are "unequipped" in translations.

DUS [0,1] status

The DUS [0,1] status indicator is informational text identifying the status of DUS 0 and DUS 1. The DUS units are not functional in 4E22 and later generics. The status indicator is a text phrase that will appear if the DUS units remain "equipped" in translations.

The DUS [0,1] status indicator will not appear if the DUS units are "unequipped" in translations.

The DUS status text phrases are ACT (Active), STBY (Standby), OOS (Out-of-service), UNK (Unknown), and UNAV (Unavailable). The text and associated colors are as follows:

- ACT — Black on green
- STBY — White on blue
- OOS — Black on red
- UNK — Red on yellow
- UNAV — Black on yellow

DGN IN PROG

The DGN IN PROG indicator is informational text identifying when any system unit is under diagnostic control. Normally, the indicator will not appear. However, when diagnostics are in progress, the indicator will appear yellow on black.

B. Page 118 — Poke Commands

6.38 There are no poke commands associated with Page 118. Global pokes can be used on page 118.

DDI Key Options (Page 119)

6.39 The Direct Data Insert (DDI) keys can be set and cleared from the Direct Data Insert (DDI) Key Options Page (Page 119). The DDI Key Options Page (Page 119) is invoked by entering Poke Command 119.

6.40 Page 119 consists of the following two-page format:

- Modified Recovery Action DDI Key Assignments (Figure 16)
- Inhibit Interrupts DDI Key Assignments (Figure 17).

6.41 Poke Command 499 (on each page) is used to toggle between the two pages. The DDI Key Options Page also provides the poke commands necessary to set and reset the DDI key assignments.

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □ PORT □   PAGE 119     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG     MCC          SYS NORM
   CC          PS        CS     IF/AU        PU       MISC       MCC DPFL
CMD:
                    499 - TOGGLE MRA / INHIBIT INTERRUPT OPTIONS
                   -MODIFY RECOVERY ACTIONS DDI KEY ASSIGNMENTS-
       401,xx,xx,.... - SET xx; 400,xx,xx,... - RESET xx; 402 - RESET ALL
  00 SET ALL INH                           16 ZERO ALL MEMORY
  01 RB RC TO TAPE 1                       17 SKIP HASHSUM CALCULATION
  02 RB RC TO TAPE 2                       18 BYPASS CC SANITY TESTS
  03 RB RC NO OF ORDRS IN DIS 1  (940)     19 RESERVED
  04 RB RC TO ORNU IN DIS 1  (940)         20 INH MAP AUDITS
  05 CLEAR SPECIFIC DISK AREAS             21 INH STORE ACCESS TESTS
  06 CLEAR NTWK MGMT CONTROLS              22 SPARE
  07 INITIALIZE TRK OOS LIST               23 ALW DUPLEX APS FAILURE IN SR
  08 RESERVED                              24 SKIP MUP RESTART DURING PC/SR
  09 RESERVED                              25 ALW MUP SUPERVISOR MODE UTIL SR
  10 RESERVED                              26 INH IFB ACCESS TEST
  11 RST DUPLEX FAILED CONTRS              27 INH AUTOMATIC DIAGNOSTICS
  12 SPARE                                 28 SPARE
  13 SPARE                                 29 SPARE
  14 ALLOW DUPLEX FAILED PUBB              30 SPARE
  15 RESERVED                              31 SPARE
```

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Figure 16. MRA DDI Key Assignments Page (Page 119)

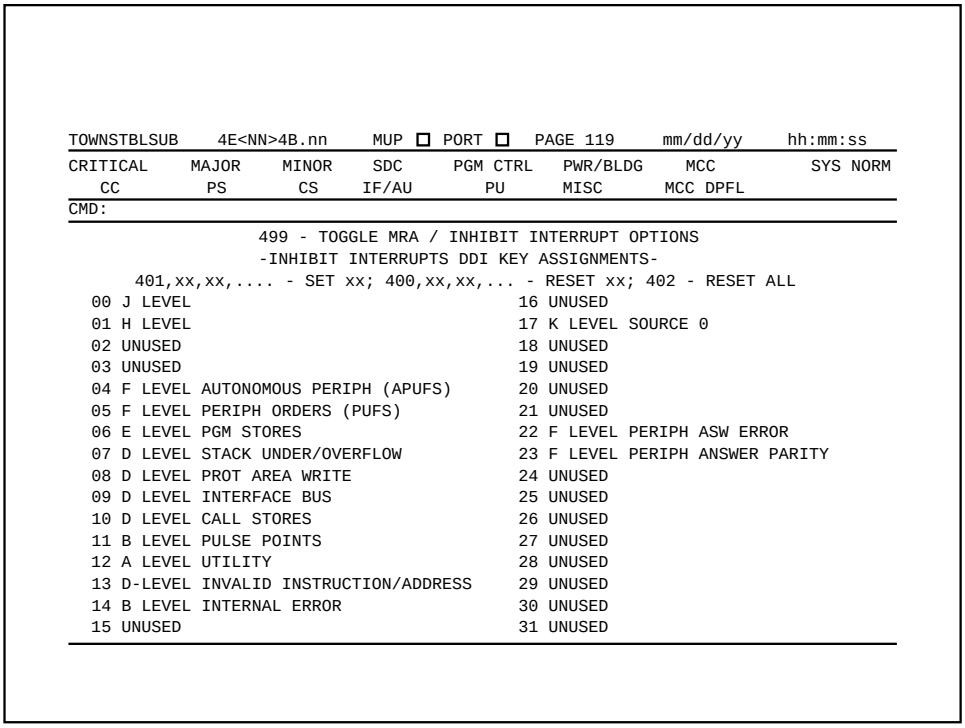

Figure 17. Inhibit Interrupts DDI Key Assignments Page (Page 119)

A. Page 119 — Indicators

6.42 The following information describes the indicators associated with Page 119. The text, colors and specific circumstances under which the indicators will change are specified.

SET xx; The "SET xx" indicator is informational text associated with Poke Command 401 used to set specified DDI keys. The indicator will appear white on black.

RESET xx The "RESET xx" indicator is informational text associated with Poke Command 400 used to reset specified DDI keys. The indicator will appear white on black.

RESET ALL The RESET ALL indicator is informational text associated with Poke Command 402 used to reset (clear) all DDI keys. The indicator will appear white on black.

DDI Page Title

The DDI Page Title is informational text identifying the current Page 119 being displayed.

The page title on the initial Page 119 is -MODIFY RECOVERY ACTIONS DDI KEY ASSIGNMENTS- and will appear white on black. This is commonly referred to as the Modify Recovery Action (MRA) format.

The page title on the second page of Page 119 is -INHIBIT INTERRUPTS ACTIONS DDI KEY ASSIGNMENTS- and will appear white on black. This is commonly referred to as the Inhibit Interrupts (INH INT) format.

The default format is the Modify Recovery Action (MRA) page.

DDI Keys 00 - 31

These indicators identify the status of DDI Keys 00-31. Each DDI key indicator has a dual function depending on the Page 119 format (MRA or INH INT). The color of each DDI key indicator is white on black in its default states (state 1 for MRA and state 3 for INH INT). Likewise, the color of each DDI key indicator is black on white in its alternate states (state 2 for MRA and state 4 for INH INT).

When Page 119 is in the MRA format, each DDI key indicator (00-31) will toggle between states 1 and 2 as its corresponding poke command is entered. When Page 119 is in the INH INT format, each DDI key indicator (00-31) will toggle between states 3 and 4 as its corresponding poke command is entered.

For example, DDI Key 00 is labeled SET ALL INH in its default state 1 of the MRA format and will appear white on black. When its corresponding Poke Command (00) is entered, the indicator toggles to state 2, is labeled CLEAR ALL INH and will appear black on white. Likewise, DDI Key 00 is labeled J LEVEL in its default state 3 of the INH INT format and will appear white on black. When its corresponding Poke Command (00) is entered, the indicator toggles to state 4, is labeled J LEVEL INH and will appear black on white.

A description of DDI keys 00 through 31 is provided in Table P. When the following terms are used in the table, their meanings are defined as:

Reserved	The term "Reserved" implies that a function has been assigned to the key, but the function will not be deployed in field software releases.
Spare	The term "Spare" implies that no function has been assigned to the key and that there are no known difficulties associated with assigning a function to the key.
Unused	The term "Unused" implies that no function has been assigned to the key and that it is not currently feasible to assign a function to the key.

Table P. DDI Key Assignments

Key	Format	States	Text
00	MRA	1,2	00 SET ALL INH
	INH INT	3,4	00 J LEVEL
01	MRA	1,2	01 RB RC TO TAPE 1
	INH INT	3,4	01 H LEVEL
02	MRA	1,2	02 RB RC TO TAPE 2
	INH INT	3,4	02 UNUSED
03	MRA	1,2	03 RB RC NO OF ORDRS IN DIS 1 (940)
	INH INT	3,4	03 UNUSED
04	MRA	1,2	04 RB RC TO ORNU IN DIS 1 (940)
	INH INT	3,4	04 F LEVEL AUTONOMOUS PERIPH (APUFS)
05	MRA	1,2	05 CLEAR SPECIFIC DISK AREAS
	INH INT	3,4	05 F LEVEL PERIPH ORDERS (PUFS)
06	MRA	1,2	06 CLEAR NTWK MGMT CONTROLS
	INH INT	3,4	06 E LEVEL PGM STORES
07	MRA	1,2	07 INITIALIZE TRK OOS LIST
	INH INT	3,4	07 D LEVEL STACK UNDER/OVERFLOW
08	MRA	1,2	08 RESERVED
	INH INT	3,4	08 D LEVEL PROT AREA WRITE
09	MRA	1,2	09 RESERVED
	INH INT	3,4	09 D LEVEL INTERFACE BUS
10	MRA	1,2	10 RESERVED
	INH INT	3,4	10 D LEVEL CALL STORES
11	MRA	1,2	11 RST DUPLEX FAILED CONTRS
	INH INT	3,4	11 B LEVEL PULSE POINTS
12	MRA	1,2	12 SPARE
	INH INT	3,4	12 A LEVEL UTILITY
13	MRA	1,2	13 SPARE
	INH INT	3,4	13 D-LEVEL INVALID INSTRUCTION/ADDRESS
14	MRA	1,2	14 ALLOW DUPLEX FAILED PUBB
	INH INT	3,4	14 B LEVEL INTERNAL ERROR
15	MRA	1,2	15 RESERVED
	INH INT	3,4	15 UNUSED
16	MRA	1,2	16 ZERO ALL MEMORY
	INH INT	3,4	16 UNUSED
17	MRA	1,2	17 SKIP HASHSUM CALCULATION
	INH INT	3,4	17 K LEVEL SOURCE 0
18	MRA	1,2	18 BYPASS CC SANITY TESTS
	INH INT	3,4	18 UNUSED
19	MRA	1,2	19 RESERVED
	INH INT	3,4	19 UNUSED
20	MRA	1,2	20 INH MAP AUDITS
	INH INT	3,4	20 UNUSED
21	MRA	1,2	21 INH STOR ACCESS TESTS
	INH INT	3,4	21 UNUSED
22	MRA	1,2	22 SPARE
	INH INT	3,4	22 F LEVEL PERIPH ASW ERROR
23	MRA	1,2	23 ALW DUPLEX APS FAILURE IN SR
	INH INT	3,4	23 F LEVEL PERIPH ANSWER PARITY

Table P. DDI Key Assignments (Contd)

Key	Format	States	Text
24	MRA	1,2	24 SKIP MUP RESTART DURING PC/SR
	INH INT	3,4	24 UNUSED
25	MRA	1,2	25 ALW MUP SUPERVISOR MODE UTIL SR
	INH INT	3,4	25 UNUSED
26	MRA	1,2	26 INH IFB ACCESS TESTS
	INH INT	3,4	26 UNUSED
27	MRA	1,2	27 INH AUTOMATIC DIAGNOSTICS
	INH INT	3,4	27 UNUSED
28	MRA	1,2	28 SPARE
	INH INT	3,4	28 UNUSED
29	MRA	1,2	29 SPARE
	INH INT	3,4	29 UNUSED
30	MRA	1,2	30 SPARE
	INH INT	3,4	30 UNUSED
31	MRA	1,2	31 SPARE
	INH INT	3,4	31 UNUSED

TOGGLE MRA / INHIBIT INTERRUPT OPTIONS

The TOGGLE MRA / INHIBIT INTERRUPT OPTIONS indicator is informational text identifying the toggle function of Page 119. The indicator will appear white on black.

B. Page 119 — Poke Commands

6.43 The following information describes the function of each Page 119 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels.

NOTE:
Poke Commands in the 400 series are specific to Page 119. Poke Commands 400,401, and 402 are valid on the EAI Page, also. Global poke commands can be executed from any page.

401,xx,xx,... SET xx

Poke Command 401 sets one or more bits in the DDI register associated with specified DDI keys. Optional inputs to Poke Command 401 must conform to the following:

- Up to 16 two-digit option values can be entered as long as each option value is followed by a comma, for example, **401,10,03,14**.
- All options must be two digits. Otherwise, the command will be rejected.
- All options must be in the range 00 through 31. Otherwise, the command will be rejected.

If Poke Command 401 is rejected for any reason, no DDI keys will be set.

400,xx,xx,... RESET xx

Poke Command 400 clears one or more bits in the DDI register associated with specified DDI keys. The criteria for accepting or rejecting Poke Command 400 is the same as previously described for Poke Command 401.

If Poke Command 401 is rejected, no DDI keys will be reset.

402 - RESET ALL

Poke Command 402 causes all 32 bits in the DDI register to be reset.

499 - TOGGLE MRA / INHIBIT INTERRUPT OPTIONS

Poke Command 499 toggles the DDI Key Assignment menu between the Modify Recovery Action (MRA) option and the Inhibit Interrupt (INH INT) option.

When a user specifies an option using Poke Command 400, 401 or 402, the user is merely setting or clearing one or more bits in a register. The register can be used to either modify recovery actions or inhibit the operation of several different interrupt types. The user identifies which way the register should be *used* by selecting Poke Command 83 (INHIBIT INT) or Poke Command 84 (MODIFY RECV) prior to selecting Poke Command 01 (HARD A) or Poke Command 02 (SOFT A) on the EAI Page.

The Page 119 menus only provide a reference to the functions assigned to the various register bits under the appropriate circumstances. The menus do not dictate or prevent the use of either Poke Command 83 or 84, nor do Poke Commands 83 and 84 dictate or prevent the use of Poke Command 499 on Page 119 to alternate menus. For example, if Page 119 is set to the MRA format the MCC will still permit the entry of Poke Command 83 (INHIBIT INT).

Data Display Page (Page 120)

6.44 The Data Display Page provides memory displays, data insert sections and utility functions. The Data Display Page is invoked by entering Poke Command 120.

6.45 The Data Display Page (Figure 18) includes the following functional sections:

- Display Section 1
- Write/GCP Allowed
- Display Section 2
- Data Insert Section 1
- Data Insert Section 2
- Various Indicators/Alarms.

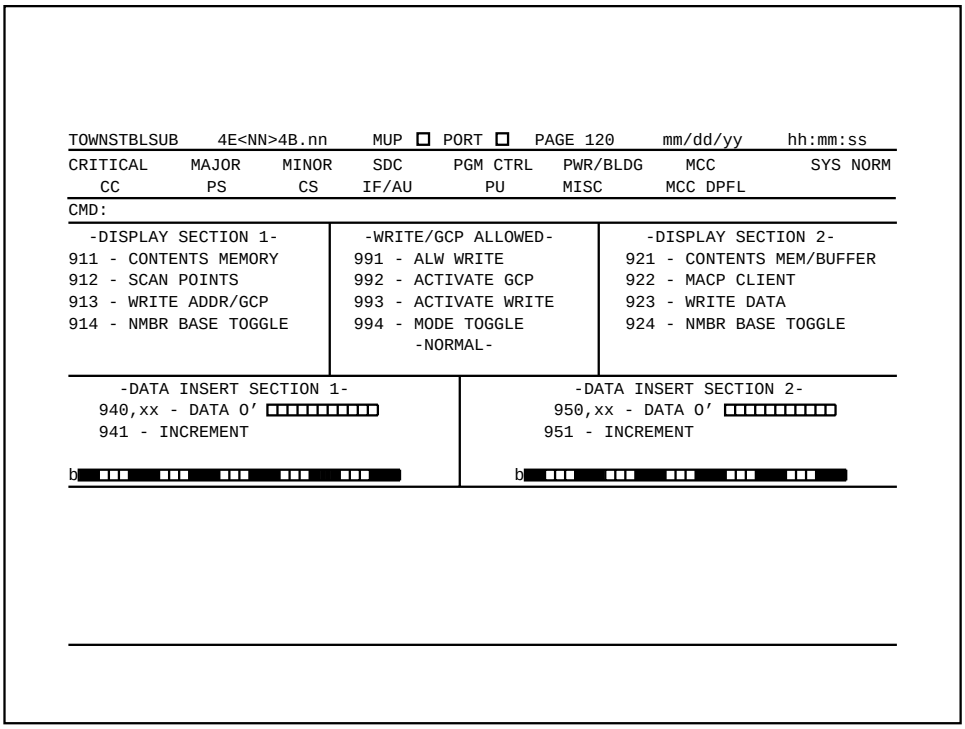

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Figure 18. Data Display Page (Page 120)

NOTE:
The digits of a numerical variable on Page 120 are represented by a square (□).

A. Page 120 — Indicators

6.46 The following information describes the indicators associated with Page 120. The text, colors and specific circumstances under which the indicators will change are specified.

DISPLAY SECTION 1

The DISPLAY SECTION 1 indicator is informational text identifying the Display Section 1 area of Page 120. The indicator will appear white on black.

CONTENTS MEMORY

The CONTENTS MEMORY indicator is informational text identifying that Data Display 1 is to show the contents of a selected memory address. Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white. The indicator is affected by Poke Commands 911, 912 and 913.

SCAN POINTS The SCAN POINTS indicator is informational text identifying that Data Display 1 is to show a selected scan point. Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white. The indicator is affected by Poke Commands 911, 912 and 913.

WRITE ADDR/GCP

The WRITE ADDR/GCP indicator is informational text identifying that Data Display 1 is to show the address of a memory location or Generated Control Pulse (GCP) to be written into. Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white. The indicator is affected by Poke Commands 911, 912 and 913.

NMBR BASE TOGGLE 1

The NMBR BASE TOGGLE 1 indicator is informational text identifying the number base (ASCII, binary, octal, decimal or hexadecimal) in which Data Display 1 data will be displayed in. The indicator will appear white on black.

DISPLAY SECTION 2

The DISPLAY SECTION 2 indicator is informational text identifying the Display Section 2 area of Page 120. The indicator will appear white on black.

CONTENTS MEM/BUFFER

The CONTENTS MEM/BUFFER indicator is informational text identifying that Data Display 2 is to display the contents of a selected memory address or a buffer bus register. Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white. The indicator is affected by Poke Commands 921, 922 and 923.

MACP CLIENT

The MACP CLIENT indicator is informational text identifying that Data Display 2 is to display the contents of an MACP client. Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white. The indicator is affected by Poke Commands 921, 922 and 923.

WRITE DATA The WRITE DATA indicator is informational text identifying that Data Display 2 is to display the value of data to be written into a memory address or Generated Control Pulse (GCP). Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white. The indicator is affected by Poke Commands 921, 922 and 923.

NMBR BASE TOGGLE 2

The NMBR BASE TOGGLE 2 indicator is informational text identifying the number base (ASCII, binary, octal, decimal or hexadecimal) that Data Display 2 data will be displayed in. The indicator will appear white on black.

DATA INSERT SECTION 1

The DATA INSERT SECTION 1 indicator is informational text identifying the Data Insert Section 1 area of Page 120. The indicator will appear white on black.

DATA Display

The DATA Display indicator is informational text identifying the parameter last entered or changed using Poke Command 940 or 941. The indicator will appear white on black.

Data Insert Display 1

The Data Insert Display 1 indicator is an informational display located in the lower section of the Data Insert Section 1 area. The display indicator identifies the results of Poke Commands 911, 912 or 913. Under switch control, the data in the display can be shown in any of the following formats:

- ASCII characters
- Number bases: binary, octal, decimal or hexadecimal.

The default mode is determined by the *4ESS* Switch.

When the ASCII format is selected, the character **A'** will appear at the left of the display and the data will be displayed as ASCII characters.

When the binary format is selected, the character **B'** will appear at the left of the display and the data will be displayed as a 32-digit binary number. When displayed in binary, the bit pattern will be displayed in alternating colors of white on black and yellow on black every three bits.

When the octal format is selected, the character **O'** will appear at the left of the display and the data will be displayed as an 11-digit octal number.

When the decimal format is selected, the character **D'** will appear at the left of the display and the data will be displayed as a 10-digit decimal number.

When the hexadecimal format is selected, the character **X'** will appear at the left of the display and the data will be displayed as an 8-digit hexadecimal number.

The display data is updated as change occurs in the underlying data but not more frequently than every 2 seconds.

The indicator is affected by Poke Command 914.

INCREMENT The INCREMENT indicator is informational text associated with Poke Command 941 used to increment the number displayed in the Data Insert Section 1 display. The indicator will appear white on black.

DATA INSERT SECTION 2

The DATA INSERT SECTION 2 indicator is informational text identifying the Data Insert Section 2 area of Page 120. The indicator will appear white on black.

DATA Display

The "DATA Display" indicator is informational text identifying the parameter last entered or changed using Poke Command 950 or 951. The indicator will appear white on black.

Data Insert Display 2

The "Data Insert Display 2" indicator is an informational display located in the lower section of the Data Insert Section 2 area. The display indicator identifies the results of Poke Commands 921, 922 or 923. Under switch control, the data in the display can be shown in any of the following formats:

- ASCII characters
- Number bases: binary, octal, decimal or hexadecimal.

The default mode is determined by the *4ESS* Switch.

When the ASCII format is selected, the character **A'** will appear at the left of the display and the data will be displayed as ASCII characters.

When the binary format is selected, the character **B'** will appear at the left of the display and the data will be displayed as a 32-digit binary number. When displayed in binary, the bit pattern will be displayed in alternating colors of white on black and yellow on black every three bits.

When the octal format is selected, the character **O'** will appear at the left of the display and the data will be displayed as an 11-digit octal number.

When the decimal format is selected, the character **D'** will appear at the left of the display and the data will be displayed as a 10-digit decimal number.

When the hexadecimal format is selected, the character **X'** will appear at the left of the display and the data will be displayed as an 8-digit hexadecimal number.

The display number is updated as change occurs in the underlying data but not more frequently than every 2 seconds.

The indicator is affected by Poke Command 924.

INCREMENT The INCREMENT indicator is informational text associated with Poke Command 951 used to increment the number displayed in the Data Insert Section 2 display. The indicator will appear white on black.

WRITE/GCP ALLOWED

The WRITE/GCP ALLOWED indicator is informational text identifying when GCP and data writes of call store or program store addresses are allowed. Normally, the indicator will not appear. However, when present, the indicator will appear white on red. The indicator is displayed and removed under MUP and 1B Processor software control.

ALW WRITE The ALW WRITE indicator is informational text identifying when memory writes are permitted. Normally, the indicator will appear white on black. However, when selected, the indicator will appear black on white.

ACTIVATE GCP

The ACTIVATE GCP indicator is informational text associated with Poke Command 992 used to activate the GCP address identified in Display 1. Normally, the indicator will not appear. However, when present, the indicator will appear white on black.

ACTIVATE WRITE

The ACTIVATE WRITE indicator is informational text associated with Poke Command 993 used to write data to memory at the address in Display 1. Normally, the indicator will appear white on black. However, when a procedure error occurs, the indicator will appear white on red.

MODE TOGGLE

The MODE TOGGLE indicator is informational text associated with Poke Command 994 used to toggle interference modes. The indicator is displayed only when the WRITE/GCP ALLOWED indicator is active and will appear white on black.

Interference Mode

The Interference Mode indicator is informational text identifying that the write mode has been selected using Poke Command 994 (MODE TOGGLE). Normally, the indicator will not appear. However, when present, the indicator will appear black on white. The indicator has five states. The five states are identified in Table Q.

Table Q. Data Display Page Interference Mode Indicators

State	Text
1	No Text (Normal State)
2	=NORMAL=
3	=CONTROL=
4	=MAINTENANCE=
5	=MTCE & CONTROL=

B. Page 120 — Poke Commands

6.47 The following information describes the function of each Page 120 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels.

NOTE:
Poke Commands in the 900 series are global poke commands and can be executed from any page.

911 - CONT MEMORY

Poke Command 911 causes the contents of the address shown in Data Insert Section 1 area to be displayed. Poke Command 911 will cause the CONT MEMORY indicator to be selected and the SCAN POINT and WRITE ADDR/GCP indicators to be retired.

912 - SCAN POINTS

Poke Command 912 causes the state of the scan point shown in Data Insert Section 1 area to be displayed. Poke Command 912 will cause the SCAN POINTS indicator to be selected and the CONTENTS MEMORY and WRITE ADDR/GCP indicators to be

retired.

913 - WRITE ADDR/GCP

Poke Command 913 causes the address shown in Data Insert Section 1 area to be displayed. Poke Command 913 will cause the WRITE ADDR/GCP indicator to be selected and the CONTENTS MEMORY and SCAN POINTS indicators to be retired.

914 - NMBR BASE TOGGLE

Poke Command 914 cycles the modes of the data displayed in Data Insert Section 1 display area as either ASCII, binary, octal, decimal or hexadecimal.

921 - CONT MEM/BUFFER

Poke Command 921 causes the contents of the address shown in Data Insert Section 2 area to be displayed. Poke Command 921 also causes the CONTENTS MEM/BUFFER indicator to be selected and the MACP CLIENT and WRITE DATA indicators to be retired.

922 - MACP CLIENT

Poke Command 922 causes information regarding the MACP CLIENT shown in Data Insert Section 2 area to be displayed. Poke Command 922 also causes the MACP CLIENT indicator to be selected and the CONTENTS MEM/BUFFER and WRITE DATA indicators to be retired.

923 - WRITE DATA

Poke Command 923 causes the data shown in Data Insert Section 2 area to be displayed. Poke Command 923 also causes the WRITE DATA indicator to be selected and the CONTENTS MEM/BUFFER and MACP CLIENT indicators to be retired.

924 - NMBR BASE TOGGLE

Poke Command 924 cycles the mode of the data displayed in Data Insert Section 2 display area as either ASCII, binary, octal, decimal or hexadecimal.

940 - DATA INSERT

Poke Command 940 allows for the insertion of data into Data Insert Section 1 area. Poke Command 940 will be rejected ("?D" acknowledgment) if a numerical parameter of 1 to 11 octal digits is not entered. If the parameter has fewer than 11 digits, leading zeroes will be assumed. The parameter is right-adjusted as the number part of the Data Insert Section 1 indicator. The entries **940,137777777777** and **940,1** (equivalent to **940,00000000001**) are both examples of valid entries.

With 4E21 and later Generic applications, the user is able to specify a 24-bit address or a 30-bit address using Poke Command 940. Bit 30 of the address will identify if a 24-bit address or a 30-bit address will accompany Poke Command 940. If bit 30 (binary digit 31) of the address associated with Poke Command 940 is set to 1, the 1B

Processor software will expect a 30-bit address (binary digits 0-29) to be specified by the user. Otherwise, if bit 30 (binary digit 31) is not set to 1, the 1B software will expect a 24- bit address (binary digits 0-23) to be specified by the user. When a 24-bit address is specified, the 1B Processor software will automatically add the Target Address Register (TAR) bits (binary digits 24-29) to convert the address to the expected 30 bits.

NOTE:
If Poke Command 911 or 913 is entered with more than 8 octal digits and bit position 30 (Binary digit 31) is not set to 1, an INVALID ADDRESS message will be received.

As examples:

(1) To access non-extended store address 7746660007 in Display 1, the user could:

(1) Enter Poke Command **940,17746660007**

(2) Enter Poke Command **911**

(3) Poke Command 940 display will contain 17746660007

(4) Data associated with address entered with Poke Command 940 will be shown in Data Insert Section 1 - Display 1.

Or

(1) Enter Poke Command **940,6660007**

(2) Enter Poke Command **911**

(3) Poke Command 940 display will contain 6660007

(4) Data associated with address entered with Poke Command 940 will be shown in Data Insert Section 1 - Display 1.

(2) To access extended store address 0006660007, the user would:

(1) Enter Poke Command **940,10006660007**

(2) Enter Poke Command **911**

(3) Poke Command 940 display will contain 10006660007

(4) Data associated with address entered with Poke Command 940 will be shown in Data Insert Section 1 - Display 1.

941 - INCREMENT

Poke Command 941 increments the DATA indicator located in the Data Insert Section 1 area by one.

950 - DATA INSERT

Poke Command 950 allows for the insertion of data into Data Insert Section 2 area. Poke Command 950 will be rejected (?D acknowledgment) if a numerical parameter of 1 to 11 octal digits is not entered. If the parameter has fewer than 11 digits, leading zeroes will be assumed. The parameter is right-adjusted as the number part of the Data Insert Section 2 indicator. The entries **950,137777777777** and **950,1** (equivalent to **950,00000000001**) are both examples of valid entries.

With 4E21 and later Generic applications, the user is to specify a 24-bit address or a 30-bit address using Poke Command 950. Bit 30 of the address will identify if a 24-bit address or a 30-bit address will accompany Poke Command 950. If bit 30 (binary digit 31) of the address associated with Poke Command 950 is set to 1, the 1B Processor software will expect a 30-bit address (binary digits 0-29) to be specified by the user. Otherwise, if bit 30 (binary digit 31) is not set to 1, the 1B software will expect a 24- bit address (binary digits 0-23) to be specified by the user. When a 24-bit address is specified, the 1B Processor software will automatically add the Target Address Register (TAR) bits (binary digits 24-29) to convert the address to the expected 30 bits.

NOTE:
If Poke Command 921 is entered with more than 8 octal digits and bit position 30 (binary digit 31) is not set to 1, an INVALID ADDRESS message will be received.

As examples:

(1) To access non-extended store address 7746660007 in Display 2, the user could:

(1) Enter Poke Command **950,17746660007**

(2) Enter Poke Command **921**

(3) Poke Command 950 display will contain 17746660007

(4) Data associated with address entered with Poke Command 950 will be shown in Data Insert Section 2 - Display 2.

Or

(1) Enter Poke Command **950,6660007**

(2) Enter Poke Command **921**

(3) Poke Command 950 display will contain 6660007

(4) Data associated with address entered with Poke Command 950 will be shown in Data Insert Section 2 - Display 2.

(2) To access extended store address 0006660007, the user would:

(1) Enter Poke Command **950,10006660007**

(2) Enter Poke Command **921**

(3) Poke Command 950 display will contain 10006660007

(4) Data associated with address entered with Poke Command 950 will be shown in Data Insert Section 2 - Display 2.

951 - INCREMENT

Poke Command 951 increments the DATA indicator located in the Data Insert Section 2 area by one.

991 - ALW WRITE

If the "allow write" function has not been selected, Poke Command 991 will select the "allow write" function enabling writes to be made to main memory on a word-by-word basis.

If the "allow write" function has been selected, Poke Command 991 will release the function. The use of Poke Command 991 is equivalent to the LOAD: TTY input message.

992 - ACTIVATE GCP

Poke Command 992 causes the *4ESS* Switch to activate the GCP address identified in Display 1. Poke Command 992 will be rejected if the WRITE/GCP ALLOWED indicator has not been activated.

993 - ACTIVATE WRITE

Poke Command 993 causes the data shown in Data Insert Section 2 - Display 2 to be written into the word of memory at the address identified in Data Insert Section 1 - Display 1. Poke Command 993 will be rejected if the WRITE/GCP ALLOWED, WRITE ADDR/GCP and WRITE DATA indicators are not selected. Poke Command 993 will, also, be rejected if the ALW WRITE, WRITE ADDR/GCP and WRITE DATA indicators are selected.

Examples:

(1) To write a value of 44 into non-extended store address 7746660007, the user would:

(1) Enter Poke Command **940,17746660007**

(2) Poke Command 940 display will contain 17746660007

(3) Enter Poke Command **950,44**

(4) Poke Command 950 display will contain 44

(5) Enter Poke Command **911**

(6) Enter Poke Command **923**

(7) Enter Poke Command **991**

(8) Enter Poke Command **994**

(9) Content of address 7746660007 will be changed to 44.

(2) To write a value of 44 into extended store address 6660007, the user would:

(1) Enter Poke Command **940,10006660007**

(2) Poke Command 940 display will contain 10006660007

(3) Enter Poke Command **950,44**

(4) Poke Command 950 display will contain 44

(5) Enter Poke Command **916**

(6) Enter Poke Command **923**

(7) Enter Poke Command **991**

(8) Enter Poke Command **994**

(9) Content of address 6660007 will be changed to 44.

994 - MODE TOGGLE

When the WRITE/GCP ALLOWED indicator is present, Poke Command 994 causes the *Write Mode* indicator to cycle through states 2, 3, 4 and 5. When the WRITE/GCP ALLOWED indicator is not present, Poke Command 994 will be rejected.

Dead Start (Page 1990)

6.48 The Dead Start Page (Page 1990) is designed to allow the highly experienced, expert user the ability to restore the 1B Processor hardware back to a sane environment if automatic and manual recovery efforts via the EAI Page have not been successful. The Dead Start Page is invoked by entering Poke Command 1990.

6.49 The Dead Start Page (Figure 19) includes the following functional sections:

- CC Control
- CC Register Access
- MUP Test
- Miscellaneous
- Status
- 1B Processor Test
- Various Status Indicators/Alarms.

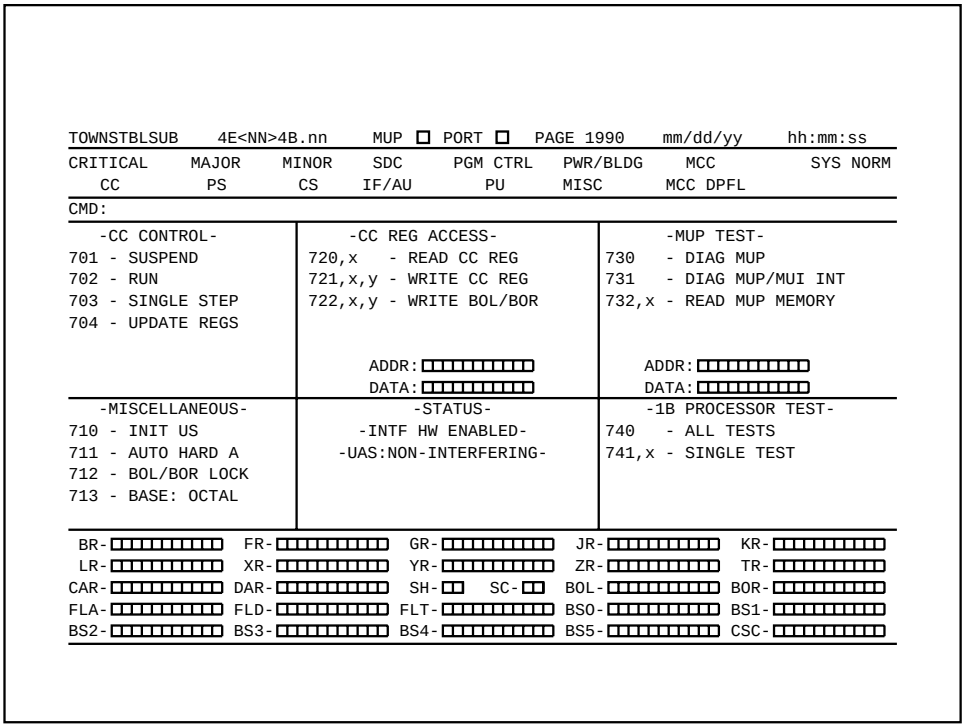

Figure 19. Dead Start Page (Page 1990)

6.50 Page 1990 is a partial replacement for the Portable Recovery Test Set (PORTS), which is an external testing device used to recover the 1A Processor. Page 1990 does not provide matchers and trace capabilities.

The Dead Start Page assists the experienced user in performing the following activities:

- Controlling CC execution
- Reading and writing to buffer bus registers
- Executing 1B Processor BOOT ROM tests
- Reading the MCC Utility Processor memory
- Diagnosing the sanity of the MUP and the MCC Utility Interface.

NOTE:
Although it is not the purpose or intent of this document to define exact user skills or job functions, it is generally assumed that the user of the Dead Start Page (Page 1990) is someone who is highly experienced in the operation and use of the MCC and the 1B Processor.

6.51 Page 1990 software will be integrated on the MUP ROM memory as part of the MCC resident software. Therefore, the 1990 Page hardware debugging capability will be immediately available to both local and remote users when it is needed at the *4ESS* Switch.

NOTE:
The digits of a numerical variable on Page 1990 is represented on Page 1990 by a square (□).

A. Command Syntax and Responses

6.52 The proper operation of Page 1990 requires a good understanding of the command line, command entry syntax and expected system responses. For additional information regarding these subjects, refer to the "Command Entry" and "Command Acknowledgment" sections discussed earlier in this practice.

A number of poke commands on Page 1990 require that the 1B Processor be in one of the UAS interfering modes as reflected by the UAS INTF ALW indicator on the MUP Status and Control Page (Page 106). The prerequisites for entry into either of the interfering modes are as follows:

(1) The 1B Processor utility interference switch must be *manually* moved from the "inhibit" to the "allow" position.

(2) Poke Command 613 (UAS INTF ALW) must be successfully entered and executed (if required).

For purposes of subsequent discussion of Page 1990 poke commands, the term "UAS Interfering mode" will imply the above conditions have occurred. The UAS Interfering mode requires that the 1B Processor utility interfering switch *remain* in the "allow" position. If the Utility interfering switch is returned to the "inhibit" position, the 1B Processor will immediately change from the UAS Interfering mode to the UAS Non-Interfering mode. The UAS Non-Interfering mode is entered via the use of Poke Command 612 (UAS NON-INTF ALW). The UAS Non-Interfering mode does not require that the 1B Processor utility interfering switch be in the "allow" position.

Any poke commands that require the suspension of the UAS Interfering mode will be terminated. For example, if the 1B Processor is suspended when the utility interference switch is returned to the "inhibited" position, the 1B Processor must be returned to the cycling mode. Except for those activities necessary to support GULP activities, writes to the buffer bus, writes to the MUP, Utility A-level interrupts and writes to the IFB bus will not be allowed.

B. Page 1990 — Indicators

6.53 The following information describes the indicators associated with Page 1990. The text, colors and specific circumstances under which the indicators will change are specified. The indicators are updated via CC software.

CC CONTROL

The CC CONTROL indicator is informational text identifying the CC Control area of Page 1990. The indicator will appear white on black.

SUSPEND The SUSPEND indicator is informational text identifying when the 1B Processor has been instructed to suspend processing. Normally, the indicator will appear white on black. When the 1B Processor is suspended, the indicator will appear white on red.

RUN The RUN indicator is informational text identifying when the 1B Processor has been instructed to resume processing. Normally, the indicator will appear black on green. When Poke Command 701 has beed entered, accepted and processing suspended, the indicator will appear white on black.

SINGLE STEP

The SINGLE STEP indicator is informational text associated with Poke Command 703. The indicator will appear white on black.

UPDATE REGS

The UPDATE REGS indicator is informational text associated with Poke Command 704. The indicator will appear white on black.

CC REG ACCESS

The CC REG ACCESS indicator is informational text identifying the central control register access area of Page 1990. The indicator will appear white on black.

READ CC REG

The READ CC REG indicator is informational text associated with Poke Command 720 used to read an active CC buffer bus register. The indicator will appear white on black.

WRITE CC REG

The WRITE CC REG indicator is informational text associated with Poke Command 721 used to write an active CC buffer bus register. The indicator will appear white on black.

WRITE BOL/BOR

The WRITE BOL/BOR indicator is informational text associated with Poke Command 722 used to write new data specifically to the BOL(x) and BOR(y) registers. The indicator will appear white on black. If only one parameter is entered, the new data will be written to the BOL register.

ADDR The ADDR indicator is informational text identifying the address display in the central control register access area. The indicator will appear white on black.

ADDR Display

The address display is an 8- or 11-character display depending on whether Poke Command 713 has been use to choose an octal or a hexadecimal base, respectively. The display data will appear white on black and be left-justified.

DATA The DATA indicator is informational text identifying the address display in the central control register access area. The indicator will appear white on black.

DATA Display

The data display is an 8- or 11-character display depending on whether Poke Command 713 has been employed to choose an octal or a hexadecimal base, respectively. The display data will appear white on black and be left justified.

MUP TEST The MUP TEST indicator is informational text identifying the MUP test area of Page 1990. The indicator will appear white on black.

DIAG MUP The DIAG MUP indicator is informational text associated with Poke Command 730 used to diagnose MUP integrity. The indicator will appear white on black.

DIAG MUP/MUI INT

The DIAG MUP/MUI INT indicator is informational text associated with Poke Command 731 used to diagnose the interface between the MUP and the MUI with existing MUP/MUI interface diagnostics. The indicator will appear white on black.

READ MUP MEMORY

The READ MUP MEMORY indicator is informational text associated with Poke Command 732 used to read the MUP memory. The indicator will appear white on black.

ADDR The ADDR indicator is informational text identifying the address display in the MUP test area. The indicator will appear white on black.

ADDR Display

The address display is an 8- or 11-character display depending on whether Poke Command 713 has been employed to choose an octal or a hexadecimal base, respectively. The display data will appear white on black and be left-justified.

DATA The DATA indicator is informational text identifying the address display in the MUP test area. The indicator will appear white on black.

DATA Display

The data display is an 8- or 11-character display depending on whether Poke Command 713 has been employed to choose an octal or a hexadecimal base, respectively. The display data will appear white on black and be left-justified.

MISCELLANEOUS

The MISCELLANEOUS indicator is informational text identifying the miscellaneous area of the Dead Start Page. The indicator will appear white on black.

INIT US The INIT US indicator is informational text associated with Poke Command 710 used to initialize the Utility System. Normally, the indicator will appear white on black. After Poke Command 710 has been successfully entered, the indicator will appear white on red until after the Utility System initialization has completed.

AUTO HARD A

The AUTO HARD A indicator is informational text associated with Poke Command 711 used to request an automatic HARD-A be sent to the 1B Processor repeatedly until the request is disabled by toggling Poke Command 711. Normally, the indicator will appear white on black. When selected, the indicator will appear black on purple.

BOL/BOR LOCK

The BOL/BOR LOCK indicator is informational text associated with Poke Command 712 used to allow a user to lock and execute the current instructions in the BOL and BOR registers repeatedly until the indicator is disabled by toggling Poke Command 712. Normally, the indicator will appear white on black. When selected, the indicator will appear black on purple.

BASE The BASE indicator is informational text associated with Poke Command 713 used to allow a user to alternate the base between hexadecimal and octal. The indicator will appear white on black.

BASE Display The base display indicator is informational text identifying which base has been chosen using Poke Command 713. The text OCTAL or HEX will appear white on black and be left-justified.

STATUS The STATUS indicator is informational text identifying the status area of Page 1990. The indicator will appear white on black.

INTF HW ENABLED

The INTF HW ENABLED indicator is informational text identifying that the 1B Processor utility interference switch has been moved to the enable position which is a major alarm condition. Normally, the indicator will not appear. However, when present, the indicator will appear white on red.

The MCC indicator in the Summary Status Area of Page 1990 will also appear white on red when the utility interference switch is enabled.

UAS Mode Indicator

The UAS Mode Indicator is a 22-character field that reflects the current utility system software state invoked on the MUP. The different *software* states represented by the UAS indicator are as follows:

- UAS: NORMAL UTIL — GULP activities can be executed.
- UAS: DISABLED — No UAS activities allowed.
- UAS: NON-INTERFERING — The user can perform non-interfering activities, such as read-only operation:
  - — Reading the buffer bus, memory or MUI
  - — Determining UAS status.

  The user cannot perform any interfering activities while in the non-interfering state.
- UAS: INTERFERING — The user can perform all non-interfering activities, as well as the following interfering activities:
  - — Writing the buffer bus, memory or MUI
  - — Changing status and configuration (as with the call stores and program stores)
  - — Suspending the CC
  - — Suspending DMA
  - — Forcing linear operation (prevents the 1B Processor from pipelining)
  - — Causing utility A-level interrupts
  - — AUTO Hard A
  - — BOL/BOR Lock.

Table R provides more detail regarding the UAS mode indicator states.

Table R. UAS Mode Indicator States

Text	Color	Function
UAS: DISABLED	Black on Yellow	The UTLSRV Process is not scheduled
UAS: NORMAL UTIL	White on Black	The UTLSRV Process allows only GULP requests
UAS: NON-INTERFERING	Black on Yellow	The UTLSRV Process performs only non-interfering requests
UAS: INTERFERING	White on Red	The UTLSRV Process performs interfering requests

1B PROCESSOR TEST

The 1B PROCESSOR TEST indicator is informational text identifying the 1B Processor test area of Page 1990. The indicator will appear white on black.

ALL TESTS The ALL TESTS indicator is informational text associated with Poke Command 740 used to execute all the 1B Processor boot ROM tests. Normally, the indicator will appear white on black. When selected, the indicator will appear white on red.

SINGLE TEST

The SINGLE TEST indicator is informational text associated with Poke Command 741 used to execute a single 1B Processor boot ROM test by specifying the specific test number. Normally, the indicator will appear white on black. When selected, the indicator will appear white on red.

Buffer Bus Register Display Section

The Buffer Bus Register Display Section contains 26 buffer bus registers. The values of these registers will not be updated constantly. Updates will be controlled primarily by Poke Command 704 (UPDATE REGS). Updates will also take place as a result of other poke commands such as 740, 741, 722, 701, 702 and 703 when used after executing Poke Command 701.

Each register has an informational text indicator followed by a display field. There will be no spaces separating the text indicator and display. All displays except the SH and SC register displays are 11 characters in octal or 8 characters in hexadecimal depending on the base selected. The SH and SC register displays are 2 characters in both octal and hexadecimal. All indicator text and register data will appear white on black.

Table S identifies the name and number of octal and hexadecimal digits associated with each register present on Page 1990.

C. Page 1990 — Poke Commands

6.54 The following information describes the function of each Page 1990 poke command, its effect on any display page indicators and the output messages (if any) directed to applicable output channels.

NOTE:
Poke Commands in the 700 series are global poke commands and can be executed from any page.

701 - SUSPEND

Poke Command 701 causes the 1B Processor to suspend processing. The poke command has no effect if the 1B Processor is already suspended. If Poke Command 701 is entered and the 1B Processor is in the UAS Interfering mode, an OK acknowledgment will be displayed in the response part of the command line. The receipt of the acknowledgment will occur whether the 1B Processor is running or suspended. If the 1B Processor is not in the UAS Interfering mode, the poke command is rejected and an NG (No Good) acknowledgment will be displayed in the response part of the command line. If Poke Command 701 is entered and the 1B Processor is running, the SUSPEND indicator will change from white on black to white on red. If the 1B Processor is suspended when Poke Command 701 is entered, the SUSPEND indicator will remain white on red.

702 - RUN Poke Command 702 causes the 1B Processor to resume processing if it has been suspended. The poke command has no effect if the 1B Processor is already running.

If Poke Command 702 is entered, an OK acknowledgment is displayed in the response part of the command line. The receipt of the acknowledgment will occur whether a single 1B Processor is running or suspended.

If Poke Command 702 is entered while the CCs are still matching, the command will be rejected and the NG, CC MATCHING acknowledgment will be be displayed in the response part of the command line.

If Poke Command 702 is entered and the 1B Processor is suspended, the RUN indicator will change from white on black to black on green. In addition, the registers in the Buffer Bus Register Display Section of Page 1990 will be updated.

If the 1B Processor is running when Poke Command 702 is entered,

the RUN indicator will appear black on green.

Table S. Dead Start Page — Buffer Bus Register Displays

Register	Octal Digits	Hexadecimal Digits
BR=	11 digits	8 digits
LR=	11 digits	8 digits
CAR=	11 digits	8 digits
FLA=	11 digits	8 digits
BS2=	11 digits	8 digits
FR=	11 digits	8 digits
XR=	11 digits	8 digits
DAR=	11 digits	8 digits
FLD=	11 digits	8 digits
BS3=	11 digits	8 digits
GR=	11 digits	8 digits
YR=	11 digits	8 digits
SH=	2 digits	2 digits
SC=	2 digits	2 digits
FLT=	11 digits	8 digits
BS4=	11 digits	8 digits
JR=	11 digits	8 digits
ZR=	11 digits	8 digits
BOL=	11 digits	8 digits
BS0=	11 digits	8 digits
BS5=	11 digits	8 digits
KR=	11 digits	8 digits
TR=	11 digits	8 digits
BOR=	11 digits	8 digits
BS1=	11 digits	8 digits
CSC=	11 digits	8 digits

703 - SINGLE STEP

Poke Command 703 permits the 1B Processor to execute a single instruction at a time. The registers in the Buffer Bus Register Display Section will be updated after the execution of each single instruction. In order for Poke Command 703 to execute successfully, the 1B Processor will have to be suspended using Poke Command 701. If Poke Command 703 is entered while the 1B Processor is still running, an NG, CC NOT SUSPENDED acknowledgment will be displayed in the response part of the command line. If Poke Command 703 is entered while the 1B Processor CCs are still matching, an NG, CC MATCHING acknowledgment will be displayed in the response part of the command line.

704 - UPDATE REGS

Poke Command 704 is used to manually refresh the values shown for the registers displayed in the Buffer Bus Register Display Section of Page 1990. The 26 registers will be updated with current data when Poke Command 704 is entered.

NOTE:
The data displayed in the buffer bus registers is only useful if the 1B Processor has suspended processing.

The successful entry of Poke Command 704 will cause an OK acknowledgment to be displayed in the response part of the command line. If the read fails for any reason, an error message will be displayed in the response part of the command line. If errors are detected for any of the registers, the displays for those registers will be blank.

720,x - READ CC REG

Poke Command 720 is used to read an active CC buffer bus register by specifying an address parameter. If the register is read successfully, the address and content of the register will be displayed in the CC REG ACCESS area's ADDR and DATA displays. The input parameter *must* use the same base as displayed by the BASE indicator. The output will also be displayed in the same base as identified by the BASE indicator.

Poke Command 720 checks the following conditions:

(1) Whether a parameter is provided with the poke command. If a parameter is not provided, the poke command will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(2) Whether the poke command and parameter are separated by a comma. If commas are absent or misplaced, the poke command will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(3) Whether the address is valid. If the address is not valid, the poke command will be rejected with a ?D acknowledgment displayed in the response part of the command line.

721,x,y - WRITE CC REG

Poke Command 721 is used to write an active CC buffer bus register. The address is specified by the first parameter and the new data is specified by the second parameter. The poke command and parameters are separated by commas. If the register is written successfully, the address and content of the register will be displayed in the CC REG ACCESS area's ADDR and DATA displays. Input parameters *must* be in the base reflected by the BASE indicator. The output will also be displayed in the same base as identified by the BASE indicator.

Poke Command 721 checks the following conditions:

(1) Whether a parameter is missing or whether there are more than two parameters provided. If there are excessive or missing parameters, the poke command will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(2) Whether there are more than two commas, fewer than two commas, or the commas are incorrectly placed. If comma syntax is incorrect, the poke command will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(3) Whether the UAS Interfering mode has been entered. If UAS Interfering mode has not been entered, the poke command will be rejected with an NG acknowledgment displayed in the response part of the command line.

(4) Whether the address is valid. If the address is not valid, the poke command will be rejected with a ?D acknowledgment displayed in the response part of the command line.

722,x,y - WRITE BOL/BOR

Poke Command 722 is used to write new data specifically to the BOL(x) and BOR(y) registers. The poke command will accept one or two parameters. The first parameter will represent the BOL register and the second parameter will represent the BOR register. The poke command and parameters will be separated by commas.

Poke Command 722 does not require the user to provide an address for these registers. The addresses and new data *will not* be displayed in the CC REG ACCESS area's ADDR and DATA displays. The new data for BOL and BOR will be displayed in the BOL and BOR register displays in the Buffer Bus Register Display Section of Page 1990.

Poke Command 722 checks for the following conditions:

(1) Whether the 1B Processor is suspended. Suspension of the 1B Processor requires that the UAS Interfering mode has been entered. If the 1B Processor has not been suspended, Poke Command 722 will be rejected with an NG acknowledgment displayed in the response part of the command line.

(2) Whether the CCs are matching. If Poke Command 722 is entered while the CCs are matching, the command will be rejected with an NG, CCs MATCHING acknowledgment displayed in the response part of the command line.

(3) Whether the parameters are in a valid range. If the parameters are not in a valid range, Poke Command 722 will be rejected with a ?D acknowledgment displayed in the response part of the command line.

(4) Whether both parameters are missing. If both parameters are missing, Poke Command 722 will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(5) Whether there are more than two parameters. If there are more than two parameters, Poke Command 722 will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(6) Whether the poke command and parameters are separated by commas. If the poke command and parameters are not separated by commas, Poke Command 722 will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(7) Whether the UAS Interfering mode has been entered. If the UAS Interfering mode has not been entered, Poke Command 722 will be rejected with an NG acknowledgment displayed in the response part of the command line.

730 - DIAG MUP

Poke Command 730 is used to diagnose MUP integrity. The command only provides access to existing MUP diagnostics. When Poke Command 730 is entered, Page 1990 will be cleared. The diagnostic process will take over control of the MUP and the user will not be allowed to enter any poke commands on the MCC terminal. In addition, any previous settings on Page 1990 will be erased. If all diagnostics run and complete without failure, the EAI Page will be refreshed. If diagnostics fail, an error message will be printed at the bottom of the MCC screen.

If Poke Command 730 is entered before the UAS Interfering mode has been entered, the command will be rejected with an NG, NO UTIL ACCESS acknowledgment displayed in the response part of the command line.

731 - DIAG MUP/MUI INT

Poke Command 731 is used to diagnose the interface between the MUP and the MUI with existing MUP/MUI interface diagnostics. If Poke Command 731 is entered, Page 1990 will be cleared. The diagnostic process will take over control of the MUP and the user will not be allowed to enter any poke commands on the MCC terminal. In addition, any previous settings on Page 1990 will be erased. If all diagnostics run and complete without failure, the EAI Page will be refreshed. If diagnostics fail, an error message will be printed at the bottom of the MCC screen.

If Poke Command 731 is entered before the UAS Interfering mode has been entered, the command will be rejected with an NG, NO UTIL ACCESS acknowledgment displayed in the response part of the command line.

732,x - READ MUP MEMORY

Poke Command 732 is used to read the MUP memory by specifying a valid address of the active MUP. For an address to be valid, it must be on an even word boundary in the MUP memory. If the register is read successfully, the address and content of the register will be displayed in the MUP TEST area's ADDR and DATA displays. The address parameter *must* use the same base as displayed by the BASE indicator. The output will also be in the same base as identified by the BASE indicator.

Poke Command 732 checks for the following conditions:

(1) Whether there is a comma between the poke command and parameter. If there is no comma between the poke command and parameter, Poke Command 732 will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(2) Whether no parameter or more than one parameter is specified with the command. If there is no parameter specified or more than one parameter specified, Poke Command 732 will be rejected with a ?E acknowledgment displayed in the response part of the command line.

(3) Whether the MUP address is valid. If the address is not valid, Poke Command 732 will be rejected with a ?D acknowledgment displayed in the response part of the command line.

710 - INIT US Poke Command 710 is used to initialize the Utility System. Poke Command 710 will cause the initialization of the utility data tables and hardware accessed by the utility library functions. If the UAS Interfering mode has not been entered, Poke Command 710 will fail and an NG (No Good) acknowledgment will be displayed in the response part of the command line.

711 - AUTO HARD A

Poke Command 711 causes an automatic HARD-A to be sent to the 1B Processor repeatedly until the command is disabled by toggling the poke command.

When Poke Command 711 is entered, the 1B Processor must be in the UAS Interfering mode. If Poke Command 711 is entered and the 1B Processor is not in the UAS Interfering mode, Poke Command 711 will be rejected and an NG acknowledgment will be displayed in the response part of the command line.

If Poke Command 711 is entered and the 1B Processor CCs are still matching, the poke command will be rejected and an NG, CC MATCHING acknowledgment will be displayed in the response part of the command line.

If Poke Command 712 is selected (active), Poke Command 711 will be rejected and an NG (No Good) acknowledgment will be displayed in the response part of the command line because BOL/BOR Lock and HARD-A cannot be performed simultaneously.

712 - BOL/BOR LOCK

Poke Command 712 allows the user to lock and execute the current instructions in the BOL and BOR registers repeatedly until the function is disabled by toggling the poke command. If the UAS Interfering mode has not been entered, the poke command will be rejected and an NG (No Good) acknowledgment will be displayed in the response part of the command line. If Poke Command 712 is entered while the 1B Processor CCs are matching, the poke command will be rejected and an NG, CC MATCHING acknowledgment will be displayed in the response part of the command line. If Poke Command 711 has been entered (active), Poke Command 712 will be rejected and an NG (No Good) acknowledgment will be displayed in the response part of the command line because BOL/BOR Lock and HARD-A cannot be performed simultaneously.

713 - BASE Poke Command 713 allows the user to alternate the base between hexadecimal and octal. If the current base is octal, the text "OCTAL" will be displayed. If the current base is hexadecimal, the text "HEX" will be displayed. All Page 1990 poke command input parameters except Poke Command 741 parameters will be in the base selected by Poke Command 713. All Page 1990 output display indicators will be in either octal or hexadecimal depending on the base chosen.

740 - ALL TESTS

Poke Command 740 provides the user the ability to execute all 1B Processor boot ROM tests. If Poke Command 740 completes successfully, all registers in the Buffer Bus Register Display Section of Page 1990 will be updated.

When Poke Command 740 is entered, the 1B Processor must be in the UAS Interfering mode. If Poke Command 740 is entered and the 1B Processor is not in the UAS Interfering mode, Poke Command 740 will be rejected and an NG (No Good) acknowledgment will be displayed in the response part of the command line. If Poke Command 740 is entered while the 1B Processor CCs are still matching, the poke command will be rejected and an NG, CC MATCHING acknowledgment will be displayed in the response part of the command line. If Poke Command 740 has previously been entered and is still in progress, the most recent Poke Command 740 will abort the previous poke command. Upon the completion of all tests whether or not they have passed, the registers in the Buffer Bus Register Display Section of Page 1990 will be updated.

741,x: SINGLE TEST

Poke Command 741 will execute a single 1B Processor boot ROM test by specifying the specific test number. The test number is always in decimal format regardless of the base selected by Poke Command 713. The following conditions will cause Poke Command 741 to be rejected.

(1) If the poke command is entered while the 1B Processor CCs are still matching, the poke command will be rejected with an NG, CC MATCHING acknowledgment displayed in the response part of the command line.

(2) The entry of more than one parameter will cause Poke Command 741 to be rejected with a ?E acknowledgment displayed in the response part of the command line.

(3) If the UAS Interfering mode has not been entered, Poke Command 741 will be rejected with an NG acknowledgment displayed in the response part of the command line.

(4) If the test number specified as a parameter is invalid, Poke Command 741 will be rejected with a ?D acknowledgment displayed in the response part of the command line.

(5) If a test is not currently in process, entry of Poke Command 741 without parameters will be rejected with an NG acknowledgment displayed in the response part of the command line.

Poke Command 741 entered with no parameters when a test is currently in process will cause the command to be rejected with an OK - TEST ABORTED acknowledgment displayed in the response part of the command line. The test currently in process will be cleared.

7. MCC Indicator and Poke Status During MUP Duplex Failure

7.01 The **MCC DPFL** indicator in the Summary Status Area of each MCC display page identifies the MCC status. Normally, the indicator will appear white on black identifying that the MCC is properly communicating with the 1B Processor via the Interface Bus (IFB). However, when communication between the MCC and 1B Processor is lost, the indicator will appear white on red.

7.02 Tables U through AD identifies the status of applicable MCC display page indicators and pokes during a MUP duplex failure.

Table T. Page 100 Poke/Indicator Status During MCC Duplex Failure

Page 100 Functional Area	Page 100 Poke/Indicator Text	Poke Status	Indicator Status
PAGE 100	EA DISP - EMERGENCY ACTION INTERFACE	Valid	N/A
	100 - PAGE INDEX	Valid	N/A
	106 - MUP STATUS AND CONTROL	Valid	Invalid
	108 - SYSTEM STATUS	Valid	Invalid
	109 - PRPGRAM STORE STATUS AND CONTROL	Valid	Invalid
	110 - CALL STORE STATUS AND CONTROL	Valid	Invalid
	111 - IFB CLIENTS STATUS AND CONTROL	Valid	N/A
	118 - 1B PROCESSOR STATUS	Valid	N/A
	119 - DDI KEY OPTIONS	Valid	N/A
	120 - DATA DISPLAY	Valid	N/A
	1990 - DEAD START	Valid	N/A

Table U. EAI Page Poke/Indicator Status During MCC Duplex Failure

EAI Page Functional Area	EAI Page Poke/Indicator Text	Poke Status	Indicator Status
FORCE FNCT	01 - Hard A	Valid	Valid
	10 - CC 0	Valid	Valid
	11 - CC 1	Valid	Valid
	20 - PS 0	Valid	Valid
	21 - PS 1	Valid	Valid
	22 - PSB 0	Valid	Valid
	23 - PSB 1	Valid	Valid
	30 - CSB 0	Valid	Valid
	31 - CSB 1	Valid	Valid
	40 - IFB 0	Valid	Valid
	41 - IFB 1	Valid	Valid
	42 - AUB 0	Valid	Valid
	43 - AUB 1	Valid	Valid
EMER CFG	48 - FULL	Valid	Valid
	49 - MIN	Valid	Valid
MANUAL PROG REQ	02 - SOFT A	Valid	Valid
	51 - PHASE 1	Valid	Valid
	52 - PHASE 2	Valid	Valid
	53 - PHASE 3	Valid	Valid
	54 - PHASE 4	Valid	Valid
	81 - CLEAR UTIL	Valid	Valid
	82 - RESTORE I/O	Valid	Valid
	83 - INHIBIT INT	Valid	Valid
	84 - MODIFY REC	Valid	Valid
FILE SELECT	61 - NORM FILE	Valid	Valid
	62 - UPD FILE	Valid	Valid
SYSTEM REINIT	63 -	Invalid	N/A
	64 - UTILITY SR	Valid	Valid
PC SEQUENCER	03,xx - SET PC STATE	Valid	Valid
	04 - INCREMENT PC	Valid	Valid
	70 - DIS AUTO PC	Valid	Valid
PC PROGRESSION	CC CS IF AU PS CMPL	N/A	Valid

Table U. EAI Page Poke/Indicator Status During MCC Duplex Failure (Contd)

EAI Page Functional Area	EAI Page Poke/Indicator Text	Poke Status	Indicator Status
DIRECT DATA INSERT	401/400,xx - SET/RESET xx	Valid	Valid
	402 - RESET ALL	Valid	Valid
EAI FAIL DATA DISPLAY	86 - CODE:	Valid	Valid
	87 - DATA:	Valid	Valid
	88 - ADDR:	Valid	Valid
	89 - CLEAR DISPLAY	Valid	Valid

Table V. Page 106 Poke/Indicator Status During MCC Duplex Failure

Page 106 Functional Area	Page 106 Poke/Indicator Text	Poke Status	Indicator Status
COMMON CONTROL	410 - SW:MUP	Invalid	Invalid
	829 - OP:OOSUNITS:MUP	Invalid	Invalid
UNIQUE CONTROL	601 - PORTS 1&3 INH/ALW	Valid	Valid
	602 - RLS MCC FORCE	Valid	Valid
UAS MODE	610 - DISABLE ALL UTIL	Valid	Valid
	611 - NORMAL UTIL	Valid	Valid
	612 - UAS NON-INTF ALW	Valid	Valid
	613 - UAS INTF ALW	Valid	Valid
N/A	UAS NORMAL UTIL	N/A	Valid
N/A	MUP ALARMS	N/A	Valid
N/A	MCC TIMEOUT	N/A	Valid
N/A	MUP FORCED	N/A	Valid
N/A	INTF HW ENABLED	N/A	Valid

Table W. Page 108 Poke/Indicator Status During MCC Duplex Failure

Page 108 Functional Area	Page 108 Poke/Indicator Text	Poke Status	Indicator Status
SYSTEM STATUS	810 - SDC	Invalid	Invalid
	811 - PGM CNTL OFF NORM	Invalid	Invalid
	812 - OVLD CTL IN EFF	Invalid	Invalid
	813 - INTRPT INH	Invalid	Invalid
	814 - REFSTAT	Invalid	Invalid
SYSTEM CONTROLS	801 - RESTRICT RC	Invalid	Invalid
	802 - INH SUP PRINT	Invalid	Invalid
	803 - INH INT PRINT	Invalid	Invalid
	804 - INH AUD PRINT	Invalid	Invalid
	805 - ELEV AUD PRINT	Invalid	Invalid
	806 - REINIT TTY SYS	Invalid	Invalid
	807 - REQ TTY AUDIT	Invalid	Invalid
	808 - CLEAR INTERRUPTS	Invalid	Invalid
	809 - CLEAR MEM REC PHASE	Invalid	Invalid
	899 - OP:OOSUNITS (ALL)	Invalid	Invalid
PROCESSOR EQUIPMENT STATUS	820 - CC	Invalid	Invalid
	821 - PSB	Invalid	Invalid
	822 - CSB	Invalid	Invalid
	823 - PS	Invalid	Invalid
	824 - CS	Invalid	Invalid
	825 - FNS	Invalid	Invalid
	826 - IFB	Invalid	Invalid
	827 - AUI	Invalid	Invalid
	828 - SSD	Invalid	Invalid
	829 - MUP	Invalid	Invalid
	830 - IOUS	Invalid	Invalid
	831 - IOUC	Invalid	Invalid
	832 - APS	Invalid	Invalid
	833 - API	Invalid	Invalid
	834 - DUS	Invalid	Invalid
	835 - TUC	Invalid	Invalid
	836 - AUB	Invalid	Invalid
	837 - PUB	Invalid	Invalid
	838 - PCD	Invalid	Invalid
	839 - XPWR	Invalid	Invalid
	840 - SFI	Invalid	Invalid
	841 - SPP	Invalid	Invalid

Table W. Page 108 Poke/Indicator Status During MCC Duplex Failure (Contd)

Page 108 Functional Area	Page 108 Poke/indicator Text	Poke Status	Indicator Status
PERIPHERAL EQUIPMENT STATUS	850 - TMSP	Invalid	Invalid
	851 - TSI	Invalid	Invalid
	852 - NCLK	Invalid	Invalid
	853 - NSCU	Invalid	Invalid
	854 - SCLK	Invalid	Invalid
	855 - SP	Invalid	Invalid
	856 - DT	Invalid	Invalid
	857 - DIF	Invalid	Invalid
	858 - VIF	Invalid	Invalid
	859 - EST	Invalid	Invalid
	860 - SCS	Invalid	Invalid
	861 - RA	Invalid	Invalid
	862 - TGR	Invalid	Invalid
	863 - SLNK	Invalid	Invalid
	864 - VFL	Invalid	Invalid
	865 - R&T	Invalid	Invalid
	866 - SVC	Invalid	Invalid
	867 - XTSI	Invalid	Invalid

Table X. Page 109 Poke/Indicator Status During MCC Duplex Failure

Page 109 Functional Area	Page 109 Poke/Indicator Text	Poke Status	Indicator Status
BUS STATUS	PSB 0 ACT	N/A	Valid
	PSB 1 STBY	N/A	Valid
STORE CONTROL	200,xx - RMV:PSB xx	Invalid	See Note
	201,xx - RMV:PS xx	Invalid	See Note
	300,xx _ RST:PSB xx	Invalid	See Note
	301,xx - RST:PS xx	Invalid	See Note
	500,xx - DGN:PSB xx	Invalid	See Note
	501,xx - DGN:PS xx	Invalid	See Note
	723 - OP:PSSTATUS	Invalid	See Note
	821 - OP:OOSUNITS:PSB	Invalid	See Note
	823 - OP:OOSUNITS:PS	Invalid	See Note
STORE STATUS	PS00	N/A	Valid
	PS01	N/A	Valid
	PS02	N/A	Valid
	PS03	N/A	Valid
	PS04	N/A	Valid
	PS05	N/A	Valid
	PS06	N/A	Valid
	PS07	N/A	Valid
	PS08	N/A	Valid
	PS09	N/A	Valid
	PS10	N/A	Valid
	PS11	N/A	Valid
	PS12	N/A	Valid
	PS13	N/A	Valid
NOTE: Indicator Color Is Valid For Associated Poke State. However, Poke Will Not Execute.			

Table Y. Page 110 Poke/Indicator Status During MCC Duplex Failure

Page 110 Functional Area	Page 110 Poke/Indicator Text	Poke Status	Indicator Status
BUS STATUS	CSB 0 STBY	N/A	Valid
	CSB 1 ACT	N/A	Valid
STORE CONTROL	200,xx - RMV:CSB xx	Invalid	See Note
	201,xx - RMV:CS xx	Invalid	See Note
	300,xx - RST:CSB xx	Invalid	See Note
	301,xx - RST:CS xx	Invalid	See Note
	500,xx - DGN:CSB xx	Invalid	See Note
	501,xx - DGN:CS xx	Invalid	See Note
	724 - OP:CSSTATUS	Invalid	See Note
	822 - OP:OOSUNITS:CSB	Invalid	See Note
	824 - OP:OOSUNITS:CS	Invalid	See Note
STORE STATUS	CS00	N/A	Valid
	CS01	N/A	Valid
	CS02	N/A	Valid
	CS03	N/A	Valid
	CS04	N/A	Valid
	CS05	N/A	Valid
	CS06	N/A	Valid
	CS07	N/A	Valid
	CS08	N/A	Valid
	CS09	N/A	Valid
	CS10	N/A	Valid
	CS11	N/A	Valid
	CS12	N/A	Valid
	CS13	N/A	Valid
	CS14	N/A	Valid
	CS15	N/A	Valid

NOTE: Indicator Color Is Valid For Associated Poke State. However, Poke Will Not Execute.

Table Y. Page 110 Poke/Indicator Status During MCC Duplex Failure (Contd)

Page 110 Functional Area	Page 110 Poke/Indicator Text	Poke Status	Indicator Status
STORE STATUS (Continued)	CS16	N/A	Valid
	CS17	N/A	Valid
	CS18	N/A	Valid
	CS19	N/A	Valid
	CS20	N/A	Valid
	CS21	N/A	Valid
	CS22	N/A	Valid
	CS23	N/A	Valid
	CS24	N/A	Valid
	CS25	N/A	Valid
	CS26	N/A	Valid
	CS27	N/A	Valid
	CS28	N/A	Valid
	CS29	N/A	Valid
	CS30	N/A	Valid
	CS31	N/A	Valid
	CS32	N/A	Valid
	CS33	N/A	Valid
	CS34	N/A	Valid
	CS35	N/A	Valid
	CS36	N/A	Valid
	CS37	N/A	Valid
	CS38	N/A	Valid
	CS39	N/A	Valid
NOTE: Indicator Color Is Valid For Associated Poke State. However, Poke Will Not Execute.			

Table Z. Page 111 Poke/Indicator Status During MCC Duplex Failure

Page 111 Functional Area	Page 111 Poke/Indicator Text	Poke Status	Indicator Status
BUS STATUS	IFB 0	N/A	Valid
	IFB 1	N/A	Valid
BUS AND CLIENT CONTROL	201,xx	Invalid	N/A
	203,xx	Invalid	N/A
	204,xx	Invalid	N/A
	205,xx	Invalid	N/A
	301,xx	Invalid	N/A
	303,xx	Invalid	N/A
	304,xx	Invalid	N/A
	305,xx	Invalid	N/A
	401	Invalid	N/A
	403	Invalid	N/A
	501,xx	Invalid	N/A
	503,xx	Invalid	N/A
	504,xx	Invalid	N/A
	505,xx	Invalid	N/A
	726	Invalid	N/A
	727	Invalid	N/A
	728	Invalid	N/A
	826	Invalid	N/A
	827	Invalid	N/A
	828	Invalid	N/A
	829	Invalid	N/A
	840	Invalid	N/A

Table AA. Page 111 Poke/Indicator Status During MCC Duplex Failure (Con't)

Page 111 Functional Area	Page 111 Poke/Indicator Text	Poke Status	Indicator Status
CLIENT STATUS	MUP 00	N/A	Valid
	MUP 01	N/A	Valid
	MUPP 00	N/A	Valid
	MUPP 01	N/A	Valid
	AUI 00	N/A	Valid
	AUI 01	N/A	Valid
	SSD 00	N/A	Invalid
	SSD 01	N/A	Invalid

Table AB. Page 118 Poke/Indicator Status During MCC Duplex Failure

Page 118 Functional Area	Page 118 Poke/Indicator Text	Poke Status	Indicator Status
PROCESSOR	CC 0	N/A	Valid
	CC 1	N/A	Valid
	PC STATE	N/A	Valid
BUSES	PSB 0	N/A	Valid
	PSB 1	N/A	Valid
	CSB 0	N/A	Valid
	CSB 1	N/A	Valid
	PUB 0	N/A	Valid
	PUB 1	N/A	Valid
	IFB 0	N/A	Valid
	IFB 1	N/A	Valid
IFB CLIENTS	MUP 0	N/A	Valid
	MUP 1	N/A	Valid
	AUI 0	N/A	Valid
	AUI 1	N/A	Valid
	SSD 0	N/A	Invalid
	SSD 1	N/A	Invalid
AUXILIARY UNITS	AUB 0	N/A	Valid
	AUB 1	N/A	Valid
	API 0	N/A	Invalid
	API 1	N/A	Invalid
	DUS 0	N/A	Invalid
	DUS 1	N/A	Invalid

Table AC. Page 119 Poke/IndicatoR Status During MCC Duplex Failure

Page 119 Functional Area	Page 119 Poke/Indicator Text	Poke Status	Indicator Status
PAGE 119	499 - TOGGLE MRA/INHIBIT INTERRUPT OPTIONS	Valid	Valid
	401,xx - SET xx	Valid	Valid
	400,xx - RESET xx	Valid	Valid
	402 - RESET ALL	Valid	Valid

Table AD. Page 120 Poke/Indicator Status During MCC Duplex Failure

Page 120 Functional Area	Page 120 Poke/Indicator Text	Poke Status	Indicator Status
DISPLAY SECTION 1	911 - CONTENTS MEMORY	Valid	Valid
	912 - SCAN POINTS	Valid	Valid
	913 - WRITE ADDR/GCP	Valid	Valid
	914 - NMBR BASE TOGGLE	Valid	Valid
WRITE/GCP ALLOWED	991 - ALW WRITE	Valid	Valid
	992 - ACTIVATE GCP	Valid	Valid
	993 - ACTIVATE WRITE	Valid	Valid
	994 - MODE TOGGLE	Valid	Valid
DISPLAY SECTION 2	921 - CONTENTS MEM/BUFFER	Valid	Valid
	922 - MACP CLIENT	Valid	Valid
	923 - WRITE DATA	Valid	Valid
	924 - NMBR BASE TOGGLE	Valid	Valid
DATA INSERT SECTION 1	940,xx - DATA O'	Valid	Valid
	941 - INCREMENT	Valid	Valid
DATA INSERT SECTION 2	950,xx - DATA O'	Valid	Valid
	951 - INCREMENT	Valid	Valid

Table AE. Page 1990 Poke/Indicator Status During MCC Duplex Failure

Page 1990 Functional Area	Page 1990 Poke/Indicator Text	Poke Status	Indicator Status
CC CONTROL	701 - SUSPEND	Valid	Valid
	702 - RUN	Valid	Valid
	703 - SINGLE STEP	Valid	Valid
	704 - UPDATE REGS	Valid	Valid
CC REG ACCESS	720,x - READ CC REG	Valid	Valid
	721,x,y - WRITE CC REG	Valid	Valid
	722,x,y - WRITE BOL/BOR	Valid	Valid
	ADDR:	N/A	Valid
	DATA:	N/A	Valid
MUP TEST	730 - DIAG MUP	Valid	Valid
	731 - DIAG MUP/MUI INT	Valid	Valid
	732,x - READ MUP MEMORY	Valid	Valid
	ADDR:	N/A	Valid
	DATA:	N/A	Valid
MISCELLANEOUS	710 - INIT US	Valid	Valid
	711 - AUTO HARD A	Valid	Valid
	712 - BOL/BOR LOCK	Valid	Valid
	713 - BASE	Valid	Valid
STATUS	INTF HW ENABLED	N/A	Valid
	UAS NON-INTERFERING	N/A	Valid
1B PROCESSOR TEST	740 - ALL TESTS	Valid	Valid
	741,x - SINGLE TEST	Valid	Valid

8. Power

MUP Power

8.01 The MUP power supply hardware is separate from the 1B Processor power supply hardware. This configuration ensures that if there is some type of 1B Processor failure the MUPs will continue to provide all Emergency Action Interface (EAI) functions using the MCC Utility Interface (MUI).

MCC Terminal Power Requirements

8.02 The MCC terminal requires 120V 60-Hz, single-phase, protected AC power from the power distribution system. Protected AC power is derived from commercial AC power and backed up by a DC-to-AC inverter.

8.03 Switch reliability requirements dictate that all *4ESS* Switch site terminals conform to National Equipment and Building Standards (NEBS) requirements, especially in the areas of office power, holdover and interference.

NOTE:
If a non-NEBS compliant terminal is used in an emergency situation, it is imperative that the terminal be replaced with a NEBS-compliant terminal as quickly as possible.

Building Power Indicator

8.04 Each MCC page has the PWR/BLDG indicator located in the Summary Status Area. Normally, the indicator will appear white on black indicating that there are no Power or Building (PWR/BLDG) alarms in effect. If a power alarm or environmental alarm is detected by the *4ESS* Switch, the PWR/BLDG indicator will appear black on yellow. The PWR/BLDG indicator will remain black on yellow until the faulty condition is corrected.

9. Maintenance

9.01 The primary system maintenance objective is to maintain call processing during error and/or fault intervals. The system monitoring and manual emergency recovery functions of the MCC terminal make these objectives an integral part of the maintenance operations plan. The MCC terminal is a major maintenance tool in the *4ESS* Switch Maintenance Operations Center (MOC).

The primary system maintenance objectives are met using the following system features:

- Hardware design
- Fault detection and diagnosis by software and/or manual test procedures
- Repairing faulty equipment
- Verification of repair by software and/or manual test procedures
- Returning repaired equipment to service.

9.02 The *4ESS* Switch maintenance philosophy and maintenance facilities are described in the ***4ESS***™ *Switch General Description*, AT&T Practice 234-100-000. The MOC is responsible for maintenance and repair of the MCC terminal.

9.03 Since the MCC terminal is the point of direct interface between the operating personnel and the system, the control and display design has been kept user friendly. Care has been taken to avoid any arrangement that might mislead or confuse operating personnel and sequential operations have been kept to a minimum.

Trouble Clearing and Routine Maintenance

9.04 Procedures for performing any routine maintenance and/or trouble clearing tasks associated with the Master Control Complex (MCC) are provided in the ***4ESS***™ *Switch 1B Processor Cabinet*, Task Oriented Practice (TOP), AT&T Practice 234-351-004.

Abbreviations and Acronyms

10.01 The following is a list of abbreviations and acronyms with accompanying definitions as applicable to this practice:

A

ACT
Active

ADDR
Address

ALW
Allow

API
Attached Processor Interface

APS
Attached Processor System

ARAR
Address-Reply-Address-Reply Status Bits

ASCII
American Standard Code for Information Interchange

ASD
Alarm Status Display

AU
Auxiliary Unit

AUB
Auxiliary Unit Bus

AUI
Auxiliary Unit Interface

C

C & D
Control and Display

CAMA
Centralized Automatic Message Accounting

CC
Central Control

CI
Critical Indicators

CIC
Customer Information Center

CLLI
Common Language Location Index

CMS
Change Management System

CNI
Common Network Interface

CNTL
Control Key

CS
Call Store

CSB
Call Store Bus

D

DAP
Distinguished Administrative Processor

DDI
Direct Data Insert

DGN
Diagnose

DIF
Digital Interface

DT
Digroup Terminal

DTR
Data Terminal Ready

DUS
Data Unit Selector

E

EA
Emergency Action

EAI
Emergency Action Interface

ESC
Escape Key

ESS
Electronic Switching System

EST
Echo Suppressor Terminal

F

FSD
Feature Specification Document

G

GCP
Generate Control Pulse

I

IFB
Interface Bus

IMR
Initial Modification Request

INH
Inhibit

IOUC
Input/Output Unit Controller

IOUS
Input/Output Unit Selector

K

Kbps
1,000 Bits Per Second

L

LAN
Local Area Network

LEC
Local Exchange Carrier

M

MCC
Master Control Complex

MMOC
Minicomputer Maintenance and Operations Center

MOC
Maintenance Operations Center

MR
Modification Request

MRA
Modify Recovery Action

MTC
Maintenance

MUI
MCC Utility Interface

MUP
MCC and Utility Processor

N

NA
No Acknowledgment

NCLK
Network Clock

NCSU
Network Clock Synchronization Unit

NEBS
National Equipment and Building Standards

NESAC
National Electronic Switching Assistance Center

NSD
Network Service Division

O

ODA
Office Data Assembler

OOS
Out-of-Service

ORNU
Order Number

OS
Operations Support

P

PAD
Packet Assembler/Disassembler

PAT
Power Alarm Test

PC
Processor Configuration

PCD
Power Conversion and Distribution

PF
Printout Follows

PGM CNTL
Program Controls

PHASE IN PROG
Phase-In-Progress

PORTS
Portable Recovery Test Set

PPI
Processor Peripheral Interface

PS
Program Store

PSB
Program Store Bus

PU
Peripheral Unit

PUB
Peripheral Unit Bus

PWR/BLDG
Power or Building

R

R&T
Ringing and Tone

RA
Recorded Announcement

RARP
Reverse Address Resolution Protocol

RB
Rollback

RBOC
Regional Bell Operating Company

RC
Recent Change

RLS
Release

RMV
Remove

ROM
Read Only Memory

RST
Restore

S

SCC
Service Circuit Controller

SCLK
System Clock

SCS
Service Circuit System

SDC
Service Degrading Condition

SFI
Switch Fabric Interface

SLNK
Signaling Link

SNMP
Simple Network Management Protocol

SP
Signal Processor

SPC
Stored Program Controlled

SPCS
Stored Program Control Switch

SPP
Switch Processing Platform

SR
System Reinitialization

SSD
Scan and Signal Distributor

STBY
Standby

SVC
Service Circuits

T

NCC
Network Control Center

TGR
Terminal Group Frame

TMS
Time Multiplexed Switch

TMSP
Time Multiplexed Switch Peripherals

TNM
Total Network Management

TOP
Task Oriented Practice

TSI
Time Slot Interchange

TTY
Teletype

TUC
Tape Unit Controller

U

UAS
Utility Access System

UNEQ
Unequipped

UNK
Unknown

V

VCS
Virtual Circuit Switch

VDT
Video Display Terminal

VFL
Voice Frequency Link

VIF
Voice Interface Frame

VTP
Virtual Terminal Protocol

W

WAN
Wide Area Network

X

XTSI
Expanded Time Slot Interchange

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How Are We Doing?

Document Title: ***4ESS***™ Switch With 1B Processor Master Control Complex (MCC) Description

Document No.: 234-301-004 Issue 5 Date: February 1999

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- ☐ Improve the overview/introduction
- ☐ Improve the table of contents
- ☐ Improve the organization
- ☐ Include more figures
- ☐ Add more examples
- ☐ Add more detail
- ☐ Make it more concise/brief
- ☐ Add more step-by-step procedures/tutorials
- ☐ Add more troubleshooting information
- ☐ Make it less technical
- ☐ Add more/better quick reference aids
- ☐ Improve the index

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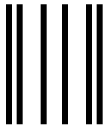

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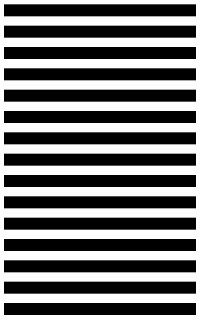

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