4ESS™ Switch with 1B Processor Peripheral Unit Bus General Description

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1. Introduction

1.01 This document describes the 4ESS™-2000 Switch Peripheral Unit Bus (PUB) system. The following information is included:

- Physical and functional description along with a theory of operation for the PUB cabling and the Peripheral Unit Bus Branching (PUBB) frame
- Description of the PUB system interface with 4ESS Switch peripheral units
- Description of how the PUBB frame signal and control circuits perform their functions
- Description of how the PUBB frame power and alarm circuits perform their functions
- PUB system growth
- PUB system power requirements
- Maintenance philosophy.

1.02 This document is being reissued to incorporate eXpanded Time Slot Interchange XTSI Release 1, 2 and 3 (4E24) changes.

1.03 This document does not contain safety labels.

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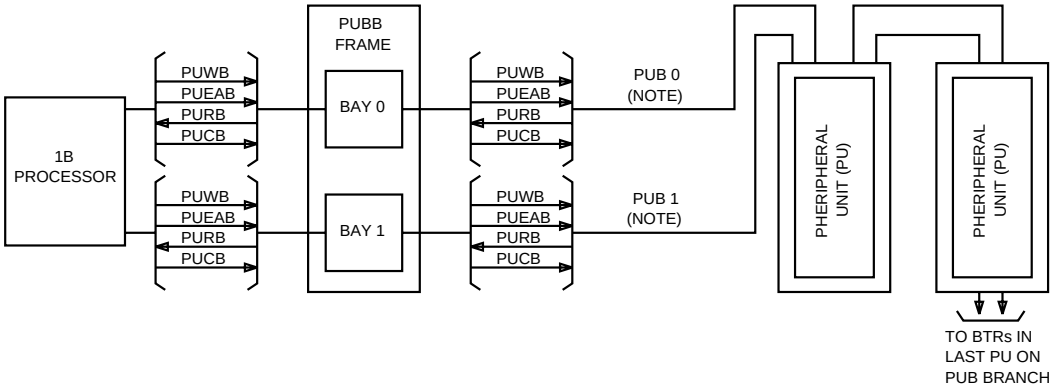
1.07 This document was developed by the Lucent Network Systems Customer Training and Information Products organization.

2. General

Purpose

2.01 The PUB system (Figure 1) is the facility that carries information between the 1B Processor and various 4ESS Switch Peripheral Units (PUs). This information is used by the PUs to control call processing, maintenance routines, and other functions of the switching office. The 1B Processor central control transmits addresses, instructions, call data, and control information to the peripheral units and receives reply data and maintenance information from the peripheral units via the PUB system.

2.02 The PUB system primarily consists of the PUB frame and the duplicated PUB, designated PUB 0 and PUB 1. The primary duplicated PUB is routed from the Processor Peripheral Interface (PPI) frame in the 1B Processor area to the PUBB frame in the 4ESS Switch area (Figure 2). The PUBB frame may branch the primary PUB into a maximum of 16 branches. Each branch of the duplicated PUB is routed serially from the PUBB frame to peripheral units in the 4ESS Switch area. In an office, a maximum of 16 branches may be routed to peripheral units.

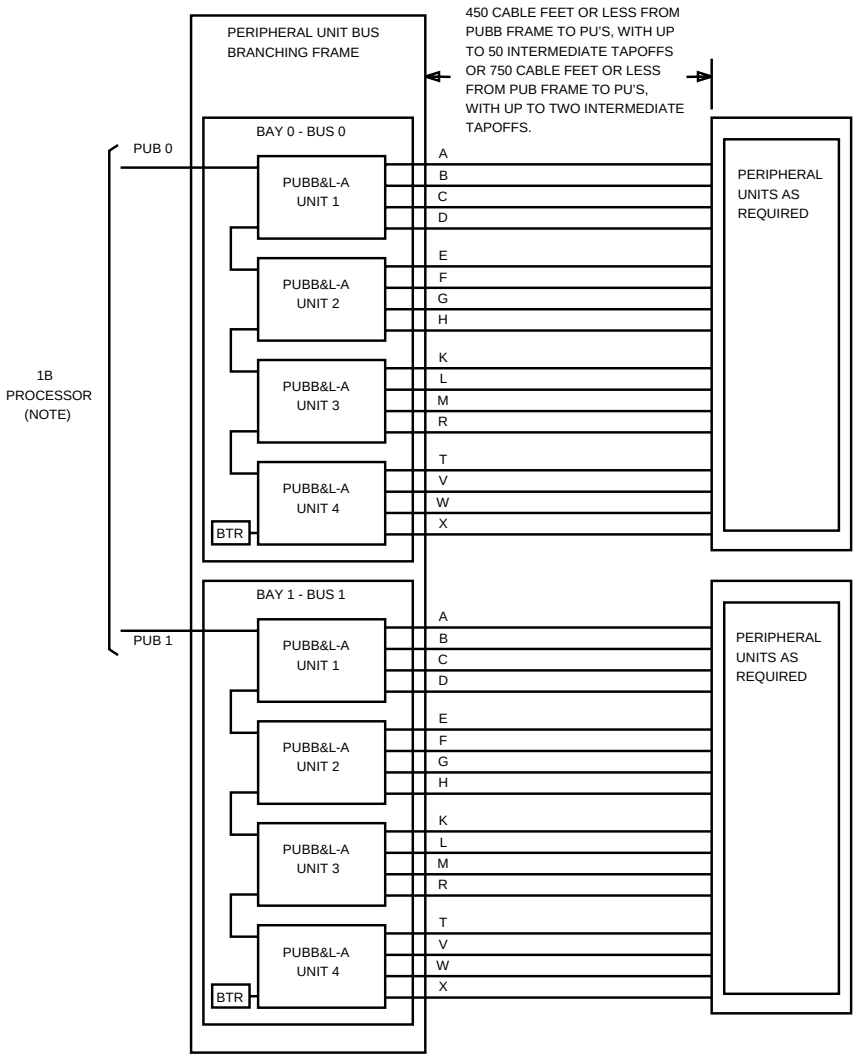


NOTE: UP TO 16 PUB BRANCHES MAY LEAVE THE PUBB FRAME AND GO TO PERIPHERAL UNITS

LEGEND:

PUCB:	PERIPHERAL UNIT CONTROL BUS
PUEAB:	PERIPHERAL UNIT ENABLE ADDRESS BUS
PURB:	PERIPHERAL UNIT REPLY BUS
PUWB:	PERIPHERAL UNIT WRITE BUS

Figure 1. Peripheral Unit Bus System



NOTE:
BUS LENGTH IS RESTRICTED TO 62 CABLE FEET OR LESS FROM CENTRAL CONTROLS THROUGH THE PUBB FRAME, WITH UP TO SIX INTERMEDIATE TAPOFFS.

LEGEND:

BTR	BUS TERMINATING RESISTOR
PU	PERIPHERAL UNIT
PUB	PERIPHERAL UNIT BUS
PUBB	PERIPHERAL UNIT BUS BRANCHING
PUBB&L-A	PERIPHERAL UNIT BUS BRANCHING AND LOOP-AROUND

Figure 2. Peripheral Unit Bus Branching Arrangement

2.03 PUB 0 and PUB 1 are each divided into four groups designated as follows:

Peripheral Unit Enable Address Bus (PUEAB)

— The PUEAB is used to transmit coded enable address information, a mode bit to indicate the operational mode of the accompanying order, a synchronization pulse, and two clock signals to the peripheral units.

Peripheral Unit Write Bus (PUWB)

— The PUWB is used to transmit peripheral unit instructions, write data, and parity to the peripheral units.

Peripheral Unit Reply Bus (PURB)

— The PURB is used to transmit reply information and autonomous peripheral unit failure responses from the peripheral units to the 1B Processor in response to peripheral orders and interrogations.

Peripheral Unit Control Bus (PUCB)

— The PUCB is used to poll and interrogate the peripheral units under 1B Processor control.

2.04 The following frame types in the 4ESS Switch peripheral community require access to the PUB system:

- Common Channel Interoffice Signaling Terminal Group Frame
- Input/Output Frame
- Input/Output Processor Frame
- Network Clock Frame
- Digital Interface Frame
- Signal Processor 1 Control Frame
- Signal Processor 2 Control Frame
- System Clock Frame
- Time Multiplexed Switching Frame
- Time Slot Interchange Frame
- Voiceband Interface Frame
- Echo Suppressor Terminal
- Attached Processor Interface Frame
- Service Circuit Controller Cabinet
- Expanded Time Slot Interchange.

Equipment Characteristics

2.05 Loop-around circuits in the PUBB frame are provided for maintenance checks of the PUB system up to the branched outputs of the frame in which they reside.

When operating in the loop-around mode, data received in selected bit positions of the PUEAB, PUWB, and PUCB by the PUBB frame is returned to the 1B Processor in dedicated bit positions of the PURB. In the case of the PUBB frame, data is returned to the 1B Processor. This data is compared with the data transmitted to check the operation of the PUB up to the PUBB frame branched outputs. All PURB data transmission from the PUBB frame to the 1B Processor may be inhibited for maintenance purposes by a PURB maintenance clamp circuit within the PUBB frame.

2.06 System timing requirements and PUB system transmission characteristics limit the maximum bus length between the central controls and the PUBB frame, and the PUBB frame and the peripheral units.

As illustrated in Figure 2, the maximum bus length from central control to the PUBB frame is 62 cable feet with a maximum of six "tapoffs." Four of these bus "tapoffs" are required by a fully equipped PUBB frame. Each branch of the PUBB frame is limited to 370 cable feet with a maximum of 50 "tapoffs" or to 670 cable feet with a maximum of two "tapoffs." The 16 PUB branches associated with the PUBB frame are identified with a suffixed bus branch letter (A, B, C, D, E, F, G, H, K, L, M, R, T, V, W, X). For the purpose of calculating branch length and number of "tapoffs," PUB branches A, C, E, G, K, M, T, and W have no internal PUBB frame "tapoffs" or bus length up to the frame male connectors which attach directly to the cable of the PUB branches. However, PUB branches B, D, F, H, L, R, V, and X each require one "tapoff" and four inches of bus length within a PUBB frame since these bus branches are used in connection with loop-around circuitry.

2.07 Bus access circuitry that consists of cable receivers and cable drivers in each peripheral unit provides the interface between the PUB signals and the peripheral units internal 1B logic signals. Figure 3 illustrates the methods employed to interface cable receivers and cable drivers to the balanced signal leads of the PUB. Cable drivers are shunt elements connected across the PUB signal leads while cable receivers are connected in series with the balanced signal leads. Bypass resistors bridged across each cable receiver "tapoff" maintain PUB continuity when cable receiver plug-in circuit packs are removed for maintenance. The 100-ohm characteristic impedance of each PUB signal lead pair is maintained by Bus Terminating Resistors (BTRs) installed at the last peripheral unit of each PUB branch.

3. Physical Description

3.01 This part provides a physical description of the PUB system and is divided as follows:

- PUBB Frame (J4A005A)
- PUBB&L-A Unit (J4A005AA)
- Control Unit (J4A005AB)

- Power Converter Unit (J4A005AD)
- Fuse Panel (J4A005AC)
- Filter Unit (J1A053AA)
- PUBB Cabling
- Growth.

PUBB Frame—J4A005A-1

3.02 The PUBB frame (Figure 4) is 7 feet high and 4 feet 4 inches wide. The frame consists of two identical but functionally independent bays, designated bay 0 and bay 1. Bay 0 and bay 1 are functionally associated with PUB 0 and PUB 1, respectively. Each bay of a fully equipped PUBB frame consists of the following:

- Four peripheral unit bus branching and loop-around (PUBB&L-A) units—J4A005AA-1
- One control unit — J4A005AB-1
- One fuse panel — J4A005AC-1
- One power converter unit — J4A005AD-1
- One filter unit — J1A053AA-1.

The location of subassemblies mounted on a frame and the location of apparatus mounted on a subassembly are determined by the coordinate numbering plan described in 254-200-001, *1B Processor, General Description*.

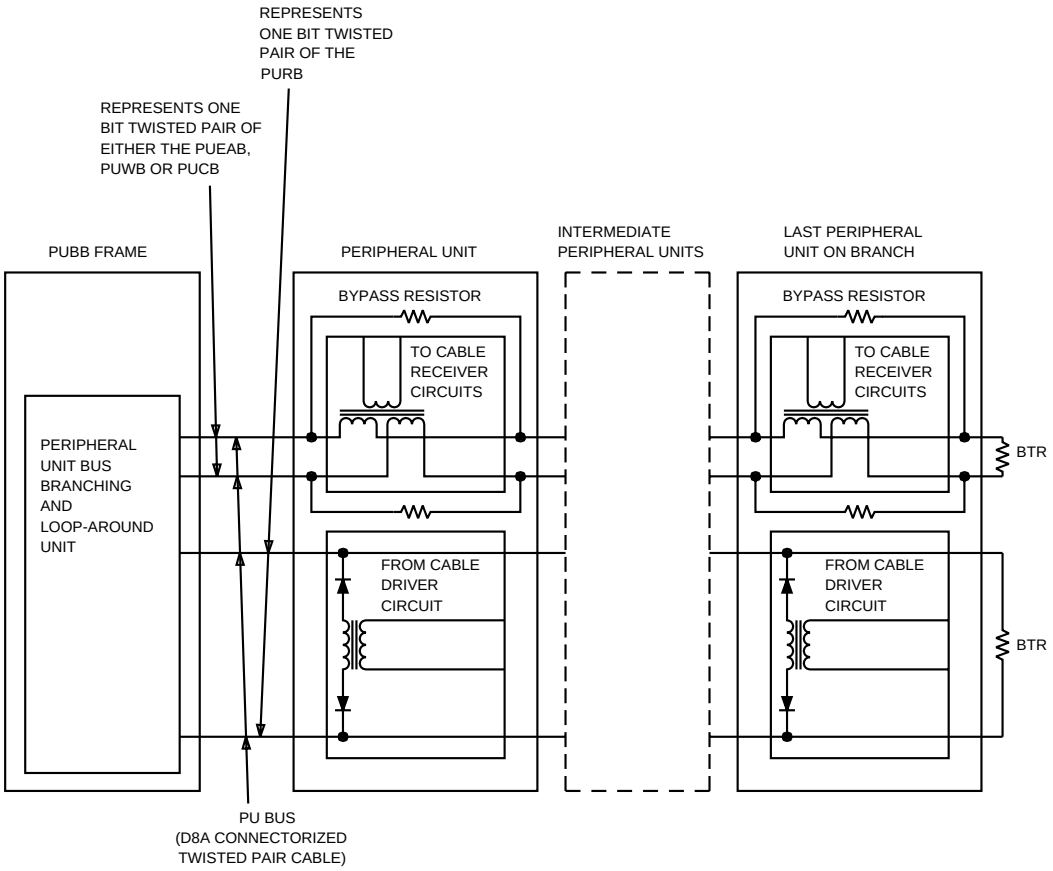


Figure 3. Peripheral Unit Bus Interface Diagram

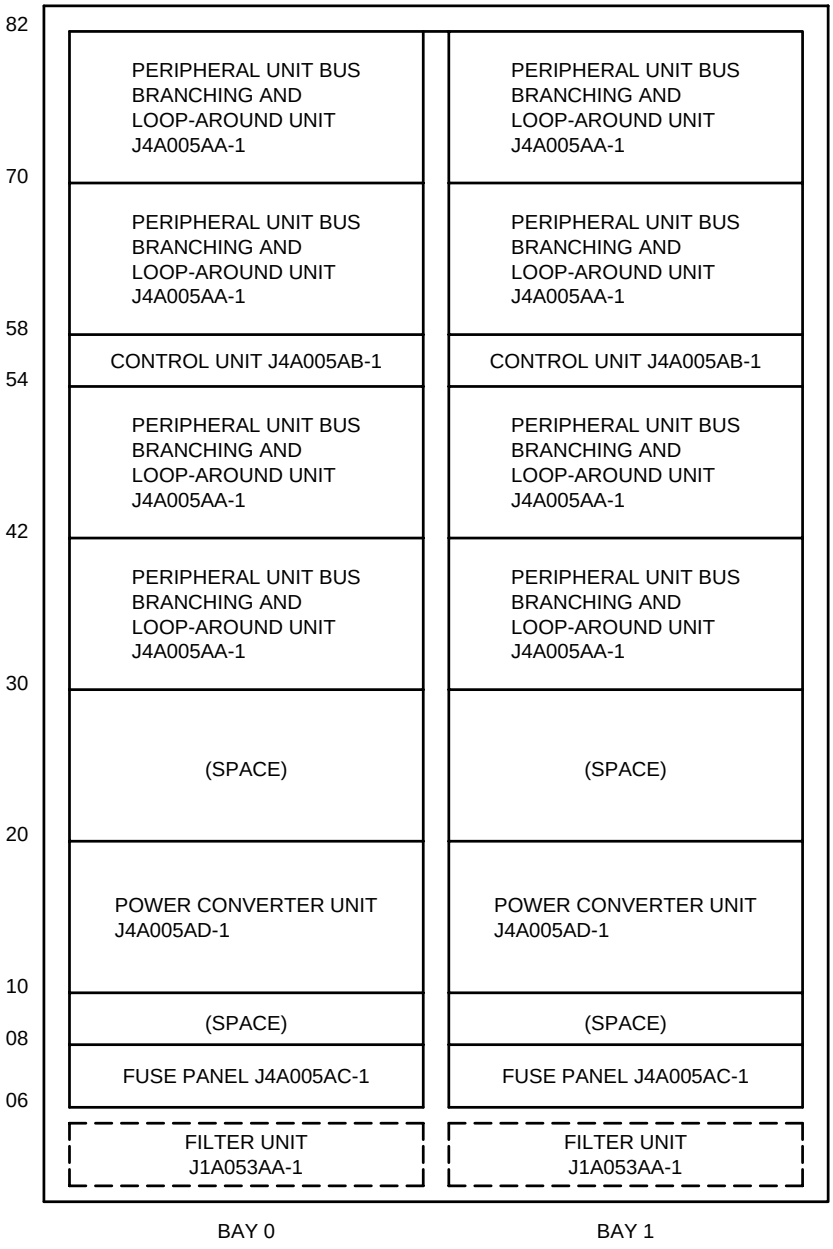


Figure 4. Peripheral Unit Bus Branching Frame J4A005A—Equipment Identification

PUBB and Loop Around (PUBB&L-A) Unit—J4A005AA-1

3.03 The PUBB&L-A unit is a 2-foot 2-inch by 1-foot mounting plate supporting a multilayer printed wiring board, nine apparatus housings, and plug-in circuit packs of the following types:

- Cable receivers
- Cable drivers
- Branch-in circuits
- Branch-out circuits
- Loop-around circuits.

Each unit provides a ***1:2 branching ratio*** (expansion-concentration ratio) of PUB 0 or PUB 1 when equipped with 50 circuit packs plus one additional circuit pack in the first unit of each bay. However, each unit is wired for a ***1:4 branching ratio***. The 1:4 branching ratio is implemented when the unit is equipped with an additional 26 circuit packs. A PUBB frame may be equipped with a maximum of eight PUBB&L-A units at equipment locations 070, 170, 058, 158, 042, 142, 030, and 130. Bus terminating resistors, initially supplied with the PPI frame, are installed on the last PUBB&L-A unit in series with the primary PUB (PUB 0 or PUB 1) from the 1B Processor (Figure 2). All equipped PUB output branches of each PUBB&L-A unit must also be terminated with BTRs. These BTRs, supplied with the PUBB&L-A unit, are installed at the last peripheral unit on each PUB output branch. Equipped but unused PUB output branches are terminated with BTRs at the PUBB&L-A unit. One ***FB152*** circuit pack, installed in the initial PUBB&L-A unit of each bay, is equipped with an alarm lamp indicator. Table A describes the functions of the PUBB&L-A unit alarm lamp indicator.

Table A. Peripheral Unit Bus Branching Frame Controls and Indicators

Assembly		Control/Indicator		
Name	**EQPT POS NO. (VERT)**	**Name**	**Type**	**Function**
Power Switch KS-20738	054, 154	-	-	Refer to 254-200-001 for identification and function of power switch controls and indicators.
3V DC-DC Converters	012, 112, 017, 117	-	Lamp Indicator (Red)	When lighted, indicates a converter Power Alarm (PA) or Fuse Alarm (FA) condition.
12V Reference Supply (FB152 Circuit Pack)	072, 172	-	Lamp Indicator (Red)	When Lighted, indicates a reference supply alarm (fuse alarm condition).
Fuse Panel	006, 106	+24V and +140	Plastic Indicator	When protruding from fuse holder, indicates a blown fuse.

Control Unit—J4A005AB-1

3.04 Each bay of the PUBB frame is equipped with a control unit mounted at vertical location 54. The control unit (Figure 5) consists of a KS-20738, L4 power switch, relays, and two terminal strips. Each unit provides power control, alarm, and test functions for the associated bay. A telephone and teletypewriter (TTY) jack assembly is provided on the bay 0 control unit only. Identification and function of the power switch controls and indicators are described in 254-200-001, *1B Processor, General Description*.

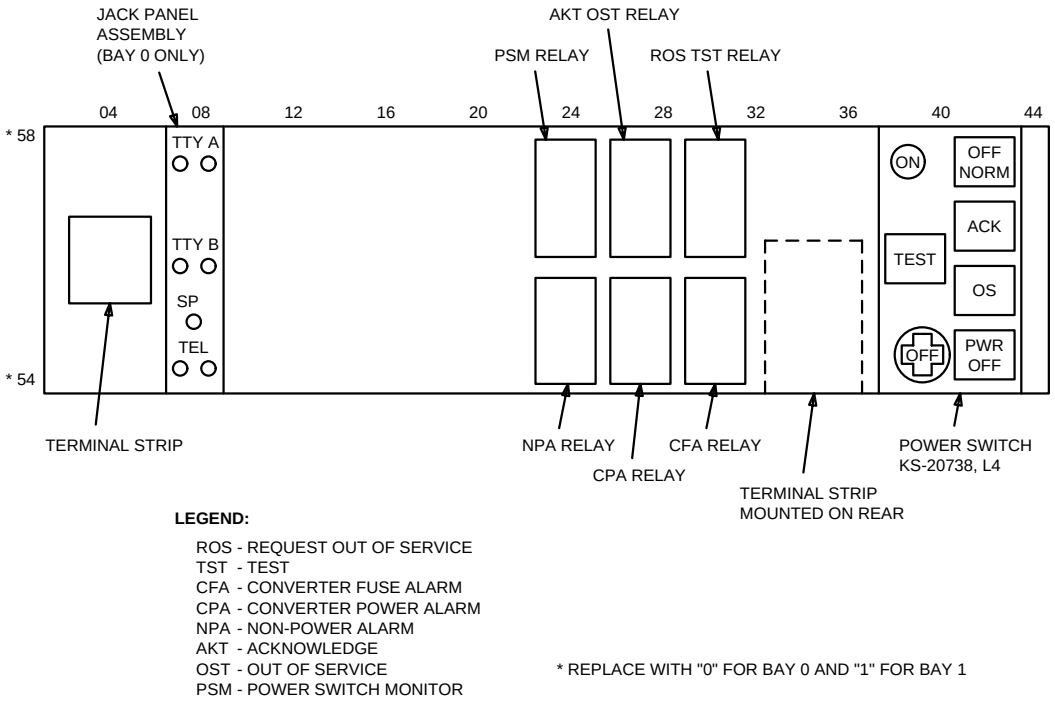


Figure 5. Control Unit J4A005AB-1—Equipment Identification

Power Converter Unit—J4A005AD-1

3.05 Each bay of the PUBB frame is equipped with a power converter unit, mounted at vertical location 10. This unit provides housing for 12 plug-in 3V DC-to-DC converters as shown in Figure 6. Three 3V/4A DC-to-DC converters (J87407A) are required for each PUBB&L-A unit with which the PUBB frame is equipped. Each 3V DC-to-DC converter is equipped with an alarm lamp. Table A describes the functions of the power converter unit alarm lamp indicator.

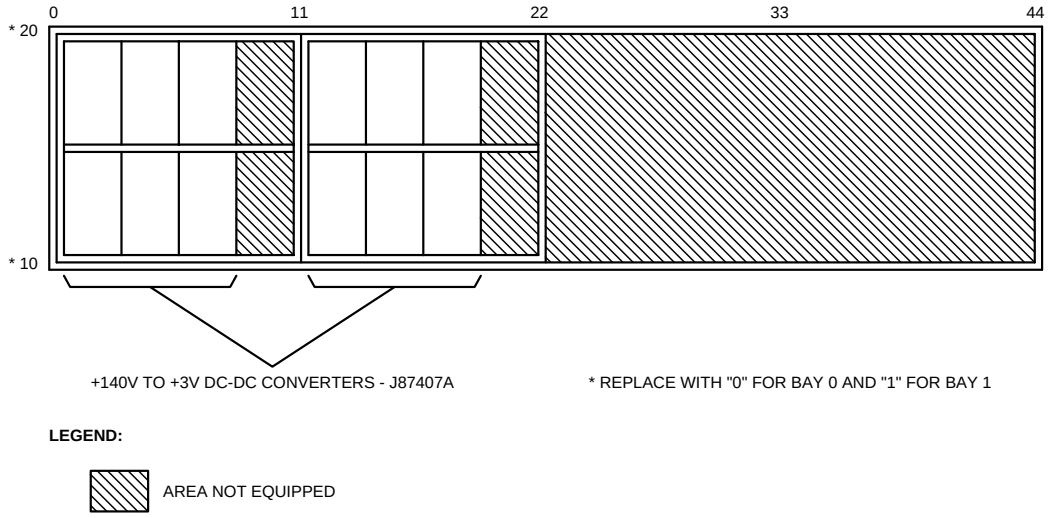


Figure 6. Power Converter Unit J4A005AD-1—Equipment Identification

Fuse Panel—J4A005AC-1

3.06 Each bay of the PUBB frame is equipped with a fuse panel (Figure 7) mounted at vertical location 06. This unit consists of four fuse blocks, one +140V fuse alarm relay, and two resistors associated with the +140V fuse alarm relay. Both +24V and +140V fusing and fuse alarm circuits are provided.

Filter Unit—J1A053AA-1

3.07 The base of each bay of the PUBB frame is equipped with a J1A053AA-1 filter unit. Each filter unit is equipped with a relay to provide switched +24V to the associated fuse panel. Filtering is provided for both switched and unswitched +24 volts.

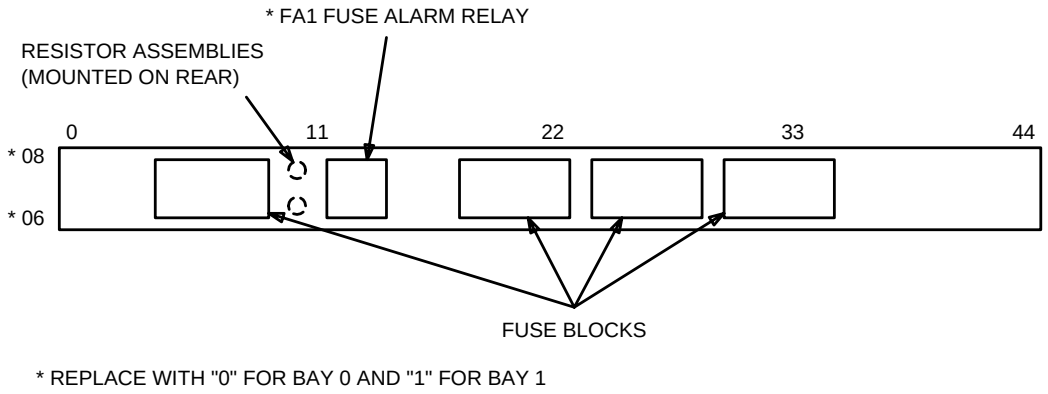


Figure 7. Fuse Panel J4A005AC-1—Equipment Identification

PUBB Cabling

3.08 D8A connectorized cables are utilized for all 4ESS Switch PUB cabling. Each D8A cable contains eight twisted conductor pairs which provide a transmission path for eight bits of information. Each cable is terminated at both ends with a female (2 rows, 10 pin-chucks) connector which may be plugged directly onto one quadrant of pins on the rear of a 947C (1A-82 pin) connector (Figure 8) utilized by all 4ESS Switch PUB access circuits. Cable driver and cable receiver circuit packs used in the 4ESS Switch each mate with a 947C connector and contain the circuitry for eight bus bits.

3.09 PUB 0 and PUB 1 are each composed of twelve D8A cables, designated group 0 through group 11. Each PUB is organized into four functional groupings (Table B). The PUEAB consists of two D8A cables which carries the peripheral unit name code from the 1B Processor, in addition to an Input/Output Clock High (IOCH) and Input/Output Clock Low (IOCL) clock signal for the input/output frame. The PURB consists of four D8A cables (32 bits) which carry reply information to the 1B Processor (three signal leads are not used). The PUWB carries write data and the PUCB carries polling signals from the 1B Processor to the peripheral units. The PUWB bit 36 is identified as a "maintenance sync" bit and is not a functional part of the PUWB. The "maintenance sync" bit functions as a software controlled sync pulse to trigger test equipment at various frames when required by maintenance personnel. The PUWB bit 37 is not used by the 4ESS Switch.

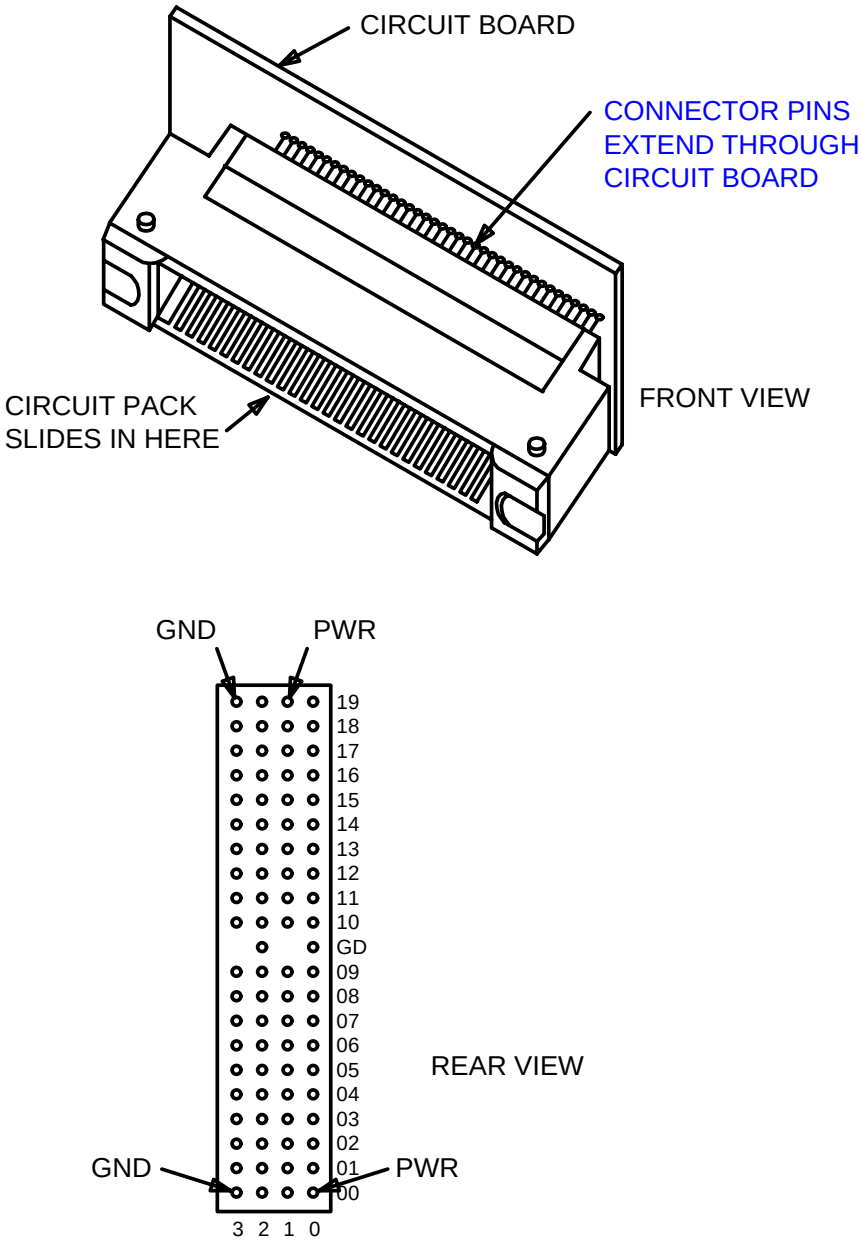


Figure 8. Type 947C (1A-82 Pin) Connector

Table B. Peripheral Unit Bus Cable Groups

Bit No.	Peripheral Unit Write Bus					Peripheral Unit Enable Address Bus		Peripheral Unit Control Bus	Peripheral Unit Reply Bus			
	Group 0	**Group 1**	**Group 2**	**Group 3**	**Group 4**	**Group 5**	**Group 6**	**Group 7**	**Group 8**	**Group 9**	**Group 10**	**Group 11**
0	PUW00	PUW08	PUW16	PUW24	PUW32	EA00	EA08	MI	PUR00	PUR08	PUR16	PUASW
1	PUW01	PUW09	PUW17	PUW25	PUW33	EA01	EA09	GI	PUR01	PUR09	PUR17	PURP
2	PUW02	PUW10	PUW18	PUW26	PUW34	EA02	EA10	CLKI	PUR02	PUR10	PUR18	APUF
3	PUW03	PUW11	PUW19	PUW27	PUW35	EA03	EA11	PHP	PUR03	PUR11	PUR19	APUT
4	PUW04	PUW12	PUW20	PUW28	PUW36 (NOTE 1)	EA04	EA12 (NOTE 3)	PLP	PUR04	PUR12	PUR20	APUB
5	PUW05	PUW13	PUW21	PUW29	PUW37 (NOTE 2)	EA05	PUSYC	PSZ	PUR05	PUR13	PUR21	D (NOTE 4)
6	PUW06	PUW14	PUW22	PUW30	PUPOD	EA06	IOCH	PDG	PUR06	PUR14	PUR22	E (NOTE 4)
7	PUW07	PUW15	PUW23	PUW31	PUPEV	EA07	IOCL	PIO	PUR07	PUR15	PUR23	F (NOTE 4)

NOTES:

1. PUW36 is the maintenance sync bit.
2. PUW37 is not used by the 4ESS switch.
3. EA12 is the maintenance mode bit (M-bit).
4. Bits D, E, and F are equipped as part of an 8-bit group but are not presently used.

3.10 Seven cables, group 0 through group 6 (PUWB and PUEAB), are engineered to identical lengths and routed to the peripheral units together. Cable group 7 (PUCB) is a single D8A cable. The PUWB, PUEAB, PURB, and PUCB of PUB0 and

PUB1 are routed to all applicable frames except the force band interface frame, which utilizes only the PURB and PUCB. All buses of a specific branch are installed via the same route through an office to serially interconnect all peripheral units assigned to that branch. The PUB branches, which serve the two base signal processor control frames, must be routed to these frames first.

Growth

3.11 A 4ESS Switch office may be equipped with additional peripheral units which require access to the PUB system. Where cable length and maximum "tapoff" restrictions are not exceeded, PUB system growth may only require additional cabling to extend the existing PUB 0 and PUB 1 branches. Extension of PUB 0 and PUB 1 from the last peripheral unit on a branch requires installation of 24 additional D8A cables to the growth peripheral unit, along with reinstallation of the BTRs at the growth unit. A growth peripheral unit may be serially connected within an existing PUB 0 and PUB 1 branch by installation of 24 D8A cables to each adjacent peripheral unit. The serial connection and routing of each PUB branch must be maintained. Since the PUB system is duplicated for reliability, the duplicity of PUB 0 and PUB 1 must be maintained when additional PUB system equipment and/or cabling are required.

3.12 There is one PUBB frame in a 4ESS Switch office. Minimum equipage of each PUBB frame bay consists of one PUBB and Loop Around unit equipped for a 1:2 branching ratio and the supporting subassemblies. The 1:4 branching ratio of each PUBB&L-A unit may be implemented with additional circuit packs and BTRs. The PUBB frame may be further equipped to provide additional PUB branches by increments of two branches per bay, up to a maximum of 16 branches per bay. The two PUBB frame bays must be identically equipped to maintain PUB system redundancy. PUBB frame growth is accomplished by equipping each bay with additional PUBB&L-A units and/or circuit packs together with the required +3V DC-to-DC converters and fuses. The primary PUB 0 and PUB 1 and the loop-around mapping select pulse point signal leads are terminated with BTRs at the last PUBB&L-A unit equipped in each bay.

3.13 In addition to the 24 D8A cables comprising the primary PUB 0 and PUB 1 between the 1B Processor PPI frame and the PUBB frame, four D8A cables are required to provide loop-around enable and loop-around mapping control signals to the initial PUBB&L-A unit equipped in each bay. These signal leads are duplicated for PUB 0 and PUB 1 to provide control of the PUBB&L-A units by either central control of the 1B Processor. Two additional D8A cables are required to apply loop-around enable signals to each additional PUBB&L-A unit from the PPI frame. Fourteen additional D8A cables are required for the extension of the primary PUB and the loop-around mapping select signals from the last PUBB&L-A unit equipped in each bay to a growth unit. The PUB branches of each growth unit are either terminated with BTRs or extended to the 4ESS Switch peripheral community with 12 D8A cables.

4. Functional Description

4.01 This part describes the functional operation of the PUB system and is divided as follows:

- **PUB functions:** Describes the purpose and functions of the four bus groups of each PUB
- **PUBB frame functions:** Describes the system interface and basic functions of the PUBB frame
- **PUBB frame expanded polling:** Describes the PUBB frame expanded polling capability
- **PUBB&L-A unit functions:** Describes the purpose and basic functions provided by this unit.

Peripheral Unit Bus Functions

4.02 Each PUB of the duplicated PUB system provides a transmission path to convey digital information in parallel form between the 1B Processor and various peripheral units in the 4ESS Switch peripheral community. Both PUB 0 and PUB 1 consist of four bus groups designated PUEAB, PUWB, PURB, and PUCB. The functions of these four bus groups are described in the following paragraphs.

4.03 The ***PUEAB*** group consists of 16 bits transmitted from the 1B Processor. Fourteen bits are used to address a specific peripheral unit type and member. This information consists of a 12 bit coded enable address (K-code), a mode bit (M-bit) that is used to indicate the mode of the accompanying peripheral order transmitted over the PUWB, and a synchronization pulse bit. The 12 bits that make up the K-code consists of 5 bits to identify the peripheral unit type and 7 bits to identify the peripheral unit member. Therefore, a maximum of 32 peripheral unit types and 128 members of each type may be uniquely addressed. The synchronization pulse is transmitted just prior to the K-code and M-bit to alert all peripheral units on the PUB system. The two remaining leads convey clock signals to the Input/Output Units (IOUs) in the input/output frame.

4.04 The ***PUWB*** group consists of 40 bits. Thirty-eight bits are transmitted from the 1B Processor at the same time the PUEAB K-code and M-bit are transmitted. This information consists of a 36 bit peripheral order (peripheral unit operation code and write data) and two parity bits. Parity is generated by the 1B Processor over the even and odd-numbered bits of the PUEAB K-code and the 36 bit peripheral order. One parity bit is generated over the even-numbered bits and the other parity bit is generated over the odd-numbered bits. This parity method is called interleaved parity. The PUWB bit 36 is a software controlled maintenance sync bit and is not operationally used by the 4ESS Switch. In addition, the PUWB bit 37 is not used.

4.05 The ***PURB*** group consists of 32 bits. Twenty-six bits convey reply information from a peripheral unit to the 1B Processor. The reply can be in response to a peripheral order received over the PUWB, or in response to a maintenance interrogation received from the 1B Processor directly or via the signal processor. The reply information consists of 24 data bits, an odd parity bit (PURB) generated by the peripheral unit over the 24 data bits, and one bit [peripheral unit all-seems-well (PUASW)] designated all-seems-well (ASW). The ASW response indicates the successful execution of a peripheral order. Three PURB bits [Autonomous Peripheral Unit Failure (APUF), Autonomous Peripheral Unit Trouble (APUT), and Autonomous Peripheral Unit Base (APUB)] convey autonomous peripheral unit trouble indicator signals via the PUCB to the 1B Processor in response to interrogation by the 1B Processor. Three PURB bits are not used in the 4ESS Switch.

4.06 The ***PUCB*** group consists of eight interrogation bits transmitted by the 1B Processor. Three of these bits are used to interrogate the autonomous peripheral units for possible trouble indicator responses and to determine the peripheral unit (group and member number) responding. Four PUCB bits are used to poll the signal processors four output buffers. The remaining PUCB bit polls the IOUs for reports and request for service. All peripheral unit reply signals, in response to interrogation signals received over the PUCB, are transmitted to the 1B Processor over the PURB.

4.07 Three methods of communication are provided by the PUB system:

- Coded enabling via the PUEAB
- Peripheral unit interrogation via the PUCB
- Maintenance access signals via the signal processor or directly from the 1B Processor.

A coded enabled peripheral unit responds when it detects a match condition between its internal hard-wired K-code and the K-code received on the PUEAB. An ASW response and, if applicable, reply information are returned to the 1B Processor on the PURB in response to the PUEAB K-code and the accompanying instruction data received on the PUWB. Interrogation signals are broadcast by the 1B Processor on the PUCB to all autonomous peripheral units which may return identifying reply signals in designated bit positions of the PURB or trouble indicator signals on the three autonomous peripheral unit trouble leads of the PURB. Maintenance reply information is transmitted on the PURB by a peripheral unit in response to a maintenance access signal received from the 1B Processor directly or via the signal processor. The fully equipped PUBB frame provides the equipment required to branch the primary PUB 0 and PUB 1 from the 1B Processor into 16 branches. The duplicated branches are routed serially to all peripheral units, in the 4ESS Switch office, that require access to the PUB. The PUBB frame consists of two functionally independent bays, designated bay 0 and bay 1. Bay 0 branches PUB 0, and bay 1 branches PUB 1. Each bay may be equipped with one to four PUBB&L-A units. Loop-around test and PURB clamp circuits are provided for diagnostic checks of the PUB and system fault isolation. These features are controlled by the 1B Processor via pulse point leads from the PPI frame. Supportive power equipment in each bay provides operating voltages for the PUBB&L-A units and frame alarms to the office alarm system.

PUBB Frame Expanded Polling

4.08 The PUBB frame expanded polling option expands the central control buffer polling capability of the Digital Interface Frame (DIF), eXpanded Time Slot Interchange (XTSI) and Service Circuit Controller (SCC) buffers to include DIF-E1 K-codes 24 through 31, and SCS 0 through 7. This option is allowed on one PUB branch per 4ESS Switch office. This expanded polling bus is restricted to TSI-B frames, DIF and DIF-E1 Frames with K-codes 24 through 31, SCS cabinets with K-codes 0 through 7, and XTSI cabinets with pseudo SP member numbers 24 through 31. Expanded polling can only be implemented on a presently unused PUB branch in the PUBB&L-A unit that is commonly equipped and wired in both bays of the PUBB frame. If an unused PUB branch is not available, a new PUBB&L-A unit must be installed in both bays of the PUBB frame or an existing branch must be unloaded by moving PU's to another branch.

4.09 The XTSI PUBB branch assignment rules follow existing DIF assignment rules. An XTSI is already assigned a pseudo SP/DIF member number for ODA trunking purposes. This pseudo SP/DIF member number should be used to assign PUBB branch routing. Any XTSI with a pseudo SP/DIF member number 2 to 23 should be attached to a normal PUBB branch. Any XTSI with a pseudo SP/DIF member number 24 through 31 should be attached to the existing Extending Polling branch that already serves the DIF in the same member number range as well as SCS frames. Assignments to new or restricted usage branches is not needed as long as the existing pseudo SP/DIF rules are followed.

4.10 The PUBB frame expanded polling capability can be applied to any available, unused PUB branch that is common to both bays in the PUBB frame. The Peripheral Unit Control Bus (PUCB) is the only bus affected on the selected branch. The Peripheral Unit Write Bus (PUWB), Peripheral Unit Enable Address Bus (PUEAB) and Peripheral Unit Reply Bus (PURB) of the selected branch remains unchanged by the expanded polling capability.

4.11 To expand the central control buffer polling to include SCS 0-7, and XTSI and DIF-E1 member numbers 24 through 31, a separate set of four pairs of leads (Poll high priority, Poll low priority, Poll seizure, and Poll digit) must be extended from the Processor Peripheral Interface (PPI) frame and connected in place of the original polling leads on the PUCB of the selected PUB branch in each PUBB bay. This PUCB and associated PUWB, PUEAB, and PURB are dedicated to XTSI and DIF-E1 frames with K-codes 24 through 31. Replies to the expanded polling on the DIF frames are on bits 0-7 of the Peripheral Unit Reply Bus (PURB).

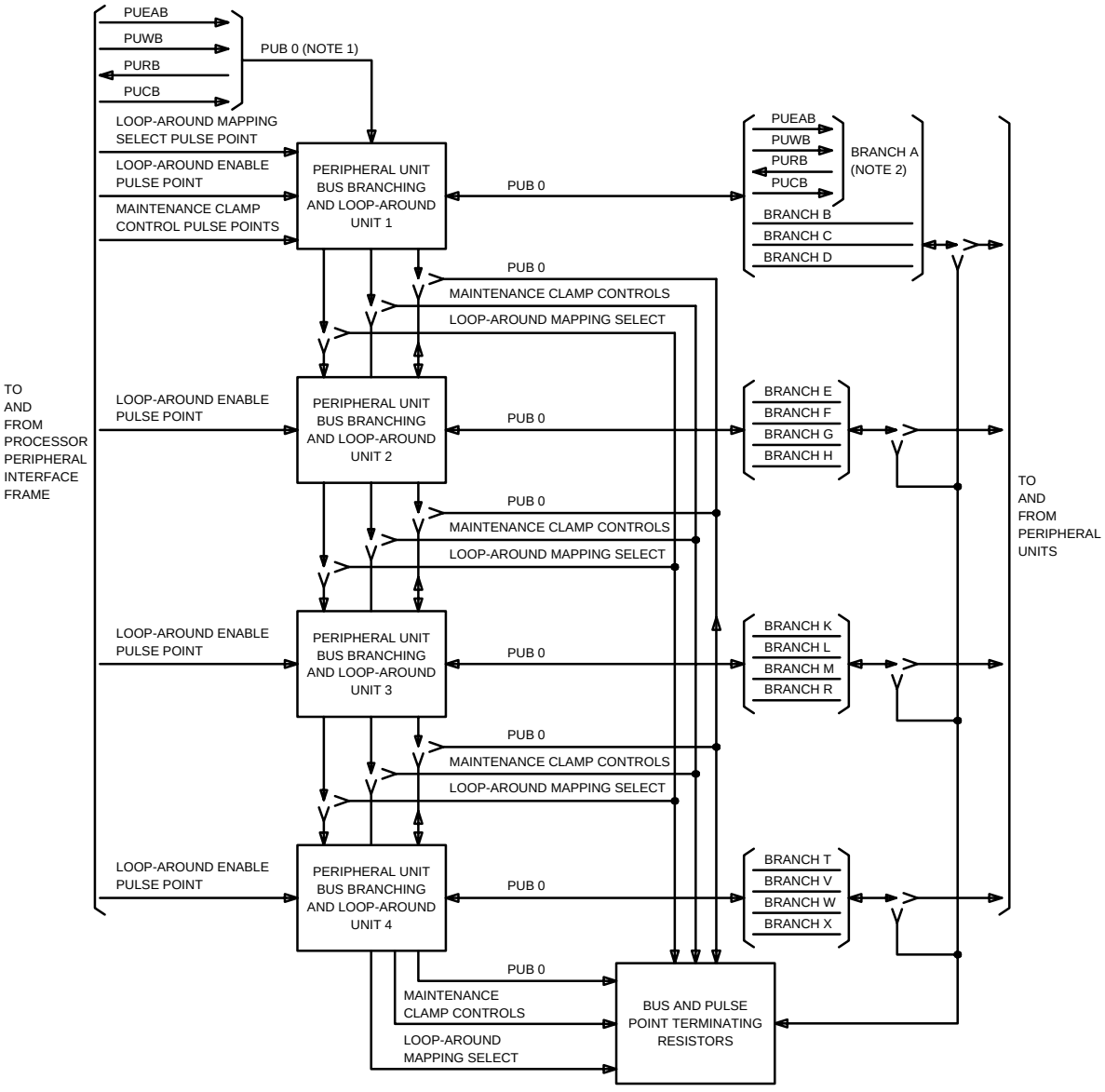
4.12 The Service Circuit System (SCS) uses the PUBB frame expanded polling option. The SCC of the SCS requires access to the PUBB arranged with the expanded polling capability to allow polling of the SCC's buffers. The expanded polling option expands the Central Control's buffer polling capabilities by extending four pairs of leads (Poll high priority, Poll low priority, Poll seizure, and Poll digit) from the Processor Peripheral Interface (PPI) frame and connecting these leads in place of the original polling leads on the PUCB of the selected PUBB branch in each PUBB bay. However, the SCC only uses two of these four buffers, Poll Low Priority and Poll Digit. The SCC

always returns a "1" (buffer empty) for the other two buffers. Replies to the expanded polling on the SCCs are on bits 8-15 of the PURB.

4.13 The PUB branch selected for expanded polling must abid by all branch length and tap-off specifications as any other PUB branch. The maximum branch length is 370 feet with 50 tap-offs or 670 feet with two tap-offs. Actual branch length is determined by the sum of the connector to connector distances of all connectorized cables from the PUBB frame to the last peripheral unit or SCS on the PUB branch plus any additional intraframe bus wiring created by multiple bus branch tap-offs within a peripheral unit on the bus branch.

PUBB&L-A Unit Functions

4.14 Since PUB 0 and PUB 1 are identical, this discussion will be based on PUB 0/bay 0 only. Each PUBB&L-A unit of bay 0 provides four identical branches of PUB 0 (Figure 9). PUB 0 is connected serially to the four PUBB&L-A units, starting with unit 1. This bus is terminated with BTRs at the last unit equipped in the bay. Equipped but unused PUB branches output from the PUBB&L-A unit must also be terminated with BTRs.



NOTES:

1. SINCE THE CIRCUITRY FOR PUB 0 (BAY 0) IS IDENTICAL TO THE CIRCUITRY FOR PUB 1 (BAY 1), ONLY PUB 0 IS SHOWN.
2. BRANCHES B THROUGH X ARE THE SAME AS BRANCH A.

Figure 9. Peripheral Unit Bus Branching Frame (Bay 0)

4.15 Each PUBB&L-A unit within the PUBB frame provides loop-around circuitry to selectively register and return the data received on the primary PUEAB, PUWB, and PUCB back to the 1B Processor on the PURB. The loop-around function provides a maintenance check of the PUB between the central control and the output side of the

PUBB frame including the cable drivers, cable receivers, and branch-in/branch-out circuitry contained in the PUBB&L-A unit. Loop-around tests are controlled via loop-around enable leads dedicated to each PUBB&L-A unit, and serially connected loop-around mapping select leads. The loop-around mapping select leads are connected to the first unit and must be terminated with BTRs at the last unit equipped in each bay. The loop-around circuits within the PUBB frame receive loop-around enable and loop-around mapping select signals from either of the duplicated central controls in the 1B Processor. However, bit patterns cannot be transmitted on one PUB and returned on the other PUB. The central control provides the loop-around enable signals and the loop-around mapping select signals.

4.16 A maintenance clamp of all PUBB&L-A units equipped in the PUBB frame is provided to prevent signals on the associated PURB branches and loop-around circuits from being transmitted on the single primary PURB to the 1B Processor. This maintenance feature is activated to stop erroneous incoming transmission, initiated by external fault conditions. The maintenance clamp feature is controlled by two serially connected pulse point leads (set maintenance clamp and clear maintenance clamp) from each central control in the 1B Processor. These leads are connected from the PPI frame to the first PUBB&L-A unit and must be terminated with BTRs at the last unit equipped in the bay.

5. Theory of Operation

5.01 The PUB system provides a transmission path to convey digital information in parallel form between the 1B Processor and various peripheral units in the 4ESS Switch peripheral community. Peripheral orders, peripheral unit address, and interrogation signals are transmitted over the PUB system from stored programs resident in the 1B Processor. Reply information is transmitted over the PUB system to the 1B Processor in response to these orders and interrogations. The PUB system is utilized only as a communication channel under 1B Processor control. Thus, the PUB system cannot generate, control, or process digital information except for the simple loop-around orders.

PUBB Frame (SD-4A019-01)

5.02 The PUBB frame consists of two identically equipped but functionally independent bays, designated bay 0 and bay 1. The PUBB frame performs two primary functions:

- Branches (expands and concentrates) PUB 0 and PUB 1 into a maximum of 16 branches of each PUB
- Provides a maintenance test of all active bus elements from central control to the output of the PUBB frame.

Bay 0 and bay 1 are functionally associated with PUB 0 and PUB 1, respectively. Since both bays are identical, this discussion is based only on the circuitry for bay 0.

A. PUBB Frame Interface

5.03 Bay 0 of the PUBB frame may be equipped with up to four PUBB&L-A units which branch the primary PUB 0 from the PPI frame into a maximum of 16 branches. The four PUBB&L-A units are designated unit 1 through unit 4. The PUEAB, PUWB, PUCB, and PURB buses that comprise PUB 0 are serially connected to each PUBB&L-A unit, starting with unit 1. Unit 1 branches PUB 0 into a maximum of four branches designated A, B, C, and D. Each succeeding PUBB&L-A unit may be equipped to provide four additional branches of PUB 0.

5.04 Pulse point signals designated loop-around mapping select and loop-around enable are routed to PUBB&L-A units to control loop-around circuits during PUB maintenance test. PUBB&L-A units contained in the PUBB frame receive loop-around enable and loop-around mapping select signals from central control. The loop-around mapping select signals are serially connected to each PUBB&L-A unit, starting with unit 1. The loop-around enable signals are connected directly to their dedicated PUBB&L-A unit. Two loop-around circuits are provided in each PUBB&L-A unit, one for every two PUB branches. The appropriate loop-around circuit may be enabled by either central control via a duplicated loop-around enable signal dedicated to each circuit. Loop-around tests are implemented by registering one of four bit mappings, one of three bit groups or all logic zeros received over the PUEAB, PUWB, and PUCB; and gating the selected bits or all zeros onto the PURB, back to the 1B Processor. One of four mappings is selected for PUBB&L-A units in the PUBB frame by either central control via four duplicated loop-around mapping select signals. The selected bit mapping, registered in all loop-around circuits, is gated onto the PURB by control of the dedicated loop-around enable signal to the desired loop-around circuit.

5.05 A maintenance clamp of all PUBB&L-A units in the bay is provided to allow central control to prevent data transmission over the PURB to the 1B Processor. This feature is activated to stop erroneous incoming transmission, initiated by external fault conditions. The maintenance clamp feature is controlled by two pulse point leads from each central control in the 1B Processor, designated set maintenance clamp and clear maintenance clamp. These leads are serially connected to each PUBB&L-A unit, starting with unit 1.

B. PUB and Pulse Point Terminating Resistors

5.06 All PUB and pulse point signals are terminated with 100-ohm BTRs, mounted on plug-on connectors. The serially connected PUB 0, loop-around mapping select, and maintenance clamp signals are terminated with BTRs at the output of the last PUBB&L-A unit equipped in bay 0. The loop-around enable signals are terminated with BTRs at each PUBB&L-A unit. All PUB 0 branches are terminated with BTRs either at the last peripheral unit on each branch or for unused but equipped branches, at the PUBB&L-A unit.

PUBB&L-A Unit (SD-4A038-01)

5.07 The PUBB&L-A unit consists of the circuitry required to branch-out the primary PUB (0 or 1) PUEAB, PUWB, and PUCB into two or four output branches and branch-in two or four associated PURB branches to the primary PUB. Each PUBB&L-A unit also provides the loop-around circuitry required to selectively register and return the data received on the primary PUEAB, PUWB, and PUCB back to the 1B Processor on the PURB during PUB maintenance tests. The loop-around test feature is required to test all active elements of each PUBB&L-A unit since the branching circuits are in series with the information flow between the 1B Processor and the 4ESS Switch peripheral community. In addition, each PUBB&L-A unit includes circuitry to implement the maintenance clamp feature.

A. PUB Branch-Out Circuit

5.08 Each bit of the PUEAB, PUWB, and PUCB of the primary PUB is serially routed through the input of a cable receiver (one for each bit) of each PUBB&L-A unit, starting with unit 1. Each of these bits is terminated with a BTR at the output of the last PUBB&L-A unit installed in a bay. Figure 10 illustrates the circuitry required to branch-out each of these bits. Each of the two cable drivers provide the drive for two output branches, one of which is routed through a cable receiver "tapoff" for the loop-around test feature.

B. PUB Branch-In Circuit

5.09 Reply data on four PURB branches entering each PUBB&L-A unit is branched-in (concentrated) to form one PURB. PUBB&L-A units within the PUBB frame concentrate PURBs to form the primary PURB. The primary PURB is routed through each PUBB&L-A unit within the PUBB frame and then to the PPI frame, starting with the last unit installed in a bay. Each primary PURB bit is terminated with a BTR at the last unit installed in a bay. Figure 11 illustrates the circuitry required to branch-in each of these bits. Each of the two shunt-type cable receivers serve to branch-in two PURB input branches, one of which is routed via the output of a cable driver for return of loop-around test data. The output, of the two cable receivers, is terminated with a diode clipping board and fan-in gate which provide the drive to the single cable driver required for each reply bit. The cable driver output is shunt connected across the balanced reply bit signal leads of the PURB. The fan-in circuit also includes a single pulse-controlled maintenance clamp flip-flop which may be set to inhibit all inputs to the primary PURB cable drivers.

C. PUB Branch A & B and Branch C & D Loop-Around Circuit

5.10 Two independent loop-around circuits are provided in each PUBB&L-A unit. Each circuit serves to selectively register 24 bits of data received from two of the four PUB output branches (A & B or C & D) and return the registered data via the branch-in circuit to the 1B Processor. Either circuit may be independently enabled by the 1B Processor. Since the loop-around circuitry for branch A & B and branch C & D are

identical, only branch A & B will be described.

5.11 The loop-around circuit contains a 24 bit loop-around register with a gated output to cable drivers. The loop-around circuitry for branch A & B is divided into two identical sections, one of which is illustrated in Figure 12. Each bit of PUB output branch A and B is connected through a cable receiver to a dedicated bit of the 24 bit register via a gated input circuit. Selection of bits to be registered is controlled by a 2 bit mapping select register provided in each of the two sections. A duplicated set of four loop-around mapping select signals is used to set the 2 bit mapping select registers to one of four logic states: inhibit and mappings 1, 2, and 3. The three-bit mappings which may be registered and returned to the 1B Processor are illustrated in Figure 13. Each loop-around mapping select signal selects one of the four loop-around states. The inhibit state inhibits the 24 bit register inputs which results in all zeros being returned to the 1B Processor. Since the four loop-around mapping select signals are serially connected to each PUBB&L-A unit, the selected bit mapping is registered in each 24 bit loop-around register.

5.12 A duplicated loop-around enable signal (one from each central control) is dedicated to each 24 bit loop-around circuit of each PUBB&L-A unit) to enable a loop-around test of either PUB branch A and B or C and D. This signal, routed to both sections of the 24 bit loop-around register, gates the registered bit mapping (or all zeros) to the reply bus cable drivers for return to the 1B Processor. A clearing flip-flop is provided in each section of the 24 bit loop-around circuit to reset the 24 bit register in preparation for incoming data. The trailing edge of the loop-around enable signal or either of the four loop-around mapping select signals will set the two clearing flip-flops. The clearing flip-flops are, in turn, cleared by a reset condition of all 12 bits of its associated 12 bit register.

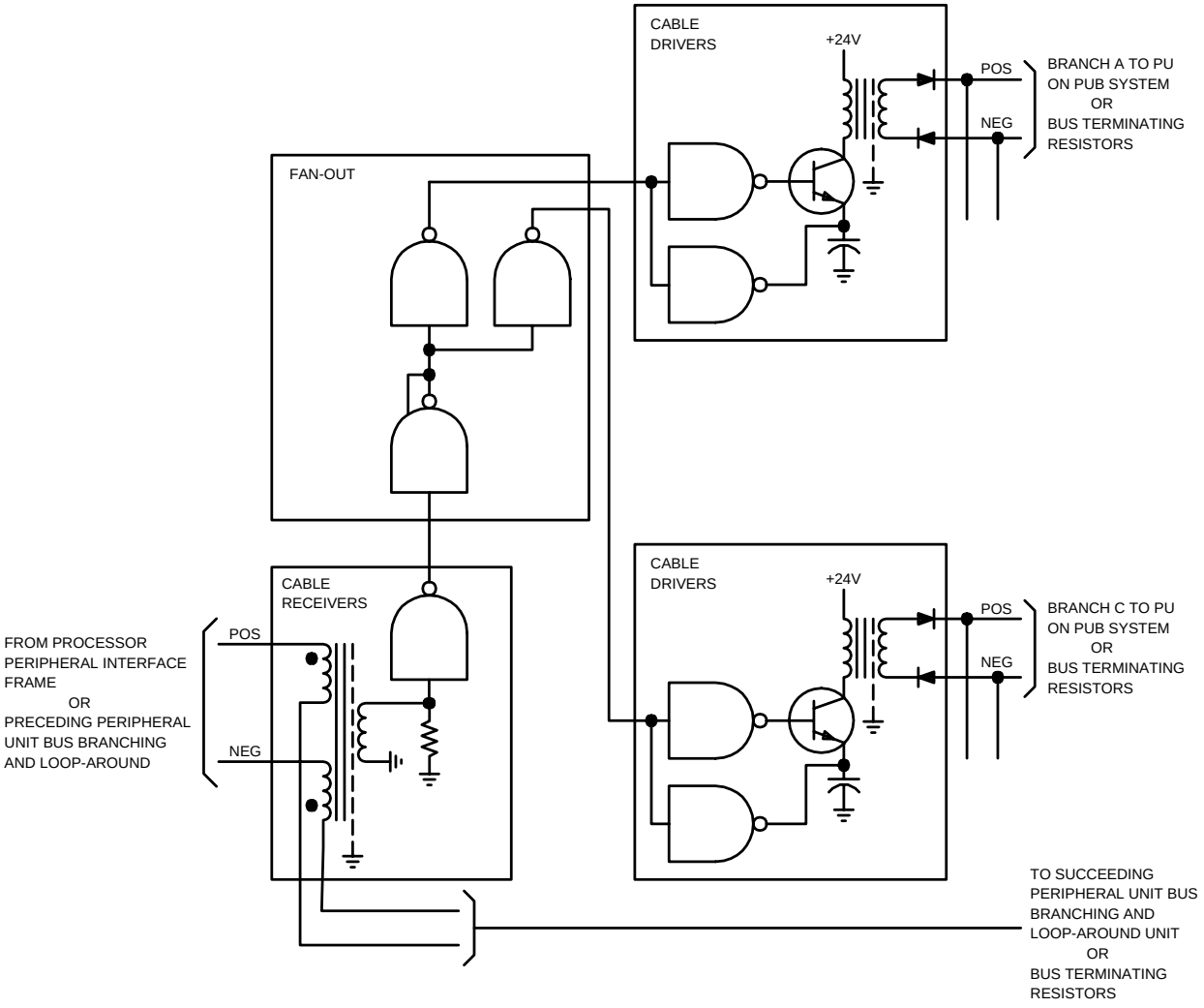
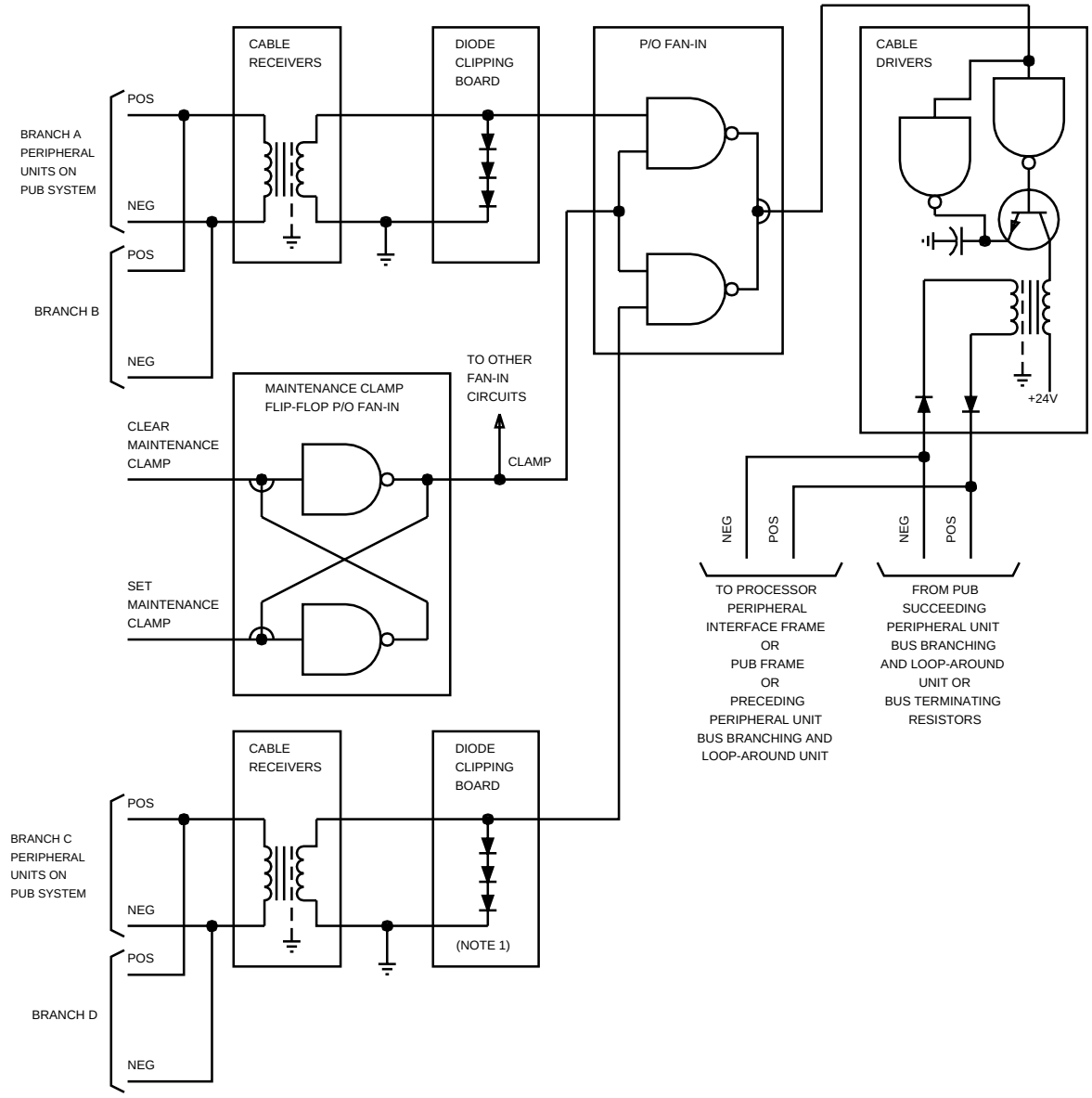


Figure 10. Peripheral Unit Bus Branch-Out Circuit — Composite Diagram



NOTE: REPLACE WITH BUS TERMINATING RESISTOR BOARD WHEN BRANCHES C AND D ARE UNEQUIPPED.

Figure 11. Peripheral Unit Bus Branch-In Circuit — Composite Diagram

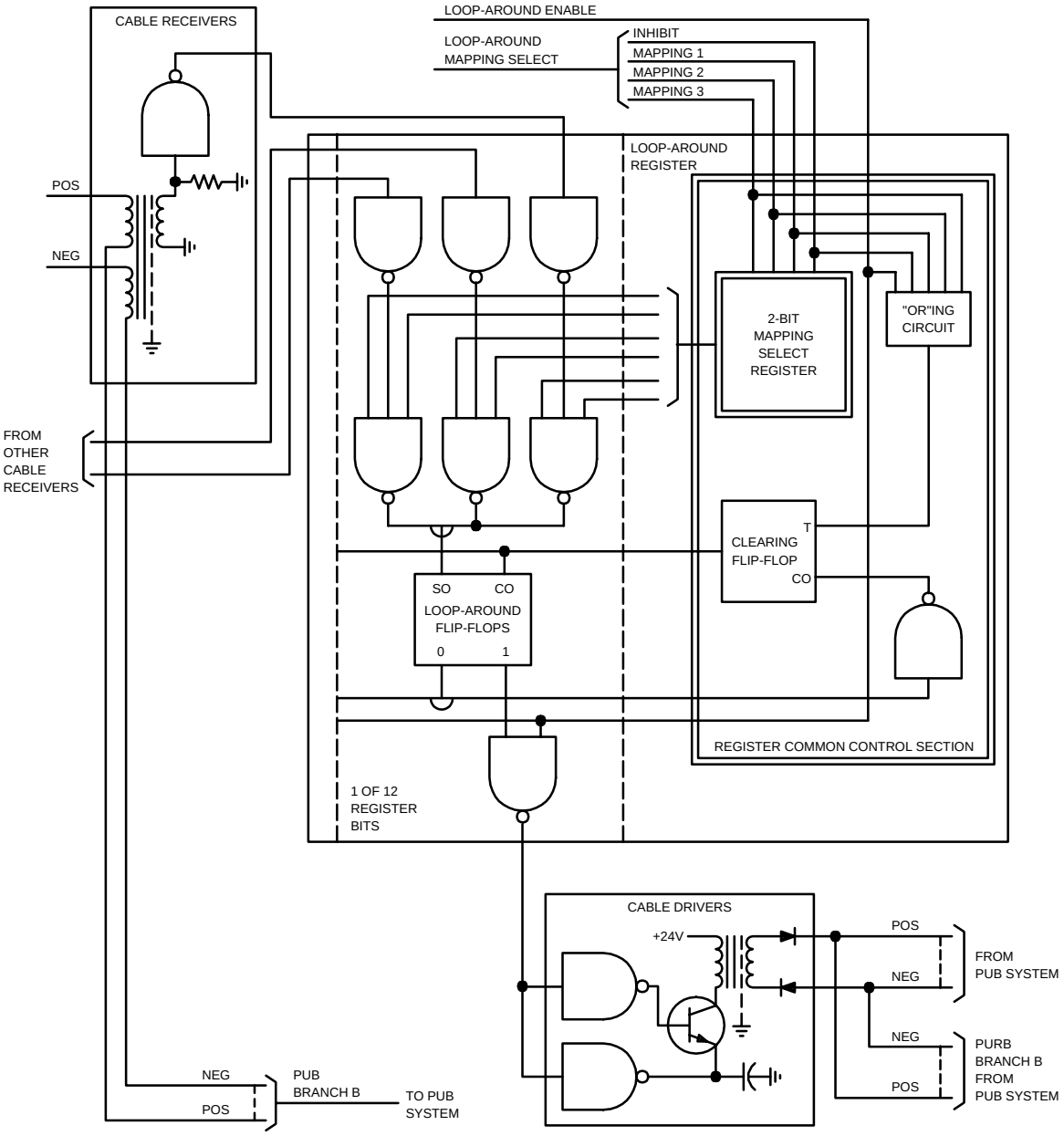
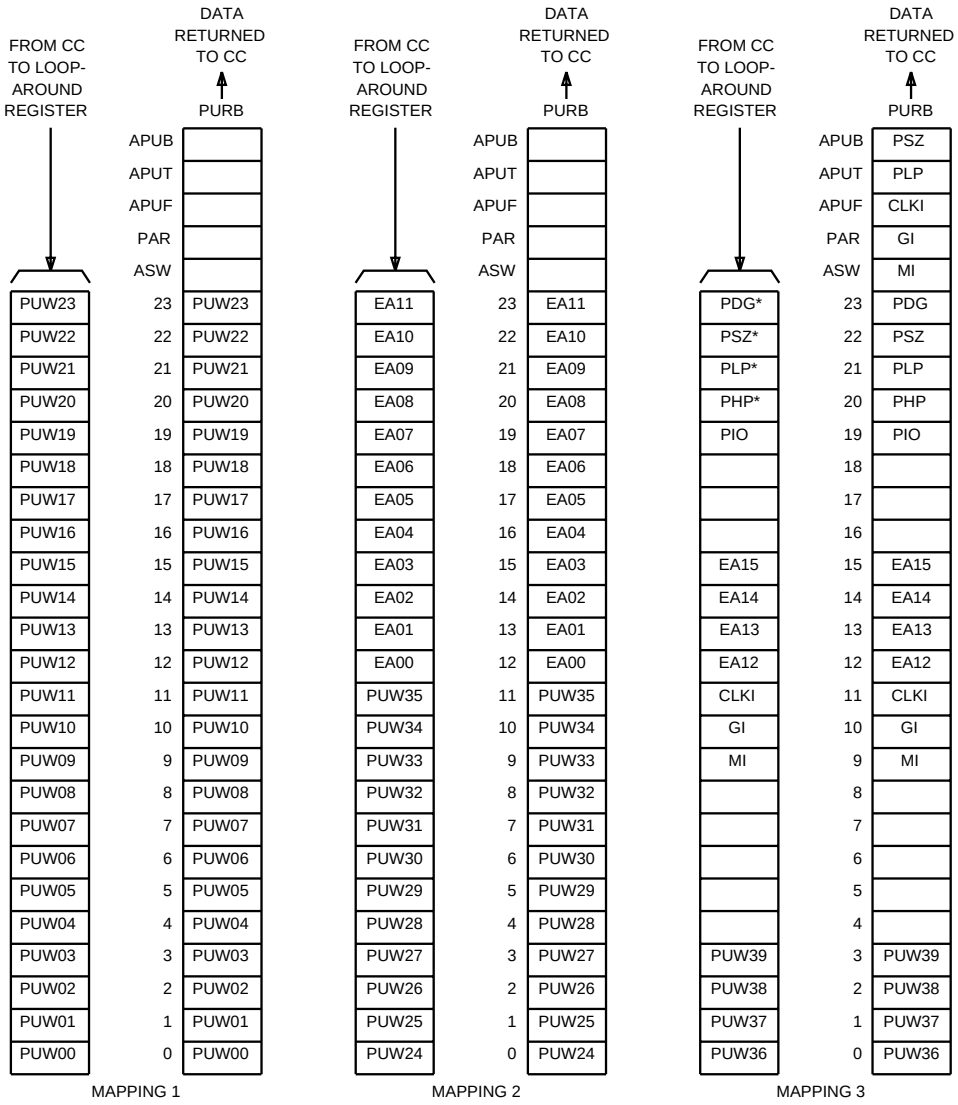


Figure 12. Peripheral Unit Bus Branch A and B Loop-Around Circuit — Composite Diagram



* FOR EXPANDED POLLING BRANCH(ES), ONLY THE ORIGINAL PDG, PSZ, PLP, PHP BITS ARE LOOPED CHECKED BY THE PUB DIAGNOSTIC. THE NEW EXPANDED PDG'; PSZ'; PLP'; PHP' BITS ARE NOT LOOPED AND MUST RELY ON THE DIF-E1 (24-31) AND SCS (0-7) DIAGNOSTIC FOR INTEGRITY CHECKS.

Figure 13. Peripheral Unit Bus Branching Frame Loop-Around Mappings (PUB Diagnostic)

D. PUB Loop-Around and Enable Circuit

5.13 The PUB loop-around and enable circuits receive the loop-around mapping select and enable signals and distribute them to the control sections of the two 24 bit loop around registers for use as previously described. The loop-around and enable circuits also receive the set and clear maintenance clamp signals for distribution to the PUB branch-in circuit. The two duplicated sets of dedicated loop-around enable signals are connected directly from the PPI frame to cable receivers (Figure 14) for distribution to their associated loop-around circuit. The BTRs are provided to terminate these four input signals. Each of the four duplicated loop-around mapping select signals and the two duplicated maintenance clamp signals are serially connected through a cable receiver in each PUBB&L-A unit, starting with unit 1. The BTRs terminate these signals at the last unit installed in a bay. The four loop-around mapping select signals are fanned-out to all loop-around circuits for selection of the bit mapping to be registered.

PUB Cabling

5.14 Each bus group of the duplicated PUB conveys specific types of digital information as illustrated in Figure 15. Each bus group is comprised of one or more D8A cables, each of which conveys eight bits.

A. Peripheral Unit Enable Address Bus

5.15 The PUEAB consists of 16 bits transmitted from the 1B Processor. Fourteen bits are used to address a specific peripheral unit type and member. This information consists of a 12 bit coded enable address (K-code), a maintenance mode bit (M-bit) that is used to indicate the mode of the accompanying peripheral order transmitted over the PUWB, and a sychronization bit. The 12 bit coded enable address (K-code) consists of 5 bits to identify the peripheral unit type and 7 bits to identify the peripheral unit member. Therefore, a maximum of 32 peripheral unit types and 128 members of each type may be uniquely addressed.

5.16 The synchronization bit is a pulse transmitted just prior to the PUEAB K-code and M-bit, and the accompanying peripheral order on the PUWB. This pulse is used by all peripheral units on the PUEAB and PUWB to initiate a short time interval during which the K-code, M-bit, and peripheral order is registered. Each peripheral unit controller then compares the received K-code with its wired K-code (unit type and member numbers) to determine whether or not it was addressed. When the received K-code fails to match the wired K-code, the peripheral order is ignored by the peripheral unit controller.

5.17 In a duplicated peripheral unit in which both controllers may operate in a duplex mode, an identical wired K-code is assigned to both controllers to permit the simultaneous acceptance and execution of a single peripheral order. In order to uniquely address one or the other controller of a pair, all peripheral orders are catagorized as either operational (normal) or maintenance orders. Operational orders are the routine instructions transmitted from the 1B Processor for normal call processing and related control functions. All other peripheral orders are maintenance orders utilized by the

maintenance and diagnostic programs stored in the 1B Processor. The mode of an order is indicated by the logic state of the M-bit (PUEAB bit 12). The M-bit is set (equal to one) for maintenance orders and reset (equal to zero) for operational orders. Each peripheral unit controller contains a Maintenance Access (MA) flip-flop which is under control of the 1B Processor. If maintenance access is set, the controller is in the maintenance mode. The maintenance access flip-flop in each peripheral unit controller and the M-bit provide the mechanism to individually address a specific peripheral unit controller.

5.18 The two remaining PUEAB bits, input/output clock high and input/output clock low, are high and low speed clock pulses generated by central control in the 1B Processor. These clock pulses are utilized by the input/output units in the input/output frames only.

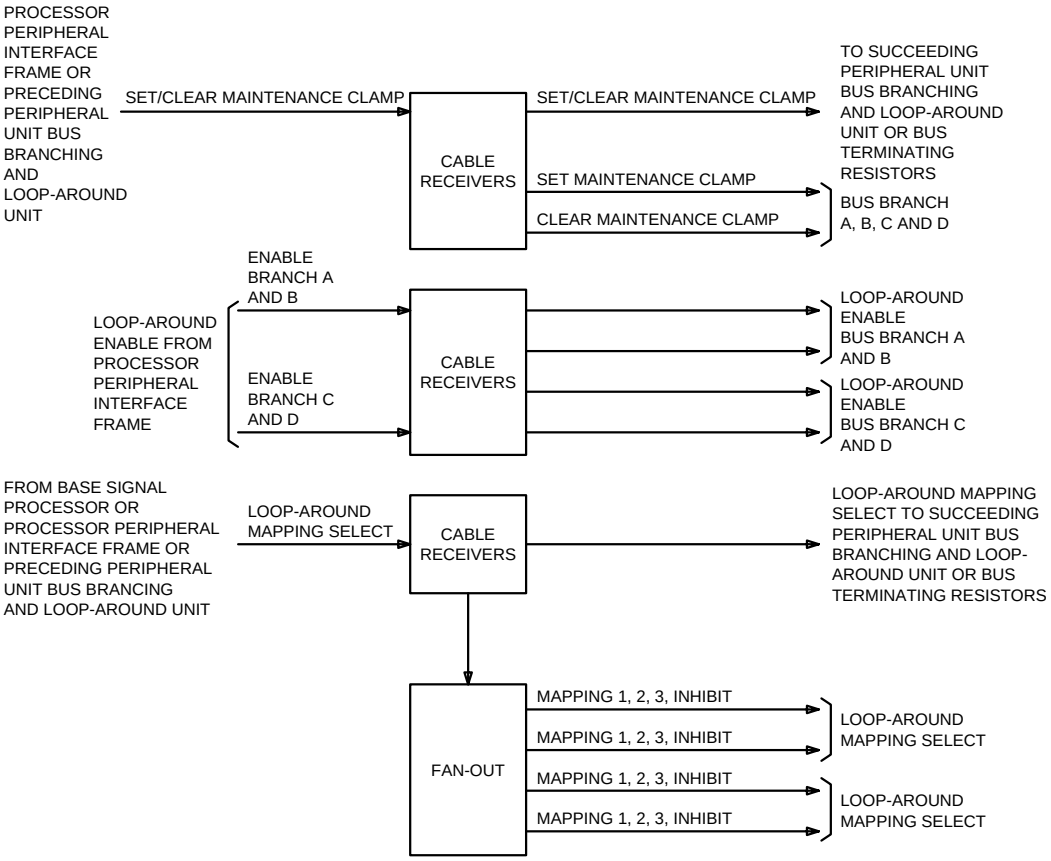
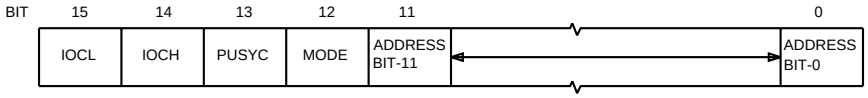


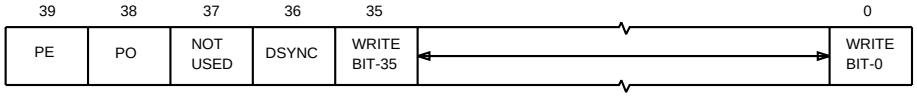
Figure 14. Peripheral Unit Bus Loop-Around Select and Enable Circuit — Composite Diagram

PERIPHERAL UNIT ENABLE ADDRESS BUS



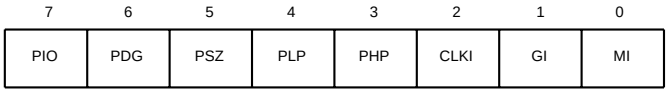
LEGEND:
IOCL = INPUT/OUTPUT CLOCK LOW
IOCH = INPUT/OUTPUT CLOCK HIGH
PUSYC = SYNC PULSE (OPENS DATA WINDOW)

PERIPHERAL UNIT WRITE BUS



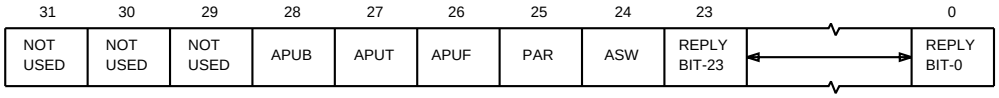
LEGEND:
DSYNC = DIAGNOSTIC SYNC
PE = ODD PARITY OVER EVEN BITS
PO = ODD PARITY OVER ODD BITS

PERHPHERAL UNIT CONTROL BUS



LEGEND:
PIO = POLL INPUT/OUTPUT
PDG = POLL DIGIT
PSZ = POLL SEIZURE
PLP = POLL LOW PRIORITY
PHP = POLL HIGH PRIORITY
CLKI = CLOCK INTERROGATE
GI = GROUP INTERROGATE
MI = MEMBER INTERROGATE

PERIPHERAL UNIT REPLY BUS



LEGEND:
APUB = AUTONOMOUS PERIPHERAL UNIT BASE
APUT = AUTONOMOUS PERIPHERAL UNIT TROUBLE
APUF = AUTONOMOUS PERIPHERAL UNIT FAILURE
ASW = ALL-SEEMS-WELL
PAR = ANSWER PARITY

Figure 15. Peripheral Unit Bus Bit Formats

B. Peripheral Unit Write Bus

5.19 The PUWB consists of 40 bit positions. Thirty-eight bits are transmitted from the 1B Processor at the same time the PUEAB K-code and M-bit are transmitted. This information consists of a 36 bit peripheral order (peripheral unit operation code and write data) and two parity bits. Odd parity is generated by the 1B Processor over the even and odd-numbered bits of the PUEAB K-code and the 36 bit peripheral order. One parity bit is generated over the even-numbered bits and the other parity bit is generated over the odd-numbered bits. This parity method is called interleaved parity. PUWB bit 36, maintenance sync, is used only to synchronize test equipment when performing maintenance at equipment frames and is not operationally used in the 4ESS Switch. PUWB bit 37 is not used.

C. Peripheral Unit Control Bus

5.20 The PUCB consists of eight bits which are individually transmitted by the 1B Processor to poll or interrogate all autonomous peripheral units simultaneously. PUCB bit assignments are illustrated in Figure 15. The function of each PUCB bit is as follows:

- ***Clock Interrogate:*** This bit is periodically pulsed to determine whether any autonomous peripheral unit has detected a trouble which warrants an autonomous maintenance (F-level) interrupt or a lower-priority trouble report. Such autonomous peripheral unit trouble responses are transmitted to the 1B Processor over the appropriate PURB bit (26, 27, or 28).
- ***Group Interrogate:*** This bit is pulsed by maintenance programs to determine the group number of any autonomous peripheral unit that caused an interrupt or trouble report (unit type SP, TMS, TSI, etc.).
- ***Member Interrogate:*** This bit is pulsed by maintenance programs to determine the specific unit (member number) of an autonomous peripheral unit that caused an interrupt or trouble report.
- ***Poll High Priority:*** This bit is an interrogation pulse used to determine which peripheral units have a high priority buffer report.
- ***Poll Low Priority:*** This bit is an interrogation pulse used to determine which PU's have a low priority buffer report.
- ***Poll Seizure:*** This bit is an interrogation pulse used to determine which PU's have a seizure buffer report.
- ***Poll Digit:*** This bit is an interrogation pulse used to determine which PU's have a digit buffer report.
- ***Poll Input/Output:*** This bit is an interrogation pulse used to determine which input/output units, in the input/output frames, have service or maintenance requests.

Autonomous peripheral units respond to PUCB polling and interrogations, except ***Clock Interrogate,*** via assigned bit positions in the PURB data field (bit 0 through 23) to indicate requests for service or maintenance, and/or for identification.

D. Peripheral Unit Reply Bus

5.21 The PURB conveys information from the peripheral units to the 1B Processor in response to peripheral orders received over the PUWB or in response to interrogations received via:

- The PUCB
- A maintenance access pulse point directly from the 1B Processor
- A maintenance access pulse point via a signal processor.

5.22 The PURB consists of 32 bit positions. PURB bits 29, 30, and 31 are not used in the 4ESS Switch. Twenty-six PURB bits convey information from a peripheral unit to the 1B Processor in response to a peripheral order. This information consists of 24 data bits, a parity bit (odd) generated by the peripheral unit over the 24 data bits, and one bit designated All-Seems-Well (ASW). The ASW response indicates the successful execution of a peripheral order and is transmitted to the 1B Processor in response to all peripheral orders regardless of whether reply data is requested (for example, peripheral order write instructions, etc). When peripheral unit reply data is requested, the ASW response, reply data, and parity bit are transmitted at the same time.

5.23 The PURB data field (bits 0 through 23) is also used to convey peripheral unit maintenance data, requests for service or maintenance, and identification information to the 1B Processor. Specific peripheral unit maintenance data is returned to the 1B Processor in response to a maintenance access pulse point signal. Peripheral unit requests for service or maintenance and/or identification information is returned to the 1B Processor in response to polling and interrogations received over the PUCB.

5.24 The remaining three PURB bits are used to report trouble indications to the 1B Processor in response to the PUCB ***Clock Interrogate*** pulse as follows:

- ***Autonomous Peripheral Unit Failure (F-level) (APUF)*** — Reports trouble of sufficient magnitude to warrant generation of an F-level interrupt.
- ***Autonomous Peripheral Unit Trouble (APUT)*** — Reports trouble of lesser urgency than APUF and activates an interject level response from the maintenance programs.
- ***Autonomous Peripheral Unit Base (APUB)*** — Reports trouble of lesser urgency than APUF or APUT and activates a base level response from the maintenance programs.

E. PUB Access Control

5.25 The PUB system configuration is controlled by the 1B Processor. During normal system operation, one PUB is designated as the active bus; the remaining bus is designated as the standby bus. Access to the duplicated PUB by the two 1B Processor central controls is controlled by a set of route control flip-flops which are located in a buffer register in each central control. These flip-flops are designated Peripheral Unit Bus Active (PUBA), peripheral Unit Bus Output (PUBO), Peripheral Unit Bus Transmit (PUBT), and Peripheral Unit Bus Receive (PUBR).

5.26 In the normal system configuration, the state of the PUBA flip-flop determines the active bus. The active bus is the bus used by the active central control for both sending and receiving. The standby central control normally sends and receives via the standby bus. The standby bus is the bus designated by the complemented state of PUBA. To alter the normal communication paths in the peripheral system, the PUBO and PUBT control flip-flops are used. Basically, PUBO controls the sending mode of the active central control; whereas, PUBT controls the receiving function in the standby central control. When the PUBO flip-flop is set, the active central control sends on both peripheral buses rather than only on the active bus. With the PUBT flip-flop set, the standby central control receives on the active bus instead of the standby bus. In both cases (with PUBO or PUBT flip-flop set), the standby central control is prohibited from sending on either bus.

5.27 The PUBR control flip-flop permits a special mode of operation that is unique to the PUB system. When the PUBR flip-flop is set, the functions of the PUBA, PUBO, and PUBT flip-flops are overridden, and the routing established is such that the active central control sends on both buses and both central controls receive on both buses. This special mode is provided to handle certain trouble situations that can arise from the sharing of bus receivers and bus drivers between controllers in peripheral units.

5.28 The PUCB group interrogate, member interrogate, and the four PUCB poll buffer bits are driven by central control pulse point sources. These pulse point sources are normally triggered only by the active central control. To ensure that all peripheral units are interrogated, these bits plus the clock interrogate bit, are transmitted on both buses independently of the central control peripheral routing flip-flops. However, central control routing flip-flops PUBA, PUBT, and PUBR determine the PURB on which the autonomous peripheral unit trouble indicator bits are received.

5.29 Peripheral unit access to PUB 0 and PUB 1 is controlled by three route control flip-flops in each peripheral unit controller. These flip-flops, designated RO, S0, and S1, provide each controller in a duplicated peripheral unit with independent access to the PUEAB, PUWB, and PUCB of PUB 0 or PUB 1; and to either, neither, or both PURBs. The logic state of the RO flip-flop in each controller determines which bus that controller is to listen to when receiving information from the 1B Processor. The S0 and S1 flip-flops in each controller determine which bus or buses to reply on when responding to the 1B Processor. Each peripheral unit controller also contains a Maintenance Access (MA) flip-flop. The MA flip-flop is used for maintenance access and does not directly control bus routing. The logic states of all four flip-flops (MA, RO, S0 and S1) are controlled via peripheral order write instructions or a maintenance access pulse point, respectively. When the maintenance access pulse point to a controller is pulsed, the RO flip-flop is toggled, the logic states of all four flip-flops, plus other maintenance information, are gated onto the PURB according to the toggled state of RO. The logic states of these flip-flops can also be determined by a peripheral order read instruction from the 1B Processor.

5.30 Peripheral unit access to all PUCB bits of either PUB 0 or PUB 1 is controlled by the state of the RO flip-flop. However, peripheral unit response to the three PUCB interrogation bits is routed to the 1B Processor over both reply buses, independently of the states of flip-flops S0 and S1. Routing of peripheral unit responses to the PUCB

polling bits is controlled in the normal manner by the states of flip-flops S0 and S1. When the MA flip-flop is set in a peripheral unit controller, response to any of the PUCB bits is inhibited.

F. PUB Electrical Characteristics

5.31 The electrical characteristics of the pulses carried by the PUB cabling are specified for compatibility with the electrical characteristics of the cable driver and cable receiver circuits. Pulses transmitted over the PUB cabling must be 9.6V peak to peak with a nominal pulse width of 500 ns at the output of the cable drivers. These pulses must also have a rise time equal to or less than 100 ns from the 10 to 90 percent points. Data received on the PUB must be at least 3.5V peak to peak for 300 ns at the input to the peripheral unit cable receivers. The branches of the PUBB frame are limited to 450 cable feet with up to 50 "tapoffs" or 750 cable feet with up to 2 "tapoffs." The PUB cabling propagation delay must be less than 2.0 ns per foot and cable loss must be less than 1.0 dB per 100 feet. PUB cabling characteristic impedance is nominally 100 ohms.

5.32 The maximum permissible branch bus length is not totally determined by the number of "tapoffs" that a cable driver can feed, nor by the attenuation due to cable length. Cable propagation delays and peripheral unit operating times versus the maximum time-out interval allowed by the 1B Processor for the completion of a peripheral order is of equal importance. It would be possible for the 1B Processor to send two peripheral orders 2.8 μs apart. However, because of PUB transmission time, the ASW signal in response to most orders does not arrive for several microseconds. The 1B Processor requires that the ASW response to a peripheral order arrive within thirty-two 700-ns cycles after the beginning of the order. If no ASW is received within this interval, the peripheral sequence is terminated, and the maintenance programs are notified that the order failed. It is clear that the total time available for the execution of a peripheral order is fixed by the maximum time-out interval designed into the 1B Processor. Part of this time is taken up by propagation delays introduced by:

- Cable length
- Logic delays through cable drivers and cable receivers in the 1B Processor and peripheral units
- Branch-out and branch-in stages of the Peripheral Unit Bus Branching and Loop-Around (PUBB&L-A) units of the PUBB frame.

5.33 Another factor that must be considered is the pulse delay variation (PDV) (jitter) between bus leads. Pulse delay variation is introduced by differences in logic delays through the active cable elements and by slight differences in cable length of the bus leads, especially at the bus connectors and within the bus circuit packs. Because the worst case value of PDV can be greater than the minimum pulse width, thus causing the possibility of non-overlapping pulses, the 1B Processor must transmit the sync pulse 400 ns prior to the transmission of the address and data. Upon reception of the sync pulse, the peripheral units must generate a window of at least 1 μs in width to receive the K-code and data.

5.34 The 2 bit interleaved odd parity, generated over the K-code and peripheral order data, and the single-bit parity on the reply bus should detect most bus errors caused by noise or bus trouble conditions. It is important that maintenance interrupts should not occur due to normal office noise causing bus transmission errors. Therefore, PUB cabling is routed within metal cable ducts which provide shielding against normal office noise. Removal of power or circuit packs from any frame on the PUB system, except the PUBB frame, does not break PUB continuity. Bypass resistor assemblies are connected to all bus cable receiver circuit packs. The bypass resistor assemblies provide bridging to ensure electrical continuity when a cable receiver circuit pack is removed. To keep the bus loss due to bypass resistance to an acceptable value, only one cable receiver circuit pack may be removed at a time.

6. Power

Power Requirements

6.01 Two +24V feeders and two +140V feeders from the power distribution system supply the PUBB frame power.

6.02 The +24V feeders, designated +24VA and +24VB, supply the filter unit in bay 0 and bay 1, respectively. After filtering, both switched and unswitched +24V is supplied to the associated fuse panel. The switched +24V from each filter unit is controlled by the associated control unit. This voltage is supplied to the associated +3V DC-to-DC converters and PUBB&L-A unit cable drivers. The unswitched +24V provides operating voltage for the associated power control, alarm, and test circuits, and the +12V reference circuit and power switch lamps.

6.03 The +140V feeders, designated +140VA and +140VB, supply the fuse panel in bay 0 and bay 1, respectively. This is the primary supply for the +3V DC-to-DC converters and requires no filtering.

Power and Alarm Circuits

6.04 The PUBB frame power and power alarm circuits (Figure 16) consist of:

- +140 to +3V DC-to-DC converters
- Filter units
- Fuse panels
- Control units
- +3V reference and filter circuits located in all PUBB&L-A units
- +12 reference circuit located in first PUBB&L-A unit equipped in each bay.

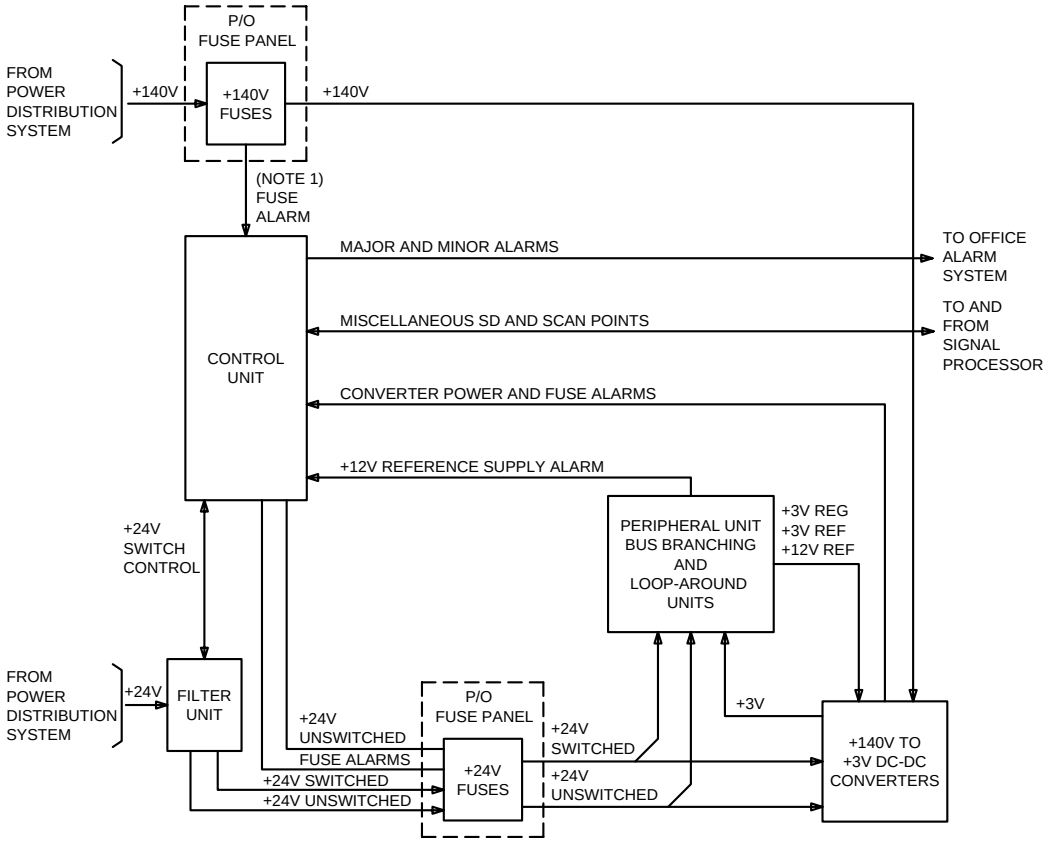


Figure 16. Peripheral Unit Bus Branching Frame Power and Power Alarm Circuits—Block Diagram

6.05 Three +3V DC-to-DC converters (J87407A) supply the power required by the +3V logic circuits in each of the PUBB&L-A units. Each of the three converters feed a portion of the associated PUBB&L-A unit backplane via two +3V filter and reference

circuits that filter the converter outputs and provide reference and sense inputs to each converter. One +12V reference circuit equipped in the first PUBB&L-A unit in each bay supplies this reference voltage to all +3V DC-to-DC converters equipped in the associated bay. Each converter contains internal current limiting and requires no output fusing. All converters and the two +12V reference circuits (***FB152*** circuit pack) contain an alarm indicator.

6.06 The filter unit, in the base of each bay, filters the associated +24V power feeder from the 4ESS Switch power distribution system. Both switched and unswitched +24V is provided to the associated fuse panel. The switched +24V is controlled by a relay in each filter unit.

6.07 The fuse panel in each bay of the PUBB frame provides distribution fusing and fuse alarms for the switched and unswitched +24V from the associated filter unit; and distribution fusing and fuse alarms for the +140V feeder which is received directly from the power distribution system. All fuses provide a plastic failure indicator.

6.08 The following are circuits that control power in each bay of the PUBB frame:

- Control unit power switch and power control, alarm, and test relays
- Fuses
- Output monitor circuits internal to each +3V DC-to-DC converter.

These circuits operate in conjunction with each other to provide the following:

- Manual control of power to each bay and automatic shutdown
- Manual and automatic Power Alarm Tests (PATs)
- Bay power status and alarm signals to the 1B Processor via two miscellaneous scan points
- Communications from the 1B Processor to each control unit via two miscellaneous Signal Distributor (SD) points (relay applique)
- Major and minor alarm signals to the office alarm system.

6.09 Each bay of the PUBB frame is equipped with a control unit. This unit provides one power switch (KS-20738, L4) and associated power control, alarm, and test relays. Each bay can only be powered up manually by operation of the power switch ON pushbutton; but it can be powered down both manually by operation of the power switch OFF pushbutton (normal power down) and automatically when an alarmed power condition occurs (alarmed condition power down). Functions of the power switch controls and indicators are described in 254-200-001, *1B Processor, General Description*.

6.10 All fuses contain an alarm contact that closes upon fuse failure and signals a fuse alarm to its associated control unit. Each +3V DC-to-DC converter contains an overcurrent (OC) and overvoltage (OV) output monitor that acts as an electronic fuse for the converter. An overcurrent or overvoltage condition causes the converter to be shut down and a Converter Fuse Alarm (CFA) signal to be sent to its associated control unit.

Each of the two +12V reference circuits contain an out-of-range voltage (OORV) output monitor. An OORV condition of either +12V reference circuit also results in a converter fuse alarm signal (reference supply alarm) to the associated control unit. Receipt of a CFA signal results in the control unit initiating an alarm condition power down and a major alarm output to the office alarm system. Each +3V DC-to-DC converter contains an OORV output monitor that outputs a Converter Power Alarm (CPA) signal to the associated control unit. The control unit outputs a minor alarm signal to the office alarm system upon receipt of a CPA from any associated converter or upon receipt of a fuse alarm from a blown +24V nonservice affecting fuse. The OORV output monitors can be tested for correct operation by performing power alarm tests.

6.11 The manual Power Alarm Test (PAT) is started by rotating the power switch OFF pushbutton to Request Out-of-Service (ROS) and depressing the TEST pushbutton for at least 0.5 second. The automatic PAT is started by a software-controlled sequence of the acknowledge (ACK) SD point followed by the Out-of-Service (OS) SD point. The control unit outputs a PAT signal to its associated converters and +12V reference circuit pack, and inhibits the resulting CPA signals from causing an office minor alarm. The +12V reference circuit CFA signal (reference supply alarm) is inhibited, thereby preventing an alarmed condition power down and a major alarm. Each properly functioning converter and +12V reference circuit pack are forced into a power alarm condition, the alarm indicator is lighted, and a low Non Power Alarm (NPA) signal is initiated. In the manual mode, test results are verified by observing that the correct alarm indicators are lighted, test restoral is accomplished by returning the OFF pushbutton to the normal position; and test restoral is verified by observing that the correct alarm indicators are extinguished, and the power switch is in the normal power on state. In the automatic mode, the test results are verified by the program via the two scan points; test restoral is accomplished by dropping OS and ACK; and test restoral is verified via the two scan points.

7. Maintenance

7.01 The primary system maintenance objective is to maintain call processing during error and/or fault conditions. To meet this objective, the following is accomplished in relation to the 4ESS Switch PUB system:

- Detection of all faults and errors
- Continuity of operation during a fault condition by automatic reconfiguration of the duplicated PUB and/or peripheral unit controllers
- Isolation of faulted equipment and removal of equipment from service via program control
- Diagnosis of faults by diagnostic program
- Repair of equipment by craft personnel
- Verification of repair by diagnostic program

- Return of repaired equipment to service.

7.02 Craft personnel are alerted to fault or error conditions by office alarms and/or TTY output messages. The messages include trouble locating information consisting of circuit packs to be replaced.

7.03 The 4ESS Switch maintenance philosophy and maintenance facilities are described in 234-100-000, *4ESS™ Switch, General Description*.

7.04 The Maintenance Operations Center (MOC) is responsible for maintenance and repair of the PUB system equipment.

Maintenance Software

7.05 Error and/or fault conditions in the PUB system are primarily detected by parity checks of the data transmitted between the peripheral units and the 1B Processor on the PUEAB, PUWB, and PURB. Two interleaved parity bits, generated over bits of the PUEAB and PUWB by the 1B Processor, are compared by the addressed peripheral unit with parity generated over the received PUWB bits and the peripheral unit wired K-code. The peripheral unit denies the ASW response to the 1B Processor when the parity check fails. This action results in a 1B Processor F-level interrupt. Parity generated by the peripheral unit over bits of the reply data (PURB) is checked by the 1B Processor. An F-level interrupt is initiated when this parity check fails.

7.06 The Peripheral Bus Fault Recovery (PBFR) program is responsible for ensuring proper continuous operation of the PUB system during hardware malfunctions. Following an F-level interrupt caused by a peripheral unit in the 4ESS Switch peripheral community, the PBFR program does the following:

- Attempts to verify that a fault exists. This includes distinguishing between transient errors and hard reproducible faults.
- Determines whether the fault is related to the PUB system or to a peripheral unit.
- Transfers fault recovery task to the appropriate peripheral unit fault recovery program for all non-PUB related faults.
- Initiates reconfiguration of PUB into a working configuration for PUB system faults.
- Requests removal from service and diagnostic tests of the faulty PUB.

7.07 The PBFR program works in conjunction with the error analysis programs ERATFMON FERA. The error analysis programs represent an additional dimension in decision making for fault detection and recovery. The programs maintain recent history information for all the unit related interrupts and attempt to derive the correct recovery action for the PBFR program.

7.08 After a faulty unit is removed from service, the appropriate diagnostic program is run by the 1B Processor. For PUB system related faults, this program is the Peripheral Unit Diagnostic Peripheral Bus (PUDPB) program. The diagnostic program resolves the fault to a small number of circuit packs.

7.09 The diagnostic programs can be requested to run automatically by fault recovery programs or manually by a TTY request. The programs can be used to diagnose faulty units, verify operation of added circuits after growth, or exercise the circuits.

7.10 Further details of software pertaining to the PUB system are provided in 234-180-260, *Diagnostic Programs*; 234-180-310, *Peripheral Units Fault Recovery Programs*; and 234-180-320, *Error Analysis Program*.

Maintenance Aids

7.11 The following units or panels are used to perform maintenance on the PUBB frame:

- Power switch (KS-20738, L4) on the control unit of each bay is used to apply power to or remove power from the associated bay.
- The states of the power switch ON pushbutton and ROS/OFF rotary pushbutton initiate configuration changes (removal from service and restoral to service).
- All +3V DC-to-DC converters contain a lamp indicator which lights to indicate power or fuse alarms.
- The +12V reference circuit pack (***FB152***) located in the first equipped PUBB&L-A unit in each bay, contains a lamp indicator which lights to indicate a reference supply alarm (fuse alarm condition).
- The telephone and TTY jack unit assembly on the control unit of bay 0 provides telephone communication between frames when performing maintenance. The assembly also provides use of the beltline channel (TTY and data set) at the PUBB frame.

7.12 Table A provides additional information on PUBB frame controls and indicators.

Routine Tasks

7.13 The procedures for performing any routine tasks at the PUBB frame are provided in the appropriate Task Oriented Practices (TOPs).

Repair and Replace Tasks

7.14 Repair and replace tasks to be performed at the PUBB frame are provided in the appropriate TOPs or covered in training.

8. References

8.01 The following list provides additional support information concerning the PUBB Frame:

Number	Title
SD-4A019-01	*Peripheral Unit Bus Branching Frame Circuit*
SD-4A038-01	*Peripheral Unit Bus Branching and Loop-Around Circuit*
SD-4A080-01	*Assignment Rules for Scanner, Distributor, and Pulse Points*

8.02 The Peripheral Unit Bus System is further discussed in the following documents.

Number	Title
234-100-000	*4ESS™ General Description*
234-180-260	*Diagnostic Programs*
234-180-310	*Peripheral Units Fault Recovery Programs*
234-180-320	*Error Analysis Program*
254-200-001	*1B Processor, General Description*

Abbreviations and Acronyms

B

BTR
Bus Terminating Resistors

F

FA Fuse Alarm

I

IOCH
Input/Output Clock High

IOCL
Input/Output Clock Low

IOU
Input/Output Units

P

PA Power Alarm

PPI Processor Peripheral Interface

PU Peripheral Units

PUB
Peripheral Unit Bus

PUBB
Peripheral Unit Bus Branching

PUCB
Peripheral Unit Control Bus

PUEAB
Peripheral Unit Enable Address Bus

PURB
Peripheral Unit Reply Bus

PURB
Peripheral Unit Write Bus

How Are We Doing?

Document Title: 4ESS™ Switch with 1B Processor Peripheral Unit Bus System Description

Document No.: 234-310-010 Issue: 1 Date: December 1998

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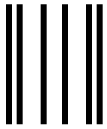

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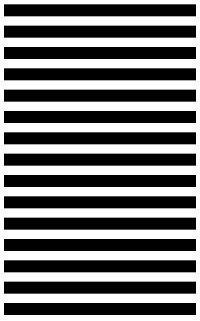

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