Lucent Technologies
Bell Labs Innovations

4ESS™ Switch
1B Processor
4E26 Generic
Maintenance Reference Handbook

Volume 1

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Issue 1
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Overview

Purpose

1.01 This handbook is intended to serve as a reference manual for experienced personnel using the ***4ESS***™ **Switch equipped with the 1B26 Processor**. The information in this issue has been prepared to the 4E26 generic program.

Scope

2.01 The data contained in this handbook is organized so that associated information is adjacent whenever possible. Access into a required set of data may be accomplished via the Table of Contents.

2.02 Teletypewriter input messages required to perform various tasks are provided. These input messages are placed in the required order to be entered to perform a task but step-by-step procedures to perform the task are not provided. Therefore, if available, the appropriate Task Oriented Practice that provides the detailed information required is referenced at the end of the messages. Teletypewriter messages of a general nature are also provided. The intent of these messages is to provide groups of messages of a particular nature that are available to the operating personnel. These messages are samples which provide the format and syntax of the message. They may require modification to suit a particular situation or location.

2.03 Teletypewriter output format precedes the word breakdown of the associated registers when that format is available. If a word breakdown is not provided, the specific word can be located in the COMPOOL. If you do not have access to COMPOOL, contact next higher support organization.

Intended Audience

3.01 The use of this book is recommended only for those familiar with the 4ESS Switch Maintenance and Operations. When in doubt, it is suggested that the appropriate handbook or Task Oriented Practices (TOP) procedure be utilized.

Reason for Reissue

4.01 Whenever this handbook is reissued, the reason(s) for reissued is listed in this paragraph.

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Audit Descriptions

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Audit Descriptions

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Audit DescriptionsAudit Descriptions

The following table contains Audit Descriptions.

Table 1-A. Audit Descriptions

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
1 CR Idle Link List	AUDSMDS2	PU32	2-Way linkage of full address Link lists occupancy counts	The head cell and the last register are passed to mutilation correction. The occupancy count is corrected by adjusting the remove-from list peg count.	H
2 CR Audit		PU9	Call register Idles audit state CRs Linkage checks for: —Link listing or CIRs —TR Linkage —DTCR Linkage —ACR Linkage	CRs in error are reported to mutilation correction.	H
3 CR/TMR Interject Level Timing Link List		PU32	Same as Audit 1	Same as Audit 1	H
4 CR/TMR Base Level Timing Link List					
5 CR Queue for MF Receivers					
6 CR Queue for MF Transmitter					
7 CR Queue for Operator Position		PU2		Same as Audit 1	M

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
8 TR Audit	AUDSMDS1	PU1	Trunk Register CCIS bit confirmed B/I status checked State code dependent data: —TR to TR linkage —Network path information —DTCR linkage Translation data (indirectly) TSN to TBMN translation	The TR in error is sent to mutilation correction.	H
9 TR Interject Level Engineered Timing List	AUDSMS1	PU6	Engineered list for TRs TR engineered list occupancy counter	TSN or TRA is out of range. Mutilation correction TR does not point to link list entry—Mutilation correction. Occupancy count errors are reported and corrected by setting the remove peg count to the add peg count minus the occupancy found by the audit. Link list Max—256 entries.	H
10 TR Base Level Engineered Timing List	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
11 TR Interject Level Timing Link List	AUDSMDS1	PU3	TR Link lists Detect broken link lists Check TR link list occupancy counters	Counters errors are corrected by setting address +2 (release count) to address +0 (add count) minus the occupancy counted by the audit. All others sent to mutilation correction.	H
12 TR Base Level Timing Link List 13 TR Trunk Maint. High & Wet Timing Link List		PU3	Same as Audit 11	Same as Audit 11	H
14 Network Path Annex Engineered List	AUDSMDS3	PU13	Network path annex B/I bits for annex slots Table to register (TR, CR) linkage	A link failure results in an error print via an audit call and the immediate idling of the entry.	M
15 TMR Audit	AUDSMDS4	PU33	TMR Register ID Link listing TR Linkage CR Linkage Timing	First the register identification item (TM4SVRID) is checked. Then, the audit state vector (TM4SVAUD): if the TMR is in the audit state (nonzero), the TMR is idled; but if any other state vector is in its audit state, the TMR is reported in error via the audit macro.	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
16 Trunk Status B/I Bits	AUDSMDS2	PU19	Trunk block B/I bits status	Both TR and TBN are passed to mutilation correction if in error. If the B/I bit should be busy, but is not, it is set to busy.	M
17 Input/output System	AUDSMDIO	—	OMR idle link list OMR translate link list OMR output link list OMR final link list Channel status channel memory block to OMR linkage OMR data timing idle OMR occupancy counter IOUC IOUS activity masks	K-register address of audit control/block exit PATTAS11 is used to report the errors with the IOUS number printed as a data word. Correction is performed before the exit is made.	L
18 TR Link List Trace to Detect Circular Link Lists	AUDSMDS1	PU2	TR link list Check for lost link list (circular lists, no head cell defined) Check for broken link lists	TRs are checked until one, with a state code indicating a link list, is detected. The last TR encountered is sent to mutilation correction in case of an error.	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
19 Maintenance Status of Trunks	AUDSMDS4	PU20	Trunk OOS list duplex failed equipment list	The mismatch error print contains the TR, disk to SL data, converted TR data, and converted to SL data. After the TR is put on the audit list, PU20 inserts code 4, TRAUD MTCE 1 into item TR4 and MTC of this TR to indicate to the audit list program that this trunk should not be idled but put in the maintenance state.	H
20 Ringing and Tone Plant (RTP)	SVCTRTAD	—	Scan point T-bits in ringing and tone plant SD Points Active RTP side determination Determine active tone appearance to dedicated TSI Memory influence by RTP	Scan point T-Bits in the RTP are initialized based upon scan point states. SD Points are initialized to normal state. A hierarchy of tones is examined to determine which side of the RTP to make active. The tone appearance, nailed up to the dedicated TSI, is made active. Memory influenced by the RTP is initialized test queues.	L
21 TMR Idle Link List	AUDSMDS2	PU32	Same as Audit 1	Same as Audit 1	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
22 MF Transmitter MF Receiver CCIS Transceiver Trunk Block Status Linkage Idle Trunks Counter	AUDSMDS2	PU18	Trunk subgroup head cell Idle trunk count Trunk block status link list	Link list errors result in rebuilding the list. Idle counts in error are corrected.	H
23 Audit List B/I Status	AUDSMCAL	PU31	Audit list Audit list B/I bits	The entry must be active and the timing flag set. If both conditions are not met, the entry is idled and an audit call made.	H
24 TR MF Origination Queue for a CR	AUDSMDS1	PU3	Same as Audit 11	Same as Audit 11	H
25 SP/DIF Dial Pulse Work List and Outpulsing Counters Audit	AUDSMDS7	PU15	Dial pulse outpulser work list	Errors are reported to mutilation detection and the counters are corrected.	H
26 Network audit	AUDSMDS3	PU10	Network map TR Path information Hardware switching memories	The error is reported via the audit macro passing the TRA.	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
27 SP/DIF Universal T-Bits	AUDSMDS7	PU14	Universal T-Bits set to ignore state Validate ignore setting Detect invalid T6 bit timing control	Any errors pass the TR to mutilation correction. T6 errors do not cause the TR to be placed on the audit list; however, this does not necessarily indicate bad call handling. The audit corrects these states. The T2T3 illegal ignore states are corrected by audit list action.	H
28 SP Miscellaneous T-Bits	AUDSMDS7	PU24	Miscellaneous T-bits to ignore state Validate ignore setting Check T6 timing control	Errors are reported via the audit macro with a print of the MSN in error. The T-bits are then corrected.	M
29 Trunk Block Status Linkage and Idle Trunks Counter	AUDSMDS2	PU18	See Audit 22	See Audit 22	H
30 Trunk Error Analysis Data Structures	TERA00	PU48		Audit message printed	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
31 Disk Administration (DKAD)	SADK		DKAD memory Outstanding disk request High and low priority disk queues AMA buffers pointers Check DMA job buffers for timeout Check CNI stream status	Audit message printed	H
32 SP/DIF SCS Polling Mask Stack Configuration Integrity Monitor Audit Request List	AUDSMDS1	PU5	SP polling mask (SP4 legal) SCS polling mask (PF4CPPUCPOL) CC stack (ability of system to perform an audit-functional test by SIMR)	Errors are reported to mutilation correction; the old mask is replaced by the new; or, the stack is reconfigured to start base level executive control.	H
33* Traffic Separations Counters	AUDSMDS4	PU28	Traffic separations counters	Message printed (do not ask for this audit manually. Length of time).	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
34 Trunk Subgroup Head Cell Information (Satellite Bit, Adjunct Linkage, MB Counters)	AUDSMDS2	PU22	Trunks subgroup head cell Link word to adjunct head cell Satellite bit Number of MB trunks Total number of MB and active trunks in TGS	Errors reported via the audits macro print the head cell, the good MB count, and the good ACTMB count. The head cell is corrected after the audit call.	H
35 Overload Timing Control	AUDSMDS2	PU25			H
36 CAMA Operator Position Occupancy Counter	AUDSMDS4	PU29	CAMA position occupancy/service counter	Audit message printed.	L
37 Miscellaneous CR Occupancy Counter Audit	AUDSMDS4	PU30	CR occupancy count	Audit message printed. System count is data words, and the Y register contains the audit count.	M
38 TR Queue for a CR (Dial Pulse In)	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
39 Files Store Paging Supervisor	PAGS4WAP		MACP client entries in page loading state	Audit message printed (page loading state checked.)	L
40 Lost Idle CRs List	AUDSMDS2	PU12	2-way link lists using full address (CRs and TMRs) Find lost CRs and TMRs	Idle link errors are reported to mutilation detection which places them in the audit state.	H
41 Quick Check of All TR Link List Head Cells	AUDSMDS1	PU4	TR link list (quick check)	Head cells and TRs are passed to mutilation correction program in case of errors.	M
42 Lost Idle TMRs	AUDSMD2	PU12	Same as Audit 40	Same as audit 40	L
43 File System-to-Core Generic	SAWSCMMN		Matching and hashing for generic only data, file system-only generic, and library program	Detects memory errors and if possible correct	L
44 Core Resident Generic Data Hash			Hashes core resident generic data		L
45 Nongeneric Core Resident and Extended Store (XS) Data Hash Check			Hashes core and extended store resident nongeneric data		L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
46 Network Management Data Structures	NMGTINIT		ATSG head cell Linkage of ATSG and TSGHC Event counters and their associated exception panel lamps	Audit message printed	M
47 Recorded Announcement (RA) System	SVCTRAUD		RA channel status RA channel call store tables	If neither the channel nor its backup can be activated, the channel is replaced by reorder.	L
48 Trunk Maintenance Structures	TMADAUDS				H
49 CCIS Link Security Structures	CCISCHI	PU21	Operational CCIS link status table Consistency with unit-type translators Validate link security terminal register (LSTR) B/I bits Check consistency between LSTRs and restrict and prohibit counters. Ensure that double prohibit A-link bands are out of service.	Terminal checks corrections are accomplished by calling the subroutine CCISINIT which must completely rebuild the data base for the input terminal number. If a double prohibit exists and none are marked OOS, an audit call is made printing the terminal and band involved.	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
50 Dedicated TSI	AUDSMDS3	PU16	Dedicated TSI nailed-up connection Idle time slot	Trunk TR is printed. A correction sequence is immediately begun to re-establish the nailed-up connection.	L
51 TR Queue for a CR Audit	AUDSMDS1	PU6			H
52*† CCIS Trunk Query	CCISAUDT		CCIS trunk status	A list of trunks with disagreeing blocking status is printed.	L
53 MAC Control Tables	MACPAUD4				L
54 TMR Job Buffer Link List	AUDMDS2	PU32	Same as Audit 1	Same as Audit 1	L
55 ITUP Origination Queue for CR(s) Audit	AUDSMDS1	PU6	Same as Audit 9		H
56 Long TR Base Level Engineered Timing List	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	M
57 TR Queue for CR (CCITT 6)	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	H
58 CR Queue for MF Receiver (Two-Stage)	AUDSMDS2	PU32	Same as Audit 1	Same as Audit 1	H
59 TR MF Origination Queue for CR (CCITT 5)	AUDSMDS1	PU3	Same as Audit 11	Same as Audit 11	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
60 ADS SADC Link Status Audit	AUDSMDS6	PU73	ANI delivery service translators	ANI delivery service translators are searched for their vendor whose SADC links are then validated.	M
61 Auxiliary CR Idle Link List	AUDSMDS2	PU32	Same as Audit 1	Same as Audit 1	H
62 ACR Audit	AUDSMDS4	PU50	ACR Idling audit state ACRs Link listing of ACRs CR Linkage TMR Linkage	ACRs in error sent to mutilation correction.	H
63 Dedicated TSI Connection Register	AUDSMDS5	PU51	Dedicated TSI connection registers TR Linkage CR Linkage TMR Linkage Timing list linkage checks	DTCRs in error are reported to mutilation correction.	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description		PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
64	CR Queue for GETS DTMF Receiver	AUDSMDS2	PU32	Same as audit 1	Same as audit 1	H
65*	TAN-to-TAN Audit	TANTOTAN	PU53	Disk plus core version of TAN-to-TAN nail-up table TR linkage	Connections found invalid are zeroed in TAN-to-TAN nail-up table and reported to mutilation correction after phases. Audit rebuilds any torn down or lost connections.	L
66	File System-to-Core Nongeneric Audit	SAWSCMMN		Matching and hashing over nongeneric data. This audit also checks file system-only data.	Detects memory errors and if possible correct	L
67	XTSI Nailup (for SPS equipped frame)	AUDSMDS3	PU7	ODA vs TSM and SPA read	Correct TSM for Nailup connection. Audit message is printed.	H
68 Thru 71	Not Assigned					
72‡	1B Memory Fault Audit	SAWSSUBR	PU21	Check accessibility and parity of all CS and PS memory	None. Fault recovery invoked if D and E level is not PESTed.	L
74‡	1B MUP Hardware/ Software Activity Audit	MCFRILEV		Check Hardware/ Software Activity status for consistency on nontroubled MUPs	Update software force bit from hardware for nontroubled MUPs.	L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
75 CR Held for PCP, GETS, CPA	AUDSMDS4	PU30	CR occupancy count	Audit message printed. System count is data words; the Y register contains the audit count.	M
76 Not Assigned					
77 TQR Audit	AUDSMDS6	PU60	B/I status of TQR, and linkage check between TQR and IR	Audit message printed and error is corrected for TQR.	H
80 Meet-me Teleconferencing Status	MMTCCNTL				L
83 Not Assigned					
84 Blue Box Fraud	BBFPCTRL				L

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
85 Large Scale Nail-Up Connection	AUDSMDS6	PU66	Large scale nail-up subtranslator table	Re-establish large scale nail-up connection correct count.	L
86 TR Origination Queue for IDTS DTMF Receiver	AUDSMDS1	PU3	Same as Audit 11	Same as Audit 11	H
87 IDTS DTMF Origination Queue for call Registers	AUDSMDS6	PU67	IDTS CR queue occupancy count	Correct count	H
88 TR Origination Queue for IWS—DTMF Receiver and CR	AUDSMDS1	PU3	Same as Audit 11	Same as Audit 11	H
89 CR Queue for DTMF	AUDSMDS2	PU32	Same as Audit 1	Same as Audit 1	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
90 ISUP Origination Queue for CRs Audit	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	H
91 Q.931 Origination Queue for CR's Audit	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	H
92 Q.931 Trunks Marked Total Signaling Failure (TSF) Audit	AUDSMDS6	PU70	Loops through all TRs associated with a D-channel or LACID looking for a trunk marked TSF	Upon a find, the audit queries the 3B RINGMON for the status of the LACID; then correct the associated TR, if necessary.	M
95* ISUP Trunk Query Audit	ISUPAUDT	ISUPAAUD	Checks all ISUP trunks in the office	Can correct an error condition with more specific action.	L
96 Quick ISUP Trunk Query Audit	ISUPAUDT	ISUPAAUD	Checks one TSN per TSG	Can correct an error condition with more specific action.	L
97 Noncall-Associated Trunks (NCAT) Register Idle Count	AUDSMDS6	PU75	Checks the number of NCAT register(s) that are in use	Can correct an error condition with more specific action.	H

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
98 NCAT Trapping Structure	AUDSMDS6	PU76	Checks the new data structures used by NCAT anomaly trapping including the trap head cells and raw data blocks used to store trap information	Can correct an error condition with more specific action.	H
99 INUP Origination Queue for CR(s) Audit	AUDSMDS1	PU6	Same as Audit 9	Same as Audit 9	H
100 CR queue for DTMF Receiver	AUDSMDS2	PU32	Same as Audit 1	Same as Audit 1	H
101 RTNR Transport Capabilities (TC) Idle Channel Count	AUDSMDS2	PU80	Counts idle channel of each TC for each NSN and compares count with that which is stored in idle channel count of TC structure	Can correct an error condition with more specific action.	H
102 RTNR Routing Pattern Index (RPI) Calls in Progress Count	AUDSMDS2	PU81	Validates the routing pattern index calls in progress count	Can correct an error condition with more specific action.	H
103 ECOS Idle Channel Count Audit	AUDSMDS2	PU82	Validates the ECOS TC idle channel count	Calls subroutine to get the sum of idle counts for the TCs for all TSGs in an area TSG list.	

See Notes, Footnotes and Legend at end of table.

Table 1-A. Audit Descriptions (Contd)

Audit Number and Description	PIDENT	Program Unit (PU)	Memory Checked	Action Taken (By Audit)	Inhibit Risk (Note)
103 ECOS Idle Channel Count Audit (Contd)				Then these counts are used to validate the counts that are stored in XL4ECOSTCA. Any incorrect counts are reported by audit and corrected	H
104 ECOS Calls-in-Progess Counts Audit	AUDSMDS2	PU83	Validates the ECOS calls in progress count for each ERPI-area	Calls subroutine to collect and compare the accumulated occurences of each ERPI-area index in the ECOS trunk data table with the call processing counts. The ECOS trunk data number is stored in a call processing interface word so that call processing can update the audit CIP if it operates on a trunk that the audit already counted. Any incorrect counts are reported by audit and corrected	H

Note: High (H), Medium (M), or Low (L) indicate the risk to basic call processing if the audit is inhibited and other problems exist. If "open defensive check" audit printouts are occuring or other numbered audits and TRs or CRs are in the output message, then any number of the High Risk Audits may be needed to achieve sanity.

* Audit cannot be demanded. Input message is not accepted.
† This audit is used by NESAC to test if audits are printing.
‡ This audit is 4E19 generic and later.

Table 1-A. Audit Descriptions (Contd)

Legend:

ACR	Auxiliary Call Register	MF	Multifrequency
ACTMB	Active Maintenance Bus	MUP	Maintenance and Utility Processor
ANI	Automatic Number Identification	NCAT	Noncall-Associated Trunk
ATSG	Adjunct Trunk Subgroup	NESAC	National Electronic Systems Assistance Center
B/I	Busy/Idle	NSN	Network Switching Number
CAMA	Central Automatic Message Accounting	ODA	Office Data Assembler
CC	Central Control	OMR	Output Message Record
CCIS	Common Channel Interoffice Signaling	OOS	Out-Of-Service
CCITT	International Telegraph and Telephone Consultative Committee	PCP	Positive Call Process
		PEST	Prevent Error Source Transmission
CIP	Call in Progress	PS	Program Store
CNI	Common Network Interface	PU	Program Unit
CPA	Common Platform Adjunct	RA	Recorded Announcement
CR	Call Register	RINGMON	Ring Monitor Kernel Process
CS	Call Store	RPI	Routing Pattern Index
DIF	Digital Interface Frame	RTNR	Real Time Network Routing
DKAD	Disk Administration	RTP	Ringing and Tone Plant
DTCR	Dedicated TSI Connection Register	SCS	Service Circuit System
DTMF	Dual Tone Multifrequency	SD	Signal Distributor
ECOS	End to End Class of Service	SIMR	System Integrity Monitior Register
GETS	Government Emergency Telecommunication Service	SP	Signal Processor
IDTS	Immediate Dial Tone Start	TAN	Trunk Appearance Number
INUP	International Integrated Services Digital Network User Part	TBMN	Trunk Block and Member Number
		TBN	Trunk Block Number
IOUC	I/O Unit Controller	TC	Transport Capabilities
IOUS	I/O Unit Selector	TMR	Trunk Maintenance Register
ISUP	Integrated Services Digital Network User Part	TR	Trunk Register
		TRA	Terminal Resource Allocator
ITUP	International Telephone User Part	TSF	Total Signaling Failure
LACID	Link Access Identification	TSG	Trunk Subgroup
LSTR	Link Security Terminal Register	TSGHC	Trunk Subgroup Head Cell
MACP	Maintenance Administration Control Program	TSI	Time Slot Interchange
		TSN	Trunk Scanner Number
MB	Maintenance Busy		

Conditional All Test Pass (CATP) Layouts

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Contents

Contents

Conditional All Test Pass (CATP) Layouts

2

API—Attached Processor Interface

Reason for Tests Skipped:

Bit 5 = Kill request message (MSG) to 3B Computer not accepted
7 = Command sent to the API was not acknowledged
8 = Diagnostic (DGN) request MSG to 3B Computer not accepted
9 = APDMI process at 3B Computer not started
10 = DGN request MSG to 3B Computer timed out
11 = Diagnostics inhibited at 3B Computer
12 = Second start dial (SSD) out-of-service
33 = GCP reply was all zeros
43 = Power monitor (PWRMON) test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

AUB—Auxiliary Bus

Reason for Tests Skipped:

Bit 13 = Auxiliary Unit (AU) helper out-of-service

20 = Unit not in normal or ROS state

22 = AU unit KCode trouble bit set

23 = AU unit "do not restore" bit set

AUI—Auxiliary Unit Interface

Reason for Tests Skipped:

Bit 6 = AUB 0 out-of-service

7 = AUB 1 out-of-service

12 = SSD out-of-service

13 = API 0 or data unit selector (DUS) 0 are not available to use as helper

14 = API 1 or DUS 1 are not available to use as helper

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs already active — try again

45 = Work table full — try again

46 = Frame request active — try again

47 = Unit not in normal state

CC—Central Control

Reason for Tests Skipped:

Bit 0 = Call store bus (CSB) 0 out-of-service
1 = CSB 1 out-of-service
2 = Duplex Master Control Complex utility processor (MUP) failure
3 = Program store bus (PSB) 0 out-of-service
4 = PSB 1 out-of-service
6 = AUI 0 helper out-of-service
7 = AUI 1 helper out-of-service
8 = Direct memory access (DMA) failure on active MUP
12 = SSD out-of-service
13 = SSD 0 helper out-of-service
14 = SSD 1 helper out-of-service
16 = Interface Bus (IFB) 0 helper out-of-service
17 = IFB 1 helper out-of-service
18 = MUP 0 helper out-of-service
19 = MUP 1 helper out-of-service
20 = CC forces in effect
22 = MUP forces in effect
23 = Disable AUTO PC in effect
24 = MUP executed code reports CATP
25 = Reserved for utility system DGN
26 = Call store helper unit not available
27 = Program store helper unit not available
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

CS—Call Store

Reason for Tests Skipped:

Bit 0 = CSB 0 out-of-service
1 = CSB 1 out-of-service
12 = SSD out-of-service
15 = Standby CC out-of-service
21 = MCC override in effect (ON)
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

CSB—Call Store Bus

Reason for Tests Skipped:

Bit 12 = SSD out-of-service
15 = Standby CC out-of-service
23 = Disable auto processor configuration (PC) in effect
36 = Call store helper unit not available
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

DIF/DIFE1—Digital Interface Frame/-Export 1

Reasons for Tests Skipped:

Bit 0 = Peripheral Unit Bus (PUB) 0 or IPUB 0 out-of-service

1 = PUB 1 or IPUB 1 out-of-service

2 = Base signal processor (SP) frame out-of-service

3 = Duplicated sp frame out-of-service

4 = Mate out-of-service

5 = Power switch in ROS state

6 = CC 0 out-of-service

7 = CC 1 out-of-service

8 = Another frame responding to CI

9 = Another frame responding to this frames member interrogate (MI)

10 = Another frame responding to this frames GI

11 = Peripheral Unit Bus (PUB) not duplex

12 = Another frame responding to autonomous peripheral unit failure (APUF) CI

13 = Another frame responding to autonomous peripheral unit trouble (APUT) CI

14 = Controller not duplex

15 = Another frame responding to autonomous peripheral unit base (APUB) CI

DIF/DIFE1—Digital Interface Frame/-Export 1 (Contd)

Bit 16 = Protection switch has taken place

17 = Another frame responding to high priority polling

18 = Another frame responding to low priority polling

19 = Another frame responding to digit buffer polling

20 = Another frame responding to seizure buffer polling

21 = PSW TTY keyboard for requesting PSW tests is not specified

22 = Controller 0 out-of-service

23 = Controller 1 out-of-service

24 = Signal processor (SP) frame duplex failed

25 = SP frame configuration failed

26 = Bus at unit (IPUB) out-of-service

41 = Network clock (NCLK) 0 out-of-service

42 = NCLK 1 out-of-service

43 = No spare digital interface units (DIU) (DIFE1 only)

44 = No available DIU

45 = Frame member number greater than 23; buffer polling tests not run

46 = Memory TTY keyboard for optional memory phases not specified (DIFE1 only)

47 = Select TTY keyword for requesting DIU bus selection tests is not specified

DT—Digroup Terminal

Reasons for Tests Skipped:

Bit 36 = SP-2 Simplex or some in-service DT in this community has DT controller out-of-service

37 = Some time slot interchange (TSI) controller is out-of-service

38 = Some DTU on this DT is on a protection switch

DUS—Data Unit Selector

Reason for Tests Skipped:

Bit 12 = SSD out-of-service

25 = Both DUS's not INS or can not configure all INS tape unit controller (TUC) to same DUS

26 = No TUC helper available

29 = Incorrect or no tape mounted

30 = Some TUC in SR mode

31 = TUC out-of-service (OOS) select verify test skipped

37 = TUC not assigned DGN function or TUC equipped with ADT

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs already active — try again

45 = Work table full — try again

46 = Frame request active — try again

47 = Unit not in normal state

EST—Echo Suppressor Terminal

Reasons for Tests Skipped:

Bit 0 = PUB 0 or IPUB 0 out-of-service
1 = PUB 1 or IPUB 1 out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
6 = CC 0 out-of-service
7 = CC 1 out-of-service
8 = CI has other units responding
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = Autonomous peripheral unit failure (APUF) CATP flag
13 = APUT CATP flag
14 = Simplex mode
15 = User saved by EUFR not zero
16 = PSW occurred
17 = TSI out-of-service
24 = SP scan/distribute point out-of-service
25 = SP bus out-of-service
26 = Bus at unit (IPUB) out-of-service

IFB—Interface Buffer

Reason for Tests Skipped:

Bit 12 = SSD out-of-service
15 = Standby CC out-of-service
24 = MUP helper client not responding
29 = AUI helper client not responding
35 = SSD helper client not responding
42 = TIC helper client not responding
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

I/O—Input/Output

Reason for Tests Skipped:

Bit 9 = PUB 0 out-of-service
10 = PUB 1 out-of-service
12 = SSD out-of-service
35 = Requires both PUBS in service
41 = Helper PUB not out-of-service
42 = Can not CONFIG all INS IOUS to same PUB
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

IOP—Input/Output Processor

Reason for Tests Skipped:

Bit 5 = Invalid peripheral controller circuit pack
7 = IOP TN82 PC port equipage is not right
9 = PUB 0 out-of-service
10 = PUB 1 out-of-service
11 = ASWEPU bit set
12 = SSD out-of-service
13 = CPD CNTL pulse order caused F-SRC
41 = Helper PUB not out-of-service
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

IOUS—Input/Output Unit Selector

Reasons for Tests Skipped:

Bit 5 = Invalid peripheral controller circuit pack

7 = TN82 PC Port equipage is incorrect; on-board DGN not run

9 = PUB 0 out-of-service

10 = PUB 1 out-of-service

11 = Peripheral unit all-seems-well error summary (ASWEPU) inhibit set

12 = SSD out-of-service

13 = CPD CNTL pulse order caused F-SRC (expanded IOP)

33 = Both IOUC helpers not out-of-service

34 = An IOUC port is in trouble

35 = Requires duplex PUBS

41 = Helper PUB not out-of-service

42 = Cannot configure all in-service IOUSs to same PUB

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs active — try again

45 = PWRMON work table full — try again

46 = Frame request for PWRMON active

47 = Unit not in normal state

MUP—Master Control Complex and Utility Processor

Reason for Tests Skipped:

Bit 6 = AUI 0 helper out-of-service
7 = AUI 1 helper out-of-service
8 = DMA failure on active MUP
12 = SSD out-of-service
13 = SSD 0 helper out-of-service
14 = SSD 1 helper out-of-service
22 = MUP forces in effect
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

NCLK—Network Clock

Reasons for Tests Skipped:

Bit 0 = PUB 0 out-of-service
1 = PUB 1 out-of-service
2 = Primary SP pulse points out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
6 = CC 0 out-of-service
7 = CC 1 out-of-service
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = Chain 0 out-of-service — tests skipped
13 = Chain 1 out-of-service — tests skipped
14 = Chain 2 out-of-service — tests skipped
15 = Chain 3 out-of-service — tests skipped
16 = Chain 3 tests skipped, bad OSC
17 = Chain 2, 3 tests skipped, bad OSC
18 = Chain 1, 2, 3 tests skipped, bad OSC
19 = OSC 0 out-of-service — tests skipped
20 = OSC 1 out-of-service — tests skipped
21 = OSC 2 out-of-service — tests skipped
22 = OSC 3 out-of-service — tests skipped
24 = SP Scan/distribute points out-of-service
25 = SP bus out-of-service

PS—Program Store

Reason for Tests Skipped:

Bit 3 = PSB 0 out-of-service
4 = PSB 1 out-of-service
12 = SSD out-of-service
15 = Standby CC out-of-service
21 = MCC override in effect (ON)
43 = PWRMON test timed out — try again
44 = Two PWRMON jobs already active — try again
45 = Work table full — try again
46 = Frame request active — try again
47 = Unit not in normal state

PSB—Program Store Bus

Reason for Tests Skipped:

Bit 12 = SSD out-of-service

15 = Standby CC out-of-service

23 = Disable auto peripheral controller (PC) in effect

36 = Store helper unit not available

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs already active — try again

45 = Work table full — try again

46 = Frame request active — try again

47 = Unit not in normal state

PUB—Peripheral Unit Bus

Reason for Tests Skipped:

Bit 0 = PUB 0 out-of-service

1 = PUB 1 out-of-service

2 = Primary SP pulse points out-of-service

3 = Secondary SP pulse points out-of-service

4 = Mate unit out-of-service

5 = Power control switch in ROS position

6 = CC 0 out-of-service

7 = CC 1 out-of-service

12 = Helper controller 0 out-of-service

13 = Helper controller 1 out-of-service

24 = SP scan/distribute points out-of-service

25 = SP bus out-of-service

26 = Bus at unit (IPUB) out-of-service

SCLK—System Clock

Reason for Tests Skipped:

Bit 0 = PUB 0 or IPUB0 out-of-service

1 = PUB 1 or IPUB1 out-of-service

2 = Primary SP pulse points out-of-service

3 = Secondary SP pulse points out-of-service

4 = Mate unit out-of-service

5 = Power control switch in ROS position

6 = CC 0 out-of-service

7 = CC 1 out-of-service

11 = PUB not duplex

12 = Network Clock Sync Unit (NCSU) out-of-service (if diagnosing SYNC unit or IPUB)

12 = System clock controller 0 out-of-service (if diagnosing controller)

13 = System clock controller 1 out-of-service

14 = NCLK chain 0 out-of-service

SCLK—System Clock (Contd)

Bit 15 = NCLK chain 1 out-of-service
16 = NCLK chain 2 out-of-service
17 = NCLK chain 3 out-of-service
18 = NCLK mate/chain 0-1 out-of-service
19 = NCLK mate/chain 2-3 out-of-service
20 = DS1A T1 unequipped
21 = DS1B T1 unequipped
22 = BSRF unequipped
24 = SP scan/distribute points out-of-service
25 = SP bus out-of-service
26 = Bus at unit (IPUB) out-of-service
28 = Controller firmware in update mode
29 = BSRF reference not in use
30 = DS1A reference not in use
31 = DS1B reference not in use

SCS—Service Circuit System

Reason for Tests Skipped:

Bit 0 = PUB 0 or IPUB 0 out-of-service
1 = PUB 1 or IPUB 1 out-of-service
2 = Primary SP pulse points out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
6 = Power monitor tests skipped on manual ROS test
7 = CC 0 out-of-service
8 = CC 1 out-of-service
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = APUF CATP flag
13 = APUT CATP flag
15 = APUB CATP flag

If subunit type is bus:

Bit 12 = Helper controller 0 out-of-service
13 = Helper controller 1 out-of-service

SCS—Service Circuit System (Contd)

Bit 16 = Hard disk unit not equipped

17 = Some other frame responding to PHP polling

18 = Some other frame responding to PLP polling

19 = Some other frame responding to PDG polling

20 = Some other frame responding to PSZ polling

21 = Unused EBI link tests skipped—Unequipped SCU ports on KCN3 circuit pack have been skipped. Restore equipment using the normal procedure.*

22 = Controller 0 out-of-service

23 = Controller 1 out-of-service

24 = SP scan/distribute points out-of-service

25 = SP bus out-of-service

26 = Bus at unit (IPUB) out-of-service

30 = SCU powered down

---

* Diagnostics on the SCS Controller test all ports on the KCN3 circuit pack. Some of these ports may not be equipped with a SCU. A diagnostic failure indicates that one or more ports on the KNC3 have failed or a looping plug on the optical cross connect panel has failed. If this occurs, the controller may be restored to service using a normal procedure. The KCN3 or looping plug(s) should be replaced at the earliest possible convenience.

SP—Signal Processor

Reason for Tests Skipped:

Bit 0 = PUB 0 or IPUB 0 out-of-service
1 = PUB 1 or IPUB 1 out-of-service
2 = Primary SP pulse points out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
6 = CC 0 out-of-service
7 = CC 1 out-of-service
8 = CI has other units responding
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = Low buffer poll has other units responding
13 = Digit buffer poll has other units responding
14 = High buffer poll has other units responding

If subunit type is bus:

Bit 12 = Helper controller 0 out-of-service
13 = Helper controller 1 out-of-service

SP—Signal Processor (Contd)

Bit 15 = Seizure buffer poll has other units responding

16 = GI, CI, MI has other units responding on bus 0

17 = GI, CI, MI has other units responding on bus 1

18 = SP bus circuit out-of-service

19 = DT out-of-service

20 = DT absolute alarms

21 = Patch overwrites in system

24 = SP scan/distribute points out-of-service

25 = SP bus out-of-service

26 = Bus at unit (IPUB) out-of-service

27 = DTs (on SP) failed "Ignore" routine (DTFRSGAL)

28 = Firmware activity bit = 0 (Inactive)

SSD—Scan and Signal Distributor

Reason for Tests Skipped:

Bit 12 = SSD out-of-service

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs already active — try again

45 = Work table full — try again

46 = Frame request active — try again

47 = Unit not in normal state

TGR—Terminal Grouping Frame

Reason for Tests Skipped:

Bit 0 = PUB 0 or IPUB 0 out-of-service

1 = PUB 1 or IPUB 1 out-of-service

2 = Primary SP pulse points out-of-service

3 = Secondary SP pulse points out-of-service

4 = Mate unit out-of-service

5 = Power control switch in ROS position

8 = CI has other units responding

9 = MI has other units responding

10 = GI has other units responding

11 = PUB not duplex

12 = TGR A, controller 0 out-of-service

13 = TGR A, controller 1 out-of-service

24 = SP scan/distribute points out-of-service

25 = SP bus out-of-service

TGR—Terminal Grouping Frame (Contd)

Bit 26 = Bus at unit (IPUB) out-of-service
27 = Terminal 00 out-of-service
28 = Terminal 01 out-of-service
29 = Terminal 02 out-of-service
30 = Terminal 03 out-of-service
31 = Terminal 04 out-of-service
32 = Terminal 05 out-of-service
33 = Terminal 06 out-of-service
34 = Terminal 07 out-of-service
35 = Terminal 08 out-of-service
36 = Terminal 09 out-of-service
37 = Terminal 10 out-of-service
38 = Terminal 11 out-of-service
39 = Terminal 12 out-of-service
40 = Terminal 13 out-of-service
41 = Terminal 14 out-of-service
42 = Terminal 15 out-of-service
43 = TGR group in growth

TMSP—Time-Multiplex Switch Port

Reason for Tests Skipped:

Bit 0 = PUB 0 or IPUB 0 out-of-service
1 = PUB 1 or IPUB 1 out-of-service
2 = Primary SP pulse points out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
8 = CI has other units responding
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = Some time slot interchanges (TSI) are out-of-service
13 = Duplex failure in TMSP—repair other controller first
14 = Mate and unit cannot be configured on same bus
15 = Controller must be in special growth
16 = Cannot place TSI's on out-of-service bus
17 = Bus 0 power control switch in ROS position
18 = Bus 1 power control switch in ROS position
24 = SP scan/distribute points out-of-service
25 = SP bus out-of-service
26 = Bus at unit (IPUB) out-of-service
36-41 = Count of TSIs used—given that some TSIs were out-of-service

TSI—Time-Slot Interchange

Reason for Tests Skipped:

Bit 0 = PUB 0 or IPUB 0 out-of-service

1 = PUB 1 or IPUB 1 out-of-service

2 = Primary SP pulse points out-of-service

3 = Secondary SP pulse points out-of-service

4 = Mate unit out-of-service

5 = Power control switch in ROS position

8 = CI has other units responding

9 = MI has other units responding

10 = GI has other units responding

11 = PUB not duplex

12 = TMSP out-of-service

13 = One or more parts on voiceband interface frame or digroup terminal unit (VIF/DTU) out-of-service

14 = Network blockage encountered

15 = Time slot interchange frame (TSIF) in growth

16 = Echo suppressor unit (ESU) out-of-service

24 = SP scan/distribute points out-of-service

25 = SP bus out-of-service

26 = Bus at unit (IPUB) out-of-service

TUC—Tape Unit Controller

Reason for Tests Skipped:

Bit 12 = SSD out-of-service

24 = DUS helper out-of-service

25 = Both DUSs not INS or can't config all INS TUCs to same DUS

27 = Series 20-40 TUC phases not run

28 = Series 30-50 TUC phases not run

29 = Incorrect or no tape mounted

30 = Some TUC in software reinitialization (SR) mode

32 = No auto tape motion tests run (tape not at valid write point)

37 = TUC not assigned DGN function or TUC equipped with ADT

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs already active — try again

45 = Work table full — try again

46 = Frame request active — try again

47 = Unit not in normal state

VIF—Voiceband Interface Frame

Reason for Tests Skipped:

Bit 0 = PUB 0 out-of-service
1 = PUB 1 out-of-service
2 = Primary SP pulse points out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
8 = CI has other units responding
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = No SM flywheel tests
13 = PSW tests skipped
14 = Simplex mode
15 = Voiceband interface unit (VIU) unavailable
16 = VIU 7 unavailable
17 = APUF—CI has other units responding
18 = APUT—CI has other units responding
24 = SP scan/distribute points out-of-service
40 = Phase 1 fails test
41 = Greater than 9 test fail

XPWR—Miscellaneous Power

Reason for Tests Skipped:

Bit 12 = SSD out-of-service

43 = PWRMON test timed out — try again

44 = Two PWRMON jobs already active — try again

45 = Work table full — try again

46 = Frame request active — try again

47 = Unit not in normal state

XTSI—Expanded Time-Slot Interchange

Reason for Tests Skipped:

Bit 0 = PUB 0 out-of-service
1 = PUB 1 out-of-service
2 = Primary SP pulse points out-of-service
3 = Secondary SP pulse points out-of-service
4 = Mate unit out-of-service
5 = Power control switch in ROS position
6 = CC 0 out-of-service
7 = CC 1 out-of-service
8 = Power monitor tests skipped on manual ROS test
9 = MI has other units responding
10 = GI has other units responding
11 = PUB not duplex
12 = APUF CATP flag
13 = APUT CATP flag
14 = Network blockage encountered
15 = TSI frame is in growth
17 = Some other frame responding to PHP polling
18 = Some other frame responding to PLP polling
19 = Some other frame responding to PDG polling
20 = Some other frame responding to PSZ polling
22 = Controller 0 out-of-service
23 = Controller 1 out-of-service
24 = SP scan/distribute point out-of-service
25 = SP bus out-of-service
26 = Some PSC is protection switched
27 = Controller not duplex
28 = One or both controller power feeds is not available

XTSI—Expanded Time-Slot Interchange (Contd)

Bit 30 = Some PSC port is PESTed
31 = Network clock 0 out-of-service
32 = Network clock 1 out-of-service
33 = TMS is out-of-service
34 = ALC powered down
35 = Controller 0 powered down
36 = Controller 1 powered down
37 = Some PSC power control switch is in ROS position
38 = Some PSC port is not running operational load
39 = D3U is not in growth or special growth
40 = D3U not protection switched
41 = IBU is out-of-service
42 = IBU power control switch is in ROS position
43 = IBU is not running operational load
44 = IBU port is PESTed

Master Control Console Terminal

3

Contents

Contents

Master Control Console Terminal

3

Video Display Pages

The functional areas of the MCC is presented as pages on a video display terminal. Pages are selected by entering a numeric command corresponding to the page number. These pages and a brief description of each are as follows:

Table 3-A. Video Display Pages

Number	Name	Description
	Emergency Action Interface	The Emergency Action Interface (EAI) page is selected by pushing the key labeled **EA DISP**. This key provides access to critical controls and functions needed to perform recovery actions. The EAI page is the default page displayed whenever communication is initialized to the MCC terminal.
100	Page Index	The Index page is selected by entering 100. This page lists all other pages and identifies the page selection number of each.

Table 3-A. Video Display Pages (Contd)

Number	Name	Description
101-105	Reserved	
106	MUP Status and Control	The MUP Status and Control page is selected by entering 106. This page provides specific MUP control and status information.
107	Reserved	
108	System Status	The System Status page provides overall switching status, alarm information and hardware equipment status for the *4ESS*™ Switch. The System Status page is selected by entering poke command **108**.
109	Program Store Status and Control	The Program Store Status and Control page provides 1B Processor program store information such as the current program store configuration and program store M-code configuration in addition to program store bus status. The Program Store Status and Control page is selected by entering poke command **109**.
110	Call Store Status and Control	The Call Store Status and Control page provides 1B Processor call store information such as the current call store configuration and call store M-code configuration in addition to call store bus status. The Call Store Status and Control page is selected by entering poke command **110**.

Table 3-A. Video Display Pages (Contd)

Number	Name	Description
111	Client Status and Control	The Client Status and Control page is selected by entering 111. This page provides the status for all IFB clients in addition to bus and client control. The Client Status area contains indicators identifying the status of each IFB Client in addition to maintenance bits.
112-117	Reserved	
118	1B Processor Status	The Processor Status page is selected by entering 118. This page provides information about the processor configuration, including active central control (CC), active program store bus (PSB), active call store bus (CSB), active interface bus (IFB), and active auxiliary unit bus (AUB), and M-Code configurations for all stores. This page toggles between a normal display and a detailed display be entering 499.
119	DDI Key Options	The Direct Data Insert (DDI) Key Options page is selected by entering 119. This page toggles between Modified Recovery Actions DDI key assignments and Inhibit Interrupts DDI key assignments by entering 499. A brief explanation of Modified Recovery Actions or Inhibit Interrupts DDI key assignments is provided on their respective page.

Table 3-A. Video Display Pages (Contd)

Number	Name	Description
120	Data Display	The Data Display page is selected by entering 120. This page provides memory displays, data insert keys, and utility functions.
1990	Dead Start	The Dead Start page is selected by entering 1990. The Dead Start page requires special maintenance capabilities. Page 1990 is designed to restore the 1B hardware into a sane environment if automatic and manual efforts to restore the 1B via the EAI page have not been successful.

Video Display Colors

Different colors are used in the displays to distinguish between problems and normal conditions. The entities in a display referred to as "Indicators" also use different colors to convey information. Indicators are displayed in a foreground and background color. The *foreground* is defined as the colored letters or numbers that make up the indicator while the *background* is defined as the color that surrounds the indicator. In general, background colors have the meanings listed in Table 3-B. Foreground colors are selected for readability and to further subdivide the associated background color into specific functions. Table 3-B lists and describes the different foreground and background colors:

Table 3-B. Video Display Colors

Background	Foreground	Meaning
Black		A black background identifies normal information or text.
	White	Information - Normal Conditions
	Yellow	Instruction - Normal Conditions
White		A white background identifies a selected state.
	Black	Selected for non-force indicators
	Purple	Selected for force indicators

Table 3-B. Video Display Colors (Contd)

Background	Foreground	Meaning
Purple		A purple background identifies an option that has been forced in hardware registers.
	Black	Force has been activated in hardware
	Light Blue	Forced but hardware error present
Yellow		A yellow background identifies a minor problem.
	Black	Minor problem - status verified
	Red	Minor problem - No status is available
Red		A red background identifies a major or critical problem. It is also used for an Out-of-Service (OOS) state.
	White	Major problem
	White (Flashing)	Critical problem
	Black	Unit is OOS
	Yellow	Forced but hardware error present
	Light Blue	Forced but hardware error present

Table 3-B. Video Display Colors (Contd)

Background	Foreground	Meaning
Green		A green background identifies an active unit or system normal condition.
	Black	Active unit or status normal
Blue		A blue background identifies a standby unit.
	White	Standby unit status
Light Blue		A light blue background is for other off-normal unalarmed conditions.
	Black	Situation specific meaning

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```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □ PORT □  PAGE 100     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG     MCC         SYS NORM
   CC          PS        CS     IF/AU        PU        MISC      MCC DPFL
CMD:

                   -4ESS MASTER CONTROL COMPLEX PAGE INDEX-

                       EA DISP - EMERGENCY ACTION DISPLAY
                           100 - PAGE INDEX
                           106 - MUP STATUS AND CONTROL
                           108 - SYSTEM STATUS
                           109 - PROGRAM STORE STATUS AND CONTROL
                           110 - CALL STORE STATUS AND CONTROL
                           111 - IFB CLIENTS STATUS AND CONTROL
                           118 - 1B PROCESSOR STATUS
                           119 - DDI KEY OPTIONS
                           120 - DATA DISPLAY
                          1990 - DEAD START


                                                                   =DGN IN PROG=
```

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EA DISP—Emergency Action Interface

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP   PORT    PAGE EAI       mm/dd/yy      hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG      MCC          SYS NORM
   CC          PS        CS     IF/AU        PU       MISC        MCC DPFL
CMD:
99 - CLEAR ALL REQUESTS       100 - PAGE INDEX
-FORCE FNCT-  | - MANUAL PROG REQ- | -PC SEQUENCER-      -REPEATED PC- -PC ATTEMPT-
01 - HARD A   | 02 - SOFT A        | 03,xx - SET PC STATE:
10 - CC 0     | 51 - PHASE 1       | 04    - INCREMENT PC          -PC PROGRESSION-
11 - CC 1     | 52 - PHASE 2       | 70    - DIS AUTO PC         CC CS IF AU PS CMPL
20 - PS 0     | 53 - PHASE 3       |
21 - PS 1     | 54 - PHASE 4       |             -DIRECT DATA INSERT-
22 - PSB 0    | 81 - CLEAR UTIL    | 401/400,xx - SET/RESET xx; 402 - RESET ALL
23 - PSB 1    | 82 - RESTORE I/O   | CONTENTS:
30 - CSB 0    | 83 - INHIBIT INT   |           -EAI FAIL DATA DISPLAY-
31 - CSB 1    | 84 - MODIFY RECV   | 86 - CODE: B'
40 - IFB 0    |                    | 87 - DATA: B'
41 - IFB 1    | -FILE SELECT-      | 88 - ADDR: B'
42 - AUB 0    | 61 - NORM FILE     | 89 - CLEAR DISPLAY
43 - AUB 1    | 62 - UPD FILE      | -INTF HW ENABLED-        | -ERRORS ON SR-
              |                    |                          | -INVALID SELECTION-
-EMER CFG-    | -SYSTEM REINIT-    |                          | -OVERRIDE IN EFFECT-
48 - FULL     | 63 -               |                          | -UPDATE IN PROG-
49 - MIN      | 64 - UTILITY SR    |                          | -PHASE IN PROG-
```

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Phase Progress Display

The progress of Phase 1, Phase 2, Phase 3, or Phase 4 is displayed on the EAI page **DIRECT DATA INSERT** section. While the phases are running, the **PHASE IN PROG** indicator is illuminated, and the following data is displayed on the **CONTENTS** indicator of the **DIRECT DATA INSERT** section:

31 24	23	22 15	14 9	8 0

Bit 0-8 = UTYPE being booted for SICO task 3, 4, 5, or 6

or

Phase module for SICO task (decimal) 8, 9, 10, or 11 decimal values

0 = Idle unprotected generic call store (SISCR)

1 = Zero select areas of disk (SIZDSK)

2 = Stops all SP and initializes SP buffers (SISTC)

3 = Initializes network busy idle maps and initializes CCIS terminals (SIMAP)

4 = Sets bits in all trunk registers for saving calls (SITRC)

5 = Idle TSG headcells, busy TB B-I bits, idle CAMA blocks (SITBN)

6 = Idles MSN(s) and MDN(s) (SIMSN)

7 = Read network controller memories to save calls (SIRNC)

8 = Search for network paths (SISSC)

9 = Write network controller memories after saving calls (SIWNC)

Phase Progress Display (Contd)

10 = Idle non-stable trunk registers (SIITR)

11 = Phase 2 (SIPHSE2)

12 = Correct TSI B-I memory maps (SIBIM)

13 = Duplex failure module (SIDPXF)

14 = Set up nailed-up connections (SINUC)

15 = Idle and relink pooled ODA structures (SILNK)

16 = Phase 1 (SIPHS1)

17 = Update trunk registers from out of service list (SITOSL)

18 = Verifies the state of all saved broadband calls (SIBBC)

19 = Verifies connections through the ATP node (SIATP)

20 = Return to SICO (SIRET)

21 = Error processing (SIERR)

NOTE:
Not all modules are executed on all phases.

Phase Progress Display (Contd)

Bit 9-14 = SICO task - values of K

K = 0 - PCRV to be called by SICO

K = 1 or 2 - Type I or type II RC rollback

K = 3, 4, 5, or 6 - Peripheral recovery level 1, 2, 3, or 4

K = 7 - Dynamic overload controls applied

K = (decimal) 8, 9, 10, or 11 - SINT phase 1, 2, 3, or 4

Bit 15-22 = Phase trigger - (decimal)

0-6 = Interject program(s) not being entered

17 = Interject protection flag failure

18 = Base cycle too long

19 = Software clock inconsistent

20 = Excessive K-level interrupts

21-22 = Multiple SIMR triggers

23 = Base cycle above overload threshold

24 = SICO error count exceeded threshold

25 = Excessive total interrupts

26 = Excessive pulse source B-levels

27 = Excessive C-levels

28 = Excessive stack counter D-levels

29 = Excessive protected area D-levels

Phase Progress Display (Contd)

Bit 15-22 = Phase trigger - [decimal (Contd)]

30 = Excessive control unit failures (D-levels)

31 = Excessive CS failure (D-levels)

32 = Excessive ORD levels (D-levels)

33 = Excessive PS failures (E-levels)

34 = Excessive PUFs (F-levels)

35 = Excessive APUFs (F-levels)

36 = Excessive error stops

37 = Duplex failure removal or zero start

38 = Total out-of-range interrupts for B-, D-, E-, and F-levels

39 = SIC error leg in phase control routine was activated (SICOPRE)

40 = SIMB re-entry check on SICO failed

41 = B-level interrupt

42-60 = Base entry failures

74-80 = Long-term interject program entry failures

90 = Long-term interject clock failure

91 = Base cycle too short

92 = Adjacent base cycle difference too large

93 = Base cycle time not equal to number or interjects

94 = Inconsistent base cycle time

Phase Progress Display (Contd)

Bit 15-22 = Phase trigger - [decimal (Contd)]

95 = TTY functional check failure

96 = Request I/O mask audit

97 = Disk statistical check failed

98 = Invalid or excessive out-of-range disk requests

99 = Disk read/write failure

103 = Minimum base cycle long-term failure

104 = Base cycle—base cycle long-term failure

105 = Base cycle—interject long-term failure

106 = Inconsistent base cycle time long-term failures

107 = Test call unsatisfactory

108 = Overload check failed

109 = Demand audits not completing

114-132 = Long-time base program entry failures

153 = Recent change time-out

Bit 23 = Flashes at rate of approximately twice per second. If flashing stops and **PHASE IN PROG** indicator is still on, a pump restarted. Display bit 23 must begin flashing within 20 seconds or system is dead or rolling in PCs.

Bit 24-31 = Unassigned

Page 106—Maintenance Utility Processor Status and Control

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □ PORT □  PAGE 106     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR    MINOR    SDC      PGM CTRL   PWR/BLDG    MCC         SYS NORM
   CC          PS       CS    IF/AU        PU       MISC      MCC DPFL
CMD:
                             MUP STATUS AND CONTROL
 -COMMON CONTROL-
410 - SW:MUP                                     AFT
829 - OP:OOSUNITS:MUP            MUP0-S00-ACT    □□□
 -UNIQUE CONTROL-                MUP1-S01-STBY   □□□
601 - PORTS 1&3 INH/ALW
602 - RLS MCC FORCE
    -UAS MODE-
610 - DISABLE ALL UTIL
611 - NORMAL UTIL
612 - UAS NON-INTF ALW
613 - UAS INTF ALW

   -UAS: NORMAL UTIL-
   -MUP ALARMS-
   -MCC TIMEOUT-
   -MUP FORCED-
   -INTF HW ENABLED-
```

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Page 108—System Status

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP    PORT    PAGE 108     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG     MCC         SYS NORM
   CC          PS        CS     IF/AU        PU       MISC       MCC DPFL
CMD:
   -SYSTEM ACTIVITY-        |     -SYSTEM STATUS-          |  -SYSTEM CONTROLS-
BASE CYCLE TIME       ms    |     -RC ACTIVITY-            | 801 - RESTRICT RC
TRAFFIC INCOMING      K     |     -DGN IN PROG-            | 802 - INH SUP PRINT
SWITCH INEF ATMPT     %     |        -ALARMS-              | 803 - INH INT PRINT
EQUIP INEF ATMPT      %     | -REF STAT-   -FREE RUN-      | 804 - INH AUD PRINT
NO. CALLS CMPLTD      K     | -PWR ROOM-   -EQUIP PWR-     | 805 - ELEV AUD PRINT
INTERRUPTS                  | -RB CAP-     -MEM REC PH-    | 806 - REINIT TTY SYS
AUDITS                      | 810 - SDC                    | 807 - REQ TTY AUDIT
SPP LINK OCCPNCY      %     | 811 - PGM CNTL OFF NORM      | 808 - CLEAR INTERRUPTS
                            | 812 - OVLD CTL IN EFF        | 809 - CLEAR MEM REC PHASE
    -MCC TIMEOUT-           | 813 - INTRPT INH             |
     -INTERRUPT-            | 814 - REFSTAT                | 899 - OP:OOSUNITS (ALL)
   -PROCESSOR EQUIPMENT STATUS-                  |   -PERIPHERAL EQUIPMENT STATUS-
820 - CC    826 - IFB    832 - APS   838 - PCD   | 850 - TMSP  856 - DT    862 - TGR
821 - PSB   827 - AUI    833 - API   839 - XPWR  | 851 - TSI   857 - DIF   863 - SLNK
822 - CSB   828 - SSD    834 -       840 - SFI   | 852 - NCLK  858 - VIF   864 - VFL
823 - PS    829 - MUP    835 -       841 - SPP   | 853 - NCSU  859 - EST   865 - R&T
824 - CS    830 - IOUS   836 - AUB               | 854 - SCLK  860 - SCS   866 - SVC
825 - FNS   831 - IOUC   837 - PUB               | 855 - SP    861 - RA    867 - XTSI
```

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Page 109—Program Store Status and Control

```
TOWNSTBLSUB    4E<NN>4B.nn    MUP □ PORT □   PAGE 109    mm/dd/yy    hh:mm:ss
CRITICAL     MAJOR    MINOR     SDC    PGM CTRL    PWR/BLDG    MCC        SYS NORM
   CC         PS       CS      IF/AU      PU        MISC      MCC DPFL
CMD:
                   - PROGRAM STORE STATUS AND CONTROL PAGE -
    -BUS STATUS-     |   -STORE STATUS-   |
                     |               MRSS |
              -CC-   |                 10 |
               0 1   | PS00 ACT  M□□□ □□□□|
              ARAR   | PS01 ACT  M□□□ □□□□|
  PSB 0 ACT  □□□□    | PS02 ACT  M□□□ □□□□|
  PSB 1 STBY □□□□    | PS03 STBY M□□□ □□□□|
   -STORE CONTROL-   | PS04 UPD  M□□□ □□□□|
200,xx - RMV:PSB xx  | PS05 STBY M□□□ □□□□|
201,xx - RMV:PS xx   | PS06 OOS  M□□□ □□□□|
300,xx - RST:PSB xx  | PS07 ACT  M□□□ □□□□|
301,xx - RST:PS xx   | PS08 UNK  M□□□ □□□□|
500,xx - DGN:PSB xx  | PS09 UNEQ          |
501,xx - DGN:PS xx   | PS10 UNEQ          |
723 -OP:PSSTATUS     | PS11 UNEQ M□□□ □□□□|
821 -OP:OOSUNITS:PSB | PS12 UNEQ          |
823 -OP:OOSUNITS:PS  | PS13 UNEQ          |           =DGN IN PROG=
```

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Page 110—Call Store Status and Control

```
TOWNSTBLSUB    4E<NN>4B.nn    MUP □ PORT □   PAGE 110    mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR    MINOR     SDC    PGM CTRL   PWR/BLDG    MCC        SYS NORM
   CC         PS       CS      IF/AU      PU       MISC      MCC DPFL
CMD:
                     - CALL STORE STATUS AND CONTROL PAGE -
    -BUS STATUS-     |                       -STORE STATUS-
                     |              MRSS|                MRSS|                 MRSS
           -CC-      |                10|                  10|                   10
            0 1      |CS00 ACT  M□□□ □□□□|CS14 UNEQ           |CS28 UNEQ
           ARAR      |CS01 ACT  M□□□ □□□□|CS15 UNEQ           |CS29 UNEQ
  CSB 0 ACT  □□□□    |CS02 ACT  M□□□ □□□□|CS16 UNEQ           |CS30 UNEQ
  CSB 1 STBY □□□□    |CS03 STBY M□□□ □□□□|CS17 UNEQ           |CS31 UNEQ
   -STORE CONTROL-   |CS04 ACT  M□□□ □□□□|CS18 UNEQ           |CS32 UNEQ
200,xx - RMV:CSB xx  |CS05 OOS  M□□□ □□□□|CS19 UNEQ           |CS33 UNEQ
201,xx - RMV:CS xx   |CS06 UPD  M□□□ □□□□|CS20 UNEQ           |CS34 UNEQ
300,xx - RST:CSB xx  |CS07 STBY M□□□ □□□□|CS21 UNEQ M□□□ □□□□|CS35 UNEQ
301,xx - RST:CS xx   |CS08 UNEQ          |CS22 UNEQ           |CS36 UNEQ
500,xx - DGN:CSB xx  |CS09 UNK  M□□□ □□□□|CS23 UNEQ           |CS37 UNEQ
501,xx - DGN:CS xx   |CS10 UNEQ          |CS24 UNEQ           |CS38 UNEQ
724 -OP:CSSTATUS     |CS11 UNEQ          |CS25 UNEQ           |CS39 UNEQ
822 -OP:OOSUNITS:CSB |CS12 UNEQ M□□□ □□□□|CS26 UNEQ           |
824 -OP:OOSUNITS:CS  |CS13 UNEQ          |CS27 UNEQ           |   =DGN IN PROG=
```

tpa 786754/01

Page 111—IFB Clients Status and Control

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □  PORT □   PAGE 111     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR    SDC      PGM CTRL   PWR/BLDG     MCC          SYS NORM
   CC          PS        CS     IF/AU       PU        MISC       MCC DPFL
CMD:
                    -IFB CLIENTS STATUS AND CONTROL PAGE-
   -BUS STATUS-    |              -BUS AND CLIENT CONTROL-
             -CC-  |
              0 1  | UNIT     RMV      RST      SW       DGN     OOS  STAT  UNIT
             ARAR  | MUP xx  201,xx   301,xx   401      501,xx  829  726   MUP xx
 IFB 0 ACT   □□□□  | SFI xx  202,xx   302,xx   NA       502,xx  840  727   SFI xx
 IFB 1 ACT   □□□□  | AUI xx  203,xx   303,xx   403      503,xx  827  NA    AUI xx
                   | SSD xx  204,xx   304,xx   NA       504,xx  828  NA    SSD xx
 -DGN IN PROGRESS- | IFB xx  205,xx   305,xx   NA       505,xx  826  728   IFB xx
                                  -CLIENT STATUS-
 MUP  00 ACT  AFT  □□□          SFI  02 UNEQ ALL             ***  ** UNEQ ***
 MUP  01 STBY AFT  □□□          SFI  03 UNEQ ALL             ***  ** UNEQ ***
 MUPP 00                        AUI  00 ACT  ATT  □□□        ***  ** UNEQ ***
 MUPP 01                        AUI  01 ACT  ATT  □□□        ***  ** UNEQ ***
 ***  ** UNEQ ***               ***  ** UNEQ ***             ***  ** UNEQ ***
 ***  ** UNEQ ***               ***  ** UNEQ ***             ***  ** UNEQ ***
 SFI  00 UNEQ ALL               ***  ** UNEQ ***             SSD  00 ACT
 SFI  01 UNEQ ALL               ***  ** UNEQ ***             SSD  01 OOS
```

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Page 118—1B Processor Status

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □  PORT □   PAGE 118     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG     MCC         SYS NORM
   CC          PS        CS     IF/AU        PU       MISC       MCC DPFL
CMD:
                               -1B PROCESSOR STATUS-
       -PROCESSOR-      |      -BUSES-       | -IFB BOOT CLIENTS- |    -AUXILIARY-
                        |             -CC-   |                    |      -UNITS-
                        |             0 1    |                    |
              PFAMTHD   |             ARAR   |              AFT   |                TT
  CC 0 ACTIVE □□□□□□□   |  PSB 0 ACT  □□□□   |  MUP 0 ACT   □□□   |  AUB 0 ACT  □□
  CC 1 STOP   □□□□□□□   |  PSB 1 STBY □□□□   |  MUP 1 STBY  □bb   |  AUB 1 ACT  □□
                        |                    |                    |
  PC STATE: □□          |  CSB 0 ACT  □□□□   |              ATT   |                T
                        |  CSB 1 STBY □□□□   |  AUI 0 ACT   □□□   |  API 0 ACT  □
                        |                    |  AUI 1 UNK   □□□   |  API 1 STBY □
                        |  PUB 0 ACT  □□□□   |                    |
                        |  PUB 1 STBY □□□□   |                    |
                        |                    |                    |
                        |  IFB 0 ACT  □□□□   |                    |
                        |  IFB 1 ACT  □□□□   |                    |
                        |                    |                    |
                        |                    |                    |  =DGN IN PROG=
```

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Page 119—Direct Data Insert Key Options

Page 119 is two pages in length and contains the Direct Data Insert (DDI) keys. One page contains the MRA DDI key assignments; the other page contains the Inhibit Interrupts DDI key assignments. Poke 499 permits toggling between the two pages. Each page is assigned a CC MCD Register [MCD(H) or MCD(L)]. The DDI keys insert data (32 bits) directly into their associated MCD register.

Page 119—Modify Recovery Actions DDI Key Assignments

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □  PORT □   PAGE 119     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG     MCC          SYS NORM
   CC         PS        CS     IF/AU        PU       MISC       MCC DPFL
CMD:
                   499 - TOGGLE MRA / INHIBIT INTERRUPT OPTIONS
                  -MODIFY RECOVERY ACTIONS DDI KEY ASSIGNMENTS-
      401,xx,xx,.... - SET xx; 400,xx,xx,... - RESET xx; 402 - RESET ALL
  00 SET ALL INH                            16 ZERO ALL MEMORY
  01 RB RC TO TAPE 1                        17 SKIP HASHSUM CALCULATION
  02 RB RC TO TAPE 2                        18 BYPASS CC SANITY TESTS
  03 RB RC NO OF ORDRS IN DIS 1  (940)      19 RESERVED
  04 RB RC TO ORNU IN DIS 1  (940)          20 INH MAP AUDITS
  05 CLEAR SPECIFIC DISK AREAS              21 INH STORE ACCESS TESTS
  06 CLEAR NTWK MGMT CONTROLS               22 SPARE
  07 INITIALIZE TRK OOS LIST                23 ALW DUPLEX APS FAILURE IN SR
  08 RESERVED                               24 SKIP MUP RESTART DURING PC/SR
  09 RESERVED                               25 ALW MUP SUPERVISOR MODE UTIL SR
  10 RESERVED                               26 INH IFB ACCESS TEST
  11 RST DUPLEX FAILED CONTRS               27 INH AUTOMATIC DIAGNOSTICS
  12 SPARE                                  28 SPARE
  13 SPARE                                  29 SPARE
  14 ALLOW DUPLEX FAILED PUBB               30 SPARE
  15 RESERVED                               31 SPARE
```

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The Modify Recovery Actions (MRA) DDI keys control various functions used during System Recovery (SR), Activate Override (AO), Processor Configuration (PC), and Phases (PH) as listed in Table 3-C:

Table 3-C. Direct Data Insert Key Identification

DDI Key	Function	Application
00	Leave all pests set during and after the phase. Leave audits in manual-only mode.	PH 1, 2, 3, 4
01	Roll back to tape 1	PH 3, 4
02	Roll back to tape 2	PH 3, 4
03	Roll back number of orders indicated by Page 120, Poke 940 (Display Section 1)	PH 2, 3, 4
04	Roll back to order number indicated by Page 120, Poke 940 (Display Section 1)	PH 2, 3, 4
05	Clear disk areas specified by system integrity program	PH 3, 4
06	Clear network management controls	PH 2, 3, 4
07	Initialize trunk OOS list (TOSL)	PH 3, 4
08-10	Reserved	
11	Restore duplex failed units	PH 3
11	Restore all units to duplex	PH 4
12-13	Reserved	
14	Allow duplex failed PUBB	PH 2, 3, 4, SR
15	Reserved	

See footnotes at end of table.

Table 3-C. Direct Data Insert Key Identification (Contd)

DDI Key	Function	Application
16	Zero all call or program store memory not backed up on disk	AO, PC (pump)
17	Skip hashsum calculations. Skip ID2FS MAP checks.	SR, AO, PC
18	Bypass CC sanity tests and PU tests	PH 3, PH 4, SR, PC
19	Reserved	SR
20	Inhibit MAP audit failures during an SR	SR
21	Inhibit store maintenance tests	SR, AO, PC (pump)
22	Not Used	
23	Allow duplex API failures during SR	SR (MIN CFG EMER MODE)
24	Skip MUP restart during PC/SR	PC, SR
25	Allow MUP supervisor mode utility SR	SR
26	Inhibit IFB access tests	PH 3, PH 4, SR
27	Inhibit automatic diagnostic	PH 3, PH 4, SR
28-31	Reserved	

* Not support for 4E19 generic program.

Legend:

AO - Activate Override
PC - Processor Configuration
PH - Phase(s)
SR - System Reinitialization

Page 119—Inhibit Interrupts DDI Key Assignments

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □  PORT □   PAGE 119     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL   PWR/BLDG     MCC         SYS NORM
   CC          PS        CS     IF/AU        PU       MISC       MCC DPFL
CMD:
                   499 - TOGGLE MRA / INHIBIT INTERRUPT OPTIONS
                   -INHIBIT INTERRUPTS DDI KEY ASSIGNMENTS-
      401,xx,xx,.... - SET xx; 400,xx,xx,... - RESET xx; 402 - RESET ALL
  00 J LEVEL                                16 UNUSED
  01 H LEVEL                                17 K LEVEL SOURCE 0
  02 UNUSED                                 18 UNUSED
  03 UNUSED                                 19 UNUSED
  04 F LEVEL AUTONOMOUS PERIPH (APUFS)      20 UNUSED
  05 F LEVEL PERIPH ORDERS (PUFS)           21 UNUSED
  06 E LEVEL PGM STORES                     22 F LEVEL PERIPH ASW ERROR
  07 D LEVEL STACK UNDER/OVERFLOW           23 F LEVEL PERIPH ANSWER PARITY
  08 D LEVEL PROT AREA WRITE                24 UNUSED
  09 D LEVEL INTERFACE BUS                  25 UNUSED
  10 D LEVEL CALL STORES                    26 UNUSED
  11 B LEVEL PULSE POINTS                   27 UNUSED
  12 A LEVEL UTILITY                        28 UNUSED
  13 D-LEVEL INVALID INSTRUCTION/ADDRESS    29 UNUSED
  14 B LEVEL INTERNAL ERROR                 30 UNUSED
  15 UNUSED                                 31 UNUSED
```

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Page 120—Data Display

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP   PORT    PAGE 120     mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL   PWR/BLDG     MCC        SYS NORM
   CC         PS        CS      IF/AU        PU      MISC       MCC DPFL
CMD:
  -DISPLAY SECTION 1-        |   -WRITE/GCP ALLOWED-     |    -DISPLAY SECTION 2-
911 - CONTENTS MEMORY        | 991 - ALW WRITE           |  921 - CONTENTS MEM/BUFFER
912 - SCAN POINTS            | 992 - ACTIVATE GCP        |  922 - MACP CLIENT
913 - WRITE ADDR/GCP         | 993 - ACTIVATE WRITE      |  923 - WRITE DATA
914 - NMBR BASE TOGGLE       | 994 - MODE TOGGLE         |  924 - NMBR BASE TOGGLE
                             |       -NORMAL-            |
     -DATA INSERT SECTION 1-             |          -DATA INSERT SECTION 2-
   940,xx - DATA O'                      |        950,xx - DATA O'
   941 - INCREMENT                       |       951 - INCREMENT

b                                        |   b
```

tpa 786428/01

Reading the Buffer Bus Registers

To read the contents of the CC Buffer Bus registers, complete the following procedure.

- Obtain the Buffer Bus register number from Chapter 9 — "CC Interrupt Data".
- Obtain Buffer Bus address by adding the Buffer Bus register number to the address below for Active, Standby, or Internal CC.

NOTE:
Read of Internal CC register may cause C-Level interrupts and is not recommended

To Read From	Address Number (Octal)
Active CC	7777776200 + Register number from CC Interrupt Data
Standby CC	7777776600 + Register number from CC Interrupt Data

NOTE:
With the 4E21 and later generic program, the user is able to specify if a 24-bit address or a 30-bit address is to accompany the Poke 950 commands. If bit 30 is set to one (950,1xxxxxxxxxx), the 1B Processor expects a 30-bit address. If bit 30 is set to zero (950,0xxxxxxxxxx), the 1B Processor expects a 24-bit address.

- At Page 120, select Poke 950,xxxxxxxxxxx where xxxxxxxxxxx equals the address in octal to be read

- Enter Poke 921 (**CONTENTS MEM/BUFFER**)
- Read the data at the bottom of the page
- The data can be displayed in Binary, Octal, Decimal, or Hexadecimal by repeatingly entering Poke 924 (**NMBR BASE TOGGLE**).

Reading Signal Processor Scan and Signal Distributor Points

To read the Signal Processor Scan and Signal Distributor Points for Miscellaneous Scanner Number (MSN), Trunk Scanner Number (TSN), Miscellaneous Distributor Number (MDN), or Trunk Distributor Number (TDN), complete the following procedure.

- Obtain the SP Point address for TSN, TDN, MSN or MDN from Chapter 5 — "Signal Processor Point Location".

  NOTE:
  With the 4E21 and later generic programs, the user is able to specify if a 24-bit address or a 30-bit address is to accompany the Poke 940 commands. If bit 30 is set to one (940,1xxxxxxxxxx), the 1B Processor expects a 30-bit address. If bit 30 is set to zero (940,1xxxxxxxxxx), the 1B Processor expects a 24-bit address.

- At Page 120, select Poke 940,xxxxxxxxxxx where xxxxxxxxxxx equals the address in octal to be read
- Enter Poke 912 (**SCAN POINTS**)
- Read the data at the bottom of the page
- The data can be displayed in Binary, Octal, Decimal, or Hexadecimal by repeatingly entering Poke 914 (**NMBR BASE TOGGLE**).

Page 1990—Dead Start

```
TOWNSTBLSUB    4E<NN>4B.nn     MUP □  PORT □   PAGE 1990    mm/dd/yy     hh:mm:ss
CRITICAL     MAJOR     MINOR     SDC      PGM CTRL    PWR/BLDG     MCC         SYS NORM
   CC          PS        CS     IF/AU        PU       MISC       MCC DPFL
CMD:
   -CC CONTROL-         |      -CC REG ACCESS-         |       -MUP TEST-
701 - SUSPEND           | 720,x    - READ CC REG       | 730   - DIAG MUP
702 - RUN               | 721,x,y - WRITE CC REG       | 731   - DIAG MUP/MUI INT
703 - SINGLE STEP       | 722,x,y - WRITE BOL/BOR      | 732,x - READ MUP MEMORY
704 - UPDATE REGS       |                              |
                        |       ADDR:□□□□□□□□□□□□      |     ADDR:□□□□□□□□□□□□
                        |       DATA:□□□□□□□□□□□□      |     DATA:□□□□□□□□□□□□
   -MISCELLANEOUS-      |          -STATUS-            |     -1B PROCESSOR TEST-
710 - INIT US           |     -INTF HW ENABLED-        | 740   - ALL TESTS
711 - AUTO HARD A       |   -UAS:NON-INTERFERING-      | 741,x - SINGLE TEST
712 - BOL/BOR LOCK      |                              |
713 - BASE: OCTAL       |                              |
 BR-□□□□□□□□□□□□  FR-□□□□□□□□□□□□  GR-□□□□□□□□□□□□  JR-□□□□□□□□□□□□  KR-□□□□□□□□□□□□
 LR-□□□□□□□□□□□□  XR-□□□□□□□□□□□□  YR-□□□□□□□□□□□□  ZR-□□□□□□□□□□□□  TR-□□□□□□□□□□□□
CAR-□□□□□□□□□□□□ DAR-□□□□□□□□□□□□  SH-□□    SC-□□  BOL-□□□□□□□□□□□□ BOR-□□□□□□□□□□□□
FLA-□□□□□□□□□□□□ FLD-□□□□□□□□□□□□ FLT-□□□□□□□□□□□□ BSO-□□□□□□□□□□□□ BS1-□□□□□□□□□□□□
BS2-□□□□□□□□□□□□ BS3-□□□□□□□□□□□□ BS4-□□□□□□□□□□□□ BS5-□□□□□□□□□□□□ CSC-□□□□□□□□□□□□
```

tpa 786436/01

Miscellaneous Information

4

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Miscellaneous Information

4

Interface Bus Client Address

AU Address Range	AU Address Bus					Auxiliary Units	
	15	**14**	**13**	**12**	**11**		
17600000 17603777	0	0	0	0	0	API-0	API K-Codes
17604000 17607777	0	0	0	0	1	API-1	
17660000 17663777	0	1	1	0	0	DUS-0	DUS K-Codes
17664000 17667777	0	1	1	0	1	DUS-1	
At least one bit 13, 14, 15 must equal zero (0) to be an AU Address							

1B Processor Memory Layout

Address Range	Attributes	Range	Type	Memory Use Description
40000000-77777777	----	MMIO	DATA	Window Memory
00000000-00027777	P(B&N)A14	LCS	DATA	High Usage - Protected
00030000-00037777	UNA14	LCS	BSS	High Usage - Unprotected
00040000-00047777	UNA21	LCS	BSS	UNA14 Overflow
00050000-02117777	UNA21	LCS	BSS†	Unprotected COMPOOL
02120000-07177777	UNA21	LCS	BSS†	ODA Engineered
07200000-07377777	PNA21	LCS	TEXT	Library Area (CS KCODE 35)
07400000-07777777	PBA21	LCS	DATA	PBAC/PBAL (CS KCODEs 36 & 37)
10000000-13777777	PBA22	PS	TEXT	PS Text
14000000-14237777 14000000 14017740 14020000	PBA22	PS	TEXT	80K Pump Area Beginning of Vector Table Beginning of Utility Execute Table Bonded Interrupt Handlers
14400000-14422677	PNA-Nonzero PNA-Zero	PS	Data	Fault Recovery Data
14422700-14507777	Core-Page	PS	Hole	Paging Areas
14510000-17777777	PBA22	PS	TEXT	PS Text

See legend and footnotes at end of table.

1B Processor Memory Layout (Contd)

Address Range	Attributes	Range	Type	Memory Use Description
20000000-20027777	PN23	UCS	DATA	Protected UCS
20030000-32357777	UN23	UCS	BSS	Unprotected ODA Unprotected COMPOOL ODA Engineered
	PB23	UCS	DATA	ODA-Translation
32360000-3357777	PB23	UCS	TEXT	PSBX (Protected, Backed Executed Text)
33600000-33777777	Core XS	UCS	Hole	Reserved for XS
34000000-37577777	----	PSE	INT	PS Text
37600000-37657777	----	MMIO	INT	Individual client MMIO O’(37600000)+(O’(1777) *IFB slot#)
37660000-37667777	----	MMIO	INT	Unused
37670000-37670377	----	MMIO	INT	Relocation Region for MMIO
37670400-37677777	----	MMIO	INT	Unused
37700000-37767777	----	ROM	INT	BOOT ROM
37770000-37775777	----	BB	INT	Unused
37776000-37776377	----	BB	INT	Active CC Buffer Bus
37776400-37776777	----	BB	INT	Standby CC Buffer Bus
37777000-37777377	----	BB	INT	Invalid Buffer Bus
37777400-37777777	----	BB	INT	Internal Buffer Bus

See legend and footnotes at end of table.

1B Processor Memory Layout (Contd)

Legend:

P	= Protected	LCS	= Lower Call Store
U*	= Unprotected (via LPA/UPA)	UCS	= Upper Call Store
B	= Disk Backed	ODA	= Office Data Assembler
A	= AUB/API Addressable	MMIO	= Memory Mapped I/O (IFB Access)
N	= Non-disk backed	PBAC	= Common ODA translators
14	= 14-bit Addressable	PBAL	= Programs and tables, loader populated
21	= 21-bit Addressable	BSS	= Uninitialized data
22	= 22-bit Addressable	TEXT	= Executable code
23	= 23-bit Addressable		
INT	= CC Internal Reserved Addresses		
DATA	= Initialized data		
PSE	= Program Store Expansion		

* This area may or may not be protected via the store write protection.

† These BSS areas are more valuable than the BSS area in UCS, which should be allocated first.

1B Processor MCODE Designations

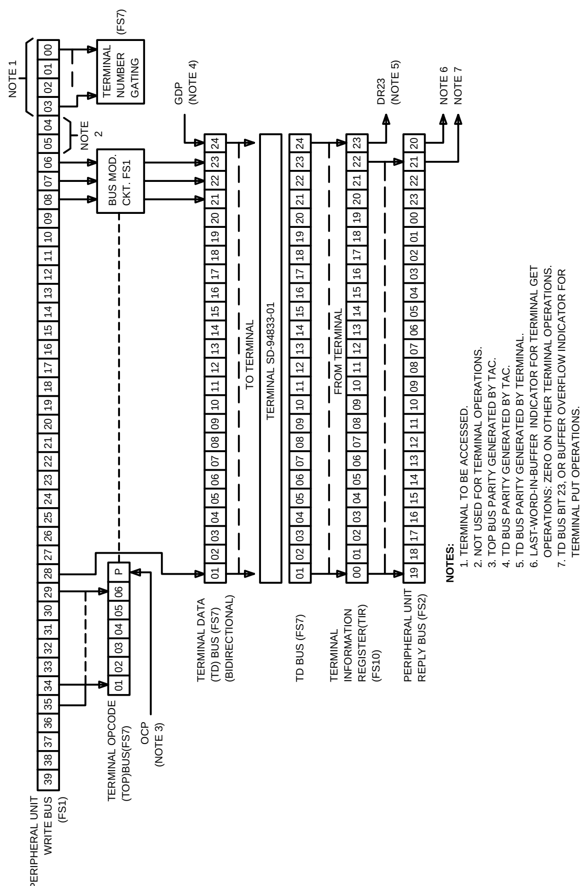
MCODE*			
Physical	**Logical**	**O'(Address Range)**	**Communities**
010-011	—	40000000-47777777	Paged-Disk Only
012-017	—	50000000-77777777	Windowed XS ‡
770	0	00000000-03777777 †	Lower CS
771	1	04000000-07777777 †	Lower CS
772	2	10000000-13777777 †	Base PS
773	3	14000000-17777777 †	Base PS, PS Power Up
774	4	20000000-23777777 †	Upper CS
775	5	24000000-27777777 †	Upper CS
776	6	30000000-33577777 † 33600000-33777777 †	Upper CS Extended Access Windows
777	7	34000000-37577777 † 37600000-37677777 † 37700000-37767777 † 37770000-37775777 † 37776000-37776377 † 37776400-37776777 † 37777000-37777377 † 37777400-37777777 †	PSE MMIO BOOT ROM Unused Active CC Standby CC Invalid Buffer Bus Internal Buffer Bus

* The term MCODE can be described in several ways. When MCODE refer to a store, the MCODE implies a 9-bit physical MCODE (bits 28-20) or a 3-bit logical MCODE (bits 22-20).

† All addresses are relative to the base address of O'(7740000000) which is loaded into Transition Address Register (TAR).

‡ MCODEs available (may not be equipped or only partially equipped depending on the office).

Common Channel Interoffice Signaling Terminal Access Controls—-Term Data Flow



Digroup Terminal Unit—Terminal Unit Bit/Function Layout

Bit	Function 0	Function 1	Function 2	Function 3 (4, 5, 6, 7)
0	NAME:PKSLPO FS1,0615 FA1114-011 PARITY CHECK ON SLIP SCAN 0616-316 STROBE-118	NAME:1CPDS90 FS2,0213 FA1136-214 *FA1112-106 XMT CONV FRAME BIT COMP (DIGROUP 1) SCAN 0616-007 STROBE-109	NAME:PV1NV1 FS10,0223 FA1125-216 TSI RCV PAIR VIOL 0-6 SCAN 0217-316 STROBE-118	NAME:CPESGLO FS6,0623 FA1120-202 E-SIG STORE COMP (TEST DG) SCAN 0217-007 STROBE-109
1	NAME:PKSLPO FS1,0615 FA1114-011 PARITY CHECK ON SLIP SCAN 0616-214 STROBE-218	NAME:2CPDS90 FS2,0211 FA1136-214 *FA1112-106 XMT CONV FRAME BIT COMP (DIGROUP 2) SCAN 0616-305 STROBE-009	NAME:PV1NVO FS10,0223 FA1125-215 TSI RCV PAIR VIOL 7 SCAN 0217-214 STROBE-218	NAME:CPESGLO FS6,0623 FA1120-202 E-SIG STORE COMP (TEST DG) SCAN 0217-305 STROBE-009
2	NAME:PKDSWRO FS1,0615 FA1114-304 PARITY CHECK ON REC DATA (DG1-5) SCAN 0616-013 STROBE-016	NAME:3CPDS90 FS2,0209 FA1136-214 *FA1112-106 XMT CONV FRAME BIT COMP (DIGROUP 3) SCAN 0616-105 STROBE-308	NAME:ALMCTR1 FS3,0224 FA1143-111 ALARM ON COUNTERS REGISTER *NAME:PV1NV1 *FS10,0223 *FA1125-216 *TSI RCV *PAIR VIOL 0-6 SCAN 0217-013 STROBE-016	NAME:CPESGLO FS6,0623 FA1120-202 E-SIG STORE COMP (TEST DG) SCAN 0217-105 STROBE-308

NOTE:
Asterisk (*) indicates layout for older vintage J68952A DT frame only.

Digroup Terminal Unit—Terminal Unit Bit/Function Layout (Contd)

	Function			
Bit	**0**	**1**	**2**	**3 (4, 5, 6, 7)**
3	NAME:1PKRCO FS1,1018 FA1110-018 RECEIVE CONVERTER PARITY CHECK (DIGROUP 1) SCAN 0616-315 STROBE-317	NAME:4CPDS90 FS2,0207 FA1136-214 *FA1112-106 XMT CONV FRAME BIT COMP (DIGROUP 4) SCAN 0616-106 STROBE-209	NAME:1PKTCO FS2,0213 FA1136-212 *FA1112-219 XMT CONV PARITY CHECK (DIGROUP 1) SCAN 0217-315 STROBE-317	NAME:ALMUGWC1 FS3,1021 FA1137-208 ALARM GWC CTR *NAME:CPESGLO *FS6,0623 *FA1120-202 *E-SIG *STORE COMP *(TEST DG) SCAN 0217-106 STROBE-209
4	NAME:2PKRCO FS1,1012 FA1110-018 RECEIVE CONVERTER PARITY CHECK (DIGROUP 2) SCAN 0616-312 STROBE-219	NAME:PKSLP1 FS1,0615 FA1114-311 PARITY CHECK ON SLIP SCAN 0616-104 STROBE-204	NAME:2PKTCO FS2,0211 FA1136-212 *FA1112-219 XMT CONV PARITY CHECK (DIGROUP 2) SCAN 0217-312 STROBE-219	NAME:PKSGLO FS6,0623 FA1120-003 ACC PARITY CHECK E-SIG (DG1-5) SCAN 0217-104 STROBE-204
5	NAME:3PKRCO FS1,1009 FA1110-018 RECEIVE CONVERTER PARITY CHECK (DIGROUP 3) SCAN 0616-115 STROBE-215	NAME:5CPDS90 FS2,0205 FA1136-214 *FA1112-106 XMT CONV FRAME BIT COMP (DIGROUP 5) SCAN 0616-005 STROBE-108	NAME:3PKTCO FS2,O209 FA1136-212 *FA1112-219 XMT CONV PARITY CHECK (DIGROUP 3) SCAN 0217-115 STROBE-215	NAME:CPKSGLO FS6,0623 FA1120-105 ACC PARITY CHECK COMP E-SIG (TEST DG) SCAN 0217-005 STROBE-108

NOTE:
Asterisk (*) indicates layout for older vintage J68952A DT frame only.

Digroup Terminal Unit—Terminal Unit Bit/Function Layout (Contd)

	Function			
Bit	**0**	**1**	**2**	**3 (4, 5, 6, 7)**
6	NAME:4PKRCO FS1,1006 FA1110-018 RECEIVE CONVERTER PARITY CHECK (DIGROUP 4) SCAN 0616-114 STROBE-314	NAME:PKDSWR1 FS1,0615 FA1114-105 PARITY CHECK ON REC DATA (TEST DG) SCAN 0616-304 STROBE-208	NAME:4PKTCO FS2,0207 FA1136-212 *FA1112-219 XMT CONV PARITY CHECK (DIGROUP 4) SCAN 0217-114 STROBE-314	NAME:ALMFRGBC1 FS3,1021 FA-1137-210 ALARM FRAMING GBC COUNTERS *NAME:CPKSGLO *FS6,0623 *FA1120-105 *ACC *PARITY CHECK *COMP E-SIG *(TEST DG) SCAN 0217-304 STROBE-208
7	NAME:SPKRCO FS1,1003 FA1110-018 RECEIVE CONVERTER PARITY CHECK (DIGROUP 5) SCAN 0616-012 STROBE-017	NAME:PKDSWR1 FS1,0615 FA1114-105 PARITY CHECK ON REC DATA (TEST DG) SCAN 0616-203 STROBE-204	NAME:5PKTCO FS2,0205 FA1136-212 *FA1112-219 XMT CONV PARITY CHECK (DIGROUP 5) SCAN 0217-012 STROBE-017	NAME:PKRMAO FS5,0620 FA1122-001 ACC PARITY CHECK RMA (DG1-5) SCAN 0217-203 STROBE-204
8	NAME:CPPYDTO FS9,0218 FA1123-105 PARITY CHECK OVER RBOX- TBOXLOOP DATA SCAN 0616-309 STROBE-011	NAME:CP1FO FS4,0624 FA1116-103 COMP STAT IN FRAME (TEST DG) SCAN 0616-003 STROBE-204	NAME:CPMSGLO FS7,0215 FA1115-013 M-STORE SIG COMP (TEST DG) SCAN 0217-309 STROBE-011	NAME:CFA11 FS10,0222 FB241-208 TSI RCV CLOCK FAIL ALARM (A) SCAN 0217-003 STROBE-204
9	NAME:PKDEVN1 FS9,0218 FA1123-003 PARITY CHECK EVEN TRANSM DATA SCAN 0616-112 STROBE-015	NAME:CPETMNO FS4,0624 FA1116-301 COMP FRAME ERR TMG (TEST DG) SCAN 0616-002 STROBE-204	NAME:CPRGPAO FS7,0215 FA1115-211 XMT STORE MX READ ADD COMP SCAN 0217-112 STROBE-015	NAME:CFA21 FS10,0222 FB241-201 TSI RCV CLOCK FAIL ALARM (B) SCAN 0217-002 STROBE-204

NOTE:
Asterisk (*) indicates layout for older vintage J68952A DT frame only.

Digroup Terminal Unit—Terminal Unit Bit/Function Layout (Contd)

Function

Bit	0	1	2	3 (4, 5, 6, 7)
10	NAME:PKDODD1 FS9,0218 FA1123-001 PARITY CHECK ODD TRANSM DATA SCAN 0616-212 STROBE-217	NAME:CPFPFO FS4,0624 FA1116-004 COMP PULSE FRAMING (TEST DG) SCAN 0616-301 STROBE-204	NAME:CPRGPAO FS7,O215 FA1115-211 XMT STORE MX WRITE ADD COMP SCAN 0217-211 STROBE-217	NAME:PKLCAO FS5,0619 FA1121-105 ACC PARITY CHECK LCA (DG1-5) SCAN 0217-301 STROBE-204
11	NAME:PK10DRO FS1,1015 FA1135-015 *FA1113-100 PARITY OUTPUT DATA REC BITS (DIGROUP 1) SCAN 0616-008 STROBE-210	NAME:CPSADEO FS4,0626 FA1118-115 COMP SHIFT ADDRESS ENABLE (TEST DG) SCAN 0616-101 STROBE-004	NAME:PKTPO FS7,0215 FA1115-207 ACC PARITY CHECK XMT PROC (DG1-5) SCAN 0217-008 STROBE-210	NAME:CPDFAO FS5,0619 FA1121-305 DFA COMPARE (TEST DG) SCAN 0217-101 STROBE-004
12	NAME:PK20DR0 FS1,1015 FA1135-015 *FA1113-205 PARITY OUTPUT DATA REC BITS (DIGROUP 2) SCAN 0616-311 STROBE-014	NAME:CPSADOO FS4,0626 FA1118-016 COMP SHIFT ADDRESS 0 (TEST DG) SCAN 0616-001 STROBE-004	NAME:PKTP1 FS7,0215 FA1115-007 ACC PARITY CHECK XMT PROC (TEST DG) SCAN 0217-311 STROBE-014	NAME:CPLCAO FS5,0619 FA1121-007 LCA COMPARE (TEST DG) SCAN 0217-001 STROBE-004
13	NAME:PK30DRO FS1,1015 FA1135-015 *FA1113-304 PARITY OUTPUT DATA REC BITS (DIGROUP 3) SCAN 0616-206 STROBE-110	NAME:CPSAD10 FA4,0626 FA1118-011 COMP SHIFT ADDRESS 1 (TEST DG) SCAN 0616-201 STROBE-004	NAME:PK1DTO FS7,0215 FA1115-008 DATA PARITY CHECK XMT PROC (DG1-5) SCAN 0217-206 STROBE-110	NAME:CPKLCA0 FS5,0619 FA1121-207 ACC PARITY CHECK COMP LCA (TEST DG) SCAN 0217-201 STROBE-004

NOTE:
Asterisk (*) indicates layout for older vintage J68952A DT frame only.

Digroup Terminal Unit—Terminal Unit Bit/Function Layout (Contd)

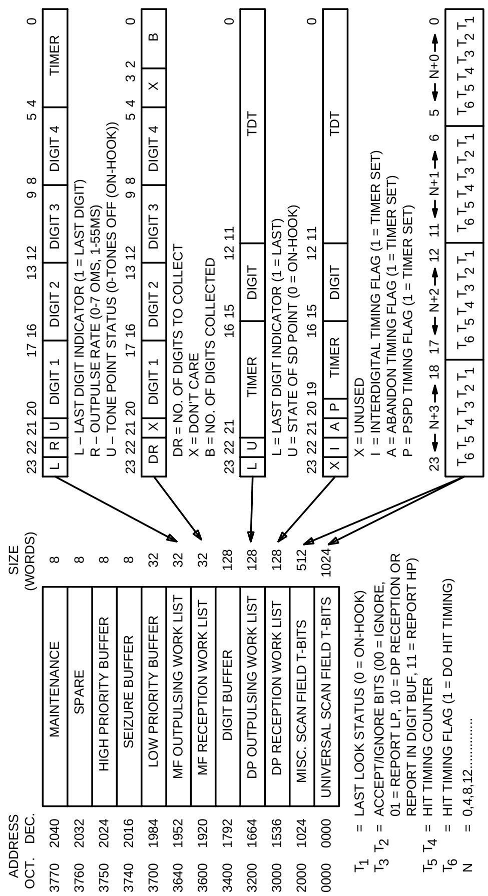
Function

Bit	0	1	2	3 (4, 5, 6, 7)
14	NAME:PK40DRO FS1,1015 FA1135-015 *FA1113-005 PARITY OUTPUT DATA REC BITS (DIGROUP 4) SCAN 0616-006 STROBE-113	NAME:CPSAD20 FS4,0626 FA1118-108 COMP SHIFT ADDRESS 2 (TEST DG) SCAN 0616-211 STROBE-O04	NAME:PK1DT1 FS7,0215 FA1115-208 DATA PARITY CHECK XMT PROC (TEST DG) SCAN 0217-006 STROBE-113	NAME:CPRMA0 FS5,0620 FA1122-018 RMA COMPARE (TEST DG) SCAN 0217-211 STROBE-004
15	NAME:PK50DRO FS1,1015 FA1135-015 *FA1113-002 PARITY OUTPUT DATA REC BITS (DIGROUP 5) SCAN 0616-010 STROBE-213	NAME:CPSAG60 FS4,0626 FA1118-106 COMP SHIFT ADDRESS>6 (TEST DG) SCAN 0616-300 STROBE-004	NAME:CPY1DTO FS7,0215 FA1115-011 XMT PROC UPDATED PARITY COMP (TEST DG) SCAN 0217-010 STROBE-213	NAME:CPKRMA0 FS5,0620 FA1122-117 ACC PARITY CHECK COMP RMA (TEST DG) SCAN 0217-300 STROBE-004

NOTE:
Asterisk (*) indicates layout for older vintage J68952A DT frame only.

Signal Processor Memory Layout

Signal Processor 1



Signal Processor 2

ADDRESS OCT.	ADDRESS DEC.		SIZE (WORDS)
5400	2816	ECHO SUPPRESSION DATA (DT4-7)	256
5100	2624	ECHO SUPPRESSION DATA (DT1-3)	192
5000	2560	SPARE	64
4400	2304	UNIVERSAL SD FIELD	256
4000	2048	UNIVERSAL SCAN FIELD	256
3770	2040	MAINTENANCE	8
3760	2032	SPARE	8
3750	2024	HIGH PRIORITY BUFFER	8
3740	2016	SEIZURE BUFFER	8
3700	1984	LOW PRIORITY BUFFER	32
3640	1952	MF OUTPULSING WORK LIST	32
3600	1920	MF RECEPTION WORK LIST	32
3400	1792	DIGIT BUFFER	128
3200	1664	DP OUTPULSING WORK LIST	128
3000	1536	DP RECEPTION WORK LIST	128
2400	1280	DT MAINTENANCE DATA	256
2000	1024	MISCELLANEOUS SCAN FIELD T-BITS	256
0000	0000	UNIVERSAL SCAN FIELD T-BITS	1024

SAME LAYOUT AS SPI

SAME LAYOUT AS SPI

ADDRESS OCT.	ADDRESS DEC.		SIZE (WORDS)
2700	1472	UNUSED	64
2660	1456	INCOMING MESSAGE HALF 2	16
2640	1440	INCOMING MESSAGE HALF 1	16
2620	1424	OUTGOING MESSAGE HALF 2	16
2600	1408	OUTGOING MESSAGE HALF 1	16
2520	1360	UNUSED	48
2500	1344	STATUS WORDS	16
2400	1280	STATUS WORD T-BITS	64

Signal Processor

Port Selection

$$\text{PM} = 0000\underbrace{40\text{XX}}_{\text{OP CODE}}$$

ADDRESS BUS OP CODE = 4000/4037
PORT = OP CODE MINUS 4000

DATA BUS OP CODE = 4040 & UP
PORT = OP CODE MINUS 4040

Signal Processor Point Location

To check the SPs scan or SD points for a failing circuit, first the TSN or TDN must be determined. Use the following verify message.

VER:TRKNAME,CIN a!

Where *a* is a valid CIN

VER:TRKNAME,CIN 1GNBONCEUDSD03T!

```
M 12 VER:TRKNAME,CIN 1 GNBO NC EU DSD 03T: ISC DOMCCIS OSC DOMCCIS
   OTAN 036601 — TAN 07 1 3 001 <- OCTAL AND DECIMAL TAN
   CIN 1 GNBO NC EU DSD 03T — BTFN 1
   TSN 1324801 — TSN O’157601 <- DECIMAL AND OCTAL TSN
   DIF 13,DIU 31, DG 1 <- DT, DIF, or VIF
   10/27/96 14:12:44
   #752
```

TST or TDT (Lower 12 bits) of the	SP Point address	K K
TSN or TDN	0000-1023	0
	1024-2047	1
	2048-3071	2
	3072-4095	3
MSN or MDN	0000-1023	4
	1024-2047	5

Subtract the lowest address in the K from the given address; divide the result by 16 (decimal) to find the row (the remainder in this division is the column); convert the row to octal, and access the appropriate SP pack location table.

Signal Processor Point Location (Contd)

TSN, TDN, MSN, OR MDN Binary Format

16 - - - 12	11 10	9 - - - - 4	3 - - 0
SP Member Number	K	Row	Column
	SP Point TST—Trunk Scanner Tag TDT—Trunk Distributor Tag		

Scan Point Pack Locations FB 230

ROWS (0CTAL)	0 - 3 0 - 3	4 - 7 4 - 7	10 - 13 8 - 11	14 - 17 12 - 15
*00-*03	-04	-05	-06	-07
*04-*07	-08	-09	-10	-11
*10-*13	-12	-13	-14	-15
*14-*17	-16	-17	-18	-19
*20-*23	-26	-27	-28	-29
*24-*27	-30	-31	-32	-33
*30-*33	-34	-35	-36	-37
*34-*37	-38	-39	-40	-41
*40-*43	-04	-05	-06	-07
*44-*47	-08	-09	-10	-11
*50-*53	-12	-13	-14	-15
*54-*57	-16	-17	-18	-19
*60-*63	-26	-27	-28	-29
*64-*67	-30	-31	-32	-33
*70-*73	-34	-35	-36	-37
*74-*77	-38	-39	-40	-41

COLUMN (OCTAL)
COLUMN (DECIMAL)

FRAME LOCATION ROWS (rows *00-*37):
150-K0, 650-K1, 163-K2, 663-K3: UNIV TSN
168-K4, 668-K5: MISC MSN

FRAME LOCATION ROWS (rows *40-*77):
250-K0, 750-K1, 263-K2, 763-K3: UNIV TSN
268-K4, 768-K5: MISC MSN

NOTES:

1. SINCE THERE ARE ONLY 2 BINARY BITS AVAILABLE FOR THE K, MISCELLANEOUS K'S 4 AND 5 MUST BE DERIVED BY ADDING 4 TO THE 0 AND 1K VALUES IN MSN'S & MDN'S.

2. NUMBERS IN CHART REPRESENT PACK LOCATIONS IN MATRIX FRAMES OF FB 230 PACKS.

* = USED TO TELL WHICH FRAME LOCATION ROW TO SELECT.

Distribute Applique Pack Locations FB 228

ROWS (OCTAL) \ COLUMNS (OCTAL) / COLUMNS (DECIMAL)	0 1 / 0 1	2 3 / 2 3	4 5 / 4 5	6 7 / 6 7	10 11 / 8 9	12 13 / 10 11	14 15 / 12 13	16 17 / 14 15	FRAME LOCATION ROWS
*00,*02 *04,*06	-2P	-04	-38P	-40	-08P	-10	-44P	-46	024-K0, 524-K1, 040-K2, 540-K3 (UNIV TDN); 056-K4, 556-K5 (MISC MDN)
*01,*03 *05,*07	-5P	-07	-41P	-43	-11P	-13	-47P	-49	
*10,*12 *14,*16	-21P	-23	-57P	-59	-27P	-29	-63P	-65	
*11,*13 *15,*17	-24P	-26	-60P	-62	-30P	-32	-66P	-68	
*20,*22 *24,*26	-2P	-04	-38P	-40	-08P	-10	-44P	-46	028-K0, 528-K1, 044-K2, 544-K3 (UNIV TDN); 060-K4, 560-K5 (MISC MDN)
*21,*23 *25,*27	-5P	-07	-41P	-43	-11P	-13	-47P	-49	
*30,*32 *34,*36	-21P	-23	-57P	-59	-27P	-29	-63P	-65	
*31,*33 *35,*37	-24P	-26	-60P	-62	-30P	-32	-66P	-68	
*40,*42 *44,*46	-2P	-04	-38P	-40	-08P	-10	-44P	-46	032-K0, 532-K1, 048-K2, 548-K3 (UNIV TDN); 064-K4, 564-K5 (MISC MDN)
*41,*43 *45,*47	-5P	-07	-41P	-43	-11P	-13	-47P	-49	
*50,*52 *54,*56	-21P	-23	-57P	-59	-27P	-29	-63P	-65	
*51,*53 *55,*57	-24P	-26	-60P	-62	-30P	-32	-66P	-68	
*60,*62 *64,*66	-2P	-04	-38P	-40	-08P	-10	-44P	-46	036-K0, 536-K1, 052-K2, 552-K3 (UNIV TDN); 068-K4, 568-K5 (MISC MDN)
*61,*63 *65,*67	-5P	-07	-41P	-43	-11P	-13	-47P	-49	
*70,*72 *74,*76	-21P	-23	-57P	-59	-27P	-29	-63P	-65	
*71,*73 *75,*77	-24P	-26	-60P	-62	-30P	-32	-66P	-68	

NOTES:

1. SINCE THERE ARE ONLY 2 BINARY BITS AVAILABLE FOR THE K, MISCELLANEOUS K'S 4 AND 5 MUST BE DERIVED BY ADDING 4 TO THE 0 AND 1K VALUES IN MSN'S AND MDN'S.
2. NUMBERS IN SQUARES REPRESENT PACK LOCATIONS IN APPLIQUE FRAME OF FB228 PACKS.

* = K, USED TO TELL WHICH FRAME LOCATION ROW TO SELECT.

Distribute Matrix Pack Locations FA 605

ROWS (OCTAL)	0 - 3 0 - 3	4 - 7 4 - 7	10 - 13 8 - 11	14 - 17 12 - 15	FRAME LOCATION PACKS
					← COLUMN (OCTAL) ← COLUMN (DECIMAL)
*00-*07	-08	-14	-09	-15	128-K0 628-K1 UNIV 132-K2 TDN 632-K3 145-K4 MISC 645-K5 MDN
*10-*17	-11	-17	-12	-18	
*20-*27	-28	-34	-29	-35	
*30-*37	-31	-37	-32	-38	
*40-*47	-08	-14	-09	-15	228-K0 728-K1 UNIV 232-K2 TDN 732-K3 245-K4 MISC 745-K5 MDN
*50-*57	-11	-17	-12	-18	
*60-*67	-28	-34	-29	-35	
*70-*77	-31	-37	-32	-38	

NOTES:

1. SINCE THERE ARE ONLY 2 BINARY BITS AVAILABLE FOR THE K, MISCELLANEOUS K'S 4 AND 5 MUST BE DERIVED BY ADDING 4 TO THE 0 AND 1 K VALUES IN MSN'S AND MDN'S.
2. NUMBERS IN CHART REPRESENT PACK LOCATIONS IN APPLIQUE FRAMES OF FA 605 PACKS.

* = K, USED TO TELL WHICH FRAME LOCATION ROW TO SELECT

Signal Distribute Pulse Points Locations

Matrix Pack Locations FA 610

ROW (OCTAL) \ COLUMN (OCTAL) / COLUMN (DECIMAL)	0 - 3 0 - 3	4 - 7 4 - 7	10 - 13 8 - 11	14 - 17 12 - 15
*40-*47	-08	-14	-09	-15
*50-*57	-11	-17	-12	-18
*60-*67	-28	-34	-29	-35
*70-*77	-31	-37	-32	-38

245-K4
745-K5

FRAME
LOCATION
ROWS

ROW
(OCTAL)

NOTES:

1. SINCE THERE ARE ONLY 2 BINARY BITS AVAILABLE FOR THE K, MISCELLANEOUS K'S 4 AND 5 MUST BE DERIVED BY ADDING 4 TO THE 0 AND 1K VALUES IN MSN'S AND MDN'S.
2. NUMBERS IN CHART REPRESENT PACK LOCATIONS IN MATRIX FRAMES OF FA 610 PACKS.

Pack Locations FB 229

ROW (OCTAL)	0 1	2 3	4 5	6 7	10 11	12 13	14 15	16 17	COLUMN (OCTAL)
	0 1	2 3	4 5	6 7	8 9	10 11	12 13	14 15	COLUMN (DECIMAL)
*40,*42 *44,*46	-02P	-04	-33P	-35	-08P	-10	-39P	-41	064-K4 564-K5
*41,*43 *45,*47	-05P	-07	-36P	-38	-11P	-13	-42P	-44	
*50,*52 *54,*56	-17P	-19	-48P	-50	-23P	-25	-54P	-56	
*51,*53 *55,*57	-20P	-22	-51P	-53	-26P	-28	-57P	-59	
*60,*62 *64,*66	-02P	-04	-33P	-35	-08P	-10	-39P	-41	068-K4 568-K5
*61,*63 *65,*67	-05P	-07	-36P	-38	-11P	-13	-42P	-44	
70,72 *74,*76	-17P	-19	-48P	-50	-23P	-25	-54P	-56	
*71,*73 *75,*77	-20P	-22	-51P	-53	-26P	-28	-57P	-59	

FRAME LOCATION ROWS

NOTES:

1. SINCE THERE ARE ONLY 2 BINARY BITS AVAILABLE FOR THE K, MISCELLANEOUS K'S 4 AND 5 MUST BE DERIVED BY ADDING 4 TO THE 0 AND 1K VALUES IN MSN'S & MDN'S.
2. NUMBERS IN CHART REPRESENT PACK LOCATIONS IN APPLIQUE FRAMES OF FB 229 PACKS.

Breakdowns

Trunk Appearance Number Breakdown (TAN)

Bit 0-6 = Time slot
7-9 = TSI level (Buffer A)
10 = SPC in TSI
11-16 = TSI member number

NOTE:
The relationship of buffer A in TAN to buffer B in TN is as follows:

BUFB = BUFA + CHAN number MOD 8

Trunk Number Breakdown (TN)

BIT 0-6 = Time slot
7-9 = Buffer B (TSI Level after decorrelation)
10 = SPC in TSI
11-16 = TSI member number

Trunk Scanner Number Breakdown (TSN)

BIT 0-3 = Column in SP matrix
4-9 = Row in SP matrix
10-11 = Block in SP matrix
12-16 = SP member number

Memory Connect/Disconnect Instruction Layout

Time-Multiplex Switch (TMS)

BIT 1-7 = Time Slot
10-16 = Source switching and permuting circuit (SPC)
17-23 = Destination SPC
24-27 = Path
29-35 = Operation code

Time-Multiplex Switch OPCODEs

Octal:

10 = Full connect
20 = Full disconnect
30 = Long memory read
40 = Memory write

Time-Slot Interface (TSI)

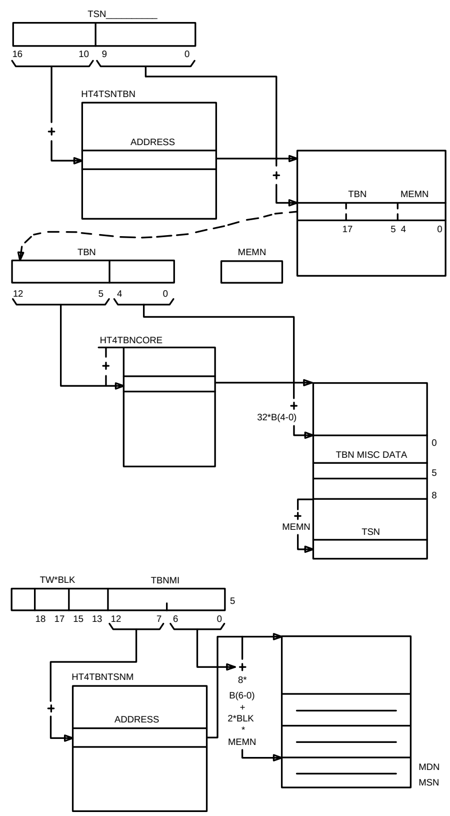
BIT 0-6 = Channel
7-9 = BMB or BMC level
10-16 = Time slot
19-21 = Serial switch level
29-35 = Operation code

Time-Slot Interface OPCODEs

Octal:

10 = Set up input
11 = Set up both
12 = Set up output
13 = Read both
15 = Read BIMM
20 = Take down input
21 = Take down both
22 = Take down output
52 = Write RTSI
53 = Write TTSI
55 = Write BIMM

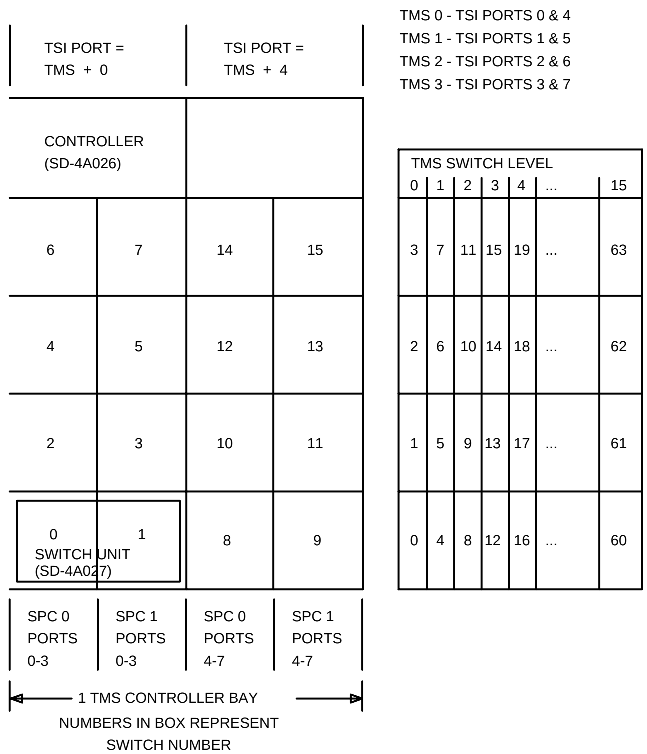
Trunk Scanner Number to Trunk Block and Memory Number Translator



NOTE: IF MISC INFORMATION IS SPECIFIED USE BLOCK DIAGRAM TBN MI.

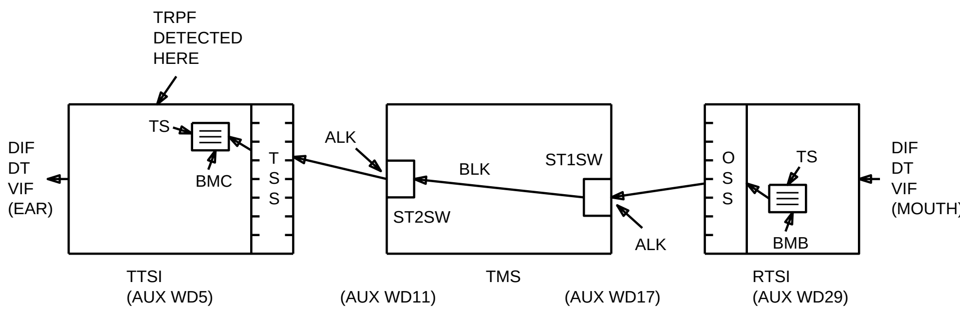
*TW = 10 FOR TBNMISC ACCESS

Time-Multiplex Switch Port to Time-Slot Interface Port Translator for 4 Time-Multiplex Switch Office



NOTE: XMT JACK ON TMS CONNECTS TO XMT ON TSI. XMT AND RCV ARE RELATIVE TO TMS.

Time-Division Number Path for Transit-Parity Failure Analysis (TRPF)



Legend:

ALK	=	A-Link	SW	=	Block
AUX	=	Auxiliary	TMS	=	Time-Multiplex Switch
BLK	=	B-Link	TRPF	=	Transit-Parity Failure
BMB	=	Buffer Memory B	TS	=	Time-slot
BMC	=	Buffer Memory C	TTSI	=	Transmit Time-slot Interchange
DIF	=	Digital Interface Frame	VIF	=	Voiceband Interface Frame
DT	=	Digital Trunk			
RTSI	=	Receive Time-slot Interchange			

Location Data

Receive Time-Slot Interchange FA533

TMS CONTR	SPC	TSI-1 EQL	TSI-2 EQL
0	0	076-03	076-23
0	1	076-04	076-22
0	2		076-07
0	3		076-06
1	0	176-03	176-23
1	1	176-04	176-22
1	2		176-07
1	3		176-06

Receive Time Slot Interchange FA533 (Contd)

Data Present at Following Pins:

RPORT	FA533 Inputs* (True Data)	FA533 Output (True Data, 2 V)
0	202 002	106
1	118 317	213
2	204 104	107
3	301 101	108
4	314 015	110
5	117 017	211
6	005 304	209
7	115 215	212

* First entry input from RCONTR 0, second from RCONTR 1.

Receive Time-Slot Interchange

FA544, FA1198, and FA545 (TSI-1)

		Horizontal EQL		Vertical EQL	
DSR Level From Trace	**FA544 (4A024-01)**	**FA1198 (4A024-01)**	**FA545**	**SPC0**	**SPC1**
0	26	26	27,28	50	72
1	25	26	27,28	50	72
2	24	24	27,28	50	72
3	23	24	27,28	50	72
4	22	22	27,28	50	72
5	21	22	27,28	50	72
6	20	20	27,28	50	72
7	19	20	27,28	50	72

Notes:

1. Data present at PIN 219 of FA544 (inverted polarity).
2. Data present at PIN 314 (even levels) and PIN 219 (odd levels) of FA 1198 (inverted polarity).
3. TSI bay is the same as RCONTR.

FA1780 (or FA1816) and FA545 (TSI-2)

RTSI Level From F-Level TRACE	Horizontal EQL		Vertical EQLS			
	FA1780 or FA1816	FB545	SPC0	SPC1	SPC2	SPC3
0	58	47,49	28	40	52	64
1	56	47,49	28	40	52	64
2	54	47,49	28	40	52	64
3	51	47,49	28	40	52	64
4	43	47,49	28	40	52	64
5	41	47,49	28	40	52	64
6	39	47,49	28	40	52	64
7	37	47,49	28	40	52	64

Notes:

1. Data present at PIN 100 of FA1780 or FA1816 (inverted polarity).
2. TSI bay is the same as RCONTR.

Transmit Time-Slot Interchange

Location Data

TMS CONTR	SPC	FA524 TSI-1 EQL	FA1808 TSI-2 EQL
0	0	076-06	076-26
0	1	076-07	076-25
0	2		076-10
0	3		076-09
1	0	176-06	176-26
1	1	176-07	176-25
1	2		176-10
1	3		176-09

Location Data (Contd)

The data is present at the following pins:

TPort	FA524 Inputs (INV Data, 2 V)	FA524 Output* (INV Data)
0	018	013 312
1	105	005 104
2	007	303 102
3	307	304 302
4	217	214 213
5	017	015 314
6	316	215 016
7	108	003 301

* First entry output to TCONTR 0, second to TCONTR 1.

FA1190, FB589, and FA546 [TTSI (TSI-1)]

L.O.D. Level From F-Level Trace	Horizontal EQL			Vertical EQL	
	FA1190	FB589	FA546	SPCO	SPC1
0	57	49	38	50	72
1	56	49	38	50	72
2	55	49	38	50	72
3	54	49	38	50	72
4	53	48	37	50	72
5	52	48	37	50	72
6	51	48	37	50	72
7	50	48	37	50	72

Notes:

1. Data present at FA1190 PINS 100, 300, and 203 with inverted polarity (See SD-4A024-01, -02, FS 20).
2. TSI bay is the same as TCONTR.

FA1784 and FA1785 (TSI-2)

L.O.D. Level From F-Level Trace	Horizontal EQL		Vertical EQLS			
	FA1784	FB1785	SPC0	SPC1	SPC2	SPC3
0	26	15	28	40	52	64
1	26	15	28	40	52	64
2	21	15	28	40	52	64
3	21	15	28	40	52	64
4	12	14	28	40	52	64
5	12	14	28	40	52	64
6	07	14	28	40	52	64
7	07	14	28	40	52	64

Notes:

1. Data present at FA1784 PIN 214 (even levels) and PIN 014 (odd levels) with inverted polarity (See SD-4A08401, FS 5).
2. TSI bay is the same as TCONTR.

Octal-Decimal Conversions

Table 4-A. Octal-Decimal Integer Conversion Table

OCT X=	0	1	2	3	4	5	6	7
000X	0000	0001	0002	0003	0004	0005	0006	0007
001X	0008	0009	0010	0011	0012	0013	0014	0015
002X	0016	0017	0018	0019	0020	0021	0022	0023
003X	0024	0025	0026	0027	0028	0029	0030	0031
004X	0032	0033	0034	0035	0036	0037	0038	0039
005X	0040	0041	0042	0043	0044	0045	0046	0047
006X	0048	0049	0050	0051	0052	0053	0054	0055
007X	0056	0057	0058	0059	0060	0061	0062	0063
010X	0064	0065	0066	0067	0068	0069	0070	0071
011X	0072	0073	0074	0075	0076	0077	0078	0079
012X	0080	0081	0082	0083	0084	0085	0086	0087
013X	0088	0089	0090	0091	0092	0093	0094	0095
014X	0096	0097	0098	0099	0100	0101	0102	0103
015X	0104	0105	0106	0107	0108	0109	0110	0111
016X	0112	0113	0114	0115	0116	0117	0118	0119
017X	0120	0121	0122	0123	0124	0125	0126	0127
020X	0128	0129	0130	0131	0132	0133	0134	0135
021X	0136	0137	0138	0139	0140	0141	0142	0143
022X	0144	0145	0146	0147	0148	0149	0150	0151
023X	0152	0153	0154	0155	0156	0157	0158	0159
024X	0160	0161	0162	0163	0164	0165	0166	0167
025X	0168	0169	0170	0171	0172	0173	0174	0175
026X	0176	0177	0178	0179	0180	0181	0182	0183
027X	0184	0185	0186	0187	0188	0189	0190	0191
030X	0192	0193	0194	0195	0196	0197	0198	0199
031X	0200	0201	0202	0203	0204	0205	0206	0207
032X	0208	0209	0210	0211	0212	0213	0214	0215
033X	0216	0217	0218	0219	0220	0221	0222	0223
034X	0224	0225	0226	0227	0228	0229	0230	0231
035X	0232	0233	0234	0235	0236	0237	0238	0239
036X	0240	0241	0242	0243	0244	0245	0246	0247
037X	0248	0249	0250	0251	0252	0253	0254	0255

DECIMAL

Table 4-A. Octal-Decimal Integer Conversion Table (Contd)

OCT X=	0	1	2	3	4	5	6	7
000X	0000	0001	0002	0003	0004	0005	0006	0007
041X	0264	0265	0266	0267	0268	0269	0270	0271
042X	0272	0273	0274	0275	0276	0277	0278	0279
043X	0280	0281	0282	0283	0284	0285	0286	0287
044X	0288	0289	0290	0291	0292	0293	0294	0295
045X	0296	0297	0298	0299	0300	0301	0302	0303
046X	0304	0305	0306	0307	0308	0309	0310	0311
047X	0312	0313	0314	0315	0316	0317	0318	0319
050X	0320	0321	0322	0323	0324	0325	0326	0327
051X	0328	0329	0330	0331	0332	0333	0334	0335
052X	0336	0337	0338	0339	0340	0341	0342	0343
053X	0344	0345	0346	0347	0348	0349	0350	0351
054X	0352	0353	0354	0355	0356	0357	0358	0359
055X	0360	0361	0362	0363	0364	0365	0366	0367
056X	0368	0369	0370	0371	0372	0373	0374	0375
057X	0376	0377	0378	0379	0380	0381	0382	0383
060X	0384	0385	0386	0387	0388	0389	0390	0391
061X	0392	0393	0394	0395	0396	0397	0398	0399
062X	0400	0401	0402	0403	0404	0405	0406	0407
063X	0408	0409	0410	0411	0412	0413	0414	0415
064X	0416	0417	0418	0419	0420	0421	0422	0423
065X	0424	0425	0426	0427	0428	0429	0430	0431
066X	0432	0433	0434	0435	0436	0437	0438	0439
067X	0440	0441	0442	0443	0444	0445	0446	0447
070X	0448	0449	0450	0451	0452	0453	0454	0455
071X	0456	0457	0458	0459	0460	0461	0462	0463
072X	0464	0465	0466	0467	0468	0469	0470	0471
073X	0472	0473	0474	0475	0476	0477	0478	0479
074X	0480	0481	0482	0483	0484	0485	0486	0487
075X	0488	0489	0490	0491	0492	0493	0494	0495
076X	0496	0497	0498	0499	0500	0501	0502	0503
077X	0504	0505	0506	0507	0508	0509	0510	0511

DECIMAL

ASCII/Teletypewriter/Hexadecimal Conversion Table

1st Hexadecimal Character

2nd Hexadecimal Character

HEX	Ø	1	2	3	4	5	6	7
Ø	NUL	DL	SPACE	Ø	@	P	`	p
1	SH	D1	!	1	A	Q	a	q
2	SX	D2	"	2	B	R	b	r
3	EX	D3	#	3	C	S	c	s
4	ET	D4	$	4	D	T	d	t
5	EQ	NK	%	5	E	U	e	u
6	AK	SY	&	6	F	V	f	v
7	🔔	EB	'	7	G	W	g	w
8	BS	CN	(	8	H	X	h	x
9	→	EM	)	9	I	Y	i	y
A	≡	SB	*	:	J	Z	j	z
B	VT	EC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	¦
D	←	GS	–	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	//

Peripheral Unit Bus (PUB)

Introduction

The PUB is the primary means of communication between the central controls (CCs) and the 4ESS switch peripheral frames. The PUB is duplicated (PUB0, PUB1) for reliability. Normally, one PUB is designated active, and the other is standby. The CCs are configured to send/receive on the PUBs according to the states of PUB0, PUBA, PUBT and PUBR (See Interrupt Data Layout Register—CSC Register).

Each PUB consists of twelve 8-pair cables or 96 twisted pair. Eight cables (64 pair) are used to send data to the peripheral frames and form the PUEA, PUWB and PUCB portions of the PUB. Four cables (32 pair) are used to receive data from the peripheral frames and form the PURB portion of the PUB. Each twisted pair acts as an ungrounded, balanced transmission line and is terminated in a 100 OHM bus terminating resistor (BTR).

The PUBs originate at the CC and are fanned-out into a maximum of 8 bus branch pair (for example, branches A/B, C/D, · · ·, O/P) via the peripheral bus branching frame (PUBB). The PUBB controls PUB power via the power control switches (PUB0, PUB1) and also provides a loop-around register for testing the PUB (see peripheral unit bus branching frame—Loop-around Mappings). Each bus branch is wired serially to all the peripheral frames connected on that branch and terminates in a BTR (100 ohm).

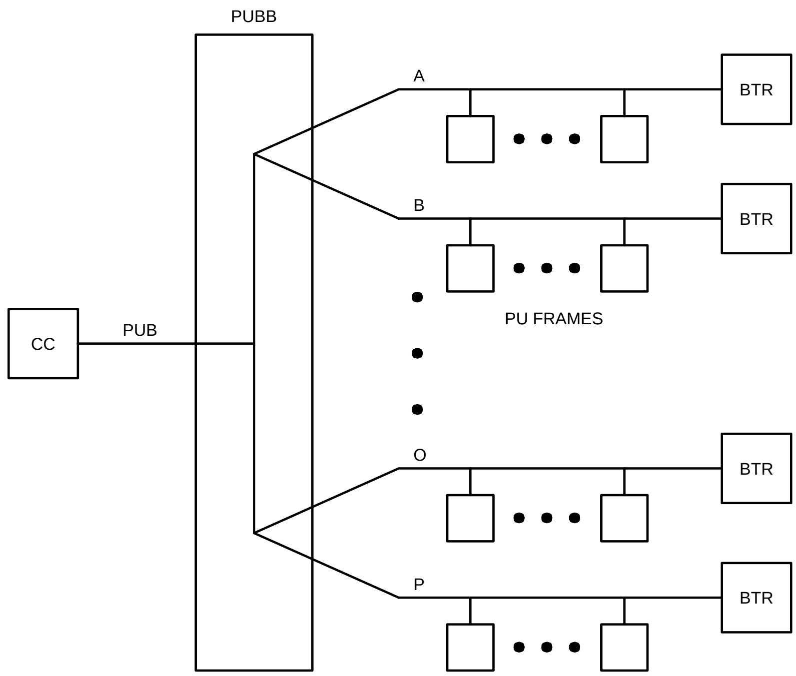
The peripheral frames connect to the PUB via cable drivers (PURB) and cable receivers (PUEA, PUWB, PUCB). The cable driver transformers are connected in parallel across each twisted pair and can be removed during circuit pack replacement with no disruption to the integrity of the bus. The cable receivers, on the other hand, use a serially connected balanced pickoff transformer (one coil in each side of the twisted pair) which, if removed, could open up the bus.

Introduction (Contd)

This is prevented by installing a permanent 4.99 ohm bypass resistor across each of the transformer coils. If the cable receiver circuit pack is removed, the bypass resistor maintains the integrity of the bus. Some bus problems can be traced to a missing or defective bypass resistor and shows up as a missing bit(s) on the PUB when a cable receiver circuit pack is removed.

See AT&T 234-110-010—*Peripheral Unit Bus System Description* for additional information.

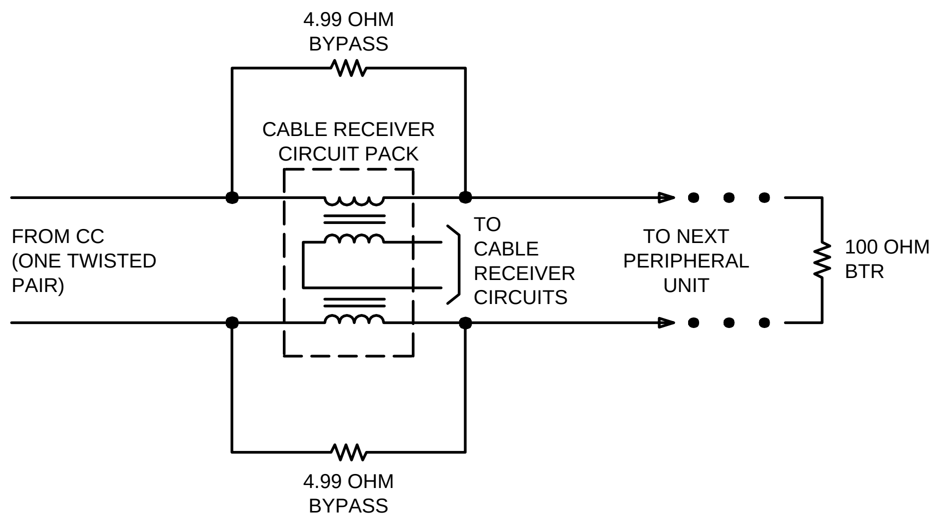
Fanout



Legend:

BTR = Bus Terminating Resistor
CC = Central Control
PU = Peripheral Unit
PUBB = Peripheral Unit Bus Branching

Bypass Resistors



Four Divisions of the Peripheral Unit Bus

The following are the four divisions of the PUB:

Bus	Acronym	Function	Size (Pairs)
Peripheral Unit Enable Address Bus	PUEA	Sending orders	16
Peripheral Unit Write Bus	PUWB	Sending orders	40
Peripheral Unit Reply Bus	PURB	Receiving replys	32
Peripheral Unit Control Bus	PUCB	Interrogating frames	8

A description of each bus follows.

Peripheral Unit Enable Address (PUEA) Bus Format

IOCL	IOCH	PUSYC	Mode	Unit ID	Member No.
15	14	13	12	11 7	6 0
				<----------------------K-Code ---------------------------> (E-Register)	

(See Interrupt Data Layouts for register descriptions)

Bit 0-11 = K-Code from E-register (See ‘‘K-Codes’’ in Volume 2)

0-6 = Member No. (Frame member number)

7-11 = Unit type identification

12 = Mode (0 = Operational order, 1 = Maintenance order) from CC PSC register Bit 8 (MTCPU)

13 = PUSYC — SYNC pulse for oscilloscope, sent .5 microsecond ahead of every peripheral order to all frames to clear their input register.

14 = IOCH — Input/output clock high pulse generated by 1B CC

15 = IOCL — Input/output clock low pulse generated by 1B CC

Peripheral Unit Write Bus (PUWB) Format

P2	P1	NC	DSYNC	OPCODE	Address Subfield	Instruction Data
39	38	37	36	35 29	28 24	23 0
				<-------MOPCODE--------> (PRM)		<---------Data---------> (PRL)
				<-----------------------P-Register----------------------->		

(See Interrupt Data Layouts for register descriptions)

Bit 0-35 = P-Register

0-23 = PRL (P-register least significant bits) — Data for PU frame

24-35 = PRM (P-register most significant bits) — MOPCODE (Modified OPCODE) contains OPCODE (29-35) and address subfield/supplementary OPCODE (24-28)

36 = DSYNC (Diagnostic SYNC pulse)

37 = No connect (Not presently used)

38 = P1 — Parity bit over odd bits of E and P-registers (odd parity)

39 = P2 — Parity bit over even bits of E and P-registers (odd parity)

Peripheral Unit Reply Bus (PURB) Format

NC	NC	NC	APUB	APUT	APUF	PAR	ASW	Reply Data	
31	30	29	28	27	26	25	24	23	0
			<---- Response ----> TO CLKI						

(See Interrupt Data Layouts for register descriptions)

Bit 0-23 = Reply data from frame in response to a peripheral order. Destination is the CC L-register. If the reply data is not identical on both PUBs, the CCs mismatch causing an F-level interrupt (PUF) (RMEGCP, RMEPU — see CC PES-register bits 16 and 17)

24 = ASW—All seems well from frame if order is successful. Otherwise, the frame inhibits ASW and causes an F-level interrupt (PUF) (ASWEPU — See CC PES-register bit 6 and CC INS-register bit 5)

25 = PAR—Answer parity (odd parity) over reply data bits 0-23. IF CC receives bad parity it generates an F-level interrupt (PUF) (APEPU, AP0PU, AP1PU — See CC PES-register bits 2, 3, 7 and CC INS-register bit 5)

26 = APUF—Autonomous peripheral unit failure. Response to CLKI interrogate pulse on PUCB. Causes an F-level interrupt (APUF) (See CC INS-register bit 4)

27 = APUT—Autonomous peripheral unit trouble. Response to CLKI interrogate pulse on PUCB. Causes an interject (APUT — See CC PES-register bit 9 and APINJ — See CC INJ-register bit 13)

28 = APUB — Autonomous peripheral unit base (not presently used) (APUB — See CC PES-register bit 8)

29-31 = No connect (not presently used)

Peripheral Unit Control Bus (PUCB) Format

PIO	PDG	PSZ	PLP	PHP	CLKI	GI	MI
7	6	5	4	3	2	1	0

<----------- Interrogation Control Group ----------->

(Bits generate reply data on PURB)

Bit 0 = MI—Member interrogate pulse. Frames with errors respond with a member no. Bit on the PURB (See MI/GI responses).

1 = GI—Group interrogate pulse. Frames with errors respond with a group number on the PURB (See MI/GI responses).

2 = CLKI—Clock interrogate pulse. Frames with errors respond with APUF, APUT, or APUB bit on the PURB. These bits cause F-level, interject, or base level interrupts, respectively. CC sends the clock I pulse every 16 cycles.

3 = PHP—Poll high priority buffer (DIF/SP 0-23). All frames respond with 0 = buffer not empty or 1 = buffer empty.

4 = PLP—Poll low priority buffer (DIF/SP 0-23). All frames respond with 0 = buffer not empty or 1 = buffer empty.

5 = PSZ—Poll seizure buffer (DIF/SP 0-23). All frames respond with 0 = buffer not empty or 1 = buffer empty.

6 = PDG—Poll digit buffer (DIF/SP 0-23). All frames respond with 0 = buffer not empty or 1 = buffer empty.

7 = PIO—Poll IO frames.

NOTE:
DIF/SP 24-31 and SCS 0-7 use 4 special GCP interrogation pulses (PDG´ PSZ´ PUP´ PHP´) for polling the buffers. These frames are isolated on a special branch of the PUB.

Peripheral Unit Bus Branching Frame (PUBB) Loop-Around Mappings

Bit	MAPPING 1: FROM CC TO LOOP-AROUND REGISTER	MAPPING 1: DATA RETURNED TO CC (PURB)	MAPPING 2: FROM CC TO LOOP-AROUND REGISTER	MAPPING 2: DATA RETURNED TO CC (PURB)	MAPPING 3: FROM CC TO LOOP-AROUND REGISTER	MAPPING 3: DATA RETURNED TO CC (PURB)
APUB						PSZ
APUT						PLP
APUF						CLKI
PAR						GI
ASW						MI
23	PUW23	PUW23	EA11	EA11	PDG*	PDG
22	PUW22	PUW22	EA10	EA10	PSZ*	PSZ
21	PUW21	PUW21	EA09	EA09	PLP*	PLP
20	PUW20	PUW20	EA08	EA08	PHP*	PHP
19	PUW19	PUW19	EA07	EA07	PIO	PIO
18	PUW18	PUW18	EA06	EA06		
17	PUW17	PUW17	EA05	EA05		
16	PUW16	PUW16	EA04	EA04		
15	PUW15	PUW15	EA03	EA03	EA15	EA15
14	PUW14	PUW14	EA02	EA02	EA14	EA14
13	PUW13	PUW13	EA01	EA01	EA13	EA13
12	PUW12	PUW12	EA00	EA00	EA12	EA12
11	PUW11	PUW11	PUW35	PUW35	CLKI	CLKI
10	PUW10	PUW10	PUW34	PUW34	GI	GI
9	PUW09	PUW09	PUW33	PUW33	MI	MI
8	PUW08	PUW08	PUW32	PUW32		
7	PUW07	PUW07	PUW31	PUW31		
6	PUW06	PUW06	PUW30	PUW30		
5	PUW05	PUW05	PUW29	PUW29		
4	PUW04	PUW04	PUW28	PUW28		
3	PUW03	PUW03	PUW27	PUW27	PUW39	PUW39
2	PUW02	PUW02	PUW26	PUW26	PUW38	PUW38
1	PUW01	PUW01	PUW25	PUW25	PUW37	PUW37
0	PUW00	PUW00	PUW24	PUW24	PUW36	PUW36

Refer to Notes 1 and 2.

Peripheral Unit BUS Branching Frame (PUBB) Loop-Around Mappings (Contd)

NOTE 1:
PUB Data is sent from the CC via the PUEA, PUWB, PUCB and is intercepted by the loop around register, as shown. The loop around register sends the PUB data back to the CC via the PURB.

NOTE 2:
PUW__ Symbols represent bits sent on PUWB
EA__ Symbols represent bits sent on PUEA
The remaining bits are sent on the PUCB.

* For expanded polling branch(es), only the original PDG, PSZ, PLP, PHP bits are looped and checked by the PUB diagnostic. The new expanded PDG′, PSZ′, PLP′, PHP′ bits are not looped and must rely on the DIFE1 (24-31) and SCS (0-7) diagnostics for integrity check.

Schematic Diagram List

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Schematic Diagram List

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Processor Equipment Schematic Diagrams

NOTE 1:
An "F" following a schematic diagram number indicates a unit interconnection drawing.

NOTE 2:
Appropriate dash numbers which correspond with local equipment must be utilized.

1B Cabinet

4A145	1B Processor Frame Circuit
4A146	Bus Driver/Receiver Unit Circuit
4A147	Interface Bus Unit Circuit
4A148	Central Control and Store Unit Circuit
4A149	Call Store Unit Circuit
4A150	Fuse and Interframe Communication Circuit
4A180	Filter Unit Circuit

Attached Processor Interface (API)

5A056(F)	API Frame
5A055	API Unit Circuit
5A024	Data Unit Selector Circuit

Input/Output (I/O)

5A021(F)	I/O Unit
5A023	I/O Peripheral Bus Circuit
5A049	Microprocessor Community Circuit
5A052(F)	I/O Processor Frame Circuit
4C049	I/O Processor Growth Unit Circuit

Tape Frame

5A025(F)	Tape Unit Controller

4ESS Switch Equipment Schematic Diagrams

Common Channel Interoffice Signaling (CCIS)

4A054(F)	Terminal Basic Frame Circuit
4A055(F)	Terminal Supplementary Frame Circuit
4A056	Peripheral Bus Interface Circuit
4A057	Terminal Access Circuit
4A058	Terminal Basic Power Control Circuit
4A059	Terminal Power Control Circuit (SUPP Frame)
4A064	Continuity Check Transceiver Circuit
4A098	Amplifier and Pad Circuit
94833	Common Channel Interoffice Signaling (CCIS) Terminal
73090	Data Set 201D
94872	CCIS Terminal Modem Interface Circuit
94874(F)	Data Set Frame Circuit
1D295	Data Set Mounting Unit
1D301	Data Set 2048A

Common Channel Signaling System 7 (CCS7)

3F006	Digital Facility Access Frame Circuit
3F007	Ring Node Frame Circuit
3F008	3B Interface Unit Circuit
3F009	Link Node Unit A Circuit
3F010	Link Node Unit B Circuit
3F019	Application Schematic
3F022	Fuse Panel and Alarm Control Unit
3F028	Digital Facility Access (DFA) Frame
3F029	Digital Facility Access Unit
3F037	Ring Node Circuit
3F038	DS1 Unit A
3F039	DS1 Unit B
3F048	High Density Integrated Ring Node (IRN) Unit
94874	Data Frame Circuit

Digital Interface Frame (DIF)

5G208	Digital Interface Circuit

Digital Interface Frame-Export 1 (DIF-E1)

5X400	Digital Interface Circuit-Export 1

Digroup Terminal (DT)

6G114	Digroup Terminal

Expanded Time-Slot Interexchange (XTSI)

4A080	4ESS Scan and Distribution Point Rules
4A196	XTSI Cabinet
4A197	XTSI Fuse and Fan Unit
4A198	XTSI Control (XTC) Unit
4A199	XTSI Fabric (XTF) Unit
4A209	XTSI Fan Unit Schematic

Echo Suppressor Terminal (EST)

5G168	Echo Suppressor Terminal Circuit
5G169	Echo Suppressor Terminal Circuit Pack INFO

Network Clock (NCLK)

4A014(F)	NCLK Frame Circuit
4A036	NCLK Unit Circuit
4A037	System Clock and Bus Controller Circuit
4A105	NCLK Synchronization Circuit

Network Management (NM)

4A073	Display Console Circuit
4A074	Display Wall Unit
4A075	Remote and Distributor Circuit
4A076	Dynamic Overload Control Transmitter Circuit
4A077(F)	Display Frame
4A079(F)	Display Frame Circuit
4A082	43A1 Carrier Telegraph IF Circuit

Peripheral Unit Bus Branching (PUBB)

4A019(F)	Peripheral Unit Bus Branching Circuit
4A038	Bus Branching and Loop-Around Circuit
4A091	PUBB Access Circuit

Remote Measurement System-Digital 2 (RMS-D2)

1P212	Remote Measurement System—Digital 2

Remote Office Test Line (ROTL)

4A021(F)	ROTL Frame Circuit
4A061	ROTL Unit Circuit
4A062	Test Line Circuit

Service Circuit System (SCS)

4A170	SCS Applications Schematics

Signal Processor 1 (SP1)

4A013	Control Circuit
4A018	Control Circuit
4A028(F)	Control Frame Circuit
4A046(F)	Distributor and Scanner Matrix Frame
4A047(F)	Distributor Applique Frame
4A048	Scanner Matrix
4A049	Distributor Matrix
4A050	Distributor Applique Relay Point Circuit
4A051	Scanner Access
4A052	Distributor Access
4A063	Distributor Applique Pulse Point Circuit
4A093	Distributor and Scan Matrix Frame Circuit
4A094	Distributor and Scan Matrix Access Circuit
4A095	Distributor and Scan Matrix Point Circuit

Signal Processor 2 (SP2)

4A063	Distributor Applique Pulse Point Circuit
4A065(F)	Control Frame
4A066	Peripheral Bus Access Circuit
4A067	Control Circuit
4A068(F)	Supplementary Matrix Frame Circuit
4A069	Supplementary Matrix Access Circuit

Time Multiplex Switch (TMS)

4A012(F)	TMS-A Frame Circuit
4A026	Controller and Bus Interface Circuit
4A027	Switch Unit Circuit
4A087(F)	TMS-B Frame Circuit
4A088	Controller and Bus Interface Circuit
4A089	Switch Unit Circuit
4A090	Peripheral Bus Access Circuit

Time Slot Interchange (TSI)

4A011(F)	TSI Frame Circuit
4A022	Peripheral Bus Interface Circuit
4A023	Timing and Control Circuit
4A024	7 X 8 Switching and Permuting Circuit
4A083(F)	TSI-2 Frame Circuit
4A084	7 X 8 Switching and Permuting Circuit (TSI-2)
4A085	TSI-2 Controller

Voiceband Interface Frame (VIF)

5G156(F)	Voiceband Interface Frame
5G157(F)	Voiceband Interface Unit
5G158(F)	Voiceband Interface Circuit
5G159	Voiceband Interface Unit Control Point Switches (CPS)
5G160	Voiceband Interface Controller and Miscellaneous Frame CPSs

Miscellaneous Circuit (Numerical Order)

4A001	Key Sheet
4A002-02	Current Drain Data
4A004	Circuit Pack Information
4A007	Interframe Communication Circuit
4A008	DC Power Distribution Circuit
4A009	AC Power Distribution Circuit (MISC A Frame)
4A010	Office Alarm Grid Circuit (MISC A/B Frame)
4A016	I/O Terminals Connections Circuit
4A025(F)	Miscellaneous Frame Circuit A
4A062	105 Test Line
4A078(F)	Miscellaneous Frame Circuit B
4A080	Assignment Rules for SP Frames
4A109(F)	Miscellaneous Frame Circuit C

Miscellaneous Equipment Schematic Diagrams

Drawing Number	Part of	Drawing Title
1C585		71J Access Panel
1P105		CMS 1B AND 1C
1P015	51A	Key Set Circuit
1P016	51A	Key Set Register and MF Generator Control Circuit
1P017	51A	Communication and Alarm Circuit
1P019	51A	Test Equipment Access Circuit
1P020	51A	Test Access Trunk Circuit
1P021	51A	2600-HZ Supply Circuit
1P022	51A	Transmission Measuring SYS Circuit
6G048	51A	58C Loop-Around Unit
81975	820A	Inverter Circuit
82156	820A	Circuit Pack Schematics
82157(F)	820A	Ring and Tone Frame
94800		Tone Detector
95277-02		Milliwatt Tone Gen. and Panel
96613		Precision Amplifier Circuit
97723	RA	Drum Storage Unit Circuit
97724	RA	Circuit Pack Schematic
97725(F)	RA	Recorded Announcement Circuit
NS-00291	PAS	Phased Announcement System
1C155		Multifrequency (MF) Signaling Test Circuit
1C378		Carot
1C453(F)		Metallic Trunk Frame

Miscellaneous Equipment Schematic Diagrams (Contd)

Drawing Number	Part of	Drawing Title
1C476		Circuit Maintenance System (CMS) Interface Register Bank Circuit
1C488		MF Transmitter
1C489		Common Tone Supply Circuit
1C490		MF Receiver
7C013(F)		Direct Formed Supergroup Frame W/F Signaling
1C498(F)		MF Frame
7C015(F)		Direct Formed Supergroup Frame W/O F Signaling
99480		D3 Channel Bank
3C304		D4 Channel Bank
99552		A-6 Unitized Terminal Equipment (UTE)
82047		–48 V BDFB
82097	620A	Converter Circuit
82098	620A	Discharge Circuit
82106		DC-DC Converter
82107	620A	Converter Control Circuit
82188-01		+140 V Area Bus Center
82194-01		DC Power DIST Circuit
82348-01	526A	Power Plant - Application Schematic Diagram
82349-01	526A	Inverter Circuit
51893	LT-1	LT-1 Connector Digital Access Unit

Teletype Messages

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Teletype Messages

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Common Channel Interoffice Signaling Messages

ALW:TGR a,TER c!
DGN:TGR a,TER c!
EX:TGR a,TER c;START!
RMV:TGR a,TER c!
RST:TGR a,TER c!
SW:TGR a!
DUMP:TGR a,TER c,CREG!
DUMP:TGR a,IREG!
DUMP:TGR a,TER c,MEM d-e!

d-e = First address minus last address

Common Channel Interoffice Signaling Messages (Contd)

CFR:SIGLK a,VFL b!
OP:SVCSSTAT!
RMV:SIGLK a!
RST:SIGLK a!
TEST:SIGLK a,VFL b!
OP:SLKSTAT a!
MON:SUTRAP; { Send | Receive | Send,Receive }:
{SIGLK[,Illegal] | CIN } ! (CCITT6 Only)
STOP:MON;SUTRAP;{ Send | Receive | Send,Receive }:
{SIGLK[,ILLEGAL] | CIN }! (CCITT6 Only)
OP: SLCSTAT; SLC a! (CCITT6 compliment SLC)
OP: BANDSTAT; SIGLK a!
TEST:TRK,TSN a;TIC!

STOP: MON; SUTRAP!

Circuit Identification Number Information

VER:TSG:CIN OATM* RTOT *****_aaa_!**

BTFN MC SC

This example specifies the circuit identification number (CIN) for a nonmessage trunk subgroup that is to be verified. Asterisks are used where no information is necessary. The CIN is made up of the following components:

BTFN = Base traffic number—The BTFN is equal to zero for all nonmessage trunk subgroups.

MC = Major category—This field is used to define the major category of a nonmessage trunk. (See CIN keywords.)

SC = Subcategory—This field is used to further define the function of the nonmessage trunk. (See CIN keywords.)

aaa = Local alphanumeric office code

Circuit Identification Number Keywords

Nonmessage Trunk Subgroup

ATM*—Automatic Trunk Measuring

RT0T	=	Remote office test line (ROTL) Port 0 test trunk
RT1T	=	ROTL Port 1 test trunk
RT0A	=	ROTL Port 0 access circuit
RT1A	=	ROTL Port 1 access circuit
RPCS	=	ROTL Port access circuit secure
RPCU	=	ROTL Port access circuit unsecure

CLN*—Code Line Test Circuit

TAT*	=	51A Testboard, test access trunk
105*	=	The 105 code is associated with the ATMS responder.
108T	=	108 Test trunk for echo suppressor test
108A	=	108 Access trunk for echo suppressor test
TND*	=	Tone detector test circuit

MIS*—Miscellaneous

CKEY	=	Centralized automatic message accounting (CAMA) keying
CTLK	=	CAMA talking
CCWS	=	CAMA call waiting/suspension
TERM	=	CCIS terminal
OBS0	=	Service observing trunk A (Circuit 0) connects to the outgoing trunk
OBS1	=	Service observing trunk B (Circuit 1) connects to the outgoing trunk

SVC*—Service Circuit

MFR*	=	Multifrequency receiver
MFX*	=	Multifrequency transmitter
XCVR	=	CCIS transceiver
XCVT	=	CCIS transceiver test circuit
MFRT	=	Multifrequency receiver test circuit
MFXT	=	Multifrequency transmitter test circuit

TAS*—Tone and Announcement Circuits

ANN*	=	Recorded announcement circuit
TONE	=	Tone circuit
MWAT	=	Milliwatt test is a 1000-HZ tone at one milliwatt power level.

Error Analysis Program

Sort—Frame Type or Specific Frame

IN:ERAPCOND SP:DATA1 RCNTHIST,ITEM1 DUTYP,EQ,VALUE 002!

Frame Type	Value
DT	014
EST	007
NC	003
PUBB	160
SC	015
SP	002
TGR	006
TMSP	004
TSI	005
VIF	013
DIF	010

Messages

ALW:ERAP *a*!

a = Function to be allowed

AUD:ERAPDATA *a*!

a = Function to be audited

CLR:ERAPCOND *a*!
CLR:ERAPCOND *a*;UCL!
CLR:ERAPDATA *a*:MFNUM *b*!
CLR:ERAPSRES *a*!
CLR:*a*;UCL!
IN:ERAPCOND *a*:DATA1 *b*,ITEM *c*,GE,VALUE *d*!
IN:ERAPDATA REPAIREC:*a*,MFNUM *c*,TRNUM *d*!
INH:ERAP *a*!
OP:ERAPCOND *a*!
OP:ERAPCOND;SUM!
OP:ERAPDATA *a*:ITEM *d*:MFNUM *b*!
OP:ERAPDATA *a*:ITEM *d*:SRES *c*!
OP:ERAPDATA *a*:MFNUM *b*!
OP:ERAPDATA *a*:SRES *c*!
OP:ERAPDATA *a*:WORD *e*:MFNUM *b*!
OP:ERAPDATA *a*:WORD *e*:SRES *c*!
OP:ERAPDATA:MRNUM *a*!
OP:ERAPSRES *a*!
OP:ERAPSRES;SUM!
OP:ERAPSUM!
OP:ERAPSUM;DETL:MFNUM *a*,FILEDATE *b*!
STOP:OP;ERAP!
UPD:ERAP FSDATA!

Copy Generic 1600 BPI and 4MM on APS (Does Not Include Tape-Only Program)

If normal file is to be copied—

AUD:NUM (43,44,45,66,72)!
COPY:UPDATE:GEN *a*,MT *b*!

If update file is to be copied—

VER:APPFILE UPD!
COPY:UPDATE: GEN *a*,MT *b*!

a = NORM (Write from normal file)
or
UPD (Write from update file)

b = Tape unit number (0 or 1)

Library Programs

Package	Program	Description
LGaaFLDS	TGAP	Trunk Group Assignment Program
	LIB1	Field Support Library Program 1
LGaaNETX	NETX	Network Exercise Library Program
LGaaPGRO	XAPP	1B Processor Translation Alteration and Print Program
LGaaPKG1	ERLI	Error Analysis Library Program
LGaaTMSG	TMSG	Time-Multiplexed Switching Growth Program

aa = Generic Number

Example messages:

LOAD:LIBSYS, FS;TAPE:PKG LG25PKG1!
EX:LIBSYS:PKG LG25PKG1, PGM ERLI, TASK 0, CLIENT 0!
IN:LIBSYS:CLIENT 0, WORD 0, BCD (01 2380,000000,012480,240000)!
IN:LIBSYS:CLIENT 0, OCT (0,0,0)!

Load Library Tape

Write Library Tape

COPY:UPDATE: LIB NORM, MT a!

Load Library Tape From Tape

OP:LIBSTAT,FS!
LOAD:LIBSYS,FS;TAPE:TD a!

Load Library Tape From Backup Tape

VER:UPDATE:TAPE,MT a!
AUD:LIBSYS,TD a;UCL!

Loop Messages

EX:SP 0, CONTR 1;START:PUB 1!
EX:SP 0:SYNC 1435,ENABLE 250!
EX:SP 0:PH 17,ADR 1420-1437!

Stop the loop
EX:SP 0!

Multifrequency Test

Receiver Test

TEST:TRK,CIN *bbcc*SVC*MFR*****ddd*;SVC:TSG,STAT
MTC.DSA<AUT>,PALL!

bb = 0 TO 23, DIF Member number

cc = 0 TO 63, DIF MF Receiver number

ddd = Local alphanumeric office code

Transmitter Test

TEST:TRK,CIN *bbcc*SVC*MFX*****ddd*;TSG,STAT
MTC.DSA<AUT>,PALL!

bb = 0 TO 23, DIF member number

cc = 0 TO 63, DIF MF transmitter number

ddd = Local alphanumeric office code

Maintenance Operating Center Messages

ALW:FC *a*!
ALW:FLEV (APUFS PUFS)! INH:
ALW:AUD:NUM 43,66! INH:
ALW:INFCRCD! INH:
ALW:MACLI,CLASS MTCE!
ALW:MUPAUD,MUP*a*;BANK *b*,[NUM {*c*|(*c*,*c*[,*c*...])}]!
ALW:DGRPT!
ALW:NCATANOM,TRAPN *a*!
ALW:RINGOVLD!
ALW:UPAD!
CLR:ADSFUNC SRM!
CLR:MACLI,CLASS *a*!
CLR:MSGRCD,FS!
COPY:OWBUF!
DGN:CC *a*;RPT 5,RAW,UCL:PH 1-21,TLP!
DUMP:PSS,ADR 14601416,L 24!
DUMP:MUP,ACT,ADR *a*[,SIZE *b*,DISP *c*][,L *d*]!
IN:OWBUF:ADR *a*,DATA *b*!
INH:MACLI,CLASS MTCE; REX ALL!
INH:DGRPT!
INH:FC *a*!
INH:NCATANOM,TRAPN *a*!
INH:RINGOVLD!
INH:UPAD!
INIT:ALM!
LOAD:MUP,ACT,ADR *a*[,SIZE *b*,DISP *c*][,L *d*]:*e*!
MON:CHAN *a*(;CHAN *b*)!
OP:ALMSTAT!
OP:CLK!
OP:CSSTATUS!
OP:DUSTATUS!

Maintenance Operating Center Messages (Contd)

OP:ERAPDATA:MRNUM *a*!
OP:ERAPDATA [*b*]:{MFNUM *c* | SRES *d* }!
OP:ERAPDATA *b*;{ITEM *e* | WORD *f* }:{MFNUM *c* | SRES *d*}!
OP:INHINT!
OP:FERAHIST,ALL!
OP:FERAHIST,SCLK*a*,NCSU*b*!
OP:MACLI,CLASS MTCE,SUBCLASS 0!
OP:MSGRCD,FS!
OP:MUPAUD!
OP:MUPSTAT!
OP:NCATANOM,TRAPN *a*!
OP:PERIFINH!
OP:PHSEHST,CORE!
OP:PHSEHST,FS!
OP:PSSTATUS!
OP:RINGMNTR!
OP:TERAWTSG!
OP:TLPQUEUE;ALL!
OP:TONESTAT,BT60 1!
OP:UTILMTCH!
OP:XPWRSTAT!
ORD:TBITS;READ:CIN *a*!
RMV:CC 0!
RMV:CS *a*!
RMV:CSB *a*!
RMV:CS,MCODE *a*;FREEZE!
RMV:CS,MCODE *a*;FREEZE;OC,PH *b*!
RMV:PS *a*!
RMV:PSS,MCODE *a*;FREEZE!
RMV:PSS,MCODE *a*;FREEZE;OC,PH *b*!
RMV:PSB *a*!

Maintenance Operating Center Messages (Contd)

RMV:SSD *a*!
RST:CC 0(;UCL)!
RST:CS *a*[{;UCL | :TLP}]!
RST:CSB *a*[{;UCL | :TLP}]!
RST:MUP *a*[{;UCL | :TLP}]!
RST:PSB *a*[{;UCL | :TLP}]!
RST:RA *a*!
RST:SSD *a*[{;UCL | :TLP}]!
RST:TONE!
RST:XPWR *a*[;UCL | :TLP]!
RTE:CHAN *a*(;CHAN *b*)!
RTR:ALM!
SET:AUD:MAN!
SET:AUD:NORM!
SET:CLK:DAY MON,DATE 033176,TIME 105059!
SET:CS *a*;{NORM | MCODE *b*}[;UCL]!
SET:PS *a*;{NORM | MCODE *b*}[;UCL]!
SET:TUC *a*;FUNCTION *b*!
STOP:MUPAUD!
SW:CC!
SW:CC;UCL!
SW:MUP[;UCL]!
TEST:CC *a*[;RPT][TSTNO *b*]!
TEST:FC *a*!
TEST:MUPAUD,MUP *a*;BANK *b*,[NUM {*c* | (*c*,*c*[,*c*...])}]!
TEST:SSD *a*!

Maintenance Operating Center Messages (Contd)

STOP:AUD;GEN!
STOP:MACLI,CLASS MTCE,SUBCLASS 0!
STOP:MON;CHAN *a*(;CHAN *b*!)
STOP:MSG!
STOP:OP;ERAP!
STOP:OP;MSGRCD,FS!
STOP:OP;TRKSTAT!
STOP:OP;TSGSTAT!
STOP:OVRWRT!
STOP:SET;TRKSTAT!
STOP:TEST;COREUPD!
STOP:TEST;PUSYS!
STOP:TEST;TRK!
STOP:UPD;CORE!
STOP:VERMSG!
SW:CC(;UCL)!
SW:DT *a*!
SW:PUB!
SW:SCLK *a*(;UCL)!
SW:SP *a*(;UCL)!
SW:VIF *a*(;VIU *b*)(;UCL)!
TEST:PUB *a*!
TEST:SYSPRFTO!
UPD:HDATA! (MTC ONLY)
VER:TRKNAME,CIN *c*;DETL!

Network Management (NWM)

Copy Network Management (1600 BPI and 4MM) on Attached Processor System

Copy:Update:NWM *a*,MT *b*!

a = NORM (Write from normal file)
or
UPD (Write from update file)

b = Tape unit number

Office Data Assembly

Copy Office Data Assembler (1600 BPI and 4MM) on Attached Processor System

COPY:UPDATE:ODA *a*,MT *b*!

a = NORM (Write from normal file)
or
UPD (Write from update file)

b = Tape unit number

On-Site Operational Report

Backup Tape—Re-enter on Attached Processor System

LOAD:APPTAPE:LTS, MT *a*! (Re-enters all blocks)

a = Tape unit number

LOAD:APPTAPE:ODIL, MT *a*!
(Re-enters 50 blocks)

a = Tape unit number

(This command restores office-dependent initial lists, 50 blocks [86-135])

Backup Tape—Write on Attached Processor System

COPY:APPTAPE:LTS, MT *a*!

a = Tape unit number

Peripheral Maintenance Operating System Messages (PMOS)

OP: PMOS; TCB! (Current PMOS executing tasks)
OP: PMOS; TRC! (PMOS Timed routine tasks)
OP: PMOS; CHAIN! (Current executing task & linkages)
INIT: PMOS, TCRTNUM *a*; ACTIVATE!
INIT: PMOS, TCRTNUM *a*; DEACT!

a = Timed routine task to be run or aborted

CAUTION:
Stops all PMOS tasks, and may cause system to hang up.

INIT:PMOS; ALL!
INIT:PMOS; UTIL, LVSAUD!
INIT:PMOS; UTIL, LVSAUD: DEPTH *b*!
INIT:PMOS; UTIL, LVSAUD: TASKID *c*!
INIT:PMOS; UTIL, LVSAUD: DEPTH *b*, TASKID *c*!

b = LVS Depth percentage
c = Specified task

INIT:PMOS; UTIL, FRMROUT!
INIT:PMOS; UTIL, END!

Recent Change Messages

OP:RCFORM *a*!	Used to call up one of the recent change data (RCDM) forms. Forms are referenced by 3 digits. Where a = 100 series TSG = 200 series TRK = 300 series Code = 400 series CAMA = 500 series RDB = 600 series MISC = 700 series Unit Type = 800 series Special
OP:RCBMSG,ORNU *c*!	Prints a copy of a buffered message identified by an order number *a*: Where *a* = 1 to 999999
OP:RCBORNU!	Lists all order numbers in the recent change buffer area
OP:RCBSPACE!	Prints the available buffer space
OP:RCRORNU,ALL! OP:RCRORNU,LAST *a*!	Lists the order numbers in the rollback area in reverse chronological order: Where *a* = A decimal number or the word tape
RCCNL:RCBORNU *a*!	Cancels a previously buffered MSG: Where *a* = 1 to 999999

Recent Change Messages (Contd)

RCCNL:ROLLBACK;UCL!	Rolls back the last entered recent change order number to its previous state.
RCTST:ORNU *a*!	Performs defensive tests on the RCDM: Where *a* = 1 to 999999
RCACT:ORNU *a*!	Activates a previously entered recent change: Where *a* = 1 to 999999
CLR:RCB!	Causes all messages on the recent change disk buffer to be cleared.
CLR:CHAN!	Clears any and all forms or MSGs from the channel on which it is input.
VER:ABSOLUTE	Verifies messages that have many Variables. See input manual for exact format.
VER:CAMASCRN VER:CODEGRP VER:CODELIST VER:RDB VER:RDBLIST VER:TRK VER:TRKNAME VER:TSG VER:TSGLIST VER:TTTE VER:UTYPE VER:MSG	

Trunk Maintenance Messages

INIT:TPDT!
MON:IAOFC,NEW:IA *b*,TIMEON *c*,TIMEOFF,RPT!
OP:DGSTAT,DT 1,DTU 0,DG 0,NUM 999,STAT SLH!
OP:DGSTAT,DT 1,DTU 0,DG 0,NUM 999,STAT SLL!
OP:TPMAP!
OP:TRKSTAT,ALL:STAT MTC.DSA <NIU>!
OP:TRKSTAT,CIN *a*!
OP:TSGSTAT,SUM:ALL!
ORD:ALTIDMWF,OPR:CIN *a*!
ORD:ALTIVU;RLS:CIN *a*!
ORD:DLOOP;OPR,DURATION *a*:CIN *b*!
ORD:MWTF;OPR:CIN *a*!
ORD:MW;OPR,DURATION *a*:CIN *b*!
RTE:C101;TPAT *a*, TP *b*!
RTE:TP *a*;TP *b*!
SCHED:TRK TEST:TIMEON 2000,TIMEOFF 0600!
SET:CONN *a*;TP*b*:CIN *e*,MODE 9(DNBR *h*)!
SET:DCON *a*; CIN *b*, MODE *c* (DNBR d)!
SET:DCON *a*; RLS!
SET:TP *a*; ON!
SET:TRKSTAT *a*,ALL;SUM (:STAT *h*)!
SET:TSGATC,CIN OSVC*MFR*****ddd*:NORM!
    ddd = Office code
SET:TSGEAC,CIN OSVC*MFR*****ddd*:NORM!
TRC:TRK,CIN *c*;HLD!
TRC:TRK,CIN *c*;RLS!
TRC:TRK,CIN *c*;TRC!

Tone Detector Circuit Test

RESTORE RT

RST:TONE,TPT *a*!
RST:TONE, AR *a*!
RST:TONE,BT60 *a*!
RST:TONE,BT120 *a*!

a = 0 or 1

RESTORE RA

RST:RA *a*,RACHAN *b*!

a = 0 or 1
b = 0 through 5

or

RST:RA *a*, ALL!

Output RA Status

OP:RASTAT *a*!

a = 0 or 1

Test Automatic Tone Detector

TEST:TRK,CIN *aaa* CLN*TDN*****ddd*;SVC:TSG,STAT MTC,PALL!

aaa = 0 through 3
ddd = Local alphanumeric office code

Trunk Out-of-Service List (TOSL)

Backup Tape—Re-enter on Attached Processor System

LOAD:APPTAPE:TOSL, MT *a*!

a = Tape unit number

Backup Tape—Write on Attached Processor System

COPY:APPTAPE:TOSL, MT *a*!

a = Tape unit number

Error Analysis Procedure

Backup Tape—Re-enter

LOAD:APPTAPE:ERAP,MT *a*!

a = Tape unit number

Backup Tape—Write

COPY:APPTAPE:ERAP,MT *a*!

a = Tape unit number

Load Trouble Locating Procedure from Tape

VER:UPDATE:TAPE,MT a!
LOAD:TLP;GEN "a";MT b! (4AP17 or earlier)
LOAD:TLP:GEN "a",MT b! (4AP18 or later

Traffic and Plant Measurements (1600 BPI and 4MM)

COPY:UPDATE:TPM NORM,MT a!

4ESS™ Switch System Recovery Procedures

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System Recovery Procedures

Introduction

Purpose

These are procedures to restore 4ESS™ Switch service when a MAJOR service affecting incident has occurred. These procedures do not guarantee service restoral because many hardware and software failures can occur that can not be resolved by following these procedures. However, if these procedures are followed, service has a high probability of being restored.

WARNING:
*These procedures **should not** be used to replace the normal escalation maintenance procedures. These procedures are intended to be used only if assistance from higher levels of technical support can not be obtained quickly.*

The 4ESS Switch System Recovery Procedures should be reviewed at least once every six months by all 4ESS Switch maintenance personnel. Many of the recovery procedures, along with additional maintenance procedures, are provided in more detail in Task Oriented Practice (TOP) 234-351-002 — 4ESS Switch With 1B Processor System Maintenance Operations Center. These procedures should be reviewed periodically by all maintenance personnel to familiarize themselves with the maintenance procedures available.

Guidelines

These procedures are divided into six parts:

(1) Introduction

(2) 4ESS Switch Modified Recovery Procedures

(3) 4ESS Switch Emergency Recovery Procedures

(4) 4ESS Switch Manual Recovery Procedures

(5) Attached Processor System Manual Recovery Procedures

(6) Attached Processor System Emergency Recovery Procedures.

Each procedure identifies **Recovery Actions** that may clear the system problem. To use the recovery procedures contained in this document, follow the identified **Recovery Actions** in the order presented.

Modified Recovery Procedures

This procedure is for recovering the 4ESS Switch using modified recovery action phases. Phase completion times are dependent on call load, number of equipped trunks, etc.

Perform **Recovery Actions** in the order listed:

Recovery Action 1

Identify functions to be performed and applicable MCC Direct Data Insert keys using the following Direct Data Insert Key Identification table. At MCC terminal: Enter EAI page. Enter poke command 401,xx (xx = DDI key).

DDI Key	Function	Application
00	Leave all pests set during and after the phase. Leave audits in manual-only mode.	PH 1, 2, 3, 4
01	Roll back to tape 1	PH 3, 4
02	Roll back to tape 2	PH 3, 4
03	Roll back number of orders indicated by Page 120, Poke 940 (Display Section 1)	PH 2, 3, 4
04	Roll back to order number indicated by Page 120, Poke 940 (Display Section 1)	PH 2, 3, 4
05	Clear disk areas specified by system integrity program	PH 3, 4
06	Clear network management controls	PH 2, 3, 4
07	Initialize trunk OOS list (TOSL)	PH 3, 4
08-10	Reserved	
11	Restore duplex failed units	PH 3
11	Restore all units to duplex	PH 4
12-13	Reserved	
14	Allow duplex failed PUBB	PH 2, 3, 4, SR
15	Multiple tape SR *	SR

See notes at end of table.

DDI Key	Function	Application
16	Zero all call or program store memory not backed up on disk	AO, PC (pump)
17	Skip hashsum calculations. Skip ID2FS MAP checks.	SR, AO, PC
18	Bypass CC sanity tests and PU tests	PH 3, PH 4, SR, PC
19	Inhibit tape error correction procedure during an SR	SR
20	Inhibit MAP audit failures during an SR	SR
21	Inhibit store maintenance tests	SR, AO, PC (pump)
22	Not Used	
23	Allow duplex API failures during SR	SR (MIN CFG EMER MODE)
24	Skip MUP restart during PC/SR	PC, SR
25	Allow MUP supervisor mode utility SR	SR
26	Inhibit IFB access tests	PH 3, PH 4, SR
27	Inhibit automatic diagnostic	PH 3, PH 4, SR
28-31	Reserved	

* Not support for 4E19 generic program.

Legend:
AO - Activate Override
PC - Processor Configuration
PH - Phase(s)
SR - System Reinitialization

Recovery Action 2

Enter poke 84 (**MODIFY RECV**).

Recovery Action 3

Enter applicable **PHASE 1, PHASE 2, PHASE 3, or PHASE 4** (Poke 51-54).

Recovery Action 4

- Select applicable **SOFT A** key (Poke 02) or **HARD A** key (Poke 01).
- Allow sufficient time (________ seconds) for system to recover.

Emergency Recovery Procedures

The use of this procedure should not circumvent any normal escalation strategy. Check for obvious problems and abnormal conditions before attempting 4ESS Switch emergency recovery:

- Power problems
- Work being performed on frames (CNs, Repairs, Growth, and others)
- Current recent change activity
- MCC terminal **EAI PC PROGRESSION CMPL** lamp remains unlighted
- Current overwrite installation [software change package (SCP), broadcast warnings Message (BWM), office data assembler (ODA), or Big generic utility program (GULP)]
- Sudden environmental changes (Air conditioning problems, electrical storm, etc.)
- Activity preceding incident
- APS MCRT Terminal **SYS EMER INDICATOR** remains lighted.

NOTE:
Contact your support organization within 5 minutes if the 4ESS Switch cannot be recovered.

PHONE NUMBER ______________________________.

Identify system **Symptoms** and perform applicable **Recovery Actions** to restore system:

Symptom 1

1B Processor Repeated PC	— **REPEATED PC** lamp lighted on master control console (MCC) terminal EAI page — Continuous **PCRV:B** messages received — **PC STATE** continues to change on MCC EAI page
1B Processor Repeated Phases	— **PHASES 1, 2, 3, and 4** remain highlighted on MCC EAI page.
1B Processor Rolling Phases	— A Phase 2 or 3 follows a previous phase within 15 minutes.

Recovery Actions

- Clear any major problems.
- If 3B Computer is down, perform **Recovery Actions** for **Symptom 2**.
- If 3B Computer is in Disk Independent Operation (DIOP), use 120 page to repair MHD subsystem.
- If work is being performed on a peripheral frame, power down frame IPUBs.
- If work is being performed on a 1B processor frame, power down processor unit.
- If problem develops with active peripheral unit bus (PUB), control console (CC), program store bus (PSB), call store bus (CSB), or auxiliary unit bus (AUB) unit while repairs are being performed on mate:

Recovery Actions (Contd)

1. Attempt 4ESS Switch Manual Recovery Procedures
2. If 4ESS Switch Manual Recovery fails, continue repairs.

- If an overwrite, recent change, growth, or 1B file is suspect, select the following MCC keys:

    1. Display active units (Poke 118)
    2. Obtain EAI DISP Page (Depress EAI Key)
    3. Clear Configuration, enter Poke 99
    4. If **NORM FILE**, enter Poke 61
    5. If **UPDATE FILE**, enter Poke 62
    6. Select **MODIFY RECV**, enter Poke 84
    7. Select or Release **DIS AUTO PC**, enter Poke 70
    8. Reset **DDI** Keys to 0, enter Poke 402
    9. Set **DDI** Key 17 to 1, enter Poke 401, 17
    10. Execute **Hard A**, enter Poke 01
    11. If **NORM FILE**, enter **UPD:COMMIT;NORMFILE!**
    12. If **UPDATE FILE**, enter **UPD:COMMIT;UPDFILE!**

- If both 1B files contain a suspect overwrite, contact support organization.
- If previous **Recovery Actions** do not apply or system does not recover, perform 4ESS Switch Manual Recovery Procedures.

Symptom 2

APS MCRT Terminal Repeated Boots	— **System Emergency** indicator on EAI page remains lighted — Continuous failing PRMs received on 3B printer — Continuous PRMs received where major ‘‘boot steps’’ count up and start over.
APS MCRT Terminal Repeated Phases	— Active CU on EAI page switches between CU 0 and CU 1 repeatedly.
3B Computer Terminal Rolling Boots	— A 52 Boot or 53 Boot follows a previous boot within 15 minutes.

Recovery Actions

- Clear any major problems.
- If work is being performed on an IOP, DFC, MHD, CU, or API, power down unit.
- If problem develops with active CU, DFC, MHD, or IOP while repairs are being performed on mate:
  1. Attempt 4ESS Switch Manual Recovery Procedures
  2. If 4ESS Switch Manual Recovery fails, continue repairs.

Recovery Actions (Contd)

- If BWM is suspect:

  1. At 3B Computer terminal, force active CU on-line (Poke 12)
  2. Force active Disk on-line (Poke 20 or 22)
  3. If 3B Computer is operating on ROOT, force BROOT (Poke 30)
  4. If 3B Computer is operating on BROOT, force ROOT (Poke 31)
  5. Perform a 53 Boot (Poke 53).

- If previous **Recovery Actions** do not apply or system does not recover, perform Attached Processor System Manual Recovery Procedures.

Symptom 3

Ring in Quiet Mode	— ROP printout reports Ring is in QUIET mode.
No Active RPCNs	— 1105 page shows no active RPCNs in group 00 and 32.
Rolling Ring Initializations	— Initialization level 2 or higher follows a previous initialization level within 15 minutes.
No Active DLNs	— 1107 Page shows no active DLNs in Group 00 and 32.

Recovery Actions

- On 3B Computer terminal emergency action interface (EAI) page, perform a 53 Boot (Poke 53).
- If the Ring does not recover within 3 minutes, on 3B Computer terminal EAI page perform the following steps:
  1. Force active CU on-line (Poke 12)
  2. Force active Disk on-line (Poke 20 or 22)
  3. If 3B Computer is operating on ROOT, force BROOT (Poke 30)
  4. If 3B Computer is operating on BROOT, force ROOT (Poke 31)
  5. Perform a 54 Boot (Poke 54).
- If system does not recover, perform **Recovery Actions** for **Symptom 2**.

Symptom 4

Duplex-Failed APIs

NOTE:
Never request a 1B Processor phase or attempt processor configuration if the attached processor interfaces (API) are duplex failed and the 1B Processor is processing calls of any type.

Recovery Actions

- If 3B Computer is down, perform **Recovery Actions** for **Symptom 2**.
- At 1B Processor MCC terminal, enter:

  1. **RST:IFB 0;UCL!**
  2. **RST:IFB 1;UCL!**
  3. **RST:AUI 0;UCL!**
  4. **RST:AUI 1;UCL!**
  5. **RST:API 0;UCL!**
  6. **RST:API 1;UCL!**

- If APIs are still duplex failed:
  1. At 3B Computer MCRT terminal, enter:

     INIT:APDRV:FPI!
  2. At 1B Processor MCC terminal, enter:

     a. **RST:API 0;UCL!**
     b. **RST:API 1;UCL!**

Symptom 4

Recovery Actions (Contd)

- If APIs are still duplex failed, on 3B Computer EAI page perform a 53 Boot (Poke 53).
- After 2 minutes, if APIs are still duplex failed:
  1. Power cycle both APIs (0 and 1)
  2. At 1B Processor MCC channel, type and enter:
     a. **RST:API 0;UCL!**
     b. **RST:API 1;UCL!**
- If the system does not recover, perform **Recovery Actions** for **Symptom 2**.

Symptom 5A

1B Processor Auto Recovery Completed And Major Units Duplex-Failed	—	50 percent of digital interfaces (DIF) and digroup terminals (DT); 50 percent of signal processors (SP) or time slot interchange (TSI) lost, or 50 percent of time multiplexed switch processors (TMSP) lost.

Recovery Actions

- Clear any major power problems.
- Clear any PUB or base SP problems.
- Select the following MCC terminal EAI keys:

  1. **MODIFY RECV** (Poke 84)
  2. **DIRECT DATA INSERT 11** (Poke 401,11)
  3. **PHASE 3** (Poke 53)
  4. **SOFT A** (Poke 02)

- If the percent of major units duplex-failed does not improve after Phase 3 completes, perform a manual check for units with power off. Check, specifically, for power off the PUB (PUBB Frame) and the base SP Pulse Points (SP0/PPL, SP1/PPL). Repeat **Symptom 5A** if a major power problem is corrected; otherwise, perform **Recovery Actions** for **Symptom 1**.

Symptom 5B

1B Processor Auto Recovery Completed And Major Units Duplex-Failed	— 80 percent of DIFs, DTs, and VIFs lost; 80 percent of SPs or TSIs lost, or all TMSPs lost.

Recovery Actions

- Clear any major power problems.
- Clear any PUB or base SP problems.
- Select the following MCC terminal EAI keys:

  1. **MODIFY RECV** (Poke 84)
  2. **DIRECT DATA INSERT 11** (Poke 401,11)
  3. **PHASE 4** (Poke 54)
  4. **SOFT A** (Poke 02)

- If major units remain duplex-failed after Phase 4 completes, select the following MCC terminal EAI keys:

  1. **PHASE 4** (Poke 54)
  2. **SOFT A** (Poke 02)

- If the percent of major units duplex-failed does not improve after Phase 4 completes, perform a manual check for units with power off. Check, specifically, for power off the PUB (PUBB Frame) and the base SP Pulse Points (SP0/PPL, SP1/PPL). Repeat **Symptom 5B** if a major power problem is corrected; otherwise, perform **Recovery Actions** for **Symptom 1**.

Symptom 6

All 1B Processor Input/Output Lost

NOTE:
Unless there are other service problems, an Input/Output problem should be suspected when the MCC is functioning and **MCC TIMEOUT** has not occurred. If no Input/Output problem is suspected, perform 4ESS Switch Manual Recovery Procedures.

Recovery Actions

- If system is in a phase, allow sufficient time for system to recover.

  NOTE:
  System is in a phase if MCC **NUMERIC DISPLAY** is counting or **PHASE IN PROGRESS** lamp is lit and bit **23** is flashing.

- If system does not recover from phase, perform **Recovery Actions** for **Symptom 1**.
- If system is not in a phase, select the following MCC terminal EAI keys:

  1. Clear any Phase request selections (**PHASE 1, PHASE 2, PHASE 3, PHASE 4**)
  2. Clear **MODIFY RECV** if selected
  3. **RESTORE I/O** (Poke 83)
  4. **SOFT A** (Poke 02)

- If previous **Recovery Actions** do not apply or system does not recover, perform 4ESS Switch Manual Recovery Procedures.

Symptom 7

All 3B Computer Input/Output Lost

Recovery Actions

- If 3B Computer is in Disk Independent Operation (DIOP), use the 3B Computer terminal 120 Page to repair MHD subsystem.
- If 3B Computer terminal EAI page can be obtained, request Craft Initialization (Poke 15).
- If 3B Computer EAI page cannot be obtained, switch port switch.
- If Input/Output does not return, check 1B Processor to determine if 3B Computer is active.
- If 3B Computer is not active, perform **Recovery Actions** for **Symptom 2**.

Symptom 8

1B MCC Access is Lost

Recovery Actions

A. Perform the following actions to restore MCC capability:

1. If IFBs are not duplex, attempt to restore the IFBs. At MTC terminal, enter:

   RST:IFB *a***!**

2. Attempt to switch the MUPs via the MCC 106 page poke (410)
3. If the system has basic Input/Output capability, at MTC terminal enter:

   SW:MUP!

4. Remove and restore the standby MUP. At MTC terminal, enter:

   RMV:MUP *a***!**
   RST:MUP *a***!**

5. Repeat Steps 3 and 4 once.
6. If system does not recover, perform **Recovery Actions** for **Symptom 8 B** (*If no MCC functionally is restored*).

Symptom 8

Recovery Actions (Contd)

B. If no MCC functionality is restored:

1. Force a MUP switch. At MCC terminal, enter:

   esc-ctrl-x:

2. Remove and restore the standby MUP. At MTC terminal, enter:

   RMV:MUP *a***!**
   RST:MUP *a***!**

3. Force a MUP reset. At MCC terminal, enter:

   esc-ctrl-r

4. Repeat steps 1 through 3
5. Power cycle both MUPs
6. Switch the RS232 port on the back of the CC back plan to which the MCC terminal connects.
7. Replace the cable and the MCC terminal
8. Repeat steps 1 through 5.

Symptom 9

Reports of No Call Processing

Recovery Actions

- At 1B Processor MCC terminal, enter:

  OP:SDC!

- If system has basic Input/Output sanity, work with MOC to isolate common failure point.
- If system has no basic Input/Output sanity, perform **Recovery Actions** for **Symptom 6**.

Symptom 10

Critical Alarm

Recovery Actions

- Analyze output message if available.
- If phase is in progress, allow sufficient time for phase to complete.
- If phase does not complete, perform **Recovery Actions** for **Symptom 1**.
- If system has no basic Input/Output sanity, perform **Recovery Actions** for **Symptom 6**.

Manual Recovery Procedures

Read the following before attempting 4ESS Switch Manual Recovery:

- Automatic recovery is not progressing if:

    1. The MCC **NUMERIC DISPLAY** is not counting, or **BINARY DISPLAY** bit **23** lamp is not flashing.
    2. **PCRV:B FAILED** message is received.

- The MCC **FAIL ADDR/DISPLAY** poke:

    1. Provide program fail data in the MCC **NUMERIC DISPLAY** and **BINARY DISPLAY**
    2. Disable recovery progress indicators.

- Three consecutive automatic Phase 3 occurrences automatically PEST all interrupts and disable audits.
- The MCC **CLR UTIL** key inhibits **PCRV:B** messages and speeds up automatic recovery if the system is stepping through processor configuration (PC) states.
- Average Phase 3 time for this office is ________________ seconds.

Perform **Recovery Actions** in the order listed:

Recovery Action 1

NOTE:
If unable to view the MCC terminal remotely, perform the **Recovery Actions** for **Symptom 8 B** (*If no MCC functionality is restored)*.

- Bring up and clear the MCC terminal EAI page (Poke 99)
- Select the following MCC EAI key:

  DIS AUTO PC (Poke 70)

- Select MCC keys for the first manual configuration listed in the Manual Configuration Table that follows this procedure. Enter the pokes from left to right. The word "off" means that this unit should be powered down for this configuration attempt.
- Allow sufficient time (_________ seconds) for system to recover.
- If system does not recover, select next manual configuration listed in the Manual Configuration Table until all possible configurations have been exhausted.
- If 3B Computer read-only printer (ROP) contains failing PRMs or rolling APDRV error messages, perform Attached processor System Manual Recovery Procedures.
- If all 3B Computer Input/Output is lost, perform Attached Processor System Manual Recovery Procedures.

Recovery Action 1 (Contd)

Manual Configuration Table

	Processor Configuration States									
Unit	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	10
CC0	10				10	10	10	10	10	off
CC1		11	11	11				off	off	11
PS0	20		20			20		20		
PS1		21		21	21		21		21	21
PSB0	22			22		22		22		
PSB1		23	23		23		23		23	23
CSB0	30			30		30		30		
CSB1		31	31		31		31		31	31
IFB0	40		40	40		40				
IFB1		41			41	41			41	41
AUB0	42			42	42		42	42		
AUB1		43	43			43			43	43
API0									off	off
API1								off		
Norm File	61	61	61	61	61	61	61	61	61	61
DDI	16,17	16,17	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00
HARD A*	01	01	01	01	01	01	01	01	01	01

* Hard A (Poke 01) must be entered last.

Recovery Action 1 (Contd)

Manual Configuration Table

Unit	Processor Configuration States								
	11	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**
CC0	10				10	10	10	10	off
CC1		11	11	11				off	11
PS0	20		20			20		20	
PS1		21		21	21		21		21
PSB0	22			22		22		22	
PSB1		23	23		23		23		23
CSB0	30			30		30		30	
CSB1		31	31		31		31		31
IFB0	40		40	40			40	40	
IFB1		41			41	41			41
AUB0	42			42	42		42	42	
AUB1		43	43			43			43
API0									off
API1								off	
UPD File	62	62	62	62	62	62	62	62	62
DDI	16,17	16,17	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00	16,17, 06,00
HARD A*	01	01	01	01	01	01	01	01	01

* Hard A (Poke 01) must be entered last.

Recovery Action 2

- If the 1B has not recovered, perform system reinitialization (SR) using 3B Computer tape units as follows:

  1. Mount 1B generic tape on 3B tape unit 0
  2. On the 3B MCRT, enter:

     VER:UPDATE:TAPE,MT 0!

  3. Obtain the generic identification number from the output message.
  4. On the 3B MCRT, enter:

     LOAD:UPDATE:GEN *a***,MT 0!**

     a = Generic identification number in the format 4E<20>.05

  5. Wait for tape to finish loading
  6. Mount 1B ODA backup tapes on 3B tape unit 0
  7. On the 3B MCRT, enter:

     VER:UPDATE:TAPE,MT 0!

  8. Obtain the base and control data from the output message
  9. On the 3B MCRT, enter:

     LOAD:UPDATE:CONT "*aaaabb***",MT 0!**

     aaaabb = Base and control data enclosed in quotes (") in the format "CHGO99"

Recovery Action 2 (Contd)

- Wait for tape to finish loading
- On the 3B MCRT, enter:

  INIT:APDRV:FPI!

- At MCC terminal EAI page, select the following keys:
  - **MODIFY RECV** (Poke 84)
  - **DIRECT DATA INSERT KEYS 17,16,06,00** (Poke 401,17)(Poke 401,16)(Poke 401,06)(Poke 401,00)
  - **CC 0** (Poke 10)
  - **PS 0** (Poke 20)
  - **PSB 0** (Poke 22)
  - **CSB 0** (Poke 30)
  - **IFB 0** (Poke 40)
  - **AUB 0** (Poke 42)
  - **DIS AUTO PC** (Poke 70)
  - **UPD FILE** (Poke 62)
  - **PHASE 4** (Poke 54)
  - **HARD A** (Poke 01)

Recovery Action 3 (Prior to 4E21 Generic)

- If the 1B did not recover from the SR using 3B Computer tape units, perform the following procedures:

  1. Mount 800 BPI generic tape on 1B TUC
  2. Depress **SR** key on 1B TUC
  3. At MCC terminal EAI page, select the following keys:

     — **MODIFY RECV** (Poke 84)
     — **DIRECT DATA INSERT KEYS 23,17,16,06** (Poke 401,23) (Poke 401,17)(Poke 401,16)(Poke 401,06)
     — **DIS AUTO PC** (Poke 70)
     — **CC 1** (Poke 11)
     — **PS 1** (Poke 21)
     — **PSB 1** (Poke 23)
     — **CSB 1** (Poke 31)
     — **IFB 1** (Poke 41)
     — **AUB 1** (Poke 43)
     — **NORMAL SR** (Poke 63)
     — **HARD A** (Poke 01)

- After addresses have been printing on MTCE, perform the following procedures:

  1. Mount 800 BPI ODA tape on another 1B TUC
  2. Depress **SR** key on ODA tape's TUC
  3. Wait for generic tape to finish loading
  4. At MCC terminal EAI page, select the following keys:

     MODIFY RECV (Poke 84)
     SOFT A (Poke 02)

  5. Wait for ODA tape to finish loading; 1B starts to recover.

Recovery Action 4

- If the SR fails or the 1B does not come up, attempt to regain the processor in the emergency configuration so that hardware can be diagnosed and repaired.
- Select MCC keys for first configuration listed in the following Emergency Mode Manual Configuration Table. Enter the pokes from left to right. The word "off" means that this unit should be powered down for this configuration attempt.
- Allow sufficient time (________seconds) for system to recover.
- If system does not recover, select next manual configuration listed in the Emergency Mode Manual Configuration Table until all possible configurations have been exhausted.

Recovery Action 4 (Contd)

Emergency Mode Manual Configuration Table

	Processor Configuration States									
Unit	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**
Emerg CFG*	48	48	48	48	48	49	49	49	49	49
CC0	10				10	10	10	10	10	Off
CC1		11	11	11				Off	Off	11
PS0	20		20			20		20		
PS1		21		21	21		21		21	21
PSB0	22			22		22		22		
PSB1		23	23		23		23		23	23
CSB0	30			30		30		30		
CSB1		31	31		31		31		31	31
IFB0	40		40	40			40	40		
IFB1		41			41	41			41	41
AUB0	42			42	42		42	42		
AUB1		43	43			43			43	43
API0									Off	Off
API1								Off		
Norm File	61	61	61	61	61	61	61	61	61	61
DDI	16,17	16,17	16,17	16,17	16,17	16,17	16,17	16,17	16,17	16,17
HARD A†	01	01	01	01	01	01	01	01	01	01

* Emergency Configuration is 48 (full) and 49 (minimum).
† **HARD A** (Poke 01) must be entered last.

Attached Processor System Manual Recovery Procedures

Read the following before performing 4ESS Switch Attached Processor System Manual Recovery.

- A typical Processor Recovery Message (PRM) identifies the following:

  Example: **PRM_A BCDE FFGG GGGG GGGG**

  A = Active CU
  B = PRM Type
  C = Boot Step
  D = Operating System
  E = Initialization Level
  F = Reason
  G = PRM Data

- Automatic system recovery is not progressing if:

  1. The EAI page active CU indicator keeps switching between CU0 and CU1.
  2. Failing PRMs are received continuously.
  3. PRMs are received continuously where the ‘‘BOOT Step’’ keeps counting up and starting over.

Perform **Recovery Actions** in the order listed:

Recovery Action 1

At 3B Computer MCRT, clear EAI page (Poke 14).

Recovery Action 2

- Select MCC keys from left to right for first manual configuration listed in the following Manual Configuration Table.
- Allow sufficient time (________ seconds) for system to recover.

  If failing PRMs or evidence the system did not recover is received, select next manual configuration listed in the Manual Configuration Table until all possible configurations have been exhausted.
- If system does not recover after all possible configurations have been exhausted, continue with **Recovery Action 3**.

Manual Configuration Table

Manual Config	Root	BROOT	Full	MIN	Primary Disk	Secondary Disk	CU0	CU1	Boot
1		30	33		20		10		53
2		30	33		20			11	53
3	31		33			22	10		53
4	31		33			22		11	53
5	31		33		20		10		54
6	31		33		20			11	54
7		30	33			22	10		54
8		30	33			22		11	54

Recovery Action 3

- If the BOOT progressed through boot step ‘‘D’’ before failing, power down both APIs (0 and 1) and repeat from **Recovery Action 2** (Manual Configurations 5 through 8).
- If the BOOT did not progress through boot step ‘‘D’’ before failing, power down CU 0 and continue with **Recovery Action 4**.

Recovery Action 4

- Select MCC keys from left to right for first manual configuration listed in the Manual Configuration Table below.
- Allow sufficient time (________ seconds) for system to recover.
- If failing PRMs or evidence the system did not recover is received, select next manual configuration listed in the Manual Configuration Table until all possible configurations have been exhausted.
- If system does not recover after all possible configurations have been exhausted, continue with **Recovery Action 5**.

Manual Configuration Table

Manual Config	Root	BROOT	Full	MIN	Primary DISK	Secondary Disk	CU0	CU1	Boot
1	31		33		20		OFF	11	54
2	31		33			22	OFF	11	54
3		30	33			22	OFF	11	54
4		30	33		20		OFF	11	54

Recovery Action 5

Power down both CU0 and CU1, power up CU0, and continue with **Recovery Action 6**.

Recovery Action 6

- Select MCC keys from left to right for first manual configuration listed in the Manual Configuration Table below.
- Allow sufficient time (________ seconds) for system to recover.
- If failing PRMs or evidence that the system did not recover is received, select next manual configuration listed in the Manual Configuration Table until all possible configurations have been exhausted.
- If system does not recover after all possible configurations have been exhausted, continue with **Recovery Action 7**.

Manual Configuration Table

Manual Config	Root	BROOT	Full	MIN	Primary Disk	Secondary Disk	CU 0	CU 1	Boot
1	31		33		20		10	OFF	54
2	31		33			22	10	OFF	54
3		30	33			22	10	OFF	54
4		30	33		20		10	OFF	54

Recovery Action 7

Power up both CUs (0 and 1) and continue with **Recovery Action 8**.

Recovery Action 8

- Select MCC keys from left to right for first manual configuration listed in the following Manual Configuration Table.

  NOTE:
  If the system recovers, the system is in the emergency mode, and call processing does not exist.

- Allow sufficient time (________ seconds) for system to recover.
- If failing PRMs or evidence the system did not recover is received, select next manual configuration listed in the Manual Configuration Table until all possible configurations have been exhausted.
- If system recovers in minimum configuration (MIN CONFG), perform Attached Processor System Emergency Recovery Procedures to recover from minimum configuration.
- If system does not recover after all possible configurations have been exhausted, continue with **Recovery Action 9**.

Manual Configuration Table

Manual Config	Root	BROOT	Full	MIN	Primary Disk	Secondary Disk	CU0	CU1	Boot
1	31			32	20		10		54
2	31			32		22	10		54
3	31			32		22		11	54
4	31			32	20			11	54
5		30		32	20		10		54
6		30		32		22	10		54
7		30		32		22		11	54
8		30		32	20			11	54

Recovery Action 9

- Obtain 3B Computer backup tapes written immediately after last 3B Computer retrofit and perform Database-SR to recover ECD files as follows:

    1. Mount TOP tape on tape unit 0
    2. Mount database (DB) tape on tape unit 1
    3. Force CU 0 on-line (Poke 10)
    4. Force Primary Disk on-line (Poke 20)
    5. Select ROOT (Poke 31)
    6. Clear flags (Poke 14)
    7. Read TOP tape (Poke 55)
    8. Wait until TOP tape is loaded
    9. Select Application Parameter (Poke 42)
    10. Clear flags (Poke D)
    11. Read DB tape (Poke 56)
    12. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that system is not recovering is received, continue with **Recovery Action 10**.

Recovery Action 10

- On 3B Computer EAI page:

    1. Force BROOT (Poke 30)
    2. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that the system is not recovering is received, continue with **Recovery Action 11**.

Recovery Action 11

- Obtain 3B Computer backup tapes that were written immediately after last retrofit, and perform Mini-SR to recover boot processes as follows:

  1. Mount TOP tape on tape unit 0.
  2. Mount RT0-1 tape on tape unit 1.
  3. Force CU0 on-line (Poke 10).
  4. Force Primary Disk on-line (Poke 20).
  5. Select ROOT (Poke 31).
  6. Select FULL CONFIG (Poke 33).
  7. Read TOP tape (Poke 55).
  8. Wait until TOP tape is loaded.
  9. Read RT0-1 tape (Poke 56).
  10. Wait 15 seconds.
  11. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that the system is not recovering is received, continue with **Recovery Action 12**.

Recovery Action 12

- On 3B Computer EAI page:

  1. Force BROOT (Poke 30)
  2. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that system is not recovering is received, continue with **Recovery Action 13**.

Recovery Action 13

Perform Generic-only LDFT by repeating **Recovery Actions 11** and **12** while allowing all RT0 tapes (RT0-1, RT0-2, RT0-3, etc.) to be read completely.

Attached Processor System Emergency Recovery Procedures

NOTE:
This procedure is for recovering the 4ESS Switch Attached Processor System (APS) from minimum configuration (MIN CONFIG) or emergency mode (EMER MODE) and assumes previous actions have been attempted to recover the APS on full configuration (FULL CONFIG) but failed.

Check for obvious problems and abnormal conditions before attempting emergency recovery:

- Power problems
- Work being performed on frames (CNs, Repairs, Growth, etc.)
- Current recent change activity
- MCC **PROCESSOR CONFIG COMPLETED** lamp does not light
- Current overwrite installation
  [Software change package (SCP), BWM, ODA, or Big GULP]
- Sudden environmental changes
  (Air conditioning problems, electrical storm, etc.)
- Activity preceding incident
- 3B Computer MCRT **SYS EMER INDICATOR** remains lighted.

NOTE:
Contact your support organization within 5 minutes if the 4ESS Switch attached processor system cannot be recovered

Phone Number ______________________________.

Perform **Recovery Actions** in the order listed below:

Recovery Action 1

- At MCRT, type and enter the following to switch FULL CONFIG bootimage with one saved after last retrofit:

  EXC:ENVIR:UPROC, FN ''/ tools / bootaud'', ARGS (''sa'', ''*xxx*'') !
  xxx = SID parameter supplied by support organization.

- Wait for SUCCESS message in response and continue with **Recovery Action 2**.

Recovery Action 2

- On 3B Computer EAI page:

  1. Select FULL CONFIG (Poke 33)
  2. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that the system is not recovering is received, continue with **Recovery Action 3**.

Recovery Action 3

- On 3B Computer EAI page:

  1. Select MIN CONFIG (Poke 32)
  2. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that system is not recovering is received, continue with **Recovery Action 4**.

Recovery Action 4

- At MCRT, type and enter the following to switch FULL CONFIG ECD with one saved most recently:

  EXC:ENVIR:UPROC, FN ''/ tools / bootaud'', ARGS (''se2'', ''*xxx*'') !
  xxx = SID parameter supplied by support organization.

- Wait for the SUCCESS message in response, and continue with **Recovery Action 5**.

Recovery Action 5

- On 3B Computer EAI page:

  1. Select FULL CONFIG (Poke 33)
  2. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that the system is not recovering is received, continue with **Recovery Action 6**.

Recovery Action 6

- On 3B Computer EAI page:

  1. Select MIN CONFIG (Poke 32)
  2. Request 54 Boot (Poke 54).

- If failing PRMs or evidence that system is not recovering is received, continue with **Recovery Action 7**.

Recovery Action 7

Repeat from **Recovery Action 4** (as necessary) using different bootaud parameter (Se0 or Se1)

‘‘Se1’’ - Selects ECD saved several months ago

‘‘Se0’’ - Selects ECD saved after the last retrofit.

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Lucent Technologies
Bell Labs Innovations

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1B Processor
4E26 Generic
Maintenance Reference Handbook

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Notice

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Register Layouts and Word Breakdown

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Register Layouts and Word Breakdown

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Interrupt Level Printouts

A-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASA(H)	AC1ASA(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	AC1SAT	AC1PCR
AC1MCO	AC1MCP	AC1MCD(H)	AC1MCD(L)	AC1TAR	

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

B-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASB(H)	AC1ASB(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	AC1SAT	AC1PCR
AC1MCO	AC1MCP	AC1MCD(H)	AC1MCD(L)	AC1ITR	AC1ACT
AC1PSQ	AC1TAR	AC1BNCTL	------	ST1ASB(H)	ST1ASB(L)

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

C-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASC(H)	AC1ASC(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1ASC(H)	ST1ASC(L)
ST1SCA	ST1SDA	ST1BR(H)	ST1BR(L)	AC1ME0(H)	AC1ME0(L)
ST1LIT	ST1LPI	AC1MSR	AC1MMR	ST1MI0(H)	ST1MI0(L)
AC1MI0(H)	AC1MI0(L)	AC1ME1(H)	AC1ME1(L)	AC1MI1(H)	AC1MI1(L)
ST1ME0(H)	ST1ME0(L)	ST1MI1(H)	ST1MI1(L)	ST1ME1(H)	ST1ME1(L)
AC1SAT	AC1TAR	AC1BNCTL	-----	-----	-----

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

D-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASD(H)	AC1ASD(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1CES	ST1ILA
AC1AP	AC1ABC	AC1IBR	ST1IBR	AC1TAR	AC1BNCTL

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

E-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASE(H)	AC1ASE(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1CES	ST1ILA
AC1AP	AC1ABC	AC1IBR	ST1IBR	AC1TAR	AC1BNTCL

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Call Store and Program Store Identification Data

FAILING	FAILING				
H_ADDR	ADDR	RCES	ST1BRS_H	ST1BRS_L	AC1SAL
AC1SAR	ST1SAL	ST1SAR	SCES	FAILING MEMN	VBOOT
BFAILRT	SYSSTAT	IBUSSTAT	SAMEMN	MNSUSP	BUSBUFFGCPS*
GCPACT_L	GCPACT_H	CR01ACT	CR10ACT	XXXXXX	FLAGS1
GCPSTBY_L	GCPSTBY_H	CR01STBY	CR10STBY	XXXXXX	FAFTRACK
CINS	C_ACT_EVEN	C_ACT_ODD	C_STBY_EVEN	C_STBY_ODD	REP_STORE
BUSSTATER	C_H_ACT_EVEN	C_H_ACT_ODD	C_H_STBY_EVEN	C_H_STBY_ODD	ST1ABC
FAILING	XXXXXX				
MCODE					

* The BUSBUFFGCPS field is for CS only and is 00000000 for program store.

Identification Register Descriptions

FAILING H_ADDR— Bits 24-29 of the 30-bit failing address

FAILING ADDR— Bits 0-23 of the 30-bit failing address

RCES—CC Error Summary Used by the Fault Recovery Program to Recover Interrupt

ST1BRS_H—High 8 Bits of the Standby CC Shadow B-Register

ST1BRS_L—Low 24 Bits of the Standby CC Shadow B-Register

AC1SAL—Save Even Address Reply on Program Fetches

AC1SAR—Save Odd Address Reply on Program Fetches

ST1SAL—Save Even Address Reply on Standby CC Program Fetches

ST1SAR—Save Odd Address Reply on Standby CC Program Fetches

SCES—Standby CES Used to Recovery Standby Store When Stores Were Duplexed

FAILING MEMN—Failing Member and Software Decisions

Bit 0-5 = Suspected failing member. MEMN removed if bit 23 = 1
21 = Bootstrap failed on first attempt (first bus)
22 = Bootstrap has been entered
23 = When set, the member indicated (bits 0-5) has been removed

VBOOT—Variable Bootstrap Status, After Recovery

Bit 0-3 = Count of bootstrap entries
4 = The member number (MEMN) in VBOOT was forced out by VBOOT
9-14 = MEMN forced out in current VBOOT state
15-17 = Variable boot state counter
18 = Two-word pump performed as part of recovery

BFAILRT—The Return Address in the Recovery Program for a Bootstrap Failure

SYSSTAT—System Status at Time of Interrupt

Bit 0 = PBO of standby CC at entry to interrupt
1 = PBA OF standby CC at entry to interrupt
2 = PBT of standby CC at entry to interrupt
3 = CBO of standby CC at entry to interrupt
4 = CBA of standby CC at entry to interrupt
5 = CBT of standby CC at entry to interrupt
6 = Indicates base MCODE (3=E-level/0=D-level) for community has been pumped when set
7 = State of CC1CCS (CC software duplex status) at time interrupt
15 = Status of AC1DIV bit (CC divorce) in CSC prior to interrupt

IBUSSTAT—BUSSTAT at Interrupt Entry (Call Store)

Bit 0 = Non-D-level entry flag
1 = Used to indicate to CALCONFIG that the call store community is to be set up in an off-line configuration
2 = When set, call store memory was pumped from disk as part of recovery
3 = When set, active CC sends over both buses
4 = Defines the bus used by the active CC. Bus 1 is active when set
5 = Both CCs will receive from the active bus when set
6 = CS bus 0 is in trouble if set
7 = CS bus 1 is in trouble if set
8 = When set, indicates there has been a change in the bus configuration
9 = Set if one or more stores are in the frozen state
11 = Set at start of phase by application program. Reset at end of phase by application program. Used to alter interrupt recovery strategy
12 = If status audit fails in CALCONFIG, this item is set before going to the hardware status update. When set, audit failure in CALCONFIG will not go to hard status
13 = Set when a call store bus routine exercise has been requested
14 = Set when a call store bus or call store routine exercise has been requested
15 = A non-backed up store has failed without a duplicate
16 = If set the standby bus is to be kept out-of-service until manual restoral request (TTY)
17 = If set, stop REX before testing next store
18 = Set when block zero has been pumped
19 = If set, the DGN is performing critical tests in case an interrupt occurs, establish configuration found in status table
21 = CS bootstrap assembled a working configuration
22 = CS bootstrap failed to assemble a working configuration using in service stores and the selected bus
23 = Used to save state of CBA/PBA (bit 4/1) prior to a bus store routine or REX

IBUSSTAT—BUSSTAT at Interrupt Entry (Program Store)

Bit 0 = When set, active CC sends over both program store buses.
1 = Defines the program store bus used by the active CC
2 = Both CCs receive from the active bus when set
3 = Non-E-level entry flag
4 = Used to indicate to CALCONFIG that the PS community is to be set up in an off-line configuration
5 = When set, PS memory was pumped from disk as part of recovery
6 = PS bus 0 is in trouble if set
7 = PS bus 1 is in trouble if set
8 = When set, indicates there has been a change in the bus configuration
9 = Set if one or more stores are in the frozen state
11 = Set at start of phase by application program. Reset at end of phase by application program. Used to alter interrupt recovery strategy
12 = If status audit fails in CALCONFIG, this item is set before going to the hardware status update. When set, audit failure in CALCONFIG will not go to hard status
13 = Set when a program store bus routine exercise has been requested
14 = Set when a program store routine exercise has been requested
16 = If set the standby bus is to be kept out-of-service until manual restoral request (TTY)
17 = If set, stop the store routine. (1/2 hour has expired since exerciser was started.) See bit 14
18 = Set when block zero has been pumped
19 = If set, the DGN is performing critical tests in case an interrupt occurs, establish configuration found in status table
21 = PS bootstrap assembled a working configuration
22 = PS bootstrap failed to assemble a working configuration using in service stores and the selected bus
23 = Used to save state of PBA prior to a REX routine

SAMEMN—Standby and Active Member Numbers for Failing MCODE
(Valid for non-bus related faults only)

Bit 0-5 = Active member number supplying MCODE interrupting
6-9 = Error count for active unit at entry to interrupt
10 = Flag for active member number (set if in service)
11 = Unused
12-17 = Standby member number suppling MCODE interrupting
18-21 = Error cont for standby unit at entry to interrupt
22 = Flag for standby member number (set if in service)
23 = Copy was in progress on standby store when interrupt occurred

MNSUSP—Suspect MEMN List

Bit 0-5 = Last MEMN having ATP DGN after interrupt
6 = When set, bits 0-5 are valid
7-12 = Next to last MEMN having ATP DGN
13 = When set, bits 7-12 are valid

BUSBUFFGCPS—Call Store Bus Buffer GCP Status Information
(Call Store only)

Bit 0 = GCP reply for call store bus 0—frame 0 (active if set)
1 = GCP reply for call store bus 0—frame 1 (active if set)
2 = GCP reply for call store bus 1—frame 0 (active if set)
3 = GCP reply for call store bus 1—frame 1 (active if set)

GCPACT_L—Low 24 Bits of Active Store GCP Response
GCPSTBY_L—Low 24 Bits of Standby Store GCP Response

Bit 0 = Send on bus 0 flip-flop
1 = Send on bus 1 flip-flop
2 = Receive on bus flip-flop
3 = Receive on bit complement
4-12 = MCODE name bits
13 = Store update bit
14 = Trap mode error
15 = MCC address match detected when set
16 = Trap write protect violation when set
17 = Trap all-seems-well fail when set
18 = Trap data parity failure when set
19 = Trap address parity failure when set
20 = Address match detected when set
21 = Communications reply inhibit when 0
22 = Store in MTCE when 1
23 = Store maintenance complement bit

GCPACT_H—High 8 Bits of Active Store GCP Response
GCPSTBY_H—High 8 Bits of Standby Store GCP Response

Bit 2 = When set, store was not listening to bus

CR01ACT—Control Read 01 Response—Active Store
CR01STBY—Control Read 01 Response—Standby Store

Bit 0 = Send on bus 0 flip-flop
1 = Send on bus 1 flip-flop
2 = Receive on bus flip-flop
3 = Receive on bus flip-flop complement
4-12 = Store MCODE name
13 = Update bit—software controlled
14 = Trap mode error bit
15 = MCC address match detected
16 = Trap write protect violation
17 = Trap all-seems-well failure
18 = Trap data parity fail
19 = Trap address parity fail
20 = Address match detected
21 = Communications reply inhibit complement
22 = Maintenance bit
23 = Maintenance bit complement

CR10ACT—Control Read 10 Response
CR10STBY—Control Read 10 Response

Bit 3 = Write protect inhibit
4 = Write protect
13 = Data parity failure byte 0
14 = Data parity failure byte 1
15 = Data parity failure byte 2
16 = Data parity failure byte 3
17 = Address parity failure byte 0
18 = Address parity failure byte 1
19 = Address parity failure byte 2
20 = Address parity failure byte 3
21-23 = Store hardware (1 = megaword)

FLAGS1—Flags and Data Relevant to Interrupt

Bit 0 = Unduplicated and suspect store interrupt
2 = Indicates the write protect program entered at MUFRWPHS [memory not protected by WPAD (Write Protect Administration Program)]
3 = MAC failed to accept the copy job
4 = Indicates a write protect violation has occurred on this interrupt and no other errors were indicated
5 = MCODEs duplexed for the failing address
6 = Standby store chosen as faulty by recovery
7 = Active store chosen as faulty by recovery
8 = Indicates parity failure only
9 = Segment memory enabled at the time of interrupt (PRDSEGMEMFLG)
12 = If PS, Last segment number enabled at the time of interrupt (PRDSEGNO)
12-15 = If CS, Last segment number enabled at the time of interrupt (PRDSEGNO)

FAFTRACK—Full Access Failure Tracking Word

Bit 0-2 = Indicates the number of times that the full access test failed
3-5 = Indicates which times through the full access failure that the standby store was removed
6-8 = Indicates which times through the full access failure that the bus was removed to recover
9-11 = Indicates which times through the full access failure that the bus was switched to recover
12 = Indicates that the standby bus was removed
13 = Indicates that the buses were switched
14 = Indicates that the pipeline was suspected of error progagation. All store tapes were cleaned and the full access tests were re-executed
15 = Indicates that full access was entered
16 = Set if bus 0 removed by fault recovery
17 = Set if bus 1 removed by fault recovery
18 = Disk pumping routine FINFILL was entered as part of recovery
19 = Two word pump inconsistency—failing address and MCODE don’t match
20 = CCs failed access tests when put in step

CINS—Active Interrupt Error Source (AC1INS) Register OR’ed with Standby (ST1INS)

C_ACT_EVEN—Contents of the Active Store at the Falling Address Aligned on an Even Word Boundary (For example, 310 = 310 and 311 = 311)
C_ACT_ODD—Contents of the Active Store at the Falling Address Aligned on an Odd Word Boundary (For example, 310 = 310 and 311 = 311)

C_STBY_EVEN—Same as C_ACT_EVEN Except for the Standby Store When Duplexed

C_STBY_ODD—Same as C_ACT_E_ODD Except for the Standby Store When Duplexed

REP_STORE—Replacement Stores Status

Bit 0-5 = Replacement member used when bit 23 = 1
6-14 = MCODE store was at when taken as a replacement
22 = Attempt to find a substitute was made
23 = Replacement found when bit = 1

BUSSTATER—At End of Recovery. See IBUSSTAT

C_H_ACT_EVEN—Bit Register Contents for the Active Store on an Even Word Boundry
C_H_ACT_ODD—Bit Register Contents for the Active Store on an Odd Word Boundry

Bit 0-7 = Contents of bits 24-31 in memory for the active store at the failing address aligned on an even word boundry (for example; 311 = 310, 310 = 310)
12-15 = Stored parity bits for the B register
18-21 = Computed parity bits for associated 32 bit word

C_H_STBY_EVEN—Same as C_H_ACT_EVEN Except for the Standby Store When Duplexed
C_H_STBY-ODD—Same as C_H_ACT_ODD Except for the Standby Store When Duplexed

ST1ABC—Standby Auxiliary Buffer Control Containing the All-Seem-Well and Parity Bits for the Reply Words of an Instruction Fetch

FAILING MCODE—Failing MCODE and Software Decisions

0-9 = MCODE associated with bits 20-23
11 = All seems well error
12 = All seems well failure response from MCODE in bits 0-9
13 = Parity error right for E-LEVEL, CS parity error for D-LEVEL
14 = Parity error left for E-LEVEL, not available for D-LEVEL
19 = Set if the pre-qualify test failed
20 = Set if the single MCODE access test failed
21 = Set if the full access test failed the first time
22 = Set if the full access test failed the second time
23 = Bus test failed

Call Store or Program Store Test Results

BOOTTAG	VBOTSTA	BR	FR	GR	JR
KR	LR	XR	YR	ZR	MEMN

Two lines of data are printed out for each store that has failed a bootstrap test.

BOOTTAG—Program Address of Routine which Identifies Reason for Bootstrap Entry (CS1RBFAILRT)

VBOTSTA—Variable Bootstrap Status Word (CS1RVBOOT)

JR—CC J-Register—Contains Address of Failing Test

MEMN—Failing Store Member Number

BR, FR, GR, KR, LR, XR, YR, ZR—CC Register Values at Time Failure Detected

D-Level Software Failure

IB1E_H_ADDR IB1D-ADDR IB1D-LHIN IB1D-RHIN IN1UPA IN1LPA

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

E-Level Software Failure

IB1E_H_ADDR IB1E-ADDR IB1E-LHIN IB1E-RHIN

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

F-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	-----
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RP0	AC1RP1	ST1RP0	ST1RP1
ST1CSC	ST1INH	PU1RFLCO0	PU1RFLCO1	PU1RFLCO2	PU1RFLCO3
PU1RFLCO4	PU1RFLCO5	PU1RFLCO6	PU1RFLCO7	-----	-----

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

For IO F-Levels:

PU1RFLCO0	PLSRPLY (MA Pulse reply)
PU1RFLCO1	USOFT-STAT (Unit Software status)
PU1RFLCO2	UHARD-STAT (Unit hardware status)
PU1RFLCO3	SU-STAT (Subunit status)
PU1RFLCO4	ESR (Error summary)
PU1RFLCO5	ACTION (Recovery action)
PU1RFLCO6	CSR (Channel status register)
PU1RFLCO7	TSTRSL7 (Test result flags)

F-Level (Contd)

For BBFR F-Levels:

PU1RFLCO0	E-Register
PU1RFLCO1	PRM P-Register Most
PU1RFLCO2	PRL P-Register Least
PU1RFLCO3	Failing Address
PU1RFLCO4	L-Register
PU1RFLCO5	Not Used
PU1RFLCO6	Not Used
PU1RFLCO7	Not Used

For other frames and PBFR F-Levels:

PU1RFLCO0	MA Pulse Reply—C0
PU1RFLCO1	MA Pulse Reply—C1
PU1RFLCO2	Hardware Status Register—C0
PU1RFLCO3	Hardware Status Register—C1
PU1RFLCO4	Error Source Register—C0
PU1RFLCO5	Error Source Register—C1
PU1RFLCO6	FAILTEST1 (See Peripheral Fault Recognition Results)
PU1RFLCO7	FAILDATA1 (See Peripheral Fault Recognition Results)

K-Level

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASK(H)	AC1ASK(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	AC1SAT	---

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Error Stop (ERSP)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	-------	-------
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	------	------

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Interject

INJ --- --- --- --- ---

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Current Address and Data Address Stacks

AC1SCA(0)	AC1SDA(0)	AC1SCA(1)	AC1SDA(1)	AC1SCA(2)	AC1SDA(2)
AC1SCA(3)	AC1SDA(3)	AC1SCA(4)	AC1SDA(4)	AC1SCA(5)	AC1SDA(5)
AC1SCA(6)	AC1SDA(6)	AC1SCA(7)	AC1SDA(7)	AC1SCA(8)	AC1SDA(8)
AC1SCA(9)	AC1SDA(9)	AC1SCA(10)	AC1SDA(10)	AC1SCA(11)	AC1SDA(11)
AC1SCA(12)	AC1SDA(12)	AC1SCA(13)	AC1SDA(13)	AC1SCA(14)	AC1SDA(14)
AC1SCA(15)	AC1SDA(15)	---	---	---	---

Error During Diagnostic Audit Analysis

When an **Error During Diagnostic** audit occurs, the AUX specifies the address of the diagnostic program that detected an error. The general registers displayed show register contents at the AUX address. In addition, four status sections of the corresponding diagnostic scratch area are displayed.

```
AUDIT AT dcontoll.adr  AUX=dgnprog.adr  CLIENT=MTC
ERROR DURING DIAGNOSTIC
CC REGS
L=octal.data      F=octal.data    G=octal.data    J=octal.data
K=octal.data      X=octal.data    Y=octal.data    Z=octal.data
SHADOW REGS
L=octal.data      F=octal.data    G=octal.data    J=octal.data
K=octal.data      X=octal.data    Y=octal.data    Z=octal.data

DIAGNOSTIC CONTROL STATUS
STATUS*
 REQID    OPSTAT   PARMS    CUROP    SPFLGS   TMPFLGS  OUTCATNO SAVY
 SAVLIT   CONFIG   ABORT    CATP2    CATPS2   INSGAD   SEGSUBS  ENSGAD
 CATP     CATPS
STATUS*
 RAWCNT   RAWTEST  PAGELNK  PAGELNK  PAGERTN  PAGEJSV  RAWTOT   RTNADRS2
 LOOPCT   REQTAB   REQTAB   DELAYCTS CNTLCL   CNTLCL   REGSVF   REGSVG
 REGSVJ   REGSVK   REGSVL   REGSVX   REGSVY   REGSVZ   REGSVFS  REGSVGS
 REGSVJS  REGSVKS  REGSVLS  REGSVXS  REGSVYS  REGSVZS  DL1SEG   RAWPTSV
 SICNT    SIDATA   SIDATA   SIDATA   SIDATA   SIDATA   SIDATA   SIDATA
 SIDATA   USERFLGS PAGEAD   RAWCALL  PSCSAVE1
STATUS*
 DBT      DBT+1    DBT+2    DBT+3    DBT+4    DBT+5    DBT+6    DBT+7
 DBT+8    DBT+9    DBT+10   DBT+11   DBT+12   DBT+13   DBT+14   DBT+15
 DBT+16   DBT+17   DBT+18   DBT+19   DBT+20   DBT+21   DBT+22   DBT+23
 DBT+24   DBT+25   DBT+26   DBT+27   DBT+28   DBT+29   DBT+30   DBT+31
STATUS†
 DATA     DATA+1   DATA+2   DATA+3   DATA+4   DATA+5   DATA+6   DATA+7
 DATA+8   DATA+9   DATA+10  DATA+11  DATA+12  DATA+13  DATA+14  DATA+15
 DATA+16  DATA+17  DATA+18  DATA+19  DATA+20  DATA+21  DATA+22  DATA+23
 DATA+24  DATA+25  DATA+26  DATA+27  DATA+28  DATA+29  DATA+30  DATA+31
```

* Prefix the follow status section with DG1.

† Prefix the follow status section with DG1RAW.

Diagnostic Control Status Descriptions

DG1REQID—Request Identification

Bit 10-16 = Member ID
17-21 = Unit ID of unit under diagnostic
22 = Controller half being tested

DG1OPSTAT—Operation Status

Bit 0 = Diagnostic being aborted
1 = Internal error detected
2 = Diagnostic abort in progress
3 = Do not store diagnostic results
4 = Application unit type
5 = DGN early terminated
6 = CPSECT address known
7-10 = Output priority
11 = Already printed illegal phase
12 = Do not pass EA the DBT
15 = First failure exit
17 = Inhibit printing raw data
18 = DL1 coded diagnostic being executed
19 = Wait state for APS=1MAAPSOP
20 = Do not go to paging area on abort
22 = TLP allowed
23 = Page in RDS

DG1PARMS—Control Parmaters Word

Bit 0-2 = Count of nested CALLSUBS
3-5 = Count of nested DOENDS
6 = Do DL1 segment end subroutine
7-13 = Each increment is .167, terminal ends automatic segment
14 = Do DL1 segment INIT subroutine
15 = Set indicates currently executing automatic segment SUB
16 = Segmenting flag:
0 = Automatic
1 = Self
17-23 = Current phase number

DG1CUROP—Conversational Commands Currently Being Executed

Bit 0 = Advancing
1 = Stepping
2 = Finding conditions at start of loop--first pass
3 = Finding conditions at end of loop--first pass
6 = Looking for sync
7 = Looking for pause
8 = Looping
21 = Set indicates defered jump ocurring

DG1SPFLGS—DCONS Jobs at Start of a Segment

Bit 0 = Return from intra-phase paging
1 = Return from inter-phase paging
2 = Return from special paging
3 = Restart diagnostic
7 = Set indicates early terminating diagnostic
8 = Raw data buffer overflow
9 = First test failure as requested
10 = Return to a task routine-3
11 = Return to a task routine-2
12 = Return to a task routine-1
13 = Return to a task routine-0
14 = Output messages
15 = Return to task routine-4-at segend
18 = Early terminate DGN
19 = Ending current phase
20 = Phase initialization in progress
21 = Request a new phase
22 = New phase needed for CONV diagnostic
23 = Terminated diagnostic

DG1TMPFLGS—Temporary Flags

Bit 0-3 = Message number in DG1OUTCATNO to be outputed
11 = Looping back to top of loop
12-23 = User temporary flags

DG1OUTCATNO—Messages to be Outputted

Bit 0-5 = CATNO 1
- 1 - Successful jump
- 2 - Successful step
- 3 - Successful advance
- 4 - Are looping
- 5 - Error in loop boundary-start
- 6 - Error in loop boundary-end
- 7 - Error in loop boundary-DOLOOP
- 8 - Error in loop boundary-subroutines
- 10 - Error in advance
- 11 - Paused
- 12 - Error after pause
- 16 - Looping complete

6-11 = CATNO 2 (Same as CATNO 1)
12-17 = CATNO 3 (Same as CATNO 1)
18-23 = CATNO 4 (Same as CATNO 1)

DG1SAVY—Save Area for Data Table Pointer

DG1SAVLIT—Save Area, Initial Read of Long Interval Timer at Start of Segment

DG1CONFIG—Save Area for DGN and System Configuration

Bit = Save of diagnostic PUBO
1 = Save of diagnostic PUBA
2 = Save of diagnostic PUBT
3 = Save of diagnostic PUBR
7 = Save of diagnostic IAPUT
8 = State of IN1IAPUT
9 = Save of PUBO
10 = Save of PUBA
11 = Save of PUBT
12 = Save of PUBR
13 = KCODE match 1 save bits-parity
14 = KCODE match 1 save bits-ASW
15 = KCODE match 0 save bits-parity
16 = KCODE match 0 save bits-ASW
17 = Diagnostic active bit

DG1ABORT—Index of abort SUB if dial or address of abort SUB if DL1

DG1CATP2— CATP Word 2

DG1CATPS2—CATP Summary Word 2

DG1INSGAD—Address of DL1 Segment INIT Subroutine

DG1SEGSUBS—Indexes of the Current Dial Segment Subroutines

Bit 0-7 = Ending segment subroutine index
8-15 = Beginning segment subroutine index

DG1ENSGAD—Address of DL1 Segment End Subroutine

DG1CATP—CATP Word

Refer to Section 3, **Conditional All Test Pass (CATP) Layouts** for layouts.

DG1CATPS—Summary CATP

Refer to Section 3, **Conditional All Test Pass (CATP) Layouts** for layouts.

DG1RAWCNT—Failing Result Counter

DG1RAWTEST—Test Counter

DG1PAGELNK—NPGSECT Linkage to Currently Executed PGSECT

Bit 0-7 = DGN program page offset
17-23 = DGN program page number

DG1PAGERTN—Save Area for Paging Controller

DG1PAGEJSV—Save Area for Paging Controller

DG1RAWTOT—Total Error Count

DG1RTNADRS2—General Save Area for Return Addresses-used by Special Operations Controller

DG1LOOPCT—Contains Count of Times Through Requested Loop on Data Table

DG1REQTAB—Request Table Contains Information Given With Request

DG1DELAYCTS—DG1PAGELNK at Start of Loop

DG1CNTLCL—Contains the Linkage to a SUB to be Run-Called by the Control Program

DG1REGSVF—Number of RD Words Passed to TLF

DG1REGSVG-DG1REGSVZ—Save of G, J, K, L, X, Y, and Z Registers

DG1REGSVFS-DG1REGSVZS—Save of F, G, J, K, L, X, Y, and Z Shadow Registers

DG1DL1SEG—DL1 ENDSEG/BEGSEG PARMS

Bit 1 = IFOPTS bit 0
2 = IFOPTS bit 1
3 = Inhibit INT
20 = Cross-over buffer bus inhibit

DG1RAWPTSV—Save of Raw Data Pointer at Buffer Overflow

DG1SICNT—Count of Supplementary Words (Maximum=7)

Bit 0-3 = Count of supplementary data words
4-11 = Supplementary data lit flags
12 = DOLOOPS on/off
13 = Subroutines on/off

DG1SIDATA—Supplementary Data

DG1USERFLGS—User Flags

Bit 1 = Test has failed
2 = No real early termination
3-4 = Save of DG1TSTRSLT
16 = OK to take pause
17-23 = Number of failing phases

DG1PAGEAD—Address of Start of Current PGSECT

DG1RAWCALL—Actual Test Counter

DG1PSCSAVE1—Diagnostics PSC Save

DG1RAWCALLS—Total Tests Executed

DG1DBT—Diagnostic Buffer Table

Bit 0-3 = Request code for diagnostic
- 0 - DGN requested by a program without GBT
- 1 - DGN requested by a program via GBT
- 2 - Manual request detected by alarm scan
- 3 - DGN requested by error analysis
- 4 - DGN requested by DGN: TTY message
- 5 - DGN requested by RST: TTY message
- 6 - DGN requested by an audit
- 7 - DGN requested by demand exercise
- 8 - DGN requested as part of a routine exercise-midnight etc
- 9 - Deferred fault recovery (DFR) requested by TTY
- 10 - DGN requested by fault recognition
- 11 - DGN requested by bootstrap programs
- 12 - DGN requested after off-line configuration
- 14 - Unconditional restoral

4-6 = Termination code for diagnostic
- 0 - Diagnostic aborted
- 1 - Initial status error detected-diagnostic not run
- 2 - Internal software error detected-diagnostic halted
- 3 - Craftsperson manually terminated DGN
- 7 - Normal termination

7-8 = Result of the diagnostic
- 0 - Conditional all tests pass
- 1 - Some test failed
- 2 - All tests passed
- 3 - No tests run

9 = Sub-unit specified in DG1SUNITRQ and DG1SMEMNRQ

10-16 = Member number under diagnosis (DG1SMEMNRQ)

17-23 = Unit type under diagnosis (DG1SUNITRQ)

DG1DBT +1 and DG1DBT +17 contain flags set by the manual input request administration (MIRA) program. DG1DBT+1 contains those flags used mainly by DCON. DG1DBT +17 contains those flags used mainly by other programs such as error analysis, the diagnostics themselves, etc. DG1DBT +1 and DG1DBT +17 are functionally divided into two halves. The left half is used for flags that have associated data arguments. The right half is used for flags that have no associated data arguments.

NOTE:
If the GBT is not set up via a manual request, these flags and data arguments may be set by any program.

DG1DBT +1

Bit 0 = Raw data requested
1 = Inhibit termination on failure
2 = Growth specified
4 = Conversational diagnostic
19 = New conversational commands typed
20 = Partial request - run specified phases
21 = Repeat diagnostic DG1RPTCNT times
22 = Output channel specified
23 = TLP specified on input

DG1DBT +2

Bit 0-7 = Number of times a DGN test is to be repeated (DG1RPTCNT)
8-15 = TTY channel on which message received
16-23 = Channel, if specified, for outputting

DG1DBT +3

Bit 0-23 = Reserved for return addresses

DG1DBT +4

Bit 0-9 = Phases 9 through 0 request bits
10-19 = Phases 9 through 0 fail bits
21-23 = MT-MV save

DG1DBT +5

Bit 0-9 = Phases 19 through 10 request bits
10-19 = Phases 19 through 10 fail bits

DG1DBT +6

Bit 0-9 = Phases 29 through 20 request bits
10-19 = Phases 29 through fail bits

DG1DBT +7

Bit 0-9 = Phases 39 through 30 request bits
10-19 = Phases 39 through 30 fail bits

DG1DBT +8

Bit 0-9 = Phases 49 through 40 request bits
10-19 = Phases 49 through 40 fail bits

DG1DBT +9

Bit 0-9 = Phases 59 through 50 request bits
10-19 = Phases 59 through 50 fail bits

DG1DBT +10

Bit 0-9 = Phases 69 through 60 request bits
10-19 = Phases 69 through 60 fail bits

DG1DBT +11

Bit 0-9 = Phases 79 through 70 request bits
10-19 = Phases 79 through 70 fail bits

DG1DBT +12

Bit 0-9 = Phases 89 through 80 request bits
10-19 = Phases 89 through 80 fail bits

DG1DBT +13

Bit 0-9 = Phases 99 through 90 request bit
10-19 = Phases 99 through 90 fail bit

DG1DBT +14

Bit 0-3 = Task number
0 - Basic unit diagnostic
4-6 = Frame scan point index
7-13 = Sub-member number requested
14-23 = Sub-unit type requested

DG1DBT +15

Bit 0 = Power alarm involved in request
1 = Request is RMV requestd by TTY
2 = Skip diagnostic request and dummy ATP
3 = Flag to show MCFWPEMO was initial entry from Maintenance Administration Control Program (MACP)
4-7 = Number of failing phases to include in TLP
9 = Sub-unit specified in DG1SUNITHP and DG1SMENHP
10-16 = Helper member number
17-23 = Helper unit type

DG1DBT +16

Bit 7-13 = Helper member number
14-23 = Helper sub-unit

DG1DBT +17

Bit 0-11 = General Flag 0 through 11
12-19 = Set indicates data in DG1DATA0 through DG1DATA7

DG1DBT +18 through DG1DBT +25

Bit 0-23 = DG1DATA0 through DG1DATA7

DG1DBT +26

Bit 0-23 = Point of maximum definition per FR analysis

DG1DBT +27

Bit 0-23 = Interrupt number associated with this request

DG1DBT +28

Bit 0-23 = Job ID of the diagnostic request

DG1DBT +29

Bit 0-23 = Error analysis processor

DG1DBT +30—Error Analysis Application

Bit 0-7 = Number of ERAT requested DGN cycles remaining to be run
8 = Text phrase present in WRD 29
9 = Indicates a DT frame diagnostic
10-11 = Count of aborts during ERATPUFH
12 = PUFH client flag for MCFWPEM0
13 = Growth unit restoral request
14 = Transfer to SYRE requested by PUFH
15 = Final handling directed by ERAT
16-22 = Error analysis decision code
23 = Final handling completed by SEQ TLB

DG1DBT +31

Bit 0-2 = Code for first abort
3-5 = Code for second abort
6 = Diagnostic aborted once
7 = Diagnostic aborted twice

DG1RAWDATA—Raw Data Area

RAWDATA +1 Through RAWDATA +61—Layout for Raw Data Storage of Failing Result

Bit 0-11 = Raw data sub catalog
12-23 = Size of raw data sub catalog

Error During Trouble Locating Procedure (TLP) Audit Analysis

When an **Error During Diagnostic** TLP audit occurs, the AUX specifies the address of the TLP program that detected an error. The general registers displayed show most register contents at the AUX address. In addition, the stack and three status sections of TLP control memory are displayed.

```
AUDIT AT dcontoll.adr  AUX=drpp_prog.adr  CLIENT=MTC
ERROR DURING DIAGNOSTIC
CC REGS
L=octal.data      F=scratch.ptr   G=prog.data     J=drpp_prog.adr
K=octal.data      X=octal.data    Y=octal.data    Z=octal.data
SHADOW REGS
L=octal.data      F=octal.data    G=octal.data    J=octal.data
K=octal.data      X=octal.data    Y=octal.data    Z=octal.data
STACK STKCNTR=n
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr  stackadr
TLP CONTROL STATUS
STATUS *
 NWDC0     SCDATA    USDAT1    SCPD      SCPD+1    SCPD+2    SCPD+3    SCPD+4
 SCPD+5    SCPD+6    SCPD+7    SCPD+8    SCPD+9    SCPD+10   SCPD+11   SCPD+12
 SCPD+13   SCPD+14   SCPD+15   SCPD+16   SCPD+17   SCPD+18   SCPD+19   SCPD+20
 SCPD+21   SCPD+22   SCPD+23   SCPD+24   SCPD+25   SCPD+26   SCPD+27   SCPD+28
 SCPD+29   SCPD+30   SCPD+31   SCPD+32   SCPD+33   SCPD+34   SCPD+35   SCPD+36
 SCPD+37   SCPD+38   SCPD+39   SCPD+40   SCPD+41   SCPD+42   SCPD+43   SCPD+44
 TPCRL0    TPCRL1    TPCRL2    TPBKAD    TPERRW
STATUS †
 LOCTID    LOCTRL    LOCFN     TAFILE    ALWUTY    TRYNO     ELAP      OVLAP
 TAPERR    TSKADL    TSKADH
STATUS *
 STLPB     STLPB+1   STLPB+2   STLPB+3   STLPB+4   STLPB+5   STLPB+6   STLPB+7
 STLPB+8   STLPB+9   STLPB+10  STLPB+11  STLPB+12  STLPB+13  STLPB+14  STLPB+15
 STLPB+16  STLPB+17  STLPB+18  STLPB+19  STLPB+20  STLPB+21  STLPB+22  STLPB+23
 STLPB+24  STLPB+25  STLPB+26  STLPB+27  STLPB+28  STLPB+29  STLPB+30  STLPB+31
 STLPB+32  STLPB+33  STLPB+34  STLPB+35  STLPB+36  STLPB+37  STLPB+38  STLPB+39
 STLPB+40  STLPB+41  STLPB+42  STLPB+43  STLPB+44  STLPB+45  STLPB+46  STLPB+47
 STLPB+48  STLPB+49  STLPB+50  STLPB+51  STLPB+52  STLPB+53  STLPB+54  STLPB+55
 STLPB+56  STLPB+57  STLPB+58  STLPB+59  STLPB+60  STLPB+61  STLPB+62  STLPB+63
```

* Prefix the following status section with DG1T_.

† Prefix the following status section with DG1A_.

Trouble Locating Procedure Status Descriptions

STACKADR 0 through STACKADR +55

DG1T_NWDC0—Number of Word Counter 0

Bit 0-12 = Number of disk raw data words
13 = Page scratch flag
14 = First pass flag
15 = End of DGN flag
16-20 = Summary TLP flag

DG1T_SCDATA—Stack Data

Bit 0-5 = Save stack counter
6-9 = Number in stack save area
10-11 = DKJ re-try counter
12 = DKJ read protected flag
13 = MACP over-written flag
14 = MACP on disk flag
15 = Queue access denied flag
16 = Queue full flag
17 = File found flag
18 = I openned queue flag
19 = TLP queue verification in progress flag
20 = No lamp flag
21 = No physical flag
22 = Verify restart flag
23 = Inhibit 25th bit processing

DG1T_USDAT1—User Data Block 1

Bit 0-7 = MEQL index
8-14 = First failing phase
15-17 = Input type data
18 = PA SMP TLP flag
19 = Force DRPP call at end of phase

DG1T_SCPD—DRPP Scatch Pad

DG1T_SCPD +1 - DG1T_SCPD +44

DG1T_TPCRL0—Tape Control 0

Bit 0-11 = Requested tape block
12 = File sequencing check
13 = Block sequence check flag
14 = Tape check pass flag
15-18 = Next disk block to be used

DG1T_TPCRL1—Tape Control 1

Bit 0-11 = Last block read
12-23 = Current tape block

DG1T_TPCRL2—Tape Control 2

Bit 0-11 = Lower bound tape block
12-23 = Upper bound tape block

DG1T_TPERRW—Tape Error Words

Bit 0 = End of file flag
1-2 = Comparative dummy block size
3-19 = Number of words read
20 = Beginning of tape flag

DG1A_LOCTID—Tape ID word

DG1A_LOCTRL—Locator Control Word

DG1A_LOCFN—Queue File Number

DG1A_TAFILE—Tape File Numbers

Bit 0-11 = Desired tape file number
12-23 = Current tape file sequences number

DG1A_ALWUTY—Queue Access Bits for Each Unit

DG1A_TRYNO—Locator or SP Attempt Number

Bit 0-1 = Input state item
2-4 = Locator attempts
5-7 = SP attempts
8-11 = Task number
12-19 = Save input channel ID

DG1A_ELAP—Time Elapsed During Tape Operation

Bit 0-11 = Maximum elapsed time
12-23 = Elapsed time

DG1A_OVLAP—Overall Elapsed Time

Bit 0-11 = Overall maximum elapsed time
12-23 = Overall elapsed time

DG1A_TAPERR—Tape Operation Error Word

Bit 0 = FSN does not agree with expected
1-3 = Output error code
4-7 = Reject error code
8 = TLP tape is empty
9 = Contents of LOCTID not in directory
10 = Tape OP error has occurred, retry
11 = SP encountered tape failure, retry
12 = Off-normal output code
13 = Off-normal success code
14 = Off-normal EOT code
15 = Immediate rejection has occured
16 = Invalid directory block
17 = Time out has occurred, retry
18 = Overall time out has occured, suspend
19 = Data block size error
20 = Block word count error
21 = Off-normal EOF encountered
22 = Off-normal BOT encountered

DG1A_TSKADL—Start Address of New Task (Low PRI)

DG1A_TSKADH—Start Address of New Task (High PRI)

DG1T_STLPB—Special TLP Block

DG1T_STLPB +1 through DG1T_STLPB +63

Processor Recovery Printouts

Processor Configuration Recovery [PCRV (ALEV, BLEV Reports)]

PCRV: A-LEVEL ENTRY (Full Version)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASA(H)	AC1ASA(L)
AC1SCA	AC1SDA	AC1CSC	AC1ILA	AC1PCR	AC1SR
AC1MCO	AC1MCP	AC1MCD(H)	AC1MCD(L)	PS1RVBOOT	CS1RVBOOT

PCRV: B-LEVEL ENTRY (Full Version)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASB(H)	AC1ASB(L)
AC1SCA	AC1SDA	AC1CSC	AC1ILA	AC1PCR	AC1SR
AC1MCO	AC1MCP	AC1MCD(H)	AC1MCD(L)	AC1INH	AC1INS

PCRV: FAILED (Full Version)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(L)	AC1FRS	AC1GRS	AC1JRS
AC1KRS	AC1LRS	AC1XRS	AC1YRS	AC1ZRS	AC1SR
AC1SC	PC1HISTORY	PC1OVER-RIDE(H)	PC1OVER-RIDE(L)	PC1FILL_ADDR	AC1PCR

PCRV: A-LEVEL ENTRY (Short Version)

AC1JR	AC1KR	AC1SCA	AC1CSC	AC1PCR	AC1SR
AC1MCO	AC1MCP	AC1MCD(H)	AC1MCD(L)		

PCRV: B REQ (Short Version)

AC1JR	AC1KR	AC1SCA	AC1CSC	AC1PCR	AC1SR

PCRV: FAILED (Short Version)

AC1JR	AC1KR	AC1SR	PC1HISSTORY	PC1OVER RIDE(H)	PC1OVER RIDE(L)

NOTE:

1. Printout is an analysis aid message.
2. Data descriptions can be found in datapool-defined locations or in CC interrupt data.
3. Printout for ‘‘B-Level Entry’’ and ‘‘failed’’ is full or short version according to PC states:

Actual PC State (Decimal)		Message Format
1 - 17	Non-Pump States & NO-OP	None
18 - 19	18 is First Pump from disk	Full
20 - 23	Pump States	Short
24 - 25	NO-OP States	None
26 - 31	Pump States	Short
32	NO-OP State	None
33 - 39	Pump States	Short
40 - 41	NO-OP States	None
42 - 47	Pump States	Short
48	NO-OP State	None
49 - 51	50 is Pumping Repeated PC	Full
52 - 55	REPC Pump States	Short
56 - 57	NO-OP States	None
58 - 63	REPC Pump States	Short

4. Printout for ‘‘A-Level Entry’’ is short for all PC states.
5. Operate MCC key ‘‘Restore Maintenance IO’’ to obtain the full version printouts.
6. Operate MCC key ‘‘Clear Utility Function’’ to inhibit printouts (This overrides MCC key ‘‘Restore Maintenance IO’’).
7. See I/O Manual for additional information.

Processor Configuration Recovery (PCRV) is a processor recovery concept that automatically tries every possible combination of the duplex units available to regain a sane simplex configuration. The different configurations are listed in Table 8-A—Processor Configuration State Table. Processor Configuration Recovery steps the processors, memories, and buses through the states until a working configuration is selected.

The Processor Configuration Recovery process may be started by any of the following:

- Called by the Software Integrity Phases
- Invoked by other fault recovery programs
- By timeout of the Processor Configuration Sanity timer (B level interrupt)
- Manual intervention from the MCC.

In the following example, Processor Configuration Recovery is started by the timing out of the Processor Configuration Sanity timer:

- A low level fault occurs. (C through K level interrupt)
- The appropriate fault recovery program is selected to isolate and correct the fault.
- At the point of interrupt, the Processor Configuration sanity timer is started.
- If the fault recovery program clears the trouble before the processor configuration sanity timer times out, Processor Configuration Recovery is not invoked; the Processor Configuration Sanity timer is reset.
- If the processor configuration sanity timer times out, a B level interrupt occurs; PCRV is started at state 1.
- After each time out, the processor configuration sanity timer is reset and restarted.

- If CC sanity tests pass, a sane configuration has been found, and the processor configuration sanity timer is reset.
- If CC sanity tests fail, the processor configuration sanity timer times out. The processor configuration state is incremented, and another configuration is selected. This condition repeats until a sane configuration is found.

Processor Configuration Recovery (PCRV) starts with minimal changes (switch CCs, then no change), then specifies the program store and the program store bus. After the first 7 attempts at processor configuration, pumping of the memory from the disk is done for each new configuration. Only the CC is forced via hardware; PSs, PSBs, CSs, CSBs, IFBs, and AUBs are forced via Boot ROM firmware. After State O'(77), repeated PCs occur as the state cycles back to O'(40), and repeated cycles on the upper states from O'(40) to O'(77). Repeated PCs continue until a working processor configuration is found, and software resets the processor configuration state counter to zero. Central control switching is done by the hardware at States 1, 4, 10, 20, 40, and 60 (during repeated PCs, the only CC switch is at State 60).

If Processor Configuration Recovery does not pull together, a working 1B Processor, manual intervention may be used to bring the system up via the MCC (with Hard and Soft A-level requests).

Table 8-A. 1B Processor Configuration State Table

State (Octal)	PS	PSB	CSB	IFB	AUB	Repeat PC	Switch CC	Comments
1	-	-	-	-	-	0	No	
2	-	-	-	-	-	0	Yes	If CC trouble bit not set
3	Toggle	-	-	-	-	0	No	Switch Base PS
4	0	0	-	-	-	0	No	PS0/PSB0
5	1	1	-	-	-	0	No	PS1/PSB1
6	0	1	-	-	-	0	No	PS0/PSB1
7	1	0	-	-	-	0	No	PS1/PSB0
10	0	0	0	1	0	0	No	Hash/Pump States
11	1	1	1	0	1	0	Yes	
12	0	1	0	1	0	0	No	
13	1	0	1	0	1	0	No	
14	0	0	1	1	0	0	No	
15	1	1	0	0	1	0	No	
16	0	1	1	1	0	0	No	
17	1	0	0	0	1	0	No	

See footnotes on last page of table.

Table 8-A. 1B Processor Configuration State Table (Contd)

State (Octal)	PS	PSB	CSB	IFB	AUB	Repeat PC	Switch CC	Comments
20	0	0	0	0	1	0	Yes	
21	1	1	1	1	0	0	No	
22	0	1	0	0	1	0	No	
23	1	0	1	1	0	0	No	
24	0	0	1	0	1	0	No	
25	1	1	0	1	0	0	No	
26	0	1	1	0	1	0	No	
27	1	0	0	1	0	0	No	
30	0	0	0	1	1	0	No	
31	1	1	1	0	0	0	No	
32	0	1	0	1	1	0	No	
33	1	0	1	0	0	0	No	
34	0	0	1	1	1	0	No	
35	1	1	0	0	0	0	No	
36	0	1	1	1	1	0	No	
37	1	0	0	0	0	0	No	

See footnotes on last page of table.

Table 8-A. 1B Processor Configuration State Table (Contd)

State (Octal)	PS	PSB	CSB	IFB	AUB	Repeat PC	Switch CC	Comments
40	0	0	0	0	0	0	Yes*	Repeated PC†
41	1	1	1	1	1	0	No	
42	0	1	0	0	0	0	No	
43	1	0	1	1	1	0	No	
44	0	0	1	0	0	0	No	
45	1	1	0	1	1	0	No	
46	0	1	1	0	0	0	No	
47	1	0	0	1	1	0	No	
50	0	0	0	1	0	1	No	Repeated PC
51	1	1	1	0	1	1	No	
52	0	1	0	1	0	1	No	
53	1	0	1	0	1	1	No	
54	0	0	1	1	0	1	No	
55	1	1	0	0	1	1	No	
56	0	1	1	1	0	1	No	
57	1	0	0	0	1	1	No	

See footnotes on last page of table.

Table 8-A. 1B Processor Configuration State Table (Contd)

State (Octal)	PS	PSB	CSB	IFB	AUB	Repeat PC	Switch CC	Comments
60	0	0	0	0	1	1	Yes	Repeated PC
61	1	1	1	1	0	1	No	
62	0	1	0	0	1	1	No	
63	1	0	1	1	0	1	No	
64	0	0	1	0	1	1	No	
65	1	1	0	1	0	1	No	
66	0	1	1	0	1	1	No	
67	1	0	0	1	0	1	No	
70	0	0	0	1	1	1	No	Repeated PC
71	1	1	1	0	0	1	No	
72	0	1	0	1	1	1	No	
73	1	0	1	0	0	1	No	
74	0	0	1	1	1	1	No	
75	1	1	0	0	0	1	No	
76	0	1	1	1	1	1	No	
77	1	0	0	0	0	1	No	Loop to O'(40) for repeated PC

* Switch CCs if not Repeated PC
† Repeated PC starts with O'(40) when cycle returns from state O'(77).

Processor Configuration Recovery Test Run and HASHSUM Results

PC1HISTORY	PC1OVERRIDE(H)	PC1OVERRIDE(L)	M_ADDR	M_DATA	M_ADDR
M_DATA	M_ADDR	M_DATA	M_ADDR	M_DATA	M_ADDR
M_DATA	M_ADDR	M_DATA	M_ADDR	M_DATA	M_ADDR

(Data block may contain up to 128 words)

PC1HISTORY—Tests Executed During Last PC State or Activate Override

Bit 0 = PU bus was switched by PC peripheral tests
1 = Unused
2 = Some transient CS was zeroed by PC
3 = PC was executed as part of a system reinitialization
4 = Call store bootstrap was requested
5 = Program store bootstrap was requested
6 = AU bootstrap was requested
7 = Hash sums were pumped due to a failure in the hash over hash check
8 = AU bus 0/1 (reset/set) was forced active by PC or activate override
9 = AU tests found a bad CS. CS bootstrap was re-executed
10 = AU tests found a bad PS. PS bootstrap was re-executed
12 = Transient data in CS 0 was zeroed by the PC
13 = Transient data in PS 0 was zeroed by the PC (always true for PC pump state or activate override)
14 = Core pump actions have been executed (entry was activate override, PC pump state, or phase of memory reinitialization)
15 = Phase entry to PC. PC circuit not inhibited
16 = Phase entry to PC. PC circuit was inhibited
17 = Phase entry to hash and correct memory. returns to phase program

PC1OVERRIDES(H)—Tests Bypassed or Overrides Requested in Last PC State or Activate Override

Bit 0 = Inhibit MUP restart on A-level and B-level
1 = Supervisory mode in utility system reinitialization
2 = Skip interface bus (IFB) access tests
3 = Inhibit diagnostic tests

PC1OVERRIDES(L)—Tests Bypassed or Overrides Requested in Last PC State or Activate Override

Bit 15 = System reinitialization completed using generic tape and a separate office data tape
16 = All nonbacked-up memory was zeroed
17 = Hash sum check of core data was bypassed
18 = CC sanity tests were bypassed
19 = Tape error correction inhibited during system reinitialization
20 = Map audits inhibited during system reinitialization
21 = Store maintenance tests were bypassed
22 = File stores were unconditionally restored with internal PESTs set
23 = Duplex file store failure specified during system reinitialization

M_ADDR—Address of Mutilated Fixed Core Data (Bit 0-23)

M_DATA—Invalid Contents of Address Mutilation (Bit 0-23)

Interrupt Data Register Layouts

The Interrupt Data Register Layouts are arranged in an alphabetical order without the AC1 (active) or ST1 (standby) prefix. The number following the register mnemonic is the buffer bus register number. Refer to Section 4, *Reading the Buffer Bus Registers* for instructions.

ABC—Auxiliary Buffer Control (317)
(Froze on Interrrupt)

Bit 0-3 = Parity bits received for the corresponding bytes in auxiliary buffer word, right (ABR) [DFRRP(0-3)1]
4-7 = Parity bits received for the corresponding bytes in auxiliary buffer work, left (ABL) [DFRLP(0-3)1]
8 = Fetch ASW response (DFASW1)
9 = Fetch ASW failure response (DFASWF1)

ACT—Auxiliary Activity Register (355)

Bit 0 = Processor configuration activity branch B (PCBACT)
1 = Program store activity branch (PSACT)
2 = Call store activity branch (CSACT)
3 = PU activity branch (PUACT)
4 = Millisecond clock activity branch (MCLACT)
5 = Processor configuration activity branch A (PCACT)
6 = Matcher activity branch (MAACT)
7 = Cycle clock and start/stop activity branch (CLKACT)
8 = CC read/write activity branch (RWACT)
9 = GCP source activity branch (PUSACT)
10 = IFB activity branch (IFACT)
11 = Cross-over buffer bus inhibit (XBBINH)
12 = CC identity: 0=CC0, 1=CC1 (R/O)(CC1ID)
13 = Peripheral unit control bus selection: 0=both busses, 1=same bus (PUCB)
14 = Invert ROM control parity (CINVPAR)
15 = Peripheral unit control bus polling select: 0=Bus0, 1=Bus1 (POCB)

AP—Address Parity Register (257)

Bit 0-3 = Parity over the corresponding byte of data address (DAP)
4-7 = Parity over the corresponding byte of fetch address (FAP)
8 = Parity over the fetch address control signals (FACP)

ASA—Interrupt Return Store A (230)

Bit 0-29 = Current program address for interrupt routines
30 = Homogeneity bit
31 = Condition code sign

ASB—Interrupt Return Store B (231)

Bit 0-31 = See ASA for bits layout

ASC—Interrupt Return Store C (232)

Bit 0-31 = See ASA for bits layout

ASD—Interrupt Return Store D (233)

Bit 0-31 = See ASA for bits layout

ASE—Interrupt Return Store E (234)

Bit 0-31 = See ASA for bits layout

ASF—Interrupt Return Store F (235)

Bit 0-31 = See ASA for bits layout

ASG—Interrupt Return Store G (236)

Bit 0-31 = See ASA for bits layout

ASH—Interrupt Return Store H (237)

Bit 0-31 = See ASA for bits layout

ASJ—Interrupt Return Store J (240)

Bit 0-31 = See ASA for bits layout

ASK—Interrupt Return Store K (241)

Bit 0-31 = See ASA for bits layout

BNCTL—Bus Node Control Register (000)

Bit 0 = ARM collection of BN stacks
1 = Memory addressing bus node special
2 = Invoke the DG snap function
3 = DGN use to enable segment number PS0 and CS14
6 = CS segmented memory enabled
7 = PS segmented memory enabled

BR—Buffer Register (377)

Bit 0-31 = Provides read/write access to the B-Register

BRS—Buffer Register Shadow (376)
(Froze on Interrrupt)

Bit 0-31 = Traps the contents of the B-Register at the time an error occurs

CCS(H)—Bus Control Status (H) (215)

Bit 24 = CC is active
25 = CC1, if not set CC0
26 = Routine matching is active in this CC
27 = CC stopped by active CC or MUP has halted CC

CCS(L)—Bus Control Status (L) (215)

Bit 0 = Send on program store bus 0
1 = Send on program store bus 1
2 = Receive on program store bus 0
3 = Send on call store bus 0
4 = Send on call store bus 1
5 = Receive on call store bus 1
6 = CC trouble flip-flop
7 = CC divorced flip-flop
8 = Send on peripheral unit write bus 0
9 = Send on peripheral unit write bus 1
10 = Receive on peripheral unit reply bus 0
11 = Receive on peripheral unit reply bus 1
12 = Attached processor interface 0 trouble
13 = Attached processor interface 1 trouble
14 = Send on interface 0 trouble
15 = Send on interface 1 trouble
16 = Receive on interface 0 trouble
17 = Receive on interface 1 trouble
18 = Auxiliary unit 0 activity flip-flop is set
19 = Auxiliary unit interface 0, trouble bus 0
20 = Auxiliary unit interface 1, trouble bus 1
21 = Auxiliary unit activity 1, flip-flop is set
22 = Auxiliary unit interface 1, trouble bus 0
23 = Auxiliary unit interface 1, trouble bus 1

CES—CC Error Summary Register (340)
(Froze on Interrrupt)

Bit 0 = Stack counter read operation (SCROP)
1 = Stack counter write operation (SCWOP)
2 = Data parity write error from CS (DPWECS)
3 = Data parity write error from PS (DPWEPS)
4-7 = Save B register generated parity bits
4 = B Register parity bit (0) on the ALU (SBRP0)
5 = B Register parity bit (1) on the ALU (SBRP1)
6 = B Register parity bit (2) on the ALU (SBRP2)
7 = B Register parity bit (3) on the ALU (SBRP3)
8 = ASW error on MMIO access (IFASWE)
9 = Parity error on MMIO response (IFPE)
10 = ASW Failure on MMIO access (IFASWF)
11 = PS ASW error (PSASWE)
12 = PS ASW failure (PSASWF)
13 = PS parity error right half (PSPER)
14 = PS parity error left half (PSPEL)
15 = CS ASW error (CSASWE)
16 = CS ASW failure (CSASWF)
17 = CS parity error (CSPE)
18 = ASW error on PROM access (RASWE)
19 = ASW failure on PROM access (RASWF)
20 = Parity error on right word read from PROM (RPER)
21 = Parity error on left word read from PROM (RPEL)
22 = CS maintenance control F/F (MTCCS)
23 = PS maintenance control F/F (MTCPS)

CLE—Clock Error Detect and Status (203)

Bit 0 = Unlatch clock error summary for clock the clock generator (CLKERR1)
1 = Active generator clock error bit (CKGAERR1)
2 = CC distribution clock error (CKDIERR1)
3 = Interface bus 0T4 distribution clock error (CKI0ERR)
4 = Interface bus 2T6 distribution clock error (CKI2ERR)
5 = Standby CC twisted ring cable (TRC) or cable fail error latched (CKGSERR)
6 = Standby CC TRC or cable fail error set (CKSGERR)
7 = Clear clock errors bits (CLRCKER)
8 = Test to set 0T4 motion detector to 0 (TMOT40)
9 = Test to set 0T4 motion detector to 1 (TMOT41)
10 = Test to set 1T5 motion detector to 1 and 2 to 0 (TMOT50)
11 = Test to set 1T5 motion detector to 1 and 2 to 0 (TMOT51)
12 = Test to set 2T6 motion detector to 1 and 2 to 0 (TM2T60
13 = Test to set 2T6 motion detector to 1 and 2 to 1 (TM2T61)
14 = Test to set 3T7 motion detector to 1 and 2 to 0 (TM3T70)
15 = Test to set 3T7 motion detector to 1 and 2 to 1 (TM3T71)
16 = Test to set 0T4 motion detector 3 to 0 (TMOT40A)
17 = Test to set 0T4 motion detector 3 to 1 (TMOT41A)
18 = Test to set 1T5 motion detector 3 to 0 (TMOT50A)
19 = Test to set 1T5 motion detector 3 to 1 (TMOT51A)
20 = Test to set 2T6 motion detector 3 to 0 (TM2T60A)
21 = Test to set 2T6 motion detector 3 to 1 (TM2T61A)
22 = Test to set 3T7 motion detector 3 to 0 (TM3T70A)
23 = Test to set 3T7 motion detector 3 to 1 (TM3T71A)

CSC—CC Status Flip-Flops (351)

Bit 0 = PS bus control—Active send on both (R/O)(PBO)
1 = PS bus control—Active bus (R/O)(PBA)
2 = PS bus control—Standby bus trouble (R/O)(PBT)
3 = CS bus control—Active send on both (R/O)(CBO)
4 = CS bus control—Active bus (R/O)(CBA)
5 = CS bus control—Standby bus trouble (R/O)(CBT)
6 = CC activity flip-flop (R/O)(CCACT)
7 = CC trouble standby flip-flop (R/O)(TCC)
8 = CC divorce mode (R/O)(DIV)
9* = PUBO—Coded enable PU bus control—Active send on both (R/O)(PUBO)
10* = PUBA—Coded enable PU bus control—Active bus (R/O)(PUBA)
11* = PUBT—Coded enable PU bus control—Standby bus trouble (R/O)(PUBT)
12* = PUBR—Coded enable PU bus control—Active Received on both (R/O)(PUBR)
13 = Processor activity status for PBO (PBOS)
14 = Processor activity status for CBO (PCOS)
15 = Processor activity status for DIV (DIVS)
21 = Call store program flip-flop (CSPGM)
22 = Freeze stop or clear stop indicator (FSTPTP)
1 = Maintenance matcher freeze-stop standby
0 = Standby CC will receive a clear-stop

* See CC to PUB Routing Table

CC to PUB Routing via CSC Bits (PUBR, PUBT, PUBA, PUBO)

Bit 12 PUBR	Bit 11 PUBT	Bit 10 PUBA	Bit 9 PUBO	Active CC		Standby CC	
				Send Bus	**RCV Bus**	**Send Bus**	**RCV Bus**
0	0	0	0	0	0	1	1
0	0	0	1	0 & 1	0	None	1
0	0	1	0	1	1	0	0
0	0	1	1	0 & 1	1	None	0
0	1	0	0	0	0	None	0
0	1	0	1	0 & 1	0	None	0
0	1	1	0	1	1	None	1
0	1	1	1	0 & 1	1	None	1
1	Don't Care	Don't Care	Don't Care	0 & 1	0 & 1	None	0 & 1

NOTE:
Both active and standby CCs should have the same values for PUBR, PUBT, PUBA, and PUBO but are interpreted differently as shown in the preceding table.

CUI—CC Utility Interface Register (211)

Bit 0-8 = CC utility interface address bits (CUIA)
9-16 = CC utility interface data bits (CUID)
17 = CC utility interface read/write bit (CUIR1WO)
18 = CC utility interface busy (CUIBSY)

DLR—Delay-Limited-Run Register (356)

Bit 0-7 = Delay following trigger before standby CC begins running (DELAY)
8-15 = Number of instruction cycles which the standby CC runs (LIMIT)
16 = CC freeze-stop after mismatch (standby CC only)(MFSTPFF)
17 = CC clear-stop after mismatch (overrides freeze-stop)(MCSTPFF)
18 = CC was freeze-stopped (R/O)
19 = Freeze-stop standby CC only (W/O)(FSTP)
20 = CC was clear-stopped (R/O)
21 = Clear-stop standby CC only (W/O)(CLSTP)
23 = Start standby CC (W/O)(START)

ELIT—End of Interrupt Long Interval Timer

Bit 0-23 = Elapsed interrupt time

EPS—Execution Pipeline State (334)

Bit 0 = DAR read request (CDARRQ)
1 = DAR write request (CDARWQ)
2 = DAR maintenance request (CDARMQ)
3 = DAR control request (CDARCQ)
4 = DAR control signal parity (CDARPQ)
5 = DAR GCP request (CDARGQ)
6 = DAR store secure (CDARSS)
7 = Data port is stack request (CDPSTK)
8 = DIR 0 active (CDIR0A)
9 = DIR 0 "Read" GOT bus (CDIR0GB)
10 = DIR 1 Active (CDIR1A)
11 = DIR 1 "Read" GOT bus (CDIR1GB)
12 = Operational interrupt hold (CINHJ)
13 = Data port protected area check flag (DPPACH)

ER—E-Register—Peripheral Unit Enable Register (200)

Bit 10-16 = Peripheral unit member (Member)
17-21 = Peripheral unit type (Bits 10-21 from the enable address)(PUTYPE)

FCE—IFBC Client Enable Register (361)

Bit 0-15 = Enable client 00 through 15 request
19 = Enable FLD/FLT shadow register access
20-23 = FLD/FLT shadow register address

FCT—IFBC Control Register (360)

Bit 0 = Poll operational interjects
1 = Poll maintenance interjects
2 = Poll maintenance interrupts
3 = Enable IFB operational interjects
4 = Enable IFB maintenance interrupts
5 = Spare
6 = Request near client 0 block
7 = Request near client E client-to-client
8 = Request near client C word
9 = Request far client 2 block
10 = Request far client 6 client-to-client
11 = Request far client 8 word
12 = DMA suspended by interrupt (read only)
14 = Test request enable
15 = IFB0 to IFBC enable
16 = IFB1 to IFBC enable
18 = IFBC to IFB0 enable (pulse)
19 = IFBC to IFB1 enable (pulse)
21 = Clear IFBC errors (pulse)
22 = IFBC errors interlock
23 = IFBC master reset (pulse)

FEE—IFBC Error Enable Register (363)

Bit 0 = IFB0 control error
1 = IFB0 address parity error
3 = IFB1 control error
4 = IFB1 address parity error
6 = MMIO control error
7 = MMIO address parity error
9 = IFBC arbiters mismatch
10 = IFB grant timeout
11 = Arbiter state invalid
12 = Store write parity error during DMA
13 = Multiple client requests
15 = Invalid client master reply code
16 = Invalid client slave reply code
18 = ASW/ASF error during DMA
19 = Enable FLA shadow register access
20-23 = FLD/FLT shadow register address

FER—IFBC Error Request Register (364)

Bit 0 = IFB0 control error
1 = Memory control bit
3 = IFB1 control error
4 = Memory maintenance bit
6 = MMIO control parity error
7 = Spare
9 = IFBC arbiters mismatch (override CDIV1)
10 = IFB grant timeout
11 = Arbiter state invalid
12 = Spare
13 = Multiple client requests
15 = Invalid client master reply code
16 = Invalid client slave reply code
18-21 = Generate address parity error, byte 0 through 3
22 = Examine near non-responding bus

FES—IFBC Error Source Register (362)

Bit 0 = IFB0 control error
1 = IFB0 address parity error
3 = IFB1 control error
4 = IFB1 address parity error
6 = MMIO control error
7 = MMIO address parity error
9 = IFBC arbiters mismatch
10 = IFB grant timeout
11 = Arbiter state invalid
12 = Store write parity error during DMA
13 = Multiple client requests
15 = Invalid client master reply
16 = Invalid client slave reply
18 = ASW/ASF error during DMA
19-20 = Spare
22 = Client maintenance interrupt active
23 = IFBC error detected

FIP—IFBC Interrupt/Interject Poll Register (366)

Bit 0-23 = Client interrupt/interject active (client 00 through 23)
29 = Copy of FCT.OU_POL (matcher/monitor store only)
30 = Copy of FCT.MU_POL (matcher/monitor store only)
31 = Copy of FCT.MIN_POL (matcher/monitor store only)

FIS—Fetch-Index State Register (332)

Bit 0 = CCFF homogeneity bit (CCCFFH)
1 = CCFF sign bit (CCCFFS)
2 = Test complete indicator (CTCOMP)
3 = Set index register select and index adder to pass "T" (CTPASS)
4 = First fetch of transfer issued (CTFFI)
5 = Last cycle memory transaction was "read" (CLCMTR)
6 = Relative addition of double index done (CRELDON)
7 = Buffer order word, left (BOL) register contents valid instruction word (CBOLV)
8 = Buffer order word, right (BOR) register contents valid instruction word (CBORV)
9 = Last instruction was "execute" (CLIWE)
10 = Pipeline mode switch [If 0 indicates processor running in linear mode (CURLIN0)]
11 = GCP instruction delay (CGCPDLY)
12 = Lock initiated (potential couplet)(FISLOCK)
13 = Locked "Write" in execution pipeline (EPSLOCK)

FLA—IFBC Last Transfer Address Register (367)

Bit 0-29 = IFB last transfer address bits 00 through 29 (shadowed)

FLD—IFBC Last Transfer Data Register (370)

Bit 0-31 = IFB last transfer data bits 00 through 31 (shadowed)

FLT—IFBC Last Transfer Type Register (371)

Bit 0-3 = Near IFBC last client granted
4 = Near IFBC granted block DMA
5 = Near IFBC granted word DMA
6 = Near IFBC granted client to client
7 = Near IFBC granted MMIO
8-11 = Far IFBC last client granted
12 = Far IFBC granted block DMA
13 = Far IFBC granted word DMA
14 = Far IFBC granted client to client
15 = Far IFBC granted MMIO
16-19 = Next client to be granted
20 = Next client requesting block DMA
21 = Next client requesting word DMA
22 = Next client requesting client to client
23 = Last cycle was read (shadowed)
24 = Last cycle was write (shadowed)
25 = Current cycle active on IFB0 (shadowed)
26 = Current cycle active on IFB1 (shadowed)
27-30 = IFB data parity bit 0 through 3 (shadowed)
31 = IFBC is active

FR—F-Register (260)

Bit 0-31 = F-Register

FRL—IFBC Relocation Lower Register (373)

Bit 0-23 = MMIO relocation address (bits 00 through 23)
29-31 = MMIO relocation address parity (bit 0 through 2)

FRS—F-Register Shadow Register

Bit 0-31 = F-Register Shadow Register

FRU—IFBC Relocation Upper Register (372)

Bit 18-23 = MMIO relocation address (bits 24 through 29)
31 = MMIO relocation address parity (bit 3)

FST—IFBC Status Register (365)

Bit 0 = IFB0-IFBC output enabled
1 = IFB1-IFBC output enabled
2-5 = IFB address parity (shadowed)
6 = IFB0 operation interject active
7 = IFB0 maintenance interject active
8 = IFB0 maintenance interrupt active
9 = IFB1 operation interject active
10 = IFB1 maintenance interject active
11 = IFB1 maintenance interrupt active
12 = IFB0 no client slave reply
13 = IFB1 no client slave reply
14 = IFB0 valid client slave reply
15 = IFB1 valid client slave reply
16-21 = Client slave reply code (bits 0 through 5)
22 = IFB0 no client master reply
23 = IFB1 no client master reply
24 = IFB0 valid client master reply
25 = IFB1 valid client master reply
26-31 = Client master reply code (bits 0 through 5)

GR—G-Register (261)

Bit 0-31 = G-Register

GRS—G-Register Shadow Register

Bit 0-31 = G-Register Shadow Register

IBR—Inhibit Buffer Bus Read Flip-Flops (345)

Bit 1 = Inhibit buffer bus read of control board 1 (CB1)(IBRBA)
2 = Inhibit buffer bus read of maintenance matcher (MM)(IBRBB)
3 = Inhibit buffer bus read of fetch index (FI)(IBRBC)
4 = Inhibit buffer bus read of fetch address (FA)(IBRBD)
5 = Inhibit buffer bus read of control board 2 (CB2)(IBRBE)
6 = Inhibit buffer bus read of interface bus control (IFBC)(IBRBF)
7 = Inhibit buffer bus read of MCC/utility interface (MUI)(IBRBG)
8 = Inhibit buffer bus read of general registers (GNRG & ALU)(IBRBH)
9 = Inhibit buffer bus read of execution decode (XDEC)(IBRBJ)
10 = Inhibit buffer bus read of clock and utilities (CKUT)(IBRBK)
11 = Data port access of MMIO (IFDP)
12 = Inhibit buffer bus read of bus node address (BNAD)(IBRBL)
14 = Inhibit grant of call store bus (INCS)
15 = Inhibit grant of program store bus (INPS)
16 = Data port access of call store (CSDP)
17 = Fetch port access of call store (CSFP)
18 = Call store was accessed (CSACC)
19 = Data port access of program store (PSDP)
20 = Fetch port access of program store (PSFP)
21 = Program store was accessed (PSACC)
22 = Data port access of PROM (PRDP)
23 = Fetch port access of PROM (PRFP)

IFR—Instruction Fetch State Register (273)

Bit 0-2 = Pipeline state. (State 7 is illegal) [PS(0-2)]
3 = Indirect transfer has fetched destination address word (INDIR1F1)
4 = Indirect transfer has fetched destination instruction word (INDIR2F1)

ILA—Interrupt Level Activity Flip-Flops (341)

Bit 0-9 = Interrupt level activity F/FS A-K levels ILA(A-K)
10 = A- on B-level interrupt (AOB)
11 = Interrupt level activity hard "A" source (MCHAO)
12 = Interrupt level activity soft "A" source (MCPAO)
13 = Interrupt level activity utility "A" source (UTASO)

ILR—Interrupt Level Request Register (342)

Bit 0-9 = Interrupt level request register A-K ILR(A-K)
10 = Modify interrupt address F/F (MOIA)
11 = Deferred interrupts F to K inhibited (INI)
12-15 = Diagnostic wait state sequencer (NMRD)(NMWE) (UTLR)(UTSY)

INH—Interrupt Inhibit Register (343)

Bit 0 = J-Level source inhibit (IJS)
1 = H-Level source inhibit (IHS)
2 = G-Level source interval timer inhibit (IIVTGS)
3 = G-Level source—Utility or directed match inhibit (IMGS)
4 = APUFS F-Level source autonomous PU failure inhibit (IAPUFS)
5 = PUFS F-Level source—Peripheral unit failure inhibit (IPUFS)
6 = E-Level source program store inhibit (IES)
7 = D-Level source stack overflow inhibit (ISCDS)
8 = D-Level source—Protected area failure inhibit (IPADS)
9 = D-Level source—IFB D-level inhibit (IIFDS)
10 = D-Level source—Call store failure inhibit (ICSDS)
11 = B-Level pulse source inhibit (IPSBS)
12 = Utility A-Level interrupt inhibit (IUTAS)
13 = Inhibit out-of-range D-Level source (IORDS)
14 = B-Level internal error inhibit (IINBS)
17 = K-Level source 0 inhibit excessive time (IKL0S)
19 = Immediate interrupt (R/O)(INTIMM)
20 = Interrupt initializing state bit (R/O)(INT)
21 = Freeze flip-flop (R/O)(FREZ)
22 = Inhibit setting of ASWEPU flip-flop (IASWEPU)
23 = Inhibit setting of APEPU flip-flop (IAPEPU)

INJ —Interject Request Register (344)

Bit 9 = Software interject source set (SINJ)
10 = Software interject source reset (W/O)(CLRSINJ)
11 = Interface bus maintenance interject source set (IFMINJ)
12 = Interface bus maintenance interject source reset (W/O)(CLIFMINJ)
13 = APU interject source set (APINJ)
14 = APU interject source reset (W/O)(CLRAPINJ)
15 = Interval timer interject source set (IVINJ)
16 = Interval timer interhect source reset (W/O)(CLRIVINJ)
17 = Operational interject source set (IFOIJ)
18 = Operational interject source reset (W/O)(CLRIFOIJ)
19 = Interject activity (INJA)
20 = Inhibit interval timer interject source (IIVINJ)
21 = Inhibit software interject source (ISINJ) (Always set for 4ESS switch)
22 = Inhibit APUT interject source (IAPUT)

INS—Interrupt Source Register (346)

Bit 0 = J-Level source (JLS)
1 = H-Level source (HLS)
2 = G-Level source—Interval timer (IVTGS)
3 = G-Level source—Utility or directed match (MGS)
4 = F-Level source—Autonomous unit failure (APUFS)
5 = F-Level source—Peripheral unit failure (PUFS)
6 = E-Level source—Program store failure (ELS)
7 = D-Level source—Stack overflow (SCDS)
8 = D-Level source—Protected area failure (PADS)
9 = D-Level source—IFB D Source failure (IFDS)
10 = D-Level source—Call store failure (CSDS)
11 = C-Level source—Match error (CLIS)
12 = Utility A-Level source (UTAS)
13 = D-Level source—Out of range (ORDS)
14 = B-Level source—Internal error (INBS)
15 = B-Level source—Pulse source error BUF (PSBSO)
16 = MCC Program soft A-Level (MCPAS)
17 = MCC hard A-Level source (MCHA)
18 = B-Level source—Pulse source failure (PSBS)
19 = B-Level processor configuration failure (PCBS)
20 = K-Level source 0—Excessive time (KL0S)
21 = Switch CC B-Level (SWBO)
22 = PROM parity or ASW B-Level (RBSO)
23 = Control parity B-Level (CPBSO)

ITR—Interval Timer Register (347)

Bit 0-8 = Read/write access to interval timer counter (IVT)
9 = Read (0)/write (1) interval timer control bit (DIRECT)
10 = Interval timer "go" flip-flop set (ITGO)
11 = Clear interval timer "go" flip-flop (CLRITGO)
12-21 = Lower address bits from last buffer bus read or write operation (R/O) (SCC)
22 = Saved CC address was a "read" (bit=0) operation or "write" (bit = 1) operation (R/O) (SCCR/W)
23 = Saved CC address via utility system (UEXEC)

JR—J-Register (266)

Bit 0-31 = J-Register

JRS—J-Register Shadow Register

Bit 0-31 = J-Register Shadow Register

KR—K-Register (262)

Bit 0-31 = K-Register

KRS—K-Register Shadow Register

Bit 0-31 = K-Register Shadow Register

LHIN—Left-Half Failure Instruction

Bit 0-23 = Left-Half Failure Instruction

LIT—Long Interval Timer (357)

Bit 0-17 = Long interval timer (LIT)
18-23 = IOCH clock counter (IOCH)

LPA—Lower Protected Area Bound (255)

Bit 12-29 = Call Store protected area lower range

LPI—Address of Last Peripheral Instruction (272)

Bit 0-29 = Address of last peripheral instruction

LR—L-Register (374)

Bit 0-31 = L-Register

LRS—L-Register Shadow Register

Bit 0-31 = L-Register Shadow Register

MCD—MCC Direct Data Insert Register (214)

Bit 0-31 = See layout for Direct Data Insert Keys Identification

MCLK—Millisecond Clock (350)

Bit 0-15 = Millisecond clock (MCL)
16-23 = IOCL clock counter (IOCL)

MCO—MCC Processor Override Register (213)

Bit 0 = Force CC 0 active (MCCC0)
1 = Force CC 1 active (MCCC1)
2 = Load program store 0 (MCPS0)
3 = Load program store 1 (MCPS1)
4 = Load call store 0 and 2 (MCCS0)
5 = Load call store 1 and 3 (MCCS1)
6 = Configure the active CC to use PS bus 0 (MCPSB0)
7 = Configure the active CC to use PS bus 1 (MCPSB1)
8 = Configure the active CC to use CS bus 0 (MCCSB0)
9 = Configure the active CC to use CS bus 1 (MCCSB1)
10 = Configure the active CC to boot using IFB 0 (MCIFB0)
11 = Configure the active CC to boot using IFB 1 (MCIFB1)
12 = Configure the active CC to use file server 0 (MCFS0)
13 = Configure the active CC to use file server 1 (MCFS1)
14 = Load the system from tape—Utility mode (MCLFTU)
15 = Load the system from tape—Normal mode (MCLFTN)
16 = Load the system from disk (MCLFD)
17-20 = Unused
21 = SR ready from the TUC (R/O) (READY)
22 = Disable auto PC state flop-flop (MCDISAPC)
23 = MCC data is valid when bit is set (MCCVALID)

ME0—External Match Register 0 (321)

Bit 0-29 = Data is updated from the AFAN bus (active CC) or ADAN bus (standby CC)
30-31 = Updated with 0 in normal operation, but buffer-bus writable to any value

ME1—External Match Register 1 (323)

Bit 0-31 = Data is updated from DADB bus (active CC) or the DBR bus (standby CC)

MI0—Internal Match Register 0 (320)

Bit 0-29 = Data is updated from the AFAN bus (active CC) or ADAN bus (standby CC)
30-31 = Updated with 0 in normal operation, but buffer-bus writable to any value

MI1—Internal Match Register 1 (322)

Bit 0-31 = Data is updated from DBR bus (active CC) or the DADB bus (standby CC)

MCP(L)—MCC A-Level Program Request Register (212)

Bit 0-5 = MCC program request phases 1-6
6 = MCC inhibit interrupt sources
7 = MCC clear utility match condition
8-12 = MCC auxiliary program
8 = MCC emergency mode minimum request
9 = MCC emergency mode minimum request
10 = MCC modified recovery action
11 = MCC restore maintenance I/O request
12 = Unused
13 = Restore system from normal program file
14 = Restore system from update program file
15 = Utility inhibit switch
16 = Force both MCC/utility processor active
17 = MUP in active-active status
18 = MUI address parity error
19 = MUI data parity error
20 = MUI detected invalid address
21 = Force enable flip-flop
22 = MC3 relay in NMDCF—Read only
23 = Near MUP active

MMR—Match Mode Control Register (324)

Bit 0 = Enables routine matching on actice CC
1 = Enables routine matching on standby CC
2 = Stop standby signal is generated whenever the internal error flag is set to 1
3 = Inhibit the update of the error latches in MSR
4 = Inhibit the update of the match registers (MI0, MI1, ME0 and ME1)
12 = Enables the generation of a C-level interrupt request when a match error occurs
18 = Inhibits the setting of the external matcher 0 error (M0E1) latch
19 = Inhibits the setting of the external matcher 1 error (M1E1) latch

MSR—Match Summary Register (325)

Bit 0 = Indicates that matching is active, if set to 1 (MACT1)
1 = Internal error flag (MLIERR1)
2 = External error flag (MLEERR1)
10 = Internal matcher 0 mismatch latch (M0E1)
11 = External matcher 0 mismatch latch (M0E1)
12 = Internal matcher 1 mismatch latch (M1I1)
13 = External matcher 1 mismatch latch (M1E1)
16 = Internal matcher 0 direct (unlatched) output (MA0I1)
17 = External matcher 0 direct (unlatched) output (MIN01)
18 = Internal matcher 1 direct (unlatched) output (MA1I1)
19 = External matcher 1 direct (unlatched) output (MIN11)

PCR—Processor Configuration Register (354)

Bit 0-5 = Processor control state counter (PCC)
6 = Enable PC sanity timer (EPCS)
7 = Inhibit normal refresh of analog timer (CANTI)
8 = Program sanity timer error trigger (PSTET)
9 = PC sanity time-out trigger (PCSTO)
10 = Deliberate trigger (DLIB)
11 = Analog time-out trigger (ATO)
12 = Active-active or standby-standby trigger occurred (ACTM)
13 = Clock error trigger (CKE)
14 = MCC trigger occurred (MCCTO)
15 = Repeated PC state occurred (REPC)

PES—Peripheral Unit Error Summary (302)

Bit 0 = All seems well from PU reply bus 0 (ASW0PU)
1 = All seems well from PU reply bus 1 (ASW1PU)
2 = Answer parity from PU reply bus 0 (PUF) (AP0PU)
3 = Answer Parity from PU reply bus 1 (PUF) (AP1PU)
6 = PU ASW error summary (PUF) (ASWEPU)
7 = PU answer parity error summary (PUF) (APEPU)
8 = Autonomous PU base level report (APUB)
9 = Autonomous peripheral unit trouble (APUT)
10 = CPD/Coded enable instruction just executed
(1=CODED)(CPDKC)
11 = Parity over write bus odd bits (R/O)(PWP1)
12 = Parity over write bus even bits (R/O)(PWP2)
13 = Inhibit all seems well (PU matchers) (R/O)(INHASW)
14 = Inhibit answer parity (PU matchers) (R/O)(INHAP)
16 = Reply mismatch error-PU GCP instruction (PUF) (RMEGCP)
17 = Reply mismatch error-PU instruction (PUF) (RMEPU)

PM0—Peripheral Unit K-Code Matcher 0 (300)

Bit 0-6 = Member number mask:
1=same bit in MK field will not match (MNK)
10-16 = Member number field (MK)
17-21 = Unit type number
(bits 10-21 match bits 10-21 in
E-register)(UTYN)
22 = Inhibit ASW failure when match occurs (IASWE)
23 = Inhibit answer parity errors when match occurs (IAPE)

PM1—Peripheral Unit K-code Matcher 1 (301)

Bit 0-6 = Member Number Mask:
1=same bit in MK field will not match (MNK)
10-16 = Member number field (MK)
17-21 = Unit type number
(bits 10-21 match bits 10-21 in
E-register)(UTYN)
22 = Inhibit ASW failure when match occurs (IASWE)
23 = Inhibit answer parity errors when match occurs (IAPE)

PRL—P-Register—Least Significant Bits (202)

Bit 0-23 = P-Register bits 0-23

PRM—P-Register—Most Significant Bits (201)

Bit 0 = P-Register bit 24
1 = P-Register bit 25
2 = P-Register bit 26
3 = P-Register bit 27
4 = P-Register bit 28
5 = P-Register bit 29
6 = P-Register bit 30
7 = P-Register bit 31
8 = P-Register bit 32
9 = P-Register bit 33
10 = P-Register bit 34
11 = P-Register bit 35

PSC—Peripheral Sequencer Control (303)

Bit 1 = Scanner response (input order)(SCR)
2 = Answer parity enable (APEN)
3 = Inhibit PU reply window (IW)
4 = Invert PU write parity P2 (IP2)
5 = Invert PU write parity P1 (IP1)
6 = Inhibit enable address sync (IS)
7 = L-Register usage determines window closure (instead of ASW)(LUDWC)
8 = MBIT/MTCPU, Maintenance PU (MTCPU)
9 = PU instruction inhibit (PINH)
10 = L-Register inhibit (LINH)
11 = Start coded enable sequencer (SCEQ)
12-16 = Coded enable sequencer state (CEQF)
17 = Coded enable PU order completed (PUOC)
18 = Peripheral pulse source (PPS)

PSQ—PU Sequencer Auxiliary Counter (306)

Bit 0-2 = CEQ state timer (TCTMR)
3-10 = Re-encoded GCP signal (R/O)(AMTCH)

RHIN—Right-Half Failure Instruction

Bit 0-23 = Right-Half Failure Instruction

RP0—PU Reply Bus 0 One(s) Catcher (304)

Bit 0-23 = Peripheral unit reply bus 0 one(s) catcher (R/O)

RP1—PU Reply Bus 1 One(s) Catcher (305)

Bit 0-23 = Peripheral unit reply bus 1 one(s) catcher (R/O)

SAL—Save Auxiliary—Left (330)
(Froze on Interrrupt)

Bit 0-31 = Same data as ABL

SAR—Save Auxiliary—Right (331)
(Froze on Interrrupt)

Bit 0-31 = Same data as ABR

SAT—Sanity Timers (352)

Bit 0-5 = Program sanity timer (PST)
6 = Reset program sanity timer enable (PSTE)
7-11 = Processor configuration sanity timer (PCST)
15 = CC Activity state (R/O) (CACTS)

SC—Stack counter (254)

Bit 0-5 = Stack counter

SCA—Saved Current Address (252)

(Froze on Interrrupt)

Bit 0-29 = Contains the values of CAR corresponding to the last 16 instructions that has gone through the indexing state
30 = Instruction was sent to DIR0 for execution
31 = Instruction was sent to DIR1 for execution

SCTR—Contents of Stack Counter + 1

SDA—Saved Data Address (271)

(Froze on Interrrupt)

Bit 0-29 = Contains the history of the addresses in DAR during the last 16 events in the execution pipeline
30-31 = Type of operation:

0 0 = GCP
0 1 = READ
1 0 = WRITE
1 1 = Non-memory operation

SEGCTL—Segment Memory Control

Bit 0 = CS segmented enabled shadow (CSSEGS1)
1-4 = CS segment number last enabled (SEGNOCS)
5 = PS segmented enabled shadow (PSSEGS1)
6 = PS segment number last enabled (SEGNOPS)
7 = SEGCTL data valid when reset (SCTLINVD)

SR—Stack register (267)

Bit 0-31 = Stack register bits 0-31

TAR—Transition Address Register (333)

Bit 23-29 = Provides the 1B24 with access to the high-order address bus

ULR—Unsuccessful L-Register Response from PU Instruction

Bit 0-23 = Unsuccessful L-Register Response

UPA—Upper Protected Area Bound (256)

Bit 12-29 = Call store protected area upper range

XR—X-Register (263)

Bit 0-31 = X-Register

XRS—X-Register Shadow Register

Bit 0-31 = X-Register Shadow Register

YR—Y-Register (264)

Bit 0-31 = Y-Register

YRS—Y-Register Shadow Register

Bit 0-31 = Y-Register Shadow Register

ZR—Z-Register (265)

Bit 0-31 = Z-Register

ZRS—Z-Register Shadow Register

Bit 0-31 = Z-Register Shadow Register

CC/AU- Central Control/Auxiliary Unit

Central Control Bus Node Data - Active

BNA_WD0(000)	BNA_WD1(000)	BNA_WD2(000)	BNA_WD0(001)	BNA_WD1(001)	BNA_WD2(001)
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
BNA_WD0(040)	BNA_WD1(040)	BNA_WD2(040)	BNA_WD0(041)	BNA_WD1(041)	BNA_WD2(041)

NOTE:
Each part contains a variable list report from entry 000 to 041 where entry 000 is the oldest in time and entry 041 is the most recent in time

BNA_WD0—Bus Node Arbiter Word 0

Bit 0-5 = Upper bits of the port address
6 = Read control signal
7 = Control parity signal
8-9 = Port identification information Number Port Identification
- 0 - Data Node Access (DNA)
- 1 - Index Node Access (XNA)
- 2 - Fetch Node Access (FNA)
- 3 - Interface Buffer Access (IBA)

10-17 = Control bits for **CC based** on active port identification information
- 0 - Write control signal from the data node
- 1 - Maintenance control signal from the data node
- 2 - Control signal from the data node
- 3 - GCP control signal from the data node
- 4 - Control signal from the index node
- 5 - Write request signal from the data node
- 6 - Interface Bus grant to data node

10-17 = Control bits for **IFB based** on active port identification information
- 0 - Write control signal from the Interface Bus Controller
- 1 - Maintenance control signal from the Interface Bus Controller
- 2 - Control signal from the Interface Bus Controller
- 3 - Word DMA request from the Interface Bus Controller

BNA_WD0—Bus Node Arbiter Word 0 (Contd)

Bit 18-20 = Access identification information
0 - NA
1 - CS
2 - PS
3 - PROM
4 - MMIO
5 - Buffer Bus

23 = Entry valid bit used by software
0 - Invalid
1 - Valid

BNA_WD1—Bus Node Arbiter Word 1

Bit 0-23 = Address on the port

BNA_WD2—Bus Node Arbiter Word 2

Bit 0-5 = Bus Node operation results
0 - All Seems Well (ASW)
1 - Data Parity Failure (DPF)
2 - All Seems Well Failure (ASWF)
3 - Node Attempted Illegal Access (NAIA)
4 - Control Parity B Source (CPBS)
5 - Controller or Client D Source (CLIDS)

6-13 = Number of the entry in the raw data bin. This number can be used to identify what ports were active at the same time
14-16 = Internal fault recovery results
17 = PS segment number
18-21 = CS segment number
22 = PS segmenting enabling
23 = CS segmenting enabling

Central Control Execution Pipeline History-Active

SCA(00)	SDA_H(00)	SDA(00)	EPH_RESULT(00)
.	.	.	.
.	.	.	.
.	.	.	.
SCA(15)	SDA_H(15)	SDA(15)	EPH_RESULT(15)

NOTE:
Entry 00 is the oldest in time and entry 15 is the most recent in time

SCA—Saved Current Address

Bit 0-23 = The address of an instruction that left indexing

SDA_H—Saved Data Address (High order bits)

Bit 0-6 = The high order bits of the 30 bit SDA. The complete data address is determined by concatenating SDA_H with SDA

SDA—Saved Data Address (Low order bits)

Bit 0-23 = The low order bits of the 30 bit SDA. The complete data address is determined by concatenating SDA_H with SDA

NOTE:
The data address (from concatenation for SDA_H and SDA) applies only when the SDA/EPH valid bit is set in the ***EPH_RESULT*** field. A valid SDA entry must be confirmed with the source listing to verify that the SDA applies to the SCA

EPH_RESULT— Execution Pipeline History Result. Applies only when the SDA/EPH valid bit is set in the ***EPH_RESULT*** field. This word represents the different pipeline states and completion of an instruction located at SCA.

Bit 0 = Instruction completion bit. If set, instruction was determined to have completed. If not set, instruction completion could not be determined.

3-7 = Final pipeline state of the instruction. A list of execution pipeline states (octal) are as follows:

000 - Nothing happened during this clock cycle. The pipeline may be empty or an instruction is stalled in decoded instruction Register 0. The instruction in indexing could be blocked waiting for another condition to clear, or we could be waiting for an instruction fetch to provide an instruction to indexing.

002 - The instruction in indexing was loaded into decoded instruction Register 1 since decoded instruction Register 0 is not available.

004 - The instruction in decoded instruction Register 0 has completed, but there is no instruction in either decoded instruction Register 1 or an index only instruction to execute. Therefore, the empty word is clocked into decoded instruction Register 0.

005 - The instruction in indexing was loaded into decoded Register 0.

007 - The instruction in indexing requires two decoded instruction registers and is loaded into both decoded Registers 0 and 1

010 - There is an instruction in both decoded instruction Registers 0 and 1, but the instruction in decoded instruction Register 0 has not completed.

014 - The instruction in decoded instruction Register 0 is complete; so, the instruction in decoded instruction Register 1 moves to decoded instruction register 0, and the empty word is loaded into decoded instruction Register 1.

016 - The instruction in decoded instruction Register 0 is complete; so, the instruction in decoded instruction Register 1 moves to decoded instruction register 0, and the instruction in indexing is loaded into decoded instruction Register 1.

9-13 = Initial pipeline state of the instruction:
[See Bit 3-7 for a execution pipeline states (octal)]

15-17 = Operation type of the instruction:

0 - The instruction that left indexing was an INDEX only operation and does not require a decoded instruction register to execute.

1 - The instruction that left indexing was a READ operation and requires at least 1 decoded instruction register to execute.

2 - The instruction that left indexing was a WRITE operation and requires at least 1 decoded instruction register to execute.

3 - The instruction that left indexing was a READ/WRITE operation and requires at least 1 decoded instruction register to execute.

4 - The instruction that left indexing was a GCP operation and does not require a decoded instruction register to execute.

5 - The instruction that left indexing was a STACK operation and requires at least 1 decoded instruction register to execute

23 = SDA/EPH data is valid if set

Central Control Interrupt Data- Active

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1SR	AC1SC	AC1CES	AC1IBR
AC1INS	AC1INJ	AC1ILA	AC1ILR	AC1ITR	AC1INH
AC1CSC	AC1SAT	AC1PCR	AC1MCLK	AC1LIT	AC1DLR
AC1LPA	AC1UPA	AC1ACT	AC1ER	AC1PRM	AC1PRL
AC1LPI	AC1PES	AC1PSC	AC1PSQ	AC1RP0	AC1RP1
AC1PM0	AC1PM1	AC1ABC	AC1SAL	AC1SAR	AC1FIS
AC1EPS	AC1IFR	AC1MMR	AC1MSR	AC1MCO(H)	AC1MCO(L)
AC1MCD(H)	AC1MCD(L)	AC1MCP	AC1CCS(H)	AC1CCS(L)	AC1CUI
AC1FCT	AC1FCE	AC1FES	AC1FEE	AC1FER	AC1FST
AC1FLA(H)	AC1FLA(L)	AC1FLD(H)	AC1FLD(L)	AC1FLT(H)	AC1FLT(L)
AC1FRU(H)	AC1FRU(L)	AC1FRL(H)	AC1FRL(L)	AC1FIP	AC1CLE

Legend:

AC1 = Active
ST1 = Standby

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Central Control Fault Recognition (CCFR) Interrupt Data

CC1BLSTAT	CC1STATUS	CC1EADAT	CC1CLDAT	CC1EXDAT	CC1DGNCC
CC1BLDGN	CC1PSRDAT	CC1CPBDAT	CC1BRBDAT	CC1BLINV	CC1SWDAT
xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
ddddddddd	ddddddddd	ddddddddd	ddddddddd	ddddddddd	ddddddddd
AC1INS	AC1INH	AC1CES	ST1INS	ST1INH	ST1CES

CC1BLSTAT—CCFR B-Level Status Word. Failing Member and Software Decisions

Bit 0 = Active CC pulse source failure occurred
1 = Active CC boot ROM parity failure occurred
2 = Active CC control parity failure occurred
3 = Standby CC pulse source failure occurred
4 = Standby CC boot ROM parity failure occurred
5 = Standby CC control parity failure occurred
9 = CC switch occurred
10 = CCFR CC switch escalation
11 = Manual CC switch requested
12 = CCFR attempted CC switch

CC1STATUS—CC Status Word

Bit 0 = Run deferred CCFR on active CC only
1 = Print results when deferred tests ATP
2 = Switch CCs and retest if deferred tests ATP
3 = Restore standby CC to service
4 = Loop on deferred CCFR
5 = Deferred CCFR in progress
6 = Software active CC member number
7 = CCs are running in step
8 = CCs are in a normal configuration (duplex)
9 = Standby CC under test
10 = Routine CC exercise in progress
11 = Standby CC diagnosed due to high error rate
12 = Active CC diagnosed due to high error rate
13 = High error rate when CCs run in step
14 = External fault recovery requested access tests
15 = Request CC diagnostics
16 = CCFR error analysis diagnostic request
17 = Deferred tests run as part of diagnostics
18 = Results of deferred CC tests during diagnostics
19 = The standby CC was removed via TTY
20 = Update CC out-of-service lamps
21 = B-Level occurred on standby CC
22 = CC stopped by CC access test

CC1EADAT—CCFR Long Term Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1CLDAT—CCFR Short Term C-Level Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1EXDAT—CCFR Short Term External Entry Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1DGNCC—CCFR Short Term C-/D-/E-/F-Level DGN Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1BLDGN—CCFR Short Term B-Level DGN Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1PSRDAT—CCFR Short Term Pulse Source Failure Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1CPBDAT—CCFR Short Term Control Parity B-Level Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1BRBDAT—CCFR Short Term Boot ROM B-Level Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1BLINV—CCFR Short Term Invalid B-Level Entry Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

CC1SWDAT—CCFR Short Term Switch CC B-Level Error Counter

Bit 0-13 = Error timer
14 = Counter enable flag (if set, counter active)
15-23 = Error counter

ddddddddd—Active CC Pulse Source B-Levels Only

Where any number from 0 to 6 "dddddddd" lines of data can occur, depending on how many GCP addresses are found in the bus node data. Each GCP address found contains the GCP address in bits 0 through 21 and a code two-bit code in bits 22 and 23 as follows:

00 = Null entry
01 = Retry of GCP address passed
10 = Retry of GCP address failed (hardware error)
11 = Invalid GCP address (software error)

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

AC1INS—Active CC Interrupt Register (CCFR B-Levels Only)

AC1INH—Active CC Inhibit Register (CCFR B-Levels Only)

AC1CES—Active CC Error Source Register (CCFR B-Levels Only)

ST1INS—Standby CC Interrupt Register (CCFR B-Levels Only)

ST1INH—Standby CC Inhibit Register (CCFR B-Levels Only)

ST1CES—Standby CC Error Source Register (CCFR B-Levels Only)

If CC is Active:

REPT:CC a INT FAIL DATA

AC1FR(H)	AC1FR(L)	AC1GR(H)	AC1GR(L)	AC1JR(H)	AC1JR(L)
AC1KR(H)	AC1KR(L)	AC1LR(H)	AC1LR(L)	AC1XR(H)	AC1XR(L)
AC1YR(H)	AC1YR(L)	AC1ZR(H)	AC1ZR(L)	AC1BR(H)	AC1BR(L)
AC1ER	AC1CSC	AC1CCS(H)	AC1CCS(L)	AC1ILA	CC1TESTFAIL
CC1ACW	CC1BCW	CC1STATUS			

If CC is Standby:

REPT:CC a INT FAIL DATA

ST1FR(H)	ST1FR(L)	ST1GR(H)	ST1GR(L)	ST1JR(H)	ST1JR(L)
ST1KR(H)	ST1KR(L)	ST1LR(H)	ST1LR(L)	ST1XR(H)	ST1XR(L)
ST1YR(H)	ST1YR(L)	ST1ZR(H)	ST1ZR(L)	ST1MMR	CC1TESTFAIL
AC1MSR	ST1MSR	ST1BR(H)	ST1BR(L)	AC1ME0(H)	AC1ME0(L)
ST1CAR(H)	ST1CAR(L)	ST1DAR(H)	ST1DAR(L)	ST1MI0(H)	ST1MI0(L)
AC1MI0(H)	AC1MI0(L)	AC1ME1(H)	AC1ME1(L)	AC1MI1(H)	AC1MI1(L)
ST1ME0(H)	ST1ME0(L)	ST1MI1(H)	ST1MI1(L)	ST1ME1(H)	ST1ME1(L)

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Variable field definitions:

a = Member number of the CC that failed. Description of selected variable names:

ACW—CCFR Control Word

BCW—Backup Control Word

STATUS—CC Status Word

TESTFAIL—Indication of Which Test Failed

CC1TESTFAIL—Failing Test Layout

Bit 0 = Buffer register tests
1 = Register and homogeneity tests
2 = Index adder tests
3 = Add-one logic tests
4 = Parity generator and checker tests
5 = Protected area tests
6 = Stack tests
7 = Boot ROM tests
8 = Matcher tests
9 = Decoder tests
10 = Buffer bus access tests
11 = Interrupt sequencer tests
12 = Fetch/execution sequencer tests
13 = Peripheral bus tests
14 = Interface bus tests
15-17 = Unused
18 = Subsystem access tests
19 = Logic tests
20 = Active matcher tests
21-23 = Unused

CC1ACW-CC1BCW—Control Word Test Selection

Bit 0 = Buffer register tests
1 = Register and homogeneity tests
2 = Index adder tests
3 = Add-one logic tests
4 = Parity tests
5 = Protected area tests
6 = Stack tests
7 = Boot ROM tests
8 = Matcher tests
9 = Decoder tests
10 = Buffer bus access tests
11 = Interrupt sequencer tests
12 = Fetch/execution sequencer tests
13 = Peripheral bus tests
14 = Interface bus tests
15 = Pulse source failure retry
16 = Internal B-Level error recovery
17 = Subsystem access tests
18 = Peripheral controller (PC) B-level all-tests-passed (ATP) termination routine
19 = Switch CC ATP routine
20 = C-level ATP routine
21 = External entry ATP routine
22 = Deferred CCFR ATP termination routine
23 = Interrupt termination routine

CC1STATUS—CC Status Word

Bit 0 = Run deferred CCFR on active CC only
1 = Print results when deferred tests ATP
2 = Switch CCs and retest if deferred tests ATP
3 = Restore standby CC to service
4 = Loop on deferred CCFR
5 = Deferred CCFR in progress
6 = Active CC indicator (which CC is active, 0 or 1)
7 = CCs are running in-step
8 = CCs were running in-step
9 = Standby CC under test
10 = Routine exercise in progress
11 = Standby CC diagnosed because of high error rate
12 = Active CC diagnosed because of high error rate
13 = High error rate when CCs run in-step
14 = External fault recovery requested CCFR tests
15 = Request CC diagnostics
16 = CCFR error analysis diagnostic flag
17 = Deferred tests run as part of diagnostics
18 = Results of deferred tests during diagnosis
19 = The standby CC was removed via TTY
20 = Update CC out-of-service lamps
21 = B-level occurred on standby CC
22 = CC halted by access test
23 = Unused

Central Control Fault Recognition Deferred Test Output Message Formats

TEST:CC *a* **DFR** *b*

If CC is Active:

TEST:CC *a* **DFR FAIL DATA**

AC1FR(H)	AC1FR(L)	AC1GR(H)	AC1GR(L)	AC1JR(H)	AC1JR(L)
AC1KR(H)	AC1KR(L)	AC1LR(H)	AC1LR(L)	AC1XR(H)	AC1XR(L)
AC1YR(H)	AC1YR(L)	AC1ZR(H)	AC1ZR(L)	AC1BR(H)	AC1BR(L)
AC1ER	AC1CSC	AC1CCS(H)	AC1CCS(L)	AC1ILA	CC1TESTFAIL
CC1ACW	CC1BCW	CC1STATUS			

If CC is Standby:

TEST:CC *a* **DFR FAIL DATA**

ST1FR(H)	ST1FR(L)	ST1GR(H)	ST1GR(L)	ST1JR(H)	ST1JR(L)
ST1KR(H)	ST1KR(L)	ST1LR(H)	ST1LR(L)	ST1XR(H)	ST1XR(L)
ST1YR(H)	ST1YR(L)	ST1ZR(H)	ST1ZR(L)	ST1MMR	CC1TESTFAIL
AC1MSR	ST1MSR	ST1BR(H)	ST1BR(L)	AC1ME0(H)	AC1ME0(L)
ST1CAR(H)	ST1CAR(L)	ST1DAR(H)	ST1DAR(L)	ST1MI0(H)	ST1MI0(L)
AC1MI0(H)	AC1MI0(L)	AC1ME1(H)	AC1ME1(L)	AC1MI1(H)	AC1MI1(L)
ST1ME0(H)	ST1ME0(L)	ST1MI1(H)	ST1MI1(L)	ST1ME1(H)	ST1ME1(L)

NOTE:
See "Interrupt Data Register Layouts" for register descriptions.

Variable field definitions:
a = Member number of the CC being tested
b = Result of non-failing test

ABORTED = Deferred CC fault recognition has been aborted because of a maintenace interrupt
ATP = All tests passed
STOPPED = The deferred CC fault recognition has been terminated by the *STOP:MACLI* input message

CCFR Deferred Test Output Message Formats (Contd)

ACW—CCFR Control Word

BCW—Backup Control Word

STATUS—CC Status Word

TESTFAIL—Indication of which Test Failed

Auxiliary Unit Status Registers

The AU client registers are defined as:

ASR—AU Status Register (Octal 12)

Bit 0-3 = Parity on data byte 0 through 3 (PARD0-PARD3)
4 = Last cycle was read (READ)
5 = Last cycle was write (WRITE)
7 = Last cycle was word DMA (always 1) (WDMA)
9 = Operational interject active (OIJACT)
10 = Maintenance interject active (MIJACT)
11 = Maintenance interrupt active (MINACT)
13 = Word DMA request (WREQ)
15 = Reserved
16 = Interface busy (IFBSY)
17 = All-seems-well response from MMIO (AUASW)
18 = AU GCP or MMIO response present (AURESP)
19 = AUI in maintenance mode (MTCE)
20 = AU activity (AUA)

AUC—AU Control Register (Octal 13)

Bit 0 = Enable IFB drivers
1 = Enable parity checking
2 = Enable address limit checking
3 = Enable operational interjects
4 = Enable maintenance interjects
5 = Enable maintenance interrupts
6 = Clear operational interjects
7 = Clear maintenance interjects
8 = Clear maintenance interrupts
9 = In-service
10 = Update in-progress
11 = AUI reset
12 = Trouble AU bus 0
13 = Trouble AU bus 1
14 = Enable AU verify match
15 = Enable AU all-seems-well failure checks
16 = Enable AU request from API 0
17 = Enable AU request from API 1
18 = Enable AU request from DUS 0
19 = Enable AU request from DUS 1
20 = Maintenance mode
21 = AU sequencer step
22 = AU sequencer INIT
23 = AU activity flip-flop

AUE—AU Error Register (Octal 14)

Bit 0 = DMA lower address limit exceeded
1 = DMA upper address limit exceeded
2 = Detected absense of ASW on IFB
3 = Detected ASWF on IFB
4 = Master detected data parity error
5 = Slave detected data parity error
6 = Slave detected common error
7 = Slave detected invalid address error
8 = Slave detected address parity error
9 = Sent ASWF
10 = AU bus detected error
11 = Interface bus detected error
12-15 = Reserved
16 = Command override error
17 = AU enable verify mismatch error
18 = AU SAP verify mismatch error
19 = AU store address bus parity error
20 = AU reply bus parity error

LLA—AU Lower Limit Address Register (Octal 15)

Bit 8-23 = AU lower limit (bits 14 through 29)

ULA—AU Upper Limit Address Register (Octal 16)

Bit 8-23 = AU lower limit (bits 14 through 29)

DR—AU Data Register (Octal 17)

Bit 0-31 = AU data register (bits 00 through 31)

UAR—AU Upper Address Register (Octal 40)

Bit 22-29 = AU upper address (bits 22 through 29)

ACM—AU Communication Register (Octal 41)

Bit 0-3 = AU enable verify expected (bits 00, 01, 12, and 13)
4-7 = Store access permitted verify (bits 00, 01, 12, and 13)
8-11 = AU reguest (bits 00, 01, 12, and 13)
12-15 = AU enable verify (bits 00, 01, 12, and 13)

AAS—AU Store Address Register (Octal 42)

Bit 0-21 = AU store address (bits 00 through 21)
22 = AU store address parity bit
AU upper address bit 22
23 = AU store address write bit
AU upper address bit 23
24 = AU store address read bit
AU upper address bit 24
25-29 = AU store address (bits 25 through 29)

AAR—AU Reply Register (Octal 43)

Bit 0-23 = AU reply register (bits 00 through 23)
24 = AU reply register all-seems-well
25 = AU reply register parity bit 1
26 = AU reply register parity bit 2

AUA—AU Address Register (Octal 44)

Bit 0-15 = AU address register (bits 00 through 15)
16 = AU address register read
17 = AU address register write
18 = AU address register control
19 = AU address register parity

AUB—AU Bus Register (Octal 45)

Bit 0 = AU Store address parity bit
1 = AU Store address write bit
2 = AU Store address read bit
3 = AU reply parity bit 1
4 = AU reply parity bit 2
5 = AU reply all-seems-well
6 = AU bus 0 operational interject
7 = AU bus 1 operational interject
8 = AU bus 0 maintenance interject
9 = AU bus 1 maintenance interject
10 = AU MMIO write register parity bit 1
11 = AU MMIO write register parity bit 2
12 = AU DMA write register parity bit 1
13 = AU DMA write register parity bit 2
14 = Invert data parity on DMA transactions
15 = Enable AU bus drivers

ADW—AU DMA Register (Octal 46)

Bit 0-23 = AU DMA write register (bits 00 through 23)

Miscellaneous Power Internal Data

XSTAT_X	XSTAT_X+1	IMAGE_X	IMAGE_X+1	IMAGE_X+2	IMAGE_X+3
STABINX_X	STABINX_X+1	BSTAT_X	0.....0	0.....0	0.....0
XSTAT	XSTAT+1	IMAGE	IMAGE+1	IMAGE+2	IMAGE+3
STABINX	STABINX+1	BSTAT	LRTW	LRCW	0.....0

NOTE:
Prefix all words with XP1R.

XSTAT_X—XPWR 0 Unit Software Word Before XPWR Base Level MTCE
XSTAT—XPWR 1 Unit Software Word After XPWR Base Level MTCE

Bit 0 = 5 V converter for CS bus 0 found faulty
1 = 5 V converter for CS bus 1 found faulty
2 = 5 V converter for PS bus 0 found faulty
3 = 5 V converter for PS bus 1 found faulty
4 = 5 V converter for IF bus 0 found faulty
5 = 5 V converter for IF bus 1 found faulty
6 = Terminating voltage of CS bus 0 found out-of-range
7 = Terminating voltage of CS bus 1 found out-of-range
8 = Terminating voltage of PS bus 0 found out-of-range
9 = Terminating voltage of PS bus 1 found out-of-range
10 = Terminating voltage of IF bus 0 found out-of-range
11 = Terminating voltage of IF bus 1 found out-of-range
12 = 24 V converter found faulty
13-14 = Current XPWR state
DGR = Degraded state
OOS = Out-of-service
ACT = Active state
UNA = Unassigned
15 = Unused
16 = SSD 0 unit is just restored
17-18 = Current SD value of XPWR 0
19 = XPWR 0 unit is just restored
20 = Need to verify XPWR scan image
21 = OOS state forced by XPWR software
22 = XPWR 0 can be restored only by TTY message
23 = Stop XPWR 0 scanning

XSTAT_X+1—XPWR 1 Unit Software Word Before XPWR Base Level MTCE
XSTAT+1—XPWR 1 Unit Software Word Before XPWR Base Level MTCE

Bit 0 = 5 V converter for CS bus 0 found faulty
1 = 5 V converter for CS bus 1 found faulty
2 = 5 V converter for PS bus 0 found faulty
3 = 5 V converter for PS bus 1 found faulty
4 = 5 V converter for IF bus 0 found faulty
5 = 5 V converter for IF bus 1 found faulty
6 = Terminating voltage of CS bus 0 found out-of-range
7 = Terminating voltage of CS bus 1 found out-of-range
8 = Terminating voltage of PS bus 0 found out-of-range
9 = Terminating voltage of PS bus 1 found out-of-range
10 = Terminating voltage of IF bus 0 found out-of-range
11 = Terminating voltage of IF bus 1 found out-of-range
12 = 24 V converter found faulty
13-14 = Current XPWR state
DGR = Degraded state
OOS = Out-of-service
ACT = Active state
UNA = Unassigned
15 = Unused
16 = SSD 1 unit is just restored
17-18 = Current SD value of XPWR 1
19 = XPWR 1 unit is just restored
20 = Need to verify XPWR scan image
21 = OOS state forced by XPWR software
22 = XPWR 1 can be restored only by TTY message
23 = Stop XPWR 1 scanning

IMAGE_X—XPWR 0 Scan Image Word 0 Before XPWR Base Level MTCE
IMAGE_XPWR 0 Scan Image Word 0 After XPWR Base Level MTCE

Bit 0 = 24 V converter status
1-5 = Unused
6 = Major alarm indicator
7 = CS bus 0 terminating voltage status
8 = CS bus 1 terminating voltage status
9 = Status of 5 V converter for CS bus 0
10 = Unused
11 = Status of 5 V converter for CS bus 1
12-13 = Unused
14 = PS bus 0 terminating voltage status
15 = PS bus 1 terminating voltage status
16 = Status of 5 V converter for PS bus 0
17 = Unused
18 = Status of 5 V converter for PS bus 1
19-23 = Unused

IMAGE_X+1—XPWR 0 Scan Image Word 1 Before XPWR Base Level MTCE
IMAGE_+1—XPWR 0 scan Image Word 1 After XPWR Base Level MTCE

Bit 0 = IF bus 0 terminating voltage status
1 = IF bus 1 terminating voltage status
2 = Status of 5 V converter for IF bus 0
3 = Unused
4 = Status of 5 V converter for IF bus 1
5-6 = Unused
7-13 = Buffer used for verifying scan image
14-23 = Unused

IMAGE_X+2—XPWR 1 Scan Image Word 0 Before XPWR base level MTCE
IMAGE_+2—XPWR 1 Scan Image Word 0 After XPWR Base Level MTCE

Bit 0 = 24 V converter status
1-5 = Unused
6 = Major alarm indicator
7 = CS bus 0 terminating voltage status
8 = CS bus 1 terminating voltage status
9 = Status of 5 V converter for CS bus 1
10 = Unused
11 = Status of 5 V converter for CS bus 0
12-13 = Unused
14 = PS bus 0 terminating voltage status
15 = PS bus 1 terminating voltage status
16 = Status of 5 V converter for PS bus 1
17 = Unused
18 = Status of 5 V converter for PS bus 0
19-23 = Unused

IMAGE_X+3—XPWR 1 Scan Image Word 1 Before XPWR Base Level MTCE
IMAGE_+3—XPWR 1 Scan Image Word 1 After XPWR Base Level MTCE

Bit 0 = IF bus 0 terminating voltage status
1 = IF bus 1 terminating voltage status
2 = Status of 5 V converter for IF bus 0
3 = Unused
4 = Status of 5 V converter for IF bus 1
5-6 = Unused
7-13 = Buffer used for verifying scan image
14-23 = Unused

STABINX_X—XPWR 0 Status Table Index Before XPWR Base Level MTCE
STABINX—XPWR 0 Status Table Index After XPWR Base Level MTCE

Bit 0-23 = Index value
Value = No fault on XPWR 0
Value = SSD 0 is OOS
Value = XPWR 0 is powered down
Value = Fault on converter for ACT bus or 24 V converter
Value = Fault on converter for OOS bus

STABINX_X+1—XPWR 1 Status Table Index Before XPWR Base Level MTCE
STABINX+1—XPWR 1 Status Table Index After XPWR Base Level MTCE

Bit 0-23 = Index value

Value = No fault on XPWR 1
Value = SSD 1 is OOS
Value = XPWR 1 is powered down
Value = Fault on converter for ACT bus or 24 V converter
Value = Fault on converter for OOS bus

BSTAT_X—Bus (CS, PS, IF Bus) Status Word Before XPWR Base Level MTCE
BSTAT—Bus (CS, PS, IF Bus) Status Word After XPWR Base Level MTCE

Bit 0 = CS bus 0 is OOS if set
1 = CS bus 1 is OOS if set
2 = PS bus 1 is OOS if set
3 = PS bus 0 is OOS if set
4 = PS bus 0 is OOS if set
5 = PS bus 1 is OOS if set
6-23 = Unused

LRTW—XPWR Long Range Timer

Bit 0-17 = XPWR long ranger timer
18-19 = Unused
20 = Long range timer enable bit
21-23 = Unused

LRCW—XPWR Long Range Counter Word

Bit 0-11 = Long ranger counter for XPWR 0
12-23 = Long ranger counter for XPWR 1

XA Window Information

AC1SDA(H)	AC1SDA(L)	AC1XACTL	AC1XAWT	AC1XAWP0	AC1XAWP1
AC1XAWP2	AC1XAWP3	AC1XAWP4	AC1XAWP5	AC1XAWP6	AC1XAWP7
ST1SDA(H)	ST1SDA(L)	ST1XACTL	ST1XAWT	ST1XAWP0	ST1XAWP1
ST1XAWP2	ST1XAWP3	ST1XAWP4	ST1XAWP5	ST1XAWP6	ST1XAWP7

SDA(H)—Saved Data Address (High order bits)

Bit 0-6 = The high order bits (24-29) of the 30 bit SDA. The complete data address is determined by concatenating SDA(H) with SDA(L)

SDA(L)—Saved Data Address (Low order bits)

Bit 0-23 = The low order bits (0-23) of the 30 bit SDA. The complete data address is determined by concatenating SDA(H) with SDA(L)

XACTL—Extended Access Control Register

Bit 0 = XAWEN0, extended access window 0 enable
1 = XAWEN1, extended access window 1 enable
2 = XAWEN2, extended access window 2 enable
3 = XAWEN3, extended access window 3 enable
4 = XAWEN4, extended access window 4 enable
5 = XAWEN5, extended access window 5 enable
6 = XAWEN6, extended access window 6 enable
7 = XAWEN7, extended access window 7 enable

XAWT—Extended Access Window Type Register

Bit 0 = XAWT0, extended access window 0 enable
1 = XAWT1, extended access window 1 enable
2 = XAWT2, extended access window 2 enable
3 = XAWT3, extended access window 3 enable
4 = XAWT4, extended access window 4 enable
5 = XAWT5, extended access window 5 enable
6 = XAWT6, extended access window 6 enable
7 = XAWT7, extended access window 7 enable

XAWPn—Extended Access Window Pointer

Bit 0-14 = Extended access window pointer

Common Printouts

Common Level Control Data (MI1CONT)

MI1CONT

Bit 0 = MARP return to reference point
1 = MARP return by rolling back to intermediate level
2 = MARP return by rolling ahead to intermediate level
3 = Audit in progress flag
4 = In restart flag
5 = CC's have been switched
6 = A pump of CS(s) has been performed
7 = A pump of PS(s) has been performed
8 = No backup area has been zeroed
9 = A phase (indicated in MI1PHASEPT) has been requested
10 = A pulse source B-level has occurred
11 = An out-of-range pulse source B-level
12 = An out-of-range call store D-level
13 = An out-of-range program store E-level
14 = An out-of-range peripheral F-level
15 = Request hash sum of area indicated in MI1HASHADRS
16 = A maintenance phase record is to be formed by ERAP
17 = A software error has occurred
18 = MARP invalid interrupt entry
19 = SAWS routine has pumped 1 bink (block of 1024 words) on intermediate level
20 = CS duplex failure occurred
21 = Application work flag 2
22 = Application work flag 1
23 = Application work flag 0

MI1CONT Control Flags

Bit 1-2 = Roll ahead or back
6-7 = Pump of CS or PS has occurred
11-14 = An out-of-range B-, D-, E- or F-level has occurred

Common Auxiliary Unit Data

EIW0	EIW1	EIW2	EIW3	FADR	FDAT
RIW0	RIW1	RIW2	RIW3	AUIBA	FBAD
CID	MID	STA	CTL	ESR	LLA
ULA	SDAT_U	SDAT_L	ACM	SAAS_U	SAAS_L
ARR	AUAR	AUB	ADW	AMW	PROGAD
TESTAD	TESTOP	TSAVF	TSAVG	TSAVJ	TSAVK
TSAVL	TSAVX	TSAVY	TSAVZ	ESR0	FGCP
STATE	ERAT	RERAC	EMRG	EAST	DTADR
LTTAT	LTTAC0	LTTAC1	LTTAC2	LTTAC3	76543210
76543210	SAPI0_BR	SAPI1_BR	SDUS0_BR	SDUS1_BR	SBSTAT_BR
76543210	SAPI0_AR	SAPI1_AR	SDUS0_AR	SDUS1_AR	BSTAT_AR

NOTE:
Prefix all words with AU1R.

EIW0-EIW3—Save Error Information Words

Bit 0-3 = Error type
6 = Indicates API 0 involved in the error
7 = Indicates API 1 involved in the error
8 = Indicates DUS 0 involved in the error
9 = Indicates DUS 1 involved in the error
12-13 = Operation in progress at the time of the error
15-16 = Read or write indicator
17 = Control node indicator
18-20 = In-service status of AUI 0
21-23 = In-service status of AUI 1

FADR—Failing Address

FDAT—Failing Data

RIW0-RIW3—Save Recovery Information Word

Bit 0-2 = Current recovery state
3 = Indicates a status update was attempted
4 = Indicates AUI tests were run
5 = Indicates an attempt was made to remove an AUI
6 = Indicates control was passed to unique AU recovery
7 = Indicates an attempt was made to remove an AU
8 = Indicates an attempt was made to remove an AU bus
9 = Indicates an AUFR bootstrap was attempted
10 = Indicates an IFFR bootstrap was requested
12 = Indicates the attempt to update status failed
13 = Indicates the AUI tests failed
14 = Indicate the attempt to remove an AUI failed
16 = Indicate the attempt to remove an AU failed
17 = Indicate the attempt to remove an AU bus failed
21-23 = Recovery state necessary for the next interrupt/interject

AUIBA—Base Address of AUI Requesting/Reporting the Error

FBAD—Base Address of Failing AU

CID—AUI Client Identification Register of Suspect AUI

Bit 0-9 = Circuit pack name

MID—AUI Microcode Identification Register

Bit 0-9 = Microcode name

STA—Status Register of Suspect AUI

Bit 0-3 = RCVD Data parity bits
4 = Last cycle was read
5 = Last cycle was write
7 = Last cycle was word DMA
9 = Operational interject active
10 = Maintenance interject active
11 = Maintenance interrupt active
13 = Word DNA request
16 = Interface busy
17 = ALl seems well from MMIO
18 = AU GCP or MMIO RESP present
19 = AUI maintenance mode status
20 = AU activity status

CTL—Control Register of Suspect AUI

Bit 0 = Client IFB enable
1 = Parity checking enable
2 = Address limit checking enable
3 = Operational interject enable
4 = Maintenance interject enable
5 = Maintenance interrupt enable
6 = Operational interject clear
7 = MTCE interject clear
8 = MTCE interrupt clear
9 = AUI is in-service—toggle flip-flop
10 = Update is in-progress—toggle flip-flop
11 = AUI reset
12 = Trouble AU bus 0
13 = Trouble AU bus 1
14 = Enable verify AU match
15 = Enable all-seems-well fail checks
16 = Enable AU request from API 0
17 = Enable AU request from API 1
18 = Enable AU request from DUS 0
19 = Enable AU request from DUS 1
20 = Maintenance mode
21 = AU sequencer step
22 = AU sequencer initialization
23 = AU activity flip-flop

ESR—Error Source Register of Suspect AUI

Bit 0 = DMA lower limit exeeded
1 = DMA upper limit exeeded
2 = Detected no all-seems-well
3 = Detected all-seems-well failure
4 = Master detected data parity error
5 = Slave detected data parity error
6 = Slave detected common error
7 = Slave detected invalid address error
8 = Slave detected address parity error
9 = Sent all-seems-well failure
10 = AU bus detected error
11 = IFB error maintenance interrupt
16 = Command overwrite error
17 = AU verify mismatch error
18 = AU SAP verify mismatch error
19 = AU store address bus parity error
20 = AU reply bus parity error

LLA—Lower DMA Limit Register of Suspect AUI

Bit 8-23 = Lowest DMA address — Bits 14-29

ULA—Upper DMA Limit Register of Suspect AUI

Bit 8-23 = High DMA address limit

SDAT_U—Data Register (Upper Byte) of Suspect AUI

SDAT_L—Data Register (Lower Byte) of Suspect AUI

ACM—Communication Register of Suspect AUI

Bit 0 = AU enable verify expected bit 00
1 = AU enable verify expected bit 01
2 = AU enable verify expected bit 12
3 = AU enable verify expected bit 13
4 = Store access permitted expected bit 00
5 = Store access permitted expected bit 01
6 = Store access permitted expected bit 12
7 = Store access permitted expected bit 13
8 = AU request bit 00
9 = AU request bit 01
10 = AU request bit 12
11 = AU request bit 13
12 = AU enable verify bit 00
13 = AU enable verify bit 01
14 = AU enable verify bit 12
15 = AU enable verify bit 13

SAAS_U—Store Address Register (Upper Byte) of Suspect AUI

Bit 0-5 = Upper address bits 24-29
0 = AU store address register read bit

SAAS_L—Store Address Register (Lower Byte) of Suspect AUI

Bit 0-23 = AU store address
22 = AU store address parity bit
23 = AU store address write bit

ARR—AU Reply Register of Suspect AUI

Bit 0-23 = AU reply register bits 0-23
0 = AU reply register all-seems-well
1 = AU reply register parity bit 1
2 = AU reply register parity bit 2

AUAR—AU Address Register of Suspect AUI

Bit 0-15 = AU address register
16 = AU address register read bit
17 = AU address register write bit
18 = AU address register control bit
19 = AU address register parity bit

AUB—AUB Register of Suspect AUI

Bit 0 = AU store address parity bit
1 = AU store address write bit
2 = AU store address read bit
3 = AU reply parity bit 1
4 = AU reply parity bit 2
5 = AU reply all-seems-well
6 = AU bus 0 operational interject
7 = AU bus 1 operational interject
8 = AU bus 0 maintenance interject
9 = AU bus 1 maintenance interject
10 = P1 parity on the AMW register
11 = P2 parity on the AMW register
12 = P1 parity on the ADW register
13 = P2 parity on the ADW register
14 = Invert data parity on DMA transaction
15 = Enable AU bus drivers

ADW—DMA Write Register of Suspect AUI

AMW—MMIO Write Register of Suspect AUI

PROGAD—Program Address at Failure Returned From Failing Tests or Bootstrap

TESTAD—Test Address at Failure Returned From Failing Tests or Bootstrap

TESTOP—Test Options and Flags Returned From Failing Tests or Bootstrap

TSAVF—TSAVZ—F-, G-, J-, K-, L-, X-, Y-, and Z-Registers Returned From Failing Tests or Bootstrap

ESR0—Error Source Register of Failing AU

FGCP—GCP Response of Failing AU

Bit 0 = Maintenance request
1 = Maintenance flip-flop set side
2 = Maintenance flip-flop reset side
3-5 = Trapping flip-flop
  3 = Clock activity error
  4 = Normal CC clock error
  5 = Maintenance CC clock error
6 = Input address parity error
7 = Data parity error (CC to DFC)
8 = Write protect error
9 = Out of range address error
10 = Mode error
11 = K-code bit 11
12 = Code bit 12
13 = K-code bit 13
14 = K-code bit 14
15 = K-code bit 15
16 = CC interface sequencer error
17-23 = Trapping flip-flop
  17 = K-code match detected
  18 = Control read mode detected
  19 = Control write mode detected
  20 = All ones address detected
  21 = All zeros address detected
  22 = All ones data detected
  23 = All zeros data detected

STATE—AUFR State Timing Word

Bit 0-8 = State timer
12-20 = Value of state timer before recovery
23 = State timing enable

ERAT—AUFR Error Analysis Timing Word

Bit 0-5 = Error analysis timer
12-17 = Value of error analysis timer before recovery
23 = Error analysis timing enable

ERAC—AUFR Error Analysis Counters

Bit 0-2 = ERA counter for passing status updates
3-5 = ERA counter for unique AU recovery no fault found returns

EMRG—AUFR Emergency Action Timing Word

Bit 0-10 = Emergency action state timer
12-22 = Value of emergency action timer before recovery
23 = Emergency action timing enable

EAST—Save Emergency Action State Counter

Bit 0-4 = AUFR emergency action state counter

DTADR—Program Address Where Bootstrap was Called

LTTAT—Long-Term Trouble Analysis Timing Word

Bit 0-11 = Long term trouble analysis timer
23 = Long term trouble analysis timer enable

LTTAC0—Long-Term Trouble Analysis Counter for AUI 0

LTTAC1—Long-Term Trouble Analysis Counter for AUI 1

SLTTAC2—Long-Term Trouble Analysis Counter for AUB 0

SLTTAC3—Long-Term Trouble Analysis Counter for AUB 1

SAPI0_BR—API 0 Status Word Before Recovery
SAPI1_BR—API 1 Status Word Before Recovery

Bit 0 = AU marked in trouble
1 = AU in offline configuration
2 = AU stopped and in maintenance mode
4 = Diagnosis to be requested for AU
5 = AU KCODE trouble
6 = AU is active unit, for API
7 = AU is standby unit, for API
8 = API is being restored
18 = Do not retore AU

SDUS0_BR—DUS 0 Status Word Before Recovery
SDUS1_BR—DUS 1 Status Word Before Recovery

Bit 0 = AU marked in trouble
1 = AU in offline configuration
2 = AU stopped and in maintenance mode
4 = Diagnosis to be requested for AU
5 = AU KCODE trouble
6 = AU is active unit, for API
18 = Do not retore AU

BSTAT_BR—AUB Status Word Before Recovery

Bit 0 = AU bus 0 trouble flip-flop in active AUI
1 = AU bus 1 trouble flip-flop in active AUI
2 = AU bus 0 trouble flip-flop in standby AUI
3 = AU bus 1 trouble flip-flop in standby AUI
4 = AU bus 0 system in offline configuration
5 = AU bus 1 system in offline configuration
6 = AU bus stopped and in maintenance mode
7 = Do not restore Au bus

SAPI0_AR—API 0 Status Word After Recovery
SAPI1_AR—API 1 Status Word After Recovery

Bit 0 = AU marked in trouble
1 = AU in offline configuration
2 = AU stopped and in maintenance mode
4 = Diagnosis to be requested for AU
5 = AU KCODE trouble
6 = AU is active unit, for API
7 = AU is standby unit, for API
8 = API is being restored
18 = Do not retore AU

SDUS0_AR—DUS 0 Status Word After Recovery
SDUS1_AR—DUS 1 Status Word After Recovery

Bit 0 = AU marked in trouble
1 = AU in offline configuration
2 = AU stopped and in maintenance mode
4 = Diagnosis to be requested for AU
5 = AU KCODE trouble
6 = AU is active unit, for API
18 = Do not retore AU

BSTAT_AR—AUB Status Word After Recovery

Bit 0 = AU bus 0 trouble flip-flop in active AUI
1 = AU bus 1 trouble flip-flop in active AUI
2 = AU bus 0 trouble flip-flop in standby AUI
3 = AU bus 1 trouble flip-flop in standby AUI
4 = AU bus 0 system in offline configuration
5 = AU bus 1 system in offline configuration
6 = AU bus stopped and in maintenance mode
7 = Do not restore AU bus

Common Interface Bus Recovery Data

See *Interface Bus Printouts*.

IFB- Interface Bus Printouts

Common Interface Bus (IFB) Recovery Data

STAT_BR0	STAT_BR1	STAT_BR2	STAT_BR3	STAT_BR4	STAT_BR5
STAT_BR6	STAT_BR7	STAT_BR8	STAT_BR9	STAT_BR10	STAT_BR11
STAT_BR12	STAT_BR13	STAT_BR14	STAT_BR15	STAT_BR16	STAT_BR17
STAT_BR18	STAT_BR19	STAT_BR20	STAT_BR21	STAT_BR22	STAT_BR23
BSTAT_BR	SRW	SSW	ECW	LTW	RAW
AFCT	AFCE	AFES	AFEE	AFER	AFIP
SFCT	SFCE	SFES	SFEE	SFER	SFIP
AFRU_U	AFRU_L	AFRL_U	AFRL_L	ACSC	CR01
SFRU_U	SFRU_L	SFRL_U	SFRL_L	RQESR	CLSTA
FADR_U	FADR_L	FDAT_U	FDAT_L	MCADR	SCADR
RCADR	DCADR	RCERA	DCERA	BSERA	ERATW
LTPASAV	LTTASAV	LTTOSAV	LTFSAV	LTGSAV	LTJSAV
LTKSAV	LTLSAV	LTXSAV	LTYSAV	LTZSAV	RESERVED
ICRAA	BSRAA	RAATW	DTW	DTADR	SEMRG
B0ANALX	B1ANALX	BANAL	BLW	BLADR	RESERVED
STAT_AR0	STAT_AR1	STAT_AR2	STAT_AR3	STAT_AR4	STAT_AR5
STAT_AR6	STAT_AR7	STAT_AR8	STAT_AR9	STAT_AR10	STAT_AR11
STAT_AR12	STAT_AR13	STAT_AR14	STAT_AR15	STAT_AR16	STAT_AR17
STAT_AR18	STAT_AR19	STAT_AR20	STAT_AR21	STAT_AR22	STAT_AR23
BSTAT_AR					

Note: Prefix all words with IF1R.

IF1RSTAT_BR0-IF1RSTAT_BR23—IFB Client Status Prior to Recovery

Bit 0 = IFB client is OOS
1 = IFB client is stopped
3 = IFB client is active
4 = IFB client is standby
5 = IFB client is forced
6 = Request DGN for IFB client
8 = IFB client is being restored
9 = Do not restore IFB client

IF1RBSTAT_BR—IFB Status Prior to Recovery

Bit 0 = IFBC activity in active CC
1 = IFB 0 trouble set in active CC
2 = IFB 1 trouble set in active CC
3 = IFBC activity in standby CC
4 = IFB 0 trouble set in standby CC
5 = IFB 1 trouble set in standby CC
8 = IFB subsystem is stopped
9 = Do not restore IFB

IF1RSRW—IFB Subsystem Recovery Word

Bit 0 = Current entry resulted from a D-level interrupt
1 = Current entry resulted from an interject
2 = Current entry resulted from a BLM
3 = Standby CC is available for use during testing
4 = Standby CC was in service at entry
5 = Multiple client maintenance requests present
6 = Requesting client bins loaded
7 = Driving client bins loaded
8 = Common bins loaded
9 = Plant measurement counts must be updated
10 = Active IFBC stack bins loaded
11 = Standby IFBC stack bins loaded

IF1RSSW—IFB Shadow Stack Word

Bit 0-1 = Indicates the stack utilized during recovery (octal)
1 - Bus node stack
2 - IFBC stack
3-7 = Stack depth utilized during recovery
9 = Indicates the standby CCs stacks were utilized

IF1RECW—IFB Error Classification Word

Bit 0-2 = Error class (octal)
- 1 - Indiscernible error
- 2 - Discernible error
- 3 - Memory unit error
- 4 - Client-specific error
- 5 - Software error

3-5 = Error sub-class (octal)
- 1 - Address parity error
- 2 - Data parity error
- 3 - Control parity error
- 4 - Invalid slave reply error
- 5 - Invalid master reply error
- 6 - All-seems-well error

6-9 = Requesting unit (octal)
- 1 - Active CC
- 2 - Standby CC
- 3 - Active CC's IFBC
- 4 - Standby CC's IFBC
- 5 - Memory unit
- 6 - Master client
- 7 - Slave client
- 10 - Uninvolved client

12-14 = In-progress operation (octal)
- 1 - MMIO
- 2 - Word DMA
- 3 - Block DMA
- 4 - Client to client

15-17 = Read/Write Indicator (octal)
- 1 - Read operation
- 2 - Write operation

IF1RECW—IFB Error Classification Word (Contd)

Bit 18-21 = Driving unit (octal)
1 - Active CC
2 - Standby CC
3 - Active CC's IFBC
4 - Standby CC's IFBC
5 - Memory unit
6 - Master client
7 - Slave client
10 - Uninvolved client

IF1RLTW—IFB Logical Test Word

Bit 0-3 = Type of logical test requested (octal)
1 - IFBC test
2 - Client MMIO test
3 - Client DMA test
5 - False responder test
6 - All tests with respect to all clients on IFB 0
7 - All tests with respect to all clients on IFB 1
10 - All tests with respect to a given client
11 - All tests with respect to all clients
9-11 = Indicates which client was tested (octal)
1 - Requesting client tested
2 - Driving client tested
21-23 = Logical test disposition (octal)
1 - Logical tests failed
2 - Logical tests passed

IF1RRAW—IFB Recovery Action Word

Bit 0-5 = Recovery action (octal)
1 - Active CC implicated
2 - Standby CC implicated
3 - Active CCs IFBC implicated
4 - Standby CCs IFBC implicated
5 - Memory unit implicated by first look
6 - Master client implicated by first look
7 - Slave client implicated by first look
10 - Uninvolved client implicated by first look
26 - Memory unit implicated by logical tests
27 - Client implicated by logical tests
30 - IFB 0 implicated
31 - IFB 1 implicated
32 - Client-specific problem implicated
33 - Software implicated
34 - IFB subsystem status implicated
35 - IFB subsystem configuration implicated
36 - Transient error implicated
37 - Inconclusive error implicated
21-23 = Recovery action disposition (octal)
1 - Recovery action failed or was denied
2 - Recovery action completed

IF1RAFCT—Active CC IFBC Control Register (AC1FCT)

IF1RAFCE—Active CC IFBC Client Enable Register (AC1FCE)

IF1RAFES—Active CC IFBC Error Source Register (AC1FES)

IF1RAFEE—Active CC IFBC Error Enable Register (AC1FEE)

IF1RAFER—Active CC IFBC Error Request Register (AC1FER)

IF1RAFIP—Active CC IFBC Poll Register (AC1FIP)

IF1RSFCT—Standby CC IFBC Control Register (ST1FCT)

IF1RSFCE—Standby CC IFBC Client Enable Register (ST1FCE)

IF1RSFES—Standby CC IFBC Error Source Register (ST1FES)

IF1RSFEE—Standby CC IFBC Error Enable Register (ST1FEE)

IF1RSFER—Standby CC IFBC Error Request Register (ST1FER)

IF1RSFIP—Standby CC IFBC Poll Register (ST1FIP)

IF1RAFRU_U—Upper Byte of Active CC IFBC Upper Relocation Register (AC1FRU)

IF1RAFRU_L—Lower Bytes of Active CC IFBC Upper Relocation Register (AC1FRU)

IF1RAFRL_U—Upper Byte of Active CC IFBC Lower Relocation Register (AC1FRL)

IF1RAFRL_L—Lower Bytes of Active CC IFBC Lower Relocation Register (AC1FRL)

IF1RACSC— Active CC Status Register (AC1CSC)

IF1RCR01—Memory Unit CR01 Register

IF1RSFRU_U—Upper Byte of Standby CC IFBC Upper Relocation Register (ST1FRU)

IF1RSFRU_L—Lower Bytes of Standby CC IFBC Upper Relocation Register (ST1FRU)

IF1RSFRL_U—Upper Byte of Standby CC IFBC Lower Relocation Register (ST1FRL)

IF1RSFRL_L—Lower Bytes of Standby CC IFBC Lower Relocation Register (ST1FRL)

IF1RRQESR—Requesting Client's Error Summary Register

Bit 0 = Lower DMA limit exceeded
1 = Upper DMA limit exceeded
2 = Master detected no all seems well
3 = Master detected all-seems-well failure
4 = Master detected data parity error
5 = Slave detected data parity error
6 = Slave detected control error
7 = Slave detected unused address error
8 = Slave detected address parity error
9 = Slave sent ASWF (summary bit for slave errors)
10 = Client error (summary bit for maintenance interject)
11 = IFB error (summary bit for master errors)
12-15 = Reserved
16-23 = Client options

IF1RCLSTA—Client's Status Register

Bit 0-3 = Data parity received by client
4 = Last cycle was a read
5 = Last cycle was a write
6 = Last cycle was block DMA
7 = Last cycle was word DMA
8 = Last cycle was client to client
9 = Operational interject active
10 = Maintenance interject active
11 = Maintenance interrupt active
12 = Block DMA request
13 = Word DMA request
14 = Client to client request
15 = Reserved
16-23 = Client options

IF1RFADR_U—Upper Byte of Failing Address

IF1RFADR_L—Lower Bytes of Failing Address

IF1RFDAT_U—Upper Byte of Failing Data

IF1RFDAT_L—Lower Bytes of Failing Data

IF1RMCADR—Base Address of Master Client

IF1RSCADR—Base Address of Slave Client

IF1RRCADR—Base Address of Requesting Client

IF1RDCADR—Base Address of Driving Client

IF1RRCERA—Requesting Client's Error Analysis Counters

Bit 0-2 = CC access error count
3-5 = Store access error count
6-8 = Client access error count
9-11 = IFBC error count
12-14 = Total error count

IF1RDCERA—Driving Client's Error Analysis Counters

Bit 0-2 = CC access error count
3-5 = Store access error count
6-8 = Client access error count
9-11 = IFBC error count
12-14 = Total error count

IF1RBSERA—Bus and Subsystem Error Analysis Counters

Bit 0-5 = IFB 0 error count
6-11 = IFB 1 error count
12-17 = IFB subsystem error count

IF1RERATW—IFB Error Analysis Timing Word

Bit 0-11 = Error analysis timer
23 = Error analysis timing enable

IF1RLTPASAV—Program Address at Logical Test Failure

IF1RLTTASAV—Test Address at Logical Test Failure

IF1RLTTOSAV—Test Options and Flags

IF1RLTFSAV—F Register at Point of Logical Test Failure

IF1RLTGSAV—G Register at Point of Logical Test Failure

IF1RLTJSAV—J Register at Point of Logical Test Failure

IF1RLTKSAV—K Register at Point of Logical Test Failure

IF1RLTLSAV—L Register at Point of Logical Test Failure

IF1RLTXSAV—X Register at Point of Logical Test Failure

IF1RLTYSAV—Y Register at Point of Logical Test Failure

IF1RLTZSAV—Z Register at Point of Logical Test Failure

IF1RICRAA—Implicated Client's Recovery Action Analysis Counters

Bit 15-17 = Client removal denied counter
18-20 = Client program no action counter
21-23 = Client tests run counter

IF1RBSRAA—Bus and Subsystem Recovery Action Analysis Counters

Bit 0-2 = IFB removal denied counter
3-5 = IFB 0 test run counter
6-8 = IFB 1 test run counter
9-11 = CC removal denied counter
12-14 = Successful status update counter
15-17 = Subsystem tests run counter
18-20 = Memory unit recovery failure counter

IF1RRAATW—Recovery Action Analysis Timing Word

Bit 0-5 = Recovery action analysis timer
23 = Recovery action analysis timing enable

IF1RDTW—IFB Double Trouble Word

Bit 0-5 = Reason for double trouble (octal)
1 - Client program requested a bootstrap
2 - Status update was attempted and failed
3 - Invalid configuration detected
4 - Client program no action threshold exceeded
5 - Client remove denied threshold exceeded
6 - Client tests run threshold exceeded
7 - IFB 0 tests run threshold exceeded
10 - IFB 1 tests run threshold exceeded
11 - IFB remove denied threshold exceeded
12 - CC remove denied threshold exceeded
13 - Status update threshold exceeded
14 - Subsystem tests run threshold exceeded
15 - Pre-termination access test failed
16 - Memory unit recovery failure threshold exceeded
23 = Indicates a bootstrap is necessary

IF1RDTADR—Program Address Where Double Trouble Condition was Detected

IF1RSEMERG—IFB Emergency Action Word

Bit 0-3 = Emergency action state
6-17 = Emergency action timer
23 = Emergency action timing enable

IF1RB0ANALX—IFB 0 Long Term Trouble Analysis Counter

IF1RB1ANALX—IFB 1 Long Term Trouble Analysis Counter

IF1RBANAL—IFB Long Term Trouble Analysis Timing Word

Bit 0-11 = Long term trouble analysis timer
23 = Long term trouble analysis timing enable

IF1RBLW—IFB Base Level Maintenance Word

Bit 0-6 = Member number of suspect unit
7-13 = Unit type number of suspect unit
18-20 = BLM client ID
21-23 = BLM client error code

IF1RBLADR—Program Address Where BLM was Called

IF1RSTAT_AR0-IF1RSTAT_AR23—IFB Client Status Following Recovery

Bit 0 = IFB client is OOS
1 = IFB client is stopped
3 = IFB client is active
4 = IFB client is standby
5 = IFB client is forced
6 = Request DGN for IFB client
8 = IFB client is being restored
9 = Do not restore IFB client

IF1RBSTAT_AR—IFB Status Following Recovery

Bit 0 = IFBC activity in active CC
1 = IFB 0 trouble set in active CC
2 = IFB 1 trouble set in active CC
3 = IFBC activity in standby CC
4 = IFB 0 trouble set in standby CC
5 = IFB 1 trouble set in standby CC
8 = IFB subsystem is stopped
9 = Do not restore IFB

Interface Bus Bootstrap Failure Data

FAIL_NUM	PROGADDR	TESTADDR	TESTOPTS	SAVF	SAVG
SAVJ	SAVK	SAVL	SAVX	SAVY	SAVZ
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.

FAIL_NUM—Number of Access Test Failures

PROGADDR—Program Address at Failure or:

- Base address of client if client is implicated
- Address of memory if store failure
- 0 for CC0 or 1 for CC1
- 0 for IFB0 or 1 for IFB1

TESTOPTS—Test Options and Flags at Failure. Also Indicates Failing Options:

Bit 0 = Active CC failed
1 = Standby CC failed
2 = Store failed
3 = IFB failed
4 = IFB client failed

SAVF-SAVZ—Save of Register Content When the Failure was Reported

NOTE:
The failure block consists of one or more instances of failure information with the size of decimal 12. The failure information was filled to the last one.

Interface Bus Client Registers

The hardware registers for the clients are defined as follows:

IF1CID—IFB Client Circuit Identification Register

Bit 0-9 = Circuit pack name

IFBCMID—IFB Microcode Circuit Identification Register

Bit 0-9 = Microcode name

IFBCSTA—IFB Client Status Register

Bit 0-3 = Received Data Parity
4 = Last cycle was read
5 = Last cycle was write
6 = Last cycle was block DMA
7 = Last cycle was word DMA
8 = Last cycle was client to client
9 = Operational interject active
10 = Maintenance interject active
11 = Maintenance interrupt active
12 = Block DMA request
13 = Word DMA request
14 = Client to client request
15 = Reserved
16-31 = Client option

IFBCCTL—IFB Client Control Register

Bit 0 = Client IFB enable
1-2 = Reserved
3 = Operational interject enable
4 = Maintenance interject enable
5 = Maintenance interrupt enable
6 = Operational interject clear
7 = Maintenance interject clear (client error)
8 = Maintenance interrupt clear (IFB error)
9 = In-service
10 = Update in-progress
11 = Reset client
12-31 = Client option

IFBCESR—IFB Client Error Source Register

Bit 0 = DMA lower limit exceeded
1 = DMA upper limit exceeded
2 = Detected no all-seems-well
3 = Detected all-seems-well failure
4 = Master detected data parity error
5 = Slave detected data parity error
6 = Slave detected control error
7 = Slave detected unused address error
8 = Slave detected address parity error
9 = Sent all-seems-well failure
10 = Client error (Maintenance interject)
11 = IFB error (Maintenance interrupt)
12-15 = Reserved
16-31 = Client option

IFBCLLA—IFB Client Lower Limit Address Register

Bit 8-23 = Lowest DMA address

IFBCULA—IFB Client Upper Limit Address Register

Bit 8-23 = High DMA address limit

IFBCDAT—IFB Client Data Register

Bit 0-31 = Client option

Interface Bus Client Stack- Active

AC1FST_HI	AC1FST_LOW	AC1FLT_HI	AC1FLT_LOW	AC1FLA_HI	AC1FLA_LOW
AC1FLD_HI	AC1FLD_LOW	AC1FST_HI	AC1FST_LOW	AC1FLT_HI	AC1FLT_LOW
AC1FLA_HI	AC1FLA_LOW	AC1FLD_HI	AC1FLD_LOW	AC1FST_HI	AC1FST_LOW
AC1FLT_HI	AC1FLT_LOW	AC1FLA_HI	AC1FLA_LOW	AC1FLD_HI	AC1FLD_LOW
AC1FST_HI	AC1FST_LOW	AC1FLT_HI	AC1FLT_LOW	AC1FLA_HI	AC1FLA_LOW
AC1FLD_HI	AC1FLD_LOW	AC1FST_HI	AC1FST_LOW	AC1FLT_HI	AC1FLT_LOW
AC1FLA_HI	AC1FLA_LOW	AC1FLD_HI	AC1FLD_LOW	AC1FST_HI	AC1FST_LOW
AC1FLT_HI	AC1FLT_LOW	AC1FLA_HI	AC1FLA_LOW	AC1FLD_HI	AC1FLD_LOW

NOTE:
Change AC1 to ST1 for standby IFBC Stack

AC1FST_HI— Upper Byte of Active IFBC Status Stack

AC1FST_LOW— Lower Bytes of Active IFBC Status Stack

AC1FLT_HI— Upper Byte of Active IFBC Last Transaction Stack

AC1FLT_LOW— Lower Bytes of Active IFBC Last Transaction Stack

AC1FLA_HI— Upper Byte of Active IFBC Last Transfer Address Stack

AC1FLA_LOW— Lower Bytes of Active IFBC Last Transfer Address Stack

AC1FLD_HI— Upper Byte of Active IFBC Last Transfer Data Stack

AC1FLD_LOW— Lower Bytes of Active IFBC Last Transfer Data Stack

MUP- Master Control Complex and Utility Processor Printouts

Unique MUP Data (Long Format)

MC1RCID0	MC1RMID0	MC1RSTA0U	MC1RSTA0	XXXXXXX	MC1RCTL0
MC1RESR0U	MC1RESR0	MC1RDAT0U	MC1RDAT0	MC1RINST0U	MC1RINST0
MC1RRPLY0U	MC1RRPLY0	XXXXXXX	XXXXXXX	MC1RSTAT0	MC1RSTAT0A
XXXXXXX	XXXXXXX	MC1RSDAT0UB	MC1RSDAT0B	MC1RSINST0UB	MC1RSINST0B
MC1RCID1	MC1RMID1	MC1RSTA1U	MC1RSTA1	XXXXXXX	MC1RCTL1
MC1RESR1U	MC1RESR1	MC1RDAT1U	MC1RDAT1	MC1RINST1U	MC1RINST1
MC1RRPLY1U	MC1RRPLY1	XXXXXXX	XXXXXXX	MC1RSTAT1	MC1RSTAT1A
XXXXXXX	XXXXXXX	MC1RSDAT1UB	MC1RSDAT1B	MC1RSINST1UB	MC1RSINST1B
MC1RFIB	MC1RFIB+1	MC1RFIB+2	MC1RSRTB	MC1RCTSWTB	MC1RLRTB
MC1RSIB	MC1RSIB+1	MC1RSIB+2	MC1RSRCB	XXXXXXX	MC1RLRCB
MC1RSFIB	MC1RSFIB+1	MC1RSFIB+2	MC1RDTBLAB	MC1RBLMRAB	MC1RBLMFIB
MC1RST0FAB	MC1RST1FAB	MC1RCTSWFAB	MC1RST0FIB	MC1RST1FIB	XXXXXXX
MC1RPGMAD	MC1RTSTAD	MC1RTSTOP	MC1RILFSAV	MC1RILGSAV	MC1RILJSAV
MC1RILKSAV	MC1RILLSAV	MC1RILXSAV	MC1RILYSAV	MC1RILZSAV	XXXXXXX

MC1RCID0—MUP 0 Client ID Register
MC1RCID1—MUP 1 Client ID Register

Bit 0-9 = Circuit pack name

MC1RMID0—MUP 0 Microcode ID Register
MC1RMID1—MUP 1 Microcode ID Register

Bit 0-9 = Micro code name

MC1STA0U—MUP 0 Status Register
MC1STA1U—MUP 1 Status Register

Bit 24 = Command register is busy

MC1RSTAO—MUP 0 Status Register
MC1RSTA1—MUP 1 Status Register

Bit 0 = Received data parity bit 0
1 = Received data parity bit 1
2 = Received data parity bit 2
3 = Received data parity bit 3
4 = Last cycle was read
5 = Last cycle was write
6 = Last cycle was block DMA
7 = Last cycle was word DMA
8 = Last cycle was client to client
9 = Operational interject active
10 = Maintenance interject active
11 = Maintenance interrupt active
12 = Block DMA request
13 = Word DMA request
14 = Client to client request
16 = MMIO trouble
17 = MUP trouble
18 = MUP not forced
19 = MUP not active
20 = Reply complete
21 = Reply in-progress
22 = Reply failure
23 = User option reply

MC1RCTL0—MUP 0 Control Register
MC1RCTL1—MUP 1 Control Register

Bit 0 = Client IFB enable
3 = Operational interject enable
4 = Maintenance interject enable
5 = Maintenance interrupt enable
6 = Operational interject clear
7 = Maintenance interject clear
8 = Maintenance interrupt clear
9 = Indicates MUP is in-service
10 = Indicates MUP is being updated
11 = Reset client
12 = MUP activity control
13 = MUP trouble control

MC1RESROU—MUP 0 Error Summary Register
MC1RESR1U—MUP 1 Error Summary Register

Bit 24 = User defined operation register

MC1RESR0—MUP 0 Error Summary Register
MC1RESR1—MUP 1 Error Summary Register

Bit 2 = Detected no all seems well
3 = Detected all-seems-well failure
4 = Master detected data parity error
5 = MUP detected data parity error
6 = MUP detected control error
7 = MUP detected unused address error
8 = MUP detected address parity error
9 = Sent all-seems-well failure
10 = Client error—Maintenance interject
11 = IFB error—Maintenance interrupt
16 = Sanity timeout
17 = 68010 bus error
18 = DRAM error
19 = Memory access error
20 = Both MUPs active
21 = Software detected error
22 = MUP forced in hardware
23 = User defined operational interject

MC1RDAT0U—MUP 0 Data Register
MC1RDAT1U—MUP 1 Data Register

Bit 24-31 = Upper byte of data

MC1RDAT0—MUP 0 Data Register
MC1RDAT1—MUP 1 Data Register

Bit 0-23 = Lower 3 bytes of data

MC1RINST0U—MUP 0 Instruction Register
MC1RINST1U—MUP 1 Instruction Register

Bit 24-31 = Upper byte of instruction

MC1RDAT0—MUP 0 Instruction Register
MC1RDAT1—MUP 1 Instruction Register

Bit 0-23 = Lower 3 bytes of instruction

MC1RRPLY0U—MUP 0 Reply Register
MC1RRPLY1U—MUP 1 Reply Register

Bit 24-31 = Upper byte of reply register

MC1RRPLY0—MUP 0 Reply Register
MC1RRPLY1—MUP 1 Reply Register

Bit 0-23 = Lower 3 bytes of reply register

MC1RSTAT0—MUP 0 Software Status Before Fault Processing
MC1RSTAT1—MUP 1 Software Status Before Fault Processing

Bit 0 = MUP is troubled
1 = MUP is stopped
3 = MUP is active
4 = MUP is standby
5 = MUP is forced in hardware
8 = MUP is being restored
9 = Do not restore MUP

MC1RSTAT0A—MUP 0 Software Status After Fault Processing
MC1RSTAT1A—MUP 1 Software Status After Fault Processing

Bit 0 = MUP is troubled
1 = MUP is stopped
3 = MUP is active
4 = MUP is standby
5 = MUP is forced in hardware
8 = MUP is being restored
9 = Do not restore MUP

MC1RSDAT0UB—MUP 0 Data Register Before the Last Stop/Start Instruction (Same as MC1RDAT0U)
MC1RSDAT1UB—MUP 1 Data Register Before the Last Stop/Start Instruction (Same as MC1RDAT0U)

MC1RSDAT0B—MUP 0 Data Register Before the Last Stop/Start Instruction (Same as MC1RDAT0)
MC1RSDAT1B—MUP 1 Data Register Before the Last Stop/Start Instruction (Same as MC1RDAT0)

MC1RSINST0UB—MUP 0 Instruction Register Before the Last Stop/Start Instruction (Same as MC1RINST0U)
MC1RSSINST1UB—MUP 1 Instruction Register Before the Last Stop/Start Instruction (Same as MC1RINST0U)

MC1RSINSTOB—MUP 0 Instruction Register Before the Last Stop/Start Instruction (Same as MC1RINST0)
MC1RSSINST1B—MUP 1 Instruction Register Before the Last Stop/Start Instruction (Same as MC1RINST0)

MC1RFIB—MUP Fault Information

Bit 0 = MUP member number
3-4 = MUPs software status on the the IFB
- 1 - Active
- 2 - Standby
- 3 - OOS

6-7 = Method of entry into fault recovery
- 1 - Interject
- 2 - Interrupt
- 3 - BLM

9-12 = Fault type
- 1 - No fault found—interject
- 2 - Both MUPs active—interject
- 3 - Memory access error—interject
- 4 - DRAM error—interject
- 5 - 68000 bus error—interject
- 6 - Sanity time-out—interject
- 7 - Software generated error—interject
- 8 - Forced active—interject
- 9 - Time-out—BLM
- 10 - DMA failed—BLM
- 11 - Hardware-software mismatch—BLM

15 = Multiply fault indicator
18-19 = Starting state
21-22 = Ending state

MC1RFIB+1—Fault Information From Fault Previous to MC1RFIB
MC1RFIB+2—Fault Information From Fault Previous to MC1RFIB+1

MC1RSRTB—MUP Long Range Timer

Bit 0-17 = Short range timer
21 = Short range timer enable

MC1RCTSWTB—MUP Context Switch Timer

Bit 0-9 = Context switch timer
21 = Context switch timer enable
22 = Indicate a restore command has been sent
23 = Context switch abort indicator

MC1RLRTB—MUP Long Range Timer

Bit 0-17 = Long range timer
21 = Long range timer enable

MC1RSIB—Steps Taken During Fault Processing

Bit 0 = Determine interrupt/interject type
1 = Both MUPs have same hardware activity state
3 = Both MUPs are active software state
4 = Hardware—Software match
6 = Recover both MUPs
7 = Remove standby MUP
9 = Restart MUP
10 = Get MUP information
12 = Reset MUP
13 = Switch MUPs
15 = Switch context
16 = DTBL called

MC1RSIB+1—Steps Taken During Processing for Fault Previous to MC1RSIB
MC1RSIB+2—Steps Taken During Processing for Fault Previous to MC1RSIB+1

MC1RSRCB—MUP Short Range Counter

Bit 0-4 = Number of force related entries

MC1RLRCB—MUP Long Range Counter

Bit 0-8 = MUP 0 long range counter
12-20 = MUP 1 long range counter

MC1RSFIB—Indicates Which Steps Failed During Fault Processing

Bit 0 = Determine interrupt/interject type
1 = Both MUPs have same hardware activity state
3 = Both MUPs are active software state
4 = Hardware—Software match
6 = Recover both MUPs
7 = Remove standby MUP
9 = Restart MUP
10 = Get MUP information
12 = Reset MUP
13 = Switch MUPs
15 = Switch context
16 = DTBL called

MC1RSFIB+1—Indicates Which Steps Failed During Fault Processing for Fault Previous to MC1RSFIB
MC1RSFIB+2—Indicates Which Steps Failed During Fault Processing for Fault Previous to MC1RSFIB+1

MC1RDTBLAB—DTBL Determination Address

MC1RBLMRAB—Return Address of the Caller of a BLM

MC1RBLMFIB—Fault Information from Caller of a BLM

MC1RST0FAB—State 0 Failing Address

MC1RST1FAB—State 1 Failing Address

MC1RCTSWFAB—Context Switch Failing Address

MC1RST0FIB—State 0 Failing Information

Bit 0-17 = Lower bits of MUP reply register
18-23 = Instruction status of restart instruction

MC1RST1FIB—State 1 Failing Information

Bit 0-23 = Lower bits of MUP reply register

MC1RPGMAD—Program Address at Failure

MC1RTSTAD—Test Address at Failure

MC1RTSTOP—Test Option

Bit 0 = Active CC failed
1 = Standby CC failed
2 = Store failed
3 = IFB failed
4 = IFB client failed
5 = False response test failed
6-12 = Client unique failure information
6 - MUP audit(s) failed
7 - MUP audit(s) failed no DMA data
8 - Active CC failed
9 - Standby CC failed
13 = Client delay segment break request flag
14 = Test standby configuration
15 = On standby configuration
16 = Run test on base level
17 = No PS test
18 = No CS test
19 = No CC test
20 = Test IFB controller
21 = Test IFB client
22 = Test store access
23 = False response test

MC1RILFSAV—F-Register at Time of MUP Acesss Test Failure

MC1RILGSAV—G-Register at Time of MUP Acesss Test Failure

MC1RILJSAV—J-Register at Time of MUP Acesss Test Failure

MC1RILKSAV—K-Register at Time of MUP Acesss Test Failure

MC1RILLSAV—L-Register at Time of MUP Acesss Test Failure

MC1RILXSAV—X-Register at Time of MUP Acesss Test Failure

MC1RILYSAV—Y-Register at Time of MUP Acesss Test Failure

MC1RILZSAV—Z-Register at Time of MUP Acesss Test Failure

Unique MUP Data (Short Format)

FREG GREG TREG XREG

FREG—Fault Encountered by Calling Program

GREG—Originator of BLM Request

TREG—Return Address of Caller

XREG—Invalid MUP Base Address

Unique SSD Data

SS1RCID	SS1RMID	SS1RSTA	SS1RESR	SS1RDAT	SS1RLRTW
SS1RLRCW	SS10ROW40	SS10ROW41	SS10ROW42	SS10ROW43	SS10ROW44
SS10ROW45	SS10ROW46	SS10ROW50	SS10ROW51	SS10ROW52	SS10ROW53
SS10ROW54	SS10ROW55	SS10ROW56			

SS1RCID—SSD 0/1 CID Register

SS1RMID—SSD 0/1 MID Register

SS1RSTA—SSD 0/1 STA Register

SS1RESR—SSD 0/1 ESR Register

SS1RDAT—SSD 0/1 DAT Register

SS1RLRTW—SSD Long Range Timer Word

SS1RLRCW—SSD Long Range Counter Word

SS10ROW40-SS10ROW56—SSD 0/1 Matrix

API/FS- Attached Processor Interface/File Store Printouts

Unique API Data (D-Level, INJ, and BLM Reports)

a. . .a	b. . .b	c. . .c	7. . .0	7. . .0	7. . .0
d. . .d	e. . .e	f. . .f	7. . .0	7. . .0	7. . .0
g. . .g	h. . .h	i. . .i	7. . .0	7. . .0	7. . .0
j. . .j	k. . .k	l. . .l	m. . .m	n. . .n	7. . .0
o. . .o	p. . .p	q. . .q	r. . .r	s. . .s	t. . .t
u. . .u	v. . .v	w. . .w	x. . .x	y. . .y	z. . .z
A. . .A	B. . .B	C. . .C	D. . .D	E. . .E	F. . .F
A. . .A	B. . .B	C. . .C	D. . .D	E. . .E	F. . .F

Defined as:

a = Error information word for state 0.
b = Error information word for state 1.
c = Error information word for state 2.
d = Recovery information word for state 0.
e = Recovery information word for state 1.
f = Recovery information word for state 2.
g = Test link results word for state 0.
h = Test link results word for state 1.
i = Test link results word for state 2.
j = Command system response mode status word.
k = Command system response mode error word.
l = Command system response mode sequence violation word.
m = Command system response mode time-out word.
n = Command system response mode—3B command and data.
o = PIC status word.
p = PIC error word.

q = PIC state word.
r = Link test output (latest result).
s = Timing word.
t = Switch fail output. If the API switch fails, this gives the reason for the failure using APFR error codes.
u = Configure fail output. If the configuration of the API fails, this gives the reason for the failure using APFR error codes.
v = Recovery miscellaneous word.
w = Base level maintenance error word.
x = CNI base level error word. (CNIBLM)
y = CNI interject error word. (TBERSTAT)
z = CNI error information word. (CNIEWD)

NOTE:
Variables A through F print two consecutive times. The first set of variables indicate the configuration failure due to command system failure. The second set of variables indicate the switch failure due to command system failures.

A = Command system initiate mode that contains command and data to be sent to the 3B computer.
B = Command system initiate mode status word.
C = Command system initiate mode error word.
D = Command system initiate mode sequence violation word.
E = Command system initiate mode 3B error word.
F = Command system initiate mode time-out word.

EIW—Error Information Word (State 0, 1, 2)

Bit 0-5 = PIC error type or base level client

PIC Error Types:

1 - CIR BUF ADR and size do not agree with PIC
2 - Pointer check failure
3 - Illegal CIR_BUF command
4 - 1B CMD register inhibited
5 - AU bus sequencer inhibited
6 - AU ADR range error
7 - AP bus parity failure
10 - PIC bus parity failure
11 - CMD check error
12 - MTC BUF address not loaded
13 - Illegal PIC RAM ADR specified
14 - PIC error
15 - Illegal instruction
20 - TB Load/End pointer fault
21 - TB unload pointer fault
22 - TB self-pointer fault
23 - TB address calculation error
24 - TB invalid header pointer

Base Level Client:

10 - Link integrity monitor (LIM)
20 - SAWS audit (SADK)
30 - APS message handler (APMH)
40 - Functional subroutines (FNCTSUBS)
50 - Common network interface (APMHCNI)

6-7 = API command parity failure

1 - Failed on write operation
2 - Failed on read operation

8 = Interrupt from on-board DGN

EIW—Error Information Word (State 0, 1, 2) (Contd)

Bit 9-11 = 3B Computer Error Type
- 1 - 3B computer buffers initialized
- 2 - 3B computer has marked an API OOS
- 3 - 3B computer system has initialized
- 4 - API sent 3B computer a PIC interrupt
- 7 - CMD system response mode failure

12 = 3B computer interrupt
13 = Dump RAM from active API
14 = Interrupt from active API
15 = Interrupt from standby API
16 = Multiple PIC errors
17 = PIC error detected
18 = No active API for this APS
19 = Unknown CMD received from 3B computer
20 = Error threshold exceeded
21 = Buffer initialization required
22 = No error found
23 = Base level recovery information

RIW—Recovery Information Word (State 0, 1, 2)

Bit 0-2 = Next recovery state
- 0 - Reconfigure active API
- 1 - Switch APIs
- 2 - Initialize COM buffers

3 = APS link test OK
4 = 3B computer buffers were initialized
5 = APS link test failed
6 = Standby APS was removed
7 = Buffer initialization failed
8 = Buffer initialization OK—Threshold exceeded
9 = API configuration failed
10 = API switch failed
11 = No configuration was found
12 = API configuration successful
13 = API switch successful
14 = Buffer initialization successful
15 = APDRV was initialized
16 = 3B has been booted
17 = CNI Stream initialization successful
23 = Pre-duplex fail analysis begun

TL Results—Test Link Results (State 0, 1, 2)

Bit 0 = API cannot be accessed
1 = 3B computer cannot be accessed
2 = 3B computer initialized COM_BUF
3 = 1B to 3B computer link OK

RM Status—Response Mode Status

Bit 0-2 = Response mode states
0 - Idle state
1 - Sync ACK sent state
2 - CMD received state
3 = CMD to API error
4 = CMD sequence violation
5 = CMD response time-out
6-14 = CMD response state code (see APFR error codes)

RM Error—Response Mode Error

Bit 0-5 = Failing command (see API commands)
9-20 = Command error code (see APFR error codes)

RM SEQ VIOL—Response Mode Sequence Violation

Bit 0-23 = (See Command Register Layout, following)

RM Timeout—Response Mode Time-Out

Bit 0-23 = (See Command Register Layout, following)

RM CMD Register—Response Mode Command Register

Bit 0-7 = Interprocessor command
8-15 = 3B computer error type
1 - 3B computer buffers initialized
2 - 3B computer has marked an API OOS
3 - 3B computer system has initialized
4 - APS sent 3B computer a PIC interrupt
7 - CMD system response mode failure

PIC Status—PIC Status Word

Bit 0 = PC emulation mode
1 = Interrupt generated by 1B alert
2 = Interrupt generated by 3B computer alert
3 = Interrupt generated by 3B computer system interrupt
4 = 1B alert function disabled
5 = 3B computer alert function disabled
6 = 1B error checking disabled
7 = 3B computer error checking disabled
8 = 1B side in loop-around mode
9 = 3B computer side in loop-around mode
10 = DMA suspended by 1B
11 = DMA suspended by 3B computer
12 = Interrupt generated by PIC error
13 = Interrupt generated by PC
14 = Interrupt generated by 1B system interrupt
15 = Interrupt generated by DGN

PIC Error—PIC Error Word

Bit 0 = BIC time-out
1 = Actual read in offset or size error
2 = 1B CMD register inhibited
3 = AU bus sequencer inhibited
4 = AU ADR range error
5 = Parity failure on AP bus
6 = Parity failure on PIC bus
7 = Pointer check failure
8 = Command check error
9 = Maintenance buffer address not loaded
10 = Illegal PIC RAM address specified
11 = PIC error
12 = BIC error
13 = DMA word count error
14 = Illegal circular buffer command
15 = Illegal instruction

PIC State—PIC State Word

Bit 0-2 = PIC state code
0 - No status
1 - Active
2 - Standby
3 - OOS

TL Output—Test Link Output

Bit 0 = AP1 cannot be accessed
1 = 3B computer cannot be accessed
2 = 3B computer initialized COM_BUF
3 = 1B to 3B computer link OK

Timing Word

Bit 0-11 = Counter for half-hour timing
12-21 = Counter for state sequence timing
22 = Half-hour timing enable
23 = State sequence timing enable

Switch Failure—API Switch Failure Code

Bit 0-11 = (See APFR Error Codes)

CONFIG Failure—API Configuration Failure Code

Bit 0-11 = (See APFR Error Codes)

MISC Recovery—Recovery Miscellaneous Word

Bit 0-5 = Not Used
6-8 = APS Number
9-14 = Count of successful buffer initializations
15-17 = State upon entry into fault recovery
18 = APDRV initialization
19 = 3B boot
20 = Pre-duplex fail analysis in-progress
21-23 = Level of phase requested on 3B

BLM Error—Base Level Maintenance Error Word

Client = APS Message Handler
Octal 3 = No active API for this APS

Client = Disk system audit
Octal 2 = No disk request completions
Octal 5 = Circular buffer invalid
Octal 30 = Bad currency pointers
Octal 34 = No completions FMI non-1B file jobs
Octal 35 = No completions non-FMI jobs

Client = Link integrity monitor (LIM)
Bit 0 = LIM command to API error
1 = LIM no access to CMD register
2 = LIM command time-out
3 = API is active
4 = API is standby
5 = 3B computer configuration request detected
6 = 3B computer DMA is suspended
7 = 3B computer is not responding
8 = Error during API status word read
9-12 = Specific API Kcode
13 = Bad status—No active API
14 = Bad status—Active/active API's
15-21 = LIM time count
22 = LIM time-out
23 = LIM timing in progress

IM CMD/Data—Initiate Mode CMD and Data

Bit 0-7 = Interprocessor command
8-15 = Data to be sent to 3B computer
(except for configuration API command)
8-11 = MEMN to be configured (CONF_API CMD only)
12-15 = Configuration state for MEMN (CONF_API CMD only)
0 - Unit not operational
1 - API is active and in-service
2 - API is standby and in-service
3 - API is OOS
4 - API is in the initialization state

IM Status—Initiate Mode Status Word

Bit 0-2 = Present command system state
0 - Idle
1 - Sync command sent
2 - Sync acknowledge received
3 - Command sent
4 - Command acknowledge received
5 - Null command sent
6 = Command to API error
7 = Sequence violation—Sync from 3B computer
8 = Time-out error
9 = 3B computer had error while processing CMD
12-14 = Command to API error count
15-16 = Command acknowledge time-out
17-21 = Sync acknowledge time-out
22 = Final time-out

IM Error—Initiate Mode Error Word

Bit 0-5 = Failing command (See API Commands, following)
9-20 = Command error code (See APFR Error Codes, following)
21-23 = Command system state
0 - Idle
1 - Sync command sent
2 - Sync acknowledge received
3 - Command sent
4 - Command acknowledge received
5 - Null command sent

IM SEQ VIOL—Initiate Mode Sequence Violation Word

Bit 0-23 = (See Command Register Layout, following)

Command Register Layout

Bit 0-5 = Command OPCODE (See API Commands, following)
6-7 = Command disposition code
0 - Completed
1 - Failed
2 - In progress
3 - CMD loaded in CMD register
8-23 = Data field

IM 3B Error—Initiate Mode 3B Computer Error Word

Bit 0-23 = (See Command Register Layout, following)

IM Timeout—Initiate Mode Time-Out Word

Bit 0-23 = (See the preceding Command Register Layout)

API Commands (Octal)

0 = Invalid command
1 = MTC_BUF size (send and receive)
2 = Lower 16 bits of 1B send MTC_BUF
3 = Upper 6 bits of 1B send MTC_BUF
4 = Lower 16 bits of 1B receive MTC_BUF
5 = Upper 6 bits of 1B receive MTC_BUF
6 = Load RAM at 16-bit ADR from my sent MTC_BUF
7 = Dump RAM at 16-bit ADR to my receive MTC_BUF
10 = Copy my sent MTC_BUF to other receive MTC_BUF
11 = Copy my receive MTC_BUF unload PTR to other send MTC_BUF unload PTR
12 = Send interrupt to other side
13 = Disable on-board DGN
14 = Suspend DMA except for MTC_BUF commands
15 = Resume DMA from point of suspension
16 = Read 8-bit DMA job number
17 = Abort DMA job in progress (if any)
20 = Disable PIC loop-around mode
21 = Enable PIC loop-around mode
22 = Disable all error checks
23 = Enable all error checks
24 = Read 16-bit API status word
25 = Clear through mask 16-bit API status word
26 = Read 16-bit API error word
27 = Clear through mask 16-bit API error word
30 = Read 16-bit API state word
31 = Write 16-bit API state word
32 = Initiate AU DGN helper
33 = Enable on-board DGN
34 = Disable alert function

API Commands (Octal) (Contd)

35 = Enable Alert Function
36 = Send 16-bit data to other processor
37 = Receive 16-bit data from other processor
40 = Disable PC emulation
41 = Enable PC emulation
42 = Send interprocessor data to other side (IPD)
43 = Read status/error word (TBERSTAT)
44 = Update status/error word (TBERSTAT)

APFR Error Codes (Octal)

100 = Failed to get buffer information from message handler
101 = API command failure
102 = Failed to restore common hardware
103 = Failed, forced by ROS key
104 = Failed, unit active main
105 = Failed, bus OOS
106 = Failed, unit not in operational state
107 = UTYP to K-code conversion failed
110 = Immediate fail return from message handler on sending message
111 = MCC forced API 00S
112 = Time-out, no message ACK on COM_BUF RST MSG to 3B computer
113 = API command time-out
114 = API command never started processing
115 = Loop-around message not in REC BUF
116 = Mate status fail, MEMN does not exist
117 = Cannot access CMD register in the API
120 = Incorrect final status detected
121 = The test message has failed
122 = The CMD system has failed
123 = An attempt was made to restore active-active
124 = Message handler failed to initialize COM_BUF
125 = No active API found for this APS
126 = Active MEMN for this APS is not operational
127 = Message handler failed to send message
130 = Time-out waiting for message ACK
131 = ACK message from 3B computer was no good
132 = No active in-service API

APFR Error Codes (Octal) (Contd)

133 = Status shows active-active state
134 = Message handler failed to initialize XCOM_BUF
135 = Initial CMD response failed
136 = CMD not sync, sequence violation occurred
137 = SACK CMD to IP_WORD failed
140 = 3B computer CMD was not found
141 = CMD response time-out in wait routine
142 = CACK CMD to IP_WORD failed
143 = Received protocol CMD, expected CMD command
201 = APS MEMN out of range
202 = Fail to restore OOS mate API before switching
203 = MEMN to base address conversion failed
204 = Switch API failed due to the OOS mate API
205 = API is powered down
206 = API is already OOS

Attached Processor Interface Dump RAM Data (API Firmware code MC5A014)

76543210	76543210	76543210	76543210	h------h	i------i
j------j	k------k	l------l	m------m	n------n	o------o
p------p	q------q	r------r	s------s	t------t	u------u
v------v	w------w	x------x	y------y	z------z	A------A
B------B	C------C	D------D	E------E	F------F	G------G
H------H	I------I	J------J	K------K	L------L	M------M
N------N	O------O	P------P	Q------Q	R------R	S------S
T------T	U------U	V------V	W------W	X------X	Y------Y
Z------Z	a1----a1	b1----b1	c1----c1	d1----d1	e1----e1
f1----f1	g1----g1	h1----h1	i1----i1	j1----j1	k1----k1
l1----l1	m1----m1	n1----n1	o1----o1	p1----p1	q1----q1
r1----r1	s1----s1	t1----t1	u1----u1	v1----v1	w1----w1
x1----x1	y1----y1	z1----z1	A1----A1	B1----B1	C1----C1
D1----D1	E1----E1	F1----F1	G1----G1	H1----H1	I1----I1
J1----J1	K1----K1	L1----L1	M1----M1	N1----N1	O1----O1
P1----P1	Q1----Q1	R1----R1	S1----S1	T1----T1	U1----U1
V1----V1	W1----W1	X1----X1	Y1----Y1	Z1----Z1	a2----a2
b2----b2	c2----c2	d2----d2	e2----e2	f2----f2	g2----g2
h2----h2	i2----i2	j2----j2	k2----k2	l2----l2	m2----m2
n2----n2	o2----o2	p2----p2	q2----q2	r2----f2	s2----s2
t2----t2	u2----u2	v2----v2	w2----w2	x2----x2	y2----y2
z2----z2	z2----z2	z2----z2	z2----z2	z2----z2	z2----z2

NOTE:
Fields h through z2 are explained in DUMP RAM field definitions that follow.

DUMP RAM Field Definitions

The following is the dump of the PIC RAM from the API that detected the error:

h = Send COM/XCOM address offset
i = Send COM/XCOM size
j = Send COM/XCOM load pointer
k = Send COM/XCOM unload pointer
l = Receive COM/XCOM virtual offset
m = Receive COM/XCOM size
n = Receive COM/XCOM load pointer
o = Receive COM/XCOM unload pointer
p = Send job buffer state vector and number of words
q = Send job buffer DMA address
r = Send job buffer client information
s = Send job buffer from, time and number
t = Send auditing timing information
u = Spare
v = Spare
w = Send job buffer checksum
x = Receive job buffer state vector and number of words
y = Receive job buffer DMA address
z = Receive job buffer client information
A = Receive job buffer from time and number
B = Receive auditing timing information
C = Spare
D = Spare
E = Receive job buffer checksum
F = PIC status register
G = Error Status register
H = Send MTCE Buffer virtual address for 3B
I = Receive MTCE Buffer virtual address for 3B
J = Send MTCE Buffer address for 1B
K = Receive MTCE Buffer address for 1B
L = Send COM/XCOM Buffer virtual address for 3B

DUMP RAM Field Definitions (Contd)

M = Receive COM/XCOM Buffer virtual address for 3B
N = Send COM/XCOM Buffer address for 1B
O = Receive COM/XCOM Buffer address for 1B
P = Size of MTCE Buffer in 3B
Q = Size of MTCE Buffer in 1B
R = Size of COM/XCOM Buffer in 3B
S = Size of COM/XCOM Buffer in 1B
T = MTCE job buffer offset in 3B
U = MTCE job buffer address in 1B
V = COM/XCOM job buffer offset in 3B
W = COM/XCOM job buffer offset in 1B
X = Size of MTCE job buffer in 3B
Y = Size of COM/XCOM job buffer in 3B
Z = Size of MTCE job buffer in 1B
a1 = Size of COM/XCOM job buffer in 1B
b1 = Number of MTCE job buffers in 3B
c1 = Number of COM/XCOM job buffers in 3B
d1 = Number of MTCE job buffers in 1B
e1 = Number of COM/XCOM job buffers in 1B
f1 = Interprocessor word sent by 3B
g1 = Interprocessor word sent by 1B
h1 = PIC detailed error information
i1 = API State word
j1 = Expanded DMA job number for send MTCE buffer
k1 = DMA requested during CNI
l1 = DMA In
m1 = DMA Out
n1 = Direction of interrupted DMA job
o1 = Common/CNI buffer polling rate
p1 = Firmware version date
q1 = Current 1B DMA job number

DUMP RAM Field Definitions (Contd)

r1 = Current 3B DMA job number
s1 = Memory integrity check word
t1 = Send TB headers address in 1B
u1 = Send TB buffer address in 1B
v1 = Send TB buffer end address in 1B
w1 = Send TB load pointer
x1 = Send TB unload pointer
y1 = Receive TB headers address in 1B
z1 = Receive TB buffer address in 1B
A1 = Receive TB buffer end address in 1B
B1 = Receive TB load pointer
C1 = Receive TB unload pointer
D1 = Pointer state during TB pointer update
E1 = Spare
F1 = Spare
G1 = Spare
H1 = Spare
I1 = Spare
J1 = API scanning status in 3B
K1 = DLN scanning status in 3B
L1 = Incoming TB start virtual address in 3B
M1 = Incoming TB end virtual address in 3B
N1 = Outgoing TB start virtual address in 3B
O1 = Outgoing TB end virtual address in 3B
P1 = Outgoing TB load pointer in 3B
Q1 = Outgoing TB end pointer in 3B
R1 = Incoming TB unload pointer in 3B
S1 = Incoming TB load pointer in 3B
T1 = Incoming TB end pointer in 3B
U1 = Outgoing TB unload pointer in 3B
V1 = Spare

DUMP RAM Field Definitions (Contd)

W1 = Spare
X1 = Spare
Y1 = Spare
Z1 = Send TB virtual address in 1B
a2 = Receive TB virtual address in 1B
b2 = Spare
c2 = Send and receive TB virtual address in 3B
d2 = TB error threshold and TB DMA transfer size for 1B
e2 = TB DMA transfer size for 3B
f2 = TB send load and receive unload error count
g2 = TB incoming load and outgoing unload error count
h2 = Interprocessor data word going to 3B from 1B
i2 = Interprocessor data word going to 1B from 3B
j2 = TB error and status word
k2 = TB DMA segment index
l2 = Spare
m2 = Spare
n2 = Spare
o2 = Spare

The following words are the contents of the last message processed by the API:

p2 = First word of APS message (From, Size, To)
q2 = Message AP type and sequence number
r2 = Message client identification
s2 = Spare
t2 = Message Checksum
u2 = Message options field
v2 = Message time and number of words
w2 = Message address
x2 = Message ETIME field
y2 = Spare
z2 = Message data

Attached Processor Interface General Control Pulse (GCP) Reply

Bit 0 = Maintenance interject request
1 = Maintenance flip-flop set side
2 = Maintenance flip-flop reset side
3 = Clock activity error
4-5 = Not used
6 = CC input address parity error
7 = CC input data parity error
8 = Not used
9 = CC out-of-range address error
10 = CC mode error
11 = K-code bit 11
12 = K-code bit 12
13 = K-code bit 13
14 = K-code bit 14
15 = K-code bit 15
16 = CC interface sequencer error
17 = K-code match detected
18 = Control read more detected
19 = Control write mode detected
20 = All ones address and PKA detected
21 = All zeros address and PKA detected
22 = All ones data and P1, P2 detected
23 = All zeros data and P1, P2 detected

Interprocessor Commands (Octal)

0 = NULL command

1 = Unassigned

2 = Synchronization Command

3 = Synchronization acknowledgement command

4 = IP_CMD command acknowledgement

5 = Reinitialize all COM_BUF resources
(including in-service APIs)

6 = Initialize in-service APIs to COM_BUF

7 = Reinitialize all XCOM_BUF resources
(including in-service APIs)

10 = Configure API as specified

11 = APS error detected (3B computer only)

12 = PS 0 Pump Request
Option 1 - Pump the first quarter of PS 0
Option 2 - Pump the first quarter of PS 0
Option 3 - Pump the first quarter of PS 0
Option 4 - Pump the first quarter of PS 0

13 = Select logical 1B-File for normal request as specified
Option 1 - Logical normal file
Option 2 - Logical update file

14 = Load PCRVPUMP into 3B Computer main memory
Option 1 - PCRVPUMP copy at DADR 200

15 = Request 3B computer to check for buffer initialization

16 = Request initialization of APDRV

17 = Request to boot the 3B system

CNI Base Level Error Word

Bit 0-2 = Type of error (See CNI Error Types, following)
3 = Side that was in error:
Set = 1B side
Reset = 3B side
4-5 = Message direction at time of error
(See Message Direction, following)
6 = CNI buffer initialization requested

Message Direction

Bit 0 = Direction was incoming to the 1B
1 = Direction was outgoing from the 1B

CNI Error Types (Octal)

1 = Self-pointer error
2 = Unload pointer error
3 = Buffer overflow error
4 = Load/end pointer error
5 = Client requested BLM error
6 = Bad messages error

CNI Error Information Word

Bit 0-2 = CNI Fault type (See CNI Error Types)
3 = Processor side that is in error:
Set = 1B
4-5 = Message direction at time of error. (See message direction)
6 = CNI buffer initialization request
7 = Request that stream be stopped

CNI Interject Error Word

Bit 0 = Self-pointer fault (TB)
1 = Unload pointer fault (TB)
2 = Load/end pointer fault (TB)
3 = Side of fault;
Set = 1B side
Reset = 3B side
4 = Stream direction; Set = from 1B, Reset = to 1B
5 = Current buffer in use;
Set = TB
Reset = CB
6 = Invalid CNI buffer header pointer
7 = Invalid pointer address
8-11 = Buffer forced out of service (diagnostics only)
12-15 = TB Scanning activated (See TB status)

TB Status

Bit 0 = Send TB for 1B active—outgoing stream
1 = Receive TB for 1B active—incoming stream
2 = Receive TB for APS active—outgoing stream
3 = Send TB for APS active—incoming stream

File Store Disk Identification Tag Definitions

MNEMONIC	Bit	
MAINT*	0	Used by FS fault recognition and diagnostics
GEN*	1	For all loader-generated data
LIB*	2	For nongeneric special programs
ODA*	3	For all ODA translations and parameters
FREE	4	For all sectors not assigned to any other ID
HIST	5	For error analysis trouble histories
TRANS	6	For all COMPOOL defined and engineered transient data
NWM*	7	For all display page infomation
TKMTC	8	For trunk status infonation
MERGE	10	For core-disk and hash tables
RCRB*	11	For recent change rollback infomation
TPM*	12	For traffic and plant schedules
OSDATA	13	OSOR long-term extended storage IDTAG

* Indicates memory areas which are hashed normally by SAWS.

File Store Error Correction Data (FSECD)

WORDS DISKADD ID FLAGS

WORDS—Number of Words Corrected by Status Failure Control

DISKADD—Start Disk Address of Correction

ID—ID Tag Associated with Record

FLAGS—Correction Control Flags

Bit 1 = Disk write is for copy
2 = Disk job being dispensed as cancel request
3 = Reread failed
4 = ID is provided by client
5 = Client requests all writes be verified
6 = Buffer Choice:
0 - Priv buffer
1 - MAC paged area
7 = Data transfer in-progress
8 = Data transfer is waiting for completion of disk write
9 = Data transfer is delayed by no DRRs
10 = Request pending completion by FSC
11 = Give client an immediate return
13 = DF is in update mode
14 = Task dispenser loaded DRR for data transfer
18 = About copy operation at first opportunity
19-20 = Priority of copy client
21 = Rewite same file
22-23 = Error correction code:
0 - Copy mode
1 - IDMM
2 - UTRAMM
3 - Exerciser error

MAC- Maintenance Control Printouts

Maintenance Control Memory Layout

CNTL+0	CNTL+1	CNTL+2	CNTL+3	CNTL+4	CNTL+5
CNTL+6	CNTL+7	CNTL+8	CNTL+9	CNTL+10	CNTL+11
CNTL+12	CNTL+13	CNTL+14	CNTL+15	CNTL+16	CNTL+17
CNTL+18	CNTL+19	CNTL+20	CNTL+21	CNTL+22	CNTL+23
CNTL+24	INFO +0	INFO +1	INFO +2	INFO +3	INFO +4

NOTE:
Prefix all words with MA1.
This dump can appear up to four times. Once for each of the three possible active maintenance control (MAC) clients (MAC1, MAC2, MAC3) and once for a generic utility client.

CNTL +0

Bit 0-18 = Job type—program—task
19-21 = Class wait states
State 0 = Normal state
State 1 = Disk operations occurring
State 2 = TTY message being processed
State 3 = Timing taking place
State 4 = Page loading in progress
State 5 = Tape operations in progress

State(s) 6 and 7 are unassigned
22 = CPSECT loaded
23 = Scratch pad activity flag (that is, SCR pad is assigned)

CNTL +0

Bit 0-14 = Program task

CNTL +0

Bit 0-6 = Task number
7-14 = Program number (MA1PGM)
15-18 = Job type (MA1JTYPE)

CNTL +1

Bit 0 = Mask AUINJ interject source
1 = Mask invalid interrupts
2 = Mask APINJ interject source
3 = Mask out-of-range interrupts
4 = Mask APUFS interject source
5 = Mask PUFS interrupt source
6 = Mask ELS interrupt source
7 = Mask SCDS interrupt source
8 = Mask pads interrupt source
9 = Mask AUDS interrupt source
10 = Mask CSDS interrupt source
11 = Mask CLIS interrupt source
12 = Mask SCUFS interrupt source
13 = Mask ORDS interrupt source
14 = Mask all interrupts
15 = Mask PSBSO interrupt source
16 = Mask error stop
17 = Mask AU base level maintenance
18 = Mask IO base level maintenance
19 = Mask PU base level maintenance
20 = Mask KLOS interrupt source
21 = Mask KL1S interrupt source
22 = Mask KL2S interrupt source
23 = Mask KL3S interrupt source

CNTL +2

Bit 0-22 = Client's next segment address
23 = Inhibit call interrupt

CNTL +3

Bit 0-22 = Client's abort address
23 = Client's abort leg in progress

CNTL +4

Bit 0-13 = Unit-type member number

CNTL +4

Bit 0-6 = Member number
7-13 = Unit-type number
14 = Unit-type blockage flag has been set
15 = Page loading completed flag
16 = Client has been aborted by interrupt
17-19 = Abort states
State 0 = Normal state
State 1 = Disk operations failed
State 2 = Maintenance interrupt has occurred
State 3 = Holding time exceeded
State 4 = Paging supervisor abort
State 5 = Open GBT failed
State 6 = Maintenance interrupt, client in progress
State 7 = By request
20-22 = Count of interrupts during client execution
State(s) 0 to 3 are unassigned
State 4 = MAX number of interrupts allowed

State(s) 5 to 7 are unassigned
23 = Unit-type blockage check was OK

CNTL +5

Bit 0-10 = Segment counter
11-13 = Job INIT State

State(s) 0 is unassigned
State 1 = Check UTYN blockage
State 2 = Check member blockage
State 3 = Check member blockage
State 4 = Check PS36 CONFIG
State 5 = Job INIT complete

State(s) 6 and 7 are unassigned
14-22 = GBT number
23 = Client in progress flag

CNTL +6

Bit 0-13 = LKPGSECT relative address
16-23 = LKPGSECT page number

CNTL +6

Bit 0-23 = LKPGSECT absolute address

CNTL +7

Bit 0-7 = LKPGSECT program number
8-15 = RETNSECT program number
16 = Inhibit G, H, and J-level interrupts
17 = Stop AU audits
18 = Inhibit AU communications option
19 = Inhibit interrupts option
20 = Save registers option
21 = Break option
22 = Bypass CPSECT option
23 = Return address saved in controller

CNTL +8

Bit 0-13 = RETNSECT relative address
16-23 = RETNSECT page number

CNTL +8

Bit 0-23 = RETNSECT absolute address

CNTL +9

Bit 0-23 = Save L shadow register

CNTL +10

Bit 0-23 = Save F shadow register

CNTL +11

Bit 0-23 = Save G shadow register

CNTL +12

Bit 0-23 = Save K shadow register

CNTL +13

Bit 0-23 = Save X shadow register

CNTL +14

Bit 0-23 = Save Y shadow register

CNTL +15

Bit 0-23 = Save Z shadow register

CNTL +16

Bit 0-23 = Save J shadow register

CNTL +17

Bit 0-13 = Relative address following last paging subroutine
14-17 = Disk ID for client
18-19 = Outstanding disk requests
20-23 = Page loading state

CNTL +18

Bit 0-9 = Relative address next subroutine in table
10-15 = Number of partial disk blocks left to read
16-23 = Count of remaining subroutines

CNTL+18

Bit 0-23 = Disk address of page directory table for page

CNTL+18

Bit 0-23 = Beginning INTSUB address

CNTL +19

Bit 0-23 = Link to next control table on load list

CNTL +20

Bit 0-23 = Client delay return address (APMH)

CNTL +21

Bit 0-23 = Save MCP-APS clients scratch pointer

CNTL +22, +23, +24 (Not used)

INFO +0

Bit 0-11 = Subclass of active client
12-22 = Class of active client
23 = Output blocks not saved

INFO +1, +2, +3, +4, (Not used)

Maintenance Control Paged Locations

Program	Address	Scratch	Address
PG1PAGECDGN	14441700	MA1MSCSCP	102000
PG1PAGEMTCE	14457700	MA1MSCP	74000
PG4PAGEMTC3	14475700	MA4MSCP3	352400
PG1PAGEADMN	14440700	MA1ADMNSCP	140317
PG1PAGEGUTL	14422700	MA1GSCP	61051
PG1PAGELCLT*	14513700	LI4SCRATCH0	351450
	14515700	LI4SCRATCH1	351510
		LI4SCRATCH2	351550
		LI4SCRATCH3	351610
		LI4SCRATCH4	351650
		LI4SCRATCH5	351710
		LI4SCRATCH6	351750
		LI4SCRATCH7	352010
PG1PAGELIBU	17400000	—	—

*Maximum of 8 libraries (of which two can be paging libraries) can be operating at any time.

MLDGN Layout

DBT+0	DBT+1	DBT+2	DBT+3	DBT+4	DBT+5
DBT+6	DBT+7	DBT+8	DBT+9	DBT+10	DBT+11
DBT+12	DBT+13	DBT+14	DBT+15	DBT+16	DBT+17
DBT+18	DBT+19	DBT+20	DBT+21	DBT+22	DBT+23
DBT+24	DBT+25	DBT+26	DBT+27	DBT+28	DBT+29
DBT+30	DBT+31				

NOTE:
Prefix all words with DG1.

DG1DBT+0—Diagnostic Buffer Table

Bit 0-3 = Request code for diagnostic
State 0 = DGN requested by a program without GBT
State 1 = DGN requested by a program via GBT
State 2 = Manual request detected by alarm scan
State 3 = DGN requested by error analysis
State 4 = DGN requested by DGN: TTY message
State 5 = DGN requested by restore: TTY message
State 6 = DGN requested by an audit
State 7 = DGN requested by demand exercise
State 8 = DGN requested as part of a routine exercise-
midnight, etc.
State 9 = Deferred FR requested by TTY
State 10 = DGN requested by fault recognition
State 11 = DGN requested by bootstrap programs
State 12 = DGN requested after off-line configuration
State 13 = Is unassigned
State 14 = Unconditional restoral
State 15 = Is unassigned
4-6 = Termination code for diagnostic
State 0 = Diagnostic aborted
State 1 = Initial status error detected diagnostic not run
State 2 = Internal software error detected—diagnostic halted
State 3 = Manually terminated DGN
State(s) 4 to 6 are unassigned
State 7 = Normal termination
7-8 = Results of diagnostic
State 0 = Conditional—all tests pass
State 1 = Some tests failed
State 2 = All tests passed
State 3 = No tests run
9 = Subunit specified in bits 7-23 of DG1DBT+14
10-16 = Member number under diagnosis
17-23 = Unit type under diagnosis

DG1DBT+1

Bit 0 = Conversational diagnostic
1 = Raw data requested
2 = Inhibit termination on failure
3 = Growth specified
5 = TLP specified on input
6 = CATLAS keyword specified
20 = New conversational command typed
21 = Partial request—run specified phases
22 = Repeat diagnostic the number of times specified in bits 0-7 of DG1DBT+2
23 = Output channel specified

DG1DBT+2

Bit 0-7 = The number of times a DGN test is to be repeated
8-15 = The TTY channel on which message received
16-23 = The channel—if specified—for outputting

DG1DBT+3

Bit 0-23 = Reserved for return address

DG1DBT+4

Bit 0-9 = Phases 9 through 0 request bits
10-19 = Phases 9 through 0 fail bits
21-23 = MT-MV save

DG1DBT+5

Bit 0-9 = Phases 19 through 10 request bits
10-19 = Phases 19 through 10 fail bits

DG1DBT+6

Bit 0-9 = Phases 29 through 20 request bits
10-19 = Phases 29 through 20 fail bits

DG1DBT+7

Bit 0-9 = Phases 39 through 30 request bits
10-19 = Phases 39 through 30 fail bits

DG1DBT+8

Bit 0-9 = Phases 49 through 40 request bits
10-19 = Phases 49 through 40 fail bits

DG1DBT+9

Bit 0-9 = Phases 59 through 50 request bits
10-19 = Phases 59 through 50 fail bits

DG1DBT+10

Bit 0-9 = Phases 69 through 60 request bits
10-19 = Phases 69 through 60 fail bits

DG1DBT+11

Bit 0-9 = Phases 79 through 70 request bits
10-19 = Phases 79 through 70 fail bits

DG1DBT+12

Bit 0-9 = Phases 89 through 80 request bits
10-19 = Phases 89 through 80 fail bits

DG1DBT+13

Bit 0-9 = Phases 99 through 90 request bits
10-19 = Phases 99 through 90 fail bits

DG1DBT+14

Bit 0-3 = Task number
State 0 = Basic unit diagnostic
State(s) 1 to 15 are unassigned
4-6 = Frame scan point index
7-13 = Submember number requested
14-23 = Subunit type requested

DG1DBT+15

BiT 0 = Power alarm involved in request
1 = If set, request is RMV requested by TTY
2 = Skip diagnostic request and dummy ATP
3 = Flag to show MCFWPEMO was initial entry from MACP
4-7 = Number of failing phases to include in TLP
9 = Subunit specified in bits 7-23 of DG1DBT+16
10-16 = Helper member number
17-23 = Helper unit number

DG1DBT+16

Bit 7-13 = Helper member number
14-23 = Helper subunit

DG1DBT+17

Bit 0 = General Flag 0
1 = General Flag 1
2 = General Flag 2
3 = General Flag 3
4 = General Flag 4
5 = General Flag 5
6 = General Flag 6
7 = General Flag 7
8 = General Flag 8
9 = General Flag 9
10 = General Flag 10
11 = General Flag 11
12 = Set indicates data in DG1DATA0
13 = Set indicates data in DG1DATA1
14 = Set indicates data in DG1DATA2
15 = Set indicates data in DG1DATA3
16 = Set indicates data in DG1DATA4
17 = Set indicates data in DG1DATA5
18 = Set indicates data in DG1DATA6
19 = Set indicates data in DG1DATA7

DG1DBT+17

Bit 0 = PC option for DGNCC input message

Bit 3 = TUC equipped with ADT in place of tape transport

DG1DBT+18

Bit 0-23 = Data word 0

DG1DBT+19

Bit 0-23 = Data word 1

DG1DBT+20

Bit 0-23 = Data word 2

DG1DBT+21

Bit 0-23 = Data word 3

DG1DBT+22

Bit 0-23 = Data word 4

DG1DBT+23

Bit 0-23 = Data word 5

DG1DBT+24

Bit 0-23 = Data word 6

DG1DBT+25

Bit 0-23 = Data word 7

DG1DBT+26

Bit 0-23 = Point of maximum definition per FR analysis

DG1DBT+27

Bit 0-23 = Interrupt number associated with this request

DG1DBT+28

Bit 0-23 = Job ID of the diagnostic request

DG1DBT+29

Bit 0-23 = Error analysis processor

Bit 0-11 = Text phrase to be passed to DCON

DG1DBT+30

Bit 0-23 = Error analysis application
Bit 0-7 = Number of ERAT requested DGN cycles remaining to be run
8 = If 1, text phrase present in word 29
9 = Indicates a DT frame diagnostic
10-11 = Count of abort during ERATPUFH
12 = PUFH client flag for MCFWPEMO
13 = Growth unit restoral request
14 = Transfer to SYRE requested by PUFH
15 = Final handling directed by ERAT
16-22 = A 7-bit error analysis decision code
23 = Final handling completed by sequence TLB

DG1DBT+31

Bit 0-2 = Code for first abort
3-5 = Code for second abort
6 = Diagnostic aborted once
7 = Diagnostic aborted twice

Supplementary Peripheral Diagnostic Data

TEST NUMBER	MISMATCH VALUE	SUPPLEMENTARY DATA WORD1	WORD2	WORD3	WORD4	WORD5
		----------	----------	----------	----------	----------
		----------	----------			

NOTE:
Minimum of 5 words of supplementary data.

WORD 1 = Test Output: Raw data from the frame on the PU reply bus/reads of buffer bus register/scan point reads/data from scratch memory

WORD 2 AND 3 = Test Input: High 12 bits of word 2 = address bus/lower 36 bits (words 2 and 3) = write bus

Address bus:
See "K-Codes (E-Register Layouts)"

Write bus:
High 7 bits = OPCODE
Low 29 bits = Data for the specific order

Other possibilities: Pulse point address/buffer bus register address

WORD 4 = Test location: Address in the phase or subroutine where the test failed

WORD 5 = Test information: Most significant digit gives the number of data words that follow; next digit gives the number of DOLOOP words; next digit gives the number of words of subroutine information data that follow; and the low 5 digits give TLP data.

DOLOOP Data: Maximum 7 words

Values printed are the values of the DOLOOP variables at the time of the test failure. Innermost DOLOOP is printed first—variable C.B.A.

Subroutine Data: Maximum 7 words

Value(s) printed are the address(es) at the call substatement(s). The address of the last executed call SUB is printed first—call SUB C.B.A.

Peripheral Unit (PU) Interrupt Printouts

Common Level Data (MI1CONT)

See Common Printouts.

F-Level

See Interrupt Level Printouts.

Central Control (CC) Interrupt Data

See Central Control/Auxiliary Unit Printouts.

MAC Control Memory Layout

See Maintenance Control Printouts.

Peripheral System Data

WORD 0	WORD 1	WORD 2	WORD 3	WORD 4	WORD 5
WORD 6	WORD 7	WORD 8	WORD 9	WORD 10	WORD 11
WORD 12					

WORD 0—State of PU bus routing Flip Flop's at Time of Interrupt

Bit 9-12 = Active CC coded enable bus select
13-15 = Active CC CPD enable address bus
16-17 = Active CC CPD enable—PU address bus
18-20 = Active CC CPD enable—PU reply bus

WORD 1—PU Bus 0 Software Status

Bit 0 = Image of PUBO flip-flop
1 = Image of PUBA flip-flop
2 = Image of PUBT flip-flop
3 = Image of PUBR flip-flop
4 = Trouble on addressing portion of bus
5 = Trouble on reply portion of bus
6 = Trouble at CC on this bus
7 = Diagnostic has been requested
8 = Peripheral bus removed via TTY
12 = Bus is out of service
16-19 = Number of units unable to receive on this bus at time of interrupt
20-23 = PU maintenance code

WORD 2—PU Bus 1 Software Status (Same as above for bus 0)

WORD 3—PU Bus/Unit Bus Failing Data During Recovery

WORD 4—PU Bus/Unit Bus Failing Test During Recovery

WORD 5—Base SP 0, Controller 0 Software Status After Recovery

WORD 6—Base SP 0, Controller 1 Software Status After Recovery

WORD 7—Base SP 1, Controller 0 Software Status After Recovery

WORD 8—Base SP 1, Controller 1 Software Status After Recovery

WORD 9—Network Clock, Chain 0 Software Status After Recovery

WORD 10—Network Clock, chain 1 Software Status After Recovery

WORD 11—Network Clock, Chain 2 Software Status After Recovery

WORD 12—Network Clock, Chain 3 Software Status After Recovery

Interrupt Source Data

WORD 0 WORD 1 WORD 2 WORD 3 WORD 4

WORD 0—State of P-Register (Bits 24-35) at Time of Interrupt (P-Upper)

Bit 0-4 = Auxiliary OPCODE
5-11 = OPCODE
(Bit 11 = 1 indicates a maintenance OPCODE)

WORD 1—State of P-Register (Bits 0-23) at Time of Interrupt (P-Lower)

Bit 0-23 = P-Register data bits 0-23

WORD 2—State of E-Register Containing K-Code of the Last Addressed Unit at Time of Interrupt

Bit 10-16 = Member number [See K-Codes (E-Register Layouts)]
17-21 = Unit-ID number [See K-Codes (E-Register Layouts)]

WORD 3—Group Interrogate Response (GI)

Bit 0-23 = Group interrogate states (See MI/GI responses)

WORD 4—Member Interrogate Response (MI)

Bit 0-23 = Member interrogate states (See MI/GI Responses)

Fault Recognition Isolation Data

WORD 0 WORD 1 WORD 2 WORD 3 WORD 4 WORD 5

WORD 0—Sequence Table or Primary Strategy Table

Bit 0-23 = Table number

WORD 1—Interrupt Sequence State or Primary Strategy Table

Bit 0-23 = State

WORD 2—Point of Maximum Definition

Bit 0-7 = PMD

WORD 3—Resolution Class

Bit 0-1 = Resolution class
State 0 = Resolved
State 1 = Unresolved
State 2 = Changed UTMN
State 3 = Internal error

WORD 4—Fault Class

Bit 0-3 = Fault class (Octal)

State 0 = No action
State 1 = Software
State 2 = Class 1—Transient
State 3 = Class 1—Hard
State 4 = Class 2—Transient
State 5 = Class 2—Hard
State 6 = Class 3—Transient
State 7 = Class 3—Hard
State 10 = Class 4—Transient
State 11 = Class 4—Hard
State 12 = Unequipped
State 13 = Growth
State 14 = TRPF—Transient
State 15 = TRPF—Unresolved

WORD 5—Number of Isolate Attempts in Which Fault Recovery Changed Suspect Unit

Bit 0 = 0 or 1 isolate attempts

Peripheral Fault Recognition Results

PU4RESULT	PU4UTMNO	PU4FRPMD	PU4FRJRG	PBFR0000	TRINDEX
FAILTEST1	FAILDATA1	RELADDR1	FAILTEST2	FAILDATA2	RELADDR2
FAILTEST3	FAILDATA3	RELADDR3	FAILTEST4	FAILDATA4	RELADDR4
FAILTEST5	FAILDATA5	RELADDR5	FAILTEST6	FAILDATA6	RELADDR6
,,	,,	,,	,,	,,	,,
,,	,,	,,	,,	,,	,,
,,	,,	,,	,,	,,	,,

PU4RESULT—Fault Recognition Summary Register

Bit 0 = CC0 found faulty
1 = CC1 found faulty
2 = Controller 0 found faulty (or NCLK chain in half 0)
3 = Controller 1 found faulty (or NCLK chain in half 1)
4 = PU bus 0 found faulty
5 = PU bus 1 found faulty
6 = PU bus 0 at unit found faulty
7 = PU bus 1 at unit found faulty
8 = Faulty unit or subunit to be removed and diagnosed
9 = Faulty unit or subunit to be removed
10 = Fault recognition was unable to find the fault
11 = Fault recognition found that a software error caused the F-level
12 = Fault recognition found that a transient caused the F-level
13 = Signal processor matrix found faulty
14 = Controller 0 pulse point is suspect
15 = Controller 1 pulse point is suspect

Continue on next page.

PU4RESULT—Fault Recognition Summary Register (Contd)

Bits 16-18 = Hardware Register Read Fail Errors

0 = Normal read
1 = 2nd read pass with both sends set and fail flags (FAILSR0 or FAILSR1 set)
2 = 2nd read pass with both sends set and fail flags (FAILSR0 or FAILSR1 not set)
3 = HDRWRDST (UNCLAMP) fails
4 = 3rd read pass (IPUB, PUB bad)
5 = 3rd read fail (controller bad)

PU4UTMNO—Unit and Member ID Register

Bit 2-8 = Submember found faulty (if any)
9 = Set if submember found faulty
10-16 = Member number found faulty (or NCLK bay number)
17-23 = Unit type found faulty

PU4FRPMD—Terminal FR Program Register

Bit 0-7 = Point of maximum definition—terminal FR subroutine INDENT.
8-14 = Fault recognition decision code
15-21 = Error analysis action code

PU4FRJRG—Save J Register

Bit 0-23 = FR program address where error was located

PBFR0000—Address of PBFR

TRINDEX—Number of Words Appearing in this Result Printout

FAILTESTn—Failing Test Information

Bit 0-8 = Failing test number
9-11 = 1 failing controller access test
= 2 failing bus loop test

For Bus Loop Test Only:

Bit 12 = Bus branch circuit half
13-14 = Bus circuit
15 = Bus number
16 = 0 PUBB 0
= 1 repeater

For Access Test Only:

Bit 17 = 1 Controller 1
= 0 Controller 0
20 = Controller 0 was access tested
21 = Controller 0 failed access test
22 = Controller 1 was access tested
23 = Controller 1 failed access test

FAILDATAn—Failing Test Data—Nonzero Bits Represent Failing Bits—Look in PBFR for more Detail on Failing Tests and Bits

RELADDRn—Relative Address in PBFR Where the Bus Loop Test or Controller Access Test was Called

Error Analysis Recent History Tables (ERAT)

RCNT+0	RCNT+1	RCNT+2	RCNT+3	RCNT+4	RCNT+5
RCNT+6	RCNT+7	RCNT+8	RCNT+9	RCNT+10	RCNT+11
RCNT+12	RCNT+13	RCNT+14	RCNT+15	RCNT+16	RCNT+17
RCNT+18	RCNT+19	RCNT+20	RCNT+21	RCNT+22	RCNT+23
RCNT+24	RCNT+25	RCNT+26	RCNT+27	RCNT+28	RCNT+29
RCNT+30	RCNT+31	RCNT+32	RCNT+33	RCNT+34	RCNT+35
RCNT+36	RCNT+37	RCNT+38	RCNT+39	RCNT+40	RCNT+41
RCNT+42	RCNT+43	RCNT+44	RCNT+45	RCNT+46	RCNT+47
RCNT+48	RCNT+49	RCNT+50	RCNT+51	RCNT+52	RCNT+53
RCNT+54	RCNT+55	RCNT+56	RCNT+57	RCNT+58	RCNT+59
RCNT+60	RCNT+61	RCNT+62	RCNT+63		

NOTE:
Prefix each word with ER4.

RCNT +0

Bit 0 = Half of suspect unit
1-7 = Member number of suspect unit
8-14 = Unit type of suspect unit
15 = 1 if a nonautonomous interrupt
16-22 = Fault recognition decision code
23 = 1 if duplex failure (DDUP)

RCNT +0

Bit 1-14 = Unit type and member number of suspect
16-19 = SA: Type of error analysis entry (FR decision code)
State 0 = Decision code of no action
State 1 = Remove and request diagnostic
State 2 = Remove
State 3 = Return to service
State 4 = Remove this half and update mate
State 5 = Diagnose this half and update mate
State 6 = Software error
State 7 = Transient error
State 8 = EA resolvable
State 9 = FR troubled controller guess
State 10 = Duplex failure state
State 11 = Divorce and run
State 12 = Switch activity
State 13 = Remove and PEST this growth unit
State 14 = Restore and request diagnostic
State 15 = Hit time the frame
20-21 = SA:Fault recognition application bits
(See RCNT +23 for DAPP assigns)
22 = Controller PEST

RCNT +1

Bit 0-11 = Bits 21-10 of E-Register
12-23 = Bits 35-24 of P-Register

RCNT +2

Bit 0-23 = Bits 0-23 of P-Register

RCNT +3

Bit 7 = AC1LUDWC
8 = AC1MTCPU
12-16 = AC1CEQF
22 = 1 IF ERATBASE entered
23 = Both controller O/S—copy of DUP bit input

RCNT +4

Bit 0 = AC1ASWOPU
1 = AC1ASW1PU
2 = AC1POPU
3 = AC1P1PU
6 = AC1ASWEPU
7 = AC1APEPU
8 = 1 if interject request, 0 if F-level
11 = 1 if BBFR is entering ERAT
12 = 1 if PBFR should go to CCPREXFR
13 = CC number causing F-level problem
14 = 1 if F-level due to active CC problem-DCC must be 1
15 = 1 if F-level due to a CC problem
16 = ERAT specified bus number
17 = ERAT minor bus flag—1 for minor—0 for major
18 = 1 if ERAT indicates duplex bus failure
19 = Bus number
20 = Minor bus flag—1 for minor—0 for major
21 = 1 if duplex bus failure
22 = 1 if PBFR implicates a bus rather than the specified unit member and half
23 = 1 if PBFR is entering ERAT

RCNT +4

Bit 14-15 = F-Level due to CC—Items DCC and DCCACT
16-18 = ERAT specified bus data—ABNO AMNBUS and ADUPB
19-21 = Inputted bus data—DBNO DMNBUS and DDUPB

RCNT +5

Bit 4 = Inhibit AUTNM PU failure summary copy
5 = Inhibit PU failure summary copy
22 = AC1IASWEPU
23 = AC1IAPEPU

RCNT +6

Bit 0-1 = SA: Equipage Status of Interrupting Unit
State 0 = Unequipped
State 1 = Growth
State 2 = Special growth
State 3 = Operational
6 = AC1ACT
7 = AC1TCC
8 = AC1DIV
9 = AC1PUBO
10 = AC1PUBA
11 = AC1PUBT
12 = AC1PUBR

RCNT +7

Bit 0-23 = GI Responses

RCNT +8

Bit 0-23 = MI Responses

RCNT +9

Bit 0-23 = L-Register

RCNT +10

Bit 0-23 = Active bus status

RCNT +11

Bit 0-23 = Standby bus status

RCNT +12

Bit 0-4 = Diagnostic sequence state (DSS)
5-9 = Next interrupt sequence state (ISS)
10-14 = Sequence table number (ST)
15-18 = RCNT Link list forward pointer
19 = RCNT almost full flag
20-23 = RCNT Link list backward pointer

RCNT +12

Bit 0-9 = Index to sequence tables

RCNT +13

Bit 0-23 = Analysis table correlated data

RCNT +13

Bit 0-17 = Error analysis temporary storage
18-23 = Analysis table entry qualifier code

RCNT +14

Bit 0-21 = Error analysis timing list register
22 = Timing list audit flag if 1 audit required
23 = EA Timing sign:

0 = Idle (if time = 0) or timing active
1 = Waiting for diagnostics (implies time = 0)

RCNT +15

Bit 0-23 = Primary error source register—suspect

RCNT +16

Bit 0-23 = Primary error source register—mate

RCNT +17

Bit 0-23 = Secondary error source register—suspect

RCNT +18

Bit 0-23 = Secondary error source register—mate

RCNT +19

Bit 0-23 = Status register—suspect

RCNT +20

Bit 0-23 = Status register—mate

RCNT +21

Bit 0-23 = Software status—suspect

RCNT +22

Bit 0-23 = Software status—mate

RCNT +23

Bit 0 = Half of suspect unit
1-7 = Member number of suspect unit
8-14 = Unit type of suspect unit
15 = 1 if a nonautonomous interrupt
16-22 = Action code
23 = Re-entry flag

RCNT +23

Bit 1-14 = Unit type and member number from action word
16-19 = SA: Error analysis action code
State 0 = Action code of no action
State 1 = Remove and request diagnostic
State 2 = Remove
State 3 = Return to service
State 4 = Remove this half and update mate
State 5 = Diagnose this half and update mate
State 6 = Software error
State 7 = Transient error
State 8 = EA Resolvable
State 9 = Troubled controller guess
State 10 = Duplex failure state
State 11 = Divorce and run
State 12 = Switch activity
State 13 = Remove and PEST this growth unit
State 14 = Restore and request diagnostic
State 15 = Hit time the frame

Bit 20-21 = SA: ER4DAPP: Fault Recognition Application State

DT

State 0 = Unassigned
State 1 = Suspect is a DTU as supplied in RCNT +32
State 2 = Unassigned
State 3 = Unassigned

EST

State 0 = Unassigned
State 1 = Suspect is the ESU as supplied in RCNT +32
State 2 = Unassigned
State 3 = Unassigned

NCLK

State 0 = Unassigned
State 1 = Suspect is chain as supplied in RCNT +32
State 2 = Unassigned
State 3 = Unassigned

SCLK

State 0 = Unassigned
State 1 = PEST SYS clock A-B counters
State 2 = NCSU
State 3 = Unassigned

SP

State 0 = Unassigned
State 1 = Suspect is matrix of specified SP—also means PEST matrix
State 2 = Suspect is DT associated with SP2-DT number supplied in RCNT +32
State 3 = Unassigned

RCNT +24

Bit 0 = Long-term fault flag
1 = DANT roll back request
2 = Roll back history flag 1 if RB has occurred
3 = Waiting for manual diagnostic request
4 = Failure override bit
5-9 = Roll back INTRPT sequence ST
10-14 = Roll back sequence table number
15-18 = RCNT MADRET link
19-22 = MAURET link pointer
23 = 1 if sequence tables are entered on F-Level

RCNT +25

Bit 0-17 = Desired audit number
18 = Interface program flag
19 = Interface program flag
20 = Interface program flag
21 = Interface program flag
22 = Interface program flag
23 = Interframe program flag

RCNT +26

Bit 0-22 = ER4 dump 1

RCNT +27

Bit 0-22 = ER4 dump 2

RCNT +28

Bit 0-22 = ER4 dump 3 RCNT +29

RCNT +29

Bit 0-8 = FR unique PMD number
22-23 = SA: Indicates Type of Return from FR
State 0 = Unassigned
State 1 = FR should unwind
State 2 = FR should roll ahead
State 3 = FR should return to reference point

RCNT +30

Bit 0-22 = First associated maintenance file number

RCNT +31

Bit 0-22 = Last associated maintenance file number

RCNT +32

Bit 0-22 = Submember word for VIUs and terms

RCNT +33

Bit 0-23 = Audit and diagnostic results word

RCNT +33

Bit 0-3 = SA: DGN source from DBT
State 0 = DGN REQ by program without A GBT
State 1 = DGN REQ by program via a GBT
State 2 = Manual REQ detected by alarm scan
State 3 = DGN REQ by error analysis
State 4 = DGN REQ by DGN: TTY message
State 5 = DGN REQ by restore: TTY message
State 6 = DGN REQ by an audit
State 7 = DGN REQ by demand exercise
State 8 = DGN REQ as part of routine exercise—midnight, etc.
State 9 = Deferred FR requested by TTY
State 10 = DGN REQ by fault recognition
State 11 = DGN REQ by bootstrap programs
State 12 = DGN REQ after off-line CONFIG
State 13 = Unassigned
State 14 = Unconditional restoral
State 15 = Unassigned

4-6 = SA: Termination Code from DBT
State 0 = Diagnostic aborted
State 1 = Internal status error detected—DGN not run
State 2 = Internal software error detected—DGN halted
State 3 = Manually terminated DGN

State(s) 4 to 6 are unassigned
State 7 = Normal termination

RCNT +33 (Contd)

7-8 = SA: DGN Test Results from DBT
State 0 = Conditional all tests pass
State 1 = Some tests failed
State 2 = All tests passed
State 3 = No tests run

9 = 1 if diagnostic has completed

17 = Audit error indicator

18-20 = SA: Reasons for Audit Canceled

State 0 = Unassigned
State 1 = Invalid MDN
State 2 = MAX REQ waits exceeded
State 3 = MAX COMP waits exceeded
State 4 = No available MAURET

State(s) 5 to 7 are unassigned

21 = 1 if the requested audit was canceled

22 = 1 if an audit has completed

23 = 1 if an audit has been requested

RCNT +33

Bit 0-8 = Overall DGN results from the DBT
21-23 = Overall audit results

RCNT +34

Bit 0-11 = First supplementary audit number
12-23 = Second supplementary audit number

RCNT +34

Bit 0-23 = First supplementary audit word

RCNT +35

Bit 0-11 = Third supplementary audit number
12-23 = Fourth supplementary audit number

RCNT +35

Bit 0-23 = Second supplementary audit word

RCNT +36

Bit 0-11 = Fifth supplementary audit number
12-23 = Sixth supplementary audit number

RCNT +36

Bit 0-23 = Third supplementary audit word

RCNT +42

Bit 0-4 = SA: Type of Unit Interrupting
State 0 = Unassigned
State 1 = Controller
State 2 = Network clock
State 3 = Terminal
State 4 = VIU
State 5 = DTU
State 6 = DT associated with SP
State 7 = CC problem
State 8 = Major bus
State 9 = Minor bus
State 10 = ESU
State 11 = Babbling bus

State(s) 12 to 31 are unassigned
6 = 1 if this is a duplex failure
9-12 = Count of number of times SECT updated
15-23 = Count of number of interrupt in this RCNT

RCNT +42

Bit 0-23 = First summary word

RCNT +43

Bit 0-4 = Copy of BRCEC
6-10 = Copy of ARCEC
12 = 1 if SSTT search performed
13 = 1 if SSTT match was found
15 = 1 if fmon RCNT analysis performed
16 = 1 if RCNT analysis was significant
17 = 1 if analysis gave unit and unit was in-service

RCNT +43

Bit 0-18 = 1 if analysis gave new SEQT ISS and DSS
20 = Flag indicating last RCNT was input RCNT
23 = Second summary word

RCNT +44

Bit 0-4 = Copy of ER4NEPT
6-9 = Copy of ER4INPT
12-15 = Previous value of RCNT +33 0-3
16-18 = Previous value of RCNT +33 bits 4-6
19-20 = Previous value of RCNT +33 bits 7-8

RCNT +44

Bit 12-20 = Previous value or RCNT +33 bits 0-8

RCNT +44

Bit 0-23 = Third summary word

RCNT +45

Bit 0-12 = Port PEST number—corresponds 1 to 1 with port number

RCNT +45

Bit 0-6 = DT member number
7-13 = DT unit type number
14 = 1 if this is the last DT that is not duplex failed
15-18 = SA: ER4ATYPE: DT action by ERAT
19 = DT controller acted on by EA
21 = Suspect DT controller—from FR PROG
22 = 1 if mate SPC recorded error
23 = 1 if mate DTC is OOS

RCNT +46

Bit 0-23 = Submember flags for controller 0

RCNT +47

Bit 0-23 = Submember flags for controller 1

RCNT +48

Bit 0-23 = Indicates subunits causing multiple interrupts

RCNT +49

Bit 0 = 1 if multiple interrupt due to current sub-member
15 = Indicator to test for special TSI and TMS duplex fail requests
18-22 = Count of number of audit tries from duplex fail sequence table
23 = Indicates possible hardware implication when DEC code = software

RCNT +50

Bit 0-23 = Value of EX4CLOCK at time of interrupt (10 ms/bit)

RCNT +51

Bit 0-22 = DELTA time since last interrupt—in 10-ms increments
23 = DELTA time overflow indicator

RCNT +52

Bit 0-22 = Leaky bucket counter
23 = EA duplex failed unit and/or requested phase 2

RCNT +53

Bit 0 = State of SP2 CO RCV from 0 FF
1 = State of SP2 CO RCV from 1 FF
3 = State of SP2 CO send to 0 FF
4 = State of SP2 CO sent to 1 FF
6 = DT CO out-of-service bit 1 = OOS
7 = DT C1 out-of-service bit 1 = OOS
9 = SP2 CO out-of-service bit 1 = OOS
12 = State of SP2 C1 RCV from 0 FF
13 = State of SP2 C1 RCV from 1 FF
15 = State of SP2 C1 send to 0 FF
16 = State of SP2 C1 send to 1 FF
17 = 1 if mate DTC clock is available
18 = DT CO out-of-service bit 1 = COS
19 = DT C1 out-of-service bit 1 = COS
20 = 1 if suspect DT can run alone
21 = SP2 C1 out-of-service bit 1 = OOS
22 = 1 if mate DT is restorable
23 = 1 if mate DT can run alone

RCNT +53

Bit 0-1 = SP2 controller 0 RCV RTG
3-4 = SP2 controller 0 send RTG
6-7 = DT CO and C1 OS status
12-13 = SP2 controller 1 RCV RTG
15-16 = SP2 controller 1 send RTG
18-19 = Same as bits 6-7

RCNT +53

Bit 0-23 = Suspect DT/SP2 routing and status-same as SP4PORTSTAT

RCNT +54

Bit 0-3 = NCLK master OSC select bits on first phase error interrupt

6-7 = NCLK, count number of phase error interrupts (PMDs 15 and 22). Third interrupt removes previously recorded master OSC (Bits 0-3).

RCNT +54

Bit 0-23 = Most recent term data (ESR)

RCNT +54

Bit 0-3 = Term
4-23 = Most recent term ESR

RCNT +54

Bit 0-5 = Bits 1-6 of R12 of VIU
6-11 = Bits 1-6 of R13 of VIU
12-17 = Bits 1-6 of R14 of VIU
18-23 = Bits 1-6 of R15 of VIU

RCNT +54

Bit 0-23 = VIU 0 error source register

RCNT +54

Bit 0-23 = DT/SP2 low port routing—suspect soft status

RCNT +55

Bit 0-23 = Most recent term data (MR)

RCNT +55

Bit 0-3 = Bit 0 set. If first term word block busy and so on
4-23 = Most recent term MR

RCNT +55

Bit 0-23 = VIU 1 error source register—same as RCNT +54

RCNT +55

Bit 0-23 = DT/SP2 high port routing—suspect soft status

RCNT +56

Bit 0-23 = Previous term data (ESR)

RCNT +56

Bit 0-3 = Term
4-23 = Previous term ESR

RCNT +56

Bit 0-23 = VIU 2 error source register—same as RCNT +54

RCNT +56

Bit 0-23 = DT/SP2 low port routing—mate soft status

RCNT +57

Bit 0-23 = Previous term data (MR)

RCNT +57

Bit 4-23 = Previous term MR

RCNT +57

Bit 0-23 = VIU 3 error source register—same as RCNT +54

RCNT +57

Bit 0-23 = DT/SP2 high port routing—mate soft status

RCNT +58

Bit 0-23 = Previous term data (ESR)

RCNT +58

Bit 0-3 = Term
4-23 = Previous term ESR

RCNT +58

Bit 0-23 = VIU 4 error source register—same as RCNT +54

RCNT +59

Bit 0-23 = Previous term data (MR)

RCNT +59

Bit 4-23 = Previous term MR

RCNT +59

Bit 0-23 = VIU 5 error source register—same as RCNT +54

RCNT +60

Bit 0-23 = Previous term data (ESR)

RCNT +60

Bit 0-3 = Term
4-23 = Previous term ESR

RCNT +60

Bit 0-23 = VIU 6 error source register—same as RCNT +54

RCNT +61

Bit 0-23 = Previous term data (MR) RCNT +61

RCNT +61

Bit 4-23 = Previous term MR

RCNT +61

Bit 0-23 = RCNT error source register—same as RCNT + 54

RCNT +61

Bit 12-15 = Failing level

RCNT +62

Bit 0-23 = VCFR F-Level access test results

RCNT +62

Bit 0-23 = VCFR INT VIC I/S VIC register 10-11

RCNT +63

Bit 0-23 = First word of Unit-Type Translator

Error Analysis Strategy Data (DIF/SCS/XTSI, FLEV, Interject BLM Reports) (NCSU BLM Reports)(FERA)

WORD 0	WORD 1	WORD 2	WORD 3	WORD 4	WORD 5
WORD 6	WORD 7	WORD 8	WORD 9	WORD 10	WORD 11
WORD 12	WORD 13	WORD 14	WORD 15	WORD 16	WORD 17
WORD 18	WORD 19	WORD 20	WORD 21	WORD 22	WORD 23
WORD 24	WORD 25	WORD 26	WORD 27	WORD 28	WORD 29
WORD 30	WORD 31				

WORD 0

Bit 0-6 = Member number
7-13 = Unit type
15-16 = Strategy
21-23 = Data file state

WORD 1

Bit 0-6 = Subunit member number
7-16 = Subunit type
21-22 = No history file code
0 = No history
2 = Found history
23 = Subunit previously implicated

WORD 2

Bit 0-3 = Interrupt level
6-13 = Number of interrupts
15-21 = Leaky bucket count

WORD 3

Bit 0-23 = Interrupt time

WORD 4

Bit 0-6 = Interrupting member number
7-13 = Interrupting unit type
15-16 = Next timed strategy
18-19 = Next timed strategy state

WORD 5

Bit 0-4 = Next primary strategy state
6-10 = Next primary strategy
12-16 = Present primary strategy state
18-22 = Present primary strategy

WORD 6

Bit 0-2 = Next secondary strategy state
3-5 = Next secondary strategy
6-8 = Present secondary strategy state
9-11 = Present secondary strategy
12-14 = Timed strategy state
15-17 = Timed strategy
18-20 = Demand analysis state
21-23 = Demand analysis

WORD 7

Bit 0-2 = Next analysis state
3-5 = Next analysis
6-8 = Present analysis state
9-11 = Present analysis
12-14 = Originator class
18 = Demand analysis trigger
21 = Demand analysis active

WORD 8

Bit 0-7 = PMD number
9-12 = Fault class
15-16 = Resolution class
18-19 = Retry status
21 = Diagnostic strategy active

WORD 9

Bit 0-6 = Member number under diagnostic analysis
7-13 = Unit type under diagnostic analysis
15 = Diagnostic strategy override
18 = Diagnostic progress
21-22 = Timed analysis active flag

WORD 10

Bit 0-16 = Subunit type and member number under diagnostic analysis

WORD 11

Bit 0-1 = Next diagnostic strategy state
2-3 = Next diagnostic strategy
4-5 = Present diagnostic strategy state
6-7 = Present diagnostic strategy
8-9 = ATP restore interrupt count
10-13 = Diagnostic request
14-16 = Diagnostic count
17-20 = Diagnostic termination code
21-22 = Diagnostic result
23 = Audit request

WORD 12

Bit 0-23 = Timed reentry time

WORDS 13-22

Bit 0-23 = Suspect array (secondary UTMNs and SUTMNs)

WORDS 23-26

Bit 0-23 = Strategy data

WORD 27

Bit 0-23 = Maintenance file number

WORD 28

Bit 0-23 = Delta time

WORDS 29-30

Bit 0-23 = Subunit summary

WORD 31

Bit 0-23 = Data file time-out time

Error Analysis Strategy Data (ERAT) (TNFR FLEV Reports)

WORD 0 WORD 1 WORD 2 WORD 3 WORD 4 WORD 5 WORD 6

WORD 0—Time of Interrupt

Bit 0-23 = Value of EX4 clock at time of interrupt (10 ms/bit)

WORD 1—Number of Interrupts

Bit 0-8 = Number of interrupts on the suspect unit since error history is kept for unit

WORD 2—Leaky Bucket Count

Bit 0-22 = Leaky bucket count on which zap, zero-start, duplex-failure actions are based

WORD 3—Sequence Table

Bit 0-4 = Error analysis choice of sequence table number

WORD 4—Interrupt Sequence State

Bit 0-4 = Error analysis choice of next interrupt state number

WORD 5—Diagnostic Sequence State

Bit 0-4 = Error analysis choice of diagnostic sequence state number

WORD 6—How to Return Choice

Bit 0-1 = Error analysis choice of unwinding mechanism
State 0 = Unassigned
State 1 = FR should unwind
State 2 = FR should roll ahead
State 3 = FR should return to reference point

Peripheral Unit Frame Printouts

GI/MI- Group Interrogate/Member Interrogate Responses

GI Response:

Reply Bit	
0	SP/DIF Members 0-23
1	SP/DIF Members 24-31
2	NC Chains 0-3
3	TMS Members 0-3
4	TSI Members 0-15
5	TSI Members 16-31
6	TSI Members 32-47
7	TSI Members 48-63
8	VIF Members 0-15
9	VIF Members 16-31
10	VIF Members 32-47
11	VIF Members 48-63
12	VIF Members 64-79
13	VIF Members 80-95
14	VIF Members 96-111
15	VIF Members 112-127
16	EST 0-15
17	EST 16-31
18	Unused
19	SCS Members 0-7
20	Unassigned

MI Response:

Bit position is respective to member number in that group.

To execute the MI/GI library program:

EX: LIBSYS:PKG LG*gg* FLDS, PGM LIB1, TASK 0!

Where *gg* = Generic number

K-Codes (E-Register Layouts)

(Bits 0-11 on PUEA bus — See Section 5, *Peripheral Enable Address (PUEA) Bus Format* in Volume 1)

PUEA Bus	UNIT Type ID*											
Bits	11	10	9	8	7	6	5	4	3	2	1	0
SP/DIF	0	0	0	1	0	Member Number					MTX	
SCLK	0	0	0	1	1	Member Number						
TMS	0	0	1	0	0						MEM NO.	
TSI	0	0	1	0	1	Member Number						SPC
TGR	0	0	1	1	0	Member Number						
IOUS	0	0	1	1	1	MEM NUM			IOUC			
EST	0	1	0	0	1	Member Number						
SCS	0	1	0	1	1	MEM NUM			SCU NUM			

* The unit type ID identified by the upper 5 bits (bits 7-11) of the PUEA bus does not necessarily have the same octal/value as the unit type codes (COMPOOL 4XLU____).
See *Unit Type Codes* in this section.

Peripheral Unit- Maincodes

Bit 20-23 Software Status (Octal)

0 = Controller is normal
1 = Controller in diagnostic
2 = Controller in exercise
3 = Controller in fault recovery/error analysis
4 = Controller in listen—only mode
(for NCLK, OSC update in—progress)
5 = Controller is unequipped
6 = Controller seized for diagnostic
7 = Controller out of service for growth
10 = Controller out of service—normal
11 = Connecting TSI is duplex failed
12 = Controller being updated
13 = PUB in process of being restored
14 = Controller left out of service following phase
15 = Controller out of service and connecting TSI is duplex failed
16 = Controller failed restore attempt
17 = For TMS, controller removed due to A-link problem for VIF, EST, controller out of service due to TSI outage

Digroup Trunk- Maincodes

See *Digroup Trunk Printouts*.

Subunit- Maincodes

Bit 20-23 Software Status (Octal)

0 = Normal
1 = Subunit out of service—normal
2 = Subunit controller is duplex failed
3 = Subunit out of service and subunit controller is duplex failed
4 = Subunit connecting TSI is duplex failed
5 = Unequipped
6 = Subunit out of service and connecting TSI is duplex failed
7 = Subunit out of service for growth
10 = Subunit controller and subunit connecting TSI are duplex failed
11 = Subunit controller, subunit, and subunit connecting TSI are all duplex failed
12 = Don’t allow protection switch for this subunit (WOPS)
13 = Subunit in diagnostic
14 = Subunit left out of service following phase

Unit-Type Codes

Octal/Decimal Values	Compool Symbol	Unit
000/0	———	Unassigned
001/1	4XLUOA	Office Dependent Alarms
002/2	4XLUSP	Signal Processor
003/3	4XLUNETCLK	Network Clock
004/4	4XLUTMS	Time-Multiplexed Switch
005/5	4XLUTSIF	Time-Slot Interface Frame
006/6	4XLUTAC	Terminal Access Circuit (CCIS)
007/7	4XLUEST	Echo Suppressor Terminal
010/8	4XLUDIF	Digital Interface Frame
011/9	4XLUPUBB	Peripheral Unit Bus Branching
012/10	———	Unassigned
013/11	4XLUVIF	Voiceband Interface Frame
014/12	4XLUDT	Digroup Terminal Frame
015/13	4XLUSYSCLK	System Clock
016/14	4XLUABC	Area Bus Center
017/15	4XLUBDFB	Battery Distribution Fuseboard
020/16	4XLU620	620 Power Plant
021/17	4XLU625	625 Power Plant
022/18	4XLUMFA	Miscellaneous Frame A
023/19	4XLUTTF0	Toll Terminal Frame 0
024/20	4XLUTTF1	Toll Terminal Frame 1
025/21	4XLUTTF2	Toll Terminal Frame 2
026/22	4XLUTTF3	Toll Terminal Frame 3
027/23	4XLUTTF4	Toll Terminal Frame 4
030/24	4XLUTTF5	Toll Terminal Frame 5
031/25	4XLUTTF6	Toll Terminal Frame 6

Octal/Decimal Values	Compool Symbol	Unit
032/26	4XLUTTF7	Toll Terminal Frame 7
033/27	4XLUMFB	Miscellaneous Frame B
034/28	4XLUNMFR	NETMGT Display Control Frame
035/29	4XLU630	630 Power Plant
036/30	4XLUCCT	Continuity Check Transceiver
037/31	4XLUCCDS	CCIS Data Set Frame (2048A Dataset)
040/32	4XLUTPOS	Test Position
041/33	4XLURECANNM	Recorded Announcement Machine
042/34	4XLURMDC	NETMGT Remote/DIST Circuit
043/35	4XLUGRID	Office Alarm Grid Circuit
044/36	4XLURTPLANT	Ringing and Tone Plant
045/37	4XLUTCONTL	NETMGT DOC Transceiver Unit (Transmitter)
046/38	4XLURCONTL	NETMGT DOC Transceiver Unit (Receiver)
047/39	4XLUMFSF	MF Signaling Frame
050/40	4XLUSCS	Service Circuit System
051/41	———	Unassigned
052/42	4XLUADG	Automatic Distribution Group
055/45	4XLUMFC	Miscellaneous Frame C
056/46	4XLUMFCT	Multifrequency Compelled Frame

Octal/Decimal Values	Compool Symbol	Unit
057/47	4XLUMFCX	Multifrequency Compelled Unit
060/48	4XLUAPS	Pseudo I/O Unit-Type
153/107	1XLUSSD	Scan & Signal Distributor (SSD)
154/108	1XLUMUP	MCC & Utility Processor (MUP)
155/109	1XLUAUI	Auxiliary Unit Interface (AUI)
156/110	1XLUIFB	Interface Bus (IFB)
157/111	1XLUPDF	Power Distribution Frame (PDF)
160/112	1XLUPUB	Peripheral Unit Bus (PUB)
161/113	1XLUDUB	Data Unit Bus (DUB)
162/114	1XLUAUB	Auxiliary Unit Bus (AUB)
163/115	1XLUCSB	Call Store Bus (CSB)
164/116	1XLUPSB	Program Store Bus (PSB)
165/117	1XLUIOUS	I/O Unit Selector (IOUS)
166/118	1XLUXPWR	Miscellaneous Power (XPWR)
167/119	1XLUTUC	Tape Unit Controller (TUC)
170/120	1XLUDUS	Data Unit Selector (DUS)
171/121	1XLUFN	Fans
173/123	1XLUCS	Call Store (CS)
174/124	1XLUPS	Program Store (PS)
175/125	1XLUCC	Central Control (CC)
176/126	1XLUAPI	Attached Processor Interface (API)

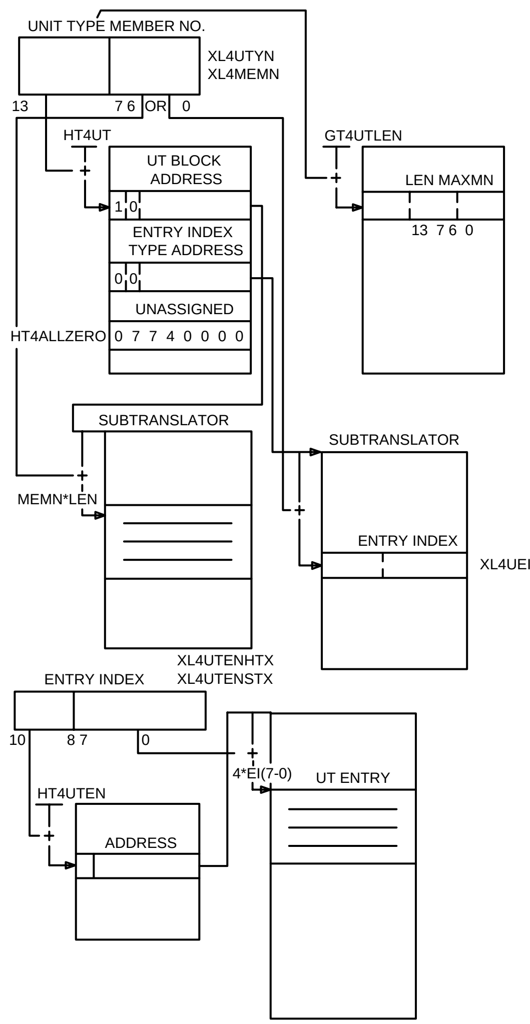
Subunit-Type Codes/Keywords

Compool Symbol *	Subunit
1KWIOUC	I/O Unit Controller
1KWCONV	Converter (PCDF)
1KWCONTR	Controller
1KWIPUB	IPUB
1KWDAMON	Distribution and Monitor Unit (PCDF)
1KWPORT	Port
1KWIOMP	I/O Microprocessor (IOP)
4KWVIU	Voiceband Interface Unit (VIF)
4KWTER	Terminal (TGR)
4KWNCSU	Network Clock Sync Unit (SCLK)
4KWCHAIN	CHAIN (NCLK)
4KWC1IPUB	Controller 1 IPUB (TMSP)
4KWC0IPUB	Controller 0 IPUB (TMSP)
4KWPPL	Pulse Point Matrix Left (SP)
4KWPPR	Pulse Point Matrix Right (SP)
4KWALC	A-Link Controller (TSI)
4KWPUBBR	PUBB Repeater
4KWCONL	Converter Left (SP)
4KWCONR	Converter Right (SP)
4KWDTU	Digroup Terminal Unit (DT)
4KWESU	Echo Suppressor Unit (EST)
4KWOSC	Oscillator (NCLK)
4KWDIU	Digital Interface Unit (DIF)
4KWREF	Reference (NCSU)
4KWSCLK	System Clock
4KWSCU	Service Circuit Unit (SCS)

* Octal/decimal values for these symbols are generic dependent. See compools IO1CATE and IO4CATE for latest values.

Unit Type Translations

See the Unit Type Translations layout on the following page.



UNIT TYPE MEMBER NO.
XL4UTYN
XL4MEMN
13
7 6
OR
0
HT4UT
GT4UTLEN
UT BLOCK ADDRESS
1 0
ENTRY INDEX TYPE ADDRESS
0 0
UNASSIGNED
HT4ALLZERO
0 7 7 4 0 0 0 0
LEN MAXMN
13 7 6 0
SUBTRANSLATOR
MEMN*LEN
SUBTRANSLATOR
ENTRY INDEX
XL4UEI
XL4UTENHTX
XL4UTENSTX
ENTRY INDEX
10
8 7
0
4*EI(7-0)
UT ENTRY
HT4UTEN
ADDRESS

Trunk Registers Printouts

Trunk Register Layout- Word 0

Bit 0-16 = Tag 1 - Function of State Code
17-23 = TR Code - State of Trunk

Decimal Value	Left Adjusted Octal	TR Codes
0	000	Unassigned
1	004	Idle Trunk
2	010	Idle trunk on which glare was detected
3	014	TR on interject engineered timing list
4	020	TR on base level engineered timing list
5	024	Trunk to dedicated TSI, or 1-Way to tone or announcement, or on base level engineered timing list
6	030	ICT in busy in a TR only state
7	034	2WOP Busy to CDO
8	040	OGT in waiting for answer state
9	044	OGT in the talking state
10	050	OGT in the clearback 1 state
11	054	OGT in the re-answer 1 state
12	060	OGT in the clearback 2 state
13	064	OGT in the re-answer 2 state
14	070	OGT in the clearback 3 state
15	074	OGT in the re-answer 3 state

Decimal Value	Left Adjusted Octal	TR Codes
16	100	Trunk used in TAN-to-TAN connection
17	104	Monitor available for use
18	110	Trunk is self-connected
19	114	Nailed-up connection busy to a TR
20	120	CAMA ICT in busy in a try only state
21	124	Trunk used for TAN nail-up
22	130	Q.931 PBX access protocol ICT on queue
23	134	ISUP (ISDN User Part) ICT on queue for a CR
24	140	ICT in clearback 1 state
25	144	ICT in re-answer 1 state
26	150	ICT in clearback 2 state
27	154	ICT in re-answer 2 state
28	160	ICT in clearback 3 state
29	164	ICT in re-answer 3 state
30	170	TR removed from MF queue
31	174	TR on MF ORIG queue
32	200	ICT busy to a CR
33	204	OGT busy to a CR
34	210	Service circuit on ICT busy to CR
35	214	Service circuit on OGT busy to CR

Decimal Value	Left Adjusted Octal	TR Codes
36	220	ICT dial tone start setup state
37	224	DTMF receiver busy to an ICT
38	230	Dial tone start ICT on queue for a DTMF receiver
39	234	IDTMFWK trunk on queue for a DTMF receiver and CR
40	240	Connection for growth testing
41	244	TR on MFC origination queue
42	250	Busy or idle occupied position keying trunk connected to MF-receiver
43	254	MF-receiver connected to position keying trunk
44	260	Service Observing
45	264	Waiting to service observe
46	270	Stall CC/VPA retest 5 sec to allow BLK received
47	274	Service circuit release timing
48	300	DP bylink trunk on 50-ms timing
49	304	DP DD-SD trunk on 150-ms timing
50	310	DP DD-SD trunk on 40-ms timing
51	314	DP bylink trunk with a digit RECON on 50-ms timing
52	320	Q.931 (PBX Access Protocol) Trunk in the clearing state

Decimal Value	Left Adjusted Octal	TR Codes
53	324	ISUP (ISDN User Part) trunk in the clearing state
54	330	MF ICT EA signaling—timing winks before connecting to an announcement
55	334	Unassigned
56	340	Guard timing
57	344	Incoming slave trunk of a broadband call
58	350	Outgoing slave trunk of a broadband call
59	354	Special CLF sent, wait RLG
60	360	Unassigned
61	364	Backward signal sent wait
62	370	Master trunk of a broadband call in the incoming stable state
63	374	Master outgoing trunk of a broadband call waiting for answer
64	400	Master outgoing trunk of a broadband call in the talking or connected state
65	404	DP origination error detected timing
66	410	INUP (CCS7 International ISUP) ICT on queue for a CR

Decimal Value	Left Adjusted Octal	TR Codes
67	414	CAMA operator position talking trunk waiting for an MF receiver to become available
68	420	INUP (CCS7 International ISUP) trunk in the clearing state
69	424	Timing the flashing of the calls waiting trunks during CAMA suspension
70	430	Timing for CAMA OP POS to ACK a DISC
71	434	CLF sent, wait RLG—CCIS or ISUP
72	440	Unassigned
73	444	CLF received, wait IAM
74	450	CLF sent, COT received, wait RLG
75	454	PDT sent, wait response—CCIS or ISUP
76	460	COT received, wait IAM
77	464	ITUP (International Telephone User Part) Trunk-in-the-Clearing State
78	470	ITUP (International Telephone User Part) ICT on queue for a CR
79	474	Unassigned
80	500	DP active state
81	504	DP active state and audit
82	510	Unassigned

Decimal Value	Left Adjusted Octal	TR Codes
83	514	Blue box fraud MFRCVR monitor connection to ICT
84	520	System integrity monitor CCIS trunk in talk state
85	524	Interim busy—CCIS, ISUP, or Q.931
86	530	CCIS trunk on engineered queue for CR
87	534	DP trunk on queue for CR
88	540	Unassigned
89	544	International MF ORIG queue for CR and RCVR
90	550	International busy to a link list
91	554	International ICT busy to a TR with voice path
92	560	International OGT busy to a TR with voice path
93	564	International 2nd TR with fixed TR4CODE
94	570	CCITT6 origination queue for a CR
95	574	Unassigned
96	600	TR is in audit state and on audit list
97	604	TR is in audit state and could not get on audit list
98	610	Test call incoming side
99	614	Test call outgoing side

Decimal Value	Left Adjusted Octal	TR Codes
100	620	System integrity confused incoming trunk
101	624	System integrity confused outgoing trunk
102	630	DPLS ICT waiting before sending answer
103	634	DPLS ICT sending answer
104	640	DPLS ICT has completed sending answer
105	644	DPLS ICT RCVD CLB while sending answer
106	650	DPLS ICT waiting before sending CLB
107	654	DPLS ICT sending CLB
108	660	DPLS ICT RCVD reanswer while sending CLB
109-110	664-670	Unassigned
111	674	international high-and-wet timing
112	700	International high-and-wet list
113	704	Out-of-service ignore
114	710	On trunk maintenance MW list—connected to MW tone
115	714	VIF operational controls being applied to this trunk
116	720	105 test line queue with TPT connection
117	724	High-and-wet timing
118	730	High-and-wet list

Decimal Value	Left Adjusted Octal	TR Codes
119	734	Trunk maintenance TR
120	740	Unassigned
121	744	Busy to trunk maintenance TR
122	750	Roll-back state
123	754	Reserved for recent change purposes
124	760	ICT busy to TMR
125	764	OGT busy to TMR
126	770	Service circuit on ICT busy to TMR
127	774	Service circuit on OGT busy to TMR

Trunk Register Layout- Word 1

Bit 0-18 = TAG 2—Function of state code
19 = RCP—Reserved for call processing
20-22 = MB—Maintenance busy bits
23 = CCS—Trunk is CCIS6, ISUP, ITUP, CCITT No. 6 or Q931

Decimal Value (Bits 20-23)	Combined CCIS and MB Bits
0	Non-CCIS trunk is not maintenance busy
1	Non-CCIS trunk is locked out due to maintenance or circuit change
2	Non-CCIS trunk is on camp-on list
3	Non-CCIS trunk is in error analysis
4	Non-CCIS trunk is in 1st filter state
5	Non-ccis trunk is in 2nd filter state
6	Non-CCIS trunk is in 3rd filter state
7	Non-CCIS trunk is in 4th filter state
8	CCIS trunk is not maintenance busy
9	CCIS lockout
10	CCIS camp-on
11	CCIS error analysis
12	CCIS blocked from far end
13	CCIS lockout and far end blocked
14	CCIS SCGA camp-on
15	CCIS lockout and timing of far-end blocking

International Second Trunk Register Layout- Word 0

Bit 0-5 = State-state of trunk within model (Program module)
6-9 = Model-processing model controlling trunk signals

Decimal Value	
0	Unassigned
1	CCITT5 incoming setup call stage
2	CCITT5 incoming post-setup call stage
3	CCITT5 incoming clearing call stage
4	CCITT5 high-and-wet model
5	CCITT5 outgoing setup call stage
6	CCITT5 Outgoing post-setup call stage
7	CCITT5 outgoing clearing call stage
8	Unassigned
9	CCITT6 incoming setup call stage
10	CCITT6 incoming post-setup call stage
11	CCITT7 incoming clearing call stage
12	CCITT7 high-and-wet model
13	CCITT6 outgoing setup call stage
14	CCITT6 outgoing post-setup call stage
15	CCITT6 outgoing clearing call stage

Bit 10 = Overlap answer required = CCITT5-In and CCITT5-Out
11 = Transit call = INTL-In and INTL-Out
12 = Time while awaiting answer
13-15 = Unassigned
16 = Linked to a call detail recording register
17-23 = TR code-state of trunk (same as TR code in 1st trunk register)

International Second Trunk Register Layout- Word 1

Bit 0-12 = RRN-(Modified) call detail recording register number
(RRN *8 +Base = RR address)
13-18 = Unassigned
19-23 = Status-CCIS, maintenance busy, reserved for call processing information

PUPHDATA- Peripheral Unit Phase Data Printouts

PUPHDATA- Digital Interface Frame (DIF) (Phase 2, 3, or 4)

See *Digital Interface Frame Printouts*.

PUPHDATA- Service Circuit System (SCS) (Phase 2, 3, or 4)

See *Service Circuit System/Service Circuit Unit (SCS/SCU) Printouts*.

PUPHDATA- Peripheral Units Phase 3 or 4

NOTE:
TTY request: **OP:ERAPDATA PUPHDATA:MFNUM** *a***!**
a = MFNUM or range of MFNUM for phase 2, 3, or 4

WORD 0	WORD 1	WORD 2	WORD 3	WORD 4	------
----------	----------	----------	----------	----------	------

(Pattern repeats in blocks of five words for each failing unit)

WORD 0

Bit 0-6 = Member number
7-13 = Unit type (right adjusted)

WORD 1

Bit 0-23 = Address where controller 0 failed

WORD 2

Bit 0-23 = Access test data that caused controller 0 to fail

WORD 3

Bit 0-23 = Address where controller 1 failed

WORD 4

Bit 0-23 = Access test data that caused controller 1 to fail

For simplex failures, address is all zeros for controller passing access test.

PUPHDATA- Duplex Failed Units

NOTE:
TTY request: **OP:ERAPDATA PUPHDATA:MFNUM** *a***!**

a = MFNUM or range of MFNUM for phase 2, 3, or 4

WORD 0 ----- ----- ----- ----- -----

WORD 0

Bit 0-6 = Member number
7-13 = Unit type (right adjusted)
14 = Indicates duplex failure

This output message form has the same number of words as the number of duplex failed units in the list printed after a phase.

CCIS- Common Channel Interoffice Signaling (CCIS) Printouts

CCIS Critical Registers

(Controller Data)

SOFTWARE STATUS C0	HARDWARE STATUS CO	ESR CO	CONTLR POLLING MASK	TERMINAL POLLING MASK	LSTR1	LSTR2*	LSTR6*
SOFTWARE STATUS C1	HARDWARE STATUS C1	ESR C1	CONTLR POLLING MASK	TERMINAL POLLING MASK	LSTR3	LSTR7*	LSTR8*

(Terminal Data Accessed via C0)

SOFTWARE STATUS REQ	MODE REQ	ESR	CONTROL REQ	INSTR ADDR REG	LSTR4	LKSTAT1*	LKSTAT2*

(Terminal Data Accessed via C1)

SOFTWARE STATUS REG	MODE REG	ESR	CONTROL REG	INSTR ADDR REG	LSTR5

NOTE:
Terminal dumped is terminal 0 when not specified in action message. Otherwise, terminal dumped is specified in action message.

* Data output for manual CREG DUMP Only.
LSTR = Link status registers (Datapool C14LSTR)
LKSTAT = Link status word (COMPOOL C140PLKSTAT)

Controller Software Status

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
6 = Indicates which controller is active
7 = Controller diagnostic requested
8 = Remove via TTY
12 = Controller OS
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on PU bus 0
17 = Controller cannot send on PU bus 0
18 = Controller cannot receive on PU bus 1
19 = Controller cannot send on PU bus 1
20-23 = PU maintenance code

Controller Hardware Status

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on bus 0
3 = Send on bus 1
4 = Divorce controller from mate
6 = Active unit
7 = False trouble indicator
8 = False data parity sent to TM
9 = False OPCODE parity sent to TM
10 = Controller appears active to TM (Quarantine)
11 = High and low SP indicators inhibited
12 = MA enable
13 = Receive on enable
14 = S0 enable
15 = S1 enable
16 = Divorce enable
18 = AU enable
19 = False TBL indicator enable
20 = FDP enable
21 = FOP enable
22 = Quarantine enable
23 = ISP enable

Controller Error Source Register

Bit 0 = ASW failure
2 = Even parity failure on PU bus
3 = Odd parity failure on PU bus
4 = TM data parity failure
5 = ASW not returned from TM
6 = ASW returned from an unaccessed TM
7 = Quarantine mode
8 = OPCODE decoder failure
9 = Data transfer failure—TIR to reply register
10 = Valid OPCODE indicator
12 = ASWF PEST
14 = PFE PEST
15 = PFO PEST
16 = TDPF PEST
17 = NTASW PEST
18 = EASW PEST
19 = QUAR PEST
20 = OPDF PEST
21 = DTF PEST
22 = VOC PEST

Controller Polling Mask

Bit 0-15 = Respective numbered TGR in-service

Terminal Polling Mask

Bit 0-15 = Respective numbered terminal in-service
(within TGR being dumped)

Terminal Software Status

Bit 7 = Terminal diagnostic requested
8 = Restore terminal by TTY
12 = Terminal OOS
15 = Terminal power off
16 = Terminal is actively signaling
17 = INIT or sync request made
18 = Terminal accessible via controller 1
19 = Terminal accessible via controller 0
20-23 = PU (terminal) maintenance code

Terminal Mode Register

Bit 5 = Maintenance read of data bus
6 = Write empty list pointer
7 = Snap contents of transfer bus and hold in PRB register
8 = Memory sequencer stop
9 = Bid overflow check
10 = CC-alert PEST
11 = Load indirect
12 = Modem maintenance control point—FT
13 = Modem maintenance control point—LT
14 = Modem maintenance control point—AL
15 = Modem maintenance control point—DL
16 = Modem maintenance control point—LC
17 = Single cycle mode
18 = Sequence check inhibit
19 = Inhibit instruction execution
20 = Terminal is stopped
21 = Ignore terminal failures
22 = Initialize terminal
23 = Terminal active = 0, standby = 1

Terminal Error Source Register

Bit 6 = Data set ready
7 = Send data (complemented)
8 = RCV data (complemented)
9 = Partial error summary B
10 = Partial error summary A
11 = Error summary
12 = Link list address error
13 = Link list data failure
14 = Modem transmit bid O/F
15 = Modem receive bid O/F
16 = Data memory C parity failure
17 = Data memory AB parity failure
18 = Program memory parity failure
19 = I/O list number error
20 = I/O decoder error
21 = Buffer O/F on I/O put
22 = I/O data parity failure
23 = I/O OPCODE parity failure

Terminal Control Register

Bit 4 = CC alert
5 = Buffer overflow
6 = Buffer full
7 = CC exercise
8 = Modem fine sync
9 = Modem external clock control
10 = Modem external clock input
11 = Modem carrier failure
12 = Data memory page 1 bit
20 = Data memory page 2 bit
21 = Transfer condition code
22 = Modem transmit bid
23 = Modem receive bid

Terminal Instruction Address Register

Bit 11-19 = TM program address at which TM stopped

CCIS Status and Pulse Point Reply

CI4TACSTREG—TGR Software Status

RCNT 21, 22

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
6 = Indicates active controller
7 = Controller diagnostic requested
8 = Controller to be restored only by TTY
12 = Controller out of service
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on bus 0
17 = Controller cannot send on bus 0
18 = Controller cannot receive on bus 1
19 = Controller cannot send on bus 1
20-23 = PU maintenance code

CI4TACSTREG—TGR Hardware Status

RCNT 19, 20

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on bus 0
3 = Send on bus 1
4 = Divorce controller from mate
6 = Indicates active controller
7 = False trouble indicator
8 = When set, false data parity is sent to TM
9 = When set, false OPCODE parity is sent to TM
10 = When set, controller will appear active to TM
11 = Inhibits high-and-low priority SP indications
12 = MA enable bit
13 = Receive on enable bit
14 = SO enable bit
15 = S1 enable bit
16 = Divorce enable bit
18 = AU enable bit
19 = Enable for false trouble indicator
20 = FDP enable bit
21 = FOP enable bit
22 = QUAR enable bit
23 = ISP enable bit

CI4TACESR—TGR Error Source Register

RCNT 15,16

Bit 0 = All-seems-well failure
2 = Even parity failure on PU bus
3 = Odd parity failure on PU bus
4 = Parity failure on term data bus
5 = All-seems-well not returned from terminal
6 = All-seems-well returned from an unaccessed terminal
7 = Controller in the quarantine mode
8 = TAC OPCODE decoder failure
9 = Error in the transfer of data from the terminal information register to reply register
10 = Valid OPCODE indicator
12 = ASWF PEST
14 = PFE PEST
15 = PFO PEST
16 = TDPF PEST
17 = NTASW PEST
18 = EASW PEST
19 = QUAR PEST set
20 = OPDF PEST
21 = DTF PEST
22 = VOC PEST

CI4ESR—Terminal Error Source Register

RCNT 54

Bit 6 = Data set ready
7 = Send data (complemented)
8 = RCV data (complemented)
9 = Partial error summary B
10 = Partial error summary A
11 = Error summary
12 = Link list address error
13 = Link list data failure
14 = Modem transmit bid O/F
15 = Modem receive bid O/F
16 = Data memory C parity failure
17 = Data memory AB parity failure
18 = Program memory parity failure
19 = I/O list number error
20 = I/O decoder error
21 = Buffer O/F on I/O put
22 = I/O data parity failure
23 = I/O OPCODE parity failure

CI4MR—Terminal Mode Register

RCNT 55

Bit 5 = Maintenance read of data bus
6 = Write empty list pointer
7 = Snap contents of transfer bus and hold in PRB register
8 = Memory sequencer stop
9 = Bid overflow check
10 = CC-alert PEST
11 = Load indirect
12 = Modem maintenance control point—FT
13 = Modem maintenance control point—LT
14 = Modem maintenance control point—AL
15 = Modem maintenance control point—DL
16 = Modem maintenance control point—LC
17 = Single cycle mode
18 = Sequence check inhibit
19 = Inhibit instruction execution
20 = Terminal is stopped
21 = Ignore terminal failures
22 = Initialize terminal
23 = Terminal active = 0, standby = 1

CI4CPR—TGR MA Pulse Point Reply

FLEV 39, 40

Bit 0 = Maintenance access bit set by pulse
1 = Receive on bus flip flop toggled by pulse
2 = State of send on bus zero flip flop
3 = State of send on bus one flip flop
4 = Quarantine state (when reset)
6 = Active unit state
8 = Peripheral bus even parity failure
9 = Peripheral bus odd parity failure
10 = Peripheral bus K-code match indication
11 = Peripheral bus M-bit indication
12 = Receive on bus flip flop
13 = Internal address field parity
14 = OPCODE decoder indication

DIF- Digital Interface Frame (DIF) Printouts

DIF/DIFE1 Critical Registers (FLEV and Interject Reports)

CSTATUS	HWSTATR	MADATA	FSTATUS	DIUOSO	DIUOS1
CESR	PEST	MPESRH	MPESRF	DIUSUMO	DIUSUM1
		MPESR*	MPRETE*		
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH
PSVL	PSVH	0....0	0....0	AUDR	TRKCNTR
		MAPESR*	EXCFESR*	EXCMASK*	
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS
SPSTATR	LUSPD0	LUSPD1	LUSPP0	LUSPP1	MPBSTAT
	MAPCNTRS*	MAPREGS*	MPSTKPTR*	MPPMCNT*	
	ESCNCNTL†				
URD1	URD2	URD3	URD4	URD5	URD6
URD7	URD8	URD9	URD10	URD11	URD12
CCPST0	CCPST1	MPIES	MPRTIS	MPMBSF	0....0
				EXECSMW*	
DACPST0	DACPST1	DRFPST0	DRFPST1	PSSSL	PSSSH
CALOW	CAHIGH	INTJ	0....0	0....0	0....0
MEMN	XLATE	FIRMWARE	5....5	5....5	5....5

Upper half = Controller 0
Lower half = Controller 1 (Not shown)

* DIFE1 Registers
† DIFE1 MF/DTMF 4ST registers

CSTATUS—Controller Software Status

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Controller divorced from mate
5 = Autonomous processing stopped (STOP)
6 = Active TSI clock
7 = Controller active
8 = Controller quarantined (EC)
10 = Cross controller update in progress (DIFE1 only)
11 = Controller slaved to mate
12 = Controller out of service
13 = Controller removed via TTY
20-23 = PU maintenance code

HWSTATR—Controller Hardware Status

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Controller divorced from mate
5 = Autonomous processing stopped
6 = Active TSI clock
7 = Controller active
8 = Controller quarantined
9 = Set for MP/SP PS memory lock
10 = Cross-controller update in progress (DIFE1 only)
11 = Controller clock slaved to mate
12 = Enable loading MA F/F
13 = Enable loading receive on (RO) F/F
14 = Enable loading S0 F/F
15 = Enable loading S1 F/F
16 = Enable loading DNORSE F/F
17 = Enable loading stop F/F
18 = Enable loading clock activity F/F
19 = Enable loading active/standby F/F
20 = Enable loading emergency cutoff F/F
21 = Enable loading PS memory write lock F/F
22 = Enable loading update bit
23 = Enable loading slave F/F

MADATA—Maintenance Access Data

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Controller divorced from mate
5 = Autonomous processing stopped
6 = Active TSI clock
7 = Controller active
8 = Receive bus parity failure even
9 = Receive bus parity failure odd
10 = K-code match
11 = Mode bit
12 = Complement of bit 1
13 = Controller quarantined
14 = AINT (Autonomous Interrupt)
15 = ASWF (All-seems-well failure)
16 = Unassigned OPCODE received
17 = Mode failure
18 = EXEC sequencer error
19 = Main clock framing error
20 = 16-mbit clock error
21 = Clock ESR summary (see CLKESR)
22 = Maintenance processor halted
23 = EXEC program store error

FSTATUS—Frame Software Status

Bit 0 = PU bus 0 at frame removed via TTY
1 = PU bus 1 at frame removed via TTY
2 = PU bus 0 out of service at frame
3 = PU bus 1 out of service at frame
4 = Switch in progress (clock SW, activity SW)
5 = Maintenance buffer overflow correction in progress
6 = Digit buffer overflow correction in progress
7 = Update controller in progress
10 = Protection switch in progress (spare DIU 32)
11 = Protection switch in progress (spare DIU 33)
12-17 = Spare assignment number for DIU 32
18-23 = Spare assignment number for DIU 33

DIUOS0—DIU Software OS Status

Bit 0-23 = DIU 0 through 23 out of service

DIUOS1—DIU Software OS Status

Bit 0-9 = DIU 24 through 33 out of service

CESR—Controller Primary ESR

Bit 0 = ASWF (All-seems-well failure—PUF F-level)
1 = AINT (Autonomous Interrupt—APUF F-Level)
2 = PU bus parity failure even
3 = PU bus parity failure odd
4 = INAPUT (Internal APUT—Interject)
5 = APUB (base level)
6 = Unassigned OPCODE received
7 = Mode failure
8 = Out-of-frame error
9 = 16-mbit clock error
10 = EXEC ESR summary (See IBIR)
11 = Internal bus ESR Summary (See IBIR)
12 = Maintenance processor ESR summary (See MPESR)
13 = SP ESR summary (See SPESR)
14 = Clock ESR summary (See CLKESR)
15 = MAP ESR summary (See MAPESR) (DIFE1 only)
15 = Frogger error (DIFE1—MF only)
16 = T1 line mismatch
17 = Internal bus mismatch
18 = Reply register mismatch
19 = Sequencer mismatch
20 = SP m-bit mismatch (DIFE1 only)
21 = Not connected (always 0)
22 = Low-frequency clock mismatch
23 = Not connected (always 0)

PEST—Controller PEST Register

Bit 0 = Inhibit ASW failure
1 = Inhibit autonomous interrupt
2 = Inhibit peripheral unit bus even parity failure
3 = Inhibit peripheral unit bus odd parity failure
4 = Inhibit internal APUT
5 = Inhibit APUB
6 = Inhibit unassigned OP-CODE
7 = Inhibit mode failure
8 = Inhibit out of frame
9 = Inhibit 16-mbit external clock error
10 = Inhibit EXEC local ESR summary
11 = Inhibit local ESR summary
12 = Inhibit MP local ESR summary
13 = Inhibit SP local ESR summary
14 = Inhibit clock local ESR summary
15 = Inhibit map local ESR summary failure
16 = Inhibit T1 line mismatch
17 = Inhibit internal bus mismatch
18 = Inhibit reply register mismatch
19 = Inhibit sequencer mismatch
20 = Inhibit SP mismatch
21 = Unused bit
22 = Inhibit low frequency clock mismatch
23 = Unused bit

MPESRH—Maintenance Processor ESR for Hardware Errors (Domestic DIF only)

Bit 0 = Hard-core parity mismatch
1 = CPU trap error
2 = DMA request time-out
3 = External bus read parity failure
4 = IB reply function failure
5 = Incoming CC port parity failure
6 = Incoming CN port parity failure
7 = Program store parity error (TM37)
8 = Unit maintenance bus error
9 = Unit scanner PEST error
10 = Unit maintenance bus shift register alarm
11 = Unit scan error 1
12 = Unit scan error 2
13 = Program store parity error (TM64)

MPESR—MP ESR and Halt PEST Bit (DIFE1 Only)

Bit 0-7 = Firmware error code (octal)
EC 0 = No errors
EC 1 = OS8 memory overload
EC 2 = Invalid macro OPCODE
EC 3 = EXEC MP service time-out
EC 4 = Compelled response not available
EC 5 = Invalid output request
EC 6 = Sanity time-out
EC 7 = Maintenance buffer overflow time-out
EC 10 = Unassigned interrupt error
EC 11 = Unused
EC 12 = Unit failure code ESR
EC 13 = Diagnostic failure code ESR
EC 14 = UMB failure pattern for EST
EC 15 = ESR pattern for scanner failure
EC 16 = MP ESR code for wrong ICOUNT
EC 17 = Micro DCON firmware failure
EC 20 = MP program store audit failure
EC 21 = SP program store audit failure
8 = Hard-core parity mismatch
9 = CPU trap error
10 = DMA request time-out
11 = External bus read parity failure
12 = Firmware ESR bit failure
13 = Incoming CC port parity failure

MPESR—MP ESR and Halt PEST bit (DIFE1 only) (Contd)

Bit 14 = Incoming CN port parity failure
15 = Main program store parity failure (TM37)
16 = Unit maintenance bus error
17 = Unit scanner PEST error
18 = Unit maintenance bus shift register alarm
19 = Unit scan error 1
20 = Unit scan error 2
21 = Always reset (0)
22 = MP halt error
23 = PEST bit for MP halt error

MPESRF—Maintenance Processor ESR for Firmware Errors (Domestic DIF only)

Bit 0-7 = Firmware error code (octal)
0 = No errors
1 = 0S8 memory overload
2 = Invalid macro OPCODE
3 = MP to EXEC service request time-out
4 = Compelled response not available
5 = Invalid output request
6 = Sanity time-out
7 = Maintenance buffer overflow time-out
10 = Unassigned interrupt error
12 = Excessive number of units alarming
14 = Unit maintenance bus error (TM38)
15 = Unit DMA scanner failure (TM43)
16 = MPESR code for bad interrupt count

MPRETE—MP Reset Enable Bit (DIFE1 Only)

Bit 0 = When set, EXEC halt interrupt (See EXCMASK) sends MPRESET

DIUSUM0—DIU 0-23 ESR Summary

Bit 0-23 = DIU 0 through 23 has an error

DIUSUM1—DIU 24-33 ESR Summary

Bit 0-9 = DIU 24 through 33 has an error

CLKESR—Clock Error Source Register

Bit 0 = CK16 energy detector for controller-unit link A
1 = Frame sync energy detector for controller-unit link A
2 = CK16 energy detector for controller-unit link B
3 = Frame sync energy detector for controller-unit link B
4 = GGC32PY and GGC32SY ESR for link A
5 = GGC32PY and GGC32SY ESR for link B
6 = GBC parity error
7 = Minor framing error
8 = Clock chain link A sync pulse error
9 = Clock chain link B sync pulse error
10 = GGCSY and 10msec clock error
11 = Super frame sync error
12 = Active/standby link A error
13 = Active/standby link B error
14 = Super frame pattern and SFSY link A error
15 = Super frame pattern and SFSY link B error
16 = Clock chain a GGCPY and GWCPY error
17 = Clock chain and SFSY ESR
18 = 1.5mhz and T1FSY link A error
19 = 1.5mhz and T1FSY link B error
20-23 = Not sourced from TM24 (CLKESR)

SPESR—Signal Processor Error ESR (Domestic DIF only)

Bit 0 = XROM output parity error
1 = XROM output parity error
2 = XROM address parity error
3 = XROM address parity error
4 = Cross-controller update loop parity error
5 = TSS output parity error
6 = Error on block M data A distribution
7 = Error on block M data B distribution
8 = Error on M data A distribution
9 = Error on M data B distribution
10 = Error on inhibit status A distribution
11 = Error on inhibit status B distribution
12 = E scanner mismatch
13 = E store address parity error
14 = M store address parity error
15 = Firmware failure to write SP register
16 = M store data mismatch
17 = IS store data mismatch
18 = XC M data loop mismatch
19 = XC is data loop mismatch
20 = IB receive parity error
21 = E data store mismatch
22 = Always reset (0)
23 = Always reset (0)

SPESR—Signal Processor ESR (DIFE1 only)

Bit 0 = State translator parity error
1 = Current trunk state parity error
2 = Looped jump control mismatch
3 = Looped RPTFLG control mismatch
4 = Block of M bit distribution update mismatch (DIU 0 through 15 and 32)
5 = Block of M bit distribution update mismatch (DIU 16 through 31 and 33)
6 = M bit distribution loop mismatch (DIU 0 through 15 and 32)
7 = M bit distribution loop mismatch (DIU 16 through 31 and 33)
8 = Looped PCIS distribution mismatch (DIU 0 through 15 and 32)
9 = Looped PCIS distribution mismatch (DIU 16 through 31 and 33)
10 = Cross-controller trunk state mismatch
11 = Always reset (0) (tied to bit 23)
12 = E bit scanner mismatch
13 = E bit store—address parity error
14 = M bit store—address parity error
15 = Duplicated E bit store mismatch
16 = Duplicated M Bit store mismatch
17 = Duplicated PCIS store mismatch
18 = Looped cross-controller M bit data mismatch
19 = Looped cross-controller PCIS data mismatch
20 = Internal bus data error
21 = TSS address parity error
22 = Current trunk state E bit mismatch
23 = Always reset (0) (tied to bit 11)

IBIR—Internal Bus ESR (Domestic DIF only)

NOTE:
Any bit 0-9 activates IBSUM bit in CESR; any bit 10-15 activates EXECSUM bit in CESR

Bit 0 = IB multiplexer A—return mismatch (TM48)
1 = IB multiplexer B—return mismatch (TM48)
2 = IB multiplexer C—return mismatch (TM48)
3 = IB multiplexer D—return mismatch (TM48)
4 = IB multiplexer E—return mismatch (TM48)
5 = Receive IB parity error
6 = Destination ACK error
7 = Source/DEST/OPCODE loop mismatch
8 = Source ACK error
9 = Maintenance buffer underflow
10 = ALU mismatch
11 = SP data ready error
12 = Unassigned MP OPCODE
13 = MP data ready error
14 = EXEC sequencer mismatch
15 = EXEC PROM parity error
16 = IB ESR summary (for bits 0-9)
17 = EXEC ESR summary (for bits 10-15)
18 = PEST for bits 0-17
19 = ROM check enable
20 = ROM check start
21 = Always reset (0) (TM59)
22 = Always reset (0) (TM59)
23 = Always reset (0) (TM59)

IBIR—Internal Bus ESR (DIFE1 only)

NOTE:
Any bit 0-9 activates IBSUM bit in CESR; any bit 10-15 and 22 activates EXECSUM bit in CESR

Bit 0 = IB multiplexer A—return mismatch (TM365)
1 = IB multiplexer B—return mismatch (TM365)
2 = IB multiplexer C—return mismatch (TM365)
3 = IB multiplexer D—return mismatch (TM365)
4 = IB multiplexer E—return mismatch (TM365)
5 = Receive IB parity error
6 = Destination ACK error
7 = Source/DEST/OPCODE loop mismatch
8 = Source ACK error
9 = Firmware error—maintenance buffer (See EXCFESR bits 11-14)
10 = ALU mismatch
11 = Firmware error—SP (See EXCFESR bits 0-10, 21, 22)
12 = Firmware error—EXEC (See EXCFESR bits 17-20)
13 = Firmware error—MP (See EXCFESR bits 15-16)
14 = EXEC sequencer mismatch
15 = EXEC PROM parity error
16 = IB ESR summary (for bits 0-9)
17 = EXEC ESR summary (for bits 10-15, 22)
18 = PEST for bits 0-17, 22
19 = ROM check enable
20 = ROM check start
21 = Always reset (0)
22 = Buffer RAM address parity check error
23 = Always reset (0)

EXR—Exercise Register

Bit 0 = MP time-out exercise
1 = General-purpose EX1
2 = General-purpose EX2
3 = General-purpose EX3
4 = General-purpose EX4
5 = General-purpose EX5
6 = General-purpose EX6
7 = Out-of-frame EX1
8 = Out-of-frame EX2
9 = Controller to subunit interface exercise
10 = Master clock A exercise
11 = Master clock B exercise
12-23 = Not sourced from TM364

PSRL—Protection Switch Request Register—Lower Half

Bit 0-15 = DIU 0 through 15 protection switch requested
17 = Lower group PSW enable

PSRH—Protection Switch Request Register—Higher Half

Bit 0-15 = DIU 16 through 31 protection switch requested
17 = Higher group PSW enable

PSVL—Protection Switch Verify—Lower Half

Bit 0-15 = PSV DIU 0 through 15
16 = PSV DIU 32
17 = No PSW active in lower half

PSVH—Protection Switch Verify—Higher Half

Bit 0-15 = PSV DIU 16 through 31
16 = PSV DIU 33
17 = No PSW active in higher half

MAPESR—Message Accounting Processor ESR and Status Register (DIFE1 only) (Bit 0-9 MAPESR, Bit 21-23 MAP Status Register) (All zeros for DIFE1-MF)

Bit 0 = Parity over receive IB data
1 = Parity on PTSS read
2 = Parity on PTSRPS read
3 = Trunk counters out of step
4 = Cross-controller link fault
5 = P-Bit link to SP fault
6 = PTSS MUX data parity
7 = Processor to PTSS parity
8 = P-bit store address parity
9 = Clock loop fault
21 = Reclocked stop for MAP
22 = Reclocked update for MAP
23 = Local PEST for MAP

EXCFESR—EXEC Firmware ESR (DIFE1 only)

Bit 0-23 = Contents of the buffer RAM error source firmware word (BRAMERR)

Bit 0 = HP report on maintenance trunk
1 = LP report on maintenance trunk
2 = SZ report on maintenance trunk
3 = DB report on maintenance trunk
4 = HP report to full buffer
5 = LP report to full buffer
6 = SZ report to full buffer
7 = DB report to full buffer
8 = SP data ready during SPINIT
9 = SP data ready during MP order
10 = SP data ready during CC order
11 = Maintenance buffer pointer underflow
12 = Maintenance buffer word counter mismatch
13 = Maintenance buffer pointers equal
14 = Maintenance buffer status underflow
15 = MP data ready error
16 = MP unassigned OPCODE
17 = Interrupt jump table—CC
18 = Interrupt jump table—MP
19 = Unassigned interrupt
20 = Front end error
21 = MFREPORT from invalid trunk (DIFE1—MF only)
22 = SP ready failure during MF report (DIFE1—MF only)
23 = Real-time frogger test failure (DIFE1—MF only)

EXCMASK—EXEC Interrupt Masks (DIFE1 only)

NOTE:
LVL 0 has the lowest priority, LVL F the highest
(setting an interrupt mask bit disables the interrupt task)

Bit 0 = Level 0—Maintenance processor
1 = Level 1—Real time
2-9 = Levels 2-9 unused
10 = Level A—Digit buffer report
11 = Level B—Seizure buffer report
12 = Level C—SP low priority buffer report
13 = Level D—SP high priority buffer report
14 = Level E—EXEC Halt
15 = Level F—CC

AUDR—Arithmetic unit data register (domestic DIF only)

Bit 0-23 = Data

TRKCNTR—SP Trunk Counters

Bit 0-11 = SP trunk counter 1 (Read)
12-23 = SP trunk counter 0 (Write)

BSTATR—Buffer Status Register

Bit 0 = High priority (HP) buffer full (0 = full, 1 = not full)
1 = High priority (HP) buffer empty (0 = empty, 1 = not empty)
2 = Low priority (LP) buffer full (0 = full, 1 = not full)
3 = Low priority (LP) buffer empty (0 = empty, 1 = not empty)
4 = Digit (DG) buffer full (0 = full, 1 = not full)
5 = Digit (DG) buffer empty (0 = empty, 1 = not empty)
6 = Seizure (SZ) buffer full (0 = full, 1 = not full)
7 = Seizure (SZ) buffer empty (0 = empty, 1 = not empty)
8 = Always reset (0)
9 = Always set (1)
10 = Always reset (0)
11 = Always set (1)

ESCNCNTL—E-Scanner Control Register
(DIF-E1 DTMF/4-State and DIF-E1 MF/4-State only)

NOTE:
L = Low (L) half DIU(s) 0-15
H = High (H) half DIU(s) 16-31

Bit 0-1 = Unused
2-5 = DIU 0-7 (Reset = 4 State, Set = Normal)
2 = L (DIU 0-1) Pair
3 = L (DIU 2-3) Pair
4 = L (DIU 4-5) Pair
5 = L (DIU 6-7) Pair
6 = DIU low half spare (32) set if spare is switched for MF or DTMF DIU
7-10 = DIU 8-15 (Reset = 4 state, Set = Normal)
7 = L (DIU 8, 9) Pair
8 = L (DIU 10, 11) Pair
9 = L (DIU 12, 13) Pair
10 = L (DIU 14, 15) Pair
11 = DIU high half spare (33) set if spare is switched for MF or DTMF DIU
12-15 = DIU 16-23 (Reset = 4 State, Set = Normal)
12 = H (DIU 16, 17) Pair
13 = H (DIU 18, 19) Pair
14 = H (DIU 20, 21) Pair
15 = H (DIU 22, 23) Pair
16 = DIU low half spare (Replicated bit 6)
17-20 = DIU 24-31 (Reset = 4 State, Set = Normal)
17 = H (DIU 24, 25) Pair
18 = H (DIU 26, 27) Pair
19 = H (DIU 28, 29) Pair
20 = H (DIU 30, 31) Pair
21 = DIU high half spare (Replicated bit 11)
22-23 = Unused

HPPTRS—High Priority Buffer Pointers

Bit 0-7 = Read pointer
8-15 = Write pointer

LPPTRS—Low Priority Buffer Pointers

Bit 0-7 = Read Pointer
8-15 = Write pointer

DBPTRS—Digit Buffer Pointers

Bit 0-7 = Read pointer
8-15 = Write pointer

SZPTRS—Seizure Buffer Pointers

Bit 0-7 = Read pointer
8-15 = Write pointer

MBPTRS—Maintenance Buffer Pointers

Bit 0-7 = Read Pointer
8-15 = Write Pointer

SPSTATR—SP Status Register

Bit 0 = Cross-controller SP update
1 = Inhibit cross-controller SP update
2-5 = Spare assignment number DIUs 0-15
6 = DIU 32 switch enable
7-10 = Spare assignment number DIUs 16-31
11 = DIU 33 switch enable
12-14 = Idle DIU's block digroup signaling exercise (octal)
EX 0 = Block signaling on digroup 1
EX 1 = Block signaling on digroup 2
EX 2 = Block signaling on digroup 3
EX 3 = Block signaling on digroup 4
EX 4 = Block signaling on digroup 5
EX 5, 6, 7 = Per digroup exercise disabled
15 = Idle DIUs block all digroup signaling exercise
16 = SP stop/run status (1 = Run)
17 = SP stop/run status for unit exercise (1 = Run)
18-22 = DIFE1 only
18 = Signal processor (SP) local PEST bit
19 = High priority (HP) buffer not full
20 = Low priority (LP) buffer not full
21 = Digit (DG) buffer not full
22 = Seizure (SZ) buffer not full

MAPCNTRS—MAP Trunk Counters (DIFE1 Only)
(All zeros for DIFE1—MF)

Bit 0-11 = Read trunk counter
12-23 = Write trunk counter

MAPREGS—MAP IPIR and PWR (DIFE1 Only) (All zeros for DIFE1—MF)

Bit 0-5 = Initial Pulsing Interval (IPI) Register
6-11 = Pulse Width (PW) Register

NOTE:
Each register contains, in octal, the number of 8-ms increments representing the IPI and PW for PPM

MPSTKPTR—MP Stack Pointer (DIFE1 Only)

Bit 0-15 = MP stack pointer (at time of error) (only valid when not all ones)
(0-7 = Low byte, 8-15 = High byte)

MPPMCNT—MP Program Counter (DIFE1 Only)

Bit 0-15 = Maintenance processor program counter (at time of error)
(only valid when not all ones)

LUSPD0—Look Up Signal Processor Link Error Data (0) (Domestic DIF Only)

Bit 0-23 = DIU 0 through 23 LUSP link error or unequipped DIU

LUSPD1—Look Up Signal Processor Link Error Data (1) (Domestic DIF Only)

Bit 0-9 = DIU 24 through 33 LUSP link error or unequipped DIU

LUSPP0—Look Up Signal Processor PEST Data (0) (Domestic DIF Only)

Bit 0-23 = LUSP PEST bits for DIU 0 through 23

LUSPP1—Look Up Signal Processor PEST data (1) (Domestic DIF Only)

Bit 0-9 = LUSP PEST bits for DIU 24 through 33

MPBSTAT—Maintenance Buffer Status

Bit 0-4 = Number of reports in EXEC MTC buffer (0-31)

URD1—12—Unit Raw Data (For Common Alarms) Common Format

BITS		
23 - - - - - - 16	15 - - - - - - 8	7 - - - - - - 0
THIRD DIU	SECOND DIU	FIRST DIU

URD1 = DIU 2, DIU 1, DIU 0
URD2 = DIU 5, DIU 4, DIU 3
URD3 = DIU 8, DIU 7, DIU 6
URD4 = DIU 11, DIU 10, DIU 9
URD5 = DIU 14, DIU 13, DIU 12
URD6 = DIU 17, DIU 16, DIU 15
URD7 = DIU 20, DIU 19, DIU 18
URD8 = DIU 23, DIU 22, DIU 21
URD9 = DIU 26, DIU 25, DIU 24
URD10 = DIU 29, DIU 28, DIU 27
URD11 = DIU 32, DIU 31, DIU 30
URD12 = ———, ———, DIU 33

Bit 0-7 = First DIU
8-15 = Second DIU
16-23 = Third DIU
Bit 0, 8, 16 = DS120 transmit alarm
1, 9, 17 = DS120 receive alarm
2, 10, 18 = Clock framing alarm
3, 11, 19 = Signaling parity alarm (EAS)
4, 12, 20 = Signaling parity alarm (MAS)
5, 13, 21 = Active/standby match alarm
6, 14, 22 = Common clear alarm
7, 15, 23 = (DIFE1 only) SP to unit interface error (SPUIE)

CCPST0—Common Alarm PESTs, DIU 0-23

Bit 0-23 = If set, indicates common alarms not PESTed for DIU 0 through 23

CCPST1—Common Alarm PESTs, DIU 24-33

Bit 0-9 = If set, indicates common alarms not PESTed for DIU 2 through 33

MPIES—MP Interrupt Enable Status Bits

0-3 = Task enable status code (octal)
0 = All tasks disabled
1 = All tasks disabled
2 = Task 1 enabled
3 = Task 1-2 enabled
4 = Task 1-3 enabled
5 = Task 1-4 enabled
6 = Task 1-5 enabled
7 = Task 1-6 enabled
10 = All tasks enabled
11 = MP halted
Task 1 = UART (TTY) task
Task 2 = MP bootstrap
Task 3 = MP macro execution
Task 4 = MP internal message execution
Task 5 = MP sanity timer
Task 6 = Unit maintenance (real-time tasks)
Task 7 = Unused

MPRTIS—MP Routine Task Inhibit Status (Domestic DIF Only)

Bit 0 = When set, routine exercise disabled
1 = When set, PSW audit disabled
2-15 = Replicated bit 0-1 data

MPRTIS—MP Routine Task Inhibit Status (DIFE1 only)

Bit 0 = When set, PSW audit disabled
1 = When set, MP program store audit disabled
2 = When set, SP program store audit disabled
3 = When set, MAP charge bit audit disabled
4 = When set, MAP rate pointer audit disabled
5 = When set, SP M, PCIS, TSW audit disabled
6 = When set, MAP routine exercise disabled
7 = When set, DIU routine exercise disabled
8-15 = Replicated bits 0-7

MPRTIS—MP Routine Task Inhibit Status (DIFE1-MF, DIFE1-DTMF only)

Bit 0 = When set, PSW audit disabled
1 = When set, MP program store audit disabled
2 = When set, SP program store audit disabled
3 = When set, TDIU, mode, ESCANNER audit disabled
4 = Not used
5 = When set, SP M, PCIS, TSW audit disabled
6 = Not used
7 = When set, DIU routine exercise disabled
8-15 = Replicated bits 0-7

EXECSMW—EXEC Saved Mask Word (DIFE1 only) Contains Image of the EXEC Interrupt Mask Saved Prior to the Interrupt (See EXCMASK)

Bit 0 = Saved MP interrupt mask (level 0)
1 = Saved real-time interrupt mask (level 1)
2 = Saved SP interrupt mask (level A,B,C,D)
7 = Saved halt interrupt mask (level E)

MPMBSF—MP MTC Maintenance Buffer Seizure Flag (Domestic DIF Only)

Bit 0 = When set, maintenance buffer in use

DACPST0—Digroup Alarm PESTs (0)

Bit 0-23 = If set, indicates digroup alarms not PESTed for DIU 0 through 23

DACPST1—Digroup Alarm PESTs (1)

Bit 0-9 = If set, indicates digroup alarms not PESTed for DIU 24 through 33

DRFPST0—Digroup Report Function PESTs (0)

Bit 0-23 = If set, indicates digroup report function not PESTed for DIU 0 through 23

DRFPST1—Digroup Report Function PESTs (1)

Bit 0-9 = If set, indicates digroup report function not PESTed for DIU 24 through 33

PSSSL—Protection Switch Firmware Status—Lower Half

Bit 0-15 = PSW status for DIU 0 through 15
17 = Lower group PSW enable

PSSSH—Protection Switch Firmware Status—Higher Half

Bit 0-15 = PSW Status for DIU 16 through 31
17 = Higher group PSW enable

CALOW—Common Alarms—Lower Half

Bit 0-6 = Suspect DIU (0-15)
7 = Multiple DIU’s alarming in lower half
8 = DS120 transmit alarm
9 = DS120 receive alarm
10 = Clock framing alarm
11 = Signaling parity alarm (EAS)
12 = Signaling parity alarm (MAS) (M + PCIS DIST.)
13 = Active/standby match alarm
14 = Common clear alarm
15 = SP to unit interface error (SPUIE) (DIFE1 only)
16 = PSW audit failure—lower half
17 = PSW audit failure—higher half
18-21 = PSW audit failure code (octal) (DIFE1-MF only)
- 0 = Unassigned
- 1 = Verify MP software image PSW low half
- 2 = Verify MP software image PSW high half
- 3 = Verify MP software image PSW low-vs-PROT switch register low
- 4 = Verify MP software image PSW high-vs-PROT switch register high
- 5 = Verify MP software image PSW low-vs-low SAN register
- 6 = Verify MP software image PSW high-vs-high SAN register
- 7 = Verify MP software image PSW low-vs-PROT switch verify register low
- 10 = Verify MP software image PSW high-vs-PROT switch verify register high

CAHIGH—Common Alarms—Higher Half

Bit 0-6 = Suspect DIU (16-33)
7 = Multiple DIUs alarming in higher half
8 = DS120 transmit alarm
9 = DS120 receive alarm
10 = Clock framing alarm
11 = Signaling parity alarm (EAS)
12 = Signaling parity alarm (MAS)
13 = Active/standby match alarm
14 = Common clear alarm
15 = SP to unit interface error (SPUIE) (DIFE1 only)
16 = PSW audit failure—lower half
17 = PSW audit failure—higher half
18-21 = PSW audit failure code (octal) (DIFE1-MF only)
- 0 = Unassigned
- 1 = Verify MP software image PSW low half
- 2 = Verify MP software image PSW high half
- 3 = Verify MP software image PSW low-vs-PROT switch register low
- 4 = Verify MP software image PSW high-vs-PROT switch register high
- 5 = Verify MP software image PSW low-vs-Low SAN register
- 6 = Verify MP software image PSW high-vs-high SAN register
- 7 = Verify MP software image PSW low-vs-PROT switch verify register low
- 10 = Verify MP software image PSW high-vs-PROT switch verify register high

INTJ—Interject Register

Bit 0 = Digit buffer overflow interject source
8 = Digit buffer overflow PEST

MEMN—DIF/DIFE1 Member Number

Bit 0-6 = DIF/DIFE1 Member Number (0-31)

XLATE—First Word of DIF/DIFE1 Unit Type Translator

Bit 18-23 = Frame type (octal)
10 = Vintage DIF (J68960A)
21 = DIFE-1 domestic
23 = MF/DIFE-1 domestic
24 = DTMF-4S/DIFE-1 domestic
25 = MF-4S/DIFE-1 domestic

FIRMWARE—Word 48 (Octal 60) of DIF/DIFE1 Unit Type Translator

Bit 0-3 = MP firmware version—controller 0
4-7 = SP Firmware version—controller 0
8-11 = EXEC firmware version—controller 0
12-15 = MP firmware version—controller 1
16-19 = SP firmware version—controller 1
20-23 = EXEC firmware version—controller 1

Auxiliary Data- (DIF/DIFE1 BLM Reports)

BSIZE	KIND	HEADER	DATA0	DATA1	DATA2
DATA3	DATA4	DATA5	DATA6	DATA7	DATA8
DATA9	DATA10	DATA11	DATA12	DATA13	DATA14
DATA15	MBPTRS*	MPBSTAT*	CCPST0*	CCPST1*	DIUOS0*
DIUOS1*					

* Data output only when kind = 1 (Illegitimate)

BSIZE—Auxiliary Data Block Size

Bit 1-6 = Block size

KIND—Kind of Report

Bit 0 = Kind of report
0 = Autonomous
1 = Illegitimate

HEADER—Frame Report Header (MB)

Bit 0-7 = Macro OPCODE
8-11 = Number of words in report
12 = segment report flag
13 = Autonomous flag
16-20 = Macro identification (assigned by Message Dispenser)

Frame Report Data Words 0-15

DATA0—Format 0—(Kind = 1, Illegitimate report)

Bit 0-23 = Data (may be a timed-out macro response,
or any format 1 below)

DATA0—Format 1—(Kind = 0, Autonomous report)

Bit 4-7 = Message ID (MID)

Use MID to distinguish DATA0 - DATA15 below

MID = 0

DATA0—Message ID=0—Digroup Alarm Report
Bit 0-3 = Digroup number
8-13 = DIU number
14 = Always zero
15 = Always zero
16-23 = SM1 digroup alarm data as shown. SM6, 7 or SM9, 10—
See DIU Internal Registers bits 0-7.

16 = XMT data alarm
17 = XMT D9 pattern alarm
18 = RCV-A alarm
19 = XMT signal alarm
20 = RCV D9 pattern alarm
21 = RCV data alarm
22 = RCV-B signal alarm
23 = RCV out-of-frame (OOF) alarm

DATA1—Message ID=0 Digroup Alarm Report
(See DIU Internal Register)
Bit 0-7 = Digroup alarm data
8-15 = Digroup report function data
16-23 = Digroup state

MID = 1

DATA0—Message ID=1—Digroup Report Function Alarm Report
Bit 0-3 = Digroup number
8-13 = DIU number
14 = Always zero
15 = Invalid PCC digroup state (SM10)
16-23 = SM1 digroup report function data as shown. SM6, 7, or SM9, 10—See DIU Internal Registers bit 0-7.
16 = Illegal inhibit signaling alarm
17 = No forced D2 status alarm
18 = Illegal forced D2 alarm
19 = RCV D2 summary alarm
20 = No inhibit signaling with OOF alarm
21 = No multiframe alignment alarm (SM9)
22 = Positive negative SLIP alarm
23 = Illegal multiframe alignment alarm (SM9)

DATA1—Message ID=1—Digroup Report Function Alarm Report (See DIU Internal Register)
Bit 0-7 = Digroup alarm data
8-15 = Digroup report function data
16-23 = Digroup state

MID = 2

DATA0—Message ID=2—Facility Status Report

Bit 0-3 = Digroup number
8-13 = DIU number
14 = 10^{-3} error rate alarm (CRC or Fe)
15 = 10^{-6} error rate alarm (CRC or Fe)
16 = Remote alarm (yellow)
17 = Local alarm (red)
18 = Out of frame (OOF)
19 = Negative SLIP
20 = Positive SLIP

For DIF or DIF-E1 (Domestic or MF)

21 = Message request
22 = Digroup alarm PEST
23 = Digroup report function PEST

For DIF-E1 (MF4ST or DTMF)

21 = Datalink down (SM10)
22 = Remote multiframe alignment alarm (SM9, SM10)
23 = Local multiframe alignment alarm (SM9, SM10)

MID = 3

DATA0—Message ID=3—Compelled Facility Status Report

Bit 0-23 = (Same format as MID = 2)

MID = 4

DATA0—Message ID=4—Routine Exercise Report
Bit 0-3 = Digroup number
8-13 = DIU number
21-23 = Failing routing code
1 = False all-unit decoding failure
2 = Overlapping UMB words failure
3 = Report stream MUX (SM2) failure
4 = Digroup MUX failure for a single digroup
5 = Common failures (SM2, SM3, SM4, SM5)
6 = Digroup exercise failure (each SM1)
7 = Service circuit digroup exercise failure (each SM6)

DATA1—Message ID=4—Routine Exercise Report
Bit 0-7 = Raw common alarm data at time of failure (for common failures) raw digroup alarm data at time of failure (for digroup failures)
9-16 = Set to zero for common failures, raw report function data at time of failure for digroup failures
18-23 = Failing test number

MID = 5

DATA0—Message ID=5—M/U Store Virtual Trunk Audit Report

Bit 0-3 = Code 0 = M store audit, 1 = U (PCIS) store audit
8-19 = Virtual trunk address
20 = Correct expected data from virtual trunk
21 = Incorrect data retrieved from virtual trunk

DATA1—Message ID=5—M/U Store Virtual Trunk Audit Report

Bit 0-8 = Total errors found

MID = 6

DATA0—Message ID=6—MAP Audit Report
(DIFE1 Domestic only)
Bit 0-3 = Task code
0 = PTSS
1 = RPS
2 = DIF-D PTSS
8-19 = Virtual trunk address
20-23 = Total errors (4 lower bits)

DATA1—Message ID=6—MAP Audit Report
(DIFE1 Domestic only)

For task code = 0 or 2

Bit 7 = Charge bit data
15 = Charge bit data
16-20 = Total errors (5 upper bits)

For task code = 1

Bit 0-6 = Failing rate pointer data
8-14 = Expected rate pointer data
16-20 = Total errors (5 upper bits)

MID = 7

DATA0—Message ID=7—SPTSS Virtual Trunk Audit Report
Bit 0-3 = Task code 0 = SPTSS
8-19 = Virtual trunk address

DATA1—Message ID=7—SPTSS Virtual Trunk Audit Report
Bit 0-15 = Correct expected data from virtual trunk
16-23 = Total errors (8 lower bits)

DATA2—Message ID=7—SPTSS Virtual Trunk Audit Report
Bit 0-15 = Incorrect data retrieved from virtual trunk
16 = Total errors (1 upper bit)

MID = 8

DATA0—Message ID=8—Mode, TDIU, ESCANNER Audit Report
Bit 0-3 = Digroup number
8-13 = DIU number
14 = ESCANNER bit for DIU pair (O = 4ST, 1 = not 4ST)
15-17 = Mode of digroup (DC if bits 0-3 = 0)
0 = ESCANNER bit and TDIU disagree
1 = One digroup in wrong mode
2 = Two digroups in wrong mode
3 = Three digroups in wrong mode
4 = Four digroups in wrong mode
5 = Unused
6 = MP "Saved Mode Word" for spare DIU incorrect
7 = SM1, SM6, SM7 has illegal bit set in digroup state word
(See DIU Internal Registers)

DATA1—Message ID=8—Mode, TDIU, ESCANNER Audit Report
Bit 0-3 = Number of digroup mode failures
4-7 = Number of digroup offset failures
8-15 = Mode of first failing digroup
16-23 = Offset of first failing digroup

MID = 9

DATA0—Message ID=9—TDIU Audit Report
Bit 0-3 = Digroup number
8-13 = DIU number
18-23 = TDIU (type of DIU)

MID = 10

DATA0—Message ID=10—Frequency Data Link Status Report
Bit 0-3 = Digroup number
8-13 = DIU number
16 = Data link status (0 = FDL up, 1 = FDL down)

MBPTRS—Maintenance Buffer Pointers

Bit 0-7 = Read pointer
8-15 = Write pointer

MPBSTAT—Maintenance Buffer Status

Bit 0-4 = Number of reports in MB (0-31)

CCPST0—Common Alarm PESTs, DIU 0-23

Bit 0-23 = If set, indicates common alarms not PESTed for DIU 0 through 23

CCPST1—Common Alarm PESTs, DIU 24-33

Bit 0-9 = If set, indicates common alarms not PESTed for DIU 24 through 33

DIUOS0—Out-of-Service DIU 0-23

Bit 0-23 = DIU 0 through 23 out of service

DIUOS1—Out-of-Service DIU 24-33

Bit 0-9 = DIU 24 through 33 out of service

DIU Internal Registers (Via TTY Request)

USTATUS	DGALM1	DGRF1	DGST1	DGALM2	DGRF2	DGST2	DGALM3
DGRF3	DGST3	DGALM4	DGRF4	DGST4	DGALM5	DGRF5	DGST5
CALM	XDIU	XDIUTDG	0....0	0....0	0....0	0....0	0....0
DGSTAT1	FD1	LCA1	RMA1	FEHIGH1	FELOW1	0....0	0....0
DGSTAT2	FD2	LCA2	RMA2	FEHIGH2	FELOW2	0....0	0....0
DGSTAT3	FD3	LCA3	RMA3	FEHIGH3	FELOW3	0....0	0....0
DGSTAT4	FD4	LCA4	RMA4	FEHIGH4	FELOW4	0....0	0....0
DGSTAT5	FD5	LCA5	RMA5	FEHIGH5	FELOW5	0....0	0....0

USTATUS—Software Unit Status Register

Bit 0 = DIU PESTed via TTY message
1 = Digroup 1 PESTed via TTY message
2 = Digroup 2 PESTed via TTY message
3 = Digroup 3 PESTed via TTY message
4 = Digroup 4 PESTed via TTY message
5 = Digroup 5 PESTed via TTY message
6 = Digroup 1 out of service
7 = Digroup 2 out of service
8 = Digroup 3 out of service
9 = Digroup 4 out of service
10 = Digroup 5 out of service
12 = DIU out of service
13 = DIU removed via TTY message
20-23 = Peripheral subunit maintenance code

DGALM1—5 SM1—Digroup Alarm data (Digroups 1 through 5)

Bit 0 = Transmit parity and zero code suppression alarm
1 = Transmit superframe parity alarm
2 = Receive ‘‘A’’ signaling ‘‘E’’ data parity alarm
3 = Transmit signaling parity alarm
4 = Receive pattern alarm
5 = Receive parity, clock and SLIP alarm
6 = Always zero
7 = Receive out-of-frame (at this instant)

DGRF1—5 SM1—Digroup Report Function Data (Digroups 1 through 5)

Bit 0 = Receive D2 forced to zero
1 = At least one out-of-frame received this 384-ms scan
2 = Receive framing error
3 = Receive negative SLIP
4 = Receive positive SLIP
5 = Receive inhibit signaling and parity alarm
6 = Transmit force D2 to zero
7 = Received at least one D2 forced to zero this 2-ms superframe

DGST1—5 SM1—Digroup State (always zero)

DGALM1—4 SM6, SM7—Digroup Alarm Data (Digroups 1 through 4)

Bit 0 = RCV PCM parity error
1 = Tone generator mismatch
2 = DSP error summary
3-7 = Always zero

DGRF1—4 SM6, SM7—Digroup Report Function Data (Digroups 1 through 4) (for DIFE1-MF SM6 and DIFE1-DTMF SM7)

Bit 0 = DSP 0 error (RCVR 3)
1 = DSP 1 error (RCVR 2)
2 = DSP 2 error (RCVR 1)
3 = DSP 3 error (RCVR 0)
4 = DSP 4 error (XMTR 3)
5 = DSP 5 error (XMTR 2)
6 = DSP 6 error (XMTR 1)
7 = DSP 7 error (XMTR 0)

DGST1—4 SM6, SM7—Digroup State (Always Zero)

DGALM1—5 SM9, SM10—Digroup Alarm Data (Digroups 1 through 5)

Bit 0 = Transmit formatter (TF): superframe sync alarm or internal parity alarm. If bit 3 is also set: input data parity alarm, SYN alarm, or lost communications with maintenance buffer (MB)
1 = Framer (FR): hardware alarm(s)
2 = Receive synchronizer (RS): signaling processing error. If bits 4 and 5 are also set: lost communication with MB
3 = TF: signaling alarm. If bit 0 is also set, see bit 0 explanation
4 = RS: pseudo random pattern error. If bits 2 and 5 are also set, see bit 2 explanation
5 = RS: RAM data output parity error system channel counter alarm, frame counter alarm, or GGC00 clock alarm. If bits 2 and 4 are also set, see bit 2 explanation
6 = SM9—Always zero
SM10—All TDIU modes except 64 CC and ESF—always zero
—64 CC and ESF modes (TDIU=037 or 060)
this bit=0 if PCC is normal
this bit=1 if PCC is not normal (See DGST 1-5 SM9, SM10—Digroup state 1, bits 4-6)
7 = FR: out-of-frame (at this instant)

DGRF1—5 SM9, SM10—Digroup Report Function Data (Digroups 1 through 5)

Bit 0 = Receiving yellow alarm
1 = At least one out-of-frame in this 384-ms scan
2 = FR: framing errors or CRC-6 errors
3 = RS: negative SLIP
4 = RS: positive SLIP
5 = RS: signaling extraction inhibited
6 = FR: transmit yellow alarm
7 = Received yellow alarm

DGST1—5 SM9, SM10—Digroup state 1 (Digroups 1 through 5) (Use if bit 7=0)

Bit 0 = Processor PROM CHECKSUM error
1 = Blue alarm
2 = Line error 0
3 = Line error 1
4-6 = SM9, SM10 (if DGALM 1-5 bit 6=0)
4 = FR: transmitting multiframe alignment alarm
5 = local multiframe alignment alarm
6 = remote multiframe alignment alarm
= SM10 (if DGALM 1-5 bit 6=1)
000 = PCC reset
001 = PCC sanity error
010 = PCC data link down
011 = PCC in PSW mode
7 = Word ID—always 0

DGST1—5 SM9, SM10—Digroup State 2 (Digroups 1 through 5)
(Use if bit 6 = 0 and bit 7 = 1)

Bit 0 = T1 frame format [SF(0) or ESF(1)]
1 = Zero code suppression, bits 1 and 2
2 = [0-NOZCS, 1-B8ZS, 2-ZCS, 3-B8ZS (64CC)]
3 = Signaling translation, bits 3 and 4
4 = (0-POTS, 1-CSDC, 2-IADC, 3-4 state)
5 = Signaling format [RB(0) or DMI(1)]
6 = Word ID—always 0
7 = Word ID—always 1

DGST1—5 SM9, SM10—Digroup state 3 (Digroups 1 through 5) (Use if bit 6=1 and bit 7=1)

Bit 0 = Programmed time of unit 0
1 = Programmed time of unit 1
2 = Programmed time of unit 2
3 = Programmed time of unit 3
4 = Programmed time of unit 4
5 = Always 0
6 = Word ID—always 1
7 = Word ID—always 1

SM9 and SM10 Notes: After SM9 or SM10 reset (power ON or MP order), the processor goes through diagnostics. If a failure exists, then DGALM, DGRF, DGST have the following values:

DGALM	DGRF	DGST	Explanation
00000377	00000377	00000377	Executing initialization code with no errors
00000377	00000377	00000240	Processor failure
00000377	00000377	00000201	Processor PROM failure
00000377	00000377	00000202	Maintenance buffer failure
00000377	00000377	00000300	PCC hardware failure (SM10 only)
00000000	00000000	00000000	Reset complete

CALM—DIU Common alarm data

Bit 0 = DS 120 transmit alarm
1 = DS 120 receive alarm
2 = Clock framing alarm
3 = E signaling parity alarm
4 = M or U signaling parity alarm
5 = Active/standby match alarm
6 = Common clear alarm
7 = SP-DIU interface error (DIFE1 only)

XDIU—DIU Translations Data

Bit 0-9 = TSI member-SPC-port
- 0-2 = TSI port connection
- 3 = (0) TSI SPC 0 (1) TSI SPC 1
- 4-9 = TSI member where DIU is connected

10-14 = Type of digroup state assignment
- 0 = Not removed when protection switched
- 1 = Removed when protection switched

15-17 = DIU member version states (states 0, 2-7 unassigned)
- state 1 = initial DIU version

18-21 = Type of hardware (THC)
- 0 = DIU not equipped
- 1 = SM1B— voice DIU
- 6 = SM6—MF service circuit DIU
- 9 = SM9—Hardware pack
- 10 = SM10 hardware pack

22-23 = Unused

XDIUTDG—Digroup Translation Data

Bit 0-3 = Type of digroup 1
4-7 = Type of digroup 2
8-11 = Type of digroup 3
12-15 = Type of digroup 4
16-19 = Type of digroup 5
20-23 = Type of hardware (5THW)

DGSTAT1—Digroup Status Information (Digroups 1 through 5)

Bit 0 = Digroup is in remote alarm state
1 = Digroup is in local alarm state
2 = Out-of-frame occurrence
3 = Last SLIP was a negative SLIP
4 = Last SLIP was a positive SLIP
5 = Deferred message request bit
6 = Remote multiframe alignment alarm
7 = Local multiframe alignment alarm

FD1-5—Digroup Forced Digit Information (Digroups 1 through 5)

Bit 0 = If set, transmit force-D2-to-zero requested
1-2 = Requested/actual force-D2-to-zero error hit timer
3-7 = Local multiframe alignment alarm timer

LCA1-5—Digroup Local Alarm Data (Digroups 1 through 5)

Bit 0-5 = Local alarm timer
6 = Digroup alarm PEST bit (0 = PEST set)
7 = DG report function PEST bit (0 = PEST set)

RMA1-5—Digroup Remote Alarm Data (Digroups 1 through 5)

Bit 0-1 = Remote alarm timer
2 = 16-second timer bit for OOS
3-4 = Digroup alarm hit timer
5-6 = Steady SLIP hit timer
7 = 16-second timer bit for SLIP

FEHIGH1-5—Digroup Frame Error High Count (Digroups 1 through 5)

Bit 0-5 = Number of framing errors for 1-in-1000 error rate calculations (16-second interval)
6-7 = Illegal inhibit status hit timer

FELOW1-5—Digroup Frame Error Low Count (Digroups 1 through 5)

Bit 0-5 = Number of framing errors for 1-in-1,000,000 error rate calculations (40-minute interval)
6 = When set, 1-in-1000 error rate was exceeded and reported
7 = When set, 1-in-1,000,000 error rate was exceeded and reported

PUPHDATA- DIF (Phase 2, 3, or 4)

NOTE:
TTY request: **OP:ERAPDATA PUPHDATA:MFNUM** ***a*****!**

a = MFNUM or range of MFNUM for phase 2, 3, or 4

WORD 0 WORD 1 WORD 2 WORD 3 WORD 4 WORD 5
WORD 6 WORD 7

WORDS 0-3 = Controller 0
WORDS 4-7 = Controller 1

WORD 0,4

Bit 0-2 = Boot task ACK code
- 0 = A boot task has been spawned
- 1 = A spawned task did not complete
- 2 = Controllers booted duplex
- 3 = One controller removed
- 4 = Both controllers failed
- 5 = Request error
- 6 = No boot task requested
- 7 = PMOS returned fail

3-5 = Request code
- 0 = Do not boot DIF frame
- 1 = Hard controller boot (PH4)
- 2 = Soft1 controller boot (PH2, PH3)
- 3 = Soft2 controller boot (PH3)
- 4 = Remove controller

WORD 0,4 (Contd)

Bit 6-9 = Request data code (octal)
0 = DIF frame unequipped
1 = DIF frame in growth state
2 = Controller in Zap Table
3 = Controller in Zero Start Table
4 = Controller in Babbling Bus Table
5 = Controller is out of service
6 = Controller boot level is hardware level 4
7 = Controller normal
10 = TSI duplex failure
11 = PUB duplex failure
12 = TSI and PUB duplex failure

10 = Final configuration request
(0 = controller removed, 1 = controller restored)

WORD 0,4 (Contd)

Bit 11-16 = Failing data code (octal)
0 = All tests pass or controller already removed prior to phase
1 = Not used
2 = Message Dispenser—frame rejected parallel INIT macro
3 = PMOS—failed to schedule ‘‘parallel polling (INIT macro)’’
4 = Not used
5 = Maincomm pulse on bus failure
6 = PU bus loop failure
7 = Internal bus loop failure
10 = Message Dispenser—parallel polling (INIT macro) timeout
12 = IPUB out-of-service failure
13-23 = See INIT macro failure code below
24 = Not Used
25 = Not Used
26 = Not Used
27 = Topic—restore failure
30 = Post restore access test failure
31 = PMOS—failed to schedule ‘‘restore’’
32 = PMOS—failed to schedule ‘‘remove’’
34 = See INIT macro failure code below
40 = MAP INIT failure
41 = SP INIT failure
52-77 = See INIT macro failure code
17-22 = Unit type

INIT Macro Failure Code

Octal Code	MP Function	INIT Macro Failure
13		Invalid data failure
14	ERSCH	ESR check failure
15	MU STORE	M store check failure
16	PSW	PSW register check failure
17	PTR INIT	Buffer pointer failure
20	UNCL	Unit MTCE bus failure
21	ZESR	EXR register failure
22	SP INIT	SP INIT failure or SP failed to write TBIT 0 = 1
23		Extended bus cutoff failure (PUC only)
34	SP INIT	Single step trunk counter failure
52	HINITMAP	MAP ESR failure
53	DISUCL	Unit MTCE bus failure
54	MU Store	U store check failure
55	MU Store	SP TSS virtual trunk INIT failure or rate pointer store failure or charge bit initialization failure
56	PSW	PSW register hardware vs software failure
57	MU Store	MAP PTSS check failure
60	PSRAC	PSWH register check failure
61	ZESR	CLCK, IBIR, SPESR, CESR register failure
62	SP INIT	SP failed to write TBIT = 0
63	PSRAC	SP SAN registers failed verify
64	PTR INIT	Buffer status register failure
65	ZESR	PEST register failure
66	ZESR	MAP ESR failed to 0
67	ESRCH	MAP ESR failed to 0
70	DICLEAR	Unit MTCE bus failure

INIT Macro Failure Code (Contd)

Octal Code	MP Function	INIT Macro Failure
71	SP INIT	TBit 0 not set
72	SP Cycle	Start SP order fails
73	SP Cycle	Inhibit update failure
74	SP INIT	Single step IBIR failure
75	SP Cycle	Block (EX0, EX1, EX2) failure
76	SP Cycle	Stop SP order fails
77	SP INIT	TRK CNTR 1 ≠ 0 After SP single step

WORDS 1,5

INIT Macro Pass

Bit 0-16 = INIT Macro DIU 0-16 Status (1 = Pass, 0 = Fail)
17-23 = Member number

INIT Macro Fail

Bit 0-16 = Failing order
17 = Fail data code (octal)
0 = Fail
1 = Success
18-23 = Fail code

WORDS 2,6

INIT Macro Pass

Bit 0-16 = INIT macro DIU 17-33 status (1 = Pass, 0 = Fail)
17 = Establish clock failure
18 = Pump failure

INIT macro fail

Bit 0-16 = Don't care
17 = Establish clock failure
18 = Pump failure

WORDS 3,7

INIT macro pass

Bit 0-23 = Always zero

INIT macro fail

Bit 0-23 = Failing reply data

DT- Digroup Trunk Printouts

DT Fault Detected

DT4STATO-DT4STAT1 PMD NUM IMP Entity PMD Add MSGHLF2 MSGHLF1

Software Status Word O

Bit 7 = DT Diagnostic request
8 = DT restore only via TTY
12 = DT duplex out of service
15 = Major power ALM
20-23 = Maintenance state
State 0 = Normal
State 1 = DT in diagnostic
State 2 = DT in exercise
State 3 = DT in FR or EA
State 4 = In time-out
State 5 = Unequipped
State 6 = In restoral update
State 7 = In growth
State 8 = Under repair
State 9 = Waiting for final restoral
State 10 = Under restoral
State 11 = Spare code
State 12 = OS by phase
State 13 = Being initialized
State 14 = Spare code
State 15 = In ignore

Software Status Word 1

Bit 0-7 = Respective numbered DTU OOS
8 = Spare unit out of service
9 = Controller 0 out of service
10 = Controller 1 out of service
12-14 = Protection switch number
15 = Enable protection switch
16 = Protection switch in progress flag
17 = System clock switch in progress flag
18 = DT SYS CLK select
19 = DT line CLK select
20 = DT MSG NTWK select

PMD Number Data

Bit 0-7 = PMD number
9-12 = ERAT decision code
15-18 = ERAT action code

Implicated Entity

Bit 0-10 = Same as 0-10 in software STAT1

PMD Address

Bit 0-23 = PMD address

The data in MSGHLF2 and MSGHLF1 is dependent on the PMD number in bits 0-7 of the PMD NUM word.

For PMD numbers 12, 15, and 23 (octal), MSGHLF2 and MSGHLF1 are zero

For PMD number 1, the formats are:

MSGHLF2 bit 0-11 = K-code of the associated SP2
12-15 = Port associated with the SP2
16-22 = DT member number
MSGHLF1 bit 0-23 = Relative address in DTFRMAIN of the failing order

For PMD number 17, the formats are:

MSGHLF2 Bit 0 = Transmitter in trouble
1 = Invalid DT OPCODE
2 = Mismatch between message sequences
3 = Mismatch between I/O sequences
4 = DT CLK bit error
5 = Frame timing error
6 = DT sanity check
7 = Reclock register serial mismatch
8 = Shift register mismatch
9 = Incoming serial bit stream parity error
10 = Invalid I/O sequence call state
15-18 = The DT port number calculated by the DT and sent to the SP2 during testing
23 = When set indicates that no data and/or no timing was received by the SP2 from the DT during link testing
MSGHLF1 Bit 0-23 = Same as MSGHLF2

PMD Address (Contd)

NOTE:
In duplex SP2 configurations, MSGHLF2 has the link results through SP controller 1, and MSGHLF1 has the link results through SP controller 0. If the associated SP2 controller 0 is out of service, MSGHLF2 and MSGHLF1 are the same, and the results are read through SP2 controller 1. If controller 1 is out of service, MSGHLF2 is all 7s and MSGHLF1 has valid data.

For all other PMD numbers, the following formats are used for MSGHLF2 and MSGHLF1:

MSGHLF2—Message Half 2

Bit 0-2 = Function number
3-6 = Time of unit number
7-10 = DT number
11-15 = DT to CC internal OPCODE

MSGHLF1—Message Half 1

The format of MSGHLF1 is dependent on MSGHLF2. The decimal equivalent of bits 3-6 (time-of-unit number) and bits 0-2 (function number) together indicate the format to be utilized (See formats listed on next page).

Format 12,6 Digroup status report

Bit 0-2 = Digroup addressed
3-6 = DT unit addressed
7 = Remote alarm status
8 = Local alarm status
9 = Out-of-frame indication
10 = SLIP indicator
11 = SLIP polarity
12 = PEST status
13 = (Format 12,7) DF report camp-on status

Format 12,7 Bipolar Test Violations

Bit 0-2 = Digroup addressed
3-6 = DT unit
7 = Unit test failed status
8 = Bipolar violation report indicator
9 = DF report camp-on status (12, 7)
10-11 = BV sample high count
12-13 = BV sample low count

Format 13,7 Protection Switch Status

Bit 0-2 = Protection switch number
3 = Enable protection switch
4-12 = DT units 0 through 8, respectively

Format 14,7 Controller ESR

Bit 1 = Report functions
2 = Clock 0 ABS
3 = ABS0
4 = Clock 1 ABS
5 = ABS1
6 = Message STRM mismatch
7 = Enable protection switch
8 = Mismatch
9 = DT system clock select
10 = DT line clock select
11 = DT message network select 0
12 = DT message network select 1
13 = Exercise 1
14 = Exercise 0
15 = Any protection SW relay

Format 15,7 UNIT ESR

Bit 0-8 = DT units 0 through 8

Bit 20-23 Software Status (Octal)

- 0 = DT is normal
- 1 = DT in diagnostic
- 2 = DT in exercise
- 3 = DT in fault recovery/error analysis
- 4 = DT in time-out
- 5 = DT is unequipped
- 6 = DT in restoral update
- 7 = DT in growth state
- 10 = DT under repair
- 11 = DT waiting for final restore
- 12 = DT under restoral
- 13 = DT spare code
- 14 = DT out of service by phase
- 15 = DT being initialized
- 16 = DT spare code
- 17 = DT in ignore

DUC/DUS- Data Unit Controller/Data Unit Selector Printout

Internal DUS Registers and Test Results Data Block (DUSREG)

DS10BR	DS1IBR	DS10AR	DS1IRA	DS1SELREG	DS1SVRM
DS10IRA	DS1MCR	DS1PCR	DS1ESR	GCPA	GCPR
TFWRD*	TADDR*	TVCTR*	TRSLT*	XFRWD0*	SVR1*
TFWRDB*	TADDRB*	TVCTRB*	TRSLTB*	XFRWD1*	SVR2*
OVSTAT+0*	STAT0+0*	RSTAT0+1*	RSTAT1+0*	RSTAT1+1*	SVR3*
STAT0+0†	STAT0+1†	STAT0+2†	STAT0+3†	STAT0+4	†STAT0+5†
STAT0+6†	STAT0+7†	STAT0+8†	STAT0+9†	STAT0+10	†STAT0+11†
STAT0+12†	STAT0+13†	STAT0+14†	STAT0+15†	AU1RSTAT+12	AU1RSTAT+13
STAT0+0†	STAT0+1†	STAT0+2†	STAT0+3†	STAT0+4†	STAT0+5†
STAT0+6†	STAT0+7†	STAT0+8†	STAT0+9†	STAT0+10†	STAT0+11†
STAT0+12†	STAT0+13†	STAT0+14†	STAT0+15†	AU1RSTAT+12	AU1RSTAT+13
STAT1+0†	STAT1+1†	STAT1+2†	STAT1+3†	STAT1+4†	STAT1+5†
STAT1+6†	STAT1+7†	STAT1+8†	STAT1+9†	STAT1+10†	STAT1+11†
STAT1+12†	STAT1+13†	STAT1+14†	STAT1+15†	XR	XR
TU1AREG	TU1DR	TU1CCREG	TU1DBR	TU1COM	TU1PCREG
TU1MR	TU1CBREG	TU1ECREG‡ TU1WDCREG¶	TU1RCRCREG‡ TU1WCRCREG¶	TU1MIS	TU1OIS
TU1TTS	TU1SRR(23-18) TU1LTCR(17-0)	TU1CIBG	TU1HLSB	0.....0	0.....0

* Prefix this word with DS1R_ or DS1R
† Prefix this word with DC1R
‡ Contain bits 12-23
¶ Contain bits 0-11

DS1OBR—DUS Output Buffer Register (Contains output data for CC-DUS reads and DUS-core writes; also contains the read/write data after a CC-DUC read/write operation)

Bit 0-23 = Output buffer register

DS1IBR—DUS Input Buffer Register (Buffers input data for CC-DUS/DUC writes and DUS-core reads)

Bit 0-23 = Input buffer register

DS1OAR—DUS Output Address Register (Contains core address for DUS-core reads and writes)

Bit 0-15 = CS/PS address
16-20 = CS/PS K-code
21 = CS/PS bit
22 = Read bit
23 = Write bit

DS1IRA—DUS Inhibit Register (Controls which DUC the DUS polls: 0 = do not poll associated DUC, 1 = poll associated DUC)

Bit 0-15 = Inhibit register bits

DS1SELREG—DUS Select Register (Indicates which DUC the DUS is polling at this time as controlled by the DUS inhibit register)

Bit 0-15 = Selector bits

DS1SVRM—DUS Select Verify Register (Contains the select verify response of the DUC just accessed)

Bit 0-15 = SVR Bits

DS10IRA—DUS Operational Interject Register [Indicates which DUC(s) are requesting operational interject]

Bit 0-15 = OIR bits
16 = OI bit from DUCs

DS1MCR—DUS Maintenance and Control Register (applies nonoperational conditions to the DUS for maintenance purposes)

Bit 0 = Inhibit DUC clock sync
1 = Inhibit ASW/ASWF reset
5 = SR complete
10 = Inhibit enable and dummy block reset
12 = Invert DUC address parity
13 = Invert DUC data select
14 = Inhibit DUC select
16 = Inhibit DUC reply reset and gatein
17 = AUS SR mode flip-flop
18 = Mode decoder 1
19 = Mode decoder 2
22 = DUC reply bus ASW
23 = DUC control bus parity

DS1PCR—DUS PEST Control Register (Allows internal DUS errors to be inhibited)

Bit 0 = Maintenance interject
1 = Operational interject
5 = CC communications
Clock sync error
Clock internal error
IAR parity failure
IBR parity failure
CC sequencer error
Decoder error
Mode error
10 = CS/PS communications
ASW/ASWF error
CS/PS sequencer error
IBR parity failure (CS/PS)
12 = DUC communications
DUC sequencer error
DUC reply bus parity failure
DUC reply bus ASW failure
DUC control bus parity failure
DUC select verify failure
DUC maintenance interject

DS1ESR—DUS Error Summary Register (Contains summary of DUS error conditions if they exist)

Bit 0 = DUC sequencer error
1 = CS/PS sequencer error
6 = Mode error
9 = IBR parity failure (CS/PS)
10 = CS/PS ASW error
12 = DUC reply parity failure
13 = DUC reply ASW failure
14 = DUC poll parity failure (control bus)
18 = DUC select verify failure
19 = DUC maintenance interject reply

GCPA—GCP Address of DUS

Bit 0-23 = GCP address

GCPR—GCP Results of DUS

Bit 0 = Maintenance interject flip-flop
1 = Maintenance (‘‘1’’ Side)
2 = Maintenance (‘‘0’’ Side)
3 = Clock sync error
4 = Clock internal error
6 = IAR parity failure
7 = IBR parity failure
9 = Decoder failure (O/N)
10 = Mode error
11 = DUC write bus parity
12 = DUC address bus parity
14 = CC COM sequencer freeze F/F
16 = CC sequencer error
17 = K-code match
18 = Control read
19 = Control write
20 = IAR all ‘‘1’’ detector
21 = IAR all ‘‘0’’ detector
22 = IBR all ‘‘1’’ detector
23 = IBR all ‘‘0’’ detector

If DS1R_XFRWD0 bit 23 = 0, then

DS1R_TFWRD(B)—Test Failure Word (Contains unique identification of the test that the DUS/DUC failed during fault recovery—for the suspected faulty DUS/DUC)

Bit 0-5 = Test group
6-11 = Test subroutine
12-17 = Test number

If DS1R_XFRWD0 bit 23 = 1, then

DS1R_TFWRD—DC1P_WORDU<DUC>

Bit 0-4 = Function number
5 = Tape is read-only or read write
6 = Tape has an SL volume reader
7 = Diagnostic in progress
8-9 = State of this unit
00 = Not linked (NLK)
01 = Active (ACT)
10 = Standby (STBY)
11 = Assigned (ASG)
10 = Autonomous operation in progress on this unit
11 = DUC is in-service
12-14 = Tape position
000 = Unknown
001 = Read at BOT
010 = Not tape mounted
011 = Released at BOT
100 = At valid write point
101 = Not at valid write point
110 = Released (not at BOT)
111 = New tape mounted
15 = File state changing
16 = File is open
17 = BOT passed
18-22 = DOC number

DS1R_TFWRDB—DC1P-WORDA <FUNCTION> Same Layout as DS1RTFWRD Word Associated with Function Specified in Item DC1P_FNUMU in Word DS1R_TFWRD

If DS1R_XFRWD0 bit 23 = 0, then

DS1R_TADDR(B)—Test Address (Contains the internal DUS/DUC address where the test failed—for the suspected faulty DUS/DUC)

If bit 10 = 0, then: Bit 0-5 = TUC address
6-9 = TUC K-code

If bit 10 = 1, then: Bit 0-9 = TUC K-code
11-15 = DUS K-code
16-21 = AU K-code

If DS1R_XFRWD0 bit 23 = 1, then

DS1R_TADDR—DC1U-DWRTN <DUC>

Bit 0-23 = DUAD address where processing will resume

DS1R_TADDRB—DC1U-TORTN <DUC>

Bit 0-23 = Usually contains DUAD address indicating last command from client

If DS1R_XFRWD0 bit 23 = 0, then

DS1R_TVCTR(B)—Test Vector (Contains the input test data— test vector—applied to the DUS/DUC—for the suspected faulty DUS/DUC)

Bit 0-23 = Test vector

If DS1R_XFRWD0 bit 23 = 1, then

DS1R_TVCTR—DC1U-UCB5 <DUC>

Bit 0 = DUC job was aborted
1 = DUC was switched to other DUS
2 = TTY message received
3 = Key change has occurred
4 = Operation complete was received
5 = Autonomous operation in progress
6 = Reconfiguration request from DUFR
7 = Start a program segment
15 = Set if request to demount key in OIS register of TUC has changed state
16 = Set if unassigned mode key in OIS register of TUC has changed state
17 = Set if AMA mode key in OIS register of TUC has changed state
18 = Set if utility mode key in OIS register of TUC has changed state
19 = Set if SR mode key in OIS register of TUC has changed state
20 = Set if remote mode key in OIS register of TUC has changed state
21 = Set if tape over reads key in OIS register of TUC has changed state
22 = Set if door opened key in OIS register of TUC has changed state
23 = Set if write enable ring key in OIS register of TUC has changed state

DS1R_TVCTRB—DC1U-UCFO <DUC>

Bit 0 = Data overwrite on last operation
1 = Late-data on last operation
2 = Time-out on last operation
3 = FOF detected on last operation
4 = LRC fail on last operation
5 = CRC fail on last operation
6 = VRC fail on last operation
7 = Read-block-completed on last operation
8 = CHR-CNT-EQ-O on last operation
9 = Invalid command detected on last operation
10 = BOT detected on last operation
11 = EOT detected on last operation
12 = BOT is present before command is sent
13 = EOT is present before command is sent
14 = Invalid mode detected on last operation
15 = State of request to demount key in OIS register of TUC
16 = State of unassigned mode key in OIS register of TUC
17 = State of AMA mode key in OIS register of TUC
18 = State of utility mode key in OIS register of TUC
19 = State of SR mode key in OIS register of TUC
20 = State of remote mode key in OIS register of TUC
21 = State of tape over heads key in OIS register of TUC
22 = State of door opened key in OIS register of TUC
23 = State of write enable ring key in OIS register of TUC

If DSR1_XFRWDO Bit 23 = 0, then

DS1R_TRSLT(B)—Test Result (Contains the output test results received from the DUS/DUC—for the suspected faulty DUS/DUC)

Bit 0-23 = Test results

If DSR1_XFRWDO bit 23 = 1, then

DS1R_TRSLT—J

Bit 0-23 = Sometimes will contain DUAD address that will explain reason for TUC removal

DS1R_TRSLTB—Test Result Buffer (Contains the output test result received from the DUS/DUC— for the DUS/DUC used in alternate route testing)

DS1R_XFRWDO—Transfer Trace Word 0 (Contains a point-by-point trace of the program flow through the pident DUFRTADM)

Bit 0 = Transfer trace point 0
1 = Transfer trace point 1
2 = Transfer trace point 2
3 = Transfer trace point 3
4 = Transfer trace point 4
5 = Transfer trace point 5
6 = Transfer trace point 6
7 = Transfer trace point 7
8 = Transfer trace point 8
9 = Transfer trace point 9
10 = Transfer trace point 10
11 = Transfer trace point 11
12 = Transfer trace point 12
13 = Transfer trace point 13
14 = Transfer trace point 14

DS1R_XFRWDO—Transfer Trace Word 0 (Contains a point-by-point trace of the program flow through the pident DUFRTADM) (Contd)

15 = Transfer trace point 15
16 = Transfer trace point 16
17 = Transfer trace point 17
18 = Transfer trace point 18
19 = Transfer trace point 19
20 = Transfer trace point 20
21 = Transfer trace point 21
22 = Transfer trace point 22
23 = Transfer trace point 23

DS1R_XFRWD1—Transfer Trace Word 1 (Contains a point-by-point trace of the program flow through the pident DUFRPUCDU)

Layout same as DS1R_XFRWDO

DS1R_TFWRDB—Test Failure Word Buffer (Contains unique identification of the test that the DUS/DUC failed during fault recovery—for the DUS/DUC used in alternate route testing)

(See DS1R_TFWRD)

DS1R_TADDRB—Test Address Buffer (Contains the internal DUS/DUC address where the test failed—for the DUS/DUC used in alternate route testing)

(See DS1R_TFWRD)

DS1R_TVCTRB—Test Vector - Buffer (Contains the input test data - test vector—applied to the DUS/DUC—for the DUS/DUC used in alternate route testing)

(See DS1R_TFWRD)

DS1R_TRSLTB—Test Result Buffer (Contains the output test results received from the DUS/DUC—for the DUS/DUC used in alternate route testing)

(See DS1R_TFWRD)

DS1R_SVR1—Contains the Identity of the DUC in Bits 0-15 (In 1/N format) that is to be used in diagnosing the DUS just removed from service

DS1R_SVR2—Contains the Identity of the DUC in Bits 0-15 (In 1/N format) used for alternate route testing by the fault recovery program

DS1ROVSTAT—Overall Status for ADS Community 0 (Status that applies to the ADS community as a whole)

Bit 0 = Inhibit fast data job requests
1-5 = Fast data job in progress
6 = Update DUC status after bootstrap
7 = AU complex configuration is frozen
8 = Off-line stop bit
9 = DUAD hold CTR over DUFR segment breaks
10 = Inhibit TUC switches
23 = Notify DUAD to update DUC status

DS1RSTATO—Status Word 0 for DUSs 0 and 1 (ADS Community 0)(Contains control and status flags)

Bit 0 = Helper unit for DGN tape motion phases
2 = RMV DUS from SRV FLG
3 = Restore DUS to SRV FLG
4 = TTY REQ to RST DUS W/O DGN
7 = REQ phase 1 of DUS DGN
8 = REQ PH1 and PH2 of DUS DGN

DS1RSTAT1—Status Word 1 for DUSs 0 and 1 (ADS Community 0) (Contains error history information)

Bit 0-2 = ESR error count
3-5 = SVR error count
6-8 = Count of DUFR TSTS=STP and DGN TSTS=ATP

DS1R—SVR3—Contains the Identity of the DUC (In 1/N format) with which the DUS was Communicating at the Time of Failure

Bit 0-15 = DUC identity

DC1RSTATO—Status Word 0 for DUCs 0 through 15 (ADS Community 0) at Interject (Contains control and status flags)

Bit 0 = DUC temporarily OSS flag
1 = Both DUS OOS indicator
2 = Out-of-service FLG
3 = RMV DUC from SRV FLG
4 = Restore DUC to SRV FLG
5 = Tape motion has failed
7 = DUC REQ CONFG change
8 = REQ DUC be configured to DUS 0 (1 = Not true)
9 = REQ DUC be configured to DUS 1 (1 = Not true)
10 = DUC presently CONF to DUS 0 (1 = not true)
11 = DUC presently CONF to DUS 1 (1 = not true)
12 = RMVD DUS 0 - suspect DUC TBL
13 = RMVD DUS 1 - suspect DUC TBL
14 = RMVD DUC - suspect DUS 0 TBL
15 = RMVD DUC - suspect DUS 1 TBL
16 = Retry DUC TST via DUS 0
17 = Retry DUC TST via DUS 1
18 = DUC TBL associated with DUS 0
19 = DUC TBL associated with DUS 1
21 = Do not restore DUC
22 = DUC off line FLG
23 = REQ DUC DGN FLG

DC1RSTATO—Status Word 0 for DUCs 0 through 15 (ADS Community 0) after Interject (contains control and status flags)

Layout same as DC1RSTATO

AU1RSTAT—Common AU Status Word for DUSs 0 and 1 (ADS Community 0) at Interject (Contains control and status flags)

Bit 0 = AU marked in trouble
1 = AU in off-line configuration
2 = AU stopped and in maintenance mode
4 = Request diagnosis for AU
5 = AU K-code trouble
8 = Do not restore AU

AU1RSTAT—Common AU Status Word for DUSs 0 and 1 (ADS Community 0) after Interject (Contains control and status flags)

Layout same as AU1RSTAT

DC1RSTAT1—Status Word 1 for DUCs 0 through 15 (ADS Community 0) (Contains control and status flags)

Bit 3 = TTY request to restore DUC W/O DGN
4 = Nonemergency remove bit
5 = INH all job requests for this DUC
8 = Normal switch request of DUC to DUS 0
9 = Normal switch request of DUC to DUS 1

DC1RSTAT2—Status Word 2 for DUCs 0 through 15 (ADS Community 0) (Contains error history information)

Bit 0-5 = Count of DUFR TST=STF and DGN TST=ATP

XR—Contains the Actual K-Code of the DUS Involved in the Interject

Bit 11-15 = DUS K-code

TU1AREG—TUC Store Address Register (Contains core address for TUC-core reads and writes)

Bit 0-21 = Address register

TU1DR—TUC Data Register (Contains output/input data for TUC-core writes/reads)

Bit 0-23 = TUC data register

TU1CCREG—TUC Character Count Register (Contains 1s complement of number of 8-bit characters to be read/written from/to tape)

Bit 0-17 = Character count register

TU1DBR—TUC Data Buffer Register (Buffers the data that is read/written from/to tape between the data register and the tape for writes onto tape. It divides the 24 bits of data into three [3] 8-bit tape characters—for read from tape. It generates a 24-bit data word from the three [3] 8-bit tape characters read from tape)

Bit 0-23 = TUC data buffer register

TU1COM—TUC Command Register (Contains the TUC tape transport operational command, that is, write, read, backspace, etc.)

Bit 0 = Stop the TUC softly
1 = Fast forward to EOT with erase current
2 = Write
3 = Fill
4 = Write EOF
8 = Rewind to BOT
9 = Fast forward to EOT
10 = Read
11 = Advance 1 block
12 = Backspace 1 block
13 = Forward locate EOF
14 = Reverse locate EOF

TU1PCREG—TUC PEST Control Register (Allows internal TUC and/or tape transport errors to be inhibited)

Bit 1 = Operational interject
2 = DUC communications
Clock sync
Address parity
R/W REG select
Data parity
3 = Autonomous sequence failures
Increment parity
CLPP self-check
Data XFER parity
Buffer parity fail on write
Internal register select
Time-out
Late data
Data overwrite
4 = Tape transfer failures
Erase-write current
CAPSTAN motion abnormal
TT converter output
TT converter –48 v input
SERVO lamp
Temperature abnormal

TU1MR—TUC Maintenance Register (Applies nonoperational conditions to the TUC for maintenance purposes)

Bit 0 = Trouble F/F
1 = Suppress tape motion and erase-write current
2 = CLPP maintenance input 1
3 = CLPP maintenance input 2
4 = Gate ECR to tape read register
5 = GOSPLE mode
6 = Step 1 clock cycle
9 = Force tape parity track to zero

TU1CBREG—TUC Control Bus Register (Contains internal TUC maintenance interject, operational interject, read, write status)

Bit 0 = MI request
1 = OI request
2 = Read request
3 = Write request

TU1ECREG—TUC Error Correct Register—9 Bits (Contains the bit to be corrected when operating in the error correct read mode)

Bit 0-8 = Error correct register

TU1WDREG—TUC Write Driver Register—9 Bits (Contains the 8-bit character and parity being written onto tape)

Bit 0-8 = Write driver register

TU1RCRCREG—TUC Read CRC Register—9 Bits (Generates and accumulates the CRC character from data being written onto tape)

Bit 0-8 = Read CRC register

TU1WCRCREG—TUC Write CRC Register—9 Bits

Bit 0-8 = Write CRC register

TU1MIS—TUC Maintenance Interject Status Register (Contains the source of the TUC maintenance interject request)

Bit 0 = Clock sync failure
1 = Address parity failure
2 = R/W Register select failure
3 = Data parity failure
8 = Increment parity failure
9 = CLPP self-check failure
10 = Data XFER parity failure
11 = Buffer parity failure on write
12 = Autonomous register select failure
13 = Time-out
14 = Late data
15 = Data overwrite
16 = Erase-write read current failure
17 = CAPSTAN motion abnormal
18 = TT DC PWR failure
19 = TT –48 v failure (R/O)
21 = SERVO lamp failure (R/O)
22 = Temperature abnormal (R/O)

TU10IS—TUC Operational Interject Status Register (Contains the source of the TUC operational interject request)

Bit 0 = Operation complete
1 = BOT detected
2 = EOT detected
3 = EOF detected
4 = VRC failure
5 = CRC failure
6 = LRC failure
8 = Read dummy-block complete
9 = CHAR count equal zero
10 = Invalid mode
11 = Invalid command
12 = AMA mode request
13 = Request to demount
14 = Unassigned mode
15 = AMA mode
16 = Utility mode
17 = SR mode
18 = SR mode buffer (R/O)
19 = Tape over heads (R/O)
20 = Remote mode (R/O)
21 = Door closed (R/O)
22 = Write-enable ring in (R/O)
23 = Key changed

TU1TTS—TUC and Tape Transport Status Register (Contains internal TUC and tape transport hardware status indications)

Bit 0 = TT ready (R/O)
1 = BOT present (R/O)
2 = EOT present (R/O)
3 = Forward motion (R/O)
4 = Reverse motion (R/O)
5 = Stopped motion (R/O)
6 = Rewinding (R/O)
7 = LRC equal zero (R/O)
8 = Busy/idle (1/0)
9 = Park/normal (1/0)
10 = Low/high speed (1/0)
11 = Forward/reverse motion (1/0)
12 = Stop/start (1/0)
14 = Enable CAPSTAN motion indicator
16 = Active
17 = Standby
18 = Assigned secondary standby
19 = Read only/read-write (1/0)
20 = File open/closed (1/0)
21 = Acknowledge demount request
22 = OK to demount

TU1SRR—TUC System Reinitialization Sequencer Register (Contains the state flip-flops of the TUC system reinitialization sequencer)

Bit 18 = SR active
19 = SR state 0
20 = SR state 1
21 = SR state 2
22 = SR after activate

TU1LTCR—TUC Long Timer Counter Register (TUC hardware timer)

Bit 0-17 = Long timer counter

TU1CIBG—TUC Write Clock and IBG Detector Register (TUC interblock gap detector register)

Bit 12-18 = Write clock
19 = Received one data character
20-23 = IBG detector

TU1HLSB—TUC Hot-Line Scan Back Results (TUC front end error indicators received on every TUC hot-line address)

Bit 0 = Hot-line decoder select
1 = Bus select F/F
2 = State of TF/F
3 = Clock out of sync
4 = Inhibit clock out of sync
5 = Auto clock set request
8 = Slow down request has occurred
9 = No correction necessary has occurred
10 = Speed up request has occurred
11 = Clock initialization has occurred
14 = Clock out of sync has occurred
15 = FB174 pack missing from LOC 72-33
16 = FB174 pack missing from LOC 76-33

EST- Echo Suppressor Terminal Printouts

EST Critical Registers (FLEV Reports)

CSTATUS	STATR	USTATUS	USTAR	CESR1	CESR2
CESR3	CESR4	PEST12	PEST34	USR	UPR
EXR	PSR	PCM	UPA	LLSSR	TSSSR
CSTATUS	STATR	USTATUS	USTAR	CESR1	CESR2
CESR3	CESR4	PEST12	PEST34	USR	UPR
EXR	PSR	PCM	UPA	LLSSR	TSSSR

Upper Half Controller 0
Lower Half Controller 1

NOTE:
Prefix all words with ES4.

CSTATUS—Software Status

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
5 = Emergency cutoff
6 = Indicates which TSI clock is being used
7 = Controller diagnostic requested
8 = Remove via TTY
9 = When set, controller is active
10 = Controller is slave to mate
11 = Controller send-ons are clamped to zero
12 = Controller out of service
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Power off controller
16 = Controller cannot receive on PU bus 0
17 = Controller cannot send on PU bus 0
18 = Controller cannot receive on PU bus 1
19 = Controller cannot send on pu bus 1
20-23 = PU maintenance code

STATR—Hardware Status

Bit 0 = Read write/MA pulse set-maintenance access bit
1 = Read write/MA toggled-PU bus which controller receives from
2 = Controller sends to PUB 0
3 = Controller sends to PUB 1
4 = Divorce controller from mate
5 = Emergency cutoff
6 = Indicates which TSI clock is being received
7 = Indicates which controller is active
8 = When set, the ESC clock is the slave of its mate
9 = Clamp send on FFS to 0
10 = Spare
11 = Spare
12 = MA enable bit (bit 0)
13 = RO enable bit (bit 1)
14 = S0 enable bit (bit 2)
15 = S1 enable bit (bit 3)
16 = DIV enable bit (bit 4)
17 = ES4EC enable bit (bit 5)
18 = ES4CA enable bit (bit 6)
19 = ES4AS enable bit (bit 7)
20 = ES4ST enable bit (bit 8)
21 = ES4SOC enable bit (bit 9)
22 = SP1 enable bit
23 = SP2 enable bit

USTATUS—Unit Software Status

Bit 0 = ESU 0 is not available
1 = ESU 1 is not available
2 = ESU 2 is not available
3 = ESU 3 is not available
4 = ESU 4 is not available
5 = ESU 5 is not available
6 = ESU 6 is not available
7 = ESU 7 is not available
8 = ESU 8 is not available
9 = ESU 9 is not available
10 = ESU 10 is not available
11 = ESU 11 is not available
12 = ESU 12 is not available
13 = ESU 13 is not available
14 = ESU 14 is not available
15-18 = Spare assignment number
14 = spare ESU number
19 = Protection switch is in progress
20 = Clock settling in progress
21 = Keep bit for controller 0 clock
22 = Keep bit for controller 1 clock

USTAR—Unit Status

Bit 0 = Clear all unit ESRS and LLS
0 = Clear
1 = Stop clear
1 = Unit exercise bit 1
2 = Unit exercise bit 2
3 = Stop the vector generator 0 = Stop, 1 = Start
4 = Vectors are running—64-MS delay complete

CESR1—Error Source Register 1

Bit 0 = ASWF (All-seems-well failure — PUF F-level)
1 = AINT (Autonomous interrupt — APUF F-level)
2 = Parity error over even bits of PU bus
3 = Parity error over odd bits of PU bus
4 = an error occurred in an ESU
5 = Sequencer mismatch-PU read/write sequencer
6 = Mode failure
7 = Reply bus parity mismatch
8 = Internal bus mismatch
9 = GGC sync mismatch for GGCA
11 = Clock out of frame
12 = 17X OPCODE destination error
13 = Unassigned OPCODE
14 = Destination code error
15 = OPCODE decoder error

CESR2—Error Source Register 2

Bit 0 = Unit summary register error
1 = Controller scanner comparison
2 = As flip-flop loop comparison
3 = TSS RAM output parity error
4 = S/F register compare input data vs written data
5 = E/D register compare function failure
6 = TSS input register parity
7 = TSS RAM daisychain loop failure
8 = Unit write compare function
9 = Vector shift register parity and daisychain ERR on maintenance bus
10 = Vector clock sync failure
11 = Vector countdown comparison error

CESR3—Error Source Register 3

Bit 0 = OR of CESR3 and CESR4
2 = TSS acknowledge
3 = LLS acknowledge
5 = Unused—ACK for new autonomous functions
6 = Autonomous function error (ASWF for AUTO FUNC)
11 = LLS to internal bus parity error
12 = LLS status register or RAM parity error
13 = LLS sequencer error
14 = LLS status register load error
15 = LLS status register read error

CESR4—Error Source Register 4

Bit 0 = 16-MB clock error (energy detector)
1 = 16-MB clock daisychain (energy detector)
2 = GBC clock error (framing check)
3 = GBC sync daisychain MM
4 = GWC counter error MM
5 = GWC sync daisychain MM
6 = GGC sync daisychain MM
7 = ORed clock daisychain error (bits 1, 3, 5, 6)
8 = Vector ROM1 parity error
9 = Vector ROM2 parity error
10 = Vector ROM3 parity error
11 = Vector ROM4 parity error

PEST12—PEST Register 12

Bit 0 = Inhibit ASWF
1 = Inhibit AINT
2 = Inhibit input
3 = CESR1MM PEST
12 = CESR1 non-MM PEST
13 = Sequencer MM PEST
14 = Mode failure PEST
15 = CESR2 PEST

PEST34—PEST Register 34

Bit 0 = PEST CESR34 summary
1 = PEST CESR3 bit-1
2 = PEST CESR3 bit-4
3 = PEST CESR3 bits-7, 8, 9
12 = CESR3 others PEST
13 = PEST CESR3 bit-5
14 = PEST CESR3 bit-6
15 = PEST CESR4

USR—Unit Error Summary

Bit 0 = Read only-error summary from unit 0
1 = Read only-error summary from unit 1
2 = Read only-error summary from unit 2
3 = Read only-error summary from unit 3
4 = Read only-error summary from unit 4
5 = Read only-error summary from unit 5
6 = Read only-error summary from unit 6
7 = Read only-error summary from unit 7
8 = Read only-error summary from unit 8
9 = Read only-error summary from unit 9
10 = Read only-error summary from unit 10
11 = Read only-error summary from unit 11
12 = Read only-error summary from unit 12
13 = Read only-error summary from unit 13
14 = Read only-error summary from unit 14

UPR—Unit PEST

Bit 0 = Inhibit errors from unit 0
1 = Inhibit errors from unit 1
2 = Inhibit errors from unit 2
3 = Inhibit errors from unit 3
4 = Inhibit errors from unit 4
5 = Inhibit errors from unit 5
6 = Inhibit errors from unit 6
7 = Inhibit errors from unit 7
8 = Inhibit errors from unit 8
9 = Inhibit errors from unit 9
10 = Inhibit errors from unit 10
11 = Inhibit errors from unit 11
12 = Inhibit errors from unit 12
13 = Inhibit errors from unit 13
14 = Inhibit errors from unit 14

EXR—Exercise

Bit 0 = Exercise error 1
1 = Exercise error 2
2 = Exercise error 3
3 = Exercise error 4
4 = Clock exercise error 5
5 = Clock exercise error 6
6 = Clock exercise error 7
7 = Exercise error 8

PSR—Protection Switch Request

Bit 0 = Protection switch request for unit 0
1 = Protection switch request for unit 1
2 = Protection switch request for unit 2
3 = Protection switch request for unit 3
4 = Protection switch request for unit 4
5 = Protection switch request for unit 5
6 = Protection switch request for unit 6
7 = Protection switch request for unit 7
8 = Protection switch request for unit 8
9 = Protection switch request for unit 9
10 = Protection switch request for unit 10
11 = Protection switch request for unit 11
12 = Protection switch request for unit 12
13 = Protection switch request for unit 13
14 = Unused
15 = PS enable RO-set via 4ESMIENPSW and 4ESMIDISPSW—writing B15 of this register does not affect ES4PSEN but sets b15 of register UPA

PCM—Protection Switch Relay Contact Monitor

Bit 0 = Protection switch monitor relay for ESU 0 read only
1 = Protection switch monitor relay for ESU 1 read only
2 = Protection switch monitor relay for ESU 2 read only
3 = Protection switch monitor relay for ESU 3 read only
4 = Protection switch monitor relay for ESU 4 read only
5 = Protection switch monitor relay for ESU 5 read only
6 = Protection switch monitor relay for ESU 6 read only
7 = Protection switch monitor relay for ESU 7 read only
8 = Protection switch monitor relay for ESU 8 read only
9 = Protection switch monitor relay for ESU 9 read only
10 = Protection switch monitor relay for ESU 10 read only
11 = Protection switch monitor relay for ESU 11 read only
12 = Protection switch monitor relay for ESU 12 read only
13 = Protection switch monitor relay for ESU 13 read only

UPA—Unit Power Alarm

Bit 0 = Power alarm unit 0
1 = Power alram unit 1
2 = Power alram unit 2
3 = Power alram unit 3
4 = Power alram unit 4
5 = Power alram unit 5
6 = Power alram unit 6
7 = Power alram unit 7
8 = Power alarm unit 8
9 = Power alarm unit 9
10 = Power alarm unit 10
11 = Power alarm unit 11
12 = Power alarm unit 12
13 = Power alarm unit 13
14 = Power alarm unit 14
15 = Enable UPA read from PSR B15—write via PSR B15—B15 of this register cannot be written

LLSSR—Last Look Store Status

Bit 0-4 = LLS address bits 1-4 = unit number and bit 0=word number
5-10 = Last look store function code

TSSSR—Trunk Status Store Status

Bit 0-3 = Spare image number
4 = S/F data for MASS update
5 = E/D data for MASS update
7 = MASS update mode = 1

EST LLS Memory (FLEV, Interject Reports)

ESU0 ESR1	ESU0 ESR0	ESU1 ESR1	ESU1 ESR0	ESU2 ESR1	ESU2 ESR0
ESU3 ESR1	ESU3 ESR0	ESU4 ESR1	ESU4 ESR0	ESU5 ESR1	ESU5 ESR0
ESU6 ESR1	ESU6 ESR0	ESU7 ESR1	ESU7 ESR0	ESU8 ESR1	ESU8 ESR0
ESU9 ESR1	ESU9 ESR0	ESU10 ESR1	ESU10 ESR0	ESU11 ESR1	ESU11 ESR0
ESU12 ESR1	ESU12 ESR0	ESU13 ESR1	ESU13 ESR0	ESU14 ESR1	ESU14 ESR0
ESU15 ESR1	ESU15 ESR0	CESR1	USR	UPR	UPA

Upper half (shown)—Dumped at time of interject (via active controller).

Lower half (not shown)—Same format as above dumped after clearing all errors and hit timing for 10 ms.

ESU0—15—Higher half ESR bits for ESU0 through ESU15

ESR1

Bit 0 = RCV Envelope > Threshold (suspect pack NH5 RCV)
1 = XMT signal peak (suspect pack NH5 XMT)
2 = XMT Envelope ≥ XMT data (suspect pack NH5 XMT)
3 = XMT Envelope > Threshold (suspect pack NH5 XMT)
4 = TRK Status store E/D (suspect pack NH8)
5 = TRK status store S/F (suspect pack NH8)
6 = GGC counter sync (suspect pack NH8)
7 = Echo suppressor initialize (suspect pack NH8)
8 = Good interval count initialize (suspect pack NH8)
9 = GWC counter sync (suspect pack NH7)
10 = Controller select (suspect pack NH7)
11-15 = Unused ESR bits
16-23 = (Not used—zeros)

NOTE:
ESR1 data for an unequipped ESU is octal 00064626 or 00013151, depending on ESU number.

ESU0—15—Lower half ESR bits for ESU0 through ESU15

ESR0

Bit 0 = RCV input framing (suspect pack NH2)
1 = RCV input framing (suspect pack NH2)
2 = RCV output data (suspect pack NH2)
3 = RCV output data and framing (suspect pack NH2)
4 = XMT input framing (suspect pack NH3)
5 = XMT input framing (suspect pack NH3)
6 = XMT output data (suspect pack NH3)
7 = XMT output data and framing (suspect pack NH3)
8 = RCV line driver out (suspect pack NH1)
9 = XMT line driver out (suspect pack NH1)
10 = Suppress control (suspect pack NH4)
11 = Noise control (suspect pack NH4)
12 = Compress control (suspect NH4)
13 = Tone disable control (suspect pack NH6)
14 = RCV signal peak (suspect pack NH5 RCV)
15 = RCV Envelope ≥ XMT data (suspect pack NH5 RCV)
16-23 = (not used—zeros)

NOTE:
ESR0 data for an unequipped ESU is octal 00064626 or 00113151, depending on ESU number.

CESR1—Controller Error Source Register 1

Bit 0-15 = (See CESR1 for EST Critical Registers)

USR—Unit Summary Register

Bit 0-14 = (See USR for EST Critical Registers)

UPR—Unit PEST Register

Bit 0-14 = (See UPR for EST Critical Registers)

UPA—Unit Power Alarm

Bit 0-15 = (See UPA for EST Critical Registers)

EST MA Pulse Point Reply

ES4MADATA—MA Pulse Point Reply FLEV 39, 40

Bit 0 = Maintenance access bit-set by pulse
1 = Receive on bus F/F toggled by pulse
2 = State of send on bus 0 F/F
3 = State of send on bus 1 F/F
4 = State of divorce F/F
5 = State of emergency cutoff flip-flop
6 = State of clock activity F/F
7 = State of active/standby F/F
8 = PU bus even parity failure indicator
9 = PU bus odd parity failure indicator
10 = PU bus K code match indicator
11 = PU bus M-bit indicator
12 = Receive on bus F/F complement
13 = Autonomous interrupt indicator
14 = All-seems-well interrupt indication
15 = Unassigned OPCODE failure, CESR1-UNASOP
16 = Slave timing
17 = One-out-of-one OPCODE checker error, CESR1-OPDEC
18 = When set, send-on is disabled
19 = Clock error, CESR4-16-MB
20 = Out of frame, cESR1-OOF
21 = Destination code error, CESR1-DESE
22 = Mode failure, CESR1-MODFL
23 = 17X DEST code error, CESR1-17XDSE

I/O- Input/Output Frame Printouts

I/O Status and Internal Data

Poll Failure

IO1RST IOUS	IO1RST IOMP	IO1RST IOUC	IOUS STATUS REG	ERROR SUMMARY REG

OR

Maintenance Request

IO1RST IOUS	IO1RST IOMP	IO1RST IOUC	IOUS STATUS REG	IOUC STATUS REG	SUPPLE MENTARY DATA

IO1RSTIOUS—IOUS Software Status

Bit 0 = IOUS maintenance state
1 = Receive bus for IOUS
2 = Send on bus 0
3 = Send on bus 1
4 = IOUS removed by fault recovery action
5 = Diagnostic requested for IPUB 0 but no GBT
6 = Diagnostic requested for IPUB 1 but no GBT
7 = Diagnostic requested for IOUS but no GBT
8 = IOUS removed by TTY request
12 = IOUS out of service
13 = IPUB 0 removed by TTY request
14 = IPUB 1 removed by TTY request
16 = IPUB 0 out of service
18 = IPUB 1 out of service
20-23 = PU MTCE code

IO1RSTIOMP—IOMP Software Status

Bit 4 = IOMP removed by fault recovery action
7 = Diagnostic requested for IOMP but no GBT
8 = IOMP removed by TTY request
12 = IOMP out of service
20-23 = PU MTCE code

IO1RSTIOUC—IOUC Software Status

Bit 0-2 = Character parity failure counter
3 = F-level PESTed for I/O K-code
4 = IOUC removed by fault recovery action
5-6 = Input buffer overflow counter
7 = Diagnostic requested for IOUC but no GBT
8 = IOUC removed by TTY request
9-10 = Character overrun counter
11 = Maintenance state of IOUC
12 = IOUC out of service
13-15 = Inter character time-out counter
16-17 = Timeout counter
19 = Restoral runjob requested
20-23 = PU MTCE code

IOUS Status Register (5A021)

Bit 0 = Maintenance flip-flop
1 = Receive on bus flip-flop
2 = Send on bus 0
3 = Send on bus 1

IOUS Status Register (5A052) (IOP)

Bit 0 = Maintenance flip-flop
1 = Receive on bus flip-flop
2 = Send on bus 0
3 = Send on bus 1
4 = IOMP 0 out of service
5 = IOMP 1 out of service
6 = Hold acknowledge monitor
7 = IOMP select monitor
8 = IOMP 1 hold acknowledge failure
9 = IOMP 0 hold acknowledge failure
10 = IOMP 1 data store request failure
11 = IOMP 0 data store request failure
12 = Invalid instruction received
13 = IOMP 0 invalid access (power problem)
14 = IOMP 1 invalid access (power problem)
15 = DMAC parity failure
17 = IOMP out-of-range memory address
18 = ROM parity failure
19 = DMAC sanity failure
20 = Character counter underflow
21 = Channel ID match failure
22 = PU bus parity failure over odd bits
23 = PU bus parity failure over even bits

IOUC Status Register (5A045) (IOP)

Bit 8 = Channel is out of service
9 = Channel is in idle state
10 = Channel is in end-of-message RCVD state
11 = Channel is in break received state
12 = Channel is in input state
13 = Channel is in output state
14 = Channel is in full duplex mode
15 = Channel buffer is empty
16 = Channel buffer should be loaded
17 = Channel buffer should be unloaded
18 = Channel is in transparent mode
21 = Invalid channel command received
22 = Software error detected
23 = Hardware error detected

Error Summary Register (5A021)

Bit 0 = All-seems-well failure
2 = Parity failure over even PU write bus bits
3 = Parity failure over odd PU write bus bits
5 = Multiple K-code match detected
6 = Invalid instruction detected by IOUS
19 = Channel response failure
20 = Channel buffer parity failure
21 = High-speed (7.7 µsec) clock monitor
22 = Low-speed (71.4 µsec) clock monitor
23 = Clock failure

Error Summary Register (4C049)

Bit 0 = PC Error Summary
1 = PC sanity failure
2 = PC routine maintenance failure
3 = PC clock failure
4 = PC RAM parity failure
5 = Enable gate through error
6 = Invert parity
14 = IOMP1 error summary
15 = IOMP0 error summary
16 = PC 0 error
17 = PC 1 error
18 = PC 2 error
19 = PC 3 error
20 = PC 4 error
21 = PC 5 error
22 = PC 6 error
23 = PC 7 error

Error Summary Register (5A049/5A052) (IOP)

Bit 0 = DMAC-IOMP gate through bit
1 = IOMP clock failure
2 = IOMP sanity failure
3 = Memory parity failure
4 = Memory—IOMP parity failure
5 = Routine maintenance error
6 = Force power failure
7 = LIU—IOMP parity failure
8-13 = DMAC routine maintenance failure code
14 = IOMP 1 error summary bit
15 = IOMP 0 error summary bit

IOUC Status Register (5A021)

Bit 8 = Channel buffer is empty
9 = Carrier failure alarm
10 = Low paper alarm
11 = Channel maintenance state
12 = Channel is in idle state
13 = Channel is in input state
14 = Channel is in output state
15 = Channel is in break received state
16 = Channel buffer should be loaded
17 = Channel buffer should be unloaded
18 = Start of input message
19 = Maintenance request
20 = Inhibit maintenance request
21 = Output buffer overflow
22 = Character parity failure
23 = Input buffer overflow

IOUC Status Register (5A049/5A052/4C049) (IOP)

Bit 0 = Channel is connected (4C049 only)
8 = Channel is out of service
9 = Channel is in idle state
10 = Channel is in end-of-message received state
11 = Channel is in break received state
12 = Channel is in input state
13 = Channel is in output state
14 = Channel operation is full duplex
15 = Channel buffer is empty
16 = Channel buffer should be loaded
17 = Channel buffer should be unloaded
18 = Channel is in transparent mode
21 = Invalid channel command received
22 = Software error detected
23 = Hardware error detected

Supplementary Data (Channel Status Bit-23 Set) (5A049/5A052)

Bit 12 = Intercharacter time-out (>45 seconds)
14 = Character overrun
15 = Input buffer overflow
16 = Serial parity failure
17 = MP to LU parity failure
18 = LU to MP parity failure
19 = Low paper
20 = No clear to send
21 = Carrier failure
22 = Automatic call unit failure

Supplementary Data (Channel Status Bit-23 Set) (4C049)

Bit 13 = Protocol halt
20 = Data set transmit error
21 = Data set receive error
22 = ACU error
23 = Protocol error

Supplementary Data (Channel Status Bit-23 Set) (5A049/5A052/4C049)

Bit 8-15 = High byte of failing address
16-23 = Low byte of failing address

I/O MA Pulse Point Reply (5A021)

Bit 0 = Overall (IOUS) maintenance
1 = Receive on bus 0 or 1
2 = Send on bus 0
3 = Send on bus 1
8 = Parity failure over even bits
9 = Parity failure over odd bits
10 = K-code match (any IOC K-code)
11 = Maintenance bit on PU enable address bus
12 = Specifies complement of R0 (address bus)
13 = Multiple K-code match
14 = Invalid instruction detected by IOUS

I/O MA Pulse Point Reply (5A049) (IOP)

Bit 0 = Maintenance access
1 = Receive on bus 0 or 1
2 = Send on bus 0
3 = Send on bus 1
4 = MP0 out of service
5 = MP1 out of service
6 = MP hold acknowledge
7 = MP select F/F state
8 = MP1 hold ACK error
9 = MP0 hold ACK error
10 = MP1 request DS ACK error
11 = MP0 request DS ACK error
12 = Invalid instruction
13 = MP0 invalid access error
14 = MP1 invalid access error
15 = DMAC parity failure
16 = Unassigned
17 = MPDS ADR OOR access error
18 = Micro INSTR ROM parity error
19 = DMAC sanity failure
20 = Character count underflow
21 = Channel ID match failure
22 = PU write bus parity odd
23 = PU write bus parity even

I/O Operational Failure Data

5A021 I/O FRAME:

ERROR CODE	CHAN-NEL #	IO1CHAN-STAT0	IO1CHAN-STAT1	ERROR SUM REG	IOUC STATUS REG

OR

5A052/5A089/4C049 I/O PROC FRAME:

ERROR CODE	CHAN-NEL #	IO1CHAN-SAT0	IO1CHAN-STAT1	IOUS STATUS REG	IOUC STATUS REG

Error Code (Octal)

1 Buffer empty indicator not set after 24 characters
2 Time-out (20 sec) of constant break signal
3 No service request after ACK (?T)
4 Time-out of channel
5 SR received but channel not in any state
12 CMS channel removed from service
13 Time-out of CMS channel in output state

Channel # Octal/ Decimal	Channel Name COMPOOL * Symbol 4IO—XXX	Channel # Octal/ Decimal	Channel Name COMPOOL * Symbol 4IO—XXX
0/0	MTC	26/22	Unassigned
1/1	SREC1	27/23	Unassigned
2/2	RCMOC	30/24	SREC2
3/3	BELT1	31/25	RCDT2
4/4	BELT2	32/26	RCDT3
5/5	Unassigned	33/27	TRF2
6/6	RCREC	34/28	NMDT3
7/7	RCDT1	35/29	TEC2
10/8	TRF1	36/30	TEC3
11/9	NMPR1	37/31	TEC4
12/10	NMDT1	40/32	TCA5
13/11	NMDT2	45/37	TCA2
14/12	TEC1	46/38	TCA3
15/13	CMS1	47/39	CA4
16/14	CMS2	50/40	TCA5
17/15	CMS3	51/41	TCA6
20/16	CMS4	56/46	RCRRT1
21/17	TCA1	57/47	RCRRT2
22/18	RMT1	60/48	NMPR2
23/19	SVOBS	61/49	NMNOC1
24/20	SCC1	62/50	TTS1
25/21	SCC2	63/51	TTS2

Footnote is listed at the end of table.

Channel # Octal/ Decimal	Channel Name COMPOOL * Symbol 4IO—XXX	Channel # Octal/ Decimal	Channel Name COMPOOL * Symbol 4IO—XXX
64/52	TTS3	106/70	MAC1
65/53	TTS4	107/71	MAC2
66/54	TTS5	110/72	MAC3
67/55	TTS6	111/73	PSIRAS
70/56	Unassigned	112/74	PSSPR
72/58	DUP1	113/75	PSSPR2
71/57	ISCC	114/76	NSA1
73/59	DUP2	115/77	NSA2
74/60	DUP3	116/78	RMS1
75/61	DUP4	117/79	RMS2
76/62	DUP5	120/80	RMS3
77/63	DUP6	121/81	RMS4
100/64	CMSH1	122/82	RMS5
101/65	CMSH2	123/83	RMS6
102/66	EDASH1	124/84	Reserved
103/67	EDASH2	125/85	Reserved
104/68	NSCS	130/90	Reserved
105/69	RC1A3B	131/91	Reserved

* Symbols 4IO—XXX (For example 4IO—MTC) are defined in COMPOOL IO4CATE

IO1CHANSTAT

Bit 0-4 = Channel state (octal values)
- 0 = Unequipped
- 1 = Idle
- 2 = Input
- 3 = Output
- 6 = Input started
- 7 = Waiting for ACK
- 10 = ACK loaded
- 11 = Last output
- 12 = Waiting for output idle SR
- 13 = Break ACK characters loaded
- 14 = Waiting for link reset
- 15 = Waiting for protocol handler analysis
- 16 = Waiting for input segment
- 17 = Waiting for next segment
- 20 = Tape timing
- 21 = Inquiry character sent
- 22 = Waiting for start of tape
- 30 = Dial-up channel disconnected
- 31 = Input call detected on dial-up channel
- 32 = Call placed on dial-up channel
- 36 = Waiting for ACK to CMS output
- 37 = Out of service

5 = Channel in transparent mode
6 = Temporary dial-up connection
10-11 = Secondary timing counter (paper tape)

IO1CHANSTAT (Contd)

Bit 12-14 = Time-out index (octal values)
- 2 = Input timing
- 3 = Output timing
- 4 = Break timing
- 5 = ACK timing
- 6 = Output timing after time-out characters sent
- 7 = Dial-up timing

15-23 = Time-out time (octal values)
- 0 = None
- 1 = None
- 2 = 2 minutes
- 3 = 15 seconds
- 6 = 2 minutes
- 7 = 5 seconds
- 10 = 5 seconds
- 11 = 15 seconds
- 13 = 20 seconds
- 17 = 15 seconds
- 20 = 20 seconds
- 21 = 5 seconds
- 22 = 5 seconds
- 30 = None
- 31 = 2 minutes
- 32 = 102 seconds
- 36 = 5 seconds
- 37 = None

NCLK- Network Clock Frame Printouts

NCLK Critical Registers (Via TTY Request)

A —— A	B —— B	C —— C	D —— D	E —— E	F —— F	O —— O	O —— O
G —— G	H —— H	I —— I	J —— J	K —— K	L —— L	O —— O	O —— O

A = Register 0 CHAIN 0
B = Register 1 CHAIN 0
C = Software Status CHAIN 0

D = Register 0 CHAIN 1
E = Register 1 CHAIN 1
F = Software Status CHAIN 1

G = Register 0 CHAIN 2
H = Register 1 CHAIN 2
I = Software Status CHAIN 2

J = Register 0 CHAIN 3
K = Register 1 CHAIN 3
L = Software Status CHAIN 3

NCLK Data (FLEV Interrupt Reports)

A —— A	B —— B	C —— C	D —— D	E —— E	F —— F	O —— O	O —— O
G —— G	H —— H	I —— I	J —— J	K —— K	L —— L	O —— O	O —— O
A' —— A'	B' —— B'	C' —— C'	D' —— D'	E' —— E'	F' —— F'	O —— O	O —— O
G' —— G'	H' —— H'	I' —— I'	J' —— J'	K' —— K'	L' —— L'	O —— O	O —— O

Upper Half = Data at time of interrupt
Lower Half(') = Data after recovery actions completed

A (A') = Register 0 CHAIN 0
B (B') = Register 1 CHAIN 0
C (C') = Software Status CHAIN 0

D (D') = Register 0 CHAIN 1
E (E') = Register 1 CHAIN 1
F (F') = Software Status CHAIN 1

G (G') = Register 0 CHAIN 2
H (H') = Register 1 CHAIN 2
I (I') = Software Status CHAIN 2

J (J') = Register 0 CHAIN 3
K (K') = Register 1 CHAIN 3
L (L') = Software Status CHAIN 3

Register 0 (READ0)

Bit 0 = Frame counter mismatch
1 = Counter mismatch
2-11 = Fanout level detector
12 = Autonomous output disconnect
13-22 = Output disconnect fanouts
23 = Unused

Register 1 (READ1)

Bit 0 = Master selected — OSC 0
1 = Master selected — OSC 1
2 = Master selected — OSC 2
3 = Master selected — OSC 3
4-7 = OSC error bits
- 4 = OSC level detector error
- 5 = OSC phase detector error (phase lock)
- 6 = Master OSC select level Detector error (MSL)
- 7 = Phase unlock detector error

8 = Master OSC output selected
9 = Phase lock release (meter solenoid operated)
10 = Error summary indicator
11 = Error source inhibit (overall PEST)
12 = Phase lock oven monitor
13 = Parity mismatch
14 = Translator pretest failure
15 = Decode all zeros (don’t care)
16 = Frame pulse detector
17-23 = Unused

Software Status (NC4STAT + CHAIN Number)

Bit 0 = OSC 0 is master
1 = OSC 1 is master
2 = OSC 2 is master
3 = OSC 3 is master
4 = OSC in this chain is out of service
5 = Matcher(s) in this chain is disabled
6 = Unused
7 = Diagnostic has been requested
8 = CHAIN removed by TTY request
9-11 = Unused
12 = This chain is out of service
13 = Error inhibit for this chain (PEST)
14 = Output disconnect
15-19 = Access test results:
15 = Power off this chain
16 = Write group 0 is functional
17 = CHAIN is able to send on bus 0
18 = Write group 1 is functional
19 = CHAIN is able to send on bus 1
20-23 = PU maintenance code

NOTE:

1. Register 0 and register 1 refer to READ0 and READ1 responses respectively from the NCLK hardware description.
2. CHAIN 0, 1, 2, and 3 refer to CHAIN 00, 01, 10 and 11 respectively in the NCLK hardware description. (Example: CHAIN 2 = CHAIN 10 = Bay 1, CHAIN 0)

NCLK CC Pulse Point Address Assignments

CC Pulse Point Address	IREG CHAIN	Bus	Clock
401020	READ 0	0	0
401040	READ 0	1	0
402001	READ 1	0	0
402002	READ 1	1	0
402004	READ 0	0	1
402010	READ 0	1	1
402020	READ 1	0	1
402040	READ 1	1	1
404001	READ 0	0	2
404002	READ 0	1	2
404004	READ 1	0	2
404010	READ 1	1	2
404020	READ 0	0	3
404040	READ 0	1	3
01000101	READ 1	0	3
01000102	READ 1	1	3

SCLK- System Clock Frame Printouts

SCLK Critical Registers (FLEV and BLM Reports) (Equipped With NCSU)

For SCLK:	SWSTAT	HSTATR	HESR	PEST	TODCTRA	TODCTRB
	CR0	CR1	CR2	CR3	CR4	CR5
	CR6	CR7	CR8	CR9	CR10	CR11
For NCSU:	CR12	CR13	CR14	CR15	CR16	CR17
	CR18	CR19	CR20	CR21	CR22	CR23
	UTMN*	7——7†	7——7	7——7	7——7	7——7

Upper Half = SCLK Controller 0 lower half (not shown) = SCLK controller 1

* MN only for BLM reports

† First word UT translator (UTTRANS)

SWSTAT—SCLK Software Status Register

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on bus 0
3 = Send on bus 1
4 = Divorced from mate
5 = Stop count
6 = Clamp NCSU from SCLK
7 = Diagnostic requested
8 = Restore by TTY
9 = Counter read select [1 = CTR-A (CLOCK 0)]
12 = Controller out of service
13 = Bus 0 power off
14 = Bus 1 power off
15 = Controller power off
16 = Controller cannot receive on bus 0
17 = Controller cannot send on bus 0
18 = Controller cannot receive on bus 1
19 = Controller cannot send on bus 1
20-23 = PU maintenance code

HSTATR—SCLK Hardware Status Register

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on bus 0
3 = Send on bus 1
4 = Divorced from mate
5 = Stop count
6 = Clamp NCSU from SCLK
7 = Counter read select [1 = CTR-A (CLOCK 0)]
12-19 = Write enables for bits 0-7

HESR—SCLK Hardware Error Source Register

Bit 0 = All-seems-well failure
1 = A and B counter mismatch
2 = Parity failure even
3 = Parity failure odd
4 = Invalid OPCODE
5 = Mode failure
6 = Reply register mismatch
7 = NCSU ASW failure

PEST—SCLK PEST Register

Bit 12 = PEST SCLK ASW failure
13 = PEST A and B counter match failure
14 = PEST NCSU ASW failure

TODCTRA—SCLK Time of Day Counter—A

Bit 0-3 = 0.1 seconds
4-8 = 1 second
9-14 = 0.5 minutes
15-20 = 0.5 hours
21 = Day toggle bit

TODCTRB—SCLK Time of Day Counter—B

Bit 0-21 = Same as TOD CTR-A

CR0—NCSU Software Status Register

Bit 0 = Maintenance access
1 = Receive from controller 0 or 1
2 = Send to controller 0
3 = Send to controller 1
7 = Reference active (0 = REG, 1 = ALT)
8 = Removed via TTY
9-11 = Operational mode
12 = NCSU out of service
13 = Regular reference out of service
14 = Alternate reference out of service
16 = Active outage
17 = Standby outage
20-23 = PU subunit maintenance code

Operational Mode Values (Bits 9-11)

0 = Normal mode (phase locked)
1 = Free running mode
2 = Fast start mode

CR1—NCSU Hardware Status and ESR Register

Bit 0 = Maintenance access
1 = Receive from controller 0 or 1
2 = Send to controller 0
3 = Send to controller 1
4 = Clock test when reset
5 = Parity test when reset
6 = Inhibit PROC sanity errors when reset
7-11 = Spare status bits
12 = ASW failure
13 = Clock parity error
14 = Clock error
15 = Processor match error
16 = Processor sanity
17 = Invalid OPCODE
18 = Processor trap
19 = Processor detected error (See CR19)
20-23 = Unassigned

CR2—NCSU Mode Register/Reference Register/ODA Reference

Bit 0-1 = Reason for free run
2 = Misframe threshold exceeded
3 = REF outage threshold exceeded
4 = Phase build-out threshold exceeded
5 = Free run threshold exceeded
6-7 = Operational mode (See CR0)

Reference Source Register

Bit 9-10 = Regular reference (BSRF=0, DS1A=1, DS1B=2, None =3)
11-12 = Alternate reference (BSRF=0, DS1A=1, DS1B=2, None=3)
13 = Active Reference (0 = REG, 1 = ALT)
14 = Regular reference out of service
15 = Alternate reference out of service

ODA Reference Register

Register value = 0—Unequipped, 1—Regular, 2—Alternate

18-19 = BSRF
20-21 = DS1A
22-23 = DS1B

CR3—NCSU Base ESR 0/Base ESR 0 Last Look

Base ESR 0

Bit 0 = Oscillator OOR
1 = OSC 0-0 OOR
2 = OSC 0-1 OOR
3 = OSC 1-0 OOR
4 = OSC 1-1 OOR
5 = BSRF outage
6 = DS1A outage
7 = DS1B outage

BASE ESR 0 Last Look

12-19 = Last look of bits 0-7

CR4—NCSU Secondary ESR/Base ESR 1

Secondary ESR

Bit 0 = OSC and UPROC mismatch
1 = OSC write data mismatch
2 = OSC 0 mismatch
3 = OSC 1 mismatch
4 = OSC 2 mismatch
5 = OSC 3 mismatch

Base ESR 1

Bit 12 = NCLK F-level phase
13 = Normal mode
15 = Fast start enter
16 = Dead slave complete
17 = Dead slave failed

CR5—Oscillator Words 0 and 1

Bit 0-7 = OSC word 0
8-15 = OSC word 1

CR6—Integral Register 0 (Bit 0-15)

CR7—Integral Register 1 (Bit 0-15)

CR8—Integral Register 2 (Bit 0-15)

CR9—Integral Register 3 (Bit 0-15)

CR10—Program Counter Before Reset (Bit 0-15)

CR11—Power Up Counter

Bit 0-5 = Power up count

CR12—UPROC Detected Data

Bit 0-15 = Additional UPROC detected error data (See CR19)
Equals OSC number for CR19 = 10, 12, 13, 14, 15, 36
Equals master OSC number for CR19 = 17
Equals reference register for CR19 = 33
Equals I/O port data for CR19 = 34
Equals contents of I/O (0xc10B) for CR19 = 35
Equals OPCODE for CR19 = 40

CR13—Unit Quality

Bit 0-15 = Number of UPROC detected errors in memory tables

CR14—Proportional Registers

Bit 0-7 = Proportional register 0
8-15 = Proportional register 1

CR15—REF Outage and Misframe Counters

Bit 0-7 = Reference outage counter
12-19 = Misframe counter

CR16—Free Run and Phase Build-Out Counters

Bit 0-7 = Free run counter
12-19 = Phase build-out counter

CR17—NCLK Software Status Register — CHAIN 0

Bit 0 = OSC 0 is master
1 = OSC 1 is master
2 = OSC 2 is master
3 = OSC 3 is master
4 = OSC in this CHAIN is out of service
5 = Matcher(s) in this CHAIN is disabled
6 = Unused
7 = Diagnostic has been requested
8 = CHAIN removed by TTY request
9-11 = Unused
12 = This chain is out of service
13 = Error inhibit for this CHAIN (PEST)
14-19 = Access test results
- 14 = Output disconnect
- 15 = Power off this CHAIN
- 16 = Write group 0 is functional
- 17 = CHAIN is able to send on bus 0
- 18 = Write group 1 is functional
- 19 = CHAIN is able to send on bus 1

20-23 = PU maintenance code

CR18—NCSU Miscellaneous Register

Bit 0 = Macro in progress
1 = Test state flip-flop
2 = Parity fail not (0 = parity failure)
3 = OSC 0-0 cutoff
4 = OSC 0-1 cutoff
5 = OSC 1-0 cutoff
6 = OSC 1-1 cutoff
7 = Parity test when reset

CR19—NCSU UPROC Detected Error Code

Bit 0-7 = Error code (octal value)

0 = OSC 0-0 readback mismatch
1 = OSC 0-1 readback mismatch
2 = OSC 1-0 readback mismatch
3 = OSC 1-1 readback mismatch
4 = OSC 0-0 data register mismatch
5 = OSC 0-1 data register mismatch
6 = OSC 1-0 data register mismatch
7 = OSC 1-1 data register mismatch
10 = Window size error
11 = Master switch during dead slave
12 = OSC word change GT 40 HEX
13 = OSC word change GT 100 HEX
14 = Illegal phase comparator bits
15 = Dead slave OSC cutoff
17 = Delta OSC word GT 1000 HEX (FAST), 100 HEX (NORM)
20 = Build-out error
21 = Integral term LT 800 HEX
22 = BSRF quality
23 = Integral term GT 3800 HEX
24 = Fast start GT 300 decimal
25 = Phase hit, delta phase MEAS GT 14 HEX
26 = Phase comparator OOR
27 = Phase error—slope short
30 = Phase error—slope medium
31 = Phase error—slope long
32 = Phase comparator jitter
33 = REF register bad data
34 = Master OSC I/O port invalid
35 = Master OSC cutoff
36 = Major OSC alarm
37 = Stuck ready bit (phase COMP)
40 = Routine exercise failure
41 = Minor OSC alarm
42 = OSC power failure

Bit 8-23 = (Not used—zeros)

CR20—NCSU Program Counter

Bit 0-15 = Program Counter

CR21—NCSU Lap Counter

Bit 0-15 = Number of 8-sec counts since last fast start

CR22—NCSU UPROC Program Mode

Bit 0-7 = UPROC Program states
Value 0 = Reset
1 = EXEC
2 = Fast start
3 = Normal
4 = Free run

CR23—SCLK Controller

Bit 0 = Indicates SCLK controller through which NCSU dump was obtained

UTMN—Unit Type and Member Number

Bit 0-6 = Member number
7-13 = Unit type

SCLK MA Pulse Point Reply

Bit 0 = MA F/F
1 = RO F/F
2 = SO F/F
3 = S1 F/F
4 = DIV F/F
5 = Stop F/F
8 = Parity fail, even bits
9 = Parity fail, odd bits
10 = K-code (mismatch)
11 = M-bit
12 = RO F/F COMPL
13 = ASW fail
14 = Invalid OPCODE
15 = Mode fail

UTTRANS—First Word Unit-Type Translator

Bit 0-23 = First word of Unit-Type Translator

SCS/SCU- Service Circuit System/Service Circuit Unit Printouts

Service Circuit System Critical Registers (FLEV and Interject Reports)

CSTATUS	**HWSTATR**	**MADATA**	**FSTATUS**	**SCUOS**	**CESR**
PEST	**CONTROL**	**EBLKSTATL**	**EBLKSTATH**	**EBLKADR**	**GRESR**
GRCNTRM	**GADRMO**	**GADRM1**	**EXESR**	**EXCSTATML**	**EXCSTATMH**
EXFPTR	**EXPC**	**EXSANTIM**	**EXSTKBL**	**EXSTKBH**	**EXSTRPTR**
EXINTR	**RLPBPTR**	**WLPBPTR**	**RDBPTR**	**WDBPTR**	**MBPTRS**
SDOWMBPTR	**MBSTAT**	**SCU0ESR**	**SCU1ESR**	**SCU2ESR**	**SCU3ESR**
SCU4ESR	**SCU5ESR**	**SCU6ESR**	**SCU7ESR**	**SCU8ESR**	**SCU9ESR**
SCU10ESR	**SCU11ESR**	**SCU12ESR**	**SCU13ESR**	**SCU14ESR**	**SCU15ESR**
FWERRBUF0	**FWERRBUF1**	**FWERRBUF2**	**FWERRBUF3**	**FWERRBUF4**	**FWERRBUF5**
FWERRBUF6	**FWERRBUF7**	**FWERRBUF8**	**FWERRBUF9**	**EBERRORM**	**EBLKADRM**
EBLKSTATML	**EBLKSTATMH**	**0.......0**	**0.......0**	**0.......0**	**0.......0**
MEMN	**XLATE**	**5.......5**	**5.......5**	**5.......5**	**5.......5**

Upper Half = Controller 0
Lower Half = Controller 1 (Not shown)

CSTATUS—Controller Software Status

Bit 0 = Maintenance access (MA)
1 = PU bus receive on select (RO)
2 = Send on bus 0 (S0)
3 = Send on bus 1 (S1)
4 = Divorce controller from mate (DIV)
5 = Stop autonomous processing (STOP)
6 = Divorce I/O synchronization (IODIV)
7 = Controller active/standby (AS)
8 = Emergency cutoff (EC)
12 = Controller out of service (OS)
13 = Controller removed via TTY (RMVTTY)
20-23 = Maintenance code (MAIN)
(See "Peripheral Unit—Maincodes")

HWSTATR—Controller Hardware Status

Bit 0 = Maintenance Access (MA)
1 = PU bus receive on select (RO)
2 = Send on bus 0 (S0)
3 = Send on bus 1 (S1)
4 = Divorce controller from mate (DIV)
5 = Stop autonomous processing (STOP)
6 = I/O synchronization divorce (IODIV)
7 = Controller active/standby (AS)
8 = Emergency cutoff (EC)
12 = Enable loading MA F/F (EMA)
13 = Enable loading RO F/F (ERO)
14 = Enable loading S0 F/F (ES0)
15 = Enable loading S1 F/F (ES1)
16 = Enable loading DIV F/F (EDIV)
17 = Enable loading STOP F/F (ESTOP)
18 = Enable loading IODIV F/F (EIODIV)
19 = Enable loading as F/F (EAS)
20 = Enable loading EC F/F (EEC)

MADATA—Maintenance Access Data

Bit 0 = Maintenance access (MAMA)
1 = Receive on bus 0 or 1 (MARO)
2 = Send on bus 0 (MAS0)
3 = Send on bus 1 (MAS1)
4 = Divorce controller from mate (MADIV)
5 = Stop autonomous processing (MASTOP)
6 = Cross-controller update bit in control register (MAXCUPD)
7 = Active/standby (1 = controller is active) (MAAS)
8 = Parity failure even (MAPUBFE)
9 = Parity failure odd (MAPUBFO)
10 = K-code match (MAKM)
11 = Mode bit (MAMBIT)
12 = Complement of RO (MAROC)
13 = Emergency cutoff (MAEC)
14 = Autonomous interrupt (MAAINT)
15 = ASW failure (MAASWF)
16 = Unassigned OP-CODE failure (MAUNASOP)
17 = Mode failure (MAMODFL)
18 = PUBI parity error (MAPPE)
19 = I/O synchronization divorce (MAIODIV)
20 = EXEC local error source summary (MAEXECSUM)
21 = Backplane error (MABPSUM)
22 = Local clock failure (MALCLKF)

FSTATUS—Frame Software Status

Bit 0 = PUB0 at frame removed via TTY (TTYIPUB0)
1 = PUB1 at frame removed via TTY (TTYIPUB1)
2 = PUB0 out of service at frame (OSIPUB0)
3 = PUB1 out of service at frame (OSIPUB1)
4 = Frame LAN PEST status (FLANPEST)
5 = Switch in progress (SIP)
6 = Maintenance buffer overflow task in progress (MBOVFL)
7 = Digit buffer overflow (DBOVFL)
8 = Stops file copy from APS to SCU(s) (STOPCOPY)
13 = Controller to RST when DUPF to DGN an SCU (UDGNCTRL)

SCUOS—SCU Software OS Status

Bit 0-15 = SCU0 through 15 out of service

CESR—Controller Primary ESR

Bit 0 = All seems well failure (ASWF)
1 = Autonomous interrupt (AINT)
2 = Peripheral unit bus even parity failure (PUPFE)
3 = Peripheral unit bus odd parity failure (PUPFO)
4 = Internal autonomous peripheral unit trouble - interject (INAPUT)
5 = Autonomous peripheral unit base level (APUB)
6 = Invalid/unassigned OP-CODE (UNASOP)
7 = Firmware error bit (SWERR0)
8 = Firmware error bit (SWERR1)
9 = Firmware error bit (SWERR2)
10 = Firmware error bit (SWERR3)
11 = Firmware error bit (SWERR4)
12 = Mode failure (MODFL)
13 = PUBI parity error (PPE)
15 = Local clock failure (LCLKF)
18 = Extended bus error summary (EBSUM)
19 = Global RAM local error source summary (GRAMSUM)
20 = EXEC local error source summary for bits 0-16 in the EXEC error source register (EXECSUM)
21 = Backplane error summary (BPSUM)
22 = Clock phase lock error (CPMM)
23 = Cross-controller mismatch (CCMM)

PEST—Controller PEST Register

Bit 0 = Inhibit ASWF (IASWF)
1 = Inhibit AINT (IAINT)
2 = Inhibit PUPFE (IPUPFE)
3 = Inhibit PUPFO (IPUPFO)
4 = Inhibit INAPUT (IINAPUT)
5 = Inhibit APUB (IAPUB)
6 = Inhibit UNASOP (IUNASOP)
7 = Inhibit SWERR0 (ISWERR0)
8 = Inhibit SWERR1 (ISWERR1)
9 = Inhibit SWERR2 (ISWERR2)
10 = Inhibit SWERR3 (ISWERR3)
11 = Inhibit SWERR4 (ISWERR4)
12 = Inhibit MODFL (IMODFL)
13 = Inhibit PPE (IPPE)
15 = Inhibit LCLKF (ILCLKF)
18 = Inhibit EBSUM (IEBSUM)
19 = Inhibit GRAMSUM (IGRAMSUM)
20 = Inhibit EXECSUM (IEXECSUM)
21 = Inhibit BPSUM (IBPSUM)
22 = Inhibit CPMM (ICPMM)
23 = Inhibit CCMM (ICCMM)

CONTROL—Controller Control Register

Bit 0 = High priority buffer empty (HPE) (Not used)
1 = Low priority buffer empty (LPE)
2 = Digit buffer empty (DGE)
3 = Seizure buffer empty (SZE) (Not used)
4 = Cross-controller update enable (XCUPD)
11 = Handshake between PUBI and EXEC during arbitration (EXARB)
12 = Disables ability for next write to reply register to initiate reply sequence. Cleared when reply register is written (RPLDIS)
13 = Control bit that initiates reply sequence without overwriting reply register (RPLY)
14 = Force clock error fast (FCLKERF)
15 = Force clock error slow (FCLKERS)
16 = Sets INAPUT in CESR (SINAPUT)
17 = Sets APUB in CESR (SAPUB)
18 = Sets UNASOP in CESR (SUNASOP)
19 = Software error bit (SWERR0)
20 = Software error bit (SWERR1)
21 = Software error bit (SWERR2)
22 = Software error bit (SWERR3)
23 = Software error bit (SWERR4)

EBLKSTATL—Extended Bus Link Status Register - Low

Bit 0 = Illegal command received by the SCU (ICRSCS)
1 = SCU receive link parity error (RLPARERR)
2 = SCU active link violation (ACTLINKV)
4 = SCU receive FIFO full (RFF)
5 = SCU receive FIFO half full (RFHF)
6 = SCU reply FIFO not empty (RFNE)
7 = SCU error summary bit (ERRSUM)
8 = Transmit sequencer active (TSA)
9-14 = Transmit sequencer state (TSEQS)
15 = Copies the WSRB bit in the extended bus control register when WSRB is strobed by WSR (STATLSSRB)
16 = Receive sequencer active (RSA)
17-21 = Receive sequencer state (RSEQS)
22 = Near operation complete (NOC)
23 = Operation complete sync (EBIOC)

EBLKSTATH—Extended Bus Link Status Register - High

Bit 0 = Illegal command received by the controller (ICRCNTR)
1 = Receive link violation (RLV)
2 = Copies the WSRB bit in the extended bus control register when WSRB is strobed by WSR (STATHSSRB)
3 = Destination data parity error (DDATPE)
4 = Receive parity error (RPE)
5 = Source parity error (SPE)
6 = Destination parity error (DPE)
7 = Transmit parity error (TPE)

EBLKADR—Extended Bus Link Address Register

Bit 0-4 = Link logical address (LLA)

GRESR—Global RAM Error Source Register

Bit 0-3 = RAM bank A parity error bits (ERAP)
4-7 = RAM bank B parity error bits (ERBP)
8-11 = Destination bus data parity error bits (EDDP)
13 = Source bus A address parity error (ESAAP)
14 = Source bus B address parity error (ESBAP)
15 = Cross-connect update bus mismatch (EXUMM)
16 = Cross-connect SYNDROBUS mismatch (EXSMM)

GRCNTRM—Global RAM Control Register (From Memory)

Bit 0 = Read count enable (CRCNTE0)
1 = Read count enable (CRCNTE1)
2 = Count down enable (CCNTDN0)
3 = Count down enable (CCNTDN1)
4 = Write count enable (CWCNTE0)
5 = Write count enable (CWCNTE1)
7 = Maintenance Test: Syndrome Bus Transmit Inhibit (MTSTSXI)
8 = Maintenance Test: Destination Data Enabled to Backplane (MTSTDEN)
9 = Maintenance Test: Destination Address Enabled to Backplane (MTSTAEN)
10 = Maintenance Test: Destination Data and Address Enabled to Update Bus (MTSTXEN)
11 = Maintenance Test: Destination Data Parity (MTSTP0)
12 = Maintenance Test: Destination Data Parity (MTSTP1)
13 = Maintenance Test: Destination Data Parity (MTSTP2)
14 = Maintenance Test: Destination Data Parity (MTSTP3)
15 = Maintenance Test: Destination Address Parity (MTSTP4)
16-21 = Maintenance Test: Destination Address Offset (MTSTOF)
22 = Maintenance Test: Destination Address Mode (MTSTMD0)
23 = Maintenance Test: Destination Address Mode (MTSTMD1)

GADRM0—Global Address Register 0 (From Memory)

Bit 0-19 = The base address with which the lower 6 bits are logically OR'ed with one of the offset fields from the microword (OFFSET0)

GADRM1—Global Address Register 1 (From Memory)

Bit 0-19 = The base address with which the lower 6 bits are logically OR'ed with one of the offset fields from the microword (OFFSET1)

EXESR—EXEC ESR Register

Bit 0 = EXEC stack boundry error (STKBNDERR)
1 = Sanity timer elapsed (SANITYTMR)
2 = ALU mismatch (ALUMM)
3 = Source parity error (SPERR)
5-12 = Micro RAM parity error (MPERR)
15 = Software defined error (SOFTERR)

EXCSTATML—EXEC Status Register - Low (From Memory)

Bit 0 = ALU carry bit (CARRY)
1 = ALU zero flag (ZERO)
2 = ALU sign bit (NEGATE)
3 = ALU overflow bit (OVERFLOW)
4 = ALU link flag (LINK)
5 = Test bits (EXCTEST0)
6 = Test bits (EXCTEST1)
7 = Always true condition bit (True)
8 = Force parity error source A byte 0 (FPESRCA0)
9 = Force parity error source A byte 1 (FPESRCA1)
10 = Force parity error source A byte 2 (FPESRCA2)
11 = Force parity error source A byte 3 (FPESRCA3)
12 = Force parity error source B byte 0 (FPESRCB0)
13 = Force parity error source B byte 1 (FPESRCB1)
14 = Force parity error source B byte 2 (FPESRCB2)
15 = Force parity error source B byte 3 (FPESRCB3)
16 = Force energy detector error (FEDE)
17 = Force clock timing mismatch bits (FCTMM0)
18 = Force clock timing mismatch bits (FCTMM1)
19 = Force ALU mismatch (FALUMM)
20 = Vector base bit (VBB)

EXCSTATMH—EXEC Status Register—High (From Memory)

Bit 0-7 = Interrupt vector (IVECT)

EXFPTR—EXEC Frame Pointer

Bit 0-15 = Frame address (FA)

EXPC—EXEC Program Counter

Bit 0-15 = Microword address (MWA)

EXSANTIM—EXEC Sanity Timer

Bit 0-23 = Timer count bits (TIMER)

EXSTKBL—EXEC Stack Boundry Register - Low

Bit 0-15 = Stack bounds low address (SBL)
16-23 = Lower half of the stack bounds high address (LSBH)

EXSTKBH—EXEC Stack Boundry Register - High

Bit 0-7 = Higher half of the stack bounds high address (HSBH)

EXSTKPTR—EXEC Stack Pointer

Bit 0-15 = Stack pointer address (EXSP)

EXINTR—EXEC Interrupt Register

Bit 0 = Spare external interrupt (SPARE0)
1 = PU bus operation interrupt from PUBI (PUBOINT)
2 = Spare external interrupt (SPARE2)
3 = PU bus error interrupt from PUBI (PUBEINT)
4 = Mask bit for SPARE0 (MSPARE0)
5 = Mask bit for PUBOINT (MPUBOINT)
6 = Mask bit for SPARE2 (MSPARE2)
7 = Mask bit for PUBEINT (MPUBEINT)
8 = Disable interrupt (DISINT)
9 = Active interrupt (ACTINT)

RLPBPTR—Low Priority Read Pointer

Bit 0-11 = Read pointer

WLPBPTR—Low Priority Write Pointer

Bit 0-11 = Write pointer

RDBPTR—Digit Buffer Read Pointer

Bit 0-11 = Read pointer

WDBPTR—Digit Buffer Write Pointer

Bit 0-11 = Write Pointer

MBPTRS—Maintenance Buffer Pointers

Bit 0-11 = Read pointer
12-23 = Write pointer

SDOWMBPTR—Shadow Maintenance Buffer Pointer

Bit 0-11 = Active read pointer

MBSTAT—Maintenance Buffer Status Register

Bit 0-8 = Number of reports in the maintenance buffer

SCU0ESR-SCU15ESR—SCU0-15 Primary ESR's

Bit 0 = EPIC parity error (ERER)
1 = Unused bit - Zero will be returned (SPARE1)
2 = Unused bit - Zero will be returned (SPARE2)
3 = Micro store memory parity error (MSPER)
4 = Sanity timeout error (SAN)
5 = Clock error (CLOCK)
6 = Table RAM read parity error (TRPER)
7 = Invalid link state - both extended bus links ACT/ACT or STBY/STBY (INVLS)
8 = Misc. error summary (SESRASUM)
9 = Disk error summary (SESRBSUM)
10 = LAN error (LANER)
11 = SCU disk pump failure (DL)
12 = DS120 link frame error (DS120)
16-22 = SCU error code (ERRCODE). See SCU Error Code List
23 = Summary of bits 0-15

FWERRBUF0—Firmware Detected Error Code

Bit 0-23 = Error Code (Octal)

SCC Base Level Error Codes

1 = SCC main scheduler loop error (ERSCMAIN)
2 = EXEC system call error (EROSEXEC)
3 = Signal system call error (EROSSIGNAL)
4 = Wait system call error (EROSWAIT)
5 = Diagnostic already in-progress error (ERDGINPROG)
6 = Main MTC buffer overflow (EROSMTCBUFOF)
7 = Tried to EXEC an invalid process (EROSINVPROC)
10 = Data corruption in EB process (EREBPOLL)
11 = SCC pump error (ERPMSCU)
12 = SCC pump buffer error (ERPMBUF)
13 = SCC pump CHECKSUM error (ERPMCHKSUM)
14 = SCC pump data error (ERPMDATA)
15 = SCU access test error (ERACCSCU)
16 = Verify program HASHSUM error (ERVPGHASH)
17 = ECD error (ERECD)
20 = PUMP SCU MSP error (ERMSP)
21 = SCC INIT. through update error (ERUPD)
22 = Low priority buffer overflow (EROSLPBUFOF)
23 = Digit buffer overflow (EROSDGBUFOF)
24 = SCC retrofit pump error (ERRETROPMIN)
25 = Disk file copy error (ERDFCINVLD)
26 = Error PU write file (ERINDDWRERR)
27 = Incomplete information to process command (ERINCMPLTD)
30 = Error in input data to the comand (ERRDERR)

SCC Interrupt Error Codes (Contd)

40 = Read RAM error (ERINRDRAM)
41 = Read register error (ERINRDREG)
42 = Write RAM error (ERINWRTRAM)
43 = Write 32 bit register error (ERINWRT32REG)
44 = Write 24 bit register error (ERINWRT24REG)
45 = MTC buffer overflow error (ERINMTCBUFOF)
46 = Macro process buffer overflow (ERINMCBUFOF)
47 = Group 1 macro error (ERINGRP1MAC)
50 = Group 2 macro error (ERINGRP2MAC)
51 = Read MTC buffer pointer error (ERINRMTCPTR)
52 = MTC buffer update error (ERINMTCUP)
53 = Clear buffer error (ERINCLRBUF)
54 = Write buffer write-pointer error (ERINWBUFWP)
55 = Write buffer read-pointer error (ERINWBUFRP)
56 = Pump macro process error (ERSCCPMIN)
57 = Write SCU status error (ERWSTATUS)
60 = Initialize SCU error (ERISCUERR)
61 = Clear SCU error (ERCLESR)
62 = Read SCC micro-RAM error (ERINRDSCCMRAM)
63 = In-service SCU macro error (ERINISSCUMAC)
64 = Out-of-service SCU macro error (ERINOSSCUMAC)
65 = ECD error (ERINECD)
66 = MSP error (ERINMSP)
67 = ECD macro error (ERINECDMAC)
70 = Deferred update announcement error (ERUPDAN)

SCC Interrupt Error Codes (Contd)

71 = SCC INIT. through update error (ERINSCCUPD)
72 = LP buffer underflow (ERINOSLPUF)
73 = Digit buffer underflow (ERINOSDGUF)
74 = Error reading the LP buffer read pointer (ERINRLPPTR)
75 = Error reading the digit buffer read pointer (ERINRDGPTR)
76 = SCC retrofit pump—illegal buffer error (ERRETROPMBUF)
77 = SCC invalid diagnostic test group number (ERINVDGNTGN)
100 = SCC received a DGN report when not divorced (ERDGNNOTDIV)
101 = Write SCC micro-RAM error (ERINWRTMRAM)
102 = Invalid breakpoint
110 = No SCU(s) equipped
111 = Unequipped SCU not PESTed
112 = EB polling is not running (EREBPROCSTOP)
113 = Macro process is not running (ERMCPROCSTOP)
114 = Bad current process address (ERSCPROCERR)
115 = Error in FIFO test interrupt routine (ERINFIFOTST)
116 = Bad SCU number from call processing (ERBADSCU)
117 = MIP error code (ERINMIP)
120 = EB polling process not running
121 = Macro process not running
122 = Current process address invalid
04000000 = Hardware error
10000000 = Illegal PUB order
77777777 = SCU interject

NOTE:
When an error code is present, FWERRBUF1-9 contains additional data saved at the time of the error.

FWERRBUF1—Origin of Error

If bit 9 equals 0 = Process error interrupt

Bit 8 equals 0 = Error during base level processing
then bits 0-7 = Process id number

Otherwise

Bit 8 equals 1 = Error during interrupt-level processing
then bits 0-7 = Interrupt vector

If bit 9 equals 1 = Hardware error interrupt
Bits 0-7 = Interrupt vector
Bit 12 = Previous error flag
Bit 13 = Non-recoverable error flag
Bit 14 = Process mode (0 = Normal, 1 = Diagnostic)

FWERRBUF2—Additional Data Saved at Time of Error

If FWERRBUF0 = Octal 10000000

Bits 0-23 = PU receive register low (Data 0-23)

Otherwise

Bits 0-23 = Data from PL (0-23)

FWERRBUF3—Additional Data Saved at Time of Error

If FWERRBUF0 = Octal 10000000

Bits 0-23 = PU receive register high

Otherwise

Bits 0-11 = OPAD from PU (24-35)

Bits 12-23 = KCODE from E (10-21)

NOTE:
See K-codes (E-Register Layouts)

FWERRBUF4—Additional Data Saved at Time of Error

Bit 0-15 = EXEC stack pointer (EXSTKPTR)
(Saved register - See EXSTKPTR Register Layout)

FWERRBUF5—Additional Data Saved at Time of Error

Bit 0-15 = Contents of the stack

FWERRBUF6—Additional Data Saved at Time of Error

Bit 0-15 = Frame pointer to local RAM

FWERRBUF7—Additional Data Saved at Time of Error

Bit 0-15 = EXEC program counter (EXPC)
(saved Register - See EXPC Register Layout)

FWERRBUF8—Additional Data Saved at Time of Error

Bit 0-23 = Current process table address

FWERRBUF9—Additional Data Saved at Time of Error

Bit 0-15 = SCU0-15 PEST bits

EBERRORM—Extended Bus Error Code (From Memory) - Interject Only

Bit 0-23 = Error code (octal)
- 0 = No error
- 1 = Digit buffer overflow
- 2 = Invalid message format from SCU
- 3 = Invalid number of words from SCU
- 4 = Invalid process ID from SCU
- 5 = Corrupt TEMP EB MTC buffer
- 6 = Corrupt process buffer
- 7 = EB buffer overflow
- 10 = Error shown in following EBLKSTATML or EBLKSTATMH Layouts

EBLKADRM—Extended Bus Link Address (From Memory)

Bit 0-23 = See EBLKADR Register Layout
Bit 0-23 = Octal 00177777 if EBERRORM error code equals 0 or 1 (No data saved)

EBLKSTATML—Extended Bus Link Status - Low (From Memory)

Bit 0-23 = See EBLKSTATL Register Layout
Bit 0-23 = Zero if EBERRORM error code equals 0 or 1 (No data saved)

EBLKSTATMH—Extended Bus Link Status - High (From Memory)

Bit 0-23 = See EBLKSTATH Register Layout
Bit 0-23 = Zero if EBERRORM error code equals 0 or 1 (No data saved)

MEMN—SCS Member Number

Bit 0-6 = SCS Member Number (0-7)

XLATE—First Word of SCS Unit Type Translator

Bit 0-15 = SCU0-7 SCU member equipage (two bits per SCU)
00 = Unequipped (future)
01 = Grow
10 = Special grow
11 = Operational
16-17 = Member equipage
18-20 = Member type hardware generation (MTHG)
21-23 = Member type (1=Standard Type)

Auxiliary Data- (SCS Interject Reports)

SEC1	KEY	COUNT	ESRHIGH	ESRLOW	MISCESR
DISKESR	SCUSTAT	ADR1	ADR2	ADR3	REG0
REG1	REG2	SEC2	REG3	REG4	REG5
REG6	REG7	REG8	REG9	REG10	REG11
REG12	REG13	REG14	REG15	USTATUS	SCUPESTR

NOTE:
This printout only occurs for a single SCU error, not multiple SCUs alarming. The **SCU(n)** number is printed on the action line.

SEC1—Start of Dump Section 1 (14 Words)

Bit 0-23 = 1

KEY—Error Data Key

Bit 0-23 = Error code (octal)

00000000 = No error since last SCU INIT
00012345 = ESR single error
00054321 = ESR multi-error (attempted but locked)
00037777 = ESR multi-error (unlocked)

COUNT—Error Count

Bit 0-23 = Number of failures (octal) when ESR is unlocked
= 1 if ESR is locked

ESRHIGH—SCU(n) Primary ESR High (esrh)

Bit 0 = Miscellaneous error summary (sesrasum)
1 = Disk error summary (sesrbsum)
2 = LAN error (laner)
3 = SCU disk pump failure (dl)
4 = DS120 link frame error (ds120)
5-7 = Unused bits
8-14 = SCU error code (errcode)—See SCU Error Code List
15 = Summary of bits 0-4 (ESRHIGH) and bits 0-7 (ESRLOW)
16-23 = Ignore

NOTE:
Bits 0-15 are the same as bits 8-23 in SCS Critical Register Dump for SCU(n)ESR

ESRLOW—SCU(n) Primary ESR Low (esrl)

Bit 0 = EPIC parity error (erer)
1 = Unused bit (spare 1)
2 = Unused bit (spare 2)
3 = Micro store memory parity error (msper)
4 = Sanity timeout error (san)
5 = Clock error (clock)
6 = Table RAM read parity error (trper)
7 = Invalid link state—both extended bus links ACT/ACT or STBY/STBY (invls)

NOTE:
Bits 0-7 are the same as bits 0-7 in SCS Critical Register Dump for SCU(n)ESR

MISCESR—Auxiliary ESR-Miscellaneous Errors (ERmisc)

Bit 0 = Table RAM (TN1983) error (TRAM)
1 = Micro store (TN1977) error (MS)
2 = Enhanced peripheral interface controller (TN1976) error (EPIC)
3 = Trace and control (L567460) error (unofficial LAB only pack) (TC)
4 = Buffer fabric (TN1982) error (BF)
5 = Buffer controller (TN1981) error (BC)
6 = Voice processor interface controller (TN1980) error (VPIC)
7 = Voice processor (TN1979) error (VP)
8-11 = Multifaceted signal processor (TN1589) pack 0-3 error (MISP0-3)
12-13 = Multifaceted interface processor (TN4001) pack 0-1 error (MISP0-1)
14 = DS120 interface and time slot interchange (TN1588) error (DXI)
15 = Extended bus and LAN interface (KCN4) error (EBL)

DISKESR—Auxiliary ESR-Disk Errors (ERrdisk)

Bit 0-2 = BIDO-2—SCSI bus device ID number:
0-3 = Hard disk drive 0-3
6 = Floppy disk drive
7 = Host adapter circuit pack (TN1978)
3-4 = BUS0,1—SCSI Bus 0,1 error
(bits 0-2 indicate which device on the bus had the error).
5-7 = Unused bits

NOTE:
The following bits are an image of bits 8-15 of register "esrl" which are used to control the LED error indicators on the disk drive circuit packs

8-11 = DSK00-03—Disk errors for SCSI bus 0
12-15 = DSK10-13—Disk errors for SCSI bus 1

SCUSTAT—SCU(n) Hardware Status Register (usr)

Bit 0 = SCU is in-service (SERV)
1 = Hard initialization (INIT)
2 = Run via EPROM (RUNEP)
3 = PEST for ERRSUM bit in EBLKSTAT (PSTESR)
4 = Inhibit transmit status (reply buffer look empty) (INHXSTAT)
5 = Inhibit ESR lock (IESRLK)
6 = Inhibit SCU access to LAN (ILAN)
7 = Inhibit SCU access to EB (IEXBUS)
8 = SCU file descriptor select (FILE0)
9 = SCU file descriptor select (FILE1)
10 = SCU file descriptor type (0 = DGN, 1 = OPER) (FILETY)
11 = SCSI bus select (FILESB)
12 = Enable writing of SERV (ESERV)
13 = Enable writing of INIT (EINIT)
14 = Enable writing of RUNEP (ERUNEP)
15 = Enable writing of PSTESR (EPSTESR)
16 = Enable writing of INHXSTAT (EINHXSTAT)
17 = Enable writing of IESRLK (EIESRLK)
18 = Enable writing of ILAN (EILAN)
19 = Enable writing of IEXBUS (EIEXBUS)
20 = Enable writing of FILE0 (EFILE0)
21 = Enable writing of FILE1 (EFILE1)
22 = Enable writing of FILETY (EFILETY)
23 = Enable writing of FILESB (EFILESB)

ADR1—First Program Return ADR

ADR2—Second Program Return ADR

ADR3—Third Program Return ADR

REG0-2—Processor ALU Register 0-2

SEC2—Start of Dump Section 2 (14 WORDS)

REG3-15—Processor ALU Registers 3-15

USTATUS—SCU(n) Software Status

Bit 0 = SCU is PESTed via TTY request (SCUP)
1 = Disk in use as copy destination (DISKIUCD)
2 = Disk in use as copy source (DISKIUCS)
3 = Disk in use-format in progress (DISKIUF)
4 = Announcement update in progress (ANUPDIP)
5 = Skip announcement update (SANNUPD)
6 = SCU remove pending (RMVPND)
7 = In progress activity monitior (IPAM)
9-11 = Announcement update status (ANUPDSTAT)
0 = No announcement update activity
1 = Complete
2 = In-progress
3 = Failed
4 = Stopped
12 = SCU is out-of-service (OS)
13 = SCU is removed via TTY request (RMVTTY)
18 = Pump of SCU for DGN succeed (UDGNPMPPASS)
20-23 = SCU MAINCODE (MAIN) (See Subunit-Maincodes)

SCUPESTR—SCU 0-15 PEST Register

Bits 0-15 = Hardware PEST bits for SCU 0-15

NOTE:
Bits 0-15 are the same as FWERRBUF9 (bits 0-15) in SCS Critical Register Dump.

Auxiliary Data- (SCS BLM Reports)

BSIZE	KIND	HEADER	DATA0	DATA1	DATA2
DATA3	DATA4	DATA5	DATA6	DATA7	DATA8
DATA9	DATA10	DATA11	DATA12	DATA13	DATA14
DATA15	MBPTRS*	SDMBPTR*	MBSTAT*	SOFTPST*	0...0
SCUOS*					

* Data output only when kind = 1 (Illegitimate)

BSIZE—Auxiliary Data Block Size

Bit 1-6 = Block size

KIND—Kind of Report

Bit 0 = Kind of report (0 = Autonomous, 1 = Illegitimate)

HEADER—Frame Report Header [Maintenance Buffer (MB)]

Bit 0-6 = Macro subopcode (See SCS Macro Subopcode List)
7 = Unused
8-11 = Number of words in report
12 = Segment report flag
13 = Autonomous report flag
14 = Error flag
15 = Unused
16-20 = Macro ID number (assigned by Message Dispenser)
21 = Source of report (0=CONTR, 1=SCU)

NOTE:
1. Invalid SCU order if bit 13=0, bit 14=1, and bit 21=1.
2. Autonomous SCU error if bit 13=1, bit 14=1, and bit 21=1.
3. Unexpected macro response if bit 13=0, bit 14=0, and bit 21=d.c.

DATA0-15—Frame Report Data Words (0-15)

DATA0—Second Header (If header bit 21 = 1)

Bit 0-3 = SCU number
4 = Command type
0 = In-service command
1 = Out-of-service command
5 = Error flag from header (bit 14)
0 = Report fail
1 = Report pass

DATA1—Error code (If header bit 21 = 1)

Bit 0-7 = SCU error subcode (See SCU Error Subcode List)
8-15 = SCU error code type
1 = Order error
2 = Audit error
3 = Hardware error
4 = Action reply (MISC)
5 = AAP error
6 = MIP-CDSU errors

DATA2—SCU First Return Address

DATA3—SCU Second Return Address

DATA4—SCU Third Return Address

DATA5—SCU ALU Register R0

DATA6—SCU ALU Register R1

DATA8—SCU ALU Register R2

DATA8—SCU ALU Register R3

DATA9—SCU ALU Register R4

DATA10—SCU ALU Register R11

DATA11—SCU ALU Register R12

DATA12—SCU ALU Register R13

DATA13—SCU ALU Register R14

DATA14—SCU ALU Register R15

DATA15—Unused

MBPTRS—Maintenance Buffer Pointers

Bit 0-11 = Read pointer
12-23 = Write pointer

SDMPTR—Shadow Maintenance Buffer Pointer

Bit 0-11 = Temporary read pointer

MBSTAT—Maintenance Buffer Status

Bit 0-11 = Number of reports

SOFTPST—SCU PEST Summary

Bit 0-15 = If set, SCU 0-15 errors are inhibited

SCUOS—SCU(s) Out of Service Summary

Bit 0-15 = If set, SCU 0-15 is out of service

SCU Internal Registers (via TTY Request)

USTATUS SCUESR SCUSTAT TRAN1 TRAN2 TRAN3 0.......0 0.......0

USTATUS—SCU Software Status

Bit 0 = SCU is PESTed via TTY request (SCUP)
1 = Disk in use as copy destination (DISKIUCD)
2 = Disk in use as copy source (DISKIUCS)
3 = Disk in use - format in progress (DISKIUF)
4 = Announcement update in progress (ANUPDIP)
5 = Skip announcement update (SANNUPD)
6 = SCU remove pending (RMVPND)
7 = In progress activity monitor (IPAM)
9-11 = Announcement update status (ANUPDSTAT)
- 0 = No announcement update activity
- 1 = Complete
- 2 = In-progress
- 3 = Failed
- 4 = Stopped

12 = SCU is out of service (OS)
13 = SCU is removed via TTY request (RMVTTY)
18 = Pump of SCU for DGN succeed (UDGNPMPPASS)
20-23 = SCU MAINCODE (MAIN) (Subunit—Maincodes)

SCUESR—SCU Error Source Register

Bit 0 = EPIC parity error (EPER)
3 = Micro store memory parity error (MSPER)
4 = Sanity timeout error (SAN)
5 = Clock error (CLOCK)
6 = Table RAM read parity error (TRPER)
7 = Invalid link state - both extended bus links ACT/ACT or STBY/STBY (INVLS)
8 = MISC. error summary (SESRASUM)
9 = Disk error summary (SESRBSUM)
10 = LAN error (LANER)
11 = SCU disk pump failure (DL)
12 = DS120 link frame error (DS120)
16-22 = SCU error code (See SCU Error Code List)
23 = Summary of bits 0-15

SCUSTAT—SCU Hardware Status Register

Bit 0 = SCU is in-service (SERV)
1 = Hard initialization (INIT)
2 = Run via EPROM (RUNEP)
3 = PEST for ERRSUM bit in EBLKSTAT (PSTESR)
4 = Inhibit transmit status (reply buffer look empty) (INHXSTAT)
5 = Inhibit ESR lock (IESRLK)
6 = Inhibit SCU access to LAN (ILAN)
7 = Inhibit SCU access to EB (IEXBUS)
8 = SCU file descriptor select (FILE0)
9 = SCU file descriptor select (FILE1)
10 = SCU file descriptor type (0=DGN, 1=OPER) (FILETY)
11 = SCSI bus select (FILESB)
12 = Enable writing of SERV (ESERV)
13 = Enable writing of INIT (EINIT)
14 = Enable writing of RUNEP (ERUNEP)
15 = Enable writing of PSTESR (EPSTESR)
16 = Enable writing of INHXSTAT (EINHXSTAT)
17 = Enable writing of IESRLK (EIESRLK)
18 = Enable writing of ILAN (EILAN)
19 = Enable writing of IEXBUS (EIEXBUS)
20 = Enable writing of FILE0 (EFILE0)
21 = Enable writing of FILE1 (EFILE1)
22 = Enable writing of FILETY (EFILETY)
23 = Enable writing of FILESB (EFILESB)

TRAN1—SCU Translation Data Word 1

Bit 0-3 = TSI Port number connected to SCU
4 = TSI SPC number connected to SCU
5-9 = TSI MEMN connected to SCU
19-20 = SCU software version
21-23 = Type of service circuit

TRAN2—SCU Translation Data Word 2

Bit 0-11 = DSP0-5 software version (2 bits per DSP)
12-23 = DSP0-5 equipage bits (2 bits per DSP)

TRAN3—SCU Translation Data Word 3

Bit 0-7 = DISK0-3 capacity indicator (2 bits per disk)
8-15 = DISK0-3 equipage bits (2 bits per disk)
16-23 LAN address

SCS Macro Subopcode List (Octal)

See Auxiliary Data—(SCS BLM Reports).
If header bits 0-6 are not zero, an unexpected macro response has occurred.

See the following tables.

SCS Controller Macros (Header bit 21=0):

Macro Subopcode Header (Bits 0-6)	Macro Description
001	Dump all SCS controller breakpoints macro
002	Initialize SCU(s) macro
003	Inter-SCU raw disk copy macro (Word 0)
004	Inter-SCU raw disk copy macro (Word 1)
005	Inter-SCU disk file copy macro (Word 0)
006	Inter-SCU disk file copy macro (Word 1)
007	Read SCC ROM version marco
010	Initialize CDSUS macro
011	Pump SCU MIPS macro
012	Update DS120 port tables
013	SCS controller initialization through update bus macro
014	SCU equipment configurations initialization macro
015	Pump SCU MSPS macro
016	Check deferred announcement update macro
017	SCS controller generic update initialization marco
020	Hard SCS controller initialization macro
022	SCS controller disk pump
023	SCS generic retrofit pump
024	EB/LAN FIFO test
025	SCS controller diagnostic
026	SCS macro task abort
027	SCS verify program HASHSUM
030	Clear all SCU primary ESRS
031	Write all SCU status registers
032	Write all SCU status registers enable
033	SCU access test
034	Write controller file to disk
035	Write low controller 16-bit address
036	Write high controller 16-bit address
037	File write bit map

SCU Macros (Header bit 21=1) :

Macro Subopcode Header (Bits 0-6)	Macro Description
001	Read RAM (Length)
002	Read RAM (16-Bit address)
003	Read announcement busy/idle status
004	Read DS120 port status
005	SCU loop
006	Start SCU task
007	Stop SCU task macro
010	Set SCU fast breakpoint
011	Set normal breakpoint
012	Set custom breakpoint (Micro-program address)
013	Set Custom breakpoint (Length)
014	Set custom breakpoint (Direct memory address)
015	Set custom breakpoint (Indirect memory address)
016	Set custom breakpoint (Indirect register address)
017	Clear one breakpoint for the SCU
020	Clear all breakpoints for the SCU
021	Dump all breakpoints for the SCU
022	Clear SCU error register (MISCERRREG and DISKERRREG)
030	Read SCU Raw data from disk
031	Read SCU file from disk
032	Read low 16-bit address

SCU Macros (Header Bit 21=1) (Contd) :

Macro Subopcode Header (Bits 0-6)	Macro Description
033	Read high 16-bit address
034	Read SCU micro-program word
035	Read SCU raw error data
036	Read SCU register
037	Read SCU program version
040	Flush SCU queues
042	Copy SCU disk file
044	Write SCU sub-block data
045	Write SCU 16-bit data word
046	Write last SCU 16-bit data word in sub-block
047	PEST SCU error reports
050	UnPEST SCU error reports
051	Read SCU error report PESTs
101	Copy SCU raw disk
103	Format SCU disk
104	SCU diagnostic
106	Write SCU raw data to disk
110	Write SCU register
111	Write SCU memory (Table RAM only)
114	Write SCU 16-bit address
116	Write SCU micro-program word
117	Write SCU micro-program data
124	Convert SCU database
127	Deferred SCU announcement update

SCU Error Code List (Octal/Hex)

See Auxiliary Data—(SCS Interject Reports),
SCS Critical Registers FLEV and Interject Reports—(SCU0ESR-SCU15ESR)
SCU Internal Registers (via TTY Request)—(SCUESR).

Octal/Hex

20/0x10	Host Adapter Circuit Pack Selection Failure, Side Select Error Interrupt
21/0x11	Queue Does Not Have Sufficient Space
22/0x12	Base Cycle (BAse) or Signal Proocessing (SPx) Phase Timeout Error
23/0x13	Disk Format Error
24/0x14	Disk 0 Not Equipped
25/0x15	Announcement Table Merge Error
26/0x16	Disk Link Vector Size Problem
27/0x017	No Free Space on Disk
30/0x018	Segment Out-of-Range
31/0x019	LAN Initialization Failure
32/0x01a	Record Error Recovery Failure, Restore SCU
33/0x01b	LAN Software Driver Problem in Deferred Announcement Update
34/0x01c	Time-Out Error in Deferred Announcement Update
35/0x01d	Event Error in Deferred Announcement update
36/0x01e	Error in Loading Txmt Buffer Descriptor
37/0x01f	Error in setting SCB and CP
40/0x020	"OPEN" Detected on LAN Cable
41/0x021	"SHORT" Detected on LAN Cable
42/0x022	LAN Overrun (rcv-dma)
43/0x023	LAN Transmit/Receive Queue Error
44/0x024	EBL Parity Error when Reading Input FIFO
45/0x025	Poll Time-Out from AAP
46/0x026	Default Error for SCU Program Download (Download did not finish within allocated time)

Octal/Hex

47/0x027	ECD Parameter Mismatch with Value Read from the Disk
50/0x028	Tone File Error
51/0x29	Error in hair-pin table
52/0x2a	Record Problems, check fail address from 4ESS interject raw data to determine error. SCU will need to be restore
53/0x2b	AXsbt process failure, (block read-write, file read-write, raw read-write, MSP download failure, etc.)
55/0x2d	Mirrored disk data structure audit failure (data mismatch between disks)
56/0x2e	Cache Memory announcement too long to be converted to an eighth-second format
57/0x2f	Announcement Cache Memory format conversion error
140/0x60	General MIP Errors
141/0x61	MIP Transmit FIFO Error
142/0x62	MIP Receive FIFO Error
143/0x63	MIP Equipage Error
144/0x64	CDSU Equipage Error
145/0x65	General Interject Type Error Message Received From CDSU

NOTE:
See *Service Circuit System (SCS)—Maintenance* TOP (234-151-077AC) to Analyze CDSU-Related BLM and Interject Error Codes

146/0x66	MIP Disk Job Error
147/0x67	MIP Miscellaneous Data Error

Octal/Hex	
150/0x68	MIP Load Check Sum Error
151/0x69	MIP or CDSU Reply Fail
152/0x6a	ASR Miscellaneous Errors
thru	
157/0x6f	ASR miscellaneous errors
160/0x70	LAN error on MIP-0
161/0x71	LAN error on MIP-1
162/0x72	LAN error on CDSU-0
163/0x73	LAN error on CDSU-1
164/0x74	LAN error on CDSU-2
165/0x75	LAN error on CDSU-3
166/0x76	LAN error on CDSU-4
167/0x77	No ping received from a CDSU
170/0x78	T1 error on MIP-0
171/0x79	T1 error on MIP-1
172/0x7a	T1 error on CDSU-0
173/0x7b	T1 error on CDSU-1
174/0x7c	T1 error on CDSU-2
175/0x7d	T1 error on CDSU-3
176/0x7e	T1 error on CDSU-4

Disk Copy (COPYX) Errors

Octal/Hex

60/0x30	ECD_SETUP
61/0x31	ECD_WRITEFLAG
62/0x32	ECD_ANN
63/0x33	ECD_EXPAND
64/0x34	ECD_CRITICAL
65/0x35	ECD_CHUNK
66/0x36	ECD_CLUSTER
67/0x37	ECD_RDSTART
70/0x38	ECD_RDEND
71/0x39	ECD_WRSTART
72/0x3a	ECD_WREND
73/0x3b	ECD_2SUB
74/0x3c	ECD_RD
75/0x3d	ECD_WR
76/0x3e	ECD_ECD
77/0x3f	ECD_AXDATJOB
100/0x40	ECD_STATEFLAG
101/0x41	ECF_CKSUM
102/0x42	ECF_FILE

SCU Error Subcode List (Octal)

See Auxiliary Data—(SCS BLM Reports)

Order Errors (DATA1 Bits 8-15 = 1)

1	Invalid Input Order or Cannot Perform the Request
2	Input Order Data Range Check
3	Input Order out of Sequence
4	Disk File Does not Exist (Size = 0)
5	Disk File Access Crosses Block Boundary
6	File Section not on Floppy Disk
7	Request below Range of the Floppy Disk File Section
10	Request above Range of the Floppy Disk File Section
11	Disk Copy Source File > Destination File
12	ECD Parameter Problem
13	Channel Hardware is already Busy
14	Playback Concatenation Limit (32) Exceeded
15	Too many disk Write-Read Jobs Pending (> 8)

Audit Errors (DATA1 Bits 8-15 = 2)

1	SCSI Bus Error Counter—Audit Failure
2	Announcement Compare—Audit Failure
3	Playback Channel—Audit Failure
4	Record Channel—Audit Failure

Hardware Errors (DATA1 Bits 8-15 = 3)

1	Disk Data Job Error
2	MSP Sanity Failure
3	MSP Equipage Failure

Action Reply—Miscellaneous (DATA1 Bits 8-15 = 4)

1	Miscellaneous Data Error
2	Check Sum Error
3	AXsbt Data Job Time-Out
4	"WAIT" Time-Out Occurred
5	Base Level Cycle Error
6	Base Level Cycle (BAse) Phase Error or Signal Processing (SPx) Phase Error
7	Miscellaneous Data Error in Record Process
10	Data Job Failure in Record Process
11	Signal Processing Error
12	"WAIT" Event Error Occurred

This group represents errors that occur when an AAP order is received/executed.

AAP Order (DATA1 Bits 8-15 = 5)

1	Another Order is in Progress
2	Process ID Mismatch
3	Bad Announcement Status
4	Illegal Order Sequence
5	Error in Moving Data from LAN RAM to TR
6	Error in Returning Frame Structures to RFA
7	Error in Loading Txmt Buffer Descriptor
10	Error in Setting SCB and CP
11	Error in Reading or Writing the Disk
12	Disk Offset Table not Initialized
13	Illegal Announcement Length (< 4 Blocks)
14	Error in Linking through Vector Table
15	Transmit (to AAP) Timed Out
16	Illegal Order from AAP
17	Order Data Range Order
20	File not found on Disk (Size = 0)
21	No Poll Request Received from AAP
22	Math Error, Overflow, Divide by Zero, etc.
23	Error in the LAN Co-Processor
24	Header Data Mismatch (for example; announcement number)
25	Data Check-Sum Error
26	Disk State Flag Error
27	Invalid Announcement Number
30	Miscellaneous Data Error

AAP Order (DATA1 Bits 8-15 = 5) (Contd):

31 Error Loading FS Parameters
32 Error Loading DLVT Parameters
33 Error Loading Version Parameters
34 Error Loading Status Parameters
35 SCSI ID Out of Range
36 Disk not Equipped
37 Not Enough Space on the Disk
40 Error during ANN Data Transfer to/from Disk
41 Poll from AAP has Timed Out
42 Error in Addressing List of Free CLUMPS in DLVT
43 Clean-up of at and DLVT Failed
44 Disk for AM Announcement not Zero
45 Not Enough Space in AM RAM for Announcement
46 Internal Assignment Mismatch
47 External Assignment Mismatch
50 LAN XMIT Hardware Error
51 LAN COP Ran out of Resources
52 CRC Error Threshold Exceeded
53 Packet Alignment Threshold Exceeded
54 Announcement Compare Mismatch
55 LAN RCV Hardware Error
56 Announcement Set Error for Assign

MIP-CDSU Errors (DATA1 Bits 8-15 = 6)

1 Invalid Message Received from a CDSU
2 General BLM Type Error Message Received from a CDSU

NOTE:
See *Service Circuit System (SCS)—Maintenance* TOP (234-151-077AC) to Analyze CDSU-Related BLM and Interject Error Codes

3 No Setup Order was Received Before a Speech Recognition Collect Order
4 No CDSU or MIP is Equipped to Process the Requested Order
5 CDSU Channel Number is not Within Range

Restore SCS Fail Data (Via TTY Message)

FAILDATA is printed to identify the reason an SCS failed to restore. The format is as follows:

RST SCS FAILDATA=[*dde***0000***f* or **04***gggggg***]**

Where: *dd* = Failure Code (Octal)
- 01 = Program update failed during controller restore
- 02 = Random access memory (RAM) update failed during controller restore
- 03 = Verify HASHSUM failed during controller restore
- 05 = Controller hard INIT failed
- 22 = SCU INIT failed
- 23 = SCU equipment configuration data (ECD) failed
- 24 = SCU multifaceted signal processor (MSP) failed
- 25 = SCU MIP marco failed
- 26 = SCU CDSU marco failed

e = Unit/macro failure code (Octal):
- 0 = Macro failed. (f contains marco failure data)
- 4 = Macro successful but unit reported failure. (f always 0)

Continued on next page

Where: *f* = Message dispenser (macro) failure data:

0 = Invalid macro ID passed to message dispenser (program error)
1 = Macro not accepted by frame (all 1's response not received from frame
2 = Macro response not received in time allowed [Peripheral Maintenance Operating System (PMOS) task hold timeout]
3 = Macro response not received in time allowed (marco response not ready)
4 = Message dispenser request was successful but a task hold was not requested (program error)

04 = Errors occurred after RAM update
gggggg = Global RAM error source register, GRESR (Octal):

Bit 0-3 = RAM Bank A parity error bits (ERAP)
4-7 = RAM Bank B parity error bits (ERBP)
8-11 = Destination bus data parity error bits (EDDP)
13 = Source Bus A address parity error (ESAAP)
14 = Source Bus B address parity error (ESBAP)
15 = Cross-connect update bus mismatch (EXUMM)
16 = Cross-connect SYNDROBUS mismatch (EXSMM)
17 = Always 1. Indicates macro success but unit reported failure.

PUPHDATA- SCS (PHASE 2, 3, OR 4)

NOTE:
TTY request: **OP:ERAPDATA PUPHDATA:MFNUM** *a***!**

a = MFNUM or range of MFNUM for Phase 2, 3, or 4

WORD 0 WORD 1 WORD 2 WORD 3 WORD 4 WORD 5 WORD 6 WORD 7

WORDS 0-3 = Controller 0
WORDS 4-7 = Controller 1

WORD 0,4

Bit 0-2 = Boot task ACK code

0 = A boot task has been spawned
1 = A spawned task did not complete
2 = Controllers booted duplex
3 = One controller removed
4 = Both controllers failed
5 = Request error
6 = No boot task requested
7 = PMOS returned fail

Bit 3-5 = Request code

0 = Do not boot frame
1 = Hard controller boot (HDWRLEV 3 or 4)
2 = Soft controller boot (HDWRLEV 1)
3 = Soft controller boot (HDWRLEV 2)
4 = Remove controller

Bit 6-9 = Request data code (octal)

0 = Frame unequipped
1 = Frame in growth state
2 = Controller in zap table
3 = Controller in zero start table
4 = Controller in babbling bus table
5 = Controller is out of service
6 = Controller boot level is HDWRLEV 3 or 4
7 = Controller normal

Bit 10 = Final configuration request
(0 = Controller removed, 1 = Controller restored)
Bit 11-16 = Failing data code (octal)

0 = All tests pass or controller already removed prior to phase
1 = Main COMM pulse on bus failure
2 = PU bus loop failure
3 = IPUB out-of-service failure
4 = Topic - restore failure
5 = Post restore access test failure
6 = PMOS - failed to schedule "Restore"
7 = PMOS - failed to schedule "Remove"
10 = Frame rejected macro
11 = PMOS - failed to schedule "Parallel Polling"
12 = Parallel polling timeout
13 = Frame failed macro
14 = Error while polling macro
15 = Controller had less good SCUs than mate
16-77 = Unused

Bit 17-22 = SCS Unit Type (Octal 50)

WORD 1,5

SCU INIT Macro Results

Bit 0-15 = SCU 0-15 pass/fail bits
0 = Fail (or unequipped)
1 = Pass
16 = Unused
17-23 = SCS member number

WORDS 2,6

Bit 0-4 = Failed macro ID code (octal)
0 = Unused
1 = SCU initialize macro
2 = Controller disk pump macro
3 = Controller update macro
4 = Controller verify HASHSUM macro
5 = SCU access test macro (hard boot)
6 = SCU ECD macro
7 = SCU MSP macro
10 = Controller hard initialize macro (soft boot)
11 = SCU access test macro (soft boot)
12 = Controller hard initialize macro (hard boot)
13 = Update DS120 port table macro
14 = SCU MIP pump macro
15 = SCU CDSU initialize marco

5 = SCU pump code
0 = This controller was not pumped from SCU disk (if duplex, this controller was updated from mate)
1 = This controller was pumped from SCU disk (using first SCU to pass SCU initialize macro - see word 1,5)

WORDS 3,8 Not Used

SP- Signal Processor Frame Printouts

SP Internal Registers (FLEV Report)

ESR2	ESR2	WPEST	WPEST	MAR	MAR
MDR	MDR	CDR	CDR	MXAR	MXAR
MXWR	MXWR	MXHR	MXHR	MFWR	MFWR
DPWR	DPWR	DPWAUX	DPWAUX	TBSR	TBSR
PLSR	PLSR	EDST	EDST	EDSTM	EDSTM
SDST	SDST	AP33	AP33	SDSTM	SDSTM
MMST	MMST	MMSTM	MMSTM	MSEC	MSEC
XMC	XMC	PSTAT	PSTAT	FHPB	FHPB
FSZB	FSZB	FLPB	FLPB	FDGB	FDGB
FDPI	FDPI	FDPO	FDPO	MALLO	MALLO
MALLZ	MALLZ	MZOZ	MZOZ	MOZO	MOZO
MEMZ	MEMZ	MEMO	MEMO	SPECT	SPECT
SVMEMA	SVMEMA	SVMEND	SVMEND	ESR3	ESR3
DTARA	DTARA	DTARB	DTARB	DTDOPA	DTDOPA
DTOPB	DTOPB	DTBST	DTBST	DTCNT	DTCNT
DTSQFF	DTSQFF	DTSANT	DTSANT	DTRCVL	DTRCVL
DTRCVU	DTRCVU				
CONTR 0	CONTR 1	CONTR 0	CONTR 1	CONTR 0	CONTR 1

NOTE:
Prefix all words with SP4.

ESR2—Error Source Register 2

Bit 0 = The PU sequencer has failed to complete a preceding PU instruction
1 = Spare F/F
2 = Matrix work register mismatch
3 = Spare F/F
4 = An ASW failure has been detected in the matrix
5 = A homogeneity failure has been detected in the matrix
6 = Matrix hold registers mismatch
7 = Matrix hold register mismatches with matrix work register

WPEST—Write PEST Register Port D0

Bit 12 = PEST error source register 1 bits 4, 8 (not applicable to SP2)
13 = PEST error source register 1 bits 2, 3, 6, 10-19, 21 (not applicable to SP2) and error source register 3 bits 2, 3 for SP2
14 = PEST error source register 2 bits 2, 4-7 (not applicable to SP2)
15 = PESTs error source register 1 bit 5
16 = PESTs error source register 1 bit 7
17 = PESTs SP2 interface error source register 3 bits 1, 2, 4-9
18 = PESTs SP2 interface error source register 3 bit 0
19-22 = Spare FFs
23 = When set, this controller receives and writes into its memory all data written into the mate controller’s memory

MAR—Memory Address Register

Bit 0-11 = Contents of memory address register

MDR—Memory Data Register

Bit 0-23 = Contents of memory data register

CDR—Coder Register

Bit 0-11 = Complete contents of coder register

MXAR—Matrix Address Register

Bit 0-8 = Contents of matrix address register

MXWR—Matrix Work Register

Bit 10-15 = MF tone point digit from MFWR
or
Bit 0-3 = Matrix homogeneity bits read from SP with work register
4-7 = Matrix ASW bits read from SP with work register
8-15 = Lower half of MX work register bits 0-7 of SD read
16-23 = Upper half of MX work register bits 8-15 of SD read

MXHR—Matrix Hold Register

Bit 0 = Matrix row homogeneity row—bits reset when a row is enabled
1 = Matrix row homogeneity row—bits set when a row is enabled
2 = Matrix row homogeneity row—bits set when a row enabled
3 = Matrix row homogeneity row—bits set when a row is enabled
4-7 = Matrix ASW for row bits 0-3, 4-7, 8-11, and 12-15. Set when row is enabled
8-23 = Contents of matrix hold register scan or SD data from matrix or contents of matrix work register SD write data to matrix

MFWR—MF Work Register Port D1

Bit 0-4 = MF work list entry timer
5-8 = MF work list entry digit four
9-12 = MF work list entry digit three
13-16 = MF work list entry digit two
17-20 = MF work list entry digit one
21 = MF transmitter tone points status U = 0 down, U = 1 up
22 = MF outpulsing rate R = 0 = 7 PPS 70 ms, R = 1 = 10 PPS 55 ms
23 = Last digit indicator L = 1 = last digit

DPWR—Dial Pulse Work Register

Bit 0-11 = Trunk distributor tag or trunk distributor address for this entry
12-15 = Digit or remaining pulses of digit being outpulsed
16-21 = Pulse and interdigit timer
22 = SD point status U = 0 = on-hook or SD = 0 U = 1 = off-hook or SD set
23 = Last digit indicator L = 1 = last digit

DPWAUX—Dial Pulse Work Register

Bit 12-15 = Digit or remaining pulses of digit being outpulsed
16-21 = Pulse and interdigit timer
22 = SD PT status 0 = on-hook 1 = off-hook
23 = Last digit indicator 1 = LDI

TBSR—T-Bit Shift Register

Bit 0-5 = Bit 0 of T1 through T6 shift register
6-11 = Bit 1 of T1 through T6 shift register
12-17 = Bit 2 of T1 through T6 shift register
18-23 = Bit 3 of T1 through T6 shift register

PLSR—Present Look Register

Bit 8-23 = Contents of present look register
or
Bit 8 = MF reception signal present point
10-15 = MF reception tone points

EDST—Executive and DP Output Sequencer

Bit 0 = Executive sequence state 0 flip-flop
1 = Executive sequence state flip-flop
2 = Executive sequence hold flip-flop
3 = Executive sequence call flip-flop
4 = 5-ms flip-flop
5 = 5-mS AUX flip-flop
6 = When set, MF sequence returned-UNIV cycle
7 = When set, MF sequence returned-MISC cycle
8 = When set, scan sequence returned-UNIV cycle
9 = When set, scan sequence returned-MISC cycle
10 = When set, DP out sequence returned
11 = Sanity timer counter 3
12 = Sanity timer counter 2
13 = Sanity timer counter 1
14 = SERR flip-flop
15-18 = DP out sequence state flip-flops
19 = When set, DP sequence returns to EXEC
20 = When set, DP sequence calls matrix sequence for 1 bit SD write
21 = When set, executive sequence match leads to mate are high all state F/F are 0 read only
23 = When set, DP sequence is stopped by DP auxiliary stop. Read only

EDSTM—Executive and DP Output Sequencer Data as Modified by Fault Recognition

Same layout as EDST

SDST—Scan and Digit Reception Sequencer

Bit 0 = Scan read request to matrix sequence
1 = When set, inhibit buffer full leads
2 = When set, ZT23 F/F forces T-bits T2, T3, to zero
3 = When set, REX F/F returns control to executive sequencer
4-8 = Digit reception state F/F
9 = When set, dial pulse work list full
10 = When set, IAUX indicates coder = 2
11 = When set, MUD F/F indicates update of memory T-BITS
12 = When set, carry over F/F bridges states 6 and 7
13 = When set, INS inhibits T-BIT shift
14 = When set, up F/F indicates update of T-BIT shift registers
15 = T-BIT update auxiliary F/F
16 = When set, the universal scan field is accessed
17 = Inhibit work flip-flop
18 = Dial pulse work list AUX. F/F read only
19-20 = T-BIT update counter
21 = When set, holds decision to modify T4T5 T-BITS on return to ST7 from work state which could overwrite DPWR
22 = When set, INSA keeps INS reset
23 = Digit reception AUX. stop, read only

AP33—Additional Scan Sequencer F/F

Bit 0 = Inhibit DP in mode when set

SDSTM—Scan and Digit Reception Sequencer Data as Modified by Fault Recognition

Same layout as SDST

MMST—Matrix and MF Out Sequencers

Bit 0-3 = These bits define the matrix point within the row. Read access only
4-6 = Matrix state F/F GDFFD, E, F
7-9 = Matrix function F/F’s GDFFA, B, C
10 = Matrix sequence stop flip-flop, BOGO, read only
11-14 = MF sequence state F/F’s
15 = Read only—MF sequence stop F/F write only—set matrix call F/F (AUX)
16 = When set, matrix sequencer does a memory operation rather than a matrix operation
19 = Homogeneity for matrix cutoff "A" leads to mate. When reset, both address cutoff "a" and data cutoff "a" are set "a 1" if either is reset
20 = Homogeneity for matrix cutoff "B" leads to mate. When reset, both address cutoff "B" and data cutoff "B" are set "A 1" if either is reset
21 = Matrix return F/F
22 = Matrix inhibit gate in F/F
23 = MF translator match 0 is match error. Read only

MMSTM—Matrix and MF Out Sequencer Data as Modified by Fault Recognition for Restarting SP Controllers

Same layout as MMST

MSEC—Millisecond Clock

Bit 0-14 = Contents of millisecond clock register
15 = Level detector test in progress, read only access, write access is via SP4CLDW
16 = Analog timer test in progress, read only access, write access is via SP4CATW

XMC—Extended Millisecond Clock

Bit 0-6 = Contents of extended MS clock counter state(s)
- 0-7 = Unassigned
- 8 = Clock has elapsed 80-msec state(s)
- 9-31 = Unassigned
- 32 = Clock has elapsed 320-msec state(s)
- 33-127 = Unassigned

7-10 = Indicates the clock phase inhibited count 0 or 15—no phase inhibited, count 1—OOTO2 inhibited. Count 14—13TOO inhibited—read only, write via SP4CEDD
11 = When set, all phases inhibited—read only write via SP4CEDD

PSTAT—Pointer Full—Empty Status Register

Bit 0 = High priority (HP) buffer full (0 = full, 1 = not full)
1 = High priority (HP) buffer empty (0 = empty, 1 = not empty)
2 = Low priority (LP) buffer full (0 = full, 1 = not full)
3 = Low priority (LP) buffer empty (0 = empty, 1 = not empty)
4 = Digit (DG) buffer full (0 = full, 1 = not full)
5 = Digit (DG) buffer empty (0 = empty, 1 = not empty)
6 = Seizure (SZ) buffer full (0 = full, 1 = not full)
7 = Seizure (SZ) buffer empty (0 = empty, 1 = not empty)
8 = Dial pulse input work list full
9 = Dial pulse input work list empty
10 = Dial pulse output work list full
11 = Dial pulse output work list empty

FHPB—High Priority Buffer Pointer R-W

Bit 0-6 = Read pointer
9-10 = Grounded returns as ones
12-18 = Write pointer
21-22 = Grounded returns as ones

FSZB—Seizure Buffer R-W Same Layout as FHPB

FLPB—Low Priority Buffer Pointer R-W

Same layout as FHPB

FDGB—Digit Buffer Pointer R-W

Same layout as FHPB

FDPI—DIal Pulse in Work List Pointer R-W

Same layout as FHPB

FDPO—Dial Pulse Out Work List Pointer R-W

Same layout as FHPB

MALLO—CO/1 All One Memory Word Parameter

MALLZ—CO/1 All Zero Memory Word Parameter

MZOZ—CO/1 Alternating Zero—One Memory Parameter

MOZO—CO/1 Alternating One—Zero Memory Parameter

MEMZ—CO/1 SP Member Identity Word One. If this SP has member number 0-23, the corresponding bit at address SP4MEMZ in SP memory will be set to one

MEMO—CO/1 SP Member Number Identify Word Zero. If this SP has member number 0-23, this corresponding bit at address SP4MEMZ in SP memory will be set to one

SPECT—(Not used)

SVMEMA—SP Fault Recognition Uses this Storage to Save the Address of memory modified in controller 0/1

SVMEMD—SP Fault Recognition Uses this Storage to Save the Data of Memory Modified in Controller 0/1

ESR3—Error Source Register 3

Bit 0 = Transmitter in trouble
1 = Invalid DT OPCODE
2 = Mismatch between message sequences
3 = Mismatch between I/O sequences
4 = DT CLK bit error
5 = Frame timing error
6 = DT sanity check
7 = Reclock register serial mismatch
8 = Shift register mismatch
9 = Incoming serial bit stream parity error
10 = Invalid I/O sequence call state
15-18 = The DT port number calculated by the DT and sent to the SP2 during testing
23 = When set, indicates that no data and/or no timing was received by the SP2 from the DT during link testing

DTARA—DT Address Register A

Bit 0-9 = Maintenance read address, maintenance write address
10-11 = These bits are set to 1

DTARB—DT Address Register B

Same layout as DTARA

DTDOPA—Shift Register Data, OPCODE and Parity A

Bit 0-15 = Shift register data
16-20 = DT OPCODE
22 = Parity bit

DTDOPB—Shift Register Data, OPCODE And Parity B

Same layout as DTDOPA

DTBST—Temporary Buffer Status for All DT's

Bit 0-15 = Indicates the temporary buffer register for a particular DT/DTS is filled. This field can only be written to all ones or zeros FA655
16 = TBR, IMADBF, BG10, is set when the SP2 receives an idle message from the DT FA655
17 = TBR, IMADBF, AG10 is set when the destination buffer is full—FA655

DTCNT—Bit and DT Count

Bit 0-10 = 11-Bit counter FA650
11-14 = DT counter FA654
15 = GDFF, Data, when set, reclocks DT data bits FA650
16 = GDFF, match, when set, matches outgoing DT data with the mate FA650
17 = When set, GDFF, APG generates an address for parity A FA650
18 = When set, GDFF, APB generates an address for parity B FA650
19 = Incoming DT message parity will set GDFF, IPC FA650

DTSQFF—Sequencer State and MISC F/F

Bit 0-2 = Message and data storage sequence state flops GDFF. STBO, GDFF. STB1, GDFF. STB2, FA652
3 = GDFF. FRSYNC is set when a DT frame pulse is received FA652
4 = When set, TBR. GOIBL, B1 enables the message and storage sequence FA652
5 = TBR. GOIBL is set when a DT destined message exists to be sent FA652
6 = GDFF. STT is toggled when the message and data storage sequence passes through state ST05 when the I/O sequence is in DT PST04 and DT PST05 or when the message and storage sequence pass through ST02, ST05, and ST07 and I/O sequence is in DT PST09 FA652
7-10 = I/O sequence state flops FA654, GDFF. STBO, GDFF. STB1, GDFF. STB2, GDFF. STB3
11 = TBR . ITOG . BO, when set, prevents the FA654 GDFF. DTB counter from changing state by inhibiting the toggle FA654
12 = TBR. ITOG. AO, when set, allows TBR. ITOG. BO to function once FA654
13-15 = State of the counter which determines what DT receives echo suppression DGFF. DTCBO, GDFF. DTCB1, DGFF. DTCB2, FA656
16 = TBR. ESDT. BG10, when set, restores the FA650 11-bit counter FA656
17 = TBR. ESDT. AG10, when set, indicates that ESD timing is being used FA656
18 = TBR. SVLD. B1, when set, indicates the mate controller is also capable of sending a SVLD priming signal to DT FA656
19 = TBR. SVLD. A1, when set, generates the timing required to gate out MSVLD FA656
20 = TBR. clock generates a stretched clock pulse from 4T6 to 5T7 FA653
21 = Monitor point for DTSTOP (read only)
22 = Monitor point for DMASTOP (read only)

DTSANT—Sanity Timer Check Flip-Flops

Bit 0 = When set by SP2 CLK 1T3, GDFF.BTBO awaits reset by DT CLK FA657

1 = When set, GDFF.BTBO did not receive DT CLK reset before SP2 CLK OT2 FA657

2 = GDFF.F32B is set when the DT frame has occurred and the low ordered bits of the 11-bit counter fail to equal 32 FA657

3 = GDFF.MFR is set when the low ordered bits of the 11-bit counter equal 32 and the DT frame is not present FA657

4 = TBR.CT015 is set if DT count = 0 and SP2 clock = 7T9 and PSEQ = State 10. Reset occurs at 7-ms mark of the base cycle FA657

5 = TBR. CTSB is set when a serial bit transmit mismatch occurs FA657

6 = Accesses TBR.MOVINGO, when set by the matrix sequence a DT interrupt request is accepted. Frame control passes to the message sequence. TBR.MOVINGO is reset when the message sequence enters state 4 or 0 (FA657)

DTRCVL—DT Port Routing—Lower

Port values are: 00 = Derouted, 01 = Routed to controller 0, 10 = Routed to controller 1, 11 = Invalid state

Bit 0-1 = Port 0
2-3 = Port 1
4-5 = Port 2
6-7 = Port 3
8-9 = Port 4
10-11 = Port 5
12-13 = Port 6
14-15 = Port 7
20 = Send on link zero
21 = Send on link one
22 = ERTOK

DTRCVU—DT Port Routing—Upper

Port Values are: 00 = Derouted, 01 = Routed to controller 0, 10 = Routed to controller 1, 11 = Invalid state

Bit 0-1 = Port 8
2-3 = Port 9
4-5 = Port 10
6-7 = Port 11
8-9 = Port 12
10-11 = Port 13
12-13 = Port 14
14-15 = Port 15
20 = Send on link zero
21 = Send on link one
22 = ERTOK

SP Status, Error Summary and MA Data

SP4STAT—Software Status

Bit 0 = Maintenance access bit
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
5 = Stop autonomous operation
6 = Indicates clock source that this controller operates from
7 = Diagnostic has been requested
8 = Controller to be restored only by TTY
12 = Controller out of service
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on bus 0
17 = Controller cannot send on bus 0
18 = Controller cannot receive on bus 1
19 = Controller cannot send on bus 1
20-23 = PU maintenance code

SP4STAT—Hardware Status

Bit 0 = Maintenance access bit
1 = Receive on (PU bus 0 or 1)
2 = Send on bus 0
3 = Send on bus 1
4 = Divorce controller from mate
5 = Stop autonomous operation
6 = Active—indicates which controller's clock supplies basic clock to this controller
7 = Matrix address cutoff A
8 = Matrix address cutoff B
9 = Matrix data cutoff B
10 = Send memory update data to mate
11 = Matrix data cutoff A
12 = Maintenance access enable bit
13 = PU bus to receive on enable bit
14 = Send on PU bus 0 enable bit
15 = Send on PU bus 1 enable bit
16 = Divorce enable bit
17 = Stop enable bit
19 = Matrix address cutoff A enable bit
20 = Matrix address cutoff B enable bit
21 = Matrix data cutoff B enable
22 = Memory update send enable bit
23 = Matrix data cutoff A enable

SP4ESR1—Error Source Register 1

Bit 0 = An error has occurred in this controller while executing a peripheral order
1 = An error has occurred in this controller while not executing a peripheral order
2 = There was a parity error over the even bits of the PU bus on a preceding PU order
3 = There was a parity error over the odd bits of the PU bus on a preceding PU order
4 = An interject request has been sent to the CC over APUT of the control bus for the digit buffer is full
5 = A gross clock failure has occurred or the controller has been stopped too long and the analog timer has timed out
6 = There is a mismatch between matrix address registers
7 = Mismatch between PU reply bus registers
8 = Dial pulse work list full CC has tried to add too many entries
9 = **SP2** DT message lost **SP2**
10 = Sequencer states mismatch
11 = Memory registers address and or data mismatch
12 = Controller has received an invalid OPCODE
13 = A clock phase has been lost or improper clock voltage has been detected
14 = Parity over the first group of memory address and data bits has failed

SP4ESR1—Error Source Register 1 (Contd)

Bit 15 = Parity over the second group of memory address and data bits has failed
16 = Set when coder scan address exceeds scan address of contents of DP work register
17 = A sequencer has entered an invalid state
18 = Executive sequencer has lost sanity
19 = Extended millisecond clock has an error
20 = Clock ring counters not synced
21 = Dial pulse in work list flag missing

SP4CPR—MA Error Summary

Bit 0 = Maintenance access bit set by pulse
1 = Receive on bus flip-flop toggled by pulse
2 = State of send on bus zero flip-flop
3 = State of send on bus one flip-flop
4 = State of divorce flip-flop
5 = State of stop flip-flop
6 = State of clock activity
7 = Matrix data cutoff A
8 = Peripheral bus even parity failure
9 = Peripheral bus odd parity failure
10 = Peripheral bus K code match indication
11 = Peripheral bus M-bit indication
12 = Receive on bus flip-flop complement
13 = Autonomous interrupt indication
14 = All-seems-well interrupt indication
15 = An invalid OPCODE has been detected
16 = Peripheral sequencer has timed out
17 = Matrix cutoff A set
18 = Matrix cutoff B set
19 = Level detector clock error or phase detector clock error
20 = Matrix data cutoff B
21 = MS clock error
22 = Peripheral order translator parity error odd
23 = Peripheral order translator parity error even

TMS- Time Multiplexed Switch Frame Printouts

TMS Critical Registers (FLEV Reports)

TG4STAT	TG4STRD	TG4ESR+0	TG4ESR+1	00000000	00000000
MEMN	UTTRANS	55555555	55555555	55555555	55555555
TG4STAT	TG4STRD	TG4ESR+0	TG4ESR+1	00000000	00000000

Upper half controller 0

Lower half controller 1

TG4STAT—Software Status

Bit 0 = Maintenance access bit
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
5 = Stop autonomous operation
7 = Diagnostic has been requested
8 = Controller to be restored only by TTY
12 = Controller out of service
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Power off controller
16 = Controller cannot receive on PU bus 0
17 = Controller cannot send on PU bus 0
18 = Controller cannot receive on PU bus 1
19 = Controller cannot send on PU bus 1
20-23 = PU maintenance code

TG4STRD—Hardware Status

Bit 0 = Maintenance access bit
1 = Receive on (PU bus 0 or 1)
2 = Send on bus 0
3 = Send on bus 1
4 = Divorce controller from mate
5 = Stop autonomous operation
6 = Inhibit busy/idle bit checks
7 = Inhibit data matching on writes
8 = Inhibit interrupts
9 = Unit is synced with TDS subsystem
10 = Soft stop autonomous operation
11 = Inhibit gating to memory registers
12 = Allow self-start
13 = Soft stop at phase 6
14 = Force zeros across matcher interface
15 = Force ones across matcher interface

TG4ESRO—Error Source Register 0

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = Parity failure even (PUB)
3 = Parity failure odd (PUB)
4 = Mode failure
5 = Order sequencer sequence check
6 = Memory address failure
7 = Time slot memory parity failure
8 = Audit error
9 = Time slot address mismatch
10 = Memory write mismatch
11 = Order sequencer abort check
12-19 = Memory address written on first write of connects and disconnects (small office). Determine by P26P25P24P10P14-P11
20-23 = Data written to memory on first write. Determine by F2X1X0P17

TG4ESR1—Error Source Register 1 (AINT Sources)

Bit 0 = Clock error (internal)
1 = Time slot counter sequence check
2 = Time slot counter mismatch
3 = Clock mismatch
4 = Time slot memory parity failure
6 = Link of memory that failed
7-13 = Time slot memory that failed
14 = Overflow-multiple interrupts have occurred
15-21 = Time slot during which failure occurred

MEMN—Member Number

Bit 0-6 = TMS member number

UTTRANS—First Word Unit-Type Translator

Bit 0-23 = First word of Unit-Type Translator

TMS MA Pulse Point Reply

Bit 0 = MA F/F
1 = RO F/F
2 = SO F/F
3 = S1 F/F
4 = Divorce F/F
5 = Stop F/F
7 = Clock error
8 = Even bits parity failure
9 = Odd bits parity failure
10 = K-Code match (1=match)
11 = M Bit
12 = RO F/F complemented
13 = Clock input check (0=failure)
14 = Order sequencer ignore signal
15 = Order sequencer abandon signal
16 = Order sequencer mode failure signal
17 = Out-of-service sequence check
18 = Out-of-service abort check

Auxiliary Data- (TMS MEMPF)

DUMP SIZE/TYPE	SOFTWARE STATUS C0	SOFTWARE STATUS C1	HARDWARE STATUS C0	HARDWARE STATUS C1	UTYPE TRANS
ASW ESR C0	ASW ESR C1	AINT ESR C0	AINT ESR C1	0......0	0......0
K-CODE	TSM	0......0	0......0 CONTR	SUSPECT	0......0
NETWORK STATUS	TIME SLOT	MEMORY READ C0	MEMORY READ C1	RETRY PASS/FAIL FLAGS	MEMORY CORRECTION FLAG

Dump Size (Word 0)

Bits 0-23 value = octal 00003060

Bit 0 = TAG (0)
1-8 = Dump size (24 decimal)
9-12 = Dump type (MEMPF=3)

SOFTWARE STATUS—Controller 0 or 1 (Words 1, 2)

Bit 0 = Maintenance access bit
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
5 = Stop autonomous operation
7 = Diagnostic has been requested
8 = Controller to be restored only by TTY
12 = Controller out of service
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Power off controller
16 = Controller cannot receive on PU bus 0
17 = Controller cannot send on PU bus 0
18 = Controller cannot receive on PU bus 1
19 = Controller cannot send on PU bus 1
20-23 = PU maintenance code

HARDWARE STATUS—Controller 0 or 1 (Words 3, 4)

Bit 0 = Maintenance access bit
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce controller from mate
5 = Stop autonomous operation
6 = Inhibit busy/idle bit checks
7 = Inhibit data matching on writes
8 = Inhibit interrupts
9 = Unit is synced with TDS subsystem
10 = Soft stop autonomous operation
11 = Inhibit gating to memory registers
12 = Allow self-start
13 = Soft stop at phase 6
14 = Forces zeros across matcher interface
15 = forces ones across matcher interface

UTYPE TRANS—Unit-Type Translator (Word 5)

Bit 0-23 = First word of Unit-Type Translator for failing TSI

ASW ESR—Controller 0 or 1 (Words 6, 7)

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = Parity failure even (PUB)
3 = Parity failure odd (PUB)
4 = Mode failure
5 = Order sequencer sequence check
6 = Memory address failure
7 = Time slot address mismatch
8 = Audit error
9 = Time slot address mismatch
10 = Memory write mismatch
11 = Order sequencer abort check

AINT ESR—Controller 0 or 1 (Words 8, 9)

Bit 0 = Clock error (Internal)
1 = Time slot counter sequence check
2 = Time slot counter mismatch
3 = Clock mismatch
4 = Time slot memory parity failure
6 = Link of memory that failed
7-13 = Time slot memory that failed
14 = Overflow-multiple interrupts have occurred
15-21 = Time slot during which failure occurred

K-Code (Word 12)

Bit 0-6 = Member number
7-11 = Unit type (TMS=4)

TSM (Word 13)

Bit 0-6 = Time slot memory

Suspect CONTR (Word 16)

Bit 0-1 = 0 — Controller 0
1 — Controller 1
2 — Both controllers

Network Status (Word 18)

Bit 0-1 = 0 — Duplex failure
1 — Controller 0 only
2 — Controller 1 only
3 — Duplex operation

Time Slot (Word 19)

Bit 0-6 = Time slot

MEMORY READ—Controller 0 or 1 (Words 20, 21)

0-11 = Odd TSM
Bit 0-3 = Data (even side)
4 = Busy/idle bit
5 = Parity bit
6-9 = Data (odd side)
10 = Busy/idle bit
11 = Parity bit
12-23 = Same format as bits 0-11 but represents even TSM

Retry Pass/Fail Flags (Word 22)

Bit 0-1 = 0 — Both controllers passed retry
1 — Controller 0 only failed retry
2 — Controller 1 only failed retry
3 — Both controllers failed retry

Memory Correction Flag (Word 23)

Bit 0-1 = 0 — No correction attempted
1 — Correction attempted
2 — Update via mate controller

TSI- Time Slot Interchange Frame Printouts

TSI-1 Critical Registers- J4A001A (Vintage and Near-Term TSI)

SOFTWARE STATUS	HARDWARE STATUS	ASW ESR	AINT ESR	S&L ESR	MISC1 ESR
TSMP	0....0	TTSMP	0....0	MISC2 ESR	0....0
BMAPF	0....0	BMBPF	0....0	0....0	0....0
TRPF	0....0	TSW	0....0	RSW	0....0
RMM	0....0	TMM	0....0	0....0	0....0
RMT0	RMT1	RMT2	RMT3	RMT4	0....0
TMT0	TMT1	TMT2	TMT3	TMT4	0....0
SPC0 PEST	SPC1 PEST	0....0	0....0	SOFTWARE PEST	0....0
TSIMN	UTTRANS	5....5	5....5	5....5	5....5

Upper half controller 0
Lower half controller 1 (Not shown)

TSI-2 Critical Registers- J4A001B (Cost Reduced TSI - CRTSI)

SOFTWARE STATUS	HARDWARE STATUS	ASW ESR	AINT ESR	S&L ESR	MISC1 ESR
RTSMP0	RTSMP1	TTSMP0	TTSMP1	BIMPF0	BIMPF1
BMAPF0	BMAPF1	BMBPF0	BMBPF1	BMA_CALC	0....0
TRPF0	TRPF1	TSW0	TSW1	RSW0	RSW1
RMM0	RMM1	TMM0	TMM1	0....0	0....0
S&L0	S&L1	S&L2	S&L3	FLYW	0....0
0....0	0....0	0....0	0....0	0....0	0....0
SPC0 PEST	SPC1 PEST	SPC2 PEST	SPC3 PEST	SOFTWARE PEST0	SOFTWARE PEST1
TSI MN	UTTRANS	5....5	5....5	5....5	5....5

Upper half controller 0
Lower half controller 1 (Not shown)

SOFTWARE STATUS — (TSI-1 Word 0, TSI-2 Word 0)

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce cross-coupled data from mate
5 = Stop controller autonomous operation
6 = Indicates active controller number
7 = Diagnostic of this controller requested
8 = Remove via TTY
9 = Indicates which TSI half sends to TMS network 0
10 = Indicates which TSI half sends to TMS network 1
11 = Indicates from which TMS network this TSI half receives
12 = Controller out of service
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on PU bus 0
17 = Controller cannot send on PU bus 0
18 = Controller cannot receive on PU bus 1
19 = Controller cannot send on PU bus 1
20-23 = PU maintenance code

Hardware Status (TSI-1 Word 1)

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce cross-coupled data from mate
5 = Stop autonomous operation
6 = Active controller number
7 = Update mode
8 = PEST inhibit interrupts
9 = Indicates which TSI bay sends to TMS network 0
10 = Indicates which TSI bay sends to TMS network 1
11 = Indicates from which TMS network this TSI bay receives
12-13 = FIS0,FIS1—Enables bits 19-22 and selects master, secondary, or TACC fan-in packs for diagnostics (normally = 00)
14 = FS—Forces zeros or ones across matchers when bit 15 = 1
15 = FE—Force enable for bit 14
16 = Loop around
17 = PTS—BMA in maintenance mode
18 = SSFE—Serial switch force enable
19 = HFIS—When bits 12-13 are not 00 selects fan-in from SPC 0 or 1
20-22 = BIS0, BIS1, BIS2—Enables 1 of 8 branches of the fan-in packs selected by bits 12-13, 19
23 = Not used

Hardware Status Register (TSI-2 Word 1)

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on (PU bus 0)
3 = Send on (PU bus 1)
4 = Divorce cross-coupled data from mate
5 = Stop autonomous action
6 = Active unit
7 = Update mode
8 = PEST inhibit interrupts
9 = Indicates which TSI half sends to TMS network 0
10 = Indicates which TSI half sends to TMS network 1
11 = Indicates from which TMS network this TSI half receives
12 = Diagnose internal read access
13 = Buffer memory C maintenance mode
14 = FS—forces zeros or ones across matcher when bit 15 = 1
15 = FE—force enable for bit 14
16 = Loop around
17 = PTS—Places BMAs in maintenance mode
18 = Diagnose SPC select
19 = Not used
20 = Diagnose matcher (data and address)
21 = Buffer memory B maintenance mode
22 = Enable all levels on memory writes
23 = Not used

ASWESR (TSI-1 Word 2, TSI-2 Word 2)

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = PUB parity failure even bits
3 = PUB parity failure odd bits
4 = Mode failure
5 = Receive time slot memory audit failure
6 = Transmit time slot memory audit failure
7 = Busy/idle memory audit failure
8 = Receive time slot memory parity failure
9 = Transmit time slot memory parity failure
10 = Busy/idle memory parity failure
11 = Address mismatch
12 = Data write mismatch
13 = Busy/idle memory write mismatch

AINTESR—(TSI-1 Word 3, TSI-2 Word 3)

Bit 0 = Clock error (internal)
1 = Time slot counter sequence check
*2 = Time slot counter mismatch
3 = Clock mismatch
(TSI-2—Twisted ring counter mismatch)
4 = Receive time slot memory parity failure
5 = Transmit time slot memory parity failure
6 = Busy/idle memory parity failure
7 = Buffer memory A parity failure
8 = Buffer memory B parity failure
10 = Leading one DET parity failure
11 = Transmitter seems well failure
12 = Receiver seems well failure
13 = Receive mismatch
14 = Transmit mismatch
*15 = STAR seems well failure
17-23 = Time slot during which failure occurred-Phase A

* Not used in TSI-2.

S&LESR—(TSI-1 Word 4, TSI-2 Word 4)

Bit 1 = Time slot counter sequence check
4 = RTSM parity failure
5 = TTSM parity failure
6 = BIMM parity failure
7 = BMA parity failure
8 = BMB parity failure
10 = Transmission parity failure
11 = Transmitter seems well failure
12 = Receiver seems well failure
13 = Receive mismatch
14 = Transmit mismatch

MISC1ESR—(TSI-1 Word 5)

Bit 0 = Ring counter out-of-phase clock error
1 = Frame missing clock error
2 = Time slot counter parity check
3 = Time slot counter framing check
4 = Time slot counter mismatch Phase B
5 = Time slot counter mismatch Phase E
6 = B/I memory parity failure SPC0
7 = B/I memory parity failure SPC1
8 = Sample of receive errors
9 = Primary sense and lock

MISC1ESR—(TSI-2 Word 5)

Bit 0 = Out of frame
1 = Framing pulse missing
2 = Time slot counter sequence check
3 = Time slot counter parity
4 = Controller 0 unique error summary
5 = Controller 1 unique error summary
6 = Controller 0 RMM error summary
7 = Controller 1 RMM error summary
8 = Inhibit read seems well

RTSMP—(TSI-1 Word 6, TSI-2 Words 6, 7)

Bit 0-7 = Receive time slot memory P.F. SPC0 or 2
8-15 = Receive time slot memory P.F. SPC1 or 3

TTSMP—(TSI-1 Word 8, TSI-2 Words 8, 9)

Bit 0-7 = Transmit time slot memory P.F. SPC0 or 2
8-15 = Transmit time slot memory P.F. SPC1 or 3

MISC2ESR—(TSI-1 Word 10)

Bit 0 = Ring counter out-of-phase clock error
1 = Frame missing clock error
2 = Time slot counter parity check
3 = Time slot counter framing check
4 = Time slot counter mismatch phase B
5 = Time slot counter mismatch phase E
6 = B/I memory parity failure SPC0
7 = B/I memory parity failure SPC1
8 = Sample of receive errors
9 = Primary sense and lock

BIMPF—(TSI-2 Words 10, 11)

Bit 0 = B/I memory parity failure SPC0 or 2
8 = B/I memory parity failure SPC1 or 3

BMAPF—(TSI-1 Word 12, TSI-2 Words 12, 13)

Bit 0-7 = Buffer memory ‘‘A’’ P.F. SPC0 or 2
8-15 = Buffer memory ‘‘A’’ P.F. SPC1 or 3

BMBPF—(TSI-1 Word 14, TSI-2 Words 14, 15)

Bit 0-7 = Buffer memory ‘‘B’’ P.F. SPC0 or 2
8-15 = Buffer memory ‘‘B’’ P.F. SPC1 or 3

BMA_CALC—Buffer Memory Calculate

Bit 0-2 = Level
12 = Indicates SPC number
13 = If set to 0 indicates even number TSI
If set to 1 indicates odd number TSI

TRPF—(TSI-1 Word 18, TSI-2 Words 18, 19)

Bit 0-7 = Leading one DET parity failure SPC0 or 2
8-15 = Leading one DET parity failure SPC1 or 3

TSW—(TSI-1 Word 20, TSI-2 Words 20, 21)

Bit 0-6 = Transmitter seems well failure SPC0 or 2
8-14 = Transmitter seems well failure SPC1 or 3

RSW—(TSI-1 Word 22, TSI-2 Words 22, 23)

Bit 0-6 = Receiver seems well failure SPC0 or 2
8-14 = Receiver seems well failure SPC1 or 3

RMM—(TSI-1 Word 24)

Bit 0-4 = Receiver mismatch SPC0
8-12 = Receiver mismatch SPC1

RMM—(TSI-2 Words 24, 25)

Bit 0-7 = Receiver mismatch SPC0 or 2
8-15 = Receiver mismatch SPC1 or 3

TMM—(TSI-1 Word 26)

Bit 0-4 = Transmitter mismatch SPC0
8-12 = Transmitter mismatch SPC1

TMM—(TSI-2 Words 26, 27)

Bit 0-7 = Transmitter mismatch SPC0 or 2
8-15 = Transmitter mismatch SPC1 or 3

RMT0—24 (TSI-1 Words 30-34)

Bit 0-7 = Receiver mismatch level SPC0
12-19 = Receiver mismatch level SPC1

S&L 0-3—(TSI-2 Words 30-33)

Bit 1 = Time slot counter sequence CK error sense and lock
4 = RTSM parity failure sense and lock
5 = TTSM parity failure sense and lock
6 = BIMM parity failure sense and lock
7 = BMA parity failure sense and lock
8 = BMB parity failure sense and lock
10 = Leading one DET PAR. failure sense and lock
11 = Transmitter seems well error sense and lock
12 = Receiver seems well error sense and lock
13 = Receive mismatch error sense and lock
14 = Transmit mismatch error sense and lock

FLYW—(TSI-2 Word 34)

Bit 0-6 = 8-ms stuffing counter SPC0
12-18 = 8-ms stuffing counter SPC1

TMT0-4—(TSI-1 Words 36-40)

Bit 0-7 = Transmitter mismatch level SPC0
12-19 = Transmitter mismatch level SPC1

SPC PEST—(TSI-1 Words 42-43, TSI-2 Words 42-45)

BIT 0-7 = Port PEST

SOFTWARE PEST—(TSI-1 Word 46, TSI-2 Words 46-47)

Bit 0-6 = Port PEST SPC0 or 2
7-14 = Port PEST SPC1 or 3

TSIMN—(TSI-1 Word 48, TSI-2 Word 48)

Bit 10-16 = TSI member number (octal)

UTTRANS—(TSI-1 Word 49, TSI-2 Word 49)

Bit 0-23 = First word of Unit-Type Translator

TSI MA Pulse Point Reply

Bit 0 = MA F/F
1 = RO F/F
2 = SO F/F
3 = S1 F/F
4 = Divorce F/F
5 = Stop F/F
6 = Active unit F/F
*7 = Clock error
8 = Even bits parity failure
9 = Odd bits parity failure
10 = K-code match error
11 = M-bit
12 = RO F/F complemented
*13 = Clock input check (1=failure)
14 = 1=order sequence hung or running
*15 = B/I matcher match point
16 = Enable bay (controller) 0 to TMS
17 = Enable bay (controller) 1 to TMS (for bits 16 and 17, pulsing the 0 half gives the configuration to net 0, pulsing the 1 half gives the configuration to net 1)
18 = Sum of NOOPS
19 = Mode error
*20 = Unique error bay 0
*21 = Unique error bay 1
*22 = Configuration control flip-flop for Controller 0
*23 = Configuration control flip-flop for Controller 1

*TSI-2—Not assigned—returned as ones

Auxiliary Data- (TSI MEMPF)

DUMP SIZE/TYPE	SOFTWARE STATUS C0	SOFTWARE STATUS C1	HARDWARE STATUS C0	HARDWARE STATUS C1	UTYPE TRANS
ASW ESR C0	ASW ESR C1	AINT ESR C0	AINT ESR C1	SAL ESR C0	SAL ESR C1
K-CODE	LEVEL	SEC ESR EVEN	SEC ESR ODD	SUSPECT CONTR	0......0
ERROR	TIME SLOT	MEMORY READ C0	MEMORY READ C1	RETRY PASS/FAIL	MEMORY CORRECTION FLAGS

DUMP SIZE (Word 0)

Bits 0-23 value = octal 00002060

Bit 0 = TAG (0)
1-8 = Dump size (24 decimal)
9-12 = Dump type (MEMPF=2)

SOFTWARE STATUS—Controller 0 or 1 (Words 1, 2)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce cross-coupled data from mate
5 = Stop controller autonomous operation
6 = Indicates active controller
7 = Diagnostic of this controller requested
8 = Remove via TTY
9 = Indicates which TSI half sends to TMS Network 0
10 = Indicates which TSI half sends to TMS Network 1
11 = Indicates from which TMS network this TSI half receives
12 = Controller OS
13 = Bus access Circuit 0 power off
14 = Bus access Circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on PU Bus 0
17 = Controller cannot send on PU Bus 0
18 = Controller cannot receive on PU Bus 1
19 = Controller cannot send on PU Bus 1
20-23 = PU maintenance code

HARDWARE STATUS—Controller 0 or 1 (TSI-1 J4A001A)
(Words 3, 4)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce
5 = Stop autonomous operation
6 = Active unit
7 = Update mode
8 = PEST—inhibit interrupts
9 = Indicates which TSI half sends to TMS Network 0
10 = Indicates which TSI half sends to TMS Network 1
11 = Indicates from which TMS network this TSI half receives
12-13 = FIS0, FIS1—enables bits 19-22 and selects master, secondary, or TACC FAN-IN packs for diagnostics (Normally = 00)
14 = FS — Forces zeros or ones across matchers when bit 15 = 1
15 = FE—force enable for bit 14
16 = Loop around
17 = PTS—Places BMAs in maintenance mode
18 = SSFE—Serial switch force enable
19 = HFIS—When bits 12-13 are not 00, selects FAN-IN from SPC 0 or 1
20-22 = BIS0, BIS1, BIS2—Enables 1 of 8 branches of the FAN-IN packs selected by bits 12-13, 19
23 = Not used

HARDWARE STATUS—Controller 0 or 1 (TSI-2 J4A001B) (Words 3, 4)

Bit 0-11 = Same as TSI-1
12 = Diagnose internal read access
13 = BMC maintenance mode
14-17 = Same as for TSI-1
18 = Diagnose SPC select
19 = Not used
20 = Diagnose matcher enable
21 = BMB maintenance mode
22 = Enable all levels on memory writes
23 = Not used

UTYPE TRANS—Unit Type Translator (Word 5)

Bit 0-23 = First word of Unit-Type Translator for failing TSI

ASW ESR—Controller 0 or 1 (Words 6, 7)

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = PUB parity failure even bits
3 = PUB parity failure odd bits
4 = Mode failure
5 = Receive time slot memory audit failure
6 = Transmit time slot memory audit failure
7 = Busy/idle memory audit failure
8 = Receive time slot memory parity failure
9 = Transmit time slot memory parity failure
10 = Busy/idle memory parity failure
11 = Address mismatch
12 = Data write mismatch
13 = Busy/idle memory write mismatch

AINT ESR—Controller 0 or 1 (Words 8, 9)

Bit 0 = Clock error (internal)
1 = Time slot counter sequence checK
2 = Time slot counter mismatch
3 = Clock mismatch (TSI-2—twisted ring counter mismatch)
4 = Receive time slot memory parity failure
5 = Transmit time slot memory parity failure
6 = Busy/idle memory parity failure
7 = Buffer memory A parity failure
8 = Buffer memory B parity failure
10 = Leading one DET parity failure
11 = Transmitter seems well failure
12 = Receiver seems well failure
13 = Receive mismatch
14 = Transmit mismatch
*15 = Star seems well failure
17-23 = Time slot during which failure occurred—Phase A

* Not used in TSI-2.

SAL ESR—Controller 0 or 1 (Words 10, 11)

Bit 0 = Clock error (internal)
1 = Time slot counter sequence check
2 = Time slot counter mismatch
3 = Clock mismatch (TSI-2—twisted ring counter mismatch)
4 = Receive time slot memory parity failure
5 = Transmit time slot memory parity failure
6 = Busy/idle memory parity failure
7 = Buffer Memory A parity failure
8 = Buffer Memory B parity failure
10 = Leading one DET parity failure
11 = Transmitter seems well failure
12 = Receiver seems well failure
13 = Receive mismatch
14 = Transmit mismatch
*15 = STAR seems well failure
17-23 = Time slot during which failure occurred—Phase A

* Not used in TSI-2.

K-Code (Word 12)

Bit 0 = SPC
1-6 = Member number
7-11 = Unit type (TSI=5)

LEVEL (Word 13)

Bit 0-2 = Failing level (0-7)

SEC ESR even (Word 14) (Any TSI-1 Member or Even TSI-2 Member)

Bit 0-7 = SPC 0, MEMPF Level 0-7
8-15 = SPC 1, MEMPF Level 0-7

SEC ESR Odd (Word 15) (TSI-2 only—Odd Member)

Bit 0-7 = SPC 0, MEMPF Level 0-7
8-15 = SPC 1, MEMPF Level 0-7

Suspect Controller (Word 16)

Bit 0-1 = 0 — Controller 0
1 — Controller 1
2 — Both controllers

Error (Word 18)

Bit 0 = 0 — RTSMPF
1 — TTSMPF

Time Slot (Word 19)

Bit 0-6 = Time slot

Memory Read CO (Word 20)

Bit 0-6 = Channel
7-9 = Serial switch level
10 = Busy/idle bit
11 = Parity bit

Memory Read C1 (Word 21)

Bit 0-6 = Channel
7-9 = Serial switch level
10 = Busy/idle bit
11 = Parity bit

Retry Pass/Fail Flags (Word 22)

Bit 0-1 = 0 — Both controllers passed retry
1 — Controller 0 only failed retry
2 — Controller 1 only failed retry
3 — Both controllers failed retry

Memory Correction Flag (Word 23)

Bit 0 = 0 — No correction attempted
1 — Correction attempted

Auxiliary Data- (TSI RSW)

DUMP SIZE/TYPE	SOFTWARE STATUS C0	SOFTWARE STATUS C1	HARDWARE STATUS C0	HARDWARE STATUS C1	0......0
UTYPE TRANS	ASW ESR C0	ASW ESR C1	AINT ESR C0	AINT ESR C1	0......0
K-CODE EVEN	LEVEL ODD	RSW ESR 0....0	RSW ESR 0....0		

Dump Size/Type (Word 0)

Bits 0-23 value = octal 00001044 or 00001045

Bit 0 = TAG = 0
1-8 = Dump size = 18 decimal
9-12 = Dump type - RSW = 1

SOFTWARE STATUS—Controller 0 or 1 (Words 1, 2)

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce cross-coupled data from mate
5 = Stop controller autonomous operation
6 = Indicates active controller
7 = Diagnostic of this controller requested
8 = Remove via TTY
9 = Indicates which TSI half sends to TMS network 0
10 = Indicates which TSI half sends to TMS network 1
11 = Indicates from which TMS network this TSI half receives
12 = Controller OS
13 = Bus access circuit 0 power off
14 = Bus access circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on PU bus 0
17 = Controller cannot send on PU bus 0
18 = Controller cannot receive on PU bus 1
19 = Controller cannot send on PU bus 1
20-23 = PU maintenance code

HARDWARE STATUS—Controller 0 or 1 (TSI-1 J4A001A)
(Words 3, 4)

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce
5 = Stop autonomous operation
6 = Active unit
7 = Update mode
8 = PEST—Inhibit interrupts
9 = Indicates which TSI half sends to TMS network 0
10 = Indicates which TSI half sends to TMS network 1
11 = Indicates from which TMS network this TSI half receives
12-13 = FIS0, FIS1—Enables bits 19-22 and selects master, secondary, or TACC FAN-IN packs for diagnostics (Normally = 00)
14 = FS—Forces zeros or ones across matchers when bit 15 = 1
15 = FE—Force enable for bit 14
16 = Loop around
17 = PTS—Places BMAs in maintenance mode
18 = SSFE—Serial switch force enable
19 = HFIS—When bits 12-13 are not 00, selects FAN-IN from SPC 0 or 1
20-22 = BIS0, BIS1, BIS2—Enables 1 of 8 branches of the FAN-IN packs selected by bits 12-13, 19
23 = Not used

HARDWARE STATUS—Controller 0 or 1 (TSI-2 J4A001B) (Words 3, 4)

Bit 0-11 = Same as TSI-1
12 = Diagnose internal read access
13 = BMC maintenance mode
14-17 = Same as for TSI1
18 = Diagnose SPC select
19 = Not used
20 = Diagnose matcher enable
21 = BMB maintenance mode
22 = Enable all levels on memory writes
23 = Not used

UTYPE TRANS—Unit-Type Translator (Word 6)

Bit 0-23 = First word of Unit-Type Translator for failing TSI

ASW ESR—Controller 0 or 1 (Words 7, 8)

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = PUB parity failure even bits
3 = PUB parity failure odd bits
4 = Mode failure
5 = Receive time slot memory audit failure
6 = Transmit time slot memory audit failure
7 = Busy/idle memory audit failure
8 = Receive time slot memory parity failure
9 = Transmit time slot memory parity failure
10 = Busy/idle memory parity failure
11 = Address mismatch
12 = Data write mismatch
13 = Busy/idle memory write mismatch

AINT ESR—Controller 0 or 1 (Words 9, 10)

Bit 0 = Clock error (internal)
1 = Time slot counter sequence check
2 = Time slot counter mismatch
3 = Clock mismatch (TSI-2—twisted ring counter mismatch)
4 = Receive time slot memory parity failure
5 = Transmit time slot memory parity failure
6 = Busy/idle memory parity failure
7 = Buffer Memory A parity failure
8 = Buffer Memory B parity failure
10 = Leading one DET parity failure
11 = Transmitter seems well failure
12 = Receiver seems well failure
13 = Receive mismatch
14 = Transmit Mismatch
*15 = STAR seems well failure
17-23 = Time slot during which failure occurred—Phase A

* Not used in TSI-2

K-Code (Word 12)

Bit 0-6 = Member ID (TMS)
= 0 = SPC
= 1-6 = Member ID (TSI)
7-11 = Unit ID

Level (Word 13)

Bit 0-2 = Level

RSW ESR—Even Member TSI (Word 14)

Bit 0-6 = Receiver seems well failure SPC 0
8-14 = Receiver seems well failure SPC 1

RSW ESR—Odd Member TSI (Word 15)

Bit 0-6 = Receiver seems well failure SPC 0
8-14 = Receiver seems well failure SPC 1

Auxiliary Data- (TSI TRPF, XTSI TRPF, PCMM)

See Appendix.

TUC- Tape Unit Controller Frame Printouts

TUC Hot-Line Functions

Scan Back Results

Bit 0 = Hot-line pulse was activated
1 = Bus 1 flip-flop
2 = Trouble flip-flop
3 = Clock out of sync
4 = Inhibit clock out of sync
5 = AUT clock set request
6 = Not used
7 = Not used
8 = Slow-down request has occurred
9 = No correction necessary has occurred
10 = Speed up request has occurred
11 = Clock initialization has occurred
12 = Not used
13 = Not used
14 = Clock out of sync has occurred
15-23 = Not used

Hot-Line Functions	Add.
Select Bus 0	60
Select Bus 1	63
Clock Set Request	65
Power Initialization	66
Scan Back only	71
Clear Clock Summary	72
Operational Initialization	74
Maintenance Freeze	77

VIF- Voice Interface Frame Printouts

VIF Critical Registers

VC4STAT	VC4VIUSTAT1	0.....0	0.....0	0.....0	0.....0
VC4R0-1	VC4R2-3	VC4R4-5	VC4R6-7	VC4R8-9	VC4R10-11
VC4R12-13	VC4R14-15	0.....0	0.....0	0.....0	0.....0
VC4R0-1	VC4R2-3	VC4R4-5	VC4R6-7	VC4R8-9	VC4R10-11
VC4R12-13	VC4R14-15	0.....0	0.....0	0.....0	0.....0

NOTE:
The first group VC4R0-1 through VC4R14-15 is Controller 0. The second group VC4R0-1 through VC4R14-15 is Controller 1.

VC4STAT—VIC Software Status

Bit 0-3 = VIU status 0-3 (Controller 0), 4-7 (Controller 1)
4 = BASM has been set
5 = State of VIU control bus flip-flop
6 = Multiple VIU failure
7 = Diagnostic requested
8 = Removed via TTY
9 = Matcher PESTs set
10 = PU Bus 0 send-on
11 = PU Bus 1 send-on
12 = Controller out of service
13 = Bus access Circuit 0 power off
14 = Bus access Circuit 1 power off
15 = Power off controller
16 = Controller cannot receive from base SP
17 = Controller cannot send on PU Bus 0
18 = Controller cannot receive from duplicate SP
19 = Controller cannot send on PU Bus 1
20-23 = PU maintenance code

VC4VIUSTAT1—Controller 1 Status

Bit 0 = VIU 4 service status
1 = VIU 5 service status
2 = VIU 6 service status
3 = VIU 7 service status

VC4R0-1—Registers 0 and 1 Read Format

Bit 0-7 = Read format for Register 0
8-15 = Read format for Register 1

VC4R2-3—Registers 2 and 3 Read Format

Bit 0-7 = Register 2 read format
8 = VIC 0 Send 0
9 = VIC 0 Send 1
10 = VIC 1 Send 0
11 = VIC 1 Send 1

VC4R4-5—Registers 4 and 5 Read Format

Bit 0 = VIU 0 failing
1 = VIU 1 failing
2 = VIU 2 failing
3 = VIU 3 failing
4 = VIU 4 failing
5 = VIU 5 failing
6 = VIU 6 failing
7 = Spare failing—1 in this item prohibits protection switch
8 = VIU 0 protection switched
9 = VIU 1 protection switched
10 = VIU 2 protection switched
11 = VIU 3 protection switched
12 = VIU 4 protection switched
13 = VIU 5 protection switched
14 = VIU 6 protection switched
15 = No protection switch active

VC4R6-7—Registers 6 and 7 Read Format

Bit 0 = PEST check frame mismatch
1 = PEST ESM mismatch
2 = PEST reply register mismatch
3 = PEST multiplexer mismatch
4 = PEST status register mismatch
5 = PEST control buffer parity violation
6 = PEST control buffer parity violation
7 = PEST PSL mismatch
8 = PEST digital signal generator mismatch
9 = PEST digital signal generator mismatch
10 = PEST reply register parity violation

VC4R8-9—Registers 8 and 9 Read Format

Bit 0-7 = Read format for register 8
8-15 = Read format for register 9

VC4R10-11—Registers 10 and 11 Read Format

Bit 0 = F-level PEST
1 = Interject PEST
2 = Set when mate controller is maintenance isolated
3 = Set when mate sends are cut off
5 = Autonomous F-level flag
6 = Interject flag
7 = Multiple VIU failure
8 = Unit select relay state
9 = Ground relay state
10 = PCM relay state

VC4R12-13—VIC Error Source Registers 12 and 13

Bit 0 = VIC 0 input register parity violation
1 = VIC 1 input register parity violation
3 = Timing receiver out of frame
4 = Trunk selector logic 0 violation
5 = Trunk selector logic 1 violation
6 = Trunk selector logic 2 violation
7 = Trunk selector logic 3 violation
8 = Timing receiver code violation
9 = Word/frame counter violation

VC4R14-15—VIC Error Source Registers 14 and 15

Bit 0 = Indicator check frame mismatch
1 = ESM mismatch on input register
2 = Input to reply register mismatch
3 = Indicator multiplexer mismatch
4 = Status memory mismatch
5 = VIU control buffer parity violation
6 = VIU control buffer parity violation
7 = PSL function code mismatch
8 = Digital signal generator mismatch
9 = Reply register parity violation
10 = Error source register mismatch
11 = Remote input parity violation
12 = Remote timing receiver code violation
13 = Remote frame counter violation

VC4R12-13—VIU Error Source Registers 12 and 13

Bit 1 = Signal failure-test Trunk 3
2 = Signal failure-test Trunk 2
3 = Signal failure-test Trunk 1
4 = Signal failure-test Trunk 0
5 = Parity violation-Decoder 0 input
6 = Transmitter parity violation
9 = High distortion-test Trunk 3
10 = High distortion-test Trunk 2
11 = High distortion-test Trunk 1
12 = High distortion-test Trunk 0
13 = Parity violation-maintenance control
14 = Parity violation-decoder 1 input

VC4R14-15—VIU Error Source Registers 14 and 15

Bit 1 = Upper output translator failure
2 = Lower output translator failure
3 = Upper input translator failure
4 = Lower input translator failure
5 = Parity violation-access control
6 = Parity violation-receiver
10 = Power supply failure
11 = Clock state
12 = Clock switchover
14 = Carrier alarm

VIC Alarms SD-5G158-01

Alarm	Source of Alarm
PO*	Bad Incoming Parity to Controller (FS2) FA 741 148-11 (0) 148-26 (1)
OOF	Out of Frame on Incoming PCM (FS8) FB481— 144-07(0) 144-31 (1)
TCO	FA 754: 156-12 (FS12)
TC1	FA 754: 156-13 (FS12) 1—and only—1 out of 128 Failure Trunk Loop Select Logic
TC2	FA 754: 156-14 (FS12)
TC3	FA 754: 156-15 (FS12)
CC0*	GBC Counter Failure (Checks that Parity Alternates) (FS8) FA 747: 144-08 (0) 144-29 (1)
CC1*	GWC Master and Slave Counters Mismatch (FS8) FA 748: 144-09 (0) 144-28 (1)
MMICF	Mismatch of Indicator Check frame ‘‘P’’ Pulses between Controllers (FS8) FA 749: 144-10 (0) 144-27(1)
MMESM	Mismatch of Enable Select Mode ‘‘F/F’’ between Controllers (FS2) FA 741: 148-11 (0) 148-26 (1)

Alarm	**Source of Alarm**
MMREP	Mismatch of 17-bit Matcher Between Controllers (FS6) FA 760: 152-18 (0) 152-19 (1)
MMMUX	Mismatch of Status Memory Multiplexer Outputs Between Controllers (FS11) FA 756: 144-17, 18 & 148-17, 18 (0) 144-20, 19 & 148-20, 19 (1)
MMSM	Mismatch of Status Memory Data Inputs Between Controllers (FS10) FA 757: 144-14 (0) 144-23(1) FA 758
MMP1	Mismatch of VIU Maintenance Control Bus Parity Bit Controllers (FS10) FA 753: 148-03 (0) 148-34 (1)
MMP2	Mismatch of VIU Access Control Bus Parity Bit Controllers (FS10) FA 753: 148-03 (0) 148-34 (1)
MMPSL	Mismatch of 5-Bit Matcher Between Controllers (FS6) FA 760: 152-18 (0) 152-19 (1)
MMDSG	Mismatch of Digital Signal Generator Output between Controllers (FS9) FA 750: 144-12 (0) 144-25 (1)
RRPE	Parity Difference between Input and Output of Reply Register (FS4) FA 745: 152-16, FA 744: 152-17 (0) FA 745: 152-21, FA 744: 152-20 (1)
MMIIB	Mismatch of II Bit Matcher Between Controllers (FS6) FA 760: 152-18 (0) 152-19 (1)
*	Suffix (L) Indicates Controller’s Indication of His Own Alarm Suffix (R) Indicates Controller’s Indication of His Mate’s Alarm

VIF Controller Phase 1 Tests

Test 7—R13/12

BIT 0	=	POL
3	=	OOF
4	=	TC0
5	=	TC1
6	=	TC2
7	=	TC3
8	=	CCOL
9	=	CCIL

Test 8—R15/14

BIT 0	=	MMICF
1	=	MMESM
2	=	MMREP
3	=	MMMUX
4	=	MMSM
5	=	MMP1
6	=	MMP2
7	=	MMPSL
8	=	MMDSG
9	=	RRPE
10	=	MMIIB
11	=	POR
12	=	CC0R
13	=	CC1R

Voice Interface Unit (VIU) Phase 1 Tests

Test 7—R13/12

Bit 1	=	S3
2	=	S2
3	=	S1
4	=	S0
5	=	P2
6	=	P1
9	=	D3
10	=	D2
11	=	D1
12	=	D0
13	=	P4
14	=	P3

Test 8—R15/14

Bit 1	=	TRU
2	=	TRL
3	=	TTU
4	=	TTL
5	=	P6
6	=	P5
10	=	PWR
11	=	CST
12	=	CSO
14	=	REF

Voice Interface Unit (VIU) Error Source Register Reformatted

RCNT = 54 VIU O.....RCMT 61 = VIU 7

Bit	Name	Description
0	RS3	Signal alarm in block containing trunk 125
1	RS2	Signal alarm in block containing trunk 127
2	RS1	Signal alarm in block containing trunk 126
3	RS0	Signal alarm in block containing trunk 0
4	RPV2	Alarms when there is a parity failure in decoder input processor (DIP)—Even information
5	RPV1	Parity over data passed between packs FA727, FA571, AND FB220
6	RD3	High distortion in block containing trunk 125
7	RD2	High distortion in block containing trunk 127
8	RD1	High distortion in block containing trunk 126
9	RD0	High distortion in block containing trunk 0
10	RPV4	Alarms when parity transmitted to access FA732 control and that formed within the access control differ
11	RPV3	Alarms when there is a parity failure in decoder input processor (DIP)—Odd information
12	RTRU	Alarms when a failure occurs in FA721, slot 15-22. the alarm monitors the output clocks from this circuit pack
13	RTRL	Alarms when a failure occurs in FA721, slot 03-22. The alarm monitors the output clocks from this circuit pack

Bit	Name	Description
14	RTTU	Alarms when a failure occurs in FA721, slot 15-09. The alarm monitors the output clocks from this circuit pack
15	RTTL	Alarms when a failure occurs in FA721, slot 03-09. The alarm monitors the output clocks from this circuit pack
16	RPV6	Parity violation in maintenance control FA731, or when parity transmitted from controller is in error
17	RPV5	Parity violation in serial reframing detector FA733, in slot 03-16, or retiming register FA730 in slot 03-17
18	RPWR	Indicates failure in 80A or 81A power supply
19	RCST	State of VIU clock not used because when set (-1), VIU alarms
21	—	—
22	RREF	Failure to frame on PCM data can be caused by (1) TSI problem, (2) coaxial line problem, or (3) problem in FB480
23	—	—

Voice Interface Frame (VIF) JA14 Circuit Pack Locations

The table, on the following page, lists the equipment locations of the JA14 circuit packs for each trunk. The example explains how to read the table.

EXAMPLE: 1 068-01

TRUNK BAY	BAY NO.	SHELF LOCATION	SLOT IDENTIFICATION
1	0	68	01

Equipment Locations

1	068-01	25	075-01	49	175-01	73	268-01	97	275-01
2	068-02	26	075-02	50	175-02	74	268-02	98	275-02
3	068-03	27	075-03	51	175-03	75	268-03	99	275-03
4	068-04	28	075-04	52	175-04	76	268-04	100	275-04
5	068-05	29	075-05	53	175-05	77	268-05	101	275-05
6	068-06	30	075-06	54	175-06	78	268-06	102	275-06
7	068-07	31	075-07	55	175-07	79	268-07	103	275-07
8	068-08	32	075-08	56	175-08	80	268-08	104	275-08
9	068-09	33	075-09	57	175-09	81	268-09	105	275-09
10	068-10	34	075-10	58	175-10	82	268-10	106	275-10
11	068-11	35	075-11	59	175-11	83	268-11	107	275-11
12	068-12	36	075-12	60	175-12	84	268-12	108	275-12
13	068-13	37	075-13	61	175-13	85	268-13	109	275-13
14	068-14	38	075-14	62	175-14	86	268-14	110	275-14
15	068-15	39	075-15	63	175-15	87	268-15	111	275-15
16	068-16	40	075-16	64	175-16	88	268-16	112	275-16
17	068-17	41	075-17	65	175-17	89	268-17	113	275-17
18	068-18	42	075-18	66	175-18	90	268-18	114	275-18
19	068-19	43	075-19	67	175-19	91	268-19	115	275-19
20	068-20	44	075-20	68	175-20	92	268-20	116	275-20
21	068-21	45	075-21	69	175-21	93	268-21	117	275-21
22	068-22	46	075-22	70	175-22	94	268-22	118	275-22
23	068-23	47	075-23	71	175-23	95	268-23	119	275-23
24	068-24	48	075-24	72	175-24	96	268-24	120	275-25

VIF JA1/JA2 Circuit Pack Layout

This table lists the associated equipment locations corresponding to each trunk and equipment locations corresponding to single and double VIU alarms.

JA1 Slot		1	2		3	4	5	6		7	8
JA2 Slot		23	24		25	26	27	28		29	30
Double Alarm											
	S	31	63		95	127	32	64		96	0
	H	27	59		91	123	28	60		92	124
D0+D2	E	23	55		87	119	24	56		88	120
(S0+S2)	L	19	51	**D**	83	115	20	52	**D**	84	116
JA4	F	15	47	**2**	79	111	16	48	**0**	80	112
(09-30)		11	43		75	107	12	44		76	108
	1	7	39		71	103	8	40		72	104
	5	3	35		67	99	4	36		68	100

	S	29	61		93	125	30	62		94	126
	H	25	57		89	121	26	58		90	122
D1+D3	E	21	53		85	117	22	54		86	118
(S1+S3)	L	17	49	**D**	81	113	18	50	**D**	82	114
JA4	F	13	45	**3**	77	109	14	46	**1**	78	110
(09-29)		9	41		73	105	10	42		74	106
	3	5	37		69	101	6	38		70	102
		1	33		65	97	2	34		66	98

Double Alarm	**Double Alarm**
D2+D3	D0+D1
(S2+S3)	(S0+S1)
JA3 (09-02)*	JA3 (09-04)*
JA6 (09-03)*	JA6 (09-05)*
JA7 (09-25)*	JA7 (09-27)*
JA5 (09-26)*	JA5 (09-28)*
S2+S3 ONLY	S0+S1 ONLY
FA723 (15-11)	FA723 (15-13)
FA724 (03-19)	FA724 (03-20)

* Input PAM

Single Alarm Resolution (See Note)

1. Swap the JA1s and JA2s associated with a single alarm into pack locations that correspond to the other alarm pair; move the four JA1s into one alarm position and the four JA2s into the other.
2. The next single alarm to occur implicates either the JA1s or JA2s. (If the single alarm did not change, see double alarm resolution.)
3. Move three of the four suspect packs into the other alarm quadrants.
4. The next single alarm to occur identifies the faulty pack.

Double Alarm Resolution (See Note)

1. Swap the JA3 and JA6 associated with a double alarm with the other JA3 and JA6.
2. If the double alarm moves with the pack swap, move one of the suspect packs back to its original location. The next double alarm identifies the faulty pack. If the double alarm remains the same, swap the JA5 and JA7 associated with double alarm with the other JA5 and JA7. The next double alarm identifies the faulty pack.
3. If a single alarm condition still exists, suspect JA4 packs.
4. If the double alarm condition still exists for signal alarms, suspect FA723 or FA724.

NOTE:
Revert back to the next previous pack move if the VIU shows an abnormal increase in number of alarms with the current pack move. Restrict the number of packs to be swapped, and proceed with a similar strategy.

Other Alarms

S0	FA 731 (03-11)
S1	FA 731 (03-11)
S2	FA 731 (03-11)
S3	FA 731 (03-11)
P1	FA 571 (15-17), FB 220 (15-21), FA727 (15-15)
P2	FA 726 (03-18)
P3	FA 726 (03-18)
P4	FA 732 (03-13)
P5	FA 733 (03-16), FA 730 (03-17)
P6	FA 731 (03-11)
CSO	FA 729(15-19)
CST	FA 729 (15-19)
PWR	80A (09-08), 81A (09-23)
REF	FB 480 (03-15) FA 733 (03-16), FA 730 (03-17)
TRL	FA 721 (03-22)
TRU	FA 721 (15-22)
TTL	FA 721 (03-09)
TTU	FA 721 (15-09)

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Expanded Time-Slot Interchange (XTSI) and Time-Slot Interchange (TSI)

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Expanded Time-Slot Interchange (XTSI) and Time-Slot Interchange (TSI)

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Expanded Time-Slot Interchange (XTSI) Printout

This Appendix contains layouts for XTSI and TSI for the 4E26 Generic.

Auxiliary Data- (TSI TRPF, XTSI TRPF, PCMM)

Word 0	Word 1*	Word 2*	Word 3*	Word 4*	Word 5*
Word 6	Word 7*	Word 8	Word 9	Word 10*	Word 11
Word 12	Word 13	Word 14	Word 15	Word 16	Word 17
Word 18	Word 19	Word 20	Word 21	Word 22	Word 23
Word 24	Word 25	Word 26	Word 27	0..........0	Word 29*
Word 30	Word 31	Word 32	Word 33	Word 34	Word 35
Word 36	Word 37*	Word 38*	Word 39*	Word 40*	Word 41
Word 42*	Word 43*	Word 44	Word 45	Word 46	Word 47
Word 48	Word 49	0..........0	Word 51	Word 52	Word 53
Word 54	Word 55	Word 56	Word 57	Word 58	Word 59
Word 60	Word 61	Word 62	Word 63	Word 64	Word 65
Word 66	Word 67	Word 68	Word 69	0..........0	0..........0

NOTE:
Word 0 through Word 59 may be used by both XTSI and TSI unless otherwise indicated. Word 60 through Word 71 are for XTSI.

* This word has a different word breakdown for XTSI and TSI.

DUMP SIZE/TYPE (Word 0)

Octal 00000220 or 00000221

Bit 0 = TAG = 0 or = 1
1-8 = Dump size = 72 decimal
9-12 = Dump type - TRPF = 0, TMM = 0, PCMM = 0

TTSI SW STAT—Controller 0 or 1 (Words 1, 2) (XTSI Only)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce controller from mate
5 = Stop autonomous processing in this controller
6 = Read-only divorce controller from mate. (Duplicate of bit 4)
7 = Active/standby. When set, this controller is active
8 = Not used
9 = Indicates which TSI controller sends to TMS 0-3 network 0
10 = Indicates which TSI controller sends to TMS 0-3 network 1
11 = Indicates which TMS 0-3 network half this TSI controller receives from
12 = Out-of-service
13 = This controller has been removed by TTY request
14-15 = Not used
16 = Loop around
17-19 = Not used
20-23 = PU maintenance code

TTSI SW STAT—Controller 0 or 1 (Words 1, 2) (TSI Only)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce cross-coupled data from mate
5 = Stop controller autonomous operation
6 = Indicates active controller
7 = Diagnostic of this controller requested
8 = Remove via TTY
9 = Indicates which TSI half sends to TMS Network 0
10 = Indicates which TSI half sends to TMS Switch 1
11 = Indicates from which TMS network this TSI half receives
12 = Controller OS
13 = Bus access Circuit 0 power off
14 = Bus access Circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on PU Bus 0
17 = Controller cannot send on PU Bus 0
18 = Controller cannot receive on PU Bus 1
19 = Controller cannot send on PU Bus 1
20-23 = PU maintenance code

TTSI HW STAT—Controller 0 or 1 (Words 3, 4) (XTSI Only)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce controller from mate
5 = Stop autonomous processing in this controller
6 = Read-only divorce controller from mate. (Duplicate of bit 4)
7 = Active/standby. When set, this controller is active
8 = Not used
9 = Indicates which TSI controller sends to TMS 0-3 Network 0
10 = Indicates which TSI controller sends to TMS 0-3 Network 1
11 = Indicates which TMS 0-3 network half this TSI controller receives from
12 = Enable clock error 1
13 = Enable clock error 2
14 = Control register exercise enable
15 = Not used
16 = Loop around
17-23 = Not used

TTSI HW STAT—Controller 0 or 1 (TSI-1 J4A001A) (Words 3, 4) (TSI Only)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce
5 = Stop autonomous operation
6 = Active unit
7 = Update mode
8 = PEST—Inhibit interrupts
9 = Indicates which TSI half sends to TMS Network 0
10 = Indicates which TSI half sends to TMS Network 1
11 = Indicates from which TMS network this TSI half receives
12-13 = FIS0, FIS1—Enables bits 19-22 and selects master, secondary, or TACC FAN-IN packs for diagnostics (Normally = 00)
14 = FS—Forces zeroes or ones across matchers when Bit 15 = 1
15 = FE—Force enable for Bit 14
16 = Loop around
17 = PTS—Places BMAs in maintenance mode
18 = SSFE—serial switch force enable
19 = HFIS—When Bits 12-13 are not 00, selects FAN-IN from SPC 0 or 1
20-22 = BIS0, BIS1, BIS2—Enables 1 of 8 branches of the FAN-IN packs selected by bits 12-13, 19
23 = Not used

TTSI HW STAT—Controller 0 or 1 (TS1-2 J4A001B) (Words 3, 4) (TSI Only)

Bit 0-11 = Same as TSI-1
12 = Diagnose internal read access
13 = BMC maintenance mode
14-17 = Same as for TSI-1
18 = Diagnose SPC select
19 = Not used
20 = Diagnose matcher enable
21 = BMB maintenance mode
22 = Enable all levels on memory writes
23 = Not used

TTSI Path (Word 5) (XTSI Only)

Bit 0-9 = Channel
10 = SPU in path
12-14 = Level
15 = SPC
16-21 = Member number

TTSI Path (Word 5) (TSI Only)

Bit 0-6 = Channel
9-11 = Level
12 = SPC
13-18 = Member number
21-23 = Terminating serial switch level

Active TMS Network (Word 6)

Bit 0 = TMS network half 0 active
1 = TMS network half 1 active

TTSM0 ARRAY—Controller 0 or 1 (Word 7,8) (XTSI Only)
TTSM1 ARRAY—Controller 0 or 1 (Word 9,10) (XTSI Only)

Bit 0-6 = Network time-slot
7-9 = A-Link
10-11 = Buffer partition
12 = Path busy/idle
13 = Forward voice control
14 = Transmit busy/idle

TTSM ARRAY—Controller 0, Controller 1 (Word 7) (TSI Only)

Bit 0-6 = Channel, Controller 0
7-9 = Level, Controller 0
10 = Busy/idle bit, Controller 0
11 = Parity, Controller 0
12-18 = Channel, Controller 1
19-21 = Level, Controller 1
22 = Busy/idle bit, Controller 1
23 = Parity, Controller 1

TTSMP—TSI-1 Word 8, TSI-2 Words 8, 9)

Bit 0-7 = Transmit time slot memory P.F. SPC0 or 2
8-15 = Transmit time slot memory P.F. SPC1 or 3

TMS ST2 Path (Word 11)

Bit 0-3 = B-level
6-9 = A-level
12-15 = Switch
18-23 = TMS member number

TMS Access Result (Word 12)

Bit 0-1 = TMS access result
0 = Both controllers passed
1 = Controller 0 failed
2 = Controller 1 failed
3 = Both controllers failed

TMS SW STAT—Controller 0 or 1 (Words 13, 14)

Bit 0 = Maintenance access
1 = Receive on (PU bus 0 or 1)
2 = Send on PU bus 0
3 = Send on PU bus 1
4 = Divorce cross-coupled data from mate
5 = Stop controller autonomous operation
6 = Not used
7 = Diagnostic of this controller requested
8 = Remove via TTY
9-11 = Not used
12 = Controller OS
13 = Bus access Circuit 0 power off
14 = Bus access Circuit 1 power off
15 = Controller power off
16 = Controller cannot receive on PU Bus 0
17 = Controller cannot send on PU Bus 0
18 = Controller cannot receive on PU Bus 1
19 = Controller cannot send on PU Bus 1
20-23 = PU maintenance code

TMS HW STAT—Controller 0 or 1 (Words 15, 16)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce
5 = Stop autonomous operation
6 = Inhibit B/I bit checks
7 = Inhibit data matching on writes
8 = PEST—Inhibit interrupts
9 = Synchronize with TDNET subsystem
10 = Soft stop controller autonomous operation
11 = Inhibit gating to memory registers
12 = Allow self-start
13 = Soft stop at Phase 6
14 = Forces zeroes across time slot matcher interface
15 = Forces ones across time slot matcher interface
16-23 = Not used

TMS ST1 Path (Word 17)

Bit 0-3 = B-level
6-9 = A-level
12-15 = Switch
18-23 = TMS member number

TMS SW2 Array—Controller 0 or 1 (Words 18, 19)

Bit 0-3 = B-level
4 = Busy/idle
5 = Parity

TMS SW1 Array—Controller 0 (Words 20 through 23), Controller 1 (Words 23 through 27)

Bit 0-3 = B-level
4 = Busy/idle
5 = Parity
6-9 = B-level
10 = Busy/idle
11 = Parity
12-15 = B-level
16 = Busy/idle
17 = Parity
18-21 = B-level
22 = Busy/idle
23 = Parity

RTSI Path (Word 29) (XTSI Only)

Bit 0-9 = Channel
10 = SPU in path
12-14 = Level
15 = SPC
16-21 = Member number

RTSI Path (Word 29) (TSI Only)

Bit 0-6 = Channel
9-11 = Level
12 = SPC
13-18 = Member number
21-23 = Terminating serial switch level

RTSI Access Result (Word 30)

Bit 0-1 = RTSI First Access Result
0 — Both Controllers Passed
1 — Controller 0 failed
2 — Controller 1 failed
3 — Both controllers failed
Bit 2-3 = RTSI Second Access Result
0 — Both Controllers Passed
1 — Controller 0 failed
2 — Controller 1 failed
3 — Both controllers failed

RTSI SW STAT—Controller 0 or 1 (Words 31, 32)

Bit 0-23 = Same as word 1, 2 format

RTSI HW STAT—Controller 0 or 1 (Words 33, 34)

Bit 0-23 = Same as word 3, 4 format

Path Timeslot (Word 35)

Bit 0-6 = Time slot

RTSI MA RESP—Controller 0 or 1 (Words 36, 37) (XTSI Only)

Bit 0 = Maintenance access
1 = Receive on (PU Bus 0 or 1)
2 = Send on PU Bus 0
3 = Send on PU Bus 1
4 = Divorce controller from mate
5 = Stop autonomous processing in this controller
6 = Cross controller update
7 = Active/standby. When set, this controller is active
8 = Peripheral unit bus even parity failure
9 = Peripheral unit bus odd parity failure
10 = KCODE match error (1 = k-code matched)
11 = Mode bit
12 = Receive on bus complement
13 = PUB sequencer active
14 = Autonomous interrupt
15 = All-seems-well failure
16 = Unassigned OPCODE failure
17 = Mode failure
18 = PUBI parity error
19 = Read-Only Divorce controller from mate. Duplicate of bit 4
20 = OR of local clock failure and clock summary in CESR
21 = TSI clock error - indicates loss of TSI clock
22 = Forced value of: TN0RO if read from controller 0 or TN1RO if read from controller 1
23 = Forced value of: TN2RO if read from controller 0 or TN3RO if read from controller 1

RTSI ASW ESR—Controller 0 or 1 (Words 37, 38) (TSI Only)

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = PUB parity failure even bits
3 = PUB parity failure odd bits
4 = Mode failure
5 = Receive time-slot memory audit failure
6 = Transmit time-slot memory audit failure
7 = Busy/idle memory audit failure
8 = Receive time-slot memory parity failure
9 = Transmit time-slot memory parity failure
10 = Busy/idle memory parity failure
11 = Address mismatch
12 = Data write mismatch
13 = Busy/idle memory write mismatch

RTSI CESR—Controller 0 or 1 (Words 38, 39) (XTSI Only)

Bit 0 = All-seems-well failure
1 = Autonomous interrupt
2 = PUB even parity failure
3 = PUB odd parity failure
4 = Autonomous peripheral unit trouble
5 = Error detected by PUB sequencers
6 = Invalid/unassigned OPCODE
7 = Resident software error bit 0
8 = Resident software error bit 1
9 = Resident software error bit 2
10 = Resident software error bit 3
11 = Audit summary
12 = Mode failure
13 = PUBI parity error
14 = Fabric error summary
15 = Local clock failure on PUBI
16 = Unused
17 = Spare Pack Error Source Summary (Future Expansion)
18 = Control bus and Image Administrator Error summary
19 = Global RAM error summary
20 = EXEC local error summary
21 = EXEC complex backplane error summary
22 = Clock error summary (OR of EXEC and TSI pack clock errors)
23 = GRAM, EXEC Cross controller mismatch

RTSI AINT ESR—Controller 0 or 1 (Words 39, 40)

Bit 0 = Clock error (internal)
1 = Time slot counter sequence check
*2 = Time slot counter mismatch
3 = Clock mismatch (TSI2—Twisted ring counter mismatch)
4 = Receive time-slot memory parity failure
5 = Transmit time-slot memory parity failure
6 = Busy/idle memory parity failure
7 = Buffer Memory A parity failure
8 = Buffer Memory B parity failure
10 = Leading one DET parity failure
11 = Transmitter seems-well failure
12 = Receiver seems-well failure
13 = Receive mismatch
14 = Transmit mismatch
*15 = STAR seems-well failure
17-23 = Time slot during which failure occurred—Phase A

* Not used in TSI-2.

RTSI Receive Error Summary—Controller 0 or 1 (Words 40, 41) (XTSI Only)

Bit 0 = Not used
1 = Not used
2 = TSI cross controller mismatch
3 = Timeslot memory 0 address parity error
4 = Timeslot memory 1 address parity error
5 = Timeslot memory 2 address parity error
6 = Timeslot memory 3 address parity error
7 = Timeslot memory 0 busy/idle parity error
8 = Timeslot memory 1 busy/idle parity error
9 = Timeslot memory 2 busy/idle parity error
10 = Timeslot memory 3 busy/idle parity error
11 = Timeslot memory 0 data parity error
12 = Timeslot memory 1 data parity error
13 = Timeslot memory 2 data parity error
14 = Timeslot memory 3 data parity error
15 = Network synchronization error
16 = 32.768 MHZ phase lock error
17 = 32.768 MHZ clock source error
18-21 = Translations mismatch errors
22 = Cross controller mismatch error

RTSM0 Array—Controller 0 or 1 (Words 42, 43) (XTSI Only)
RTSM1 Array—Controller 0 or 1 (Words 44, 45) (XTSI Only)

Bit 0-9 = Channel
10-11 = Buffer partition
12 = Path busy/idle
13 = Don’t care
14 = Transmit busy/idle

RTSM ARRAY—Controller 0 (Words 42 through 45), Controller 1 (Words 46 through 49) (TSI Only)

0-11 = Even level
Bit 0-6 = Channel
7-9 = Level
10 = Busy/idle
11 = Parity

Bit 12-23 = Odd level
12-18 = Channel
19-21 = Level
22 = Busy/idle
23 = Parity

RTSI Pest—Controller 0 or 1(Word 46, 47) (XTSI Only)

Bit 0 = All-seems-well failure inhibit
1 = Autonomous interrupt inhibit
2 = PUB even parity failure inhibit
3 = PUB odd parity failure inhibit
4 = Autonomous peripheral unit trouble inhibit
5 = PUB sequencer error inhibit
6 = Invalid/unassigned OPCODE inhibit
7 = Resident Software error bit 0 inhibit
8 = Resident Software error bit 1 inhibit
9 = Resident Software error bit 2 inhibit
10 = Resident Software error bit 3 inhibit
11 = Audit summary inhibit
12 = Mode failure inhibit
13 = PUBI parity error inhibit
14 = Fabric error summary inhibit
15 = Local clock failure inhibit on PUBI
16 = Unused
17 = Spare pack Error Source Summary (Future Expansion)
18 = Control bus and Image Administrator Error summary inhibit
19 = Global RAM error summary inhibit
20 = EXEC error summary inhibit
21 = Backplane error summary inhibit
22 = Clock error summary inhibit
23 = Cross controller mismatch inhibit

RTSI SPU Nailup (Word 48, 49) (XTSI Only)

Bit 12-15 = SPU Digroup
18-22 = SPU Number

Original Suspect List (Word 51)

Bit 0 = TTSI Controller 0
1 = TTSI Controller 1
2 = TMS Controller 0
3 = TMS Controller 1
4 = RTSI Controller 0
5 = RTSI Controller 1

Trace Outcome (Word 52)

Bit 0-4 = Decimal value = Outcome
0 — TTSI Routing
1 — TTSI No Data
2 — Pass
3 — TTSI Data Mismatch
4 — TMS Access Failure
5 — TMS Data Mismatch
6 — TMS Software
7 — RTSI Duplicate Failure
10 — RTSI Access Failure
11 — RTSI Routing
12 — RTSI Data Mismatch
13 — RTSI Software
14 — RTSI Network Mismatch
15 — Good Path
16 — TMS Duplex Failed

Outcome Suspect List (Word 53)

Bit 0 = TTSI Controller 0
1 = TTSI Controller 1
2 = TMS Controller 0
3 = TMS Controller 1
4 = RTSI Controller 0
5 = RTSI Controller 1

TTSI UTYPE TRANS (Word 54)

Bit 0-15 = First word of Unit-Type Translator for failing TTSI
16-17 = UTMN Equippage
0 - Unequipped
1 - Growth
2 - Special growth
3 - Equipped

18-20 = Member type hardware generation (MTHG)
21-23 = Member type
1 - Original TSI frame
2 - Cost reduced TSI
3 - Cost reduced TSI companion
4 - XTSI
5 - XTSI companion

TMS UTYPE TRANS (Word 55)

Bit 0-23 = First word of Unit-Type Translator for failing TMS

RTSI UTYPE TRANS (Word 56)

Bit 0-15 = First word of Unit-Type Translator for failing RTSI
16-17 = UTMN Equippage
0 - Unequipped
1 - Growth
2 - Special growth
3 - Equipped

18-20 = Member type hardware generation (MTHG)
21-23 = Member type
1 - Original TSI frame
2 - Cost reduced TSI
3 - Cost reduced TSI companion
4 - XTSI
5 - XTSI companion

TTSI UTMN (Word 57)

Bit 0-6 = TSI member number
7-13 = Unit type (TSI = 5)

TMS UTMN (Word 58) (TSI Only)

Bit 0-6 = TMS member number
7-13 = Unit type (TMS = 4)

RTSI UTMN (Word 59)

Bit 0-6 = TSI member number
7-13 = Unit type (TSI = 5)

PCMIL—Controller 0 or 1 (XTSI) (Word 60, 61)

Bit 0-7 = Input bus 0
8-15 = Input bus 1
16 = Input bus 0 parity bit
17 = Input bus 1 parity bit
18 = BM0 input MUX select (TSXRO bit 12)
19 = BM0 input MUX select (TSXRO bit 13)
20 = BM1 input MUX select (TSXR1 bit 12)
21 = BM0 input MUX select (TSXR1 bit 13)
22-23 = Not used

PCMIH—Controller 0 or 1 (XTSI) (Word 62, 63)

Bit 0-7 = Input bus 2
8-15 = Input bus 3
16 = Input bus 2 parity bit
17 = Input bus 3 parity bit
18 = BM2 input MUX select (TSXR2 bit 12)
19 = BM2 input MUX select (TSXR2 bit 13)
20 = BM3 input MUX select (TSXR3 bit 12)
21 = BM3 input MUX select (TSXR3 bit 13)
22-23 = Not used

PCMOL—Controller 0 or 1 (Word 64, 65)

Bit 0-7 = Output bus 0
8-15 = Output bus 1
16 = Output bus 0 parity bit
17 = Output bus 1 parity bit
18 = TSM0 busy/idle bit 12
19 = TSM0 busy/idle bit 13
20 = TSM1 busy/idle bit 12
21 = TSM1 busy/idle bit 13
22-23 = Not used

PCMOH—Controller 0 or 1 (Word 66, 67)

Bit 0-7 = Output bus 2
8-15 = Output bus 3
16 = Output bus 2 parity bit
17 = Output bus 3 parity bit
18 = TSM2 busy/idle bit 12
19 = TSM2 busy/idle bit 13
20 = TSM3 busy/idle bit 12
21 = TSM3 busy/idle bit 13
22-23 = Not used

TTSM Channel/LOD B—Controller 0 or 1 (Word 68,69) (XTSI Only)

Bit 0-9 = Channel
10 = LOD B/I bit
12-15 = SPU Digroup
16-17 = Not Used
18-22 = SPU number

Auxiliary Data- (XTSI BLM Reports)

BSIZE	LPBK_ERR /KIND	HEADER	DATA0	DATA1	DATA2
DATA3	DATA4	DATA5	DATA6	DATA7	DATA8
DATA9	DATA10	DATA11	DATA12	DATA13	DATA14
DATA15	MBPTRS	SDMBPTR	MBSTAT	PSC_OS	PSC_PEST
0.......0					

BSIZE—Auxiliary Data Block Size

Bit 1-6 = Block size

LPBK_ERR/KIND—Loopback Error Flag/Kind of Report

Bit 0 = Kind of report. Only valid if bit equal 0
- 0 = Autonomous
- 1 = Illegitimate

1 = Loopback error flag
- 0 = No loopback error
- 1 = Loopback error result in BLM; therefore, ignore state of bit 0

HEADER—Frame Report Header

If this is a Loopback Report, Frame Report Header is reset.

Bit 0-6 = If Bit 13 = 0; last subopcode in original macro

For subopcode values if source of report is CONTR, see XTSI Group 1 Macro Subopcodes (opcode octal 140) and/or see XTSI In-Service Controller Macro Subopcodes (octal 35)

For subopcode values if source of report is PSC, see Protection Switch Client (PSC) Macro (octal 37)

If Bit 13 = 1; Error Code [see XTSI MB (Header) Defined Error Code]

XTSI Group 1 Macro Subopcodes (Octal)		
Value	**Name**	**Description**
3	IXTC	Hard Initialization
5	FLASHCP	Flash Copy File
11	RRAMV	Read RAM Version
13	ITUPBUS	Initialize Memory Through the XTC Update Bus
14	ITTSRAM	Time-Slot RAM Initialization
15	ITTXRAM	Time-Slot Translation RAM Initialization
16	ITBIMM	Initialize ALF Busy/Idle Memory
20	ITSTRTADR	Starting Address of Initialization
21	ITENDADR	Ending Address of Initialization
22	FPUMP	XTC Flash Pump
25	DGNXTC	XTC Diagnostic
27	VPH	Verify Program hashsum
33	CLAMPPSC	Clamp PSC
34	UCLAMPPSC	Unclamp PSC
35	PSCUPDT	USEC Protection Switch Update
40	SPSNUM	SPU Nailup/Tear Down Execute

XTSI In-Service Controller Macro Subopcodes (Octal)

Value	Name	Description
100	ERSFMEM	Erase Flash Memory
101	WFLASHFILE	Write Flash File
102	RFLASHFILE	Read Flash File
103	SNDFLADDL	Send Low 16 Bits of Flash Memory Address
104	SNDFLADDH	Send High 14 Bits of Flash Memory Address
110	PSCDGNHLP	PSC Diagnostics with XTC Helper
111	FVQ	File Version Query
112	DABP	Dump All XTSI Breakpoints
113	AUDTSMBI	Audit TSM Busy/Idle Bits
114	FPSCINFO	Fetch PSC Information
115	TSIRAM_OM	TSI RAM Initialization Operational Macro
116	ITSTRTADR_OM	Starting Address of Initialization Operational Macro
117	ITENDADR_OM	Ending Address of Initialization Operational Macro

Protection Switch Client (PSC) Macro Subopcodes (Octal)		
Value	**Name**	**Description**
1	ADPSC	Address Protection Switch Client
2	RPSCLRAML	Read PSC Local RAM Low 16-Bits of Address
3	RPSCLRAMH	Read PSC RAM Length and High 8 Address Bits
10	SFPSCBPL	Set Fast Breakpoint on PSC
11	SNPSCBPL	Set Normal Breakpoint on PSC
12	SCPSCBPL	Set Custom Breakpoint on PSC
13	SCPSCBPH	Set Custom Breakpoint on PSC Length
14	SCPSCBPDMA	Set Custom Breakpoint on PSC Direct Memory Address
15	SCPSCBPIMA	Set Custom Breakpoint on PSC Indirect Memory Address
17	SPSCMPBPH	Send PSC Micro-Program Breakpoint on PSC High 8-Bit Address
22	DALLPSCBP	Dump all Breakpoints on PSC
25	PSCDIAG	PSC Diagnostic
26	PSCLPTSTL	Protection Switch Client Loop Test (Low)
27	PSCLPTSTH	Protection Switch Client Loop Test (High)
30	LPSTREQ	Read DS1/DS3 Looparound Status
32	WPSCLRAMAL	Write PSC Local RAM (Low 16-Bit Address)
33	WPSCLRAMAH	Write PSC Local RAM (High 8-Bit Address)
34	WPSCLRAMDL	Write PSC Local RAM Data (Low)
35	WPSCLRAMDH	Write PSC Local RAM Data (High)
36	PSCTINIT	PSC Transmission Initialization

XTSI MB (Header) Defined Error Code

Hex	Octal	Meaning
1	1	XTSI autonomous facility alarm MB report
2	2	XTSI autonomous performance monitoring MB report
3	3	XTSI autonomous FDL (USEC) change in state MB report
4	4	XTSI autonomous loop back MB report
5	5	XTSI autonomous PSC breakpoint (triggered) report
6	6	XTSI autonomous report sent by D3U firmware
7	7	XTSI autonomous report for performance monitoring threshold crossing
41	101	XTSI autonomous PSC PCS service transition report
42	102	Flash memory error
43	103	Busy idle audit error for TSM
44	104	XTSI autonomous PSC power converter alarm
45	105	XTSI autonomous controller breakpoint (triggered) report
46	106	Flash memory or USEC audit disabled
49	111	XTSI autonomous fan/fuse MB report
4A	112	XTC Scheduler Has Been Stopped For 5 Minutes

Other undefined code will results in BLMs.

HEADER—Frame Report Header (Contd)

Bit 8-11 = Number of words in the MB report excluding header
12 = Segment flag
0 = Continued report; not last segment of message
1 = Final report; last segment of message
13 = Autonomous flag
0 = Not autonomous report (client reply)
1 = Autonomous report
14 = Error flag
0 = No error found
1 = Error found
16-20 = Macro ID value sent to the frame
21-22 = Source of report
0 = Controller is source
1 = PSC is source
23 = Unused

DATA0-DATA15—Data Word.

If LPBK_ERR, data words are from LPBK pident. If not LPBK_ERR, data words are the MB report.

MBPTRS—Maintenance Buffer Pointers

Bit 0-11 = Read pointer
12-23 = Write pointer

SDMBPTR—Shadow Maintenance Buffer Pointers

Bit 0-11 = Temporary Read pointer
12-23 = Unused

MBSTAT—Maintenance Buffer Status

Bit 0-11 = Number of reports in MB
12-23 = Unused

PSC_OS—Protection Switch Client OS Bit Array

Bit 0 = PSC 0 (D3U 6) out-of-service
1 = PSC 1 (D3U 0) out-of-service
2 = PSC 2 (D3U 1) out-of-service
3 = PSC 3 (D3U 2) out-of-service
4 = PSC 4 (Spare PCS 0) out-of-service
5 = PSC 5 (Spare PCS 1) out-of-service
6 = PSC 6 (Spare PCS 2) out-of-service
7 = PSC 7 (Spare PCS 3) out-of-service
8 = PSC 8 (D3U 7) out-of-service
9 = PSC 9 (D3U 3) out-of-service
10 = PSC 10 (D3U 4) out-of-service
11 = PSC 11 (D3U 5) out-of-service
12 = PSC 12 (SPU 10) out-of-service
13 = PSC 13 (SPU 0) out-of-service
14 = PSC 14 (SPU 1) out-of-service
15 = PSC 15 (SPU 2) out-of-service
16 = PSC 16 (SPU 3) out-of-service
17 = PSC 17 (SPU 4) out-of-service
18 = PSC 18 (SPU 11) out-of-service
19 = PSC 19 (SPU 5) out-of-service
20 = PSC 20 (SPU 6) out-of-service
21 = PSC 21 (SPU 7) out-of-service
22 = PSC 22 (SPU 8) out-of-service
23 = PSC 23 (SPU 9) out-of-service

PSC_PEST—Protection Switch Client PEST Bit Array

Bit 0 = PSC 0 (D3U 6) PEST status (1 if PESTed)
1 = PSC 1 (D3U 0) PEST status (1 if PESTed)
2 = PSC 2 (D3U 1) PEST status (1 if PESTed)
3 = PSC 3 (D3U 2) PEST status (1 if PESTed)
4 = PSC 4 (Spare PCS 0) PEST status (1 if PESTed)
5 = PSC 5 (Spare PCS 1) PEST status (1 if PESTed)
6 = PSC 6 (Spare PCS 2) PEST status (1 if PESTed)
7 = PSC 7 (Spare PCS 3) PEST status (1 if PESTed)
8 = PSC 8 (D3U 7) PEST status (1 if PESTed)
9 = PSC 9 (D3U 3) PEST status (1 if PESTed)
10 = PSC 10 (D3U 4) PEST status (1 if PESTed)
11 = PSC 11 (D3U 5) PEST status (1 if PESTed)
12 = PSC 12 (SPU 10) PEST status (1 if PESTed)
13 = PSC 13 (SPU 0) PEST status (1 if PESTed)
14 = PSC 14 (SPU 1) PEST status (1 if PESTed)
15 = PSC 15 (SPU 2) PEST status (1 if PESTed)
16 = PSC 16 (SPU 3) PEST status (1 if PESTed)
17 = PSC 17 (SPU 4) PEST status (1 if PESTed)
18 = PSC 18 (SPU 11) PEST status (1 if PESTed)
19 = PSC 19 (SPU 5) PEST status (1 if PESTed)
20 = PSC 20 (SPU 6) PEST status (1 if PESTed)
21 = PSC 21 (SPU 7) PEST status (1 if PESTed)
22 = PSC 22 (SPU 8) PEST status (1 if PESTed)
23 = PSC 23 (SPU 9) PEST status (1 if PESTed)

Control Bus Memory Layout

Control Bus Slot Address	Sack	Client_ID	PSC Number	Subunit/ Circuit Pack
0X10	0115(0X4d)	6 O(6)	PSC 0	D3U 6
0X11	0116(0x4e)	0 O(0)	PSC 1	D3U 0
0X12	0123(0x53)	1 O(1)	PSC 2	D3U 1
0X13	0125(0x55)	2 O(2)	PSC 3	D3U 2
0X14	0126(0x56)	20 O(24)	PSC 4	Spare PCS 0
0X15	0131(0x59)	22 O(26)	PSC 5	Spare PCS 2
0X16	0132(0x5a)	21 O(25)	PSC 6	Spare PCS 1
0X17	0134(0x5c)	23 O(27)	PSC 7	IBU
0X18	0143(0x63)	7 O(7)	PSC 8	D3U 7
0X19	0145(0x65)	3 O(3)	PSC 9	D3U 3
0X1a	0146(0x66)	4 O(4)	PSC 10	D3U 4
0X1b	0151(0x69)	5 O(5)	PSC 11	D3U 5
0X1c	0152(0x6a)	18 O(22)	PSC 12	SPU 10
0X1d	0154(0x6c)	8 O(10)	PSC 13	SPU 0
0X1e	0161(0x71)	9 O(11)	PSC 14	SPU 1
0X1f	0162(0x72)	10 O(12)	PSC 15	SPU 2
0X20	0164(0x74)	11 O(13)	PSC 16	SPU 3
0X21	0170(0X78)	12 O(14)	PSC 17	SPU 4
0X22	0207(0x87)	19 O(23)	PSC 18	SPU 11
0X23	0213(0x8b)	13 O(15)	PSC 19	SPU 5
0X24	0215(0x8d)	14 O(16)	PSC 20	SPU 6
0X25	0216(0x8e)	15 O(17)	PSC 21	SPU 7
0X26	0223(0x93)	16 O(20)	PSC 22	SPU 8
0X27	0225(0x95)	17 O(21)	PSC 23	SPU 9

Control Bus Memory Layout (Contd)

Control Bus Slot Address	Sack	Client_ID	PSC Number	Subunit/ Circuit Pack
0x0	0017(0x0f)	29 O(35)	—	TSI
0x1	0027(0x17)	24 O(30)	—	FBI
0X2	0033(0x1b)	25 O(31)	—	ALF0
0X3	0035(0x1d)	26 O(32)	—	ALF1
0X4	0036(0x1e)	27 O(33)	—	(ALF2 - Future)
0X5	0047(0x27)	28 O(34)	—	(ALF3 - Future)
0x6	—	30 O(36)	—	CSP
0X7	—	31 O(37)	—	FTERM H C
0X8	—	31 O(37)	—	FTERM L B

D3U Shared Memory Auxiliary Data Dump

DUMP SIZE	CLIENT_ID	ER_CODE_H	ER_CODE_L	RTN_ADR_H	RTN_ADR_L
D3UX	D3UX USTAT	D3UX STAT	D3UX ESR	D3UX CTL	D3UX EXR
WTT WD1	WTT WD2	WTT WD3	WTT WD4	WTT WD5	WTT WD6
WTT WD7	WTT WD8	WTT WD9	WTT WD10	WTT WD11	WTT WD12
WTT WD13	WTT WD14	WTT WD15	WTT WD16	WTT WD17	WTT WD18
WTT WD19	WTT WD20	WTT WD21	WTT WD22	WTT WD23	WTT WD24
WTT WD25	WTT WD26	WTT WD27	WTT WD28	WTT WD29	WTT WD30
WTT WD31	WTT WD32	WTT WD33	WTT WD34	WTT WD35	WTT WD36
WTT WD37	WTT WD38	WTT WD39	WTT WD40	WTT WD41	WTT WD42
WTT WD43	WTT WD44	WTT WD45	WTT WD46	WTT WD47	WTT WD48
WTT WD49	WTT WD50	WTT WD51	WTT WD52	WTT WD53	WTT WD54
WTT WD55	WTT WD56	WTT WD57	WTT WD58	WTT WD59	WTT WD60
WTT WD61	WTT WD62	WTT WD63	WTT WD64	WTT WD65	WTT WD66
WTT WD67	WTT WD68	TASK_ID	ERR_DATA1	ERR_DATA2	ERR_DATA3
ERR_DATA4	ERR_DATA5	ERR_DATA6	ERR_DATA7	ERR_DATA8	ERR_DATA9
ERR_DATA10	ERR_DATA11	ERR_DATA12	ERR_DATA13	ERR_DATA14	ERR_DATA15
STACK WD1	STACK WD2	STACK WD3	STACK WD4	STACK WD5	STACK WD6
STACK WD7	STACK WD8	STACK WD9	STACK WD10	STACK WD11	STACK WD12
STACK WD13	STACK WD14	STACK WD15	STACK WD16	STACK WD17	STACK WD18

DUMP SIZE—Report Type and Block Size
Octal 00010344

CLIENT_ID—Contains the suspect client ID.
(See Control Bus Memory Layout.)

ER_CODE_H—High 8-bit of a 32-bits Error Code

Bit 0-7 = Contains the software issue number

ER_CODE_L—Low 24-bit of a 32-bits Error Code

Bit 0-11 = Contains the code (See Error Codes and Class Layout for values.)
12-15 = Contains the error class (See Error Codes and Class Layout for values.)
16-23 = Number of 32 bit error words reported/found in Auxiliary Data Dump. The remainder is stack information (up to maximum number of error words).

RTN_ADR_H—Pack Type

Bit 0-8 = D3U pack type = 1

RTN_ADR_L—Low 24-Bits of Failing Address

Bit 0-23 = Failing Address

D3UX Subunit—D3U Subunit Data

Bit 0-8 = D3U unit member number (between 0 and 7) (UTMEM)
9-11 = D3U Unit type = 0
12-23 = Unused

D3UX USTAT—D3U Software Status Register

See *XTSI D3U Registers* for Bit Layouts

D3UX STAT—D3U Status Register

See *XTSI D3U Registers* for Bit Layouts

D3UX ESR—D3U Error Source Register

See *XTSI D3U Registers* for Bit Layouts

D3UX CTL— D3U Control Register

See *XTSI D3U Registers* for Bit Layouts

D3UX EXR—D3U Exercise Register

See *XTSI D3U Registers* for Bit Layouts

WTT WDx—Work Task Table (1-68)

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits data words.

NOTE:
WTT WD68 (Work task table 68) bits 0-7 contain the firmware issue number.

TASK_ID—Task Executing at Time Of Interrupt

Bit 0-7 = Task index
8-15 = Switch generic number
16-23 = Switch load number

Octal Value	Description
00	DS1 FDL (Group 1 Index)
12	DS2 Alarm (Group 2 Index)
13	DS3 Alarm (Group 2 Index + 1)
14	Feature (Group 2 Index +2)
15	XTC_Interface (Group 2 Index + 3)
24	PCC TX (Group 3 Index)
25	DS1 Parse (Group 3 Index + 1)
36	DS1 Alarm (Group 4 Index)
37	DS1 NE PM (Group 4 Index + 1)
40	DS1 FE PM (Group 4 Index + 2)
41	PCC_TO (Group 4 Index + 3)
42	DS3 NE PM (Group 4 Index + 4)
43	PBSA (Group 4 Index + 5)
44	TTDL XMIT (Group 4 Index + 6)
45	Audits (Group 4 Index + 6)

ERR_DATAyy—Specific Error Information for a Particular Fault

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits

STACK WDzz—First 12-Words in the PSC Stack

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits data words.

F-Level XTC Software Error Code (Octal)

Value	Description
1	XTC main scheduler loop error code
2	Tried to EXEC an invalid PID error code
3	Process being EXEC is in a invalid state error code
4	Signal system call error code
5	Wait system call error code
6	Diagnostic macro is already in-progress error code
7	Main maintenance buffer overflow
10	Tried to EXEC an invalid process
11	Macro process EXEC error
12	Macro RAM audit error
13	Macro process queue error
14	Macro process busy error
15	Error in PCIS table in shared memory and GRAM copy
20	Disk job timeout
21	Disk drive interval error
22	Sync error
23	Test error
24	Disk drive in invalid state
25	PSC polling error
26	Error in PSC get word routine
27	Error in calculating PID buffer
30	Controller 0 active/standby state error
31	Controller 1 active/standby state error
32	Controller 0 or 1 active/standby state error
33	PSC heartbeat error
34	Error protection switch update process
35	Error PSC Send Routine
36	Error in writing diagnostic maintenance buffer in operational load

F-Level XTC Software Error Code [(Octal) Contd]

Value	Description
40	Read client register/memory error code
41	Read register error code
42	Write client register/memory error code
43	Write 32-bit register error code
44	Write 24-bit register error code
45	Maintenance buffer overflow error code
46	Macro process buffer overflow
47	Group 1 macro error
50	Group 2 macro error
51	Read maintenance buffer pointer error code
52	Maintenance buffer update error
53	Read XTC micro-RAM error code
54	Write XTC micro-RAM error code
55	XTC—invalid diagnostic test group number
56	Diagnostic request when not divorced
57	Invalid file descriptor number
60	Invalid operational macro received
61	Send high 14-bits of flash address error
62	Send low 16-bits of flash address error
63	Error in loading file in DRAM
64	Error in disk data write
65	Error in write disk file
66	XTC pump failed
67	Bad current process address
70	Macro process is not running
71	PSC polling process is not running
73	Error in starting initialization address
74	Error in end initialization address
76	Error found in file descriptor table interrupt routine
200-377	Reserved for CSP call processing

F-Level XTC Software Error Code [(Octal) Contd]

Value	Description
400	Both the PSO and SBO bits were set in the search TSM order
401	Used in set up and take down 1- and 2-way connection to indicate that Bit 23 (ERINT) is set in the EXEC Interrupt Register
402	Error in clamping PSC interrupt routine
403	Error in unclamping PSC interrupt routine
404	Error in USEC interrupt routine
405	Error in PSC diagnostic with Helper interrupt routine
406	Error in USEC protection switch update interrupt routine
407	Error in copy flash or copy disk interrupt routine
410	PSC pump error
411	Error in PSC in-service interrupt routine
412	Bad set software breakpoint order received or invalid BP context
413	Flash operation is in-progress
414	Flash read error
415	Read compelled alarm report error
416	PSC send operational command error
417	PSC send macro command error
420	SCANPT out-of-range client ID
421	SPU bypass Map Audit error
422	SPU iPCC Map Audit error
423	SPU bypass-iPCC Map Update error
424	USEC Audit detected data error
425	TSXR GRAM Audit Map error
426	TSXR-Inverse GRAM Audit Map error
427	TSXR and TSI fabric memory incorrect

F-Level XTC Software Error Code [(Octal) Contd]

Value	Description
430	Read of A/B scan point-invalid PSC number
431	Error in protection switch state (MSC1 = inconsistent client ID)
432	PM read data command error
433	PM reset DS1 command error
434	PM protection switch command error
435	FLtuple, flash access semaphore used
436	FLtuple, no JEDEC tuple code found
437	FLtuple, invalid MFG ID code found
440	FLreset, Flash access semaphore used
441	FLreset, invalid MFG ID code found
442	FLreset, invalid MFG ID code found
443	FLreadlw, Flash access semaphore used
444	FLreadlw, invalid MFG ID code found
445	FLwritelw, Flash access semaphore used
446	FLwritelw, invalid MFG ID code found
447	FLwritelw failed
450	FLblkerase, Flash access semphore used
451	FLblkerase, Invalid MFG ID code found
452	FLblkerase failed
453	FLblklock, Flash access semphore used
454	FLblklock, invalid MFG ID code found
455	INTEL failed block lock at CSR check
456	INTEL failed block lock at BSR check
457	FLitlVppon, Flash access semaphone used

F-Level XTC Software Error Code [(Octal) Contd]

Value	Description
460	FLitVppon failed due to timeout
461-467	Reserved
470-473	Reserved
474	Nailup queue count mismatches
475	Nailup queue overflow or pointer corruption detected
476	Invalid digroup number
477	Invalid client ID
500	Queue order/macro received while macro is already running
501	Channel does not correspond to first DS0 of that digroup
502	TSI memory write failed
503	Error in DGintfail
504	Error in DGintend
505	TSI memory write blocked by search
506	Attempting to nailup/teardown invalid SPU client ID/XTSI-member combination
507	Error in file version query interrupt command
510	Corruption found in GLtsxr_strt translation table for a non-nailed up SPU
511	Corruption found in Translation Memory (TRXM) for a non-nailed up SPU
512	Corruption found in GLtsxr_addrs SPU TS look-up table

F-Level XTC Software Error Code [(Octal) Contd]

Value	Description
513	One or more of the 96 memory words associated with the nail up for the given Digroup have been corrupted
514	P2 Time Slot Memory has bit 12 set a non-nailed up timeslot
515	P2-P3 GRAM Inverse table entry values are not all consistent for an associated SPU digroup that is not nailed up
516	Error in writing the IBU quick queue at interrupt level
517	Error in update CSP buffer command, no bit set
520	Error in CSP buffer update, buffer out of range
521	Error in read CSP buffer command, either no bit set or more than one bit set
522	Error in read CSP buffer, buffer out of range
523	Error in write PCIS 0/1 interrupt routine
524	Error in read PCIS 0/1 interrupt routine
525	Error in CSP pump interrupt routine
526	Error in INXRAMCONF interrupt routine
527	Error in audit STS on CSP circuit pack memory
530	Error in PCIS interrupt routine
531	Error in CSP START/STOP interrupt routine
532	IBU buffer pointers out of range

IBU Shared Memory Auxiliary Data Dump

DUMP SIZE	CLIENT_ID	ER_CODE_H	ER_CODE_L	RTN_ADR_H	RTN_ADR_L
IBUX	IBUX USTAT	IBUX STAT	IBUX ESR	IBUX CTL	IBUX EXR
WTT WD1	WTT WD2	WTT WD3	WTT WD4	WTT WD5	WTT WD6
WTT WD7	WTT WD8	WTT WD9	WTT WD10	WTT WD11	WTT WD12
WTT WD13	WTT WD14	WTT WD15	WTT WD16	WTT WD17	WTT WD18
WTT WD19	WTT WD20	WTT WD21	WTT WD22	WTT WD23	WTT WD24
TASK_ID	ERR_DATA1	ERR_DATA2	ERR_DATA3	ERR_DATA4	ERR_DATA5
ERR_DATA6	ERR_DATA7	ERR_DATA8	ERR_DATA9	ERR_DATA10	ERR_DATA11
.	.	.	.	.	.
.	.	.	.	.	.
ERR_DATA72	ERR_DATA73	ERR_DATA74	ERR_DATA75	ERR_DATA76	ERR_DATA77

DUMP SIZE—Report Type and Block Size

Octal 000012344

Bit 0 = Tag
1-8 = Output size = 114
9-12 = Unit type = 10

Client-ID—Contains the client ID.
(See Control Bus Memory Layout.)

ER_CODE_H—High 8-bit of a 32-bits Error Code

Bit 0-7 = Contains the software issue number

ER_CODE_L—Low 24-bit of a 32-bits Error Code

Bit 0-11 = Contains the code (See Error Codes and Class for values.)
12-15 = Contains the error class (See Error Codes and Class for values.)
16-23 = Number of 32 bit error words reported/found in Auxiliary Data Dump. The remainder is stack information (up to maximum number of error words).

RTN_ADR_H—Pack Type

Bit 0-8 = IBU pack type = 4

RTN_ADR_L—Low 24-Bits of Failing Address

Bit 0-23 = Failing Address

IBUX Subunit—IBUX Subunit Data

Bit 0-8 = IBUX unit member number (0) (UTMEM)
9-11 = IBUX Unit type = 2
12-23 = Unused

IBUX USTAT—IBU Software Status Register

See *XTSI IBU Registers* for Bit Layouts

IBUX STAT—IBU Status Register

See *XTSI IBU Registers* for Bit Layouts

IBUX ESR—IBU Error Source Register

See *XTSI IBU Registers* for Bit Layouts

IBUX CTL— IBU Control Register

See *XTSI IBU Registers* for Bit Layouts

IBUX EXR—IBU Exercise Register

See *XTSI IBU Registers* for Bit Layouts

WTT WDx—Work Task Table (1-68)

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits data words.

TASK_ID—Task Executing at Time Of Interrupt

Octal Value	Description
00	IBU iPCC (Group 1 Index)
01	IBU Bypass (Group 1 Index+ 1)
12	XTC_Interface (Group 2 Index)
13	IBU ET109 (Group 2 Index + 1)
14	IBU inband (Group 2 Index + 2)
15	Audit (Group 2 Index + 3)

ERR_DATAyy—Specific Error Information for a Particular Fault

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits

STACK WDzz—First 12-Words in the PSC Stack

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits data words. These 32-bits words contain the following:

Miscellaneous Error Source Auxiliary Data Dump

DUMP SIZE   CLIENT_ID   0........0   0........0   0........0   FAULT_TYPE

DUMP SIZE—Report Type and Block Size
Octal 00005014

CLIENT_ID—Contains the suspect client ID (See Control Bus Memory for bit layouts.)

FAULT_TYPE—for development only

PSC Auxiliary Data Dump

DUMP SIZE (SUBUNIT)	CLIENT_ID	DATA2	DATA3	DATA4	FAULT_TYPE
D3U0	D3U0 USTAT	D3U0 STAT	D3U0 ESR	D3U0 CTL	D3U0 EXR
D3U1	D3U1 USTAT	D3U1 STAT	D3U1 ESR	D3U1 CTL	D3U1 EXR
D3U2	D3U2 USTAT	D3U2 STAT	D3U2 ESR	D3U2 CTL	D3U2 EXR
D3U3	D3U3 USTAT	D3U3 STAT	D3U3 ESR	D3U3 CTL	D3U3 EXR
D3U4	D3U4 USTAT	D3U4 STAT	D3U4 ESR	D3U4 CTL	D3U4 EXR
D3U5	D3U5 USTAT	D3U5 STAT	D3U5 ESR	D3U5 CTL	D3U5 EXR
D3U6	D3U6 USTAT	D3U6 STAT	D3U6 ESR	D3U6 CTL	D3U6 EXR
D3U7	D3U7 USTAT	D3U7 STAT	D3U7 ESR	D3U7 CTL	D3U7 EXR
SPU0	SPU0 USTAT	SPU0 STAT	SPU0 ESR	SPU0 CTL	SPU0 EXR
SPU1	SPU1 USTAT	SPU1 STAT	SPU1 ESR	SPU1 CTL	SPU1 EXR
SPU2	SPU2 USTAT	SPU2 STAT	SPU2 ESR	SPU2 CTL	SPU2 EXR
SPU3	SPU3 USTAT	SPU3 STAT	SPU3 ESR	SPU3 CTL	SPU3 EXR
SPU4	SPU4 USTAT	SPU4 STAT	SPU4 ESR	SPU4 CTL	SPU4 EXR
SPU5	SPU5 USTAT	SPU5 STAT	SPU5 ESR	SPU5 CTL	SPU5 EXR
SPU6	SPU6 USTAT	SPU6 STAT	SPU6 ESR	SPU6 CTL	SPU6 EXR
SPU7	SPU7 USTAT	SPU7 STAT	SPU7 ESR	SPU7 CTL	SPU7 EXR
SPU8	SPU8 USTAT	SPU8 STAT	SPU8 ESR	SPU8 CTL	SPU8 EXR
SPU9	SPU9 USTAT	SPU9 STAT	SPU9 ESR	SPU9 CTL	SPU9 EXR
SPU10	SPU10 USTAT	SPU10 STAT	SPU10 ESR	SPU10 CTL	SPU10 EXR
SPU11	SPU11 USTAT	SPU11 STAT	SPU11 ESR	SPU11 CTL	SPU11 EXR
IBU0	IBU0 USTAT	IBU0 TDR	IBU0 ESR	IBU0 CTL	IBU0 EXR
0..........0	0..........0	0..........0	0..........0	0..........0	0..........0
0..........0	0..........0	0..........0	0..........0	0..........0	0..........0
0..........0	0..........0	0..........0	0..........0	0..........0	0..........0

DUMP SIZE—Report Type and Block Size
Octal 00006454

CLIENT_ID—contains the Client ID

Bit 0-4 = Contains the suspect client ID (See Control Bus Memory Layout)

DATA2 - DATA3—May contain fault isolation data (for development only).

FAULT_TYPE—for development only

D3UX Subunit, SPUX Subunit and IBU0 Subunit—contains the following format:

Bit 0-8 = Unit member number (UTMEM)
For D3U - Member number is between 0 - 7
For SPU - Member number is between 0 - 11
For IBU - Member number is 0
9-11 = Unit type
0 - D3U
1 - SPU
2 - IBU
12-23 = Unused

D3UX USTAT—D3U Hardware Status Register

See *XTSI D3U Registers* for Bit Layouts

D3UX STAT—D3U Software Status Register

See *XTSI D3U Registers* for Bit Layouts

D3UX ESR—D3U Error Source Register

See *XTSI D3U Registers* for Bit Layouts

D3UX CTL— D3U Control Register

See *XTSI D3U Registers* for Bit Layouts

D3UX EXR—D3U Exercise Register

See *XTSI D3U Registers* for Bit Layouts

SPUX USTAT—SPU Hardware Status Register

See *XTSI SPU Registers for Bit Layouts*

SPUX STAT—SPU Software Status Register

See *XTSI SPU Registers for Bit Layouts*

SPUX ESR—SPU Error Source Register

See *XTSI SPU Registers for Bit Layouts*

SPUX CTL—SPU Control Register

See *XTSI SPU Registers for Bit Layouts*

SPUX ESR—SPU Exercise Register

See *XTSI SPU Registers for Bit Layouts*

IBU0 USTAT—IBU Hardware Status Register

See *XTSI IBU Registers for Bit Layouts*

IBU0 TDR—IBU Software Status Register

See *XTSI IBU Registers for Bit Layouts*

IBU0 ESR—IBU Error Source Register

See *XTSI IBU Registers for Bit Layouts*

IBU0 CTL—IBU Control Register

See *XTSI IBU Registers for Bit Layouts*

IBU0 ESR—IBU Exercise Register

See *XTSI IBU Registers for Bit Layouts*

PSC Circuit Pack Error Source Auxiliary Data Dump

NOTE:
In this layout, the word "unit" is replaced with either D3U, SPU or IBU.

DUMP SIZE	CLIENT_ID	0........0	0........0	0........0	FAULT_TYPE
UNIT	unit USTAT	unit STAT	unit ESR	unit CTL	unit EXR

DUMP SIZE—Report Type and Block Size
Octal 000010030 (D3U) or
Octal 000011030 (SPU)
Octal 000012030 (IBU)

CLIENT_ID—Contains the suspect client ID.
(See Control Bus Memory Layout.)

FAULT_TYPE—for development only

UNIT—Client Subunit

Bit 0-8 = Unit member number (UTMEM)

For D3U - Member number is between 0 - 7

For SPU - Member number is between 0 - 11

For IBU - Member number is 0

9-11 = Unit type

0 - D3U

1 - SPU

2 - IBU

12-23 = Unused

unit USTAT—D3UX/SPUX/IBUX Software Status

(See XTSI D3U/SPU/IBU Registers for bit layouts)

unit STAT—D3UX/SPUX/IBUX Hardware Status

(See XTSI D3U/SPU/IBU Registers for bit layouts)

unit ESR—D3UX/SPUX/IBUX Error Source Register

(See XTSI D3U/SPU/IBU Registers for bit layouts)

unit CTL—D3UX/SPUX/IBUX Control Register

(See XTSI D3U/SPU/IBU Registers for bit layouts)

unit EXR—D3UX/SPUX/IBUX Exercise Register

(See XTSI D3U/SPU/IBU Registers for bit layouts)

PSC Error Codes and Class Layout (Octal)

Code	Class *	Description
PSC Common Error Codes		
1	0	BP states do not match number of BPs active
2	1	D3U read offset into D3U message queue is out of bound
3	1	End routine was called by executive
4	1	Bus or parity error was detected
5	1	Addressing error was detected
6	1	Illegal instruction was executed
7	1	Divide by zero attempted
10	1	Software watchdog timer was not refreshed on time
11	1	Audit task was not executed on time
12	1	An undefined error code was passed to the error handler
13	3	Program checksum audit failure
14	1	CBI task error
15	1	Attempt made to send audit message
16	1	An ESR bit was set. This error is not generated by any of the SW module but is called by ISR routine when any ESR bit is set undefined interrupt
17	1	Undefined interrupt
20	2	D3U message queue error
21	2	XTC message queue error
22	2	Invalid report type on queue

* See Legend at end of table.

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
PSC Common Error Codes (Contd)		
23	2	Invalid subopcode on queue
24	2	Out-of-sequence on queue
25	2	Invalid priority message received
26	3	An audit of working task table failed. WTT is corrupted.
27	2	Invalid trap, unknown BP is reached
30	4	FW processor sanity test fail (non-error) when the PSC was configured as a spare. No audit message should be sent.
31	1	An audit of WTT failed. The task was not running at the required frequency.
D3U Specific Error Codes		
240	2	PBSA detected all bad configure
241	0	Corrupted PCC/FDL message queue
242	0	An invalid message has been received, either too short or too long, over the FDL
243	0	PCC_stores does not match configuration, alarm, initialization or data
244	0	FDL information audit fail
245	0	LB message invalid
246	0	FEAC audit failed
247	0	DS3 BER 107 detected

* See Legend at end of table.

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
D3U Specific Error Codes (Contd)		
250	0	Invalid equipment status received from PUFR
251	0	An invalid DS1 number
252	1	D3U not initialized yet
253	1	FDL register underflow
254	1	FDL register overflow
255	1	Configuration data audit failed
256	1	No EOF on FDL read message
257	1	Tx buffer contains an unknown message
260	1	DS1/DS3 hardware registers are corrupted
261	1	DS1/DS3 write-read sanity audit failure
262	1	CPU/DS1/DS3 static register/bit audit failure
263	1	DPA software audit failure
264	1	Corrupt message type
265	1	PBSA detected a bad configuration
266	1	PBSA internal audit failed
267	1	DS3 alarm task/audit failure
270	1	DS3 invalid yellow action requested
271	1	DS3 invalid alarm value passed to alarm report
272	1	DS3 invalid official alarm value found in the official alarm state variable
273	1	DS3 invalid BOC requested to transmit
274	2	PBSA detected paddleboard failure
275	3	DS3 yellow alarm option is corrupted
276	3	D3U configuration number is corrupted

* See Legend at end of table.

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
D3U Specific Error Codes (Contd)		
277	3	DS1 frame format option is corrupted
300	3	DS3 application type is corrupted
301	3	Line build-out option is corrupted
302	3	Software configuration data structures are corrupted
303	0	DPA alarm or data failure
304	0	DS1 alarm data failure
305	1	DS1 yellow arguments bad
306	1	DS1 state machine return code
307	0	LB PM report data structure
310	N/A	Error in the PM transmit state of FDL
311	1	Shared memory audit error code
312	2	Bad arguments in release 2 clear count order
313	0	Invalid DS1 PM version
314	3	The configuration data structure checksum check failed, indicating R2 PM configuration structure is corrupt
315	0	DS1 p.m. audit failure
316	4	Bad pack type in version string
317	1	A/B and IBSS configuration data should be mutually exclusive
320	1	Invalid pointer to T1 audit array
321	1	Signaling interface error
322	1	Signaling interface audit failure
323	1	Back plane signaling bit parity error
324	1	DS1 framing message received when spare error
325	4	Bad PCIS usage value

* See Legend at end of table.

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
SPU Specific Error Codes		
400	1	PCC audit failure requiring soft initialization
401	3	PCC audit failure requiring hard initialization
402	1	First txinit not received, SPU not initialized yet
403	3	SPU configuration number is invalid number
404	1	Possible txinit message lost during restore or protection switch configuration and pack ID inconsistent
405	1	Timeslot mapping ptr corrupted
406	3	Configuration data structure is corrupted as determined by a checksum failure
407	1	TrueVoice configuration toggle is corrupted
410	1	TrueVoice configuration types is corrupted
411	3	SPU configuration iterations is corrupted
412	1	One or more SPU hardware registers are corrupted
413	1	CPU audit failure
414	1	ECP/R4 static register/bit audit failure
415	1	TrueVoice (page 0) static register/bit audit failure
416	1	PF static register/bit audit failure
417	1	AVC static register/bit audit failure

* See Legend at end of table.

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
SPU Specific Error Codes		
420	1	Tag static register/bit audit failure
421	1	Error for eT109 test failed
422	1	Error for eT109 audit failed
423	1	Error for eT109 phase to test
424	1	EPROM checksum audit failed
425	0	eT109 disable order received
426	0	eT109 disable timer fired
427	1	et109 status error
430	1	et109 restart requests error
431	1	Mismatch between ecp_max register global and ECPR4 hardware version

* See Legend at end of table.

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
IBU Specific Error Codes		
1000	1	O(15) order is for MF only
1001	1	Invalid DSP Message Type Received
1002	1	DSP Interface Task Error Report Worklist Queue Overflowed
1003	1	Miscellaneous Scan Point Task Worklist Queue Overflowed
1004	1	Audit Task Worklist Overflowed
1005	1	X-mit Orders Task Worklist Queue Overflowed
1006	1	RTB Task Worklist Queue Overflowed
1007	1	A DSP Client Task Worklist Control Block is corrupt
1010	1	Invalid order
1011	1	Invalid message
1012	0	Invalid order of messages
1013	1	Invalid channel number
1014	1	Audit of struct failed
1015	0	Lost message
1016	1	Corrupt data
1017	0	Last bit set incorrectly

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
IBU Specific Error Codes (Contd)		
1020	0	Digit timer
1021	0	Completition timer
1022	1	Invalid DSP number
1023	1	RCV/XMT QMQ Read offset bad
1024	1	RCV/XMT QMQ Write offset bad
1025	1	Type in table is corrupt
1026	1	DSP did not receive final error report in time
1027	3	Fatal DSP error code rcvd
1030	1	EXEC buffer read pointer
1031	1	EXEC buffer write pointer
1032	1	IBU buffer read pointer
1033	1	IBU buffer write pointer
1034	1	Invalid queue address
1035	1	Audit of global variables failed
1036	1	DSP SPST Message Type Bad
1037	1	DSP SPST Channel Bad

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
IBU Specific Error Codes (Contd)		
1040	1	FPGAs INIT stuck low?
1041	1	FPGA INIT/PROG stuck hi?
1042	1	INIT low for > 5ms after PROG
1043	1	CRC error detected in bitstream or FPGA config otherwise failed
1044	1	Audit CPU variables
1045	3	Fatal ROM error, Vector Table not accessible
1046	3	Fatal ROM error, DRAM not accessible
1047	3	Fatal ROM error, Queue pointers not accessible
1050	3	Fatal ROM error, IBU/XTC queues not accessible
1051	1	Machine Check Exception
1052	1	Data Storage Exception
1053	1	Instruction Storage Exception
1054	1	External Exception
1055	1	Alignment Exception
1056	1	Program Exception
1057	1	Floating Point Unavailable Exception

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
IBU Specific Error Codes (Contd)		
1060	1	System Call Exception
1061	1	Trace Exception
1062	1	Floating Point Assist Exception
1063	1	NOT DEFINED Exception
1064	1	Software Emulation Exception
1065	1	Instruction TLB Miss Exception
1066	1	Data TLB Miss Exception
1067	1	Instruction TLB Error Exception
1070	1	Data TLB Error Exception
1071	1	Data Breakpoint Exception
1072	1	Instruction Breakpoint Exception
1073	1	Peripheral Breakpoint Exception
1074	1	Non Maskable Development Point Exception
1075	3	dgn_dsp_pump() failed
1076	3	DSP Checksum Audit has recieved a bad or unexpected report from DSP
1077	3	DSP Checksum Audit has found a checksum mismatch

PSC Error Codes and Class Layout (Octal) (Contd)

Code	Class *	Description
IBU Specific Error Codes (Contd)		
1100	4	DSP Checksum Audit has found two bad checksums in a row
1101	3	dsp_pump() failed
1102	3	local ram chip select failure
1103	3	shared ram chip select failure
1104	3	dspColdStartMemTst() failure from fw_main()
1105	3	dspColdBoot() failure from fw_main()
1106	1	failure during dsp_digit_rx
1107	1	failure during rx_audit

Legend:

The error class and description are as following:

0 Base level message
1 Soft initialization
2 Implicates the XTC
3 Hard initialization
4 Hard reset

PUPHDATA-XTSI (Phase 2, 3, or 4)

NOTE:
TTY request **OP:ERAPDATA PUPHDATA:MFNUM *a*!**
a= MFNUM or range of MFNUM for Phase 2, 3, or 4

WORD 0 WORD 1 WORD 2 WORD 3 WORD 4 WORD 5
WORD 6 WORD 7

Words 0-3 = Controller 0
Words 4-7 = Controller 1

WORD 0 (Controller 0) and WORD 4 (Controller 1)

Bit 0-2 = Boot Task Acknowledgement Code (in octal)
- 0 - A boot task has been spawned
- 1 - A spawned task did not complete
- 2 - Controllers booted duplex
- 3 - One controller removed
- 4 - Both controllers failed
- 5 - Request error
- 6 - No boot task requested
- 7 - PMOS returned fail

3-5 = Controller Request Code
- 0 - Do not boot XTSI frame
- 1 - Hard controller fault (HDWRLEV 4)
- 2 - Soft controller fault (HDWRLEV 1, 2 OR 3)
- 3 - Remove controller

WORD 0 (Controller 0) and WORD 4 (Controller 1) (Contd)

Bit 6-9 = Request Data (Octal)
- 0 = XTSI frame unequipped
- 1 = XTSI frame in growth state
- 2 = Controller in zap table
- 3 = Controller in zero start table
- 4 = Controller in babbling bus table
- 5 = Controller is out-of-service
- 6 = Controller boot level is hardware level 4
- 7 = Controller normal
- 10 = TSI duplex failure

10 = Final Configuration Request
- 0 = Controller removed
- 1 = Controller restored

11-16 = Failing Data Code (octal)
- 0 = ATP (valid for all HDWRLEVs), or Controller already removed prior to phase (only valid if HDWRLEV 1, 2, 3)
- 1 = MAINCOMM pulse on bus failure
- 2 = Peripheral unit bus loop failure
- 3 = IPUB out-of-service failure
- 4 = Topic failed to restore controller
- 5 = Post topic restore access test failure
- 6 = PMOS failed to schedule topic restore
- 7 = PMOS failed to schedule topic remove
- 10 = Frame rejected macro
- 11 = PMOS failed to schedule macro parallel polling
- 12 = Parallel polling macro timeout
- 13 = Frame failed macro
- 14 = Error occurred while polling macro
- 15 = XTSI status register failure
- 16 = Read file status query results in: invalid file or no file found

WORD 0 (Controller 0) and WORD 4 (Controller 1) (Contd)

Bit 11-16 = Failing Data Code (octal (Contd))
17 = GESR (Global RAM ESR) bit(s) set
20 = PCM babbling fault
21 = Program counter is in ROM
22 = Checksum not equal
23 = Network clock failure
17-22 = XTSI unit type equal TSI unit type = octal 5

WORD 1 (Controller 0) and WORD 5 (Controller 1)

Bit 0-6 = XTSI member number
7-12 = Failed controller macro identification code (in octal)
1 = Load file macro
2 = Flash pump macro
3 = Initialize TSI translation RAM macro
4 = Initialize TSI RAM macro
5 = Initialize busy/idle memory macro
6 = Initialize ALF (A-Link Interface) translation RAM macro
7 = Update MRAM (MICRO-RAM) macro
10 = Hard initialize macro
11 = Verify controller hashsum macro
12 = Update other RAM macro
13 = Unclamp PSC macro
14 = Clamp PSC macro
15 = Transmission initialization macro
16 = Pump D3U macro
20 = USEC protection switch update macro
21 = Nailup macro

WORD 2 (Controller 0) and WORD 6 (Controller 1) are not used.

WORD 3 (Controller 0) and WORD 7 (Controller 1) are not used.

Restore XTSI Controller Fail Data

RST: XTSI *a* **CONTR** *b* **ABORTED FAILDATA=***c*

Where: *a* = TSI member number
b = Controller number
c = Failing data
Bit 0-3 = Message Dispenser Fail Reason
- 0 = Invalid macro parameters passed into procedure
- 1 = Message dispenser request fail
- 2 = PMOS task hold timeout
- 3 = Macro response not ready
- 4 = Message dispenser request was successful but no task hold was requested
- 5 = Macro response ready

4-5 = Unused
6-12 = File number (valid range 0-127)
15-16 = Not used
17 = Message dispenser pass/fail indicator
- 0 = Message dispenser failure or peripheral order sent
- 1 = Message dispenser successful but macro response indicated a failure

18-23 = Configuration return code (Octal)
- 0 = XTSI controller pump/fabric initialization successful
- 1 = XTSI controller pump failed—Read file status order failed
- 2 = XTSI controller pump failed—Miscellaneous error macro failed
- 3 = XTSI controller pump failed—Flash pump macro failed
- 4 = XTSI fabric initialization failed—TSI status register error

Bit 18-23 = Configuration return code [(Octal) Contd]

5 = XTSI fabric initialization failed—TSI translation RAM macro failed
6 = XTSI fabric initialization failed—TSI time slot memory macro failed
7 = XTSI fabric initialization failed—ALF busy/idle memory macro failed
10 = XTSI fabric initialization failed—ALF translation RAM macro failed
11 = XTSI controller pump failed—Invalid reply (all zeroes)
12 = XTSI update program RAM failed—Update failure
13 = XTSI update program RAM failed—Hard initialization failure
14 = XTSI update program RAM failed—Hashsum failure
15 = XTSI update other RAM failed—Update RAM failure
16 = XTSI update other RAM failed—GESR (global ram error source register) BIT(s) SET
17 = XTSI update failed—Internal error
20 = XTSI update failed—Lock step failed
21 = XTSI pump failed—First checksum failed
22 = XTSI pump failed—Recalculated checksum failed
23 = XTSI update program memory—Update macro failed
24 = XTSI access test failed
25 = XTSI pump failed—Internal error
26 = XTSI update failed—Controller 0 checksum not equal controller 1 checksum
27 = XTSI update failed—One controller indicates no file found; the other controller indicates file found IN_FLASH
30 = XTSI pump failed—Disk job
31 = XTSI pump failed—Empty file
32 = XTSI pump failed—Control bus copy

Continued on next page

Bit 18-23 = Configuration return code [(Octal) Contd]

33 = XTSI pump failed—Transfer
34 = XTSI pump failed—File error
35 = XTSI SPU tear-down Nailup success
36 = XTSI SPU tear-down Nailup maintenance buffer read failed
37 = XTSI SPU tear-down Frame failed nailup macro
40 = XTSI Controller pump CSP failed—Read file status order failed
41 = XTSI Controller pump CSP failed—Miscellaneous error macro failed
42 = XTSI Controller pump CSP failed—Flash pump macro failed
43 = XTSI Pump CSP failed—Internal error
44 = XTSI initialize CSP memory failed

SPU Shared Memory Auxiliary Data Dump

DUMP SIZE	CLIENT_ID	ER_CODE_H	ER_CODE_L	RTN_ADR_H	RTN_ADR_L
SPUX	SPUX USTAT	SPUX STAT	SPUX ESR	SPUX CTL	SPUX EXR
WTT WD1	WTT WD2	WTT WD3	WTT WD4	WTT WD5	WTT WD6
WTT WD7	WTT WD8	WTT WD9	WTT WD10	WTT WD11	WTT WD12
WTT WD13	WTT WD14	WTT WD15	WTT WD16	WTT WD17	WTT WD18
WTT WD19	WTT WD20	WTT WD21	WTT WD22	WTT WD23	WTT WD24
WTT WD25	WTT WD26	WTT WD27	TASK_ID	ERR_DATA1	ERR_DATA2
ERR_DATA3	ERR_DATA4	ERR_DATA5	ERR_DATA6	ERR_DATA7	ERR_DATA8
ERR_DATA9	ERR_DATA10	ERR_DATA11	ERR_DATA12	ERR_DATA13	ERR_DATA14
.	.	.	.	.	.
.	.	.	.	.	.
ERR_DATA69	ERR_DATA70	ERR_DATA71	ERR_DATA72	ERR_DATA73	ERR_DATA74

DUMP SIZE—Report Type and Block Size

Octal 000011344 (SPU)

Bit 0 = Tag
1-8 = Output size = 114
9-12 = Unit type = 9

CLIENT_ID—Contains the suspect client ID.
(See Control Bus Memory Layout.)

ER_CODE_H—High 8-bit of a 32-bits Error Code

Bit 0-7 = Contains the software issue number

ER_CODE_L—Low 24-bit of a 32-bits Error Code

Bit 0-11 = Contains the code (See Error Codes and Class for values.)
12-15 = Contains the error class (See Error Codes and Class for values.)
16-23 = Number of 32 bit error words reported/found in Auxiliary Data Dump. The remainder is stack information (up to maximum number of error words).

RTN_ADR_H—Pack Type

Bit 0-8 = SPU pack type = 2

RTN_ADR_L—Low 24-Bits of Failing Address

Bit 0-23 = Failing Address

SPUX Subunit—SPUX Subunit Data

Bit 0-8 = SPU unit member number (between 0 and 11) (UTMEM)
9-11 = SPU Unit type = 1
12-23 = Unused

SPUX USTAT—SPU Software Status Register

See *XTSI SPU Registers* for Bit Layouts

SPUX STAT—SPU Status Register

See *XTSI SPU Registers* for Bit Layouts

SPUX ESR—SPU Error Source Register

See *XTSI SPU Registers* for Bit Layouts

SPUX CTL— SPU Control Register

See *XTSI SPU Registers* for Bit Layouts

SPUX EXR—SPU Exercise Register

See *XTSI SPU Registers* for Bit Layouts

WTT WDx—Work Task Table (1-68)

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits data words.

TASK_ID—Task Executing at Time Of Interrupt

Octal Value	Description
00	SPU iPCC (Group 1 Index)
01	SPU Bypass (Group 1 Index+ 1)
12	XTC_Interface (Group 2 Index)
13	SPU ET109 (Group 2 Index + 1)
14	SPU inband (Group 2 Index + 2)
15	Audit (Group 2 Index + 3)

ERR_DATAyy—Specific Error Information for a Particular Fault

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits

STACK WDzz—First 12-Words in the PSC Stack

These words are only useful for development. Each row represents four 32-bits data words packed into six 24-bits data words. These 32-bits words contain the following:

XTSI Critical Register Layout (FLEV, IREG)

NOTE:
The F-level layout does not display columns 7 and 8 and 7............7 are replaced with 5............5.

CSTATUS	STATR	MADATA	FSTATUS0	FSTATUS1	CESR	0............0	0............0
PEST	CNTL	EXCNTLSTATL	EXCNTLSTATH	EXESR	GESR	0............0	0............0
GCNTL	GADDR0	GADDR1	EXINTR	CIAESCL	EXSANTIM	0............0	0............0
EXSTKBNDL	EXSTKBNDH	MBPTR	SHDWMBPTR	CIARADDRL	CIARADDRH	0............0	0............0
CIADATAL	CIADATAH	PSSNS	XTFERSUM	TSICTL	TSITSC	0............0	0............0
TSISTAT	TSITSEL	TSIEXR0	TSIEXR1	TSIESR0	TSIESR1	0............0	0............0
CSPETSC*	FBICTL	PSCSUM	PSCPEST	PSCPSE	PSCPCMCO	0............0	0............0
PSCCBCO	ALFESR0	ALFESR1	TRPFER0	TRPFER1	ALNKER0	0............0	0............0
ALNKER1	CSPESR0*	CSPESR1*	CSPSTAT*	CSPCTL0*	CSPCTL1*	0............0	0............0
CSPTCERR*	PSCEQUIP†	PSCINSRV†	GRSVERCODE†	GRSVCAUSE†	GRSVMISC1†	0............0	0............0
GRSVMISC2†	GRSVSP†	GRSVSTK†	GRSVFP†	GRSVPC†	GRSVLOAD†	0............0	0............0
GRSVCHKSUM†	CTLEQIP†	0............0	0............0	0............0	0............0	0............0	0............0
MEMN†	XLATE†	7............7	7............7	7............7	7............7	7............7	7............7

NOTE:
Upper Half = Controller 0
Lower Half = Controller 1

* This word contains zeroes in the 4E24 Release 1 generic.
† This word is part of the IREG layout.

CSTATUS—Controller Software Status

Bit 0 = Maintenance Access (MA)
1 = Receive on (RO) select
2 = Send on bus 0 (S0)
3 = Send on bus 1 (S1)
4 = Divorce controller from mate. When set, ability of controller to mismatch is turned off (DIV)
5 = Stop autonomous processing in this controller
6 = Read-Only Divorce controller from mate. Duplicate of bit 4 (RODIV)
7 = Active/Standby. When set, this controller is active
8 = Unused
9 = Indicates which TSI Controller sends to TMS 0-3 Network 0 (TN0RO)
10 = Indicates which TSI Controller sends to TMS 0-3 Network 1 (TN1RO)
11 = Indicates which TMS 0-3 Network half this TSI Controller receives from (NT0RO)
12 = Out-of-Service
13 = This controller has been removed by TTY request (RMVTTY)
14-15 = Unused
16 = Loop Around. When set, ALF transmitters loop to ALF receivers
17-19 = Unused
20-23 = Maintenance Codes:
20 = MAIN0
21 = MAIN1
22 = MAIN2
23 = MAIN3

STATR—Controller Hardware Status

Bit 0 = Maintenance Access Flip-Flop
1 = Receive On (RO) (PU bus designated by logic level)
2 = Send-On Bus 0 (S0)
3 = Send-On Bus 1 (S1)
4 = Divorce Controller From Mate = 1 (DIV)
5 = Stop Autonomous Processing = 1 (STOP)
6 = Read-Only Divorce controller from mate. Duplicate of bit 4 (RODIV)
7 = Active/Standby (1 = this controller is active [in current TSI bit reads as which controller is active for example 1 = C1 is active])
8 = Unused
9 = Indicates which TSI Controller sends to TMS 0-3 Network 0 (TN0RO)
10 = Indicates which TSI Controller sends to TMS 0-3 Network 1 (TN1RO)
11 = Indicates which TMS 0-3 Network half this TSI Controller receives from (NT0RO)
12 = Enable Clock Error 1 (ENCKER1)
13 = Enable Clock Error 2 (ENCKER2)
14 = Control Register Exercise Enable (CREXEN). This bit must be set for the following Control Register bits to produce their effects: FCLKE3, FCLKE4, XCUPD, OVRDIV, FAS0ERR and FAS1ERR. These bits may also require the EXEREN bit of the Control Register to be set.
15 = Buffer Polling is enabled when SP Number strap on backplane
16 = Loop Around (LA). When set, loops ALF transmitters to ALF receivers (bypass Network)
17-23 = Unused

MADATA—MA Data Response

Bit 0 = Maintenance Access (MA)
1 = Receive On Bus 0 or 1 (RO)
2 = Send On Bus 0 (S0)
3 = Send On Bus 1 (S1)
4 = Divorce Controller From Mate (DIV)
5 = Stop Autonomous Processing (STOP)
6 = Controller Update (from active to standby) (XCUPD)
7 = Active/Standby. (1 = this controller active) (AS)
8 = Peripheral Unit Bus Even Parity Failure (PUPFE)
9 = Peripheral Unit Bus Odd Parity Failure (PUPFO)
10 = K-Code Match (1 = k-code matched) (KM)
11 = Mode Bit (MBIT)
12 = Receive On Bus Complement (logical inversion of bit 1) (ROC)
13 = PUB Sequencer active (PUBSQA)
14 = Autonomous Interrupt (AINT)
15 = All Seems Well Failure (ASWF)
16 = Unassigned Opcode Failure (UNASOP)
17 = Mode Failure (MODFL)
18 = PUBI Parity Error (PPE)
19 = Read-Only Divorce controller from mate. Duplicate of bit 4 (RODIV)
20 = OR of Local Clock Failure (LCLKF) and Clock Summary (CLKSUM) in CESR
21 = TSI Clock Error - Indicates loss of TSI Clock (TSICLKER)
22 = Forced value of: TN0RO if read from Controller 0 or TN1RO if read from Controller 1
23 = Forced value of: TN2RO if read from Controller 0 or TN3RO if read from Controller 1

FSTATUS0—Frame Software Status Word 0

Bit 0 = PUB 0 at frame (IPUB0) removed via TTY (TTYIPUB0)
1 = PUB 1 at frame (IPUB1) removed via TTY (TTYIPUB1)
2 = PUB 0 OOS at frame (IPUB0) (OSIPUB0)
3 = PUB 1 OOS at frame (IPUB1) (OSIPUB1)
4 = Switch in progress (SIP)
5 = Maintenance Buffer Overflow (MBOVFL)
6 = A-Link0 OOS0 (OSALNK0)
7 = A-Link1 OOS1 (OSALNK1)
8 = A-Link 0 Removed via TTY (ALC0TTRM)
9 = A-Link 1 Removed via TTY (ALC1TTRM)
10 = Frame diagnostics in-progress (DGIP)
11 = Frame digit buffer full (DGBF)
12 = Update TSS memory in-progress (UPDTSSIP)
13-23 = Unused

FSTATUS1—Frame Software Status Word 1

Bit 0-2 = Spare Assignment Number for D3U6
(Legal values: 0, 1, 2 and 6) (SPAD3U6)
3 = Unused
4 = Protection Switch in Progress SPARE D3U6 (PSIPD3U6)
5 = Unused
6-8 = Spare Assignment Number for D3U7
(Legal values: 3, 4, 5 and 7) (SPAD3U7)
9 = Unused
10 = Protection Switch in Progress SPARE D3U7 (PSIPD3U7)
11 = Unused
12-15 = Spare Assignment Number for SPU10
(Legal Value: 0, 1, 2, 3, 4, 10) (SPASPS10)
16 = Protection Switch in Progress Spare SPU10 (PSIPSPS10)
17 = Unused
18-21 = Spare Assignment Number for SPU11
(Legal Value: 5, 6, 7, 8, 9, 11) (SPASPS11)
22 = Protection Switch in Progress Spare SPS11 (PSIPSPS11)
23 = Unused

CESR—Controller Primary Error Source Register (ESR)

NOTE:
When bit 0 or bit 1 are set, APUF is returned on CLKI.

Bit 0 = All Seems Well Failure (ASWF)
1 = Autonomous Interrupt (AINT)
2 = Peripheral Unit Bus Even Parity Failure (PUPFE)
3 = Peripheral Unit Bus Odd Parity Failure (PUPFO)
4 = Autonomous Peripheral Unit Trouble (APUT)
5 = Error detected by PUB sequencers (PUBSEQ)
6 = Invalid/Unassigned Opcode (UNASOP)
7 = Resident Software Error Bit 0, Forces Soft Initialization (restarts at point of error) (SWERR0)
8 = Resident Software Error Bit 1, Forces Hard Initialization (does not clear stable calls) (SWERR1)
9 = Resident Software Error Bit 2, Forces Zero Start (clears stable calls) (SWERR2)
10 = Resident Software Error Bit 3, PSC Software Detection Error (SWERR3)
11 = Audit Error Source Summary (AUDSUM)
12 = Mode Failure (MODFL)
13 = PUBI Parity Error (PPE)
14 = XTSI Fabric Error Source Summary (XTFSUM)
15 = Local Clock Failure on PUBI (LCLKF)
16 = Unused
17 = Spare Pack Error Source Summary (Future Expansion) (SPARESUM)
18 = Control Bus and Image Administrator Error Source Summary (CIASUM)
19 = Global RAM Local Error Source Summary (GRAMSUM)
20 = EXEC Local Error Source Summary (EXECSUM)
21 = EXEC Complex Backplane Error Source Summary (BPSUM)
22 = Clock Error Source Summary (OR of EXEC and TSI pack clock errors) (CLKSUM)
23 = GRAM, EXEC Complex Cross Controller Mismatch (CCMM)

PEST—Controller Programmable Error Source Inhibit Register

Bit 0 = Inhibit All Seems Well Failure (IASWF)
1 = Inhibit Autonomous Interrupt (IAINT)
2 = Inhibit Peripheral Unit Bus Even Parity Failure (IPUPFE)
3 = Inhibit Peripheral Unit Bus Odd Parity Failure (IPUPFO)
4 = Inhibit Autonomous Peripheral Unit Trouble (IAPUT)
5 = Inhibit PUB Sequencer error (IPUBSEQ)
6 = Inhibit Invalid/Unassigned Opcode (IUNASOP)
7 = Inhibit Resident Software Error Bit 0, Forces Soft Initialization (restarts at point of error) (ISWERR0)
8 = Inhibit Resident Software Error Bit 1, Forces Hard Initialization (does not clear stable calls) (ISWERR1)
9 = Inhibit Resident Software Error Bit 2, Forces Zero Start (clears stable calls) (ISWERR2)
10 = Inhibit Resident Software Error Bit 3, PSC Software Detection Error (ISWERR3)
11 = Inhibit Audit Error Source Summary (IAUDSUM)
12 = Inhibit Mode Failure (IMODFL)
13 = Inhibit PUBI Parity Error (IPPE)
14 = Inhibit XTSI Fabric Error Source Summary (IXTFSUM)
15 = Inhibit Local Clock Failure (ILCLKF)
16 = Unused
17 = Inhibit Spare Pack Error Source Summary (Future Expansion) (ISPARESUM)
18 = Inhibit Control Bus and Image Administrator Error Source Summary (ICIASUM)
19 = Inhibit Global Ram Local Error Source Summary (IGRAMSUM)
20 = Inhibit EXEC Local Error Source Summary (IEXECSUM)
21 = Inhibit Backplane Error Source Summary (IBPSUM)
22 = Inhibit Clock Error Source Summary (ICLKSUM)
23 = Inhibit Cross Controller Mismatch (ICCMM)

CNTL—Controller Control Register

Bit 0 = Force Clock Error 1. Used by diagnostics to force clock phase alignment error. Bit EXEREN must also be set along with ENCKER1 in the STATR register to cause effect. (FCLKE1)
1 = Force Clock Error 2. Used by diagnostics to force loss of clock reference error. Bit EXEREN must also be set along with ENCKER2 in the STATR register to cause effect. (FCLKE2)
2 = Force Clock Error 3. Used by diagnostics to force a clock branch failure on the PUBI. EXEREN and CREXEN of Status Register must also be set to cause effect. (FCLKE3)
3 = Force Clock Error 4. Used by diagnostics to force a PUB sequencer clock failure. EXEREN and CREXEN of the Status Register must also be set to cause effect. (FCLKE4)
4 = Cross-Controller Update enable. CREXEN of Status Register must also be set. (XCUPD)
5 = Override Divorce, when set controller always performs matching, overriding DIV bit and the CCMM bit in ESR. CREXEN in Status Register must also be set. (OVRDIV)
6 = Exercise Enable. Bit must be set in order to enable the diagnostic error-causing functions. (EXEREN)
7 = Error Source Register Clear. When set clears all ESR bits in controller (and PSC’s if active controller). (ESRCLR)
8 = Force Active/Standby Zero Error. Inverts the 0 branches (also called "a" branches) of A/S distribution. CREXEN must also be set. (FAS0ERR)
9 = Force Active/Standby One Error. Inverts the 1 branches (also called "b" branches) of A/S distribution. CREXEN must also be set. (FAS1ERR)
10 = Power-On Clear, status bit that indicates a power on clear when set, as opposed to EXEC reset when clear. (POC)
11 = EXEC arbitration used for handshaking between the EXEC and PUB sequencers on PUBI. (EXARB)

CNTL—Controller Control Register (Contd)

12 = Reply Disable, when set inhibits the initiation of a reply sequence with the next write to the Reply Register. (RPLDIS)
13 = Reply, reply sequence initiated if the Reply Sequencer waiting for Reply Register. Not stored, can retransmit a reply. (RPLY)
14 = CSP divorce low, setting this bit causes the divorce signal going to the CSP pack to be low
15 = Spare
16 = Set autonomous peripheral unit trouble
17 = Spare
18 = Set Unassigned Opcode, setting this non-stored bit sets the UNASOP bit in the CESR register if not pested. (SUNASOP)
19-22 = Set software error; setting any of these non-stored bits sets the corresponding bit in the CESR register if not pested. (SSWERR0-SSWERR3)
23 = Set Audit Summary, setting this non-stored bit sets the AUDSUM bit in the CESR register if not pested. (SAUDSUM)

EXCNTLSTATL—EXEC Control/Status Register Low 24 Bits

Bit 0 = ALU Carry Bit (CARRY)
1 = ALU Zero Bit (ZERO)
2 = ALU Sign Bit (NEGATE)
3 = ALU Overflow Bit (OVERFLOW)
4 = ALU Link Flag (LINK)
5 = Backplane Test Bit 0 (TEST0)
6 = Backplane Test Bit 1 (TEST1)
7 = Always True Condition Bit (TRUE)
8-11 = Source A Force Parity Error (Byte 0-3)
12-15 = Source B Force Parity Error (Byte 0-3)
16 = Force Clock Energy Detector Error (FEDE)
17 = Force Controller Timing Mismatch (FCTMM)
18 = Externally READ/Writeable (SPARE)
19 = Control Timing Mismatch Direction (CTMMDIR)
20 = Vector Base Bit, if set, execute RAM (VBB)
21 = Clear Clock Error (CLCLKER)
22 = Internal Spare (INTSPARE)
23 = Read/Write Spare (RWSPARE)

EXCNTLSTATH—EXEC Control/Status Register High 8 Bits

Bit 0-7 = Interrupt Vector (IVECT[0-7])

EXESR—EXEC Error Source Register

Bit 0 = Stack Bounds Error (STKBND)
1 = Sanity Timer Expiration (SANTIMEX)
2 = Illegal Opcode (ILLOC)
3 = Source Parity Error (SRCPERR)
4 = Unused
5-12 = MicroRAM Parity Error (MRPE[0:7])
13 = Clock Phase Error (ECKPHS)
14 = Unused
15 = Software Error (causes EXEC ESR bit to be set in PUBI) (SOFTERR)
16-23 = Force Parity Error in Microword (FPEMW[0:7])
16 = FPEMW0
17 = FPEMW4
18 = FPEMW1
19 = FPEMW5
20 = FPEMW2
21 = FREMW6
22 = FREMW3
23 = FREMW7

GESR—Global RAM Error Source Register

Bit 0-7 = Logical OR for GRAMSUM Error in CESR
0-3 = RAM Bank A Parity Error (ERAP[0:3])
4-7 = RAM Bank B Parity Error (ERBP[0:3])
8-14 = Logical OR for BPSUM Error in CESR
8-11 = Destination Bus Data Parity Error (EDDP[0:3])
12 = Destination Bus Address Parity Error (EDAP)
13 = Source Bus A Address Parity Error (ESAAP)
14 = Source Bus B Address Parity Error (ESBAP)
15-16 = Logical OR for CCMM Error in CESR
15 = Update Bus Mismatch (EXUMM)
16 = Syndrome Mismatch (EXSMM)
17-23 = All zeroes

GCNTL—Global RAM Control Register

Bit 0 = For GADDR register 0, read count enable—allows auto increment/decrement when using GADDR0 for a global RAM read. (CRCNTE0)
1 = For GADDR register 1, read count enable—allows auto increment/decrement when using GADDR1 for a global RAM read. (CRCNTE1)
2 = For GADDR register 0, turn on auto decrement when this bit equals 1 and bit 0 or 4 also set. A value of 0 in this bit turns on auto increment, instead. (CCNTDN0)
3 = For GADDR register 1, turn on auto decrement when this bit equals 1 and bit 1 or 5 also set. A value of 0 in this bit turns on auto increment, instead. (CCNTDN1)
4 = For GADDR register 0, write count enable. Allows auto increment/decrement when using GADDR0 for a global RAM write. (CWCNTE0)
5 = For GADDR register 1, write count enable. Allows auto increment/decrement when using GADDR1 for a global RAM write. (CWCNTE1)
6 = Spare
7 = Syndrome Bus Transmit Inhibit (MTSTSXI)
8 = GTESTD Data and Associated Parity (bits 11-14, MTSTP0-3) Enabled to Backplane (MTSTDEN)
9 = Control Address and Associated Parity (bit 15, MTSTP4) Enabled to Backplane. (MTSTAEN)
10 = GTESTD Data and Address Enabled to Update Bus (Cross-Connect) (MTSTXEN)
11-14 = GTESTD Data Parity (MTSTP[0:3])
15 = Control Address Destination Parity (MTSTP4)
16-21 = Destination Address Offset (MTSTOF[0:5])
22-23 = Destination Address Mode (MTSTMD[0:1])

GADDR0—Global RAM Address Memory 0

Bit 0-17 = Base Address Pointer to window in GRAM, the lower six bits are logically ORed with the microword (BADR0 [0:17])
18-23 = Unused, Write no action, Read zeroes

GADDR1—Global RAM Address Memory 1

Bit 0-17 = Base Address Pointer to window in GRAM, the lower six bits are logically ORed with the microword (BADR1 [0:17])
18-23 = Unused, Write no action, Read zeroes

EXINTR—EXEC Interrupt Register

Bit 0 = Spare Interrupt 0 (SPINT0)
1 = Operational Interrupt (OPINT)
2 = Spare Interrupt 1 (SPINT1)
3 = Error Interrupt (ERINT)
4 = Mask For Spare Interrupt 0 (MSPINT0)
5 = Mask For Operational Interrupt (MOPINT)
6 = Mask For Spare Interrupt 1 (MSPINT1)
7 = Mask For Error Interrupt (MERINT)
8 = Mask For All Interrupts (MINT)
9 = Interrupt In Progress When 2nd Interrupt Received (INTPND)
10-11 = Zeros
12 = EXEC circuit pack has in-band signalling
13-23 = Zeros

CIAESCL—CIA Error, Status, and Control Register

Bit 0-7 = Reset ability, Part of CIASUM in CESR
0 = Flash Write Parity Error (Writing clears bits 0-7) (FLWPE)
1 = Source A Data Parity Error (DSATPE)
2 = Destination Data Parity Error (DDATPE)
3 = Source Mode and Offset Parity Error (SMOPE)
4 = Destination Mode and Offset Parity Error (DMOPE)
5 = XTF Client Write Parity Error (XTFWPE)
6 = XTF Client Read parity Error (XTFRPE)
7 = Client SACK Error (ESACK)
8-23 = Status Bits
8-15 = Last SACK received. Gives value of SACK received during last control bus transfer (LSACK[0:7])
16-23 = Expected SACK. Gives value of SACK expected during last control bus transfer (LSACKEXP[0:7])

NOTE:
CIAESCL is a 32-bits register. Only the low 24-bits of the register is printed in the critical register dump. The high 8-bits contain some flash control bits.

EXSANTIM—Sanity Timer Register

Bit 0-23 = Timer Count Bits (SANTIM[0:23])

EXSTKBNDL—Stack Boundary Register Low

Bit 0-15 = Stack Boundary Low Address (SBL[0:15])
16-23 = Stack Boundary High Address Low 8 Bits (SBH[0:7])

EXSTKBNDH—Stack Boundary Register High

Bit 0-7 = Stack Boundary High Address High 8 Bits (SBH[8:15])

MBPTR—Maintenance Buffer Pointer

Bit 0-11 = Read pointer
11-23 = Write pointer

SHDWMBPTR—Shadow Maintenance Buffer Pointer

Bit 0-11 = Temporary read pointer
12-23 = Unused

CIARADDRL—CIA Read Address Register Low 24 Bits

Bit 0-23 = Memory Address, Written or Read (ADD[00:23])

CIARADDRH—CIA Read Address Register High 8 Bits

Bit 0-6 = Slot Address (SLOTADD[0:6])
7 = Multi-Cast, address all clients (MLTCST)

CIADATAL—CIA Control Bus Data Register Low 24 Bits

Bit 0-23 = Control Bus Data (DATA[0:23])

CIADATAH—CIA Control Bus Data Register High 8 Bits

Bit 0-7 = Control Bus Data (DATA[24:31])

PSSNS—Protection Switch Sense Register

Bit 0-5 = Protection Switch Sense. Each bit (when set) indicates the respective D3U paddle-board is protection switched. If paddleboard is not present, the bit always reads zero (PSSENSE)
6-23 = Unused; can not be written; are read as zero.

NOTE:
Bits 0-5 are for corresponding DS3 line numbers 1-6.

XTFERSUM—XTF Fabric Error Summary Register

Bit 0-3 = FBI errors

0 = Indicates a byte 0 parity error occurred on an FBI local control bus write. (WTPERB0)

1 = Indicates a byte 1 parity error occurred on an FBI local control bus write. (WTPERB1)

2 = Indicates a byte 2 parity error occurred on an FBI local control bus write. (WTPERB2)

3 = Indicates a byte 3 parity error occurred on an FBI local control bus write. (WTPERB3)

4-21 = Control bus and PCM bus errors:

4 = Indicates any control bus related error on ALF 0. (ALF0CBER)

5 = Indicates any PCM related error on ALF 0 and can cause autonomous reconfiguration of the A-link. Latches the Time-Slot counter on the TSI pack. (ALF0PCMER)

6 = Indicates any control bus related error on ALF 1. (ALF1CBER)

7 = Indicates any PCM related error on ALF 1. Can cause autonomous reconfiguration of the A-Link. Latches the Time-Slot counter on the TSI pack. (ALF1PCMER)

8 = Indicates any Control bus related error (Bit reserved for ALF2). (ALF2CBER)

9 = Indicates any PCM related error (Bit reserved for ALF 2). Can cause autonomous reconfiguration of the A-Link. Latches the Time-Slot counter on the TSI pack. (ALF2PCMER)

10 = Indicates any Control bus related error (Bit reserved for ALF3). (ALF3CBER)

11 = Indicates any PCM related error (Bit reserved for ALF3). Can cause autonomous reconfiguration of the A-Link. Latches the Time-Slot counter on the TSI pack. (ALF3PCMER)

XTFERSUM—XTF Fabric Error Summary Register (Contd)

12 = Indicates CSP detected error (CSPERR)

If CSP is not present indicates any control bus related error on F spare controller client (SPARECBER)

13 = Indicates any PCM bus related error on F spare controller client (SPAREPCMER)

14 = Indicates any Control bus related error on the TERM0 controller client (TERM0CBER)

15 = Indicates any PCM bus related error on the TERM0 controller client (TERM0PCMER)

16 = Indicates any Control bus related error on the TERM1 controller client (TERM1CBER)

17 = Indicates any PCM bus related error on the TERM1 controller client (TERM1PCMER)

18 = Indicates any TSI detected PCM error. Can cause autonomous reconfiguration of the A-link. Latches the Time-slot counter on the TSI pack (TSIPCMNMER).

19 = Indicates any TSI detected cross-controller mismatch PCM error (TSIPCMMER)

20 = Indicates any TSI detected Control bus related error (TSICBER)

21 = Indicates that a PSC error summary bit is set in the PSCERSUM register (PSCSUM)

22 = Indicates a mismatch between the duplicated active/standby signals within the local controller or a mismatch between the active/standby state of controller 0 and the active/standby state of controller 1 (active/active or standby/standby) (ASMMER)

23 = Unused—Can not be written, and is read as zero.

TSICTL—TSI Control Register

Bit 0 = Control Bus Address Loop-around (CBALOOP)
1 = Exercise Enable (TSIEXEREN)
2 = Error Lock Inhibit (turns off sense and lock) (ELOCKIN)
3 = Externally Read/Writeable (SPARE)
4 = TSI Control Bus Error Pest (TCBEPEST)
5 = TSI Cross-Controller Mismatch Error Pest (TCMEPEST)
6 = TSI Non-mismatch Error Pest (TNMEPEST)
7 = Externally Read/Writeable (SPARE)
8-23 = Unused

TSITSC—TSI Time-Slot Counter

Bit 0-11 = Time-Slot Count (TSCNT[00:11])
12 = Odd/Even Frame Count Bit (FRCNT)
13-23 = Unused

Alternate Layout: If Bits 3-4 = 0, use this layout

Bit 0-2 = Port Number. Is an A-Link port if A-Link partition. (TSCPORT[0:2])
3-4 = Partition - Zero is the A-Link partition. (TSCPART[0:1])
5-11 = Network Time-Slot (NETTS[0:6])
12 = Odd/Even Frame Count Bit (FRCNT)
13-23 = Unused

TSISTAT—TSI Status Register

Bit 0-7 = Buffer Memory Diagnostic Read (BMDR[0:7])
8 = Buffer Memory Diagnostic Read of data parity (BMDR8)
9 = Buffer Memory Diagnostic Read of address parity (BMDR9)
10 = Buffer Memory Diagnostic. Detects if the BM Input Multiplexer is in the Diagnostic State (BMDGN)
11 = ESR Clear Signal is Active (Not Latched) (ESRCA)
12 = ALF Error Latch has been set (latches TSITSEL) (High 12 bits) (ATSELA)
13 = TSC Error Latch has been set (latches TSITSEL) (Low 12 bits) (TTSELA)
14 = TSM Search is in progress (Active) (Not Latched) (SRCHA)
15-23 = Unused

TSITSEL—TSI Time-Slot Error Latch

Bit 0-11 = Time-Slot Count Error Latch (TSI and non-TRPF ALF bits) (TSCER[0-11])
12-23 = Time-Slot Count Error Latch (ALF TRPF bits) (TSCER[12-23])

TSIEXR0—TSI Exercise Register 0

Bit 0 = TSM/TSXR X Memory Access (Only for diagnostic purposes.) (TSIXMEM)
1 = TSM/TSXR Y Memory Access (Only for diagnostic purposes.) (TSIYMEM)
2 = Time-Slot Counter Stop Bit. Stops TSITSC when set. (STOPTSC)
3 = Time-Slot Counter Step Bit. Singles step TSITSC. (STEPTSC)
4 = TSITSC Step Enable Bit. Enables step bit and must also be set with STEPTSC. (TSTEPEN)
5 = Search Counter (TSISCTR) Stop Bit (STOPSCTR)
6 = Search Counter Step Bit. Singles step TSISCTR (TSISCTR must be stopped to single step.) (STEPSCTR)
7 = TSISCTR Step Enable Bit. Enables step bit and must also be set with STEPSCTR. (SSTEPEN)
8 = Force TSC Parity Error over Even Bits. (FTSCEVN)
9 = Force TSC Parity Error over Odd Bits. (FTSCODD)
10 = Force 32.768MHz Clock High (Creating CSE) (FCSEH)
11 = Force 32.768MHz Clock Low (Creating CSE) (FCSEL)
12 = Force 32.768MHz Phase Lock Up (PLE) (FPLEU)
13 = Force 32.768MHz Phase Lock Down (PLE) (FPLED)
14 = Force Network Sync Error (NSE) (FNSE)
15 = Force Bad PCA Parity (All TSMs) (FBPCA)
16 = Force Bad PCD Parity (All TSMs) (FBPCD)
17 = Force Bad PCB Parity (All TSMs) or Bad PCE Parity (All TSXRs) (FBPCB)
18 = Busy/Idle Compliment Signal Invert (BICINV)
19 = TSM Bad Parity Write Enable. When set allows write to occur regardless of parity value. (TSMBPWE)

TSIEXR0—TSI Exercise Register 0 (Contd)

20 = Buffer Memory Diagnostic Read Select 0 (See Table) (BMDRS0)
21 = Buffer Memory Diagnostic Read Select 1 (See Table) (BMDRS1)
22 = When Set, Bit 0 of TSC continues to Toggle When it is Halted. (TOGGLE)
23 = Force a Cross-Controller Mismatch Error (FCCME)

BMDRS0 and BMDRS1 are used to select which BM output PCM bus to be latched into the status register during diagnostics:

BMDRS0	BMDRS1	PCM Bus Selected
0	0	0PCMO
1	0	1PCMO
0	1	2PCMO
1	1	3PCMO

Hardware reset sets all bits to zero. Global ESR clears register. See TSISTAT bit layouts for more information.

TSIEXR1—TSI Exercise Register 1

Bit 0-7 = Invert Cross-Controller Mismatch Output Bit[0:7] to Mate TSI (ICCMO[0:7])
8 = Invert Cross-Controller Mismatch Output Bit P to Mate TSI (ICCMOP)
9 = Force 0PCMI Parity Error (Forces bad parity on input PCM Bus 0) (F0PCMIPE)
10 = Force 1PCMI Parity Error (Forces bad parity on input PCM Bus 1) (F1PCMIPE)
11 = Force 2PCMI Parity Error (Forces bad parity on input PCM Bus 2) (F2PCMIPE)
12 = Force 3PCMI Parity Error (Forces bad parity on input PCM Bus 3) (F3PCMIPE)
13 = Force 0PCMO Parity Error (Forces bad parity on output PCM Bus 0) (F0PCMOPE)
14 = Force 1PCMO Parity Error (Forces bad parity on output PCM Bus 1) (F1PCMOPE)
15 = Force 2PCMO Parity Error (Forces bad parity on output PCM Bus 2) (F2PCMOPE)
16 = Force 3PCMO Parity Error (Forces bad parity on output PCM Bus 3) (F3PCMOPE)
17-23 = Read/Writeable (SPARE)

TSIESR0—TSI Error Source Register 0

Bit 0 = Control Bus Data Write Parity Error for Byte 0 (CBDPE0)
1 = Control Bus Data Write Parity Error for Byte 1 (CBDPE1)
2 = Control Bus Data Write Parity Error for Byte 2 (CBDPE2)
3 = Control Bus Data Write Parity Error for Byte 3 (CBDPE3)
4 = Time-Slot Counter Error. Does not match framing interval from network clock (TSCERR)
5 = Unused
6 = Cross-Controller Mismatch Error (CCME)
7 = Network Sync Error—Network clock signal stuck Low or High (NSE)
8 = 32.768 MHz Phase Lock Error (PLE)
9 = 32.768 MHz Clock Source Error—32 MHz Distribution stuck Low or High (CSE)
10-19 = Non-cross controller mismatch (NM)
 10-13 = Mismatch Error (TSXRMM [0:3])
 14 = TSXR0 PCM Enable Parity Error (PCE0)
 15 = TSXR1 PCM Enable Parity Error (PCE1)
 16 = TSXR2 PCM Enable Parity Error (PCE2)
 17 = TSXR3 PCM Enable Parity Error (PCE3)
 18 = Active/Standby Signal Mismatch Error (ACTMME)
 19 = Buffer Memory Input MUX Select Error (BMIMSE)
20-23 = Unused

TSIESR1—TSI Error Source Register 1

Bit 0 = PCM 0 Input Parity error (from clients) (0PCMIPER)
1 = PCM 1 Input Parity error (from clients) (1PCMIPER)
2 = PCM 2 Input Parity error (from clients) (2PCMIPER)
3 = PCM 3 Input Parity error (from clients) (3PCMIPER)
4 = Time-Slot Memory 0 Mismatch Error (TSM0MM)
5 = Time-Slot Memory 1 Mismatch Error (TSM1MM)
6 = Time-Slot Memory 2 Mismatch Error (TSM2MM)
7 = Time-Slot Memory 3 Mismatch Error (TSM3MM)
8 = Time-Slot Memory 0 Address Parity Error (PCA0)
9 = Time-Slot Memory 1 Address Parity Error (PCA1)
10 = Time-Slot Memory 2 Address Parity Error (PCA2)
11 = Time-Slot Memory 3 Address Parity Error (PCA3)
12 = Time-Slot Memory 0 Data Parity Error (PCD0)
13 = Time-Slot Memory 1 Data Parity Error (PCD1)
14 = Time-Slot Memory 2 Data Parity Error (PCD2)
15 = Time-Slot Memory 3 Data Parity Error (PCD3)
16 = Time-Slot Memory 0 Busy/Idle Parity Error (PCB0)
17 = Time-Slot Memory 1 Busy/Idle Parity Error (PCB1)
18 = Time-Slot Memory 2 Busy/Idle Parity Error (PCB2)
19 = Time-Slot Memory 3 Busy/Idle Parity Error (PCB3)
20 = Buffer Memory 0 Output Parity Error (BM0OPE)
21 = Buffer Memory 1 Output Parity Error (BM1OPE)
22 = Buffer Memory 2 Output Parity Error (BM2OPE)
23 = Buffer Memory 3 Output Parity Error (BM3OPE)

CSPETSC—CSP Extended Timeslot Counter Register

Bit 0-4 = This bits always set to zero
5-11 = TSC bits 5-11 from TSI (TSC)
12-18 = Extended Time Slot Count 0-6 (ETSC[0:6])
19-23 = Unused

FBICTL—FBI Control Register

Bit 0 = When set, any control bus read of the FBI will return contents of FBI Control bus Address Latch. Cleared by power on clear. (FBICALRD)

1 = When set, functions of FBIEXER are enabled. When this bit is reset, FBIEXER functions are disabled. Cleared by power on clear. (FBIEXEREN)

2-3 = Unused

4 = Cuts ALF 0 off of the PCM bus. Set by power-on clear. (ALF0PCMCO)

5 = Cuts ALF 1 off of the PCM bus. Set by power-on clear. (ALF1PCMCO)

6 = Cuts Spare (bit reserved for ALF2) off of the PCM bus. Set by power-on clear. (ALF2PCMCO)

7 = Cuts Spare (bit reserved for ALF3) off of the PCM bus. Set by power-on clear. (ALF3PCMCO)

8 = Cuts spare controller circuit pack off the PCM bus. Set by power-on clear.

9 = Cuts the TERM 0 controller circuit pack off the PCM bus. Set by power-on clear.

10 = Cuts the TERM 1 controller circuit pack off the PCM bus. Set by power-on clear.

11 = Cuts ALF 0 off of the Control bus. Set by power-on clear. (ALF0CBCO)

12 = Cuts ALF 1 off of the Control bus. Set by power-on clear. (ALF1CBCO)

13 = Cuts Spare (bit reserved for ALF2) off of the Control bus. Set by power-on clear. (ALF2CBCO)

14 = Cuts Spare (bit reserved for ALF3) off of the Control bus. Set by power-on clear. (ALF3CBCO)

15 = Cuts CSP (controller signal processor) off of the Control bus. Set by power-on clear. (CSPCBCO)

16 = Cuts the TERM 0 controller circuit pack off the Control bus. Set by power-on clear.

FBICTL—FBI Control Register (Contd)

17 = Cuts TERM1 CONTR pack off the Control bus
18 = Cuts TSI off the Control bus. Set by power-on clear.
19-23 = Unused.

PSCSUM—PSC Error Summary Register
See Control Bus Memory Layout.

Bit 0-23 = Protection Switch Client Reporting Error. Each bit (when set) indicates that some error is detected on that respective PSC number. Each bit is level sensitive and reflect the state of the respective PSC summary bit. (PSERSUM[0-23])

PSCPEST—PSC Error Pest Register
See Control Bus Memory Layout.

Bit 0-23 = Protection Switch Client Error Pest. When set pests that respective PSC number. (PSCERRP[0-23])

PSCPSE—PSC Read Protection Switch Enable Register
See Control Bus Memory Layout.

0-2 = Protection Switch Group 0. Protection Switch Register Read
0 = If set, PSC 1 is protection switched (PSREAD1)
1 = If set, PSC 2 is protection switched (PSREAD2)
2 = If set, PSC 3 is protection switched (PSREAD3)

3-5 = Protection Switch Group 1. Protection Switch Register Read
9 = If set, PSC 9 is protection switched (PSREAD9)
10 = If set, PSC 10 is protection switched (PSREAD10)
11 = If set, PSC 11 is protection switched (PSREAD11)

6-8 = Protection Switch Group 2 (PSREAD[13-15]) (Not Used)
9-11 = Protection Switch Group 3 (PSREAD[21-23]) (Not Used)
12-23 = Unused (read as zeroes).

PSCPCMCO—PSC PCM Cutoff Register
See Control Bus Memory Layout.

Bit 0-23 = PCM Bus Cutoffs for respective PSC numbers (PCMCO[0-23])

PSCCBCO—PSC Control bus Cutoff Register
See Control Bus Memory Layout.

Bit 0-23 = Control Bus Cutoffs for respective PSC numbers (CBCO[0-23])

ALFESR0—ALF Error Source Register 0 (SPC 0 and 1)
ALFESR1—ALF Error Source Register 1 (SPC 2 and 3)

Bit 0 = Indicates a parity error was detected on data from the Control Bus Byte 0 (CBDPE0)
1 = Indicates a parity error was detected on data from the Control Bus Byte 1 (CBDPE1)
2 = Indicates a parity error was detected on data from the Control Bus Byte 2 (CBDPE2)
3 = Indicates a parity error was detected on data from the Control Bus Byte 3 (CBDPE3)
4 = Wrote ALFIDLE0 or ALFIDLE1 without having the corresponding enable bit set in ALFCTL. (ERIDLWR)
5-7 = Unused
8 = Indicates a parity error was detected on the TSC even bits (ALFTSCPEE)
9 = Indicates a parity error was detected on the TSC odd bits (ALFTSCPEO)
10 = Indicates a parity error was detected on PCM bus busy idle 0 (ALFPCMBIE0)
11 = Indicates a parity error was detected on PCM bus busy idle 1 (ALFPCMBIE1)
12 = Indicates a parity error was detected on data from PCM output bus 0 (ALFPCMOPE0)
13 = Indicates a parity error was detected on data from PCM output bus 1 (ALFPCMOPE1)
14 = Indicates a parity error was detected on data from the ALF for PCM input bus 0 (ALFPCMIPE0)
15 = Indicates a parity error was detected on data from the ALF for PCM input bus 1 (ALFPCMIPE1)
16 = Indicates a parity error was detected in one or more of the 16 A’-Link circuits. ALF register ALNKPER indicates which circuit detected the error (ALNKSUM)

ALFESR0—ALF Error Register 0 (SPC 0 and 1)
ALFESR1—ALF Error Register 0 (SPC 2 and 3) (Contd)

Bit 17 = Indicates that a transmission parity error (TRPF) was detected in one or more of the 16 A'-Link circuits. ALF register TRPFPER indicates which circuit detected the error (TRPFSUM)

18 = Indicates a parity error was detected on data from the Busy/Idle Memory Circuit 0 (BIMAPER0)

19 = Indicates a parity error was detected on data from the Busy/Idle Memory Circuit 1 (BIMAPER1)

20 = Indicates a parity error was detected on leading-ones detector buffer memory 0 read address (BUF0PER)

21 = Indicates a parity error was detected on leading-ones detector buffer memory 1 read address (BUF1PER)

22 = Indicates that an internal matching error in the LOD delayed busy/idle circuit was detected
(Summary bit for the DBIER register) (DBISUM)

23 = This bit always reads zero. A write to the ALFESR with bit 23 set causes a 60ns pulse that clears BUF(0/1)PER in the ALFESR.

TRPFER0—ALF Primary TRPF Error Register (SPC 0 and 1)
TRPFER1—ALF Primary TRPF Error Register (SPC 2 and 3)

Bit 0 = Indicates that A'-Link circuit 00 detected bad parity on PCM data (TRPF00)
1 = Indicates that A'-Link circuit 01 detected bad parity on PCM data (TRPF01)
2 = Indicates that A'-Link circuit 02 detected bad parity on PCM data (TRPF02)
3 = Indicates that A'-Link circuit 03 detected bad parity on PCM data. This bit will be forced set when fault (Pin C047) is held low (TRPF03)
4 = Indicates that A'-Link circuit 04 detected bad parity on PCM data (TRPF04)
5 = Indicates that A'-Link circuit 05 detected bad parity on PCM data (TRPF05)
6 = Indicates that A'-Link circuit 06 detected bad parity on PCM data (TRPF06)
7 = Indicates that A'-Link circuit 07 detected bad parity on PCM data (TRPF07)
8 = Indicates that A'-Link circuit 010 (octal) detected bad parity on PCM data (TRPF10)
9 = Indicates that A'-Link circuit 011 (octal) detected bad parity on PCM data (TRPF11)
10 = Indicates that A'-Link circuit 012 (octal) detected bad parity on PCM data (TRPF12)
11 = Indicates that A'-Link circuit 013 (octal) detected bad parity on PCM data (TRPF13)
12 = Indicates that A'-Link circuit 014 (octal) detected bad parity on PCM data (TRPF14)
13 = Indicates that A'-Link circuit 015 (octal) detected bad parity on PCM data (TRPF15)
14 = Indicates that A'-Link circuit 016 (octal) detected bad parity on PCM data (TRPF16)
15 = Indicates that A'-Link circuit 017 (octal) detected bad parity on PCM data (TRPF17)
16-23 = Unused

ALNKER0—ALF Primary A-Link Error Register 0 (SPC 0 and 1)
ALNKER1—ALF Primary A-Link Error Register 1 (SPC 2 and 3)

Bit 0 = Indicates that A-Link circuit 00 detected bad parity on PCM data (ALNER00)
1 = Indicates that A-Link circuit 01 detected bad parity on PCM data (ALNER01)
2 = Indicates that A-Link circuit 02 detected bad parity on PCM data (ALNER02)
3 = Indicates that A-Link circuit 03 detected bad parity on PCM data (ALNER03).
4 = Indicates that A-Link circuit 04 detected bad parity on PCM data (ALNER04)
5 = Indicates that A-Link circuit 05 detected bad parity on PCM data (ALNER05)
6 = Indicates that A-Link circuit 06 detected bad parity on PCM data (ALNER06)
7 = Indicates that A-Link circuit 07 detected bad parity on PCM data (ALNER07)
8 = Indicates that A-Link circuit 010 (octal) detected bad parity on PCM data. This bit will be forced set when fault (Pin C053) is held low (ALNER10)
9 = Indicates that A-Link circuit 011 (octal) detected bad parity on PCM data (ALNER11)
10 = Indicates that A-Link circuit 012 (octal) detected bad parity on PCM data (ALNER12)
11 = Indicates that A-Link circuit 013 (octal) detected bad parity on PCM data (ALNER13)
12 = Indicates that A-Link circuit 014 (octal) detected bad parity on PCM data (ALNER14)
13 = Indicates that A-Link circuit 015 (octal) detected bad parity on PCM data (ALNER15)
14 = Indicates that A-Link circuit 016 (octal) detected bad parity on PCM data (ALNER16)
15 = Indicates that A-Link circuit 017 (octal) detected bad parity on PCM data (ALNER17)
16-23 = Unused

CSPESR0—CSP Error Source Register 0

Bit 0 = Control Bus Data Write Parity Error, Byte 0 (CBDPE0)
1 = Control Bus Data Write Parity Error, Byte 1 (CBDPE1)
2 = Control Bus Data Write Parity Error, Byte 2 (CBDPE2)
3 = Control Bus Data Write Parity Error, Byte 3 (CBDPE3)
4 = Address or Data Parity Error detected on the STS (STSPE)
5 = Parity Error Detected by the Buffer Interface FP GA on STS Data, OP, and MR Signals (STS2BUFPE)
6 = Mismatch detected between the Working and Reference E-store (ESTLMM)
7 = Mismatch detected between the Working and Reference M-store (MSTLMM)
8 = Detected trunk state mismatch between Controller 0 and Controller 1 (XCTSTMM)
9 = Detected Trunk State Mismatch between the controller and its corresponding backplane. A backplane fault can be used by the mate controller as well as locally (LOCTSTMM)
10 = Address or Data parity error detected on the TSS (TSSPE)
11 = Mismatch detected between the working and reference 10 millisecond timer (LOCTENMSMM)
12 = Mismatch detected between the working and reference Trunk Counter (LOCTCMM)
13 = Mismatch detected between the working and reference Extended Timeslot Counter (LOCETSCMM)
14 = Time of Unit Pulse Parity Error (XPTUPER1)
15 = Translated Extended TimeSlot Pulse XETSC Parity Error (XPXETSCPER)
16 = Control Signal Parity Error Detected On Translation PROM (XPCTLPER)

CSPESR0—CSP Error Source Register 0

17 = Address Parity Error Detected on the Translation PROM (XPADDPER)
18 = Summary of D3ULNKER (Bits 0-7 from CSPESR1 Register) (D3ULNKERSUM)
19 = Timeslot count parity Error from TSI circuit pack (TSCPARERR)
20 = Mismatch detected between the Working and Reference T-Bit translation logic (TBITXTER)
21 = Detected write to buffer for a report on a maintenance trunk (MTR2BER)
22 = Unused
23 = Digit Buffer Full - asserted and latched when the digit buffer is full (DGBUFFL)

CSPESR1—CSP Error Source Register 1

Bit 0-7 = Error detected on the E-Data stream of the associated D3U (D3ULNKER)
8-23 = Unused

CSPSTAT—CSP Status Register

Bit 0 = High Priority Buffer is Full (HPBFULL)
1 = High Priority Buffer is Empty (HPBEMPT)
2 = Low Priority Buffer is Full (LPBFULL)
3 = Low Priority Buffer is Empty (LPBEMPT)
4 = Digit Buffer is Full (DGBFULL)
5 = Digit Buffer is Empty (DGBEMPT)
6 = Seizure Buffer is Full (SZBFULL)
7 = Seizure Buffer is Empty (SZBEMPT)
8 = Indicates Buffer Write did not occur due to buffer full condition (NOBUFWT)
9 = Trunk Counter is stopped (STOPTC)
10-23 = Unused bits

CSPCTL0— CSP Control Register 0

Bit 0 = Control Bus Address Loop-around. When set, a read of any CSP address will cause the address value in the Control Bus Address Latch to be put out on the Control Bus Address/Data bus. This bit must be reset to resume normal operation (CBALOOP)
1 = Enable the Exercise Register to allow board faults to occur (CSPEXEREN)
2 = CSP Cross-Controller Mismatch Error Pest. This bit is used to pest Bit 8 & 9 of CSPESR (CSPXCMMPEST)
3 = Pests all CSP errors to the FBI (CSPERRPEST)
4-23 = Unused

CSPCTL1—CSP Control Register 1

Bit 0 = Flush out the high priority buffer (HPBUFFLSH)
1 = Flush out the low priority buffer (LPBUFFLSH)
2 = Flush out the digit buffer (DGBUFFLSH)
3 = Flush out the seizure buffer (SZBUFFLSH)
4 = Set stop bit
5 = Clear stop bit
6-7 = Low spare assignment number [LSAN(0:1)] (See valid state below.)
8-9 = High spare assignment number [HSAN(0:1)] (See valid state below.)
10-17 = Pest errors associated with individual D3Us [D3UPEST(0:7)]
18-23 = Prohibit CSP from updating E-store from the associated DS3 [D3UPEST(0:7)]

NOTE:
Bits 0-5 returns zero when read. To execute a specific action, set the corresponding bit in the register. After the corresponding action of the bit is executed, a reset pulse is issue to clear out the bit. It is expected to complete the action within 180ns.

Bits 6 through 23 are set on power up.

Valid State for LSAN and HSAN
Low Spare Assignment Number (Bits 6-7)
DSU 0 Assigned as Spare 0 0
DSU 1 Assigned as Spare 0 1
DSU 2 Assigned as Spare 1 0
DSU 6 Assigned as Spare 1 1
High Spare Assignment Number (Bits 8-9)
DSU 3 Assigned as Spare 0 0
DSU 4 Assigned as Spare 0 1
DSU 5 Assigned as Spare 1 0
DSU 7 Assigned as Spare 1 1
Note: LSAN and HSAN are set to 1s on Power-up.

CSPTCERR—CSP Trunk Counter Error Latch Register

Bit 0-11 = Trunk Counter Value latched whenever an error occurs except for DBFUL (CSPESR0 bit 23) TC[0:11]
12-23 = Unused bits return zero during read

PSCEQUIP—GRAM Status of PSC Equippage Code

Bit 0-23 = Indicates the status of PSC equippage code

PSCINSRV—GRAM Status of PSC In-Service Status

Bit 0-23 = Indicates the status of PSC In-service status

GRSVERCODE—GRAM F-Level Error Code

Bit 0-23 = Saved F-Level Error Code (SVERCODE[0:23]) (See F-Level Software Error Code)

GRSVCAUSE—GRAM Cause of F-Level Error

Bit 0-23 = Saved Cause of F-Level Error (SVCAUSE[0:23])

GRSVMISC1—GRAM Miscellaneous Firmware Buffer 1

Bit 0-23 = Miscellaneous Firmware Buffer 1 Data is context dependent. For F-levels on orders, data is PU Receive Low Register (SVMISC1[0-23])

GRSVMISC2—GRAM Miscellaneous Firmware Buffer 2

Bit 0-23 = Miscellaneous Firmware Buffer 2 Data is context dependent. For F-levels on orders, data is PU Receive Low Register (SVMISC2[0-23])

GRSVSP—GRAM Stack Pointer Register

Bit 0-23 = EXEC Stack Pointer Where Error Occurred (SVSP[0:23])

GRSVSTK—GRAM Stack Contents Register

Bit 0-23 = EXEC Stack Contents (SVSTK[0:23])

GRSVFP—GRAM Frame Pointer Register

Bit 0-23 = EXEC Frame Pointer Where Error Occurred (SVFP[0:23])

GRSVPC—GRAM Program Counter Register

Bit 0-23 = EXEC Program Counter Where Error Occurred (SVPC[0:23])

GRSVLOAD—GRAM Version Load Register

Bit 0-11 = Software issue
12-14 = Quarterly release
15-20 = AP load number

GRSVCHKSUM—GRAM Checksum Register

Bit 0-23 = GRAM Checksum Over Current Load

CTLEQUIP—Control Equipage

Bit 0 = CSP In-Service State
1 = CSP Equippage State
2-11 = Not Used
12 = Indicates circuit pack
0 = KBN16
1 = KBN23

13 = Indicates that the backplane jumper that enables DIF functionality is installed (DIFEN)
14 = Indicates the state of the High Priority Buffer Empty Signal originating on the CSP (HPBE)
15 = Indicates the state of the Low Priority Buffer Empty Signal originating on the CSP (LPBE)
16 = Indicates the state of the Digital Buffer Empty Signal originating on the CSP (DGBE)
17 = Indicates the state of the Seizure Buffer Empty Signal originating on the CSP (SZBE)
18 = Indicates the state of the CSP Stop signal originating on the CSP pack (CSPSTOP)

MEMN—XTSI Member Number

Bit 0-6 = XTSI Member Number (0-31)

XLATE—First Word of XTSI Unit Type Translator

Bit 0-15 = TSI port equipage for SPC 0

(where 00 = unequiped, 01 = growth, 10 = special growth and 11 = operational)

0-1 = Port 0
2-3 = Port 1
4-5 = Port 2
6-7 = Port 3
8-9 = Port 4
10-11 = Port 5
12-13 = Port 6
14-15 = Port 7

16-17 = Member equipage

(where 00 = unequiped, 01 = growth, 10 = special growth and 11 = operational)

18-20 = Hardware generation

000 = Units with no hardware differences or DS120 XTSI
001 = TSI with babbling bus fix (no ODA requirement)
010 = Near term TSI
011 = XTSI units which are used for D3U or DS3
100 = XTSI units with inband signaling enabled

21-23 = Member type

001 = TSI frame
010 = Cost reduced TSI
011 = Cost reduced companion TSI
100 = Expanded even TSI Frame
101 = Expanded mate/companion TSI

XTSI D3U Registers (via TTY Request)

D3USSTATUS	D3USTAT	D3UESR	D3UCTL	D3UEXR	TRANS1	TRANS2	TRANS3*
TRANS4*	TRANS5*	TRANS6*	TRANS7*	TRANS8*	TRANS9*	TRANS10*	

* If the spare D3U is requested (D3U 6 or D3U 7), these words (TRANS3-10) are not included in the dump.

D3USSTATUS—XTSI D3U Software Status

Bit 0 = D3U PESTed via TTY message (D3UPST)
1-2 = Unused
3-9 = D3U configuration status. (See Status of Configuration Request List for layout.) A zero indicates successful configuration request and non-zero indicates an error in configuration request (CNFGSTAT)
10-11 = Unused
12 = D3U out-of-service (D3UOS)
13 = D3U removed via TTY message (D3URMVTTY)
14-19 = Unused
20-23 = See Peripheral Subunit Maintenance Code (D3UMAIN) for layout

Status of Configuration Request List (Bits 3-9)	
Decimal	**Meaning**
0	Configuration successful
1	Readfile returned invalid
2	Returned file does not exist in FDT (file descriptor table)
3	Readfile returns error in file header
4	Loadfile failed with disk job failed
5	Loadfile failed with empty file
6	Flashpump macro failed
7	Flashpump macro error in file or flash
8	Flashpump macro failed with micro RAM checksum error
9	Flashpump macro failed copy over control bus
10	OSRAM bit not set in PSC hardware status: start task failed
11	Fail internal error
12	Fail clamp PSC macro during bootstrap
14	Fail unclamp PSC macro during bootstrap
16	Fail CIA ESC (error, status and control register) check
17	Fail controller activity check
18	Reject translation initialize macro
19	Translation initialize macro fail
20	Translation initialize macro invalid data received
21	Translation initialize macro some DS1 provisioning changed
22	Clamp PSC macro reject
23	Clamp PSC MACRO FAIL
24	PSC macro internal failure
25	Unclamp PSC macro reject in configuration
26	Unclamp PSC macro fail in configuration
27	Unclamp PSC macro internal failure in configuration
28	Compensate USEC macro reject
29	Compensate USEC macro fail
30	Schedule fail for macro
31	Timeout fail

Status of Configuration Request List (Bits 3-9) (Contd)

Decimal	Meaning
32	Polling fail
33	Invalid configuration number (D3U and SPU only)
34	Invalid DS3 yellow option (D3U only)
35	Configuration change to provisioned DS3 (D3U only)
36	Configuration change to provisioned DS1 (D3U only)
37	Unit software error
38	PSC PCM babble error
39	Problem with re-restore due to a failed translation_initialize macro
40	Audit of configuration data sent to PSC failed (D3U and SPU only)
41	PCM babble or CB babble fail
42	Trouble to read PSC status register
43	USEC protection switch update fail (D3U and SPU only)
44	PSC not in RAM
45	Two out of PCM, CB and PEST fail
46	D3U/SPU/IBU RST TEST — CB access — PSC TDR check test fails
47	D3U/SPU/IBU RST TEST — TSI TDR check test fails
48	Readfile of XCVR returned invalid (IBU only)
49	Returned XCVR file does not exist in FDT (IBU only)
50	Readfile of XCVR returns error in file header (IBU only)
51	Flashpump macro error in XCVR file or flash (IBU only)
52	Flashpump macro for XCVR failed with macro RAM checksum error (IBU only)
53	Flashpump macro for XCVR failed copy over control bus (IBU only)
54	Readfile of TST returned invalid (IBU only)
55	Returned TST file does not exist in FDT (IBU only)

Status of Configuration Request List (Bits 3-9) (Contd)

Decimal	Meaning
56	Readfile of TST returns error in file header (IBU only)
57	Flashpump macro error in TST file or flash (IBU only)
58	Flashpump macro for TST failed with macro RAM checksum error (IBU only)
59	Flashpump macro for TST failed copy over control bus (IBU only)
60	XCVR DSP flashpump macro failed (IBU only)
61	TST DSP flashpump macro failed (IBU only)
62	R2 PM Configuration values not valid (D3U only)
63	R3 functionality not supported (D3U only)
64	In-band, A/B configuration, mutually exclusive (D3U only)
65	Invalid configuration number transition (SPU only)
66	Invalid Tone disable (SPU only)
67	Hybrid return loss option (SPU only)
68	True voice type (SPU only)
69	Internal error (SPU only)
70	PCIS MAP update macro rejected
71	PCIS MAP update macro failed
72	Polling fail (IBU only)

Peripheral Subunit Maintenance Code (Bits 20-23)

Code	Meaning
0	Subunit is normal
1	OOS subunit is normal
2	Subunit CONTR is duplex failed
3	OOS subunit CONTR is duplex failed
4	Subunit connecting TSI is duplex failed
5	Subunit is unequipped
6	OOS subunit connecting TSI is duplex failed
7	Subunit is in growth
8	Subunit CONTR and connecting TSI are duplex failed
9	OOS subunit CONTR and connecting TSI are duplex failed
10	Don’t allow protection switch for this subunit
11	Subunit in diagnostic
12	Subunit left OOS following phase

D3USTAT—D3U Status Register

Bit 0 = Message pending from the D3U. D3U processor has the ability to set/reset this bit (MSGPND)
1 = Active/Standby signal from Controller 0, active high. Redundant active signals are provided by both XTSI controllers for reliability (ACTIVE0A)
2 = Active/Standby signal from Controller 0, active high. Redundant active signals are provided by both XTSI controllers for reliability (ACTIVE0B)
3 = Active/Standby signal from Controller 1, active high. Redundant active signals are provided by both XTSI controllers for reliability (ACTIVE1A)
4 = Active/Standby signal from Controller 1, active high. Redundant ACTIVE signals are provided by both XTSI controllers for reliability (ACTIVE1B)
5 = Signal that indicates which controller the D3U believes is active (ACTIVE)
6 = PCM bandwidth verify bit 0. Should match D3U CNTL bits 4 and 5 (PCMBWV0)
7 = PCM bandwidth verify bit 1. Should match D3U CNTL bits 4 and 5 (PCMBWV1)
8 = Present state of the ACK bit from the FBI (PSCACK)
9 = Present state of the OS bit from the FBI (PSCOS)
10 = Indicates that both input PCM buses of controller 0 are clamped (PCMIN0CL)
11 = Indicates that both input PCM buses of controller 1 are clamped (PCMIN1CL)
12 = 48V to 5V Power Converter A is Off (PCONOFFA)
13 = 48V to 5V Power Converter B is Off (PCONOFFB)
14 = 48V lost at 48V to 5V converter input, branch A (48VCONVA)
15 = 48V lost at 48V to 5V converter input, branch B (48VCONVB)
16 = 48V lost at input to in-rush circuit, branch A (48VRUSHA)

D3USTAT—D3U Status Register (Contd)

Bit 17 = 48V lost at input to in-rush circuit, branch B (48VRUSHB)
18 = 12-volt lost from controller 0 (12VSNS0)
19 = 12-volt lost from controller 1 (12VSNS1)
20 = Indicates that the D3U processor is executing from its RAM operating system. D3U processor has the ability to set/reset this bit (OSRAM)
21 = Indicates that the D3U processor is frozen and initiated background mode (PFREEZE)
22 = Utility paddleboard present bit (UTILBRD)
23 = Unused

D3UESR—D3U Error Source Register

Bit 0 = Control Bus data parity error, byte 0 (CBDPE0)
1 = Control Bus data parity error, byte 1 (CBDPE1)
2 = Control Bus data parity error, byte 2 (CBDPE2)
3 = Control Bus data parity error, byte 3 (CBDPE3)
4 = Time-Slot Count even bits parity error (TSCPEE)
5 = Time-Slot Count odd bits parity error (TSCPEO)
6 = PCM out bus 0 (2) busy/idle error. (PCM bus busy/idle bits don't agree.) (PCMBIE0)
7 = PCM out bus 1 (3) busy/idle error. (PCM bus busy/idle bits don't agree.) (PCMBIE1)
8 = PCM out bus 0 (2) parity error (PCMOPE0)
9 = PCM out bus 1 (3) parity error (PCMOPE1)
10 = PCM out sequence error (PCMOSEQ)
11 = PCM in sequence error (PCMISEQ)
12 = PCM Control Interface Error (TSC state machine error) (PCMTCLE)
13 = DS1 clock phase error (DS1CLKPE)
14 = 33MHz clock phase error (CLKPE)
15 = D3U Processor Halt (PHALT)
16 = D3U Processor bus error (PBUSE)
17 = D3U Processor parity error (PPARE)
18 = Software error. D3U processor will have the ability to set this bit (D3USWERR)
19 = CSP signaling interface error (SIGINTE)
20-23 = Unused

D3UCTL—D3U Control Register

Bit 0 = Control Bus Address Loop-around. When set, a read of any D3U address causes the address value in the Control Bus Address Latch to be put out on the Control Bus Address/Data bus. This bit must be reset to resume normal operation (CBALOOP)

1 = Enable the Exercise Register to allow board faults to occur (D3UEXEREN)

2 = Hard reset for the D3U Processor. XTC must set this bit and wait at least 8 EXEC instructions before clearing for a valid reset to occur. To reset the whole board, use the SD Interface (ACK, OS) (D3URESET)

3 = Interrupt the D3U Processor. D3U processor has the ability to clear this bit after an interrupt (D3UINT)

4 = PCM Bandwidth select bit 0 (See PCM Bandwidth Select Assignment) (PCMBWS0)

5 = PCM Bandwidth select bit 1 (See PCM Bandwidth Select Assignment) (PCMBWS1)

6 = Dual Power Restart - To restart the disabled power converter, set for 1 second, then clear. See the D3U Status Register for details on detecting a disabled power converter (DPRSTRT1)

7-23 = Unused

PCM Bandwidth Select Assignment

DS3 Facility Number	Subunit Number	PCM Bandwidth Select 1	PCM Bandwidth Select 0
No Facility	—	0	0
DS3 Facility 0	D3U 0	0	1
DS3 Facility 1	D3U 1	1	0
DS3 Facility 2	D3U 2	1	1
DS3 Facility 3	D3U 3	0	1
DS3 Facility 4	D3U 4	1	0
DS3 Facility 5	D3U 5	1	1
Spare	D3U6	0	1
Spare	D3U7	0	1

D3UEXR—D3U Exercise Register

Bit 0 = Force TSC even bits parity error. (Affects ESR bit 4) (FTSCPEE)
1 = Force TSC odd bits parity error. (Affects ESR bit 5) (FTSCPEO)
2 = Force PCM out bus 0 busy/idle error. (Affects ESR bit 6) (FPCMBIE0)
3 = Force PCM out bus 1 busy/idle error. (Affects ESR bit 7) (FPCMBIE1)
4 = Force PCM out bus 0 parity error. (Affects ESR bit 8) (FPCMOPE0)
5 = Force PCM out bus 1 parity error. (Affects ESR bit 9) (FPCMOPE1)
6 = Force PCM decode error (FPCMDE)
7 = Force PCM load error (FPCMLE)
8 = Force DS1 clock phase error (FDS1CPE)
9 = Force 33MHz clock phase error (FCLKPE)
10 = Force Power Alarm (D3U is inhibited from power down) (FPALRM)
11 = Force PCM Control Address parity error. (Affects ESR bit 10.) (FPCMCAPE)
12 = Force PCM Control Data parity error. (Affects ESR bit 10.) (FPCMCDPE)
13 = Controller 1 Scan Lead Inversion. (Inverts both scan signals to Controller 1) (C1SCNINV)
14 = Inhibit 48-volt feed to in-rush circuit. (Affects D3USTAT bits 12 - 17.) (INH48V)
15 = Select 48-volt in-rush feed (0 = Bus A, 1 = Bus B). (Affects D3USTAT bits 12 -17.) (SEL48V)
16 = Inhibit major alarm. (External alarm) (INHMAJOR)
17 = Listen to Standby Controller (LSN2STBY)
18-23 = Unused

TRANS1—D3U Translation Data Word 1

Bit 0-5 = If D3U 0, D3U 1, D3U 2, or D3U 6; Overall D3U equipage is:
- 0-1 = D3U 0 Equipage (XLUD3UEQ0)
- 2-3 = D3U 1 Equipage (XLUD3UEQ1)
- 4-5 = D3U 2 Equipage (XLUD3UEQ2)

Bit 0-5 = If D3U 3, D3U 4, D3U 5, or D3U 7; Overall D3U equipage is:
- 0-1 = D3U 3 Equipage (XLUD3UEQ3)
- 2-3 = D3U 4 Equipage (XLUD3UEQ4)
- 4-5 = D3U 5 Equipage (XLUD3UEQ5)

6-11 = Unused
12-15 = Valid port equipage type. (is 6 for D3U) (XL4UPRTYPE)
16-23 = Unused

TRANS2—D3U Translation Data Word 2

Bit 0-15 = Unused
16-18 = Spare D3U software version (if D3U 0-2 or 6 spare is D3U 6, else spare is D3U 7) (XL4USFVD3US)
19-21 = Spare D3U hardware version (if D3U 0-2 or 6 spare is D3U 6, else spare is D3U 7) (XL4USD3UV)
22-23 = Spare D3U equipage (if D3U 0-2 or 6 spare is D3U 6, else spare is D3U 7) (XL4SD3UE)

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS3—D3U Translation Data Word 3

Bit 0-11 = Unused
12 = D3U application (XL4UDU_APP)
13 = D3U maximum line build out for cable length (XL4UDU_MXLB)
14-15 = D3U remote alarm indication (XL4UDU_RALRM)
16-18 = Software version of D3U (XL4USFVD3U_)
19-21 = Hardware version of D3U (XL4UVD3U_)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS4—D3U Translation Data Word 4

Bit 0 = D3U Digroup 1 Equipage (XL4UDU_EQDG01)
1 = D3U Digroup 1 Frame Format (XL4UDU_FFDG01)
2 = D3U Digroup 1 2-Wire Termination (XL4UDU_TWDG01)
3 = D3U Digroup 1 In-Band Signaling Equipage (XL4UDU_IBDG01)
6 = D3U Digroup 2 Equipage (XL4UDU_EQDG02)
7 = D3U Digroup 2 Frame Format (XL4UDU_FFDG02)
8 = D3U Digroup 2 2-Wire Termination (XL4UDU_TWDG02)
9 = D3U Digroup 2 In-Band Signaling Equipage (XL4UDU_IBDG02)
12 = D3U Digroup 3 Equipage (XL4UDU_EQDG03)
13 = D3U Digroup 3 Frame Format (XL4UDU_FFDG03)
14 = D3U Digroup 3 2-Wire Termination (XL4UDU_TWDG03)
15 = D3U Digroup 3 In-Band Signaling Equipage (XL4UDU_IBDG03)
18 = D3U Digroup 4 Equipage (XL4UDU_EQDG04)
19 = D3U Digroup 4 Frame Format (XL4UDU_FFDG04)
20 = D3U Digroup 4 2-Wire Termination (XL4UDU_TWDG04)
21 = D3U Digroup 4 In-Band Signaling Equipage (XL4UDU_IBDG04)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS5—D3U Translation Data Word 5

Bit 0 = D3U Digroup 5 Equipage (XL4UDU_EQDG05)
1 = D3U Digroup 5 Frame Format (XL4UDU_FFDG05)
2 = D3U Digroup 5 2-Wire Termination (XL4UDU_TWDG05)
3 = D3U Digroup 5 In-Band Signaling Equipage (XL4UDU_IBDG05)
6 = D3U Digroup 6 Equipage (XL4UDU_EQDG06)
7 = D3U Digroup 6 Frame Format (XL4UDU_FFDG06)
8 = D3U Digroup 6 2-Wire Termination (XL4UDU_TWDG06)
9 = D3U Digroup 6 In-Band Signaling Equipage (XL4UDU_IBDG06)
12 = D3U Digroup 7 Equipage (XL4UDU_EQDG07)
13 = D3U Digroup 7 Frame Format (XL4UDU_FFDG07)
14 = D3U Digroup 7 2-Wire Termination (XL4UDU_TWDG07)
15 = D3U Digroup 7 In-Band Signaling Equipage (XL4UDU_IBDG07)
18 = D3U Digroup 8 Equipage (XL4UDU_EQDG08)
19 = D3U Digroup 8 Frame Format (XL4UDU_FFDG08)
20 = D3U Digroup 8 2-Wire Termination (XL4UDU_TWDG08)
21 = D3U Digroup 8 In-Band Signaling Equipage (XL4UDU_IBDG08)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS6—D3U Translation Data Word 6

Bit 0 = D3U Digroup 9 Equipage (XL4UDU_EQDG09)
1 = D3U Digroup 9 Frame Format (XL4UDU_FFDG09)
2 = D3U Digroup 9 2-Wire Termination (XL4UDU_TWDG09)
3 = D3U Digroup 9 In-Band Signaling Equipage (XL4UDU_IBDG09)
6 = D3U Digroup 10 Equipage (XL4UDU_EQDG10)
7 = D3U Digroup 10 Frame Format (XL4UDU_FFDG10)
8 = D3U Digroup 10 2-Wire Termination (XL4UDU_TWDG10)
9 = D3U Digroup 10 In-Band Signaling Equipage (XL4UDU_IBDG10)
12 = D3U Digroup 11 Equipage (XL4UDU_EQDG11)
13 = D3U Digroup 11 Frame Format (XL4UDU_FFDG11)
14 = D3U Digroup 11 2-Wire Termination (XL4UDU_TWDG11)
15 = D3U Digroup 11 In-Band Signaling Equipage (XL4UDU_IBDG11)
18 = D3U Digroup 12 Equipage (XL4UDU_EQDG12)
19 = D3U Digroup 12 Frame Format (XL4UDU_FFDG12)
20 = D3U Digroup 12 2-Wire Termination (XL4UDU_TWDG12)
21 = D3U Digroup 12 In-Band Signaling Equipage (XL4UDU_IBDGxx)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS7—D3U Translation Data Word 7

Bit 0 = D3U Digroup 13 Equipage (XL4UDU_EQDG13)
1 = D3U Digroup 13 Frame Format (XL4UDU_FFDG13)
2 = D3U Digroup 13 2-Wire Termination (XL4UDU_TWDG13)
3 = D3U Digroup 13 In-Band Signaling Equipage (XL4UDU_IBDG13)
6 = D3U Digroup 14 Equipage (XL4UDU_EQDG14)
7 = D3U Digroup 14 Frame Format (XL4UDU_FFDG14)
8 = D3U Digroup 14 2-Wire Termination (XL4UDU_TWDG14)
9 = D3U Digroup 14 In-Band Signaling Equipage (XL4UDU_IBDG14)
12 = D3U Digroup 15 Equipage (XL4UDU_EQDG15)
13 = D3U Digroup 15 Frame Format (XL4UDU_FFDG15)
14 = D3U Digroup 15 2-Wire Termination (XL4UDU_TWDG15)
15 = D3U Digroup 15 In-Band Signaling Equipage (XL4UDU_IBDG15)
18 = D3U Digroup 16 Equipage (XL4UDU_EQDG16)
19 = D3U Digroup 16 Frame Format (XL4UDU_FFDG16)
20 = D3U Digroup 16 2-Wire Termination (XL4UDU_TWDG16)
21 = D3U Digroup 16 In-Band Signaling Equipage (XL4UDU_IBDG16)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS8—D3U Translation Data Word 8

Bit 0 = D3U Digroup 17 Equipage (XL4UDU_EQDG17)
1 = D3U Digroup 17 Frame Format (XL4UDU_FFDG17)
2 = D3U Digroup 17 2-Wire Termination (XL4UDU_TWDG17)
3 = D3U Digroup 17 In-Band Signaling Equipage (XL4UDU_IBDG17)
6 = D3U Digroup 18 Equipage (XL4UDU_EQDG18)
7 = D3U Digroup 18 Frame Format (XL4UDU_FFDG18)
8 = D3U Digroup 18 2-Wire Termination (XL4UDU_TWDG18)
9 = D3U Digroup 18 In-Band Signaling Equipage (XL4UDU_IBDG18)
12 = D3U Digroup 19 Equipage (XL4UDU_EQDG19)
13 = D3U Digroup 19 Frame Format (XL4UDU_FFDG19)
14 = D3U Digroup 19 2-Wire Termination (XL4UDU_TWDG19)
15 = D3U Digroup 19 In-Band Signaling Equipage (XL4UDU_IBDG19)
18 = D3U Digroup 20 Equipage (XL4UDU_EQDG20)
19 = D3U Digroup 20 Frame Format (XL4UDU_FFDG20)
20 = D3U Digroup 20 2-Wire Termination (XL4UDU_TWDG20)
21 = D3U Digroup 20 In-Band Signaling Equipage (XL4UDU_IBDG20)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS9—D3U Translation Data Word 9

Bit 0 = D3U Digroup 21 Equipage (XL4UDU_EQDG21)
1 = D3U Digroup 21 Frame Format (XL4UDU_FFDG21)
2 = D3U Digroup 21 2-Wire Termination (XL4UDU_TWDG21)
3 = D3U Digroup 21 In-Band Signaling Equipage (XL4UDU_IBDG21)
6 = D3U Digroup 22 Equipage (XL4UDU_EQDG22)
7 = D3U Digroup 22 Frame Format (XL4UDU_FFDG22)
8 = D3U Digroup 22 2-Wire Termination (XL4UDU_TWDG22)
9 = D3U Digroup 22 In-Band Signaling Equipage (XL4UDU_IBDG22)
12 = D3U Digroup 23 Equipage (XL4UDU_EQDG23)
13 = D3U Digroup 23 Frame Format (XL4UDU_FFDG23)
14 = D3U Digroup 23 2-Wire Termination (XL4UDU_TWDG23)
15 = D3U Digroup 23 In-Band Signaling Equipage (XL4UDU_IBDG23)
18 = D3U Digroup 24 Equipage (XL4UDU_EQDG24)
19 = D3U Digroup 24 Frame Format (XL4UDU_FFDG24)
20 = D3U Digroup 24 2-Wire Termination (XL4UDU_TWDG24)
21 = D3U Digroup 24 In-Band Signaling Equipage (XL4UDU_IBDG24)
22-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the D3U number.

TRANS10—D3U Translation Data Word 10

Bit 0 = D3U Digroup 25 Equipage (XL4UDU_EQDG25)
1 = D3U Digroup 25 Frame Format (XL4UDU_FFDG25)
2 = D3U Digroup 25 2-Wire Termination (XL4UDU_TWDG25)
3 = D3U Digroup 25 In-Band Signaling Equipage (XL4UDU_IBDG25)
6 = D3U Digroup 26 Equipage (XL4UDU_EQDG26)
7 = D3U Digroup 26 Frame Format (XL4UDU_FFDG26)
8 = D3U Digroup 26 2-Wire Termination (XL4UDU_TWDG26)
9 = D3U Digroup 26 In-Band Signaling Equipage (XL4UDU_IBDG26)
12 = D3U Digroup 27 Equipage (XL4UDU_EQDG27)
13 = D3U Digroup 27 Frame Format (XL4UDU_FFDG27)
14 = D3U Digroup 27 2-Wire Termination (XL4UDU_TWDG27)
15 = D3U Digroup 27 In-Band Signaling Equipage (XL4UDU_IBDG27)
18 = D3U Digroup 28 equipage (XL4UDU_EQDG28)
19 = D3U Digroup 28 Frame Format (XL4UDU_FFDG28)
20 = D3U Digroup 28 2-Wire Termination (XL4UDU_TWDG28)
21 = D3U Digroup 28 In-Band Signaling Equipage (XL4UDU_IBDG28)
22-23 = Unused

XTSI IBU Registers (via TTY Request)

IBUSTATUS IBUSTAT IBUESR IBUCTL IBUEXR TRANS1 FW_VERL FW_VERH SW_VERL SW_VERH

IBUSSTATUS—IBU Software Status

Bit 0 = IBU pested via TTY message (SPSPST)
1-2 = Unused
3-9 = IBU configuration status. (See Status of Configuration Request List in the XTSI D3U Registers for layout.) A zero indicates successful configuration request and non-zero indicates an error in configuration request (CNFGSTAT)
10-11 = Unused
12 = IBU Out-of-Service (OS)
13 = IBU removed via TTY message (RMVTTY)
14 = IBU removed pending (request OS) (RMVPND)
15-19 = Unused
20-23 = See Peripheral Subunit Maintenance Code (MAIN) in the XTSI D3U Registers for layout

IBUSTAT—IBU Status Register

Bit 0 = Message pending from the IBU. IBU processor (MCU) set by a one (1) from PORT D9 (Bit 6) (MSGPND)
1 = Active/Standby signal from Controller 0, active high. Redundant ACTIVE signals are provided by both XTSI controllers for reliability (ACTIVE0A)
2 = Active/Standby signal from Controller 0, active high. Redundant ACTIVE signals are provided by both XTSI controllers for reliability (ACTIVE0B)
3 = Active/Standby signal from Controller 1, active high. Redundant ACTIVE signals are provided by both XTSI controllers for reliability (ACTIVE1A)
4 = Active/Standby signal from Controller 1, active high. Redundant ACTIVE signals are provided by both XTSI controllers for reliability (ACTIVE1B)
5 = Signal that indicates which controller the IBU believes is active (Derived from 4 Active Signals) (ACTIVE)
6-7 = Spare
8 = Present state of the ACK bit from the FBI (PSCACK)
9 = Present state of the OS bit from the FBI (PSCOS)
10 = Indicates that both PCM Input Buses of Controller 0 are clamped (PCMIN0CL)
11 = Indicates that both PCM Input Buses of Controller 1 are clamped (PCMIN1CL)
12 = 48V to 3.3V Power Converter A is Off (PCONOFFA)
13 = 48V to 3.3V Power Converter B is Off (PCONOFFB)
14 = 48V lost at 48V to 3.3V converter input, branch A (48VCONVA)
15 = 48V lost at 48V to 3.3V converter input, branch B (48VCONVB)
16 = Low Input Voltage/power (LIP LED) on feed 48V to inrush circuit, branch A (48VRUSHA)
17 = Low Input Voltage/power (LIP LED) on feed 48V to inrush circuit, branch B (48VRUSHB)

IBUSTAT—IBU Status Register (Contd)

18 = 12-volt lost from controller 0 (12VSNS0)
19 = 12-volt lost from controller 1 (12VSNS1)
20 = Indicates that the IBU processor is executing from its RAM operating system. This bit follows the signal from MCU PORT D7 (bit 8) (OSRAM)
21 = Spare
22 = Utility paddleboard present bit (UTILBRD)
23 = Spare
24-31 = Unused

IBUCTL—IBU Control Register

Bit 0 = Control Bus Address Loop-around. When set, a read of any IBU address will cause the address value in the Control Bus Address Latch to be put out on the Control Bus Address/Data bus. This bit must be cleared to resume normal operation (CBALOOP)
1 = Enable the Exercise Register to allow board faults to occur (IBUEXEREN)
2 = Hard reset for the IBU Processor (IBURESET)
3 = High Priority Message Interrupt to the IBU Processor. The MCU will clear this bit to acknowledge the reception of the interrupt. It may be clear by a one (1) from MCU via PORT D11 (Bit 4) (IBUINT)
4 = Spare; reserved for maintenance(0)/operational(1) TS mapping
5 = Spare
6 = Dual Power Restart (DPWRSTRT)
7 = Spare
8-23 = Unused

IBUESR—IBU Error Source Register

Bit 0 = Control Bus Data Parity Error, Byte 0 (CBDPE0)
1 = Control Bus Data Parity Error, Byte 1 (CBDPE1)
2 = Control Bus Data Parity Error, Byte 2 (CBDPE2)
3 = Control Bus Data Parity Error, Byte 3 (CBDPE3)
4 = Parity Error Over Even Bits of TSC (TSCEPE)
5 = Parity Error Over Odd Bits of TSC (TSCOPE)
6 = PCM Control Memory Parity Error Over Whole Data Word (PCMDATPE)
7 = Clock Lost Error from MCU's Clock Branch (CLKMCU)
8 = PCM Output Bus 0 Parity Error from TSI (OBUS0)
9 = PCM Output Bus 1 Parity Error from TSI (OBUS1)
10 = PCM Output Bus 0 Parity Error from PBI (PCM Bus Interface) FPGA's RAM (ORAM0)
11 = PCM Output Bus 1 Parity Error from PBI (PCM Bus Interface) FPGA's RAM (ORAM1)
12 = (IRAM0) PCM Input Bus 0 Parity Error from PCMIO FPGA's RAM
13 = PCM Input Bus 1 Parity Error from PCMIO FPGA's RAM (IRAM1)
14-15 = Spare
16 = Clock Error from Composite DSP Error Register (CLKDSP)
17 = Program Error from Composite DSP Error Register (PRGDSP)
18 = Link Error on serial PCMO from Composite DSP Error Register (SPODSP)
19 = Link Error on serial PCMI from Composite DSP Error Register (SPIDSP)
20 = Spare
21 = Unassigned (reserved for MCU set by a one from Port D05 (bit 10)
22 = Unassigned (reserved for MCU set by a one from Port D04 (bit 11)
23 = IBU Software Error. IBU processor controls this bit by setting Port D03 [Bit 12]. (IBUSWERR)

IBUEXR—IBU Exercise Register

Bit 0 = Force PCM Control RAM Address (TSC) Parity Error (FCRAMAPE)
1 = Force PCM Control RAM Data Parity Error (FCRAMDPE)
2 = Force Clock error from MCU (FCLKMCU)
3 = Spare
4 = Write even parity into PBI FPGA's buffer RAM on PCM-o Bus 0 (FORAM0)
5 = Write even parity into PBI FPGA's buffer RAM on PCM-o Bus 1 (FORAM1)
6 = Write even parity into PBI FPGA's buffer RAM on PCM-i us 0 (FIRAM0)
7 = Write even parity into PBI FPGA's buffer RAM on PCM-i us 1 (FIRAM1)
8-10 = DSP Selection for (FSPODSP) IBUEXR[11]. Valid ran is 0-5. (FSPSELDSP)
11 = Force error on serial link on DSP selected by FSPSELDSP (bit 8-10) (FSPODSP)
12-13 = Spare
14 = Force Power Alarm (IBU is inhibited from power down) (FPALRM)
15 = Invert SCAN lead on Controller 1 (C1SCNINV)
16 = Inhibit 48-volt feed from inrush circuit (INH48V)
17 = Select 48-volt inrush circuit for bit 16 (0 = Bus A, 1 = Bus B). (SEL48V)
18 = Inhibit Major Alarm (INHMAJOR)
19 = Listen to Standby Controller (LSN2STBY)
20-23 = Spare

TRANS1—IBU Translation Data Word 1

Bit 0 = Type of signaling—receivers/transmitters (XL4UIBSIG)
- 0 = IBU supports MF signaling
- 1 = IBU supports DTMF signaling

1 = Type of miscellaneous service circuits (XL4UIBUMISC)
- 0 = IBU supports 16 CCT service circuits
- 1 = IBU supports 16 CCT service circuits and miscellaneous service circuits enabled

2-14 = Unused
15 = Indicates service circuit TANs associated with IBU have been reserved (XL4UIBUTANRSV)
16-18 = IBU Software version (XL4USFVIBU)
19-21 = IBU Hardware version (XL4UHIBU)
22-23 = IBU equippage (XL4UIBUE)

FW_VERH holds the Most Significant 8 bits of Firmware Version Number
FW_VERL holds the Least Significant 24 bits of Firmware Version Number Firmware Version Number is store in IBU Share Memory (ADR X(84)). Firmware Version Number is AABBCCDD (32 bits word with each letter indicates a byte).

A = Issue # stored in FW_VERH
B = LOAD # stored in FW_VERL
C = GENERIC # stored in FW_VERL
D = Hardware type stored in FW_VERL always equal to 4

SW_VERH holds the Most Significant 8 bits of Software Version Number
SW_VERL holds the Least Significant 24 bits of Software Version Number Software Version Number is store in IBU Share Memory (ADR X(85)). Software Version Number is AABBCCDD (32 bits word with each letter indicates a byte).

A = Issue # stored in SW_VERH
B = LOAD # stored in SW_VERL
C = GENERIC # stored in SW_VERL
D = Software Version stored in SW_VERL always equal to 4

XTSI SPU Registers (via TTY Request)

SPSSTATUS SPSSTAT SPSESR SPSCTL SPSEXR TRANS1 TRANS2* TRANS3*
TRANS4* TRANS5*

* If the spare SPU is requested (SPU 10 or SPU 11), these words (TRANS2-5) are not included in the dump.

SPSSTATUS—SPU Software Status

Bit 0 = SPU pested via TTY message (SPSPST)
1-2 = Unused
3-9 = SPU configuration status. (See Status of Configuration Request List in the XTSI D3U Registers for layout.) A zero indicates successful configuration request and non-zero indicates an error in configuration request (CNFGSTAT)
10-11 = Unused
12 = SPU Out-of-Service (OS)
13 = SPU removed via TTY message (RMVTTY)
14-19 = Unused
20-23 = See Peripheral Subunit Maintenance Code (MAIN) in the XTSI D3U Registers for layout

SPSSTAT—SPU Status Register

Bit 0 = Message pending from the SPU. SPU processor has the ability to set/reset this bit (MSGPND)
1 = Active/Standby signal from Controller 0, active high. Redundant active signals are provided by both XTSI controllers for reliability (ACTIVE0A)
2 = Active/Standby signal from Controller 0, active high. Redundant active signals are provided by both XTSI controllers for reliability (ACTIVE0B)
3 = Active/Standby signal from Controller 1, active high. Redundant active signals are provided by both XTSI controllers for reliability (ACTIVE1A)
4 = Active/Standby signal from Controller 1, active high. Redundant ACTIVE signals are provided by both XTSI controllers for reliability (ACTIVE1B)
5 = Signal that indicates which controller the SPU believes is active (ACTIVE)
6-7 = Not Used
8 = Present state of the ACK bit from the FBI (SPSACK)
9 = Present state of the OS bit from the FBI (SPSOS)
10 = Indicates that both input PCM Buses of controller 0 are clamped (PCMIN0CL)
11 = Indicates that both input PCM Buses of controller 1 are clamped (PCMIN1CL)
12 = 48V to 5V Power Converter A is Off (PCONOFFA)
13 = 48V to 5V Power Converter B is Off (PCONOFFB)
14 = 48V lost at 48V to 5V converter input, branch A (48VCONVA)
15 = 48V lost at 48V to 5V converter input, branch B (48VCONVB)
16 = 48V lost at input to in-rush circuit, branch A (48VRUSHA)
17 = 48V lost at input to in-rush circuit, branch B (48VRUSHB)
18 = 12-volt lost from controller 0 (12VSNS0)
19 = 12-volt lost from controller 1 (12VSNS1)

SPSSTAT—SPU Status Register (Contd)

20 = Indicates that the SPU processor is executing from its RAM operating system. SPU processor has the ability to set/reset this bit (OSRAM)
21 = Indicates that the SPU processor is frozen and initiated background mode (PFREEZE)
22 = Utility paddleboard present bit (UTILBRD)
23 = Unused

SPSESR—SPU Error Source Register

Bit 0 = Control Bus data parity error, byte 0 (CBDPE0)
1 = Control Bus data parity error, byte 1 (CBDPE1)
2 = Control Bus data parity error, byte 2 (CBDPE2)
3 = Control Bus data parity error, byte 3 (CBDPE3)
4 = Time-Slot Count even bits parity error (TSCPEE)
5 = Time-Slot Count odd bits parity error (TSCPEO)
6 = PCM out bus 0 error (PCMOE0)
7 = PCM out bus 1 error (PCMOE1)
8 = PCM in bus 0 error (PCMIE0)
9 = PCM in bus 1 error (PCMIE1)
10 = PCM out error summary bit (EPCMOES1)
11 = PCM in error summary bit (EPCMIES1)
12 = TrueVoice summation error (ETVSM1)
13 = ECP/R4 summation error (EECPSUM1)
14 = 33MHz clock phase error (CLKPE)
15 = SPU Processor Halt (PHALT)
16 = SPU Processor bus error (PBUSE)
17 = SPU Processor parity error (PPARE)
18 = SPU Software error. SPU processor has the ability to set this bit (SPSSWERR)
19 = PCM out bus 0 busy idle error (0EPCMBI1)
20 = PCM out bus 1 busy idle error (1EPCMBI1)
21-23 = Unused

SPSCTL—SPU Control Register

Bit 0 = Control Bus Address Loop-around. When set, a read of any SPU address causes the address value in the Control Bus Address Latch to be put out on the Control Bus Address/Data bus. This bit must be reset to resume normal operation (CBALOOP)

1 = Enable the Exercise Register to allow board faults to occur (SPSEXEREN)

2 = Hard reset for the SPU Processor. XTC must set this bit and wait at least 8 EXEC instructions before clearing for a valid reset to occur. To reset the whole board, use the SD Interface (ACK, OS) (SPSRESET)

3 = Interrupt the SPU Processor. SPU processor has the ability to clear this bit after an interrupt (SPSINT)

4 = Dual power restart (DPRSTR1)

5 = SPU PCM channel configuration logic address 0 (See SPU PCM Channel Configuration Logic Address) (LOGADR0)

6 = SPU PCM channel configuration logic address 1 (See SPU PCM Channel Configuration Logic Address) (LOGADR1)

7 = SPU PCM channel configuration logic address 2 (See SPU PCM Channel Configuration Logic Address) (LOGADR2)

8-23 = Unused

	SPU PCM Channel Configuration Logic Address Assignment			
	SPU Number	**LOGADR2**	**LOGADR1**	**LOGADR0**
Spare	SPU 10	0	0	0
	SPU 0	0	0	1
	SPU 1	0	1	0
	SPU 2	0	1	1
	SPU 3	1	0	0
	SPU 4	1	0	1
Spare	SPU 11	0	0	0
	SPU 5	0	0	1
	SPU 6	0	1	0
	SPU 7	0	1	1
	SPU 8	1	0	0
	SPU 9	1	0	1

SPSEXR—SPU Exercise Register

Bit 0 = Force TSC even bits parity error (FTSCPEE)
1 = Force TSC odd bits parity error (FTSCPEO)
2 = Force PCM out bus 0 busy/idle error (F0PCMO1)
3 = Force PCM out bus 1 busy/idle error (F1PCMO1)
4 = Force PCM out bus 0 parity error (F0PCMI1)
5 = Force PCM out bus 1 parity error (F1PCMI1)
6 = Reserved
7 = Reserved
8 = Reserved
9 = Force 33MHz clock phase error (FCLKPE)
10 = Force Power Alarm (SPU is inhibited from power down) (FPALRM)
11 = Force ECP/R4 parity error (FECP0)
12 = Force TrueVoice parity error (FTVPE1)
13 = Controller 1 Scan Lead Inversion (C1SCNINV)
14 = Inhibit 48-volt feed to in-rush circuit (INH48V)
15 = Select 48-volt in-rush feed (0 = Bus A, 1 = Bus B) (SEL48V)
16 = Inhibit major alarm (INHMAJOR)
17 = Listen to Standby Controller (LSN2STBY)
18 = Force busy/idle error for PCM out bus 0 (0FPCMBI1)
19 = Force busy/idle error for PCM out bus 1 (1FPCMBI1)
20-23 = Unused

TRANS1—SPU Translation Data Word 1

Bit 0-15 = Unused
16-18 = Software version of Spare SPU (XL4USFVSPSS)
19-21 = Hardware version of Spare SPU (XL4UHVSPSS)
22-23 = Spare SPU equippage (XL4USPSUES)

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the SPU number.

TRANS2—SPU Translation Data Word 2

Bit 0-15 = Unused
16-18 = Software version of SPU (XL4USFVSPS_)
19-21 = Hardware version of SPU (XL4UHVSPS_)
22-23 = SPU equippage (XL4USPSUE_)

TRANS3—SPU Translation Data Word 3

Bit 0-1 = SPU echo cancellation tone-disabler for SPC 0 (XL4USPS_TD0)
- 0 = Tone-dialer 2100 Hz tone with phase reversal (4XLUSPSECTDPR)
- 1 = Tone-dialer 2100 Hz tone with or without phase reversal (or phase independent) (4XLUSPSECTDPS)
- 2 = Tone-dialer disabled (no tone disabling) (4XLUSPSECTDOFF)

2 = SPU echo cancellation Noise Matching for SPC 0 (XL4USPS_NM0)
- 0 = Noise matching enabled (4XLUSPSECNME)
- 1 = Noise matching disabled (4XLUSPSECNMD)

3-5 = SPU echo cancellation hybrid return loss for SPC 0 (XL4USPS_HR0)
- 0 = 6db hybrid return loss (4XLUSPSECHR6)
- 1 = 5db hybrid return loss (4XLUSPSECHR5)
- 2 = 4db hybrid return loss (4XLUSPSECHR4)
- 3 = 3db hybrid return loss (4XLUSPSECHR3)
- 4 = 2db hybrid return loss (4XLUSPSECHR2)
- 5 = 1db hybrid return loss (4XLUSPSECHR1)
- 6 = 0db hybrid return loss (4XLUSPSECHR0)

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the SPU number.

TRANS3—SPU Translation Data Word 3 (Contd)

12-13 = SPU echo cancellation tone-disabler for SPC 1
(Same states as bits 0-1) (XL4USPS_TD1)
14 = SPU echo cancellation Noise Matching for SPC 1 (Same states as bit 2) (XL4USPS_NM1)
15-17 = SPU echo cancellation hybrid return loss for SPC 1
(Same states as bits 3-5) (XL4USPS_HR1)
18-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the SPU number.

TRANS4—SPU Translation Data Word 4

Bit 0-1 = TV type for SPC 0 Digroup 0 on SPU (XL4USPS_TY0DG0)
- 0 = Enhance (4XLUSPSTYENH)
- 1 = Tone only (4XLUSPSTYTONY)
- 2 = None (4XLUSPSTYNONE)

2-3 = TV type for SPC 0 Digroup 1 on SPU (XL4USPS_TY0DG1) (Same values as bits 0-1)
4-5 = TV type for SPC 0 Digroup 2 on SPU (XL4USPS_TY0DG2) (Same values as bits 0-1)
6-7 = TV type for SPC 0 Digroup 3 on SPU (XL4USPS_TY0DG3) (Same values as bits 0-1)
8-9 = TV type for SPC 0 Digroup 4 on SPU (XL4USPS_TY0DG4) (Same values as bits 0-1)
10-11 = TV type for SPC 0 Digroup 5 on SPU (XL4USPS_TY0DG5) (Same values as bits 0-1)
12-13 = TV type for SPC 0 Digroup 6 on SPU (XL4USPS_TY0DG6) (Same values as bits 0-1)
14-15 = TV type for SPC 0 Digroup 7 on SPU (XL4USPS_TY0DG7) (Same values as bits 0-1)
16-17 = TV type for SPC 0 Digroup 8 on SPU (XL4USPS_TY0DG8) (Same values as bits 0-1)
18-23 = Unused

NOTE:
All underscores within the symbol names (symbols begin with XL4U) should be replaced with the SPU number.

TRANS5—SPU Translation Data Word 5

Bit 0-1 = TV type for SPC 1 Digroup 0 on SPU
(XL4USPS_TY1DG0)
0 = Enhance (4XLUSPSTYENH)
1 = Tone only (4XLUSPSTYTONY)
2 = None (4XLUSPSTYNONE)
2-3 = TV type for SPC 1 Digroup 1 on SPU
(XL4USPS_TY1DG1) (Same values as bits 0-1)
4-5 = TV type for SPC 1 Digroup 2 on SPU
(XL4USPS_TY1DG2) (Same values as bits 0-1)
6-7 = TV type for SPC 1 Digroup 3 on SPU
(XL4USPS_TY1DG3) (Same values as bits 0-1)
8-9 = TV type for SPC 1 Digroup 4 on SPU
(XL4USPS_TY1DG4) (Same values as bits 0-1)
10-11 = TV type for SPC 1 Digroup 5 on SPU
(XL4USPS_TY1DG5) (Same values as bits 0-1)
12-13 = TV type for SPC 1 Digroup 6 on SPU
(XL4USPS_TY1DG6) (Same values as bits 0-1)
14-15 = TV type for SPC 1 Digroup 7 on SPU
(XL4USPS_TY1DG7) (Same values as bits 0-1)
16-17 = TV type for SPC 1 Digroup 8 on SPU
(XL4USPS_TY1DG8) (Same values as bits 0-1)
18-23 = Unused

XTSI PCM Bus Mismatch Auxiliary Dump

				TRANS	TRANS
DUMP SIZE	TIME SLOT	TRANS C0	TRANS C1	QUERY C0	QUERY C1
PCMIL C0	PCMIL C1	PCMIH C0	PCMIH C1	PCMOL C0	PCMOL C1
PCMOH C0	PCMOH C1	TSM C0	TSM C1	SYNDR C0	SYNDR C1
SYNDR CALC	CLIENT	SUB-BRANCH	00000000	00000000	00000000
PSCX0	PSCX0 SWSTAT	PSCX0 HWSTAT	PSCX0 ESR	PSCX0 CTL	PSCX0 EXR
PSCX1	PSCX1 SWSTAT	PSCX1 HWSTAT	PSCX1 ESR	PSCX1 CTL	PSCX1 EXR
PSCX2	PSCX2 SWSTAT	PSCX2 HWSTAT	PSCX2 ESR	PSCX2 CTL	PSCX2 EXR
PSCX3	PSCX3 SWSTAT	PSCX3 HWSTAT	PSCX3 ESR	PSCX3 CTL	PSCX3 EXR
PSCX4	PSCX4 SWSTAT	PSCX4 HWSTAT	PSCX4 ESR	PSCX4 CTL	PSCX4 EXR
PSCX5	PSCX5 SWSTAT	PSCX5 HWSTAT	PSCX5 ESR	PSCX5 CTL	PSCX5 EXR

DUMP SIZE/TYPE (Word 0)

Octal 00004170

Bit 0 = TAG (0)
1-8 = Dump size (60 decimal)
9-12 = Dump type-XTSI PCM data mismatch=0(4)

TIMESLOT—Timeslot (Word 1)

Bit 0-11 = Time slot

TRANS—Translations RAM—Controller 0 or 1 (Words 2,3)

Bit 0-11 = Translation RAM value
12-13 = PCM bus

TRANS QUERY—Translations Query—Controller 0 or 1 (Words 4,5)

Bit 0-11 = Translation RAM value
12-13 = PCM bus

PCMIL—Controller 0 or 1 (Words 6,7)

Bit 0-7 = Input bus 0
8-15 = Input bus 1
16 = Input bus 0 parity bit
17 = Input bus 1 parity bit
18 = BM0 input MUX (multiplexer) select (TSXR0 bit 12)
19 = BM0 input MUX select (TSXR0 bit 13)
20 = BM1 input MUX select (TSXR0 bit 12)
21 = BM1 input MUX select (TSXR0 bit 13)

PCMIH—Controller 0 or 1 (Words 8,9)

Bit 0-7 = Input bus 2
8-15 = Input bus 3
16 = Input bus 2 parity bit
17 = Input bus 3 parity bit
18 = BM0 input MUX select (TSXR2 bit 12)
19 = BM0 input MUX select (TSXR2 bit 13)
20 = BM1 input MUX select (TSXR3 bit 12)
21 = BM1 input MUX select (TSXR3 bit 13)

PCMOL—Controller 0 or 1 (Words 10,11)

Bit 0-7 = Output bus 0
8-15 = Output bus 1
16 = Output bus 0 parity bus
17 = Output bus 1 parity bus
18 = TSM0 Busy/idle bit 12
19 = TSM0 Busy/idle bit 13
20 = TSM1 Busy/idle bit 12
21 = TSM1 Busy/idle bit 13

PCMOH—Controller 0 or 1 (Words 12,13)

Bit 0-7 = Output bus 2
8-15 = Output bus 3
16 = Output bus 2 parity bus
17 = Output bus 3 parity bus
18 = TSM2 Busy/idle bit 12
19 = TSM2 Busy/idle bit 13
20 = TSM3 Busy/idle bit 12
21 = TSM3 Busy/idle bit 13

TSM—Controller 0 or 1 (Words 14,15)

Bit 0-9 = TSM address
10-11 = Buffer partition
12 = Path busy/idle bit
13 = Forward voice control
14 = Transmit busy/idle bit

SYNDR—Syndrome Register—Controller 0 or 1 (Words 16,17)

Bit 0 = Bit 0 from each PCM bus and TSM0 bit 12
1 = Bit 1 from each PCM bus and TSM1 bit 12
2 = Bit 2 from each PCM bus and TSM2 bit 12
3 = Bit 3 from each PCM bus and TSM3 bit 12
4 = Bit 4 from each PCM bus and TSM0 bit 13
5 = Bit 5 from each PCM bus and TSM1 bit 13
6 = Bit 6 from each PCM bus and TSM2 bit 13
7 = Bit 7 from each PCM bus and TSM3 bit 13
8 = Parity bits from each PCM bus

SYNDR CALC—Calculated Syndrome Register—(Word 18)

Bit 0 = Bit 0 from each PCM bus and TSM0 bit 12
1 = Bit 1 from each PCM bus and TSM1 bit 12
2 = Bit 2 from each PCM bus and TSM2 bit 12
3 = Bit 3 from each PCM bus and TSM3 bit 12
4 = Bit 4 from each PCM bus and TSM0 bit 13
5 = Bit 5 from each PCM bus and TSM1 bit 13
6 = Bit 6 from each PCM bus and TSM2 bit 13
7 = Bit 7 from each PCM bus and TSM3 bit 13
8 = Parity bits from each PCM bus

CLIENT—(Word 19)

Bit 0-6 = Sub-member number
7-13 = Sub-unit type

Sub-Branch—(Word 20)

Bit 0-1 = Sub-branch number

The data layout is on the EVEN or ODD member of the XTSI frame and sub-branch within the member The data layout clients reside on sub-branch are as following:

PCM Sub-Branch Layout

Frame Member	PC_Sub-Branch	Client 1	Client 2	Client 3	Client 4	Client 5	Client 6
ATIXMEMN_E	0	SPS0	SPS1	SPS2	SPS3	SPS4	SPS10
	1	ALF0	ALF0	ALF0	ALF0	ALF0	ALF0
	2	D3U0	D3U1	D3U2	D3U6	SPARE0	SPARE2
ATIXMEMN_0	0	SPS5	SPS6	SPS7	SPS8	SPS9	SPS11
	1	ALF1	ALF1	ALF1	ALF1	ALF1	ALF1
	2	D3U3	D3U4	D3U5	D3U7	SPARE1	IBU0

PSCX Client (0-5) Subunit—(Words 24,30,36,42,48,54)

Bit 0-8 = Unit member number (UTMEM)
For D3U - Member number is between 0 - 7
For SPU - Member number is between 0 - 11
For IBU - Member number is between 0 - 8
9-11 = Unit type
0 = D3U
1 = SPU
2 = IBU

PSCX Client (0-5) HWSTAT—(Words 26,32,38,44,50,56)

If PSCX Client unit type is D3U, See XTSI D3U Registers (D3USTAT—D3U Status Register) for bit layout.

If PSCX Client unit type is SPU, See XTSI SPU Registers (SPSSTAT—SPU Status Register) for bit layout.

If PSCX Client unit type is IBU, See XTSI IBU Registers (IBUSTAT—IBU Status Register) for bit layout.

PSCX Client (0-5) SWSTAT—(Words 25,31,37,43,49,55)

If PSCX Subunit type is D3U, See XTSI D3U Registers (D3USSSTATUS—XTSI D3U Software Status Register) for bit layout.

If PSCX Subunit type is SPU, See XTSI SPU Registers (SPSSTATUS—SPU Software Status Register) for bit layout.

If PSCX Client unit type is IBU, See XTSI IBU Registers (IBUSTATUS—IBU Status Register) for bit layout.

PSCX Client (0-5) ESR—(Words 27,33,39,45,51,57)

If D3U Subunit type is D3U, See XTSI D3U Registers (D3UESR—D3U Error Source Register) for bit layout.

If SPU Subunit type is SPU, See XTSI SPU Registers (SPSESR—SPU Error Source Register) for bit layout.

If PSCX Client unit type is IBU, See XTSI IBU Registers (IBUESR—IBU Error Source Register) for bit layout.

PSCX Client (0-5) Control—(Words 28,34,40,46,52,58)

If D3U Subunit type is D3U, See XTSI D3U Registers (D3UCTL—D3U Control Register) for bit layout.

If SPU Subunit type is SPU, See XTSI SPU Registers (SPSCTL—SPU Control Register) for bit layout.

If PSCX Client unit type is IBU, See XTSI IBU Registers (IBUCTL—IBU Control Register) for bit layout.

PSCX Client (0-5) EXR—(Words 29,35,41,47,53,59)

If D3U Subunit type is D3U, See XTSI D3U Registers (D3UEXR—D3U Exercise Register) for bit layout.

If SPU Subunit type is SPU, See XTSI SPU Registers (SPSEXR—SPU Exercise Register) for bit layout.

If PSCX Client unit type is IBU, See XTSI IBU Registers (IBUEXR—IBU Exercise Register) for bit layout.

XTSI PCM Bus Sub-Branch Mismatch Auxiliary Dump

DUMP SIZE	CLIENT_ID	TIME_SLOT	TRANS DATA	QUERY DATA	FAULT_TYPE
PSCX0	PSCX0 USTAT	PSCX0 HWSTAT	PSCX0 ESR	PSCX0 CTL	PSCX0 EXR
PSCX1	PSCX1 USTAT	PSCX1 HWSTAT	PSCX1 ESR	PSCX1 CTL	PSCX1 EXR
PSCX2	PSCX2 USTAT	PSCX2 HWSTAT	PSCX2 ESR	PSCX2 CTL	PSCX2 EXR
PSCX3	PSCX3 USTAT	PSCX3 HWSTAT	PSCX3 ESR	PSCX3 CTL	PSCX3 EXR
PSCX4	PSCX4 USTAT	PSCX4 HWSTAT	PSCX4 ESR	PSCX4 CTL	PSCX4 EXR
PSCX5	PSCX5 USTAT	PSCX5 HWSTAT	PSCX5 ESR	PSCX5 CTL	PSCX5 EXR

DUMP SIZE—Report Type and Block Size

Octal 00006124

Bit 0 = TAG = 0
1-8 = Dump size (42 decimal)
9-12 = Dump type-XTSI PSC data mismatch=0(4)

CLIENT_ID—Word 1

Bit 0-4 = Contains initially suspected client ID (Same as Client ID in TRANS_DATA, but may not be the same unit/subunit implicated by the F-level.) (See Control Bus Memory Layouts)

TIME_SLOT—Word 2

Bit 0-11 = Adjusted time slot count

TRANS_DATA—Translations RAM (Expected Value) for TIME_SLOT

Bit 0-11 = Translation RAM Value
12-13 = PCM Input Bus Sub-Branch (0-2)
14-18 = Client ID (Same as CLIENT_ID Word 1)
(See Control Bus Memory Layout)

QUERY_DATA—Translations Query (Current Value) for TIME_SLOT

Bit 0-11 = Translation RAM Value
12-13 = PCM Input Bus Sub-Branch (0-2)

FAULT_TYPE—for development only

PSCX Client (0-5) Subunit—PSCX Subunit Type Number

Bit 0-8 = Unit member number (UTMEM)
For D3U - Member number is between 0 - 7
For SPU - Member number is between 0 - 11
For IBU - Member number is 0

9-11 = Unit type

0 - D3U
1 - SPU
2 - IBU
3 - Unused PSC Slot

12-23 = Unused

PSCX Client (0-5)—USTAT-PSCX Software Status

(See XTSI PCM Bus Mismatch Auxiliary Dump for bit layout)

PSCX Client (0-5)—HWSTAT-PSCX Hardware Status

(See XTSI PCM Bus Mismatch Auxiliary Dump for bit layout)

PSCX Client (0-5)—ESR-PSCX Error Source Status

(See XTSI PCM Bus Mismatch Auxiliary Dump for bit layout)

PSCX Client (0-5)—CTL-PSCX Control Status

(See XTSI PCM Bus Mismatch Auxiliary Dump for bit layout)

PSCX Client (0-5)—EXR-PSCX Exercise Status

(See XTSI PCM Bus Mismatch Auxiliary Dump for bit layout)

XTSI Non-PSC Auxiliary Data Dump

DUMP_SIZE CLIENT_ID PUFR_INT2 PUFR_INT3 PUFR_INT4 PUFR_INT5

DUMP SIZE—Report Type and Block Size

Octal 00005014

Bit 0 = TAG
1-8 = Output size = 6
9-12 = Report type = 5

CLIENT_ID—Word 1

Bit 0-4 = Contains suspect client ID
(See Control Bus Memory Layouts)

PUFR_INT2 PUFR_INT3 PUFR_INT4 PUFR_INT5—Development Only.

Abbreviations

A

ABC
Auxiliary Buffer Control

ACR
Auxiliary Call Register

ACT
Auxiliary Activity

ACTMB
Active Maintenance Bus

ADT
Automatic Digital Testing

ALEV
A-Level

ALK
A-Link

ANI
Automatic Number Identification

AO
Activate Override

API
Attached Processor Interface

APUB
Autonomous Peripheral Unit Base

APUF
Autonomous Peripheral Unit Failure

APUT
Autonomous Peripheral Unit Trouble

ASG
Assigned

ASW
All Seems Well

ATM
Automatic Trunk Measuring

ATMS
Automatic Transmission Measurement System

ATP
All Test Passed

ATSG
Adjunct Trunk Subgroup

AUB
Auxiliary Unit Bus

AUI
Auxiliary Unit Interface

AUTO
Autonomous

AUX
Auxiliary

B

B/I
Busy/Idle

BC
Buffer Controller

BF
Buffer Fabric

BLEV
B-Level

BLK
B-Link

BLM
Base Level Maintenance

BMB
Buffer Memory B

BMC
Buffer Memory C

BTFN
Base Traffic Number

BTR
Bus Terminating Resistor

BWM
Broadcast Warning Message

C

CAMA
Central Automatic Message Accounting

CAMA
Centralized Automatic Message Accounting

CB
Control Bus

CC
Central Control

CC
Control Console

CCFR
Central Control Fault Recognition

CCIS
Common Channeling Interoffice Signaling

CCITT
International Telegraph and Telephone Consultative Committee

CCWS
CAMA Call Waiting/Suspension

CFG
Configuration

CIN
Circuit Identification Number

CINVPAR
Invert ROM Control Parity

CIP
Call in Progress

CKEY
Centralized Automatic Message Accounting Keying

CLIDS
Controller or Client D Source

CLKACT
Clock Activity

CLN
Code Line Test Circuit

CLRCKER
Clear Clock Error

CMD
Command

CMS
Circuit Maintenance System

CNI
Common Network Interface

CNTL
Control

CONFIG
Configuration

CPA
Common Platform Adjunct

CPBS
Control Parity B Source

CPS
Control Point Switch

CR
Call Register

CS
Call Store

CSACT
Call Store Activity

CSB
Call Store Bus

CSPGM
Call Store Program

CSR
Channel Status Register

CTLK
CAMA Talking

D

DB
Database

DBT
Diagnostic Buffer Table

DCON
Diagnostic Control

DDI
Direct Data Insert

DFA
Digital Facility Access

DFR
Deferred Fault Recovery

DGN
Diagnostic

DIF
Digital Interface Frame

DIF-E1
Digital Interface Frame-Export 1

DIOP
Disk Independent Operation

DIU
Digital Interface Unit

DKAD
Disk Administration

DMA
Direct Memory Access

DPF
Data Parity Failure

DSS
Diagnostic Sequence State

DT
Digroup Terminal

DT
Digital Trunk

DTCR
Dedicated TSI Connection Register

DTMF
Dual Tone Multifrequency

DUB
Data Unit Bus

DUS
Data Unit Selector

E

EAI
Emergency Action Interface

EBL
Extended Bus and LAN

ECD
Equipment Configuration Data

ECOS
End-to-End Class of Service

EPIC
Enhanced Peripheral Interface Controller

ERSP
Error Stop

ESR
Error Summary

EST
Echo Suppressor Terminal

ESU
Echo Suppressor Unit

F

FBI
Favric Bus Interface

FLEV
F-Level

FR
Fault Recovery

FUNC
Function

G

GCP
General Control Pulse

GETS
Government Emergency Telecommunication Service

GI
Group Interrogate

GULP
Generic Utility Program

I

I/O
Input/Output

ID
Identification

IDTS
Immediate Dial Tone Start

IFACT
Interface Bus Activity

IFB
Interface Bus

IFBSY
Interface Busy

INIT
Initialization

INT
Intermediate

INUP
International Integrated Services

IOCH
Input/Output Clock High

IOCL
Input/Output Clock Low

IOUC
I/O Unit Controller

IOUS
Input/Output Unit Selector

IPD
Interprocessor Data

IPI
Initial Pulsing Interval

IPUB
Interface to Peripheral Unit Bus at Frame

IRN
Integrated Ring Node

ISS
Interrupt Sequence State

ISUP
Integrated Services Digital Network User Part

ITUP
International Telephone User Part

L

LACID
Link Access Identification

LCS
Lower Call Store

LSTR
Link Security Terminal Register

M

MA
Maintenance

MAC
Maintenance Control

MACP
Maintenance Administration Control Program

MB
Maintenance Busy

MC
Major Category

MCC
Master Control Console

MCD
MCC Direct Data Insert Register

MEMN
Member Number

MF
Multifrequency

MFR
Multifrequency Receiver

MFRT
Multifrequency Receiver Test Circuit

MFX
Multifrequency Transmitter

MFXT
Multifrequency Transmitter Test Circuit

MI
Maintenance Interject

MI
Member Interrogate

MIN
Minimum

MIRA
Manual Input Request Administration

MIS
Miscellaneous

MMIO
Memory Mapped Input/Output

MRA
Modified Recovery Action

MS
Microstore

MSG
Message

MSL
Master Select Level

MSN
Miscellaneous Scanner Number

MSP
Multifaceted Signal Processor

MUP
Master Control Complex Utility Processor

N

NAIA
Node Attempted Illegal Access

NC
Network Clock

NCAT
Non-Call Associated Trunks

NCLK
Network Clock

NCSU
Network Clock Sync Unit

NESAC
National Electronic System Assistance Center

NLK
Not Linked

NM
Network Management

NORM
Normal

NSN
Network Switching Number

NWM
Network Management

O

OBS0
Service Observing Circuit 0

ODA
Office Data Assembler

OMR
Output Message Record

OOS
Out-of-Service

OSC
Oscillator

P

PC
Processor Configuration

PC
Peripheral Controller

PCP
Positive Call Process

PCRV
Processor Configuration Recovery

PDF
Power Distribution Frame

PEST
Prevent Error Source Transmission

PH
Phases

PLSRPLY
Pulse Reply

PMOS
Peripheral Maintenance Operating System

PMOS
Peripheral Maintenance Operating System Messages

PPS
Peripheral Pulse Error

PRM
Processor Recovery Message

PS
Program Store

PSB
Program Store Bus

PSBX
Protected, Backed Executed Text

PU
Program Unit

PU
Peripheral Unit

PUB
Peripheral Unit Bus

PUBB
Peripheral Unit Bus Branching

PUC
Peripheral Unit Control

PUCB
Peripheral Unit Control Bus

PUEA
Peripheral Unit Enable Address

PURB
Peripheral Unit Reply Bus

PUWB
Peripheral Unit Write Bus

PW
Pulse Width

PWRMON
Power Monitor

R

RA
Recorded Announcement

RAM
Random Access Memory

RCDM
Recent Change Data

RCV
Receive

REG
Register

RINGMON
Ring Monitor Kernel Process

RMS-D2
Remote Measurement System-Digital 2

RO
Receive On

ROP
Read-Only Printer

ROS
Request Out-of-Service

ROTL
Remote Office Test Line

RPI
Routing Pattern Index

RS
Receive Synchronizer

RST
Restore

RSW
Receiver Seems Well

RTNR
Real Time Network Routing

RTP
Ring and Tone Plant

RTSI
Receive Time-Slot Interchange

S

SAST
System Audit of Stores Using Tape

SC
Subcategory

SCAR
Stable Call Accumulation Register

SCLK
System Clock

SCP
Software Change Package

SCS
Service Circuit System

SD
Signal Distributor

SIMR
System Integrity Monitor Register

SP
Signal Processor

SPC
Switching and Permuting Circuit

SPUIE
Signal Processor Unit Interface Error

SR
System Recovery

SR
System Reinitialization

SRAM
Static Random Access Memory

SSD
Scan and Signal Distributor

SSD
Second Start Dial

ST
Sequence Table

STBY
Standby

SU-STAT
Subunit Status

T

TAN
Trunk Appearance Number

TAR
Transition Address Register

TAS
Tone and Announcement Circuits

TAT
Test Access Trunk

TBMN
Trunk Block and Member Number

TBMN
Trunk Block and Memory Number

TBN
Trunk Block Number

TC
Transport Capabilities

TC
Trace and Control

TDN
Time Division Number

TDN
Trunk Distributor Number

TERM
Terminal

TF
Tape Frame

TGR
Terminal Grouping Frame

TLP
Trouble Locating Procedure

TMR
Trunk Maintenance Register

TMS
Time Multiplex Switch

TMSP
Time Multiplex Switch Port

TMTC
Trunk Maintenance

TN
Trunk Number

TND
Tone Detector Test

TOSL
Trunk Out-of-Service List

TPM
Traffic Plant Measurement

TR
Trunk Register

TRA
Terminal Resource Allocator

TRAM
Table RAM

TRC
Twisted Ring Cable

TRPF
Transit Parity Failure

TS
Time Slot

TSF
Total Signaling Failure

TSG
Trunk Subgroup

TSGHC
Trunk Subgroup Head Cell

TSI
Time Slot Interchange

TSN
Trunk Scanner Number

TSTRSL
Test Result

TSW
Transmitter Seems Well

TTSI
Transmit Time Slot Interchange

TUC
Tape Unit Controller

U

UCS
Upper Call Store

UHARD-STAT
Unit Hardware Status

UID
Unit Identification

UPD
Update

USOFT-STAT
Unit Software Status

UTE
Unitized Terminal Equipment

V

VBB
Vector Base Bit

VIF
Voiceband Interface Frame

VIU
Voiceband Interface Unit

VP
Voice Processor

VPIC
Voice Processor Interface Controller

W

WOPS
Without Protection Switch

X

XCVR
Transceiver

XCVT
Transceiver Test Circuit

XPWR
Miscellaneous Power

XTSI
Expanded Time-Slot Interchange

Index

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