

**5ESS[®]-2000 Switch
Maintenance Reference Handbook
5E10 and Later Software Releases**

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Acknowledgment

Developed by Lucent Technologies Customer Training and Information Products.

1. INTRODUCTION

1.1 PURPOSE

This handbook is a convenient reference for maintaining the 5ESS[®]-2000 switch for software releases 5E10 and later. It contains commonly used information to help respond to reported faults and abnormal operating conditions.

The handbook is not a troubleshooting guide. Nor is it, because of its limited content, a substitute for detailed system documentation. It is a memory jogger and a reference guide to appropriate instruction materials.

1.2 UPDATE INFORMATION

In accordance with the 5ESS[®]-2000 Switch Software Support Plan, the 5E10 software release will be rated Discontinued Availability (DA) on December 4, 1998. The information supporting 5E10 is being removed from this information product (IP). The actual removal of the information will occur over time instead of concurrently.

This IP is being reissued to cover the 5E13 software release, any software update information, and editorial changes. Changes relating to the 5E13 software release are in the following:

- Chapter 1
- Chapter 5.3
- Index.

1.3 RESTRICTION

The use of this handbook should be restricted to persons familiar with 5ESS[®]-2000 switch operations and maintenance. Its use by inexperienced personnel could result in damage to system integrity.

Potential users should do the following:

- Be familiar with telephone equipment and terminology
- Have completed switch maintenance training on the 5ESS[®]-2000 switch
- Be familiar with the information in 235-900-10X, *Product Specifications*.

1.4 ORGANIZATION

The manual contains Sections 1 through 6, glossary, and index. A table of contents at the front of the manual gives a condensed view of the major subjects covered in each section.

Each section has a table of contents with a more comprehensive view of the subjects covered in that particular section. Figures and tables appear within the text of the section as close as possible to their respective references.

The material presented in this manual includes the name of the appropriate manual where in-depth, trouble-clearing procedures can be located, how to clear alarms and how circuit packs are coded. There is a section on power distribution and a glossary that contains 5ESS[®]-2000 switch specific terms including those for the features in 5E13 software release.

The major section in this manual, Section 5.3, addresses the functional modules of the 5ESS[®]-2000 switch. Subsections contain the equipment bay and shelf layouts for the Administrative Module, Communication Module,

Switching Module, the Common Network Interface and their associated peripheral units. The illustrations show shelf layout, EQL numbers, pack codes and backplane information for some of the shelves.

The maintenance-related functions are found in the diagnostic phase description tables at the end of each functional module's subsection.

The last section of the manual is a subject index.

1.5 USER FEEDBACK

The producers of this manual are constantly striving to improve quality and usability. Please use the enclosed user feedback form for your comments and to advise us of any errors. If the form is missing or your comments do not fit, you can write to the following address:

Lucent Technologies
Quality Department
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Winston-Salem, NC 27106

Please include the issue number and/or date of the manual, your complete mailing address and telephone number. We try to answer all correspondence within 30 days.

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technical assistance center where problems are dispatched immediately to your local RTAC. All other problems are referred to your local RTAC on the next regular business day.

2. MAINTENANCE SUPPORT DOCUMENTATION

2.1 GENERAL

Familiarity with the contents of 235-001-001, *Documentation Description and Ordering Guide*, can be helpful to anyone involved in 5ESS[®]-2000 switch operations. Specifically, be familiar with documents considered "system interactive" within the structure of the guide, especially those designed for maintenance functions. See Table 2-1 for a list of support documents interaction.

2.2 SYSTEM INTERACTIVE DOCUMENTS

The following is a list of reference documents for personnel in maintenance operations. A brief description of each document is given.

- 235-105-110, *System Maintenance Requirements and Tools*: This document describes maintenance concepts and built-in maintenance capabilities of the switch. It contains sections covering maintenance philosophy, maintenance tools and Master Control Center (MCC) display pages.
- 235-105-210, *Routine Operations and Maintenance Procedures*: This document contains the descriptive material and detailed procedures for routine operations and maintenance of the 5ESS[®]-2000 switch.
- 235-105-220, *Corrective Maintenance Procedures*: This document contains hardware-maintenance procedures, office dependent data maintenance procedures, supporting list of diagnostic phase descriptions and an appendixes group of job aids.
- 235-105-250, *System Recovery Procedures*: This document contains descriptive material and detailed procedures for hardware and software recovery.
- 235-105-119, *Maintenance Guide Utilizing OMS5*: This document contains information related to the use of the OMS5 program for office performance summaries.
- 235-600-115, *Input Reference Guide*: This document, is a "mind jogger," a summary of MCC index display pages, function keys, system responses and input message formats.

2.3 ASSOCIATED DOCUMENTS

Refer to the following list for documents that address maintenance procedures and associated information.

- 235-600-700, *Input Messages Manual*
- 235-600-750, *Output Messages Manual*
- 235-600-10X, *Translation Data*

NOTE: X denotes the variable that reflects the respective software release.

- 235-600-400, *Audits Manual and Appendix*
- 235-600-500, *Asserts Manual and Appendix*.

NOTE: For the number of a software release specific document, refer to 235-000-000, *Numerical Index*.

Table 2-1 Support Document Interaction

Document Number	Document Title	Document Description
235-001-001	<i>Documentation Description and Ordering Guide</i>	List of 5ESS®-2000 switch documents with brief descriptions.
235-000-000	<i>Numerical Index</i>	Menu of documents available as of index date.
SYSTEM INTERACTION DOCUMENTS		
235-105-110	<i>System Maintenance Requirements and Tools</i>	<ul style="list-style-type: none"> • Maintenance Philosophy • Maintenance Tools • MCC Display Pages
235-105-210	<i>Routine Operations and Maintenance Procedures</i>	<ul style="list-style-type: none"> • Equipment Test List • Memory Alteration Description and Procedures • Abnormal Input Message Acknowledgment Procedures • Office Alarm Test Procedures • Call Trace Procedures • Miscellaneous Routine Procedures • Appendix - O&M Checklist
235-105-220	<i>Corrective Maintenance Procedures</i>	<ul style="list-style-type: none"> • Hardware Maintenance Procedures • Office Dependent Data Maintenance Procedures • Diagnostic Phase Descriptions • Job Aid ^a
235-600-115	<i>Input Reference Guide</i>	Summary of MCC index display pages, function keys system responses and construction of input message formats.
BE FAMILIAR WITH DOCUMENTS		
235-100-125	<i>System Description</i>	b
235-105-119	<i>Maintenance Guide Utilizing OMS5</i>	b
235-105-200	<i>Precutover and Cutover Procedures</i>	b
235-105-250	<i>System Recovery</i>	b
235-190-101	<i>Business and Residence Modular Features</i>	b
235-080-100	<i>TG-5 Translations Guide</i>	b
Notes:		
a. For the number of a software release specific document, refer to 235-000-000, <i>Numerical Index</i> .		
b. See document overview for the document description.		

2.4 DOCUMENTS REFERENCED FROM MAINTENANCE PROCEDURES

Table 2-2 is an index of document numbers and sections that address specific maintenance procedures.

The listed procedures appear in subject groups in alphabetical order.

Because all referenced documents are in the 235-105 series, only the last three digits of the official number appear in the column headed DOCUMENT.

System Initialization/Reinitialization Procedures are not in this table. Refer to 235-105-250 for those procedures.

Table 2-2 Documents Referenced From Maintenance Procedures

PROCEDURE	DOCUMENT
AC	
Check and Adjust AC Amplifiers in Test Access Unit	220
ACKNOWLEDGMENTS	
Resolve Abnormal Input Message Acknowledgments	210
Resolve Abnormal Recent Change Acknowledgments	210
Resolve Abnormal Trunk Line Work Station (TLWS)	210
ACTIVATE	
Execute the Activate Form	210
AIR FILTERS	
Replace Fan Unit Air Filters	210
ALARMS	
Access Alarm Display Pages at MCC Video Terminal	220
Office Test Critical Alarm	210
Office Test Major Alarm	210
Office Test Major Misc. Alarm	210
Office Test Minor Alarm	210
Office Test Minor Misc. Alarm	210
Remove and Replace Fan Unit Alarm Board	220
Respond to Switch Alarms	220
Respond To and Resolve Alarm Associated with an ESM Fault	220
Respond To and Resolve DAYLOG Message Lost Alarm	220
Respond To and Resolve RC/V Log Warning Alarm	220
Test Office Alarms — RSM	210
Test RSM Office Alarms	210
Verify Status of Office Critical Alarm Circuits	220
Verify Status of Office Exit Pilot Alarm Circuits	220
Verify Status of Office Major Alarm Circuits	220
Verify Status of Office Major Misc. Alarm Circuits	220
Verify Status of Office Minor Alarm Circuits	210
Verify Status of Office Minor Misc. Alarm Circuits	220
A-LINK	
Clear In Line Unit A-Link Failure	220
AUTOMATIC MESSAGE ACCOUNTING (AMA)	
Allow an AMA Session	210
Analyze and Resolve Assert Error Report	220
Analyze and Resolve Audit Error Report	220
Bring Up AMATPS	210
Change AMAOPTION Attribute	210
Check Hardware Config. AMATPS	210
Clear AMA Configuration Information	210
Equip AMA Disk Partitions	210
Initialize AMA System Process (AMCP)	210
Initialize User Level Automatic Restart Process	210
Manually Test 48FRI Backup Unit	210
Mount and Verify AMA Tape	210
Procedure for AMA Teleprocessing Emergency Tape Writing	210
Remove AMA Tape	210
Review AMAOPTION Attribute	210
Set AMA Stream Value	210
Set Option Attribute for AMA	210
Set Option Attribute for AMATPS	210
Set up AMA Control File	210
Write AMA Data from Disk to Tape	210
B-LINK	
Clear B-Link or LUCHAN Failure in Line Unit	220
CALL PROCESSING	
Analyze and Clear Per-Call-Test Failure	220
Perform Ringer Count Check, On an On-Hook Analog Line — Using DCTU	220

CALL TRACE	
Analyze Hardware Summary Output Messages	220
Analyze Software Data Output Messages	220
Call Trace Procedures	220
Determine Hardware and Software Used During Call Processing	220
Obtain Most Recent Software Call Trace Data	220
Perform In-Process Call Trace	220
Perform Nuisance (Terminating Tandem/Interoffice) Call Trace	220
CARRIER CHANNELS	
Identify SLC [®] Carrier Channels	210
Install Channel Units in RT and Update Recent Change Form	220
Provision SLC [®] 5 Carrier Channel Units	210
CIRCUIT PACKS	
Perform Sequential Removal and Insertion Circuit Packs - LU	220
COIN PHONE	
To Determine Line State Near-to-Far-End Check of Analog Coin Phone Line	220
COMMUNICATION MODULE (CM)	
Perform CM2 Fuse Alarm Tests	210
Test CM2 Fan Units	210
COMMUNICATION MODULE PROCESSOR (CMP)	
NOTE: These procedures contain references to CMP.	
Analyze and Clear Nondiagnosable CMP Memory Errors	220
Backup Memory (in-core)	210
Clear Diagnostic Failure in Hardware of Switch	220
Obtain ODD Backup Schedule	210
Perform CM2 Fuse Alarm Test	210
Perform Power-Up/Power-Down of Equipment	220
Respond to a Fuse Alarm, Power Alarm Failure	220
Respond to and Resolve an RC/V Log Warning Alarm	220
Diagnostic Phase Descriptions	220
CENTRALIZED TRUNK TEST UNIT (CTTU)	
Attributes Necessary to Add CTTU Interface	210
Bring Up CTTU	210
Define Logical Test Port Group	210
Enable CTTU to Be a Recipient of 101 Test Line	210
CONTROL UNIT (CU)	
Analyze and Clear Nondiagnosable CU Memory Errors	220
DATA BASE	
Change Update Data Base Using Lucent 3B Computer Recent Change	210
Update Backup Data Bases	210
DATA LINK	
Start Reader and Writer Processes Data Link	210
DATA SET1	
Check Special Cable Between Data Set and TN75C Data Set	210
Set DIP Switches Data Set 212	210
Set Options 2024, 2048, and 2096 Series Data Set	210
Set/Verify Data Set Options After IMLT Growth	210
DIAGNOSTIC	
Clear Diagnostic Failure in Hardware (Units/Circuits) of Switch	220
DIGITAL	
Basic Rate Interface (BRI) Access to the 108 Test Line	220
Evaluate Digital Subscriber Line Automatic Line Using ALE	220
Monitor Digital Subscriber Line Protocol	220
Perform Loopback Test on a Digital Line	210
Test Digital Subscriber Line BRI Integrity Using BRI Dial-Up Test	220
Test Digital Subscriber Line Basic Rate Interface (BRI) Dial-Up	220
Verify Digital Equipment Number of a Digital Trunk	220
DIRECTLY CONNECTED TEST UNIT (DCTU)	
Assign Route Index to DCTU LTP	210
Define Logical Test Port Group Member for DCTU	210
Define Logical Test Port Trunk Group for DCTU	210
Grow DCTU Port TG, TG Member, and RI Before IMLT2 Growth	210
Perform Distance-to-Open Measurement on a Line Using DCTU	220
Perform Ringer Count Check On an On-Hook POTS Line Using DCTU	220
Power-Up and Restore to Service Update DFC, DCTURTI on SM	210
DISK	
Connect Off-Line Spare in Running System Disk	210
Convert Warm Disk Spare to Off-Line Spare Disk Config. Disk	210
Replace System Disk (0 or 1) With Simplex Disk (14 or 15)	210
DISK FILE CONTROLLER (DFC)	

Remove DFC From Service	210
ENGINEERING AND ADMINISTRATIVE DATA ACQUISITION SYSTEM (EADAS)	
Bring Up EADAS	210
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Analyze and Clear Per-Call-Test Failure	220
FAULT	
Determine Fault Locating in the AM, CM, or SM Equipment	220
FIXED ROUTE	
Define Treatment and Route Index for Fixed Route	210
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Replace Blown Fuse, Filter at PDF	220
Replace Fuses, Load and Indicator at PDF	220
GROWTH/DEGROWTH TESTING	
Grow ISLC Channel Test After IMLT2 Growth S96CTST	210
INTEGRATED MECHANIZED LOOP TESTING SYSTEM 2 (IMLT 2)	
Grow DCTU Port TG, TG Members, and RI Before IMLT2 Growth	210
LINES	
Analyze and Clear Line Having a Subscribing Customer Complaint	220
Clear LEN Failure in Line Unit Grid	220
Near-to-Far-End Check of Coin Phone Link to Determine Line State	220
Perform Automatic Line Insulation Test (ALIT)	210
Perform Line Maintenance Using the TLWS	220
Perform Line Signaling	220
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Measure/Record Transmission Loss on Optical Link	220
Update Linkages	210
LINE TRUNK PERIPHERAL (LTP)	
Assign Route Index to DCTU LTP	210
Define Trunk Group Member LTP	210
LINE UNIT (LU)	
Clear LU Grid Exercise Test Failure	220
Perform Line Status Check of Busy Line	220
Perform Power-Up of LUs and ISLUs	220
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Perform Metallic Measurements of an Analog Trunk Using DC Jacks	220
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NOTE: Also see Small Computer System Interface (SCSI)	
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Power Down and Remove Cabling from Defective MHD	210
Power Down and Replace Cables MHD-1, MHD-2, and DFC-0	210
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Analyze OP TRC HLSC Output Message Utility Call Trace	220
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Analyze OP TRC NTWK Output Message Utility Call Trace	220
Analyze OP TRC PROC Output Message Utility Call Trace	220
Analyze TRC UTIL Line Output Message Utility Call Trace	220
Analyze TRC UTIL Trunk Output Message Utility Call Trace	220
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Obtain Most Recent Software Call Trace Data Utility Call Trace	220
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Resolve Power Problem at PDF or Power Plant	220
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Bring Up RMAS	210
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Clear External Monitor Unit Trouble	220
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Remove and/or Install Small Computer System Interface (SCSI) Disk Unit Package (DUP)	220
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SOFTWARE CHANGE ADMINISTRATION AND NOTIFICATION SYSTEM (SCANS)	
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Verify SCANS II Dial Up Data Link	210
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Perform Station Ringer Touch-Tone Test for an MLHG	220
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SOFTWARE UPDATE	
Activate Software Update	210
Back Out Software Update	210
Check/Activate Temporary Software Updates	210
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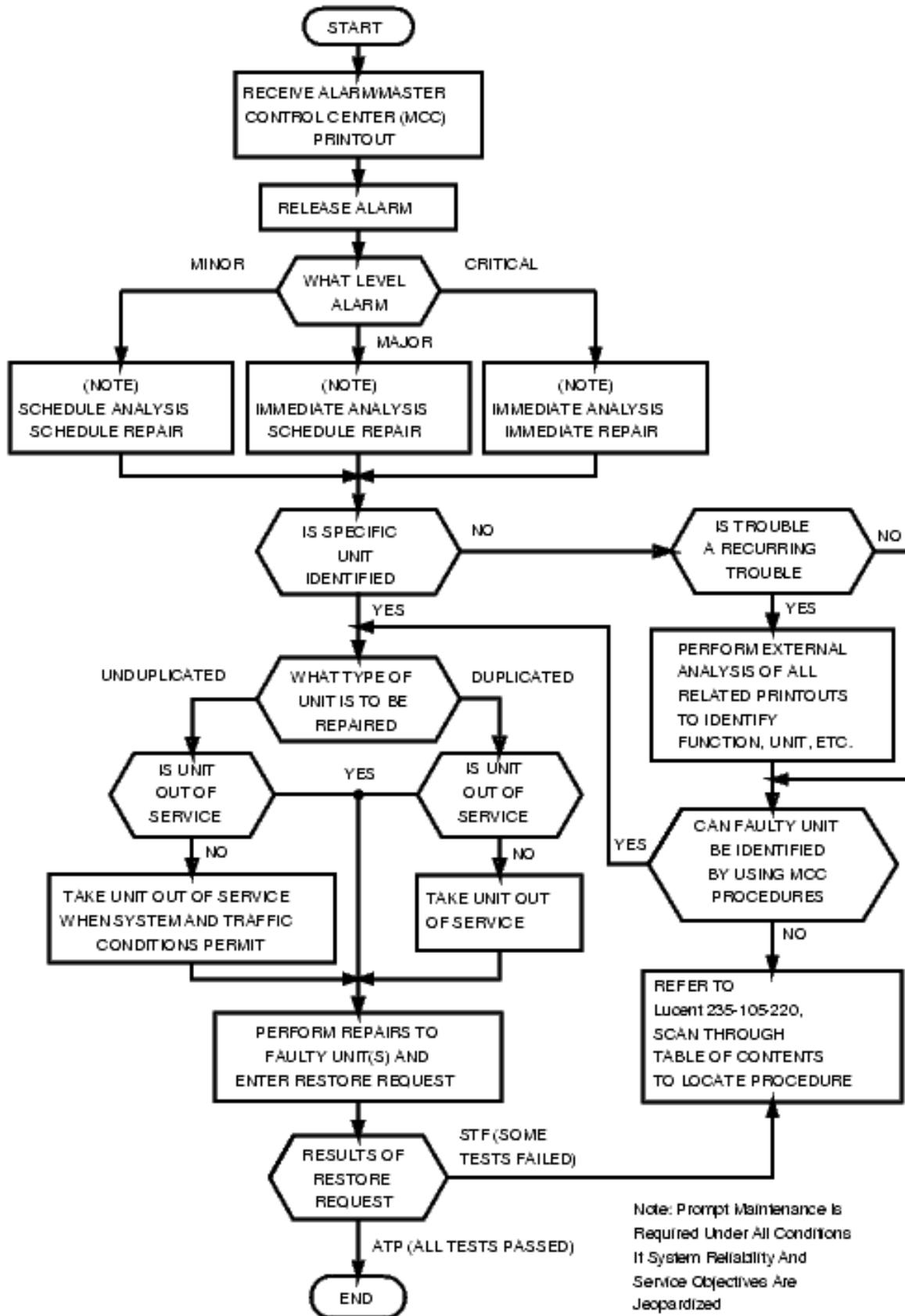
Request Long Summary of Software Updates	210
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Analyze and Clear Nondiagnosable SM Memory Errors	220
Down Load Updates SM Pumpable Peripheral Unit	210
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Perform ODD Memory Growth SM	210
Perform SM Fuse Alarm Tests	210
Pump All Off-Line SMs	210
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Change Status from Grow to OOS SDLC and SDL for CTTU Data Link	210
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Change Status from Unequip to Grow SDLC and SDL for EADAS Data Link	210
Change Status from Unequip to Grow SDLC and SDL for RMAS Data Link	210
Change Status from Unequip to Grow SDLC and SDL for SES II Data Link	210
Diagnose SDLC	210
Restore SDLC to Service	210
SYSTEM INITIALIZATION/REINITIALIZATION	
For any System Initialization Activity, always refer to Lucent 235-105-250.	
Replace System, Disk (0 or 1), With Simplex Disk (14 or 15)	210
S96CTST, Grow ISLC Channel Test After IMLT2 Growth	210
TAPE DRIVE	
Mount Tape on Tape Drive	210
Perform Operational Tests on Tape Drive <i>KEYSTONE</i> [®] III Tape Drive	210
Perform Periodic Test On <i>KEYSTONE</i> [®] III Tape Drive	210
Unmount Tape from Tape Drive	210
TERMINAL	
Select and Prepare Terminal for RC/V Activities	210
TIME MULTIPLEXED SWITCH (TMS)	
Fuse Alarm Tests CM1 TMS	210
Test TMS Fan Units CM1	210
TONE	
Exchange Tone With Distant Office Using Portable Test Equipment	220
TRANSLATION SPLITS	
Analyze and Clear Translation Splits	220
TRUNK AND LINE WORK STATION (TLWS)	
Calibrate TLWS Measurements	220
TRUNKS	
Measure and Record Trunk Transmission Loss Analyze	220
Perform Operational Test Trunk (In-Service)	220
Perform Trunk Maintenance Using the TLWS	220
Test Incoming Trunk, Using 101 Test Line	220
Test Interoffice Trunk using 108-Type Test Line	220
Verify Trunk Equipment Number of an Analog Trunk	220
Verify Trunk Group and Trunk Group Member Number	220
VIDEO TERMINAL	
Respond to and Resolve Locked Up Video Terminal	220

3. MAINTENANCE PROCEDURES SUPPORT INFORMATION

3.1 INTRODUCTION

This section contains information related to operating and maintaining the 5ESS[®]-2000 switch. The basic data are generally referenced to the master control center (MCC) displays and audible notices.

Figure 3-1 is a flowchart that describes a typical procedure for determining maintenance requirements.



Note: Prompt Maintenance is Required Under All Conditions If System Reliability And Service Objectives Are Jeopardized

Figure 3-1 Determining Maintenance Requirements

3.2 AUDIBLE AND VISUAL ALARMS

3.2.1 DISPLAY OF SWITCH STATES

Whenever an alarm condition occurs, an audible/visual alarm is activated to ensure that maintenance personnel are informed even if the MCC terminal is not being monitored. To make it easier for maintenance personnel to quickly locate off-normal conditions on the video displays, various video attributes such as reverse video, flashing, intensity and color (optional) are used in addition to text. The particular combination of these attributes depends on the maintenance "state." Table 3-1 lists the most commonly used MCC states and their video characteristics. For more detailed listings of switch states, refer to 235-105-110, *System Maintenance Requirements and Tools*.

Table 3-1 Display of 5ESS[®]-2000 Switch States Master Control Center Video Terminal

STATE	TEXT DISPLAYED	COLOR TERMINAL	BLACK AND WHITE TERMINAL
Critical Alarm	none	Steady or flashing white on red	Steady or flashing black on white
Deferred	DEFR	Steady yellow on red	Steady black on white
Major Alarm	none	Steady or flashing red on yellow	Steady or flashing black on white
Minor Alarm	none	Steady or flashing black on white	Steady or flashing black on white
Active	ACT	Steady black on green	Steady white on black
Active Forced	ACTF	Steady red on green	Steady white on black
Degrade	DGR	Steady red on green	Steady black on white
Degrade Forced	DGRF	Steady red on green	Steady white on black
Growth	GROW	Steady black on cyan	Steady white on black
Idle	IDLE	Steady black on white	Steady black on white
Inhibit	INH	Steady blue on yellow	Steady black on white
Initialization	INIT	Steady black on yellow	Steady white on black
Limited	LMTD	Steady red on white	Steady white on black
Normal (default)	none	Steady white on black	Steady white on black
Out of Service	OOS	Steady white on red	Steady black on white
Out-of-Service Power	OOSP	Steady white on red	Steady black on white
Out-of-Service Transient	OOST	Steady blue on white	Steady white on black
Out-of-Service Family	OOSF	Steady red on white	Steady white on black
Special Growth	SGRO	Steady black on cyan	Steady white on black
Standby	STBY	Steady black on white	Steady white on black
Test	TEST	Steady blue on white	Steady white on black

Trouble	none	Steady white on red	Steady black on white
Unavailable	UNV	Steady red on yellow	Steady black on white
Unavailable Power	UNVP	Steady red on yellow	Steady black on white
Unavailable Transient	UNVT	Steady blue on yellow	Steady black on white
Unequipped	UNEQ	Steady white on black	Steady white on black
Customer	CDNY ^a	Steady red on yellow	Steady black on white
Camp On	CAMP	Steady red on green	Steady white on black
Notes:			
a. CDNY is displayed after camp-on time-out occurs on ISLU LGC and some LU COMC circuits.			

3.3 SIMULATE OFFICE ALARMS

Table 3-2 lists the procedures used to simulate office alarms.

Table 3-2 Simulate Office Alarms

ALARM	COMMENT ^a
Critical fire	Use local procedures.
Fire alarm trouble	Use local procedures.
High temperature	Apply heat to sensor.
Low temperature	Apply ice to sensor.
Air dryer	Remove fuse of power ON air dryer.
Door intrusion	Open door.
Air conditioner	Remove power at AC disconnect.
Miscellaneous power supplies	Not applicable
Miscellaneous alarm circuit	Not applicable
Discharge fuse fail	On power plant, short pins 8 and 9 on any of the circuit breakers.
Inverter fail	To simulate loss of -48 volts from the inverter, short pins 2 and 3 on TB5 of K1 relay of the inverter.
Inverter transfer alarm	Operate the TEST switch at the front of inverter.
Miscellaneous	Not applicable
Low voltage	With conditions permitting, power down all battery charging rectifiers. Low-volt alarm will activate when plant voltage monitor reads between -48.25 and -51.25 volts.
Rectifier fail	Power any single rectifier down.
Fuse ALM PDF	Insert blown indicator fuse in at least one fuse position of each fuse block.
Alarm battery ALM	Insert blown indicator fuse in Alarm Battery Source.
CO BATT DISCHG	Power all battery charging rectifiers down.
STBY PLANT ALM	See STBY PLANT manual.
High volt	Increase voltage output of one rectifier enough to raise plant voltage monitor to -53.25 volts.
Commercial power failure	Operate TEST switch at front of inverter.
Notes:	
a. Due to possible danger, difficulty, or potential damage to unit when attempting to force a true alarm condition, a short across the scan lead or an open in the scan lead loop should be used to simulate an alarm for alarms where no comment is given. The "TERM" column of the office engineering records indicates whether an alarm is normally opened or closed.	

3.4 ACTIVATION OF OFFICE ALARMS (REMOTE SWITCHING MODULE)

Table 3-3 lists the procedure to follow in testing activation of remote switching module office alarms.

Table 3-3 Activation of Office Alarms Remote Switching Module

ALARM	COMMENT
Critical Fire	See fire alarm manual to activate fire sensing device.
Fire Alarm Trouble	See fire alarm manual.
High Temperature	Apply heat to sensor.
Low Temperature	Apply ice near sensor.
Air Dryer	Remove fuse of power ON air dryer.
Door Intrusion	Open door.
Air Conditioner	Remove power at AC disconnect.
Miscellaneous Power	Remove power source.
Miscellaneous Alarms	a
Discharge Fuse Fail	Short pins 8 and 9 on one of the circuit breakers.
Miscellaneous Power	a
Low Voltage	If conditions permit, power down all battery charging rectifiers. Low voltage alarm will activate when plant voltage is between -48.25 V and -51.25 V. If alarm does not activate when voltage goes below -48.25 V, power up rectifiers and follow procedure. a
Rectifier Fail	Power any single rectifier down.
Fuse ALM PDF	Insert blown indicator fuse in at least one fuse position of each fuse block of each power distribution frame (PDF).
Alarm Battery	Insert blown indicator fuse in Alarm Battery Source.
Battery Discharge	Power all battery charging rectifiers down.
Standby	See STBY (standby) PLANT manual.
High Voltage	If rectifiers have been properly balanced, DO NOT try to simulate a high-voltage alarm by altering rectifier control. If conditions permit, increase voltage output of one rectifier enough to raise plant voltage to -53.25 V. If alarm is not activated, then follow procedure described in footnote.
Commercial Power Failure	a
Notes:	
a. Where possible danger, difficulty, or potential damage to a unit exists when attempting to simulate an alarm condition, locate the scan leads nearest to its sensor and simulate the alarm at that point. Either open the scan lead loop, or short scan leads, as applicable. Unfortunately, this method does NOT verify the actual sensing device; but in many cases, it is the safest method.	

3.5 OPERATIONS AND MAINTENANCE (O&M) CHECKLIST

Table 3-4 lists O&M checks to be performed on the 5ESS[®]-2000 switch.

Table 3-4 5ESS[®]-2000 Switch—O&M Checklist

CHK NO	ITEM(s) FOR CHECK	HOW TO CHECK	HOW TO CLEAR
A. CONTINUOUS CHECKS/MONITORING			
1	Critical or major alarm	Audible and visual alarm present. At top of MCC display, check STATUS area.	If system recovery action is in progress, give it time to complete. If manual intervention is required, use Lucent 235-105-250, <i>System Recovery</i> . If unable to resolve with Lucent 235-105-250, attempt resolution (in priority order) using procedures in Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> . Critical alarms require immediate attention. Problems causing major alarms (for example, MCTSI diagnostic) need craft intervention within an hour or so.
2	Minor alarms	Audible alarm present. At top of MCC	Problems causing minor alarms may be

		display, check STATUS area.	deferred several hours, but should be resolved at least on a daily basis. To resolve use procedures in Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> .
B. DAILY CHECKS (Listed by Priority)			
1	Excessive AM or SM Initializations	Use OMS5 Daily Report or scan ROP printouts for ``INIT AM...'' or ``INIT SM...'' output messages. Also look for ``HWLVL=''. An 8 or above is an SM initialization. This message gives the reason for the initialization. For AM inits: check for any failing/asserting PRMs.	Use Lucent 235-600-750, <i>Output Message Manual</i> , and Lucent 235-600-500, <i>Asserts Manual</i> , to analyze the ``INIT'' and associated messages (for example, ``PMSLOT...'', ``INITIALIZATION TRIGGER...'', ``AUD....''). Determine the cause of the initializations and correct it (if it hasn't already been done). If necessary, seek technical assistance.
2	Excessive Interrupts	Use OMS5 Daily Report or scan ROP printouts for ``REPT...'' output messages. Check for ``INTERRUPT'', ``TRBL'', etc.	Analyze the interrupt reports and try to correlate them to a specific hardware (unit/circuit) and remove it from service (if this hasn't already been done). If the interrupts persist or the suspect unit cannot be repaired in a timely manner, seek technical assistance.
3	Grid fabric failures	Use OMS5 Daily Report or scan ROP printouts for ``TST GRID...STF'' or ``TST GRIDBD...STF'' output messages.	Use Procedure in Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> .
4	Equipment, out-of-service (OOS)	Use OMS5 Daily Report or enter the appropriate input messages and check resulting output message. Examples: OP:cfgstat:OOS, OP:cfgstat:OOS,SM=x, etc.	For each OOS unit or circuit, scan ROP printouts for related DGN output messages. Use Procedure in Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> .
5	Lines, OOS	Use OMS5 Daily Report or enter OP:LIST,LINES;OOS and check resulting output message.	Refer to procedure in Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> .
6	Trunks, OOS	Use OMS5 Daily Report or enter OP:LIST,TRUNKS;OOS and check resulting output message.	Refer to Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> .
7	Excessive MDII reports	Use OMS5 Daily Report, the RC/V view, or scan the ROP printouts for ``REPT:MDII...'' output messages.	Use ROP printouts to identify a specific trunk or TU equipment. For trunk testing, refer to Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> , or MLT facilities (as appropriate).
8	Excessive call failure reports (operational, per-call test, or call cutoff)	Use OMS5 Daily Report or scan the ROP printouts for ``REPT...'' output messages. Look for ``PCTF'', ``SWITCH CUTOFF'' if switch cutoff call facility is turned on.	Use Lucent 235-600-750, <i>Output Message Manual</i> , to correlate the reports for specific circuits to be removed and repaired (if this hasn't already been done). For ``REPT ALINK (or BLINK, LUCHAN, LEN, or PCTF)...'' problems, refer to Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> . For call cutoffs, the input message ``ALW:SCORPT,TRC...'' may be helpful.
9	Data base relation REORG failures	Use OMS5 Daily Report or scan the ROP printouts for ``REORG NEEDED (or CANCELLED)...'' output messages.	Refer to Lucent 235-105-220, <i>Corrective Maintenance Procedures</i> .
10	Excessive DCFs (defensive check failures)	Use OMS5 Daily Report or scan the ROP printouts for ``REPT...DCF...'' output	Use Lucent 235-600-500, <i>Asserts Manual</i> , and Lucent 235-600-750, <i>Output Message</i>

		messages. Or, scan for ``DEF-CHK" or ``RTA DCF".	<i>Manual</i> , to resolve any ``REPT RTA DCFs...". Attempt resolution promptly; DCFs may be serious service effects.
11	Excessive audit reports	Use OMS5 Daily Report or scan the ROP printouts for ``AUD..." output messages.	Use Lucent 235-600-400, <i>Audits Manual</i> .
12	ODD Backup failures	Use OMS5 Daily Report or scan the ROP printouts for ``BKUP ODD, ABORTED" output messages.	Try to do the backup again. Switch the FPC via SW:FPC= and try again; or INH:RC and keep everyone out while performing the BKUP:ODD and try again; or INH:RC get everyone out CLR:TRN (wait for completion) and try again. Note: CLR:TRN will fire any data base audits needed such as OPNDC, TRNDC, and MEMMAN. Also, look for an assert message (in DAYLOG file) associated with the failure using the Lucent 235-600-500, <i>Asserts Manual</i> . Otherwise, seek next higher level of technical assistance.
13	Manual inhibits of automatic checks and functions	Use ``OP:INH" and ``OP:REXINH" input messages and check resulting output messages.	Remove each inhibit using the appropriate ``ALW:..." input message unless there is a valid reason for the inhibit. Unless otherwise directed, there should be no inhibits.
C. SCHEDULED TASKS			
-	All scheduled routine maintenance tasks	Per procedures located in Section 2 — Equipment Test List (ETL), Lucent 235-105-210, <i>Routine Operations and Maintenance Procedures</i> .	Each switch may have variations of the ETL due to specific hardware and software configurations.
Notes:			
a. Use of the OMS5 program on the switching control center system (SCCS) is highly recommended as a time-saver in doing the daily checks identified in 1 through 13 listed as follows. When interpreting the OMS5 Daily Reports, refer to the Lucent 235-105-119, <i>Maintenance Guide Utilizing OMS5</i> , and Lucent 235-600-750, <i>Output Message Manual</i> .			

3.6 EMERGENCY ACTION INTERFACE (EAI) MAINTENANCE COMMANDS

Table 3-5 lists EAI commands and their resulting actions.

Table 3-5 Emergency Action Interface Maintenance Commands

COMMAND	DESCRIPTION
Commands 10 through 15 have a direct and immediate effect on the system. Some commands force the Administration Module (AM) into a particular configuration and some release a forced configuration.	
10	Inhibits automatic processor recovery switch capability. Forces CU0 to be the on-line processor and CU1 to be the off-line processor. May result in recovery action if CU0 was off-line at time of force.
11	Same as 10, except CU1 is forced on-line and CU0 is forced off-line.
12	Same as 10, except the currently active processor is forced on-line and the other is forced off-line.
13	Removes on-line and off-line forces and allows automatic processor recovery action to determine the on-line and off-line CU.
14	Clears all of the following which may be in effect: forces on- or off-line, sets on primary or secondary disk and timer inhibits.
15 a	Initializes all craft interface related processes in the active CU.
Commands 20 through 43 are preparation commands that specify certain conditions prior to a system initialization. These conditions do not take effect until an initialization command is given.	
20	Inhibits automatic processor recovery disk until selection and forces both processors to access their primary disk units on a boot.
21	Removes force on primary disk unit select.
22	Same as 20, except forces the processors to access their secondary disk units.
23	Removes force on secondary unit select.
24	Inhibits the sanity timer from expiring and initiating automatic recovery action.

	Video and to remain displayed until released.
25	Removes the sanity timer inhibit.
26	Releases any trapped failure PRMs (processor recovery messages) and causes the next failure PRM to be displayed in reverse.
27	Releases any trapped failure PRMs and allows further PRMs to be displayed.
28 b	Dumps to the display and printer the contents of the buffer in the active CU containing nonfatal error PRMs generated during the most recent processor recovery.
30 c	Forces the processor to initialize from the backup root file system.
31 c	Allows the processor to initialize from the primary root file system.
32 c	Forces the processor to initialize only the <i>UNIX</i> [®] RTR operating system. The application software is not initialized.
33 c	Allows the processor to initialize both the <i>UNIX</i> [®] RTR operating system and the application software.
34 c	Inhibits hardware checks from initiating automatic recovery action.
35 c	Allows the hardware checks to initiate automatic recovery action.
36 c	Inhibits software checks from initiating automatic recovery action.
37 c	Allows software checks to initiate automatic recovery action.
38 c	Inhibits error interrupts.
39 c	Allows error interrupts.
40 c	Inhibits the use of cache memory.
41 c	Allows the use of cache memory.
42 c	Allows the setting of a parameter which is made available to application software.
43 c	Clears the application parameter.
Commands 50 through 56 are initialization commands. They cause the conditions that were specified previously with commands 20 through 43 to take effect.	
50 d	Signals the application software to initialize.
51 d	Forces initialization of the duplex <i>UNIX</i> [®] RTR (level 1 initialization).
52 d	Forces bootstrap and reloads the <i>UNIX</i> [®] RTR operating system from disk (level 2 initialization).
53 d	Same as 52, plus, reloads Equipment Configuration Data (level 3 initialization).
54 d	Same as 53, plus, clearing of the memory (level 4 initialization).
55 d e	Loads selected disk from tape unit 0.
56 d e	Loads selected disk from tape unit 1.
Notes:	
a. Command 15 is not operational during DIOP regardless of OK or NG system response.	
b. Command 28 is not supported in the current <i>UNIX</i> [®] RTR operating system software release	
c. Commands 30 through 43 generate the next state of the MTTY (maintenance teletypewriter) peripheral control information which is sent to the processor the next time commands 50 through 56 are executed.	
d. Commands 50 through 56, in addition to the description given, cause the current next state information to be sent to the processor.	
e. Commands 55 and 56 require a CU to be forced on-line (Commands 10, 11, or 12) and a disk unit to be selected (Commands 20 or 22).	

3.7 TYPICAL SCAN POINT ASSIGNMENTS - OFFICE ALARMS (REMOTE SWITCHING MODULES)

Tables 3-6 and 3-7 show a typical scan point assignment scheme for office input/output alarms in a remote switching module, respectively.

Table 3-6 Typical Scan Point Assignments, Office Alarms - Remote Switching Module (Alarm Input Option)

SCAN POINT	UNIT/FRAME/CONDITION	ALARM LEAD
SC00	Fire Alarm ^a	Critical

SC01	Fire Alarm Trouble ^a	Major
SC02	High Temperature ^b	Major
SC03	Low Temperature ^b	Major
SC04	Air Dryer Trouble ^b	Major
SC05	Air Conditioner ^b	Major
SC06	Low Voltage ^b	Major
SC07	Low Humidity ^b	Major
SC08	High Humidity ^b	Major
SC09	Door Alarm ^b	Minor
SC10	Window Alarm ^b	Minor
SC11	Carrier Alarm ^b	Minor
SC12	^c	
SC31		
SC32	Discharge Fuse Alarm ^a	Major
SC33	Inverter Failure Alarm ^a	Major
SC34	Miscellaneous Power Failure Alarm ^a	Major ^d
SC35	Miscellaneous Power Failure Alarm ^a	Major ^d
SC36	Miscellaneous Power Failure Alarm ^a	Minor ^d
SC37	Rectifier Failure Alarm ^a	Major
SC38	Alarm Battery Failure Alarm ^a	Major
SC39	CO Battery Discharge Alarm ^a	Major
SC40	High-Voltage Alarm ^a	Major
SC41	Commercial Power Failure Alarm ^a	Major
SC42	Standby Plant Low-Fuel Alarm ^a	Minor
SC43	Standby Plant Operating Alarm ^a	Major
SC44	Standby Plant Rectifier Failure Alarm ^a	Minor
SC45	Standby Plant Failure Alarm ^a	Major
SC46	Miscellaneous Cabinet Fuse Alarm 0 ^a	Major
SC47	Miscellaneous Cabinet Fuse Alarm 1 ^a	Major
SC48	PDF-0 Fuse Failure Alarm ^a	Major
SC49	PDF-1 Fuse Failure Alarm 1 ^a	Major
Notes:		
a. Mandatory assignment.		
b. Typical assignment: actual assignment determined by operating telephone company (OTC).		
c. Assignment determined by OTC.		
d. Status can be MINOR, MAJOR, or CRITICAL. Operating Company makes decision. Default is MINOR.		

Table 3-7 Typical Scan Point Assignments, Office Alarms - Remote Switching Module (Alarm Output Option)

SC/SD	UNIT/FRAME/CONDITION	ALARM LEAD
SC50	ASC/RAU Alarm Active	Info ^a
SC51	ASC/RAU Alarm Test Switch	Info ^a
SC52	ASC/RAU Power Fail	Info ^a
SC53	ASC/RAU Alarm RET Switch	Info ^a
SC54	ASC Alarm Manual Mode Switch	Info ^a
SD100	ASC CTR/RAU Sanity	Info ^a
SD101	ASC SMTBL/RAU EON	Info ^a
SD102	ASC/RAU Building Power	Info ^a
SD103	ASC/RAU Test In Progress	Info ^a

SD104	ASC/RAU Critical Lamp	Info a
SD105	ASC/RAU Standard Alarm Lamp	Info a
SD106	ASC/RAU Major Lamp	Info a
SD107	ASC/RAU Minor Lamp	Info a
SD108	ASC OSMAB/RAU ATST	Info a
SD109	ASC Manual Mode Lamp	Info a
SD110	ASC Critical Audible	Info a
SD111	ASC Major Audible	Info a
SD112	ASC Minor Audible	Info a
SD113	ASC Cycle Timer Inhibit	Info a
Notes:		
a. These default values cannot be changed.		

4. EQUIPMENT

4.1 INTRODUCTION

This section contains information on the physical equipment that makes up the 5ESS[®]-2000 switch. It has location and identification information that is helpful for switch maintenance.

4.2 EQUIPMENT LOCATIONS

A standard method of locating equipment is to identify an office floor, an aisle on the floor, a frame in the aisle, a bay in the frame, equipment shelves in the bay and circuit packs in the shelves. Further, circuit pack connectors and their respective pin assignments are standard reference points for maintenance procedures.

NOTE: When used in diagnostic reports to designate equipment locations, the term **frame** refers to a specific bay (cabinet) lineup; do not confuse this with the support structure (frame) of a bay.

An aisle is a series of frames arranged for maintenance access at both the front and rear of each unit.

A frame is one or more bays of equipment, usually identified functionally, such as Switching Module 1 (SM1).

Bays in a frame are identified by number, beginning with 0.

The locations of shelves, circuit packs and backplane pins within a bay are defined using a coordinate numbering system to establish an equipment location (EQL) number. A complete EQL number consists of nine digits (**xxx-yyy-zzz**), which may be used to locate components or connector pins. Sometimes, a building and floor number is in the master control center (MCC) printout.

A typical EQL number is illustrated and defined in Figure 4-1 .

Less than the full 9-digit EQL number may be referenced depending on the level at which the EQL is being used. For example, yy-zz may be used as the EQL for a backplane connector pin; designating the horizontal row number and the pin number.

4.2.1 CABINET (BAY) LOCATION

The **first digit (x)** of the EQL is the bay number in the frame. In single-bay frames, the bay number is ``0." In multiple-bay frames, the bay numbers start with ``0" and number consecutively to the right when the frame is viewed from the front.

NOTE: CM2 can have two-digit bay numbers. The bay number may be omitted for some cabinets (that is, ring node).

4.2.2 SHELF ASSEMBLY LOCATION

The **second and third digits (xx)** of an EQL indicate the shelf assembly. The digits represent the vertical distance that the shelf is located from the base of the frame. Vertical increments (of four inches) are stamped on the front and rear of the frame uprights. The markings start at the base and range from ``00 to 72."

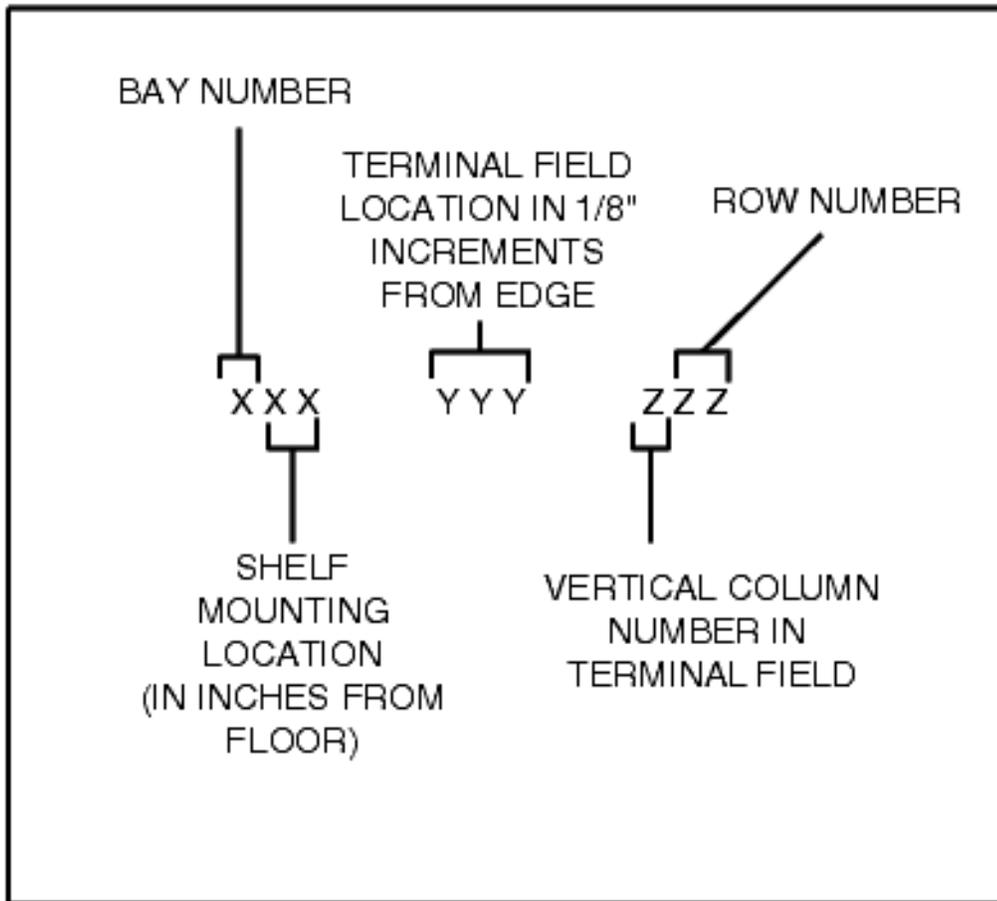


Figure 4-1 EQL Number Defined

4.2.3 CIRCUIT PACK LOCATION

The **second group of three digits (yy)** specifies the horizontal location of a circuit pack in a shelf assembly. Horizontal locations are stamped on the designation strips above the circuit pack apertures. The stamping begins at the front left of the shelf and range from 006 to 184.

EQLs identifying circuit pack locations in integrated services line unit (ISLU) drawer units require a third dimension number. The third number represents the location of the circuit pack in the "pull-out" shelf unit. For example, the EQL 49-006-110 identifies the KCD3 line group controller located at shelf number 49, drawer unit at horizontal aperture number 006 and drawer unit circuit pack 110. The third number group appears in the fault reporting MCC printout when ISLU faults are addressed.

Horizontal increment numbers are stamped along the bottom of the backplane. When viewed from the back (wiring side) of the backplane, the horizontal increments are counted from right to left beginning at the bottom right.

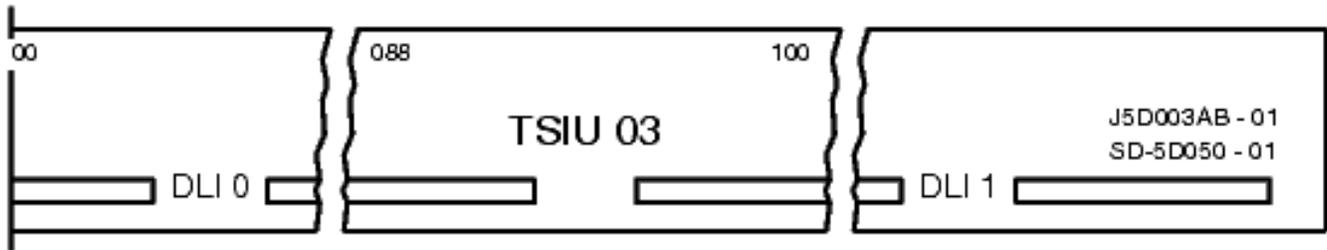
There is a hinged "flip-up" label strip mounted above each shelf unit in a bay. On its front, the strip has a self-adhesive label mounted which contains information about the contents of the shelf unit, such as unit names and service group designations. On its back, the strip also has a label which identifies the unit vertical level, circuit pack locations and pack identity information. Figure 4-2 illustrates the front and back labels and defines the information. Some of the information is required and some is optional. It is recommended that enough information be present to make the use of the strip worthwhile.

4.2.4 PIN LOCATION

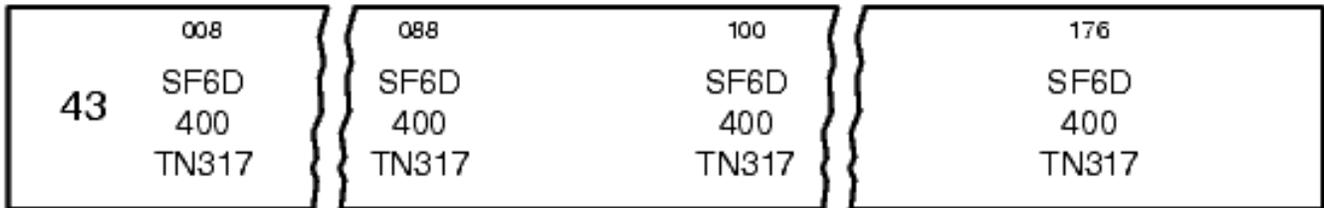
The last three EQL digits (**zzz**) specify the pin number on a printed wiring board and they correspond with the same pin code on the backplane. Each pin field is made up of single-digit column numbers (**z**) (0 to 7), read horizontally and 2-digit row numbers (**zz**) (00 to 56), read vertically. Rows are numbered 00 to 24 upward to the horizontal center line of the shelf and 32 to 56 upward from the horizontal center line. Row numbers 25 through 31 are not generally used as backplane pin locations. They appear in the spaces normally used as "key zones." Figure 4-3 illustrates the pin layout and the means of location.

When viewed from the rear of the backplane, the digits are numbered from right to left beginning with "0." These locations are numbered for both equipped and unequipped pin positions.

When circuit pack connectors contain fewer than the maximum number of pins, pin rows are numbered according to the pin location in the full connector. This numbering convention ensures that the backplane pin numbers and the connector pin numbers agree.



FRONT OF LABEL



BACK OF LABEL

Figure 4-2 Equipment Label

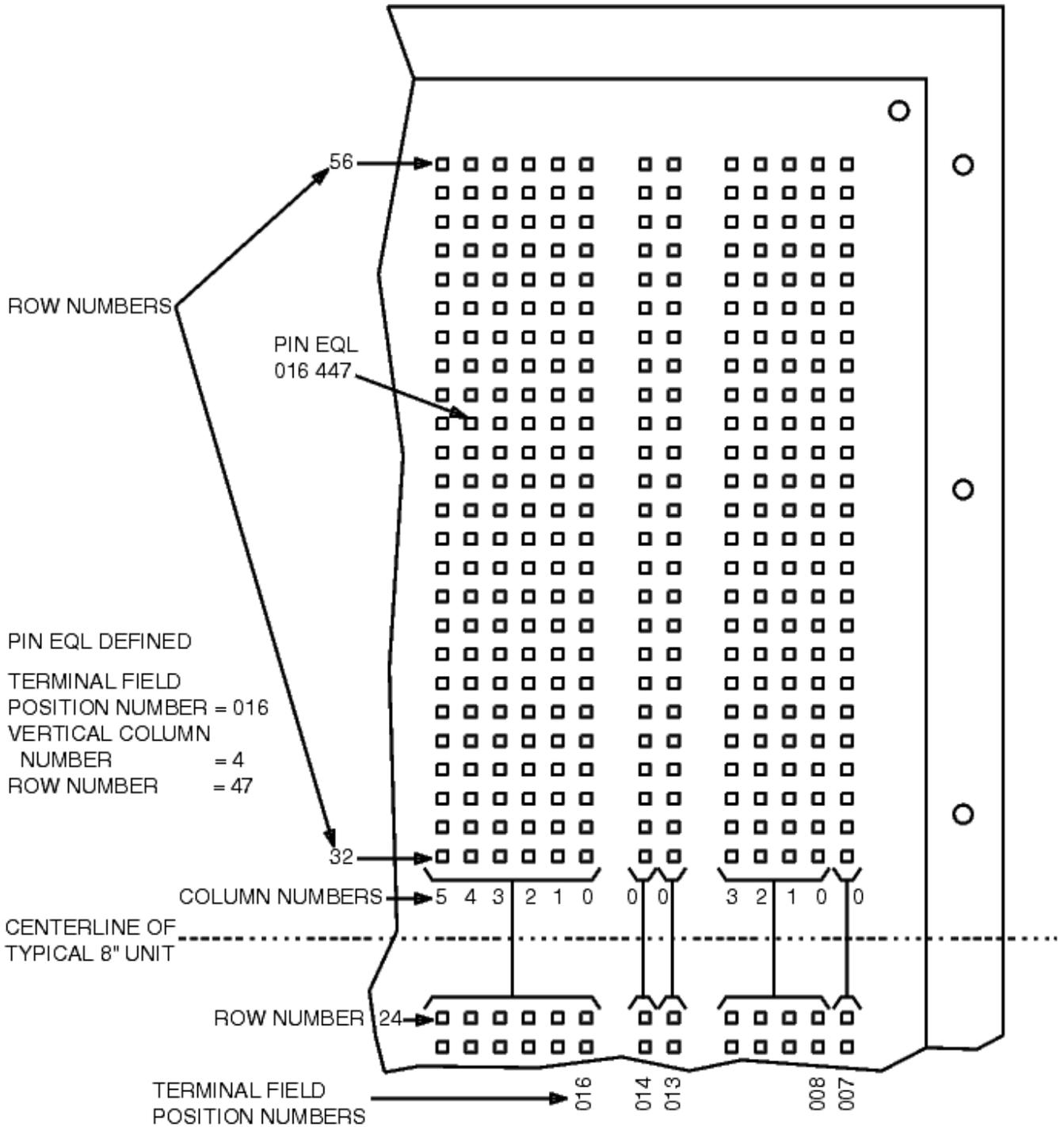


Figure 4-3 Terminal Field Position, Horizontal Row and Vertical Pin Numbers

4.2.5 EXAMPLES

Following are two examples that explain how to use an EQL to locate specific points of interest.

Example 1 is a report specifying the location of a faulty circuit pack. Example 2 is a request to locate a specific pin number on a backplane.

Example 1:

When a circuit pack is suspected of a fault, an MCC/read-only printer (ROP) report appears giving the pack location. This report includes the aisle number, the frame number, the bay number and a 9-digit EQL number or a portion thereof. Using the EQL number, determine the location of the circuit pack. For detailed identification, the code number of the circuit pack is on the report.

Refer to Figure 4-4 for an illustration of Example 1.

Example 2:

To locate a connector pin, use the EQL and the panel stamping on the back of the frame. For example, EQL 016 447 indicates panel stamped pin field 016 and the pin at vertical column 4, row 47.

Refer to Figure 4-3 for an illustration of Example 2.

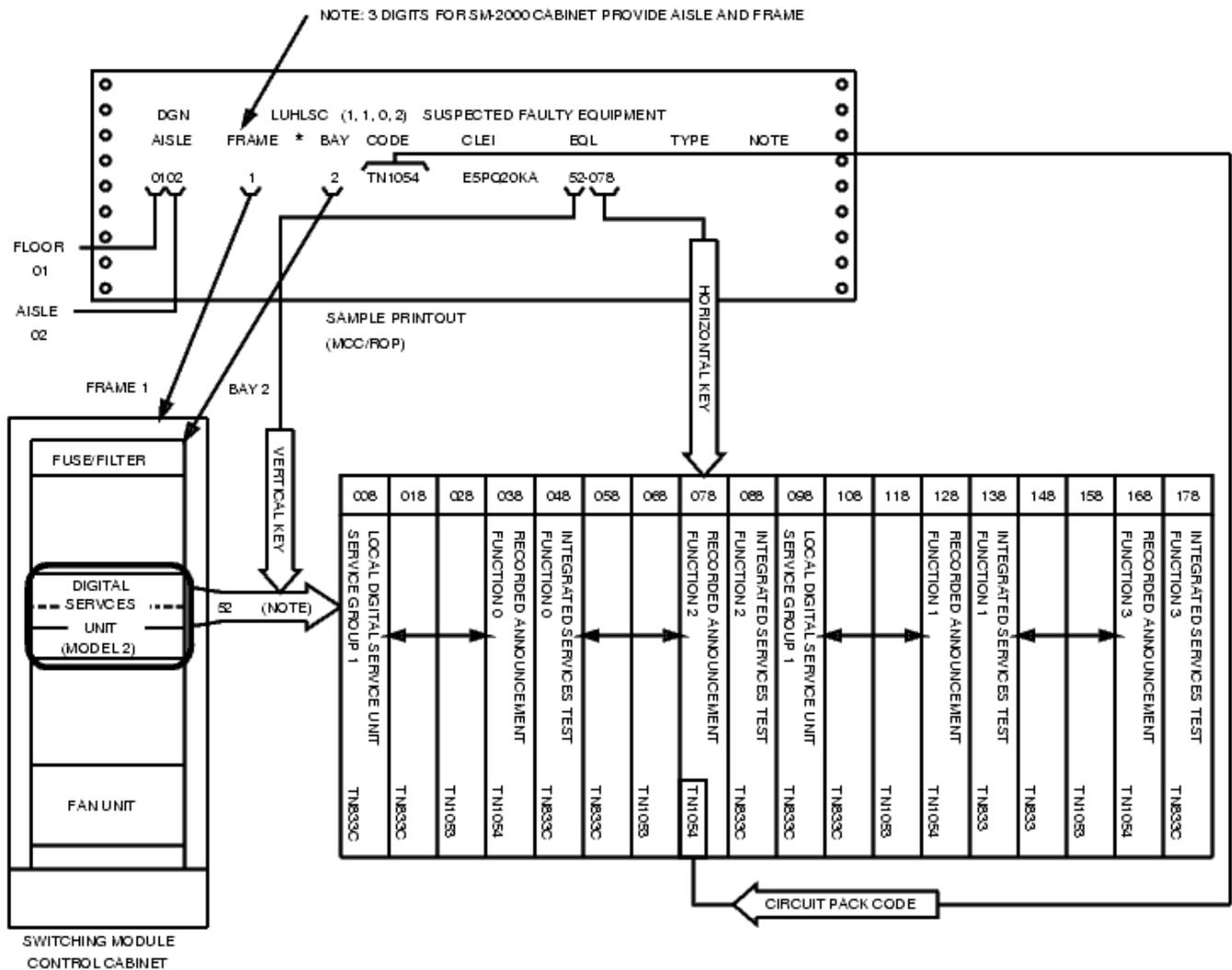


Figure 4-4 Circuit Pack Location

4.3 CIRCUIT PACKS

4.3.1 INTRODUCTION

Interaction of circuit packs within the switch establish the capability and reliability of the system. Circuit fault detection, identification and replacement make up a significant part of switch maintenance. Circuit packs have interchangeable information.

This section contains information about circuit packs; how to identify, handle, install and replace them.

4.3.2 CIRCUIT PACK IDENTITY CODES

Identity codes consist of an apparatus code, a series number, and a CLEI code. There are two types of circuit packs: a microcoded circuit pack that contains firmware and a circuit pack which contains no firmware. This information is screened on the faceplate (which has replaced the tab and latch and is interchangeable). The microcoded circuit pack contains the letters "MC" in the alphanumeric firmware identifier located at the top of the faceplate.

Figure 4-5 illustrates examples of the circuit pack identification information screened on the faceplate.

The circuit pack code identifies the type of circuit pack with an alphanumeric designation. For example: TN336. (TN-type pack connectors contain 200 pins in 4 columns and UN-type pack connectors contain 300 pins in 6 columns.)

The series number indicates the hardware level of the circuit pack. For example, "1" is located under the carrier pack code on the faceplate.

The CLEI code is the an identifier of circuit packs. The *CLEI*TM code is used mainly for inventory control, but it is also the means of identifying a specific circuit pack during maintenance procedures. The *CLEI*TM code appears on a self-adhering label on the circuit pack latch. Information on that portion of the label consists of scannable bar codes plus a readable 10-character *CLEI*TM code.

A breakdown of the *CLEI*TM code follows:

- Characters 1 through 3 describe the family and the subfamily.
- Character 4 is the code type.
- Characters 5 through 7 are a unique identity code.
- Characters 8 through 10 are the manufacturer, supplier and complementary data.

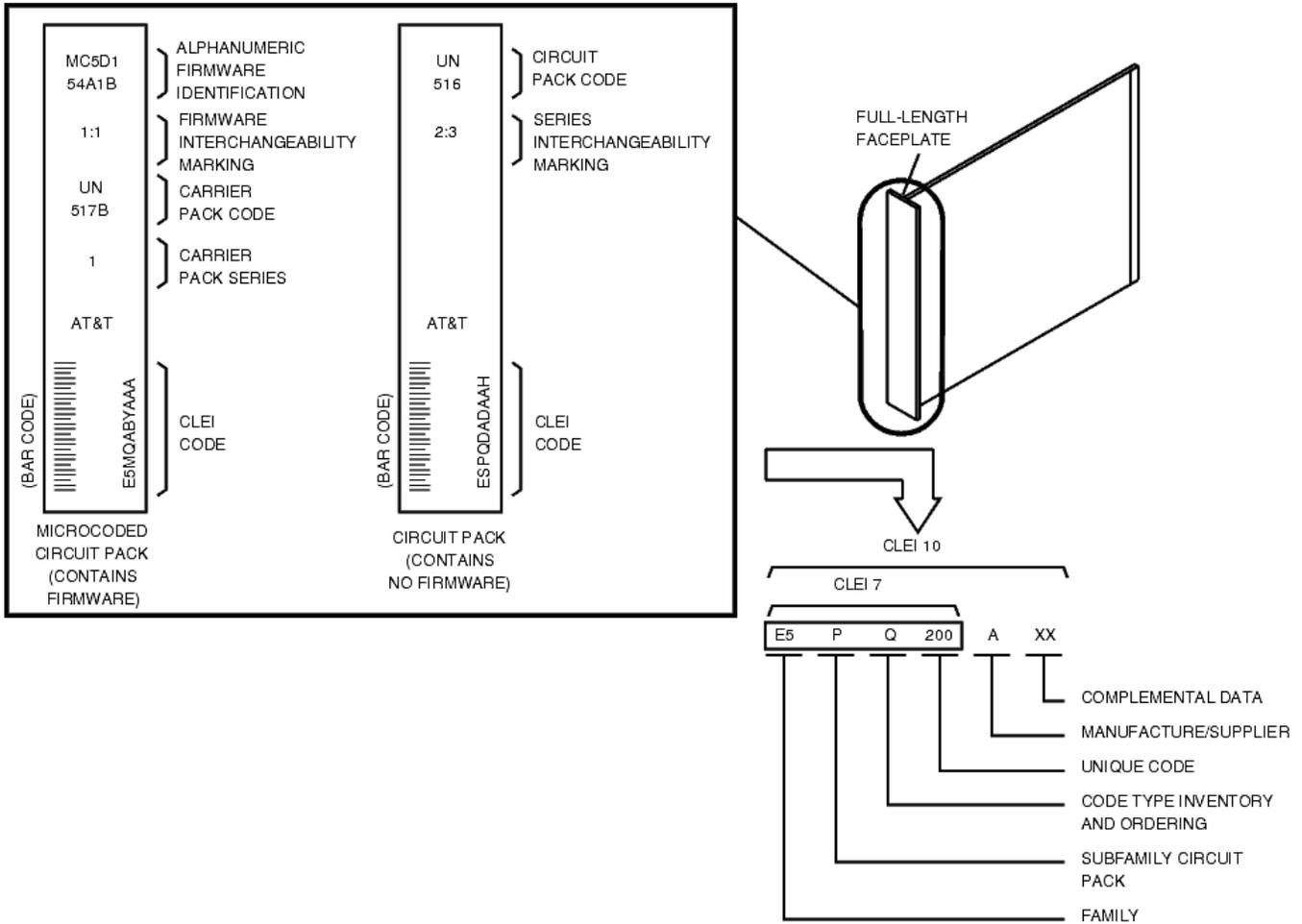


Figure 4-5 Circuit Packs

The first seven characters (CLEI 7) of the code reflect any changes to a pack. Whenever a new CLEI 7 code is assigned, a new bar code and designation strip are generated.

The circuit pack firmware label appearing on the circuit pack faceplate contains a fourth identifying code called a MICROCODE (MC) number. The information on the MC label consists of the alphanumeric firmware identification and the firmware issue number, for example, MC4C 001A1 10.

4.3.3 HANDLING CIRCUIT PACKS

4.3.3.1 Cautions

When it is necessary to handle circuit packs, ALWAYS observe the following cautions:

CAUTION 1: Handle circuit packs by their edges or face plates to avoid deforming components and leads or scratching the gold plated contacts. Damage or contamination can cause poor connections.

CAUTION 2: Before removing or inserting a circuit pack, power down the circuit, unless otherwise specifically directed by a maintenance procedure.

CAUTION 3: Sequential circuit pack removal and replacement is sometimes required. For example, Line Unit circuit packs may require this action (see 235-105-220). Always refer to detailed maintenance procedures if you have any questions about the removal sequence.

CAUTION 4: When changing circuit packs to locate a problem, always restore a pack to its original location if the replacement pack does not clear the fault. This helps isolate the trouble by returning the circuit to the original configuration which existed at the time the failure was first detected.

CAUTION 5: When handling circuit packs, always use care to avoid static discharges. Keep circuit packs in their antistatic shipping containers or some other antistatic environment until inserted. When inserting or removing circuit packs, be properly grounded, using a wrist strap connected to a frame ground or a designated ground connect point.

4.3.3.2 Replacing Circuit Packs

Review the cautions in this handbook for handling circuit packs.

Using information in the MCC, locate the suspected faulty circuit pack.

Most repairs of line and trunk units in switch modules do not need power removal and restoration. However, high-level control units (CU, DFC, IOP, MSCU, ONTC, DLI, RLI and MCTSI) have a power control/display pack (TN3, TN5, TN6, SN412, SN516, SN1077, etc.) and need unit power down before a circuit pack is removed or replaced.

Figure 4-6 illustrates the controls and indicators on a control/display pack

If unit power removal is required, do the following steps:

- (1) Move the RST/ROS slide switch to the ROS position and wait for the ROS light-emitting diode (LED) to light.
- (2) Wait until the RQIP LED lights, then goes off.
- (3) Wait until the Out Of Service (OOS) lamp lights.
- (4) Press the OFF push button and wait until OFF LED lights.

Unit power is now off.

Open the circuit pack latch and remove the pack. Keep the pack nearby if immediate replacement is needed.

Verify that the replacement circuit pack is the correct type and issue number.

Inspect the replacement pack for visible defects.

Inspect the contact surfaces and mating connectors for missing gold contacts, bent springs and any other visible defects.

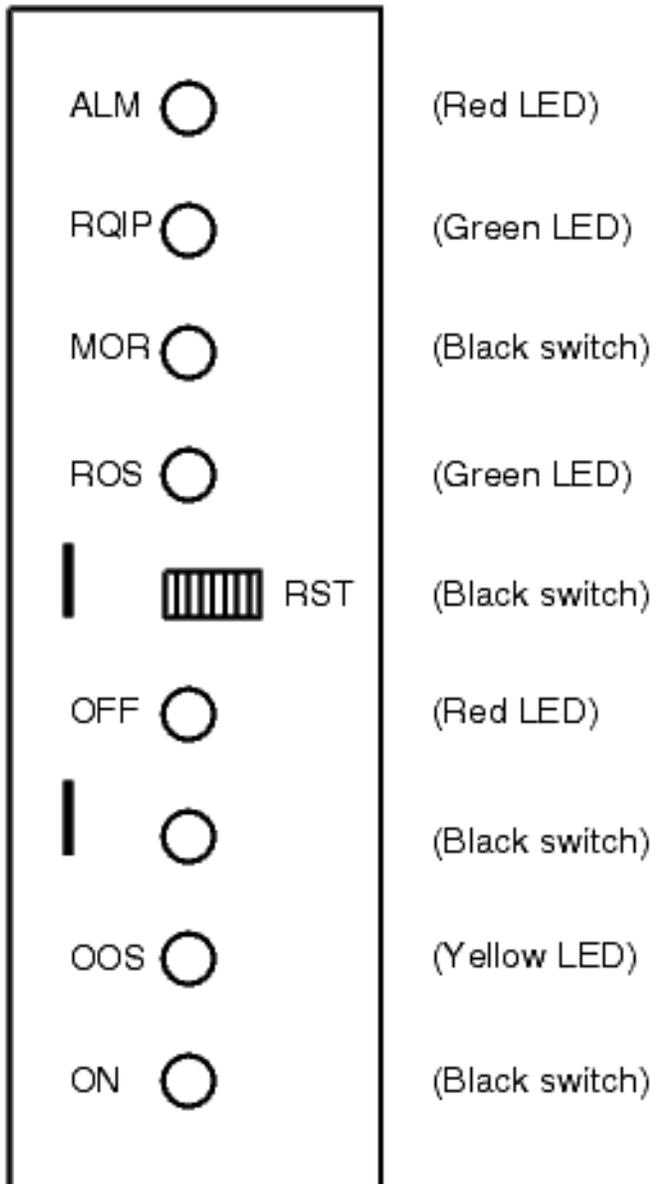
Carefully align the circuit pack with the upper and lower guide slots.

Insert the circuit pack into the guide slots and seat it by pushing firmly on the tabs located on the faceplate.

Restore power to the unit with the replaced pack by performing the following steps:

- (1) Press the ON push button and wait until OFF LED goes off.
- (2) Move the RST/ROS slide switch to the RST position.
- (3) Wait for the RQIP lamp to light and the OOS and RQIP lamps to go off.

Power is now restored to the unit.



LEGEND:

- ALM - ALARM
- LED - LIGHT-EMITTING DIODE
- MOR - MANUAL OVERRIDE
- ROS - REQUEST OUT OF SERVICE
- RQIP - REQUEST IN PROGRESS
- RST - RESTORE TO SERVICE
- OOS - OUT OF SERVICE

Figure 4-6 Control Display Circuit Pack

4.4 FANS AND FILTERS

4.4.1 FAN TYPES

Five types of fan assemblies are used in the switching module (SM) bays. The types are shown in Table 4-1 with a figure reference for each.

Table 4-1 SM Fans

ASSEMBLY	ID NO.	USED IN	FIGURE
3 Fans	J5D003BE-X(1-2)	SM Bays	4-7
6 Fans	J5D003BN-X(1-2)	SM Bays	4-8
3 Fans	J5D004AK-1	ISLU Drawers	4-9, 4-10 ^a
6 Fans	J5D003BW-1	SM Bays	4-11 ^b
3/6 Fans	J5D003FH-2	CM2C 5ESS [®] -2000 cabinets	4-12

Notes:

a. There are two versions of this fan assembly: one manufactured prior to June 1989 and one made since that date. The principal difference between the two versions is access for replacement. In the pre-June version, access is from the bottom of the assembly; in the later version, it is from the top.

b. This fan assembly is required only when there are more than three packet switches mounted in an SM bay. It is an exhaust fan only, requiring no filter, and it mounts in the top of the bay. It is used to supplement the standard bay fans.

4.4.1.1 Fan Assembly J5D003BE-X(1-2)

This is a 3-fan assembly (Figure 4-7) that is generally used throughout all configurations. It is mounted in the bottom aperture of a bay and access to the filter is from the front of the bay.

4.4.1.2 Fan Assembly J5D003BN-X(1-2)

This is a 6-fan assembly (Figure 4-8) that accommodates the addition of packet switches and the module controller time slot interchanger, model 2 (MCTSU2). It is mounted in the bottom shelf position of a bay and access to the filter is from the front of the bay.

4.4.1.3 Fan Assembly J5D004AK-1

This is a 3-fan assembly (Figures 4-9 and 4-10) that is mounted in each integrated service line unit (ISLU) drawer to cool the contents of the drawer. It supplements the 6-fan assembly in the bay. Access to the filter is from the rear of the drawer unit.

The two versions of the drawer fan assembly are as follows:

- One version, manufactured before June 1989, requires access from underneath the drawer to replace a fan.
- The second version, manufactured after June 1989, has access from the top of the drawer.

4.4.1.4 Fan Assembly J5D003BW-1

This is a 6-fan assembly (Figure 4-11) that mounts in the top shelf position of an SM bay containing packet switches. It is an exhaust fan unit required to supplement the standard bay fan assemblies when more than three packet switches are mounted in the bay. It contains no filter.

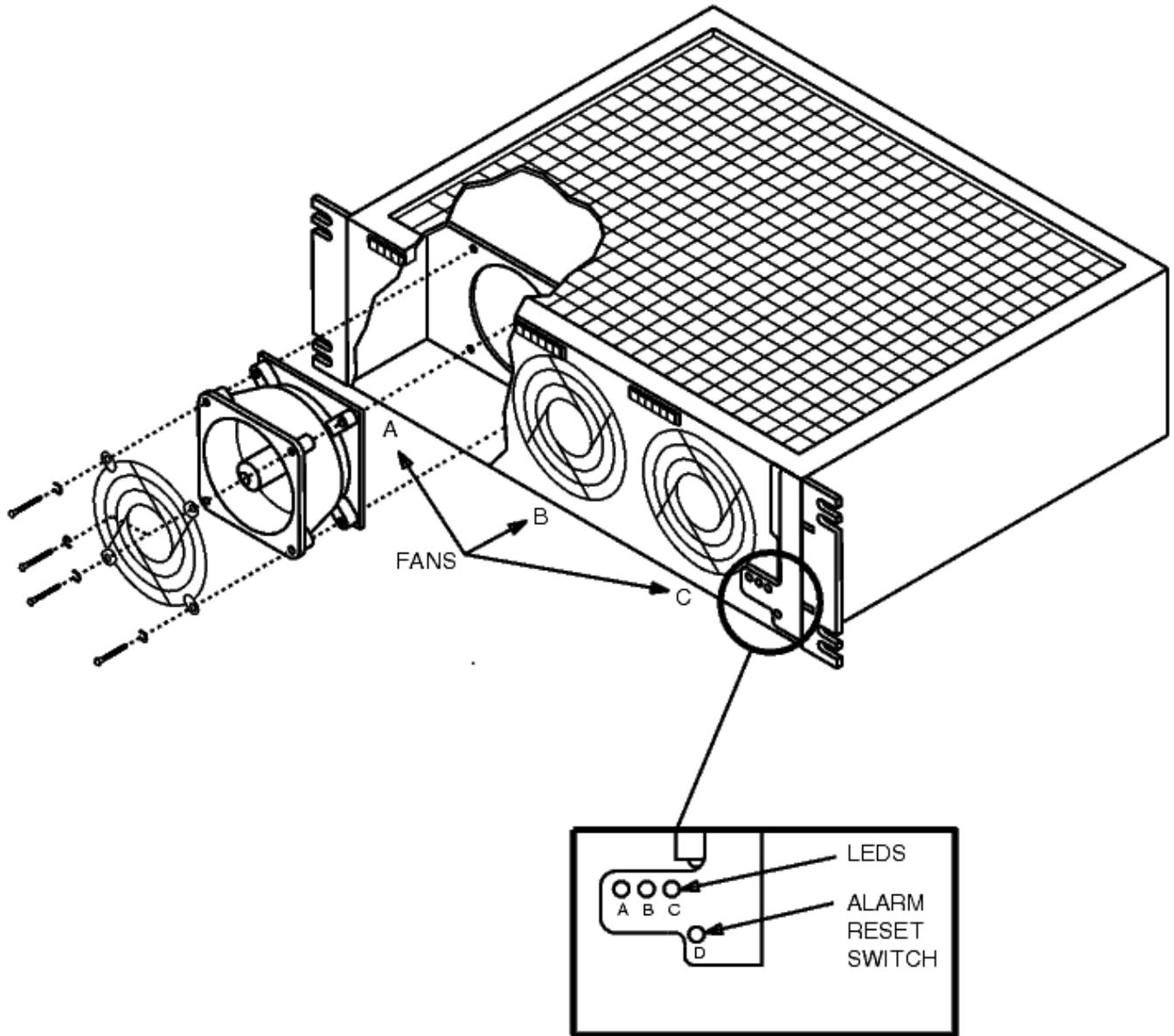


Figure 4-7 Fan Assembly (3 Fans) - J5D003BE-X (1-2)

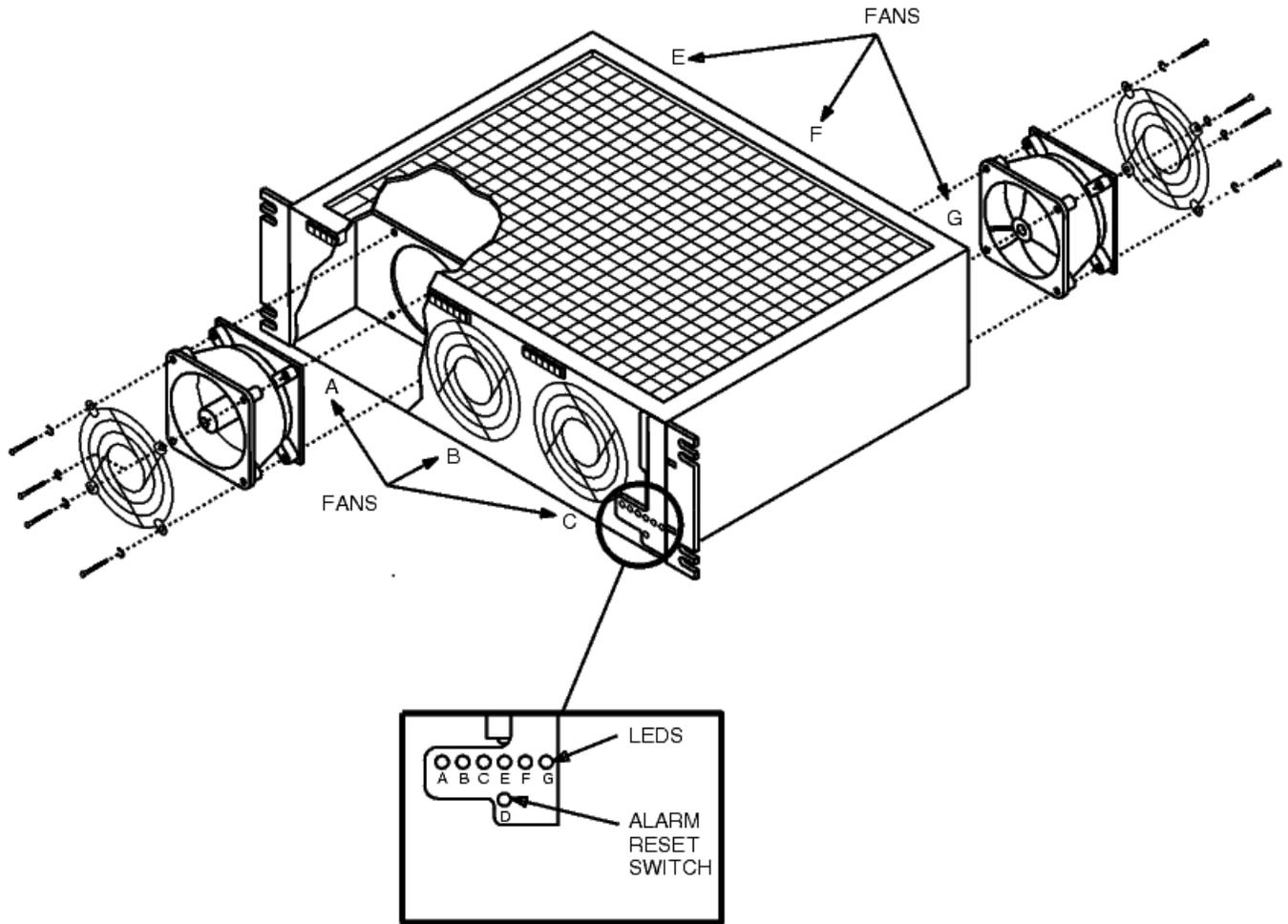


Figure 4-8 Fan Assembly (6 Fans) - J5D003BN-X (1-2)

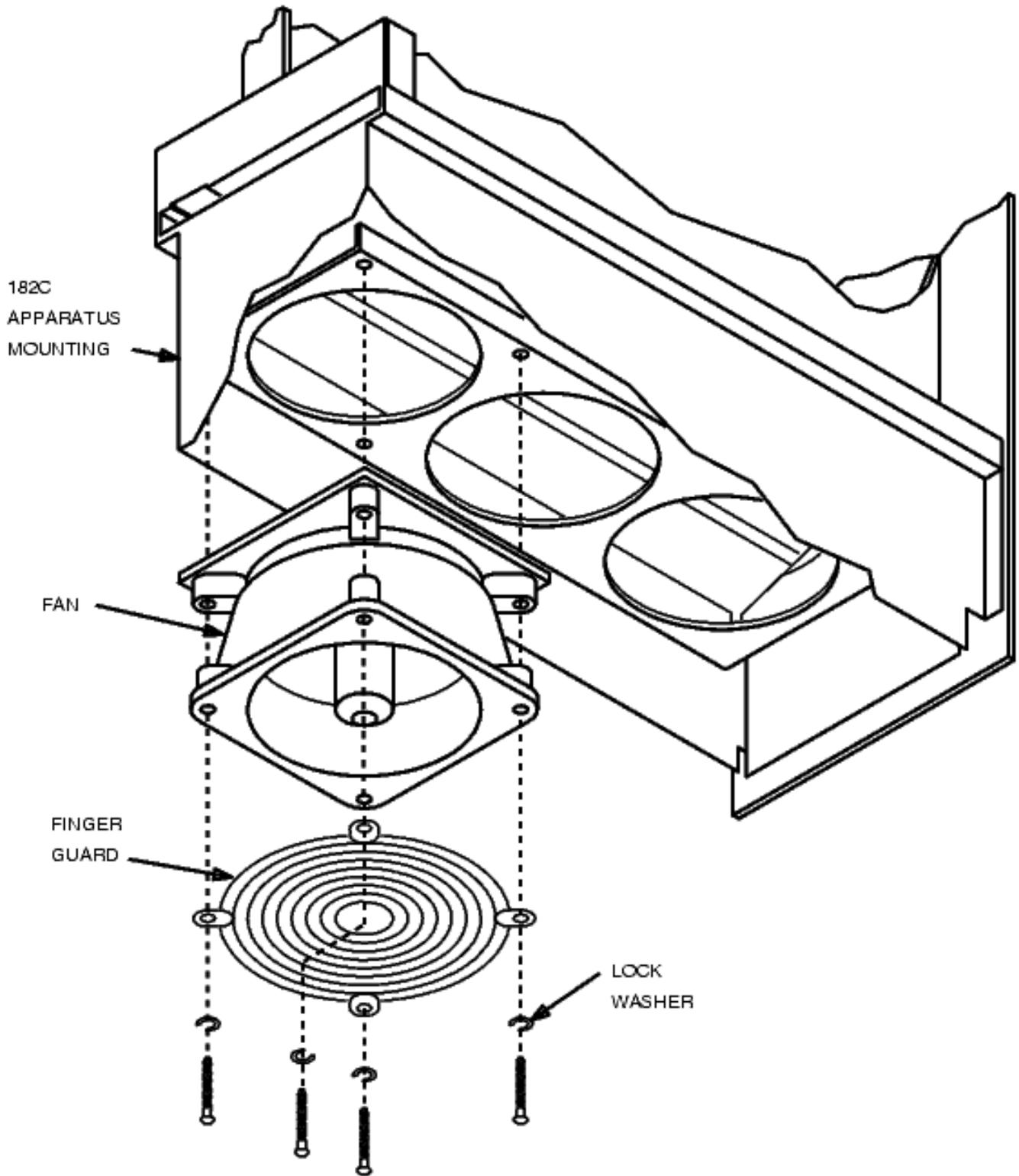


Figure 4-9 Fan Assembly J5D004AK-1 (Pre-June 1989)

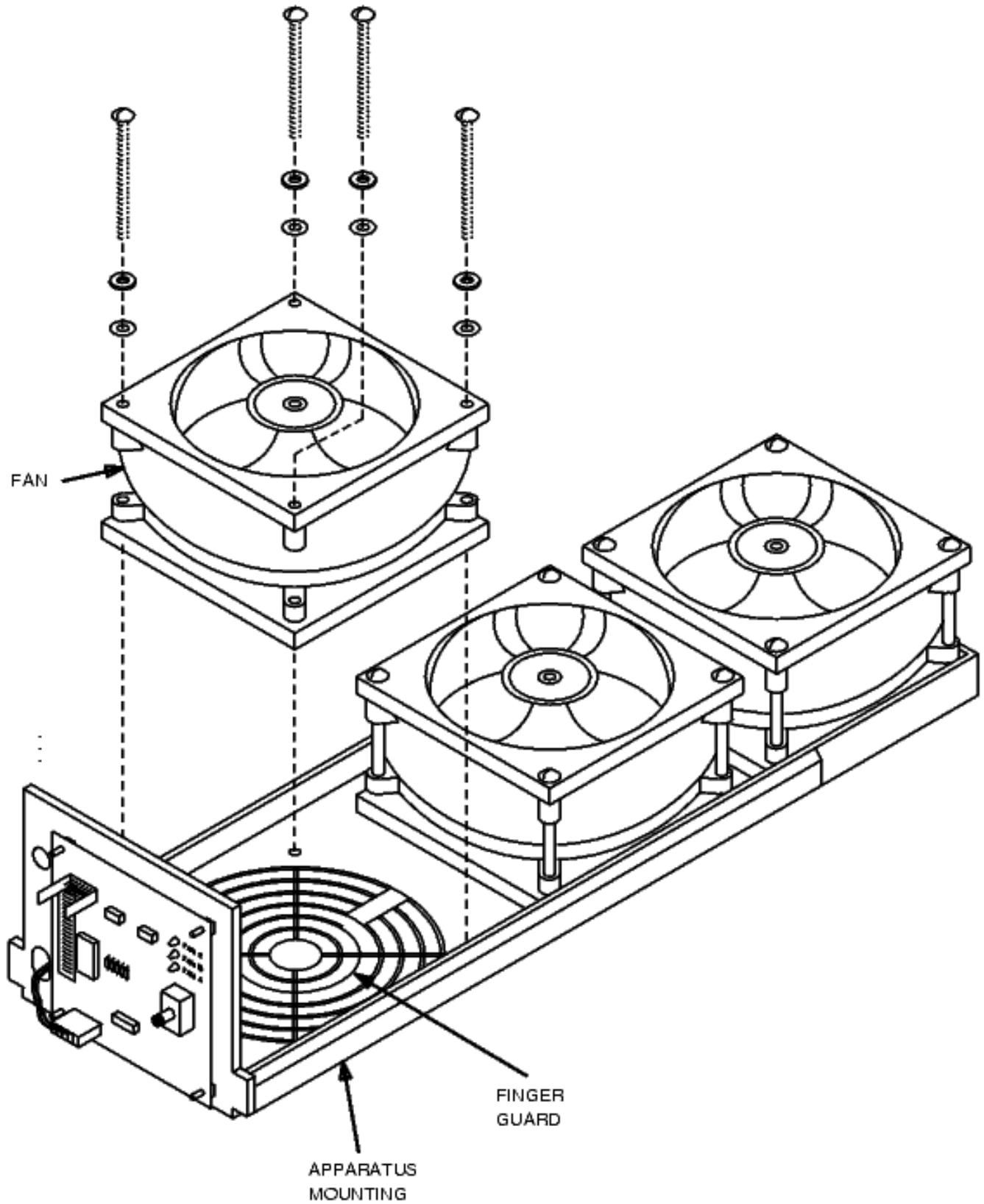


Figure 4-10 Fan Assembly J5D004AK-1 (Post-June 1989)

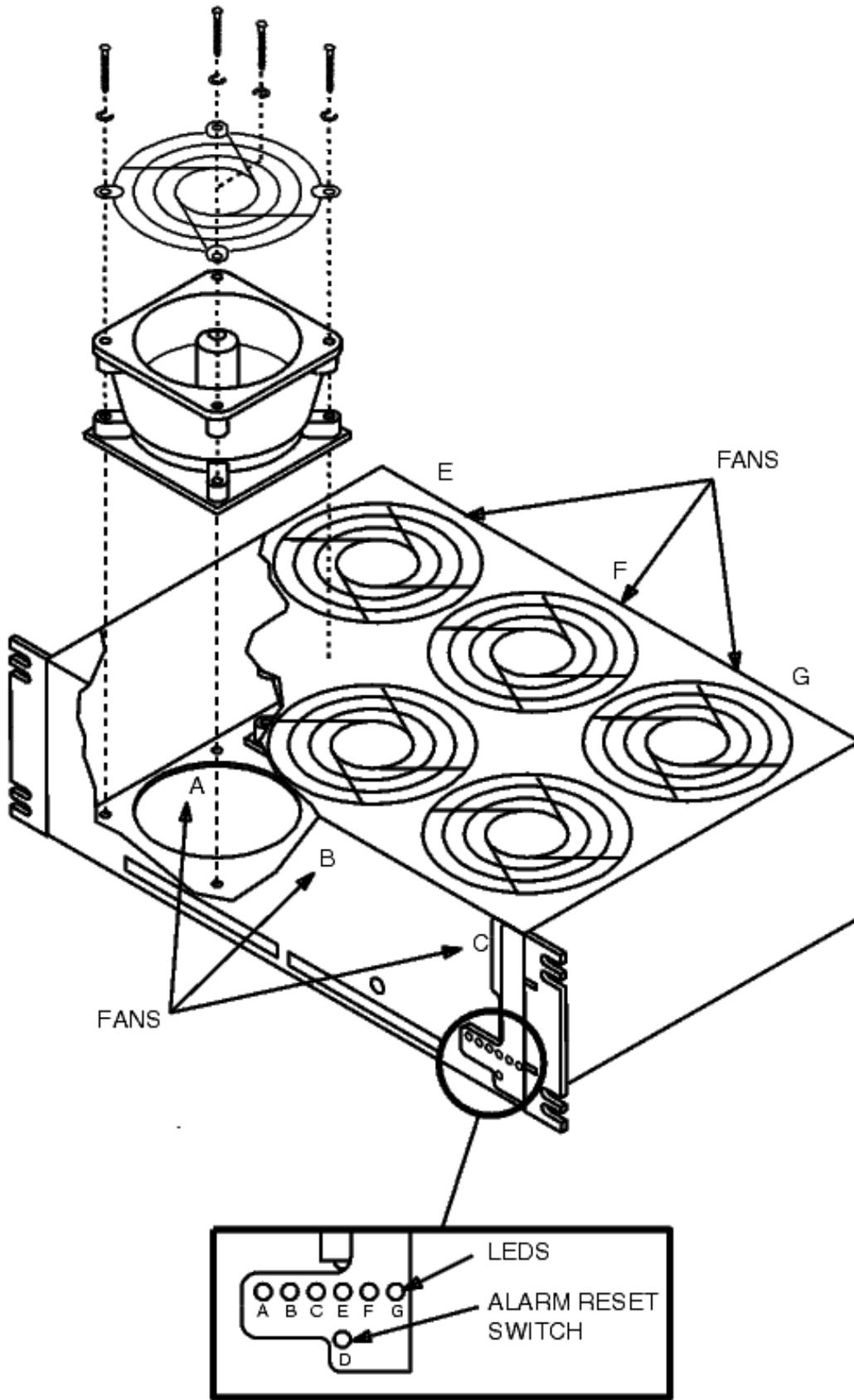


Figure 4-11 Fan Assembly J5D003BW-1 (6-Fan Exhaust)

4.4.1.5 Six-Fan Bi-directional Mid Fan Unit - J5D003FH-2

This fan unit is located in the middle position of a cabinet. This is a 3- to 6-fan assembly. This fan unit is currently only used with the SM-2000 for additional cooling to the upper and lower shelves. Figures 4-12 and 4-13 show the rear and front views of the fan unit.

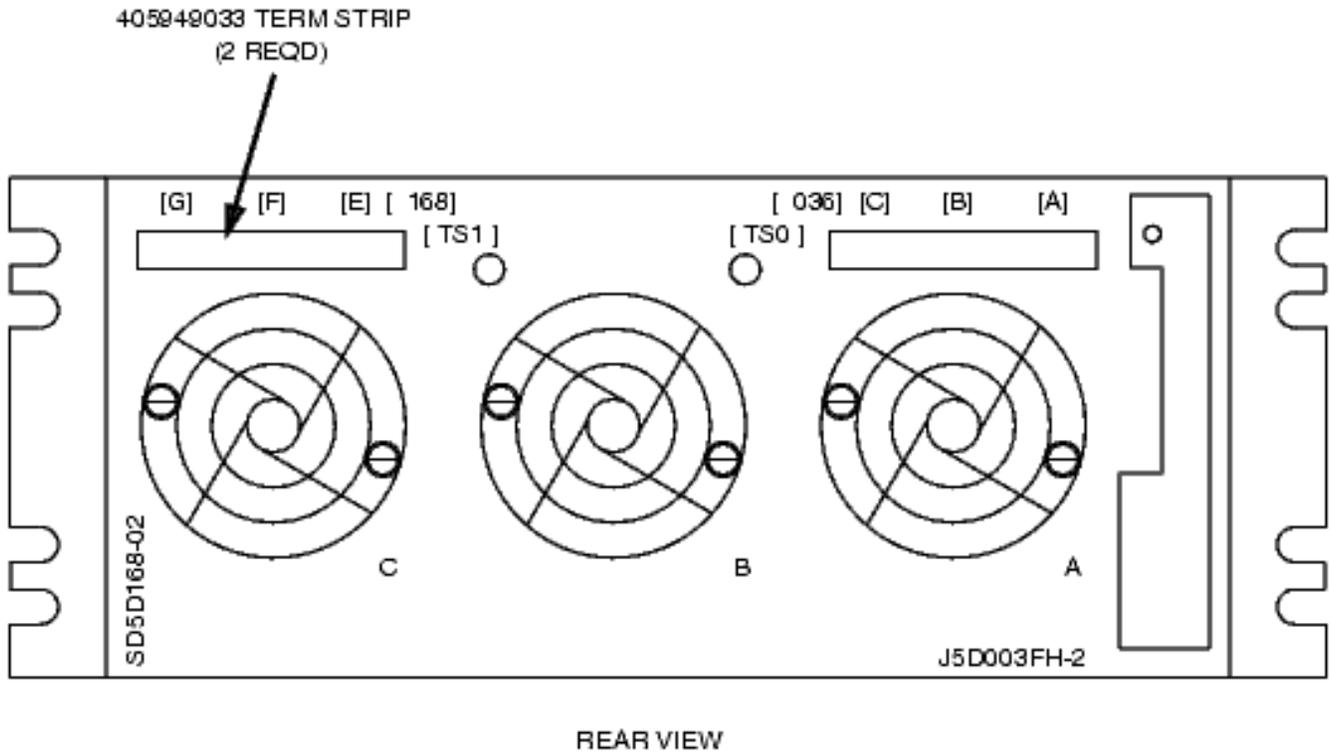


Figure 4-12 Fan Assembly (3-6 Fans) Rear View - J5D003FH-2

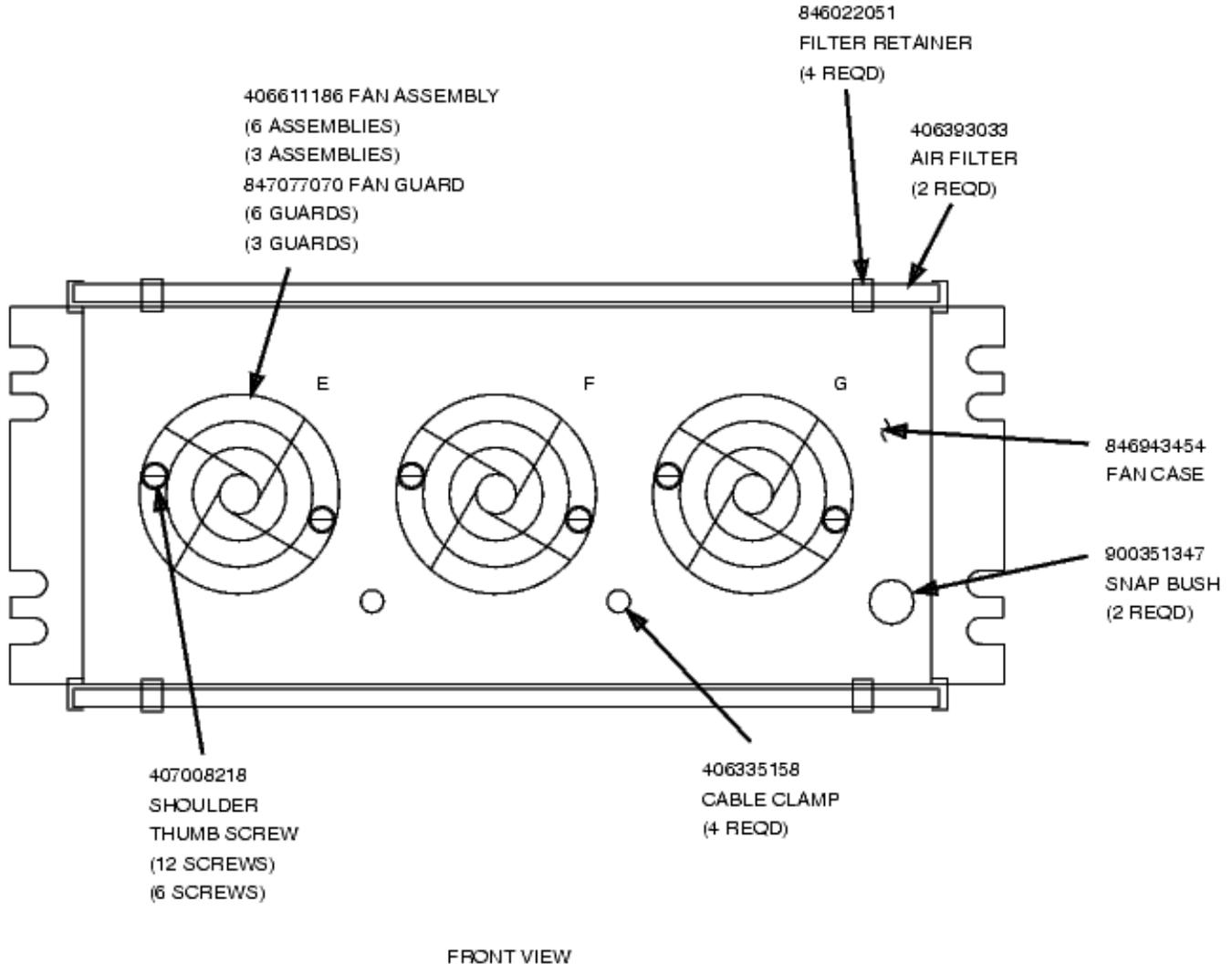


Figure 4-13 Fan Assembly (3-6 Fans) Front View - J5D003FH-2

4.4.2 GENERAL FAN OPERATION

Once turned on, the fans run continuously at +5 V DC, converted from -48 V DC. Fuses located in the fuse/filter panel may be removed to power down fan assemblies, except for the ISLU drawer fans.

Details for fusing and alarming assignments are shown on the office ED-5D651-15.

Fan performance for the 3-fan, 6-fan, bidirectional fan and exhaust fan units is monitored by an alarm circuit pack located in the rear of the fan unit. Fan performance for the ISLU is monitored by a 256A alarm circuit pack located on the rear of the fan unit for each ISLU drawer. Other fan units have their own alarm card. Lighted LEDs on the circuit pack identify a defective fan. The LED at the top of the switching module controller (SMC) or the line trunk peripheral (LTP) bay containing the fan also lights.

Powering down a fan unit does not result in an alarm condition. Fan alarm circuits are normally open and close only as a result of a fan malfunction.

Fan malfunctions are indicated by messages at the MCC and a major audible alarm. LEDs also light on the fan unit as seen from the rear of the bay and at the top of the bay as seen from the front.

It is not necessary to power down a fan unit to replace a filter except in the ISLU drawers. It is necessary to power down an ISLU fan to replace a filter. Fans in ISLU drawers share fuses with line groups in the drawers; therefore, **DO NOT REMOVE FUSES TO POWER DOWN AN ISLU FAN UNIT**. The ISLU drawer/fuse relationship is shown in Table 4-2.

Table 4-2 ISLU Drawer/Fuse Relationship

FANS	DRAWERS			
	1	2	3	4
A	LG3	LG7	LG11	LG15
B	LG2	LG6	LG10	LG14
C	LG1	LG5	LG9	LG13

To remove ISLU fan power, disconnect the upper cable assembly which may prevent removal of the filter (Figure 4-14).

Detailed procedures for filter replacement are found in 235-105-210.

Use fan blockers to restrict contaminated air flow while a filter is being replaced, but do not use fan blockers in fans located at the front of the bay.

Power down any fan unit to replace a faulty fan. When fan replacement is complete, reinsert the fuse (or reconnect the cable on the ISLU fan unit) to re-start the unit.

Detailed procedures for faulty fan replacement are found in Lucent 235-105-220.

The ISLU alarm pack (256A) must be connected to other ISLUs in the module and to the 3-fan and 6-fan units in the bottom of LTP SMC bays.

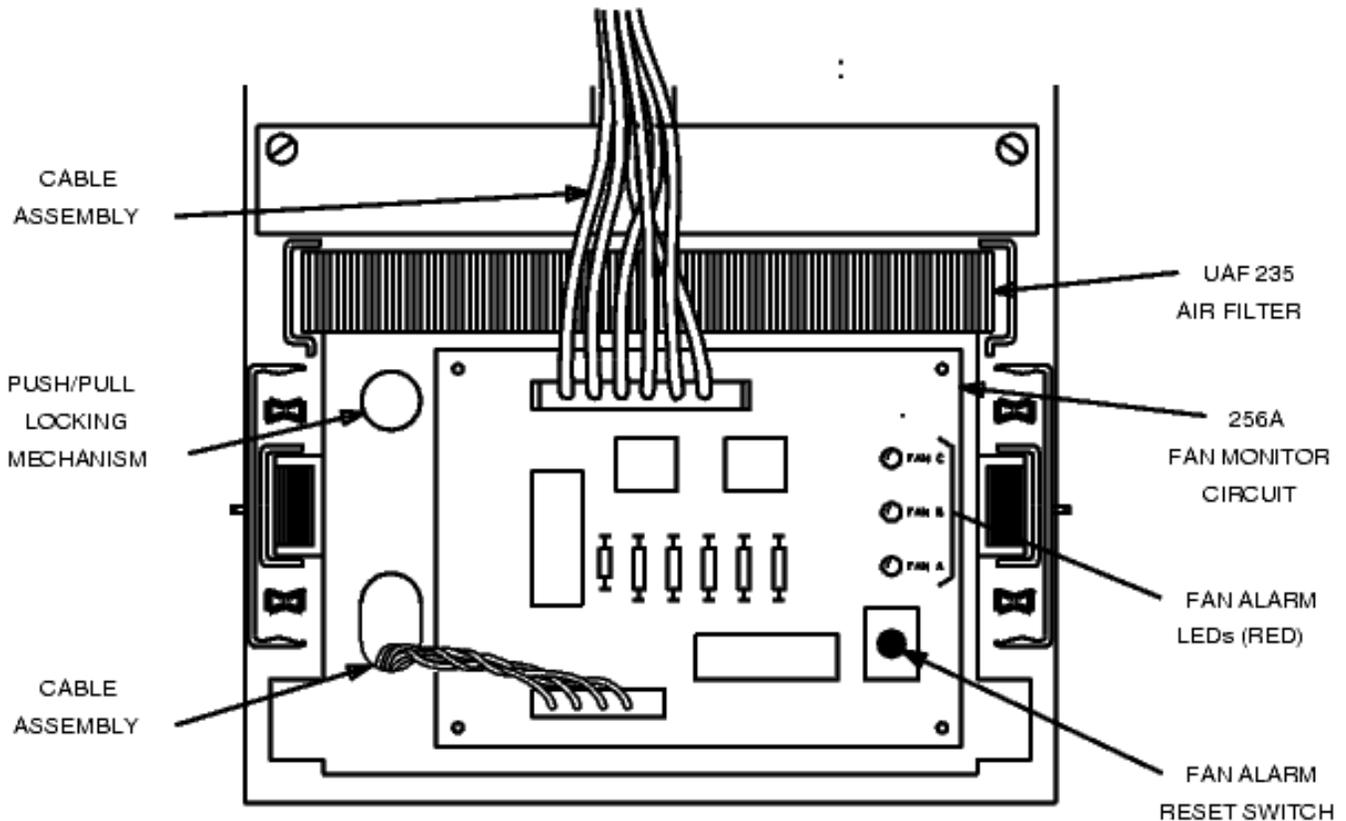


Figure 4-14 Rear View of ISLU Drawer Fan Assembly

5. FUNCTIONAL MODULES

This section gives information about the four modules that control the operations of the 5ESS[®]-2000 switch. Each module section is "stand alone" to find information easily.

The four sections are:

Section 5.1 - Administrative Module.

Section 5.2 - Communication Module.

Section 5.3 - Switching Modules.

Section 5.4 - Common Network Interface.

Table 5-1 lists functional module component units and their associated J Code and SD numbers.

Following is a list of tables that identify the circuit packs in the functional modules of the switch.

- (1) Table 5-2
- (2) Table 5-3
- (3) Table 5-4
- (4) Table 5-5
- (5) Table 5-6
- (6) Table 5-7
- (7) Table 5-8
- (8) Table 5-9
- (9) Table 5-10
- (10) Table 5-11
- (11) Table 5-12
- (12) Table 5-13
- (13) Table 5-14
- (14) Table 5-15
- (15) Table 5-16
- (16) Table 5-17
- (17) Table 5-18
- (18) Table 5-19
- (19) Table 5-20
- (20) Table 5-21

- (21) Table 5-22
- (22) Table 5-23
- (23) Table 5-24
- (24) Table 5-25
- (25) Table 5-26
- (26) Table 5-27
- (27) Table 5-28
- (28) Table 5-29
- (29) Table 5-30
- (30) Table 5-31
- (31) Table 5-32
- (32) Table 5-33
- (33) Table 5-34
- (34) Table 5-35
- (35) Table 5-36
- (36) Table 5-37
- (37) Table 5-38
- (38) Table 5-39
- (39) Table 5-40
- (40) Table 5-41
- (41) Table 5-42
- (42) Table 5-43
- (43) Table 5-44
- (44) Table 5-45
- (45) Table 5-46
- (46) Table 5-47
- (47) Table 5-48
- (48) Table 5-49
- (49) Table 5-50

(50) Table 5-51

(51) Table 5-52

(52) Table 5-53

(53) Table 5-54

The two types of tables are:

- One type (Table 5-2 , for example) lists the circuit packs present in a complete module and the number of each required to equip the respective units in the module.
- Another type (Table 5-3 , for example) lists the circuit pack contents of an individual unit (identified by J numbers), the number required and alternate compatible circuit packs, if any, that can be used.

The circuit packs are only those referred to in this document. The tables are not intended to list **ALL** circuit packs for any version of a switch. For variations in local circuit pack requirements, refer to office drawing T-XXXX-DO-3780. (The variable XXXX represents the number applicable to the local office "T" drawing.)

Also see ED4C168-14 and ED4C168-17 (IMS/CNI) for circuit pack interchangeability information.

Table 5-1 Functional Modules, Unit J-Codes and SD Numbers

UNIT NAME	J CODE	SD NUMBER
ADMINISTRATIVE MODULE		
Administrative Module (3B20D)	J1C176C-1	SD4C122-02
Processor Unit Cabinet (3B21D)	J3T060AA-1	SD3T011-01
Growth Unit Cabinet (3B21D)	J3T060AB	SD3T012-01
Power Distribution Unit	J1C147BE-1	SD4C102-01
Central Processor Unit	J1C147BA-1	SD4C098-01
Main Store Input/Output Disk File Controller Unit	J1C147BB-1	SD4C099-01
Main Store Input/Output Growth Unit	J1C147BC-1	SD4C097-01
Cooling Unit	ED-4C387-30	N/A
Port Switch Unit	J1C130BC-1	SD4C065-01
Tape/Disk Cabinet	J1C186A-1	SD4C126-01
Small Computer System Interface (SCSI) Unit	J3T027A	SD3T006-01
SCSI Disk File Controller	J3T027AA	N/A
Computer Peripheral	J3T059A-1	SD3T013-01
Growth Cabinet (3B21D)	N/A	N/A
Computer Processor Cabinet (3B21D)	J3T060A-1	SD3T014-01
Computer Processor Unit (3B21D)	J3T060AA-1	SD3T011-01
Computer Growth Unit (3B21D)	J3T060AB-1	SD3T012-01
Processor Computer System (3B21D)	J3T061A-1	SD3T015-01
Moving Head Disk(s)	KS22483	N/A
MSCU Model 3	J5D020AH-1	SD5D508-01
Tape Drive	KS23113	N/A
Digital Audio Tape	J3T060A-1	N/A
COMMUNICATION MODULES		
Message Switch Cabinet	J5D006C-1	SD5D146-01
Message Switch Control Unit	J5D006AB-1	SD5D026-01
Message Switch Peripheral Unit (Community 1)	J5D006AD-1	SD5D136-01
Message Switch Peripheral Unit (Community 2 & 3)	J5D006AC-1	SD5D126-01
Message Switch Peripheral Unit-Model 3	J5D020AC-1	SD5D078-01
Message Interface Clock Unit	J5D006ED-1	SD5D082-01
Time Multiplex Switch Cabinet	J5D001C-1	SD5D147-01
Time Multiplex Switch Unit	J5D007AB-1	SD5D043-01
Time Multiplexed Switch Unit Model 2	J5D020AD-1	SD5D061-01
Time Multiplexed Switch Unit Model 3	J5D020AG-1	SD5D061-01
Time Multiplex Control Unit	J5D001AA	SD5D037-01
Communication Module - Model 2 (Basic)	J5D020A-1	SD5D140-01
Communication Module - Model 2 (Growth)	J5D020B-1	SD5D140-01
Time Multiplexed Switch Unit Model 2	J5D020AD-1	SD5D061-01

Time Multiplexed Switch Unit Model 3	J5D020AG-1	SD5D191-01
Communication Module Control Unit	J5D020AA-1	SD5D060-01
Message Switch Control Unit-Model 2	J5D020AB-1	SD5D077-01
Message Switch Control Unit-Model 3	J5D020AH-1	SD5D508-01
Message Switch Peripheral Unit-Model 3	J5D020AC-1	SD5D078-01
Communication Module-Model 2 (Basic)	J5D020A-1	SD5D140-01
Communication Module-Model 2 (Growth)	J5D020B-1	SD5D140-01
Communication Module Control Unit	J5D020AA-1	SD5D060-01
Communication Module Processor Unit	J5D020AF-1	SD5D178-01
Communication Module Unit	J5D020AJ-5	SD5D513-01
E Bus Unit	J5D020E-1	N/A
SWITCHING MODULES		
FIU Module 3 (supports RSMs)	J5D003AP-3	SD5D401-02
Switching Module Control Cabinet	J5D003E-1	SD5D118-03
TRCU (supports ORMs)	J5D003ED-2	SD5D118-03
Switching Module Control Cabinet	J5D003L-1	SD5D160-01
Remote Control Unit (supports RSM)	J5D003FC-1	SD5D075-01
Digital Line Trunk Unit (RISLU)	J5D003FF-1	
Line Trunk Peripheral Unit	J5D003F-1 or F-2	SD5D119-01
Basic Digital Carrier Unit - Model 2	J5D003AR-2	SD5D202-01
Supplementary Digital Carrier Unit - Model 2	J5D003AS-2	SD5D203-02
Digital Service Unit (Local or Global)	J5D003AE-1	SD5D035-01
Digital Service Unit - Model 2	J5D003EA-1	SD5D042-01
Digital Service Unit - Model 2 (RAF & ISTF)	J5D003EA-1	SD5D092-01
Digital Service Unit - Model 3	N/A	N/A
Modular Metallic Service Unit	J5D003BD-1	SD5D015-01
Directly Connected Test Unit	J1P023AM-1	SD2P077-01
Memory Expansion Unit	J5D003BH-1	SD5D048-01
Module Controller Time Slot Interchanger	J5D003EC-1	SD5D094-01
Line Unit - Model 2	J5D004AC-2	SD5D052-01
Line Unit - Model 3	J5D004AD-1	SD5D180-01
Digital Line Trunk Unit (DLTU)	J5D003AD-1	SD5D201-01
Digital Line Trunk Unit - Model 2 (DLTU2)	J5D003xxx	SD5D5xxx
Analog Trunk Unit	J5D003AC-1	SD5D300-01
Switching Module Control Cabinet	J5D003L-1	SD5D160-01
Integrated Digital Carrier Unit	J5D003FL-1	SD5D301-01
Integrated Services Line Unit	J5D004AK-1	SD5D091-01
Digital Service Unit - Model 2 (RAF & ISTF)	J5D003EA-1	SD5D092-01
Packet Switch Unit	J5D003BL-1	SD5D074-01
Module Controller Time Slot Interchanger - (Model 2)	J5D003LA-1	SD5D151-01
Module Controller Time Slot Interchanger - (Model 3)	J5D003LB-1	SD5D536-01
Switch Module Processor 2	J5D003AY-1	SD5D129-01
Digital Network Unit-SONET	J5D003FR-1	SD5D525-01
5ESS® 2000 Switch Cabinet	J5D003N-1	SD5D198-01
TSIU4	J5D003NB-1	SD5D196-01
SMPU4	J5D003NA-1	SD5D195-01
DSU3	J5D003NC-1	SD5D197-01
COMMON NETWORK INTERFACE (CNI)		
CNI Cabinet	J3F011C-1	
Group 00:		
—Shelves Positions 0 and 1	J3F011AA	SD3F008-01
—Shelf Position 2	J3F011AC	SD3F010-01
Group 32:		
—Shelves Positions 3 and 4	J3F011AA	SD3F008-01
—Shelf Position 5	J3F011AC	SD3F010-01
Digital Facility Access (DFA) Cabinet	J3F010F1	SD3F027-01
Digital Service Unit	J3F010BE-1	
Digital Service Adapter Unit	J3F010BA-1	

Table 5-2 Administrative Module (AM) Circuit Packs (3B20D)

CP CODE	FUNCTION	UNITS ^a				
		C	I	I	I	P
		P	O	O	O	S
		U	P	P	P	U
			B	G	D	
			U	U	F	
					C	

					U	
TC5	Power Control	1				
TF2	Scanner Signal Distributor Interface					1
TF4	Port Switch					2
TN3B	Disk File Controller Power Control				1	
TN5B	Power Control	1				
TN6	I/O Power Controller		1			
TN9	Power Converter		2	2		
TN10	Emergency Act Interface	1				
TN14	Microcontrol Store B				1	
TN56	Main Store Array			8	8	
TN61B	Peripheral Interface Controller		1	1		
TN64B	Duplex Dual Serial Bus Selector				1	
TN68	Microcontrol A				2	
TN69B	Duplex Serial Bus Selector		1	1		
TN70B	Bus Interface Controller		1		1	
TN74B	TTY Peripheral Controller		1	1		
TN83B	Maintenance Terminal Controller		1	1		
TN84B	Microcontrol Store		1	1		
TN983	Maintenance Terminal Controller		1	1		
TN2012	Main Store Array			8	8	
UN1C	Data Manipulation Unit 0	1	1			
UN2B	Special Register 0	1	1			
UN3B	Special Register 1	1	1			
UN3C	Special Register 1	1				
UN6B	Store Data Control	1				
UN9B	Dual Serial Channel			4	1	
UN10B	Cache Memory Controller	2				
UN10C	Cache Memory Controller	2				
UN11C	Cache Memory	1				
UN15B	Microlevel Test Set	1				
UN19B	Dual Serial Channels			4		
UN21B	Utility Circuit	1				
UN23C	Data Manipulation Unit	1				
UN25B	Selectable Microprocessor Interface		2			
UN28B	Maintenance Channel	1				
UN33D	Maintenance Channel		8			
UN43C	Store Address Control	1				
UN43D	Store Address Control	1				
UN45B	Store Address Control	1				
UN45C	Store Address Control	1				
UN46C	Direct Memory Access				3	
UN48B	4KWMS	3				
UN55	Disk File Controller Interface				1	
UN59C	Main Store Controller				1	
UN64	Peripheral Disk Interface				1	
UN133	Main Store Update	1				
UN133B	Main Store Update	1				
UN139	MC4C	1				
UN245	Special Register 1	1				
195FA	Power Unit	2		2	2	

Notes:

a. Legend for Acronyms

CPU Central Processor Unit

IOPBU Input/Output Basic Unit

IOPGU Input/Output Growth Unit MAS Growth

IOPDFCU I/O Disk File Controller

PSU Port Switch Unit

Table 5-3 AM Central Processor Unit J1C147BA-1 Circuit Packs (3B20D)

CP CODE	FUNCTION	NO REQ	ALT CP
---------	----------	--------	--------

195FA	Power Unit	2	-
TC5	Power Control	1	-
TN5B	Power Control	1	-
TN10	Emergency Act Interface	1	-
UN1C	Data Manipulation Unit 0	1	-
UN2B	Special Register 0	1	-
UN3B	Special Register 1	1	-
UN3C	Special Register 1	1	-
UN6B	Store Data Control	1	-
UN10B	Cache Memory (Controller)	2	-
UN10C	Cache Memory (Controller)	2	-
UN11C	Cache Memory	1	-
UN15B	Microlevel Test Set	1	-
UN21B	Utility Circuit	1	-
UN23C	Data Manipulation Unit 1	1	-
UN28B	Maintenance Channel	1	-
UN43C	Store Address Control	1	-
UN43D	Store Address Control	1	-
UN45B	Store Address Translator	1	-
UN45C	Store Address Translator	1	-
UN48B	4KWMS	3	-
UN133	Main Store Update	1	-
UN133B	Main Store Update	1	-
UN139	MC4C	1	-
UN245	Special Register 1	1	-

Table 5-4 AM Input/Output Basic Unit J1C147BD-1 Circuit Packs (3B20D)

CP CODE	FUNCTION	NO REQ	ALT CP
494G1	Power Unit Controller	1	-
495FA	Power Unit	2	-
TN6	I/O Power Controller	1	-
TN9	Power Converter	2	-
TN61B	Peripheral Interface Controller	1	-
TN69B	Duplex Serial Bus Selector	1	-
TN70B	Bus Interface Controller	1	-
TN74B	TTY Peripheral Controller	1	-
TN83B	Maintenance Terminal Controller	1	TN983
TN84B	Microcontrol Store	1	-
TN983	Maintenance Terminal Controller	1	TN83B
UN25B	Selectable Microprocessor Interface	2	-
UN33D	Peripheral Controller	8	-

Table 5-5 AM Input/Output Growth Unit J1C147BC-1 Circuit Packs (3B20D)

CP CODE	NAME	NO REQ	ALT CP
195FA	Power Unit	2	-
TN9	Power Converter	2	-
TN28	Main Store Array	8	TN56
TN56	Main Store Array	8	TN28
UN9B	Dual Serial Channels	4	UN19B
UN19B	Dual Serial Channels	4	UN9B
a	Peripheral Controllers	8	-

Notes:

a. Various Peripheral Controllers are optional for use in the IOP Growth Unit. For specific local-office assignments, refer to office drawing T-XXXX-DO-3780.

Table 5-6 AM Input/Output Disk File Controller J1C147BB-1 Circuit Packs (3B20D)

CP CODE	NAME	NO REQ	ALT CP
195FA	Power Unit	2	-
TN3B	Disk File Controller Power Control	1	-
TN14	Microcontrol Store B	1	-
TN28	Main Store	8	TN56
TN56	Main Store	8	TN28
TN64B	Duplex Dual Serial Bus Selector	1	-
TN68	Microcontrol A	2	-
TN70B	Bus Interface Controller	1	-
TN2012	Main Store	8	TN56

UN9B	Dual Serial Channel	1	-
UN46C	Direct Memory Access	3	-
UN55	Disk File Controller Interface	1	-
UN59C	Main Store Controller	1	-
UN64	Peripheral Disk Interface	1	-

Table 5-7 AM Port Switch Unit J1C130BC-1 Circuit Packs (3B20D)

CP CODE	NAME	NO REQ	ALT CP
TF2	Scanner Sig. Dist. Interface	1	-
TF4	Port Switch	2	-

Table 5-8 Administrative Module (AM) Circuit Packs (3B21D)

CP CODE	FUNCTION	UNITS		
		CU	DFC	IOP
410AA	Power Converter	2	2	8
KBN10	Input/Output Processor			4
KBN15	Direct Memory Access	2		
KLW31	Central Control	2		
KLW40	Memory Module	2		
TN74B	Terminal Controller			27
TN75C	Sync DLC			20
TN82C	X.25 Sync DLC			2
TN983	Maintenance TTY			2
TN1820	IOP Switch			4
TN1821	Control Unit Power Switch	2		
TN2116	Disk File Controller B		2	
UN33D	Scanner & Signal Distributor			13
UN373	Disk File Controller A		2	
UN375	SCSI Disk (MHD)		16	
UN377	Port Switch & Distributor Buffer			1
UN379	Utility Circuit	2		

Table 5-9 AM Processor Unit (Basic) J3T060AA-1 Circuit Packs (3B21D)

CP CODE	FUNCTION	NO REQ	ALT CP
410AA	Power Converter	5	-
KBN10	Input/Output Processor	1	-
KBN15	Direct Memory Access	1	-
KLW31	Central Control	1	-
KLW40	Memory Module	1	-
TN74B	Terminal Controller	8	-
TN75C	Sync DLC	8	-
TN82C	X.25 Sync DLC	1	-
TN1820	Input/Output Process Power Switch	1	-
TN1821	Control Unit Power Switch	1	-
TN2116	Disk File Controller B	1	-
TN983	MTTY Controller	1	-
UN33D	Scan & Scan Distributor	7	-
UN373	Disk File Controller A	1	-
UN375	SCSI Disk	4	-
UN377	Port Switch & Distributor Buffer	1	-
UN379	Utility Circuit	1	-

Table 5-10 AM Growth Unit J3T060AB-1 Circuit Packs (3B21D)

CP CODE	FUNCTION	NO REQ	ALT CP
410AA	Power Converter	2	-
KBN10	Input/Output Processor	1	-
TN74B	Terminal Controller	16	-
TN75C	Sync DLC	16	-
TN1820	Input/Output Power Switch	1	-
UN82C	X.25 Sync DLC	16	-
UN375	SCSI Disk (MHD)	5	-

Table 5-11 Communication Module (CM) Circuit Packs

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CP CODE	FUNCTION	UNITS ^a											
		C	C	E	M	M	M	M	M	M	T	T	T
		M	M	B	I	S	S	S	S	S	M	M	M
		C	P	U	C	C	P	P	P	C	S	S	S
		U	U	S	U	U	U	U	U	U	U	U	U
								2		3			2
410AA	-5 V Power Converter	1	1										2
410CA	-2 V Power Converter												1
495FB	Power Converter					2	2	1	2	2	2	4	
495G1	Power							1					
495KA	+12 V, +5 V, Power Converter	1			1								
495MA	-2 V Power Converter	1											
KBN1/4	Fabric Board												4
KBN2	Fabric Controller												2
SN412	Power Control & Display	1	1			1	2	1	1	2			1
SN516	Power Control & Display	1	1			1	2			2			1
TN61B	Peripheral Interface Cont.					1							
TN69B	Duplex Dual Serial Bus Sel.						1						
TN70B	Bus Interface Cont.					1	1						
UN183	Control Interface	1											
TN242	Fabric Board											8	
TN243	Link Interface											1	
												4	
												2	
TN244	Shelf Interface												
TN245	Sync./Standalone				1								
TN252	Message Link Interface									1			
TN265	TMS Main Board									1			
TN267	Test Board									1			
TN268	TMS Controller (UP)									1			
TN269	TMS Interface									1			
TN270	Clock Interface									1			
TN698	Duplex Dual Serial Bus Sel.					1							
TN834	Link Interface				1								
TN835	Link Interface				1								
TN848	Microcontrol Store					2							
TN856	Message Sw. Periph. Processor							2	2				
TN856B	Message Sw. Periph. Processor						2			8			
TN858	Module Message Processor							8					
TN1681	Quad-Link Interface 2											1	
TN1682	Quad-Link Packet Switch											1	
TN1683	Quad-Link Gateway Processor Board	1											
TN1684	Quad-Link Processor Board	1											
TN859	Message Interface				1								
TN860	Message Interface				1								
TN861	Message Interface				1								
TN862	Message Interface				1								
TN870	Message Interface Bus Cont.									8			
TN881	Clock Interface	1											
TN882	Control Interface Bus	1											
TN883	Foundation Link Interface												1
TN884	Time Multiplexed Sw. Cont.	1											
TN886	Pump Periph. Controller					1	1	1					
TN888	Quad Link Interface												8
TN1034	Dual Message Interface	2											
TN1130	Digital Phase Lock Loop				1								
TN1131	Controller				1								
TN1274B	Synchronizer	1											
TN1276	Digital Phase Lock Loop	1											
TN1284	Oscillator	1											
TN1286	Oscillator	1											
TN1368	Comm. Mod. Processor		1					1	1				
TN1369	Memory		1					1					
TN1800	Comm. Mod. Processor		1										
UN25B	I/O Microprocessor Interface					2	4						

SN516	Power Control and Display	1	
TN1368	Comm. Mod. Processor	1	
TN1369	Processor Memory	1	
TN1800	Comm. Mod. Processor	1	
TN1681	Quad-Link Interface 2	1	
TN1682	Quad-Link Packet Switch	1	
TN1683/4	Quad-Link Gateway Processor Bd	1	

Table 5-14 CM E Bus Unit Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
UN197	Multiplexer and Controller	1	
UN198	Loop Around	4	
UN310	End Data	3	
UN311	Transmit Data	3	
UN312	End Clock	1	
UN313	Transmit Clock	1	

Table 5-15 CM Message Interface Clock Unit J5D006ED-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495KA	+12V, +5V, Power Converter	1	
TN245	Sync./Standalone	1	
TN834	Link Interface	1	
TN835	Link Interface	1	
TN859	Message Interface	1	
TN860	Message Interface	1	
TN861	Message Interface	1	
TN862	Message Interface	1	
TN1130	Digital Phase Lock Loop	1	
TN1131	Controller	1	

Table 5-16 CM Message Switch Control Unit J5D006AB-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
SN412	Power Control and Display	1	
SN516	Power Control and Display	1	
TN61B	Peripheral Interface Cont.	1	
TN70B	Bus Interface Controller	1	
TN698	Duplex Dual Serial Bus Sel.	1	
TN848	Microcontrol Store	2	
TN886	Pump Peripheral Controller	1	
UN25B	I/O Microprocessor Interface	2	

Table 5-17 CM Message Switch Control Unit 2 J5D020AB-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
SN412	Power Control and Display	2	
SN516	Power Control and Display	2	
TN69B	Duplex Dual Serial Bus Sel.	1	
TN70C	Bus Interface Cont.	1	
TN856C	Msg. Sw. Periph. Processor	2	
TN886	Pump Periph. Controller	1	
UN25B	I/O Microprocessor Interface	4	
UN173	Foundation Periph. Controller	1	
UN178	Periph. Interface Controller	1	
UN199	Programmable Microcont. Store	1	

Table 5-18 CM Message Switch Control Unit 3 J5D020AH-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
SN516B	Message Switch Peripheral Unit Control & Display	1	
495FB	Message Switch Peripheral Unit Conv	1	
TN856C	Message Switch Peripheral Processor	1	
TN886	Pump Peripheral Controller	1	
UN173	Foundation Peripheral Controller	1	

SN516B	Message Switch Control Unit Control & Display	1	
495FB	Message Switch Control Unit Conv	1	
UN25B	Input/Output Microprocessor Interface	3	
KBN10	IOP2/MSC3	1	

Table 5-19 CM Message Switch Peripheral Unit J5D006AD-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	1	
SN412	Control and Display	1	
TN856	Msg. Switch Periph. Processor	2	
TN886	Pump Periph. Controller	1	
TN1368	Comm. Mod. Processor	1	
TN1369	Message Switch Memory	1	
UN173	Foundation Periph. Cont.	1	

Table 5-20 CM Message Switch Peripheral Unit 2 J5D020AB-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495G1	Power Converter	1	
SN412	Power Control and Display	1	
TN856	Msg. Sw. Periph. Processor	2	
TN858	Module Msg. Processor	8	
TN1368	Comm. Module Processor	1	
UN170	Module Msg. Processor	4	

Table 5-21 CM Message Switch Peripheral Unit 3 J5D020AC-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
SN412	Power Control and Display	2	
SN516C	Power Control and Display	2	
TN856B	Msg. Sw. Periph. Processor	8	
TN870	Msg. Interface Bus Cont.	8	

Table 5-22 CM Time-Multiplexed Control Unit J5D001AA-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
TN252	Msg. Link Interface	1	
TN265	TMS Main Board	1	
TN267	Test Board	1	
TN268	TMS Controller (UP)	1	
TN269	TMS Interface	1	
TN270	Clock Interface	1	

Table 5-23 CM Time-Multiplexed Switch Unit J5D001AB-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	4	
TN242	Fabric Board	8	
TN243	Link Interface	14	
TN244	Shelf Interface	2	
UN74	Fan Out	2	

Table 5-24 CM Time-Multiplexed Switch Unit 2 J5D020AD-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
410AA	-5 V Power Converter	2	
410CA	-2 V Power Converter	1	
KBN1/4	Fabric Board	4	
KBN2	Fabric Controller	2	
SN412	Power Control and Display	1	
SN516	Power Control and Display	1	
TN883	Foundation Link Interface	1	
TN888	Quad Link Interface	8	
UN182	Shelf Utility Board	1	
TN1681	Quad-Link Interface 2	1	

TN1682	Quad-Link Packet Switch	1	
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Table 5-25 CM Time-Multiplexed Switch Unit 3 J5D020AG-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
410AA	-5 V Power Converter	2	
410CA	-2 V Power Converter	1	
495CA	-2 V Power Converter	1	
KBN5	Fabric Board	1	
SN516	Power Control and Display	1	
TN883	Foundation Link Interface	1	
TN888	Quad Link Interface	8	
TN1681	Quad Link Interface 2	8	
TN1682	Quad-Link Packet Switch	4	
UN182	Shelf Utility Board	1	

Table 5-26 Communication Module (CM) Circuit Packs

CP CODE	FUNCTION	UNITS	
		CMU	CMPU
410AA	-5 V Power Converter	1	2
KBN10	MSCU3	1	
SN516B	Power Control and Display	1	2
TN856C	Message Switch Peripheral Processor	3	
TN870	Message Interface Bus Controller	1	
TN886	Pump Peripheral Controller	1	
TN1274B	External Synchronizer	1	
TN1276	Digital Phase Lock Loop	1	
TN1284B	High Stability Oscillator	1	
TN1286B	Medium Stability Oscillator	1	
TN1812	CM2C Clock and Control Interface	1	
TN1813	CM2C TMS Controller Board	1	
TN1830	CM2C SMLI Board	1	
TN1369	CMP Memory Board		2
TN1800	CMP Core Board		2
UN173	Foundation Peripheral Controller	1	
UN187	Message Interface Controller	1	

Table 5-27 Communication Module Unit Circuit Packs J5D020AJ-5

CP CODE	FUNCTION	NO REQ	ALT CP
410AA	-5 V Power Converter	1	
KBN10	MSCU3	1	
SN516B	Power Control and Display	1	
TN856C	Message Switch Peripheral Processor	4	
TN870	Message Interface Bus Controller	2	
TN886	Pump Peripheral Controller	1	
TN1274B	External Synchronizer	1	
TN1276	Digital Phase Lock Loop	1	
TN1284B	High Stability Oscillator	1	TN1286B
TN1286B	Medium Stability Oscillator	1	TN1284B
TN1812	CM2C Clock and Control Interface	1	
TN1813	CM2C TMS Controller Board	1	
TN1830	CM2C SMLI Board	1	
UN173	Foundation Peripheral Controller	1	
UN187	Message Interface Controller	1	

Table 5-28 Digital Network Unit - SONET Circuit Packs J5D003FR-1

CP CODE	FUNCTION	MAX	NO REQ
KLU2	Common Controller	2	2
KLU3	Common Data	4	2
KTU1	Transmission Multiplexer	14	1
KTU3	STXS-1 Facility Interface	4	2
9822DY	STXS-1 Line Interface	12	0
BKD2	Peripheral Link Interface	24	2
982TN	Common Optical Termination	24	2

Table 5-29 Switching Module (SM) Circuit Packs

CP	FUNCTION	UNITS ^a																		
		A	I	B	S	D	D	G	L	L	D	D	D	L	L	M	M	M	M	P
		T	S	D	D	L	L	D	D	D	S	S	C	U	E	C	C	C	M	S
		U	L	C	C	T	T	S	S	S	U	U	T	3	U	T	T	T	S	U
		U	C	L	L	U	U	U	U	U	2	2	U			U	U	U	U	
		S	U	U	U	2		((2	3			
		U		2	2))											
295FB	Power (-5V)												1							
299FB	Power (-5V)												1							
410AA	Power Converter															2				
414AA	Power Converter																2			
429AA	Pwr. Cont./Displ. & Pwr. Conv.																			2
494GB	Power Unit	2											2	2						
494LA	Power Converter			2														2		
494NA	Power (-12V)												2							
495D	Power (-150V)												2							
495FB	Power Converter							2	2	2					2					
495JC	Power Unit		2																	
ANN3B	Digital Fac. Intfc.					1														
						0														
ANN4B	SLC [®] Carr. Digl. Fac. Intfc.			2	1															
				0	0															
ANN5B	Digital Fac. Intfc.					1														
						0														
KBN6	Periph. Trmsn. Intfc.																			2
KBN7	Elect. Line Intfc.																			2
KBN17	w/32MB for 5EE8 bas. & stan. SMs																			
KBN18	w/64MB for 5EE8, loaded SMs																			
KBN19	w/96MB opt. for 5EE8 & later																			
KBN20	w/32MB for 5E10 bas. & stan. SMs																			
KBN21	w/64MB for 5E10, loaded SMs																			
KBN22	w/96MB opt. for 5E10 & later																			
SN100	Test Access Circuit	2																		
SN101B	Control Data Intfc.	2																		
SN215	Equalizer			1	1	1														
SN216	Equalizer			1	1	1														
SN217	Equalizer			1	1	1														
SN218	Equalizer			1	1	1														
SN219	Equalizer			1	1	1														
SN248B	Port Circuit												4							
SN346B	Power			2	1	1	1													
SN422	Controller												1							
SN423	Eqpt. Access												3							

KLU1	TSIS (Release 1)	1-4	
KLU1	TSIS (Release 2)	1-10	
BKD1*	NLI (Release 1)	2-8	
BKD1*	NLI (Release 2)	2-20	
BKD2*	PLI (Release 2)	0-20	
BKD3*	ENLI (Release 2)	0-6	
410AA	Power		2
SN516B	C/D		1
UN540	Core 40		1
UN560	Core 60 (Release 2)		1
TN1685	Memory (Release 2)		1
KBN8	BSN		1
UN538	Message Handler		2-4
UN539	APC		1
TN1042	PI		1
UN395	PI2 (Release 2)		1
UN71B	CI		1
UN363	DSC3		2
UN1841	SAS DSC (DSU2)		1
UN1842	SAS Memory Board (DSU2)		1

Notes:

a. Legend for Acronyms

* Optional

APC Application Control Board

BSN Bus Service Node Board

C/D Control and Display

CI Control Interface

DSC3 Digital Service Circuit - Model 3

DSU Digital Service Unit

DX Data Expansion Board

ENLI Electrical Network Line Interface

NLI Network Link Interface

PI Packet Interface

PLI Peripheral Link Interface

SMPU Switching Module Processor Unit

TSICOM Time Slot Interchange Common

TSIS Time Slot Interface Slice

TSIU Time Slot Interchange Unit

Table 5-31 SM Analog Trunk Unit J5D003AC-1 Circuit Packs

CP CODE ^a	FUNCTION	NO REQ	ALT CP
494GB	Power Unit	2	
SN100	Test Access Circuit	2	
SN101B	Control Data Interface	2	

Notes:

- a. The following circuit packs can be used in a service group (MAX 8): SN102C, SN103C, SN104, SN105, SN107, SN112, SN113B, SN114, and SN115.

Table 5-32 SM Integrated Digital Carrier Unit J5D003FL-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
KBN6	Periph. Trmsn. Interface	2	
KBN7	Elecl. Line Interface	2	
TN1670	Loop Side Interface	4	
429AA	Power Cont./Displ. & Power Conv.	2	
UN359	Common Control Processor	2	

Table 5-33 SM ISLU Common Shelf Unit J5D004AG-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495JC	Power Unit	2	
TN844E	High-Level Srv. Circuit	6	
TN1346	Common Control Procr.	2	
TN1347B	Ring Generator	2	
TN1348B	Metallic Access Network	4	
TN1384B	Ring Generator	2	
TN1401B	High-Level Srv. Circuit	6	
UN106	Common Control	2	
UN306	Common Control Interface	2	
UN307	Common Data	4	

Table 5-34 SM Basic Digital Carrier Line Unit 2 J5D003AR-2 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
494LA	Power Converter	2	
ANN4B	SLC [®] Carr. Digi. Fac. Interface	20	
SN215	Equalizer	1 a	
SN216	Equalizer	1 a	
SN217	Equalizer	1 a	
SN218	Equalizer	1 a	
SN219	Equalizer	1 a	
SN346B	Power	2	
UN120	Control Multiplexer	2	
UN121	Data Multiplexer	2	

Notes:

a. Determined by engineering requirements.

Table 5-35 SM Supplementary Digital Carrier Line Unit J5D003AS-2 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
ANN4B	SLC [®] Digi. Fac. Interface	10	
SN215	Equalizer	1 a	
SN216	Equalizer	1 a	
SN217	Equalizer	1 a	
SN218	Equalizer	1 a	
SN219	Equalizer	1 a	
SN346B	Power	1	

Notes:

a. Only one equalizer required; determined by engineering requirements.

Table 5-36 SM Digital Line Trunk Unit J5D003AD-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
ANN3C	Digital Fac. Interface	10	
ANN5C	Digital Fac. Interface	10	
SN215	Equalizer	1 a	

SN216	Equalizer	1 a	
SN217	Equalizer	1 a	
SN218	Equalizer	1 a	
SN219	Equalizer	1 a	
SN346B	Power	1	
Notes:			
a. Only one equalizer required; determined by engineering requirements.			

Table 5-37 SM Digital Line Trunk Unit 2 J5D024AA-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
SN346B	Power	1	
TN1611B	Digital Fac. Interface	10	
TN1612B	Digital Fac. Interface	10	

Table 5-38 SM Global Digital Service Unit J5D003AE-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
TN128	Digl. Srv. Unit (Common)	2	
TN234	Universal Conference	2	
TN302	TTF Common	1	
TN303	TTF Tone Generator Board	1	
TN304B	TTF Measurement Board	3	
TN305	TTF Common	1	
TN841	Universal Conference	2	
TN1032	Universal Conference	2	

Table 5-39 SM Local Digital Service Unit J5D003AE-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
TN128	Digl. Srv. Unit (Common)	2	
TN132	Univ. Tone Generator	2	
TN133	Univ. Tone Decoder	14	

Table 5-40 SM Local Digital Service Unit (Modified) J5D003AE-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
TN1637	Digital Service Circuit	2	

Table 5-41 SM Digital Service Unit 2 J5D003EA-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
TN833	Local Digl. Srv. Unit	2	

Table 5-42 SM Digital Service Unit 2 (Peripheral) J5D003EA-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
TN833	Local Digl. Srv. Unit	4	
TN1053	Recorded Ancmt. Function	4	
TN1054	Recorded Ancmt. Function	8	

Table 5-43 SM Directly Connected Test Unit J1P023AM-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
295FB	-5V Power	1	
299FB	-5V Power	1	
494NA	-12V Power	2	
495D	-150V Power	2	
SN248B	Port Circuit	4	
SN422	Controller	1	
SN423	Eqpt. Access Network	3	
TN629B	PICB Interface	1	

Table 5-44 SM Line Unit 2 J5D004AC-2 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
494GB	Power Unit	2	
TN335E	Channels	8	
TN831B	Gated Diode XPoint	2	
TN832B	Gated Diode XPoint	2	
TN838	Half Grid	16	
TN842B	Common Data	2	
TN843	Common Control	2	
TN844E	High-Level Srv. Circuit	6	
TN1048	Half Grid	16	
TN1058C	Half Grid	16	

Table 5-45 SM Line Unit 3 J5D004AD-2 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
494GB	Power Unit	2	
TN335E	Channels	8	
TN831B	Gated Diode XPoint	2	
TN832B	Gated Diode XPoint	2	
TN838	Half Grid	20	
TN844E	High-Level Srv. Circuit	6	
TN1048	Half Grid	20	
TN1058C	Half Grid	20	
TN1561	Half Grid	20	
UN322	Common Data & Control	2	

Table 5-46 SM Memory Expansion Unit J5D003BH-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FB	Power Converter	2	
TN56	Memory	14	
TN2012	Memory	6	

Table 5-47 SM Module Controller/Time Slot Interchanger J5D003EC-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
410AA	Power Converter	2	
SN516	Control and Display	2	
TN56	Memory	10	
TN871B	Module Processor	2	
TN872	Module Processor	2	
TN873	Module Processor	2	
TN874B	Module Processor	2	
TN875C	Module Processor	2	
TN876	Data Interface	4	
TN878	Bootstrapper	1	
TN1077B	Dual Link Interface	2	
TN1086B	Time Slot Intfc. Sig. Procr.	2	
TN1397	Module Processor	2	
TN1407(B)	Module Processor	2	
TN1423	Module Processor	2	
TN1527	Module Processor	2	
TN1533	Module Processor	2	
TN2012	Memory	10	
UN71B	Control Interface	4	

Table 5-48 SM Module Controller/Time Slot Interchanger 2 J5D003LA-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
414AA	Power Converter	2	
TN833	Local Digl. Srv. Unit	4	
TN1042B	Packet Interface	2	
TN1077E	Dual Link Interface	2	
TN1086B	TS Intfc. Sig. Procr.	2	
TN1374	Memory	12	
TN1376	Memory	12	TN1661

TN1377	Data Interface	4	
TN1524	Data Interface	4	
UN71B	Control Interface	4	
UN515B	Processor Core	2	
UN516B	Core Support	2	UN520
UN517B	Core Support	2	
UN518	Application	2	

Table 5-49 SM Modular Metallic Service Unit J5D003BD-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
494LA	Power Pack	2	
TN138	Metallic Access Pack	8	
TN220B	Scan	2	
TN221	Signal Distributor	2	
TN328B	Auto. Line Insn. Test Pack	2 a	
TN329	Auto. Line Insn. Test Pack	2 a	
TN330	Auto. Line Insn. Test Pack	2 a	
TN879B	Common Pack	1	
TN880	GDX Compensator Pack	2 a	
TN1040	Distn. Frame Test Acc. Ckt.	2	
TN1422	Subscriber Line Insn. Measurement Board	1 a b	

Notes:
a. Optional
b. Additional boards are permitted

Table 5-50 SM Packet Switch Unit J5D003BL-1 Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
TN1081B	Protocol Handler	1-16	
TN1082B	Control Fanout	2	
TN1083C	Packet Fanout	2	
TN1366B	Protocol Handler 2	1-16	
TN1367	Protocol Handler 3	1-16	
UN192B	Data Fanout	2	

Table 5-51 Common Network Interface (CNI) Circuit Packs

CP CODE	FUNCTION	UNITS ^a		
		DLN	RPCN	LN
495FA	Power Unit	1	1	1
TN69B	Duplex Dual Serial Bus Selector	1	1	
TN914	3B20D Computer Interface	1	1	
TN915	Padded Interface Buffer		1	1
TN916	Link Interface (Non-Encrypted)			1
TN917	Link Interface (Encrypted)			1
TN918	Interframe Buffer (Not always present)	1	1	1
TN922	Node Processor	1	1	1
TN1340	Attached Processor	1		
UN122C	Ring Interface 0	1	1	1
UN123B	Ring Interface 1	1	1	1

Notes:
a. Legend For Acronyms
DLN Direct Link Node
RPCN Ring Peripheral Controller Node
LN Link Node

Table 5-52 CNI Direct Link Node Unit Circuit Packs

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CP CODE	FUNCTION	NO REQ	ALT CP
495FA	Power Unit	1	
TN69B	Duplex Dual Serial Bus Selector	1	
TN914	3B20D Computer Interface	1	
TN918	Interframe Buffer	1	
TN922	Node Processor	1	
TN1340	Attached Processor	1	
UN122C	Ring Interface 0	1	
UN123B	Ring Interface 1	1	

Table 5-53 CNI Ring Peripheral Controller Node Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FA	Power Unit	1	
TN69B	Duplex Dual Serial Bus Selector	1	
TN914	3B20D Computer Interface	1	
TN915	Padded Interface Buffer	1	
	(Not Always Present)		
TN918	Interframe Buffer (Not Always Present)	1	
TN922	Node Processor	1	
UN122C	Ring Interface 0	1	
UN123B	Ring Interface 1	1	

Table 5-54 CNI Link Node Unit Circuit Packs

CP CODE	FUNCTION	NO REQ	ALT CP
495FA	Power Unit	1	
TN915	Padded Interface Buffer	1	
TN916	Link Interface	1	
TN917	Link Interface	1	
TN918	Interframe Buffer	1	
TN922	Node Processor	1	
UN122C	Ring Interface 0	1	
UN123B	Ring Interface 1	1	

5.1 ADMINISTRATIVE MODULE

5.1.1 3B20D COMPUTER - J1C176C-1

The Administrative Module (AM) consists of an Lucent 3B20D - Model 3 processor, a tape disk cabinet and associated devices (terminals and printers) to control input and output. The 3B21D is necessary to support the SM-2000. Each processor cabinet contains the following shelf assemblies:

- Central Processing Unit
- Main Store, Input/Output Processor, Disk File Controller Unit
- Input/Output Processor Basic Unit
- Input/Output Processor Growth Unit
- Power Distribution Unit
- Port Switch (Cabinet 0 only)
- Cooling Unit.

Figure 5.1-1 illustrates the typical AM and units contained in the Processor Cabinet and Tape/Disk Cabinet.

The 3B20D - Model 3 computer (processor) is in a cabinet separated into Bay 0 and Bay 1. All units are duplicated except the port switch.

This processor performs the central processing functions, controls data flow between the disk drives and the high-speed tape and data flow among other dedicated processors throughout the remaining units.

Diagnostic Phase descriptions for the AM are in Table 5.1-1 .

The tape disk cabinet contains a tape drive and disk units as required for recording, storing and reading data. Self-diagnostics are run on the tape transport and the fault recovery codes may be displayed as described in Table 5.1-2 .

A typical small computer system interface (SCSI) can be used with the AM and is described in this section.

Figure 5.1-2 illustrates a typical AM (3B20D) including the SCSI configuration. Refer to Table 5.1-3 for SCSI controller unit information and bus assignments.

For diagnostic execution input message and POKE command source information, refer to the following documents:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-750, *Output Message Manual*.

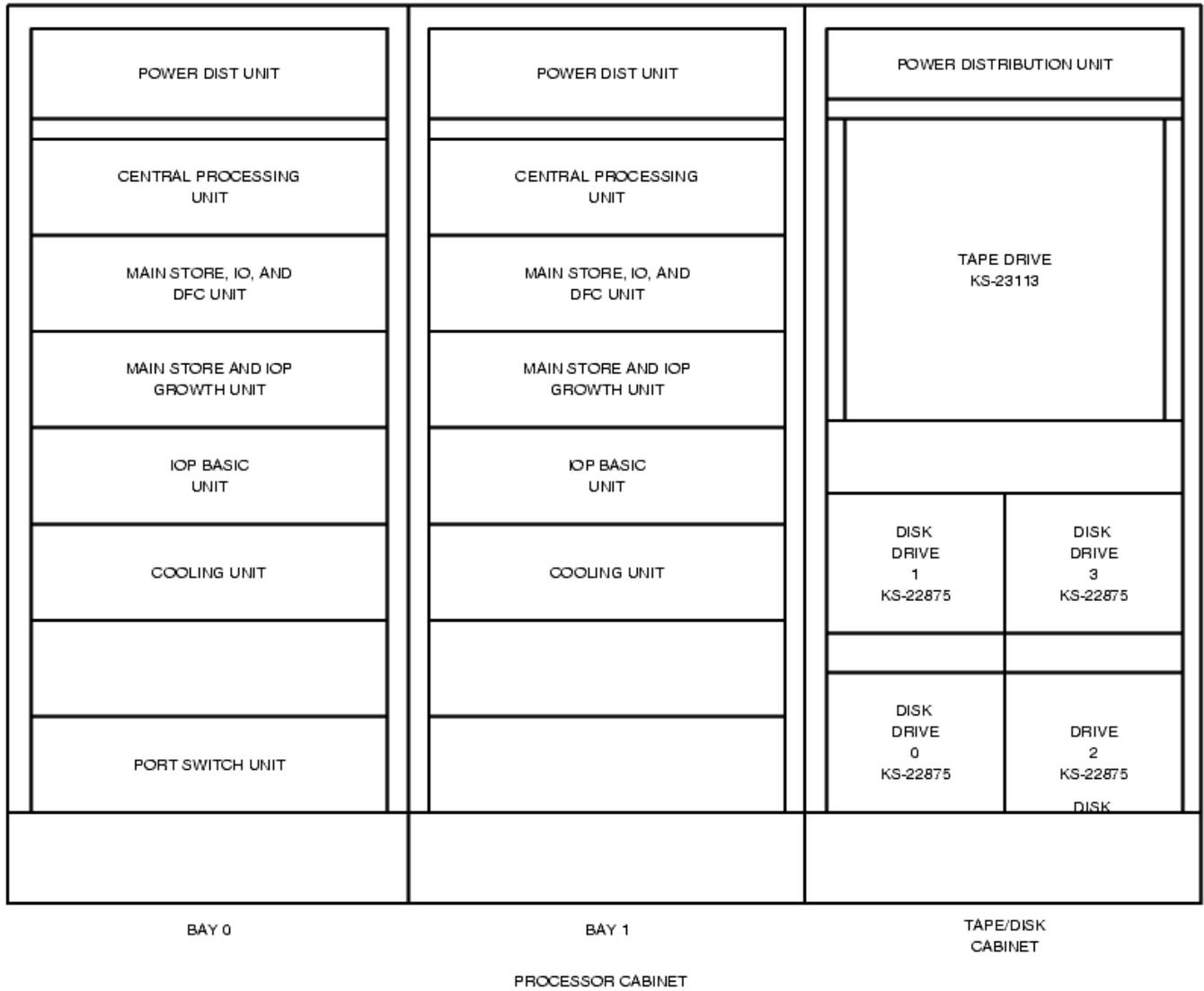


Figure 5.1-1 Administrative Module - 3B20D

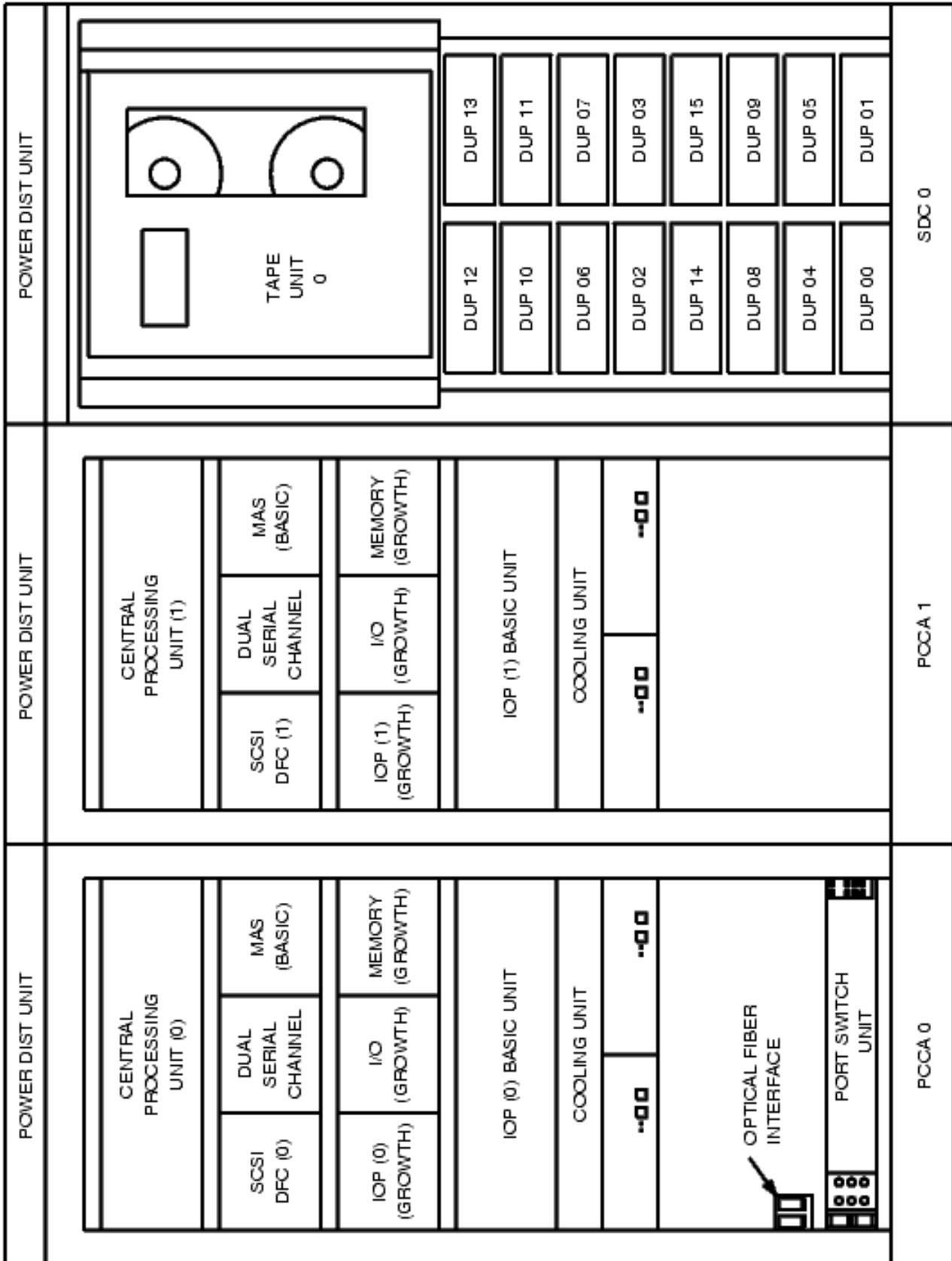


Figure 5.1-2 Administrative Module - 3B20D (Including SCSI)

Table 5.1-1 Administrative Module Diagnostic Phase Descriptions

DIAGNOSTIC ID	PHASE	DESCRIPTION/WHAT IS TESTED	PR NAME
APPLICATION CHANNEL INTERFACE (ACHI)	1	Tests the CC I/O bus interface.	DL:ACHI01
	2	Performs the data register looparound tests.	DL:ACHI02
	3	Performs the miscellaneous function tests.	DL:ACHI03
CONTROL UNIT CENTRAL CONTROL (CUCC)	1	Performs the on-line MCH master tests.	DL:CC01
	2	Performs the MCH slave communication tests.	DL:CC02
	3	Performs the MCH slave command tests.	DL:CC03
	4	Performs the MCH microstore address and data register tests.	DL:CC04
	5	Performs the MC (microcontrol) clock circuit tests, the microinstruction register tests, and the MC parity tests.	DL:CC05
	6	Tests the MC immediate data path, MCH access to test multiplexer, buffered bi-directional gating register parity bits, and path to CC error register.	DL:CC06
	7	Tests the MC address sequencer, verifies basic address path for unconditional branch and no branch.	DL:CC07
	8	Tests the MC address sequencer, conditional jump logic, OPCODE jam path, MC address stack, INT command to MCH, set interrupt set, and interrupt mask registers.	DL:CC08
	9	Performs the address and memory verification of UN28 ROM in CU frame slot 0. (Requires equipage bits in ECD.)	DL:CC09
	10	Performs the microstore address bus parity tests.	DL:CC10
	11	Tests the status registers - hardware status register, program status word, and system status register.	DL:CC11
	12	Tests the pulse point register.	DL:CC12
	13	Tests the gate through data manipulation unit and the byte rotate.	DL:CC13
	14	Tests the data manipulation unit bit rotate.	DL:CC14
	15	Tests the arithmetic logic unit matcher.	DL:CC15
	16	Tests the data manipulation unit Q-register.	DL:CC16
	17	Tests the data manipulation unit XOR, Z-flag, and ONES.	DL:CC17
	18	Tests the data manipulation unit general registers.	DL:CC18
	19	Tests the arithmetic logic unit and gating paths.	DL:CC19
	20	Tests the 24-bit mode.	DL:CC20
	21	Tests the data manipulation unit looparound.	DL:CC21
	22	Tests the temporary registers.	DL:CC22
	26	Performs the MC privileged programmable ROM (PROM) tests.	DL:CC26
	27	Performs the MC privileged PROM tests.	DL:CC27
	28	Performs the MC privileged PROM tests.	DL:CC28
	30	Writable microstore: bidirectional gating bus, microstore data bus, and microstore address bus access. Tests UN48 (4K writable microstore) or UN248 (16K writable microstore) in CU frame slot 1. (Requires equipage bits in ECD.)	DL:CC30
	31	Writable microstore control logic. Tests UN48 (4K writable microstore) or UN248 (16K writable microstore) in CU frame slot 1. (Requires equipage bits in ECD.)	DL:CC31
	32	Tests the writable microstore, bi-directional gating bus, microstore data bus, and microstore address	DL:CC32

	bus access. Tests the UN48 (4K writable microstore) in CU frame slot 1. (Requires equipage bits in ECD.)	
33	Writable microstore: bidirectional gating bus, microstore data bus, and microstore address bus access. Tests UN48 (4K writable microstore) or UN248 (16K writable microstore) in CU frame slot 2. (Requires equipage bits in ECD.)	DL:CC33
34	Writable microstore control logic. Tests UN48 (4K writable microstore) or UN248 (16K writable microstore) in CU frame slot 2. (Requires equipage bits in ECD.)	DL:CC34
35	(Demand, REX, and DEX phase). Tests the writable microstore control logic. Tests the UN48 (4K writable microstore) in CU frame slot 1. (Requires equipage bits in ECD.)	DL:CC35
36	Writable microstore: bidirectional gating bus, microstore data bus, and microstore address bus access. Tests UN48 (4K writable microstore) or UN248 (16K writable microstore) in CU frame slot 3. (Requires equipage bits in ECD.)	DL:CC36
37	Writable microstore control logic. Tests UN48 (4K writable microstore) or UN248 (16K writable microstore) in CU frame slot 3. (Requires equipage bits in ECD.)	DL:CC37
38	(Demand, REX, and DEX phase). Tests the address and memory test of the UN48 (4K writable microstore) in CU frame slot 1. (Requires equipage bits in ECD.)	DL:CC38
39	Tests the data manipulation unit parity.	DL:CC39
40	Tests the store control register/store control field of microinstruction register to store control register.	DL:CC40
41	Tests the store data register, store instruction register, and instruction buffer.	DL:CC41
42	Tests the store address register and program address register.	DL:CC42
43	Tests the instruction buffer parity circuit.	DL:CC43
44	Tests the address increment and parity predict.	DL:CC44
45	Tests the address increment (store address register only).	DL:CC45
46	Tests the store instruction register path to halfword multiplexer to instruction buffer.	DL:CC46
47	Tests the store instruction register path to halfword multiplexer to instruction buffer.	DL:CC47
48	Tests the store instruction register path to halfword multiplexer to instruction buffer.	DL:CC48
49	Tests the store instruction register path to halfword multiplexer to instruction buffer.	DL:CC49
52	Tests the A and B select and rotate amount multiplexer.	DL:CC52
53	Tests the mask ROM.	DL:CC53
54	Tests the find low zero.	DL:CC54
55	Tests the interrupt registers and logic.	DL:CC55
56	Tests the timers (includes CL-PT MCH command check).	DL:CC56
57	Tests the channel data register.	DL:CC57
58	Tests the CC I/O bus sanity.	DL:CC58
59	(Demand phase only). Tests the CC interrupt logic circuits connected to units other than the	DL:CC59 ^a

	<p>60 CC. Tests the error response logic. 61 Tests the emergency action interface. The following three PRMs should be displayed: PRM_z 0123 4567 89AB CDEF xx xx xx PRM_z 0000 0000 0000 0000 xx xx xx PRM_z FFFF FFFF FFFF FFFF xx xx xx</p> <p>62 Performs the off-line MCH master side tests. 70 Performs the address and memory verification of the UN28 (ROM) in CU frame slot 2. (Requires equipage bits in ECD.) 71 Performs the address and memory verification of the UN28 (ROM) in CU frame slot 2. (Requires equipage bits in ECD.) 93 (Demand and DEX phase). This phase tests the EAI lamp display (located next to the power switch on the CU) and the ability of the EAI to transmit PRMs. A series of PRMs appear on the EAI display page on the video terminal located at the MCC and is printed on the ROP (if powered). Then the lamps on the EAI displayed are cycled through the specific pattern for that phase. The following seven PRMs should be displayed: PRM_z 0123 4567 89AB CDEF xx xx xx PRM_z AAAA AAAA AAAA AAAA xx xx xx PRM_z 5555 5555 5555 5555 xx xx xx PRM_z EEEE EEEE EEEE EEEE xx xx xx PRM_z 1111 1111 1111 1111 xx xx xx PRM_z 0000 0000 0000 0000 xx xx xx PRM_z FFFF FFFF FFFF FFFF xx xx xx You should now observe the following pattern: Digits 0 through F are sequenced on the hexadecimal digit display. The sequence starts with 0-F-0 to warn you that this part of the phase is beginning. Next, each light-emitting diode lights and then goes off in a pattern running down the display. Later lamp flash may occur and should be ignored. If you do not observe these patterns, the test failed. A lamp display failure indicates that the EAI (TN11) is defective. A PRM failure may be due to a defective EAI or a defective MCRT controller (TN83) in the IOP to which the affected MCRT or ROP is connected. ^b</p>	<p>DL:CC60 DL:CC61</p> <p>DL:CC62 DL:CC70</p> <p>DL:CC71</p> <p>CL:CC93</p>	
<p>CONTROL UNIT DUAL SERIAL CHANNEL (CUCH)</p>	<p>1 2 3 8 9 10 11 12 13</p>	<p>Tests the DSCH - I/O bus interface. Performs the data register (FIFO) tests. Performs the DSCH error tests. Tests the port 0 selection, interrupts, and service requests. Tests the port 1 selection, interrupts, and service requests. Tests the port 2 selection, interrupts, and service requests. Tests the port 3 selection, interrupts, and service requests. Tests the port 4 selection, interrupts, and service requests. Will complete CATP when a CNI ring with DLNs is equipped on this channel. Tests the port 5 selection, interrupts, and service</p>	<p>DL:DSCH01 DL:DSCH02 DL:DSCH03 DL:DSCH08 DL:DSCH09 DL:DSCH10 DL:DSCH11 DL:DSCH12 DL:DSCH13</p>

	requests.	
14	Tests the port 6 selection, interrupts, and service requests.	DL:DSCH14
15	Tests the port 7 selection, interrupts, and service requests.	DL:DSCH15
16	Tests the port 8 selection, interrupts, and service requests.	DL:DSCH16
17	Tests the port 9 selection, interrupts, and service requests.	DL:DSCH17
18	Tests the port 10 selection, interrupts, and service requests.	DL:DSCH18
19	Tests the port 11 selection, interrupts, and service requests.	DL:DSCH19
20	Tests the port 12 selection, interrupts, and service requests.	DL:DSCH20
21	Tests the port 13 selection, interrupts, and service requests.	DL:DSCH21
22	Tests the port 14 selection, interrupts, and service requests.	DL:DSCH22
23	Tests the port 15 selection, interrupts, and service requests.	DL:DSCH23
24	Performs the port 0 DSCH - DBS communication tests.	DL:DSCH24
25	Performs the port 1 DSCH - DBS communication tests.	DL:DSCH25
26	Performs the port 2 DSCH - DBS communication tests.	DL:DSCH26
27	Performs the port 3 DSCH - DBS communication tests.	DL:DSCH27
28	Performs the port 4 DSCH - DBS communication tests.	DL:DSCH28
29	Performs the port 5 DSCH - DBS communication tests.	DL:DSCH29
30	Performs the port 6 DSCH - DBS communication tests.	DL:DSCH30
31	Performs the port 7 DSCH - DBS communication tests.	DL:DSCH31
32	Performs the port 8 DSCH - DBS communication tests.	DL:DSCH32
33	Performs the port 9 DSCH - DBS communication tests.	DL:DSCH33
34	Performs the port 10 DSCH - DBS communication tests.	DL:DSCH34
35	Performs the port 11 DSCH - DBS communication tests.	DL:DSCH35
36	Performs the port 12 DSCH - DBS communication tests.	DL:DSCH36
37	Performs the port 13 DSCH - DBS communication tests.	DL:DSCH37
38	Performs the port 14 DSCH - DBS communication tests.	DL:DSCH38
39	Performs the port 15 DSCH - DBS communication tests.	DL:DSCH39
40	(Demand and DEX phase). This phase tests data communication between the CUCH (in the CU) and the bus interface controller (in a DFC or IOP). Specify the DFC or IOP in the DGN input message as a helper unit; use DFC 0, DFC 1, IOP 0, and IOP 1. The unit must be OOS (out-of-service) when the diagnostic is run.	DL:DSCH40
44	(Demand phase only). This phase tests reading	DL:DSCH44

		the normal bootstrap data from the disk into main store. Either DFC 0 or DFC 1 must be OOS for this phase. Run this phase if it is suspected a particular CU and DFC combination will not boot.	
CONTROL UNIT CACHE STORE UNIT (CUCSU) MODEL 1	1	Performs access to cache memories and kernel/interrupt stack enable tests.	DL:CSU01
	2	Performs cache memory match tests.	DL:CSU02
	3	Tests the hit/miss matchers (ATBA to tags A and B).	DL:CSU03
	4	Tests the hit/miss matchers (ATBB to tags A and B).	DL:CSU04
	5	Tests the hit/miss matchers (ATBA to tags C and D).	DL:CSU05
	6	Tests the hit/miss matchers (ATBB to tags C and D).	DL:CSU06
	7	Tests the select enable logic.	DL:CSU07
	8	Tests the write tag control logic (tags A and B).	DL:CSU08
	9	Tests the write tag control logic (tags C and D).	DL:CSU09
	10	Tests the SAT interface (ATBA to tags A and C).	DL:CSU10
	11	Tests the SAT interface (ATBB to tags A and C).	DL:CSU11
	12	Tests the tag parity generators.	DL:CSU12
	13	Tests the tag parity checkers.	DL:CSU13
	14	Tests the hit and miss counters.	DL:CSU14
	15	Model 1	DL:CSU15
		Tests the cache store write control logic.	
16	Tests the cache store write control logic.	DL:CSU16	
17	Tests the error check circuits on the cache memory board.	DL:CSU17	
18	(Demand, REX, and DEX phase). This phase exercises the mechanism that writes values from the off-line main store to the cache. This test can be run whenever the CUCC, CUSAT, CUCSU, and CUMASC tests pass, but trouble is suspected in those areas. This phase should be run with the RAW option.	DL:CSU18	
		During this phase, a selection of memory addresses are accessed using various modes. Upon completion of tests, the contents of main memory, ATBs (address translation buffers), and cache are compared. If no differences are found, the test continues. Differences are reported as errors. If no errors are found, this phase runs for 40 seconds.	
	90	(Demand phase). This phase is the same as phase 18, except that it runs for 40 minutes if no fault is found. This phase can be run whenever an intermittent or data-dependent fault is suspected. Always run this phase with the RAW option.	DL:CSU90
CONTROL UNIT CACHE STORE UNIT (CUCSU) MODEL 2 & 3	1	Access to cache memories and interrupt stack enable tests.	DL:CSU01
	2	Cache tag and cache store memory match tests.	DL:CSU02
	3	Hit/miss matchers (ATBA to tags A and B).	DL:CSU03
	4	Hit/miss matchers (ATBB to tags A and B).	DL:CSU04
	5	Hit/miss matchers (ATBA to tags C and D).	DL:CSU05
	6	Hit/miss matchers (ATBB to tags C and D).	DL:CSU06
	7	Hit/miss matchers (ATBA to tags E and F).	DL:CSU07
	8	Hit/miss matchers (ATBB to tags E and F).	DL:CSU08
	9	Hit/miss matchers (ATBA to tags G and H).	DL:CSU09
	10	Hit/miss matchers (ATBB to tags G and H).	DL:CSU10
	11	Select enable logic.	DL:CSU11

	12	Cache tag memory write control logic (tags A and B).	DL:CSU12
	13	Cache tag memory write control logic (tags C and D).	DL:CSU13
	14	Cache tag memory write control logic (tags E and F).	DL:CSU14
	15	Cache tag memory write control logic (tags G and H).	DL:CSU15
	16	ATBA relocation address to tag memory mod A and E.	DL:CSU16
	17	ATBA relocation address to tag memory mod B and F.	DL:CSU17
	18	ATBA relocation address to tag memory mod C and G.	DL:CSU18
	19	ATBA relocation address to tag memory mod D and H.	DL:CSU19
	20	Address and data parity generators.	DL:CSU20
	21	Address and data parity checkers (tags A, B, C, and D).	DL:CSU21
	22	Address and data parity checkers (tags E, F, G, and H).	DL:CSU22
	23	Models 2&3	DL:CSU23
	24	Cache store write control logic - stack write and write update operations (all tags: A, B, C, D, E, F, G, and H). Cache store write control logic - normal read stack read and test cache mods updated at store complete time (all tags: A, B, C, D, E, F, G, and H).	DL:CSU24
	25	Error check circuits on cache memory board.	DL:CSU25
	26	(Demand, REX, and DEX phase). Cache exercise test (40 seconds). Run when CC, SAT, cache, and main store tests pass but a trouble is still suspected in one of these areas. A selection of memory address is accessed using various modes. Then the contents of main memory ATBs, and cache are compared. If no differences are found, the test continues. Differences are reported as errors. If no errors are found, this phase runs for 40 seconds. Always run this phase with the RAW option.	DL:CSU26
	90	(Demand phase). Cache exercise test (40 minutes). Run when an intermittent or data dependent fault is suspected. Same as phase 26 except runs more extensive and longer tests. <u>Always run this phase with the RAW option.</u>	DL:CSU90
CONTROL UNIT DIRECT MEMORY ACCESS (CUDMA)	1	Tests the DMA CC I/O bus interface.	DL:DMA01
	2	Performs the status tests.	DL:DMA02
	3	Performs the RAM/register tests.	DL:DMA03
	4	Performs the sequencer tests.	DL:DMA04
	5	Tests the request priority circuit.	DL:DMA05
	6	Performs the store address tests.	DL:DMA06
	7	Performs the store data tests.	DL:DMA07
	8	Performs the DMA error tests.	DL:DMA08
	9	Performs the DMA/Cache interface tests (CAC0).	DL:DMA09
	10	Performs the DMA/Cache interface tests (CAC1).	DL:DMA10
	11	Tests MASU priority and arbitration functions.	DL:DMA11
CONTROL UNIT MAIN STORE CONTROLLER	1	Tests the inactive state of errors B/C and basic MASC response.	DL:MASC01

(CUMASC)	2	Tests the address looparound.	DL:MASC02
	4	Performs the data communication tests.	DL:MASC04
	5	Tests the parity circuit (data, address, control tests, and halfword and byte decoding).	DL:MASC05
	6	Performs the maintenance commands, microstore time-out, microinterrupt, and store go-error tests.	DL:MASC06
	7	Performs the MASC memory array response tests.	DL:MASC07
	8	Performs the refresh rate tests.	DL:MASC08
	9	Performs the MASC timing chain tests.	DL:MASC09
	10	Performs the special memory operations and array parity tests (main store array 0).	DL:MASC10
	11	Tests the destination and source wait states.	DL:MASC11
	12	Performs single-bit hamming correction tests.	DL:MASC12
	13	Performs the double-bit error (hamming) tests.	DL:MASC13
	14-28	Performs the same as phase 10 (for memory store arrays 1-15).	DL:MASC14 THRU
	29	Tests the address looparound through main store update (duplex mode).	DL:MASC28 DL:MASC29
	30	Tests the data communication tests through main store update (duplex mode).	DL:MASC30
	31	Tests the control lead parity and other store error tests through main store update (duplex mode).	DL:MASC31
	32	Performs the microstore error B/C tests.	DL:MASC32
	33	(Demand and DEX phase). This phase applies memory patterns and access tests to the main memory.	DL:MASC33
	34	(Demand and DEX phase). This phase applies memory patterns and access tests to the main memory.	DL:MASC34
	35	Performs the memory data pattern tests.	DL:MASC35
	36	(Demand and DEX phase). This phase applies memory patterns and access tests to the main memory.	DL:MASC36
	37	Tests the ability to trap a failing address on errors A, C, and D.	DL:MASC37
	38	Tests to ensure that the CC and MASC can fetch and execute instructions.	DL:MASC38
	39	Performs the update mode and refresh data parity check functional tests.	DL:MASC39
40	(Demand and DEX phase). This phase applies memory patterns and access tests to the main memory.	DL:MASC40	
41	(Demand, REX, and DEX phase). Update mode and refresh data parity tests to entire main memory.	DL:MASC41	
42	Tests MASU priority and arbitration functions.	DL:MASC42	
93	(Demand, REX, and DEX phase). Tests main and duplicate refresh address counters.	DL:MASC93	
95	(Demand phase only). This phase applies memory patterns and access tests to the main memory. This phase allows limits to be set at run time.	DL:MASC95	
96	(Demand phase only). Tests update mode and refresh data parity to all main memories. This phase allows limits to be set at run time.	DL:MASC96	
CONTROL UNIT STORE ADDRESS TRANSLATOR (CUSAT)	1	Tests the store control register control flip-flops.	DL:SAT01
	2	Tests the ATB access and parity.	DL:SAT02
	3	Tests the ATB memory.	DL:SAT03
	4	Tests the counter and invalidate circuit.	DL:SAT04
	5	Tests the address multiplexer.	DL:SAT05

CONTROL UNIT UTILITY CIRCUIT (CUUC)	6	Tests the write control circuit.	DL:SAT06
	7	Tests the compare and bit circuit.	DL:SAT07
	8	Tests the protection circuit.	DL:SAT08
	9	Tests the matchers.	DL:SAT09
	10	Tests the main store interface.	DL:SAT10
	1	Tests the bi-directional gating bus - access and enable.	DL:UC01
	2	Performs the access matcher, address leads, and read/write tests.	DL:UC02
	3	Performs the block address matcher, address leads, and read/write tests.	DL:UC03
	4	Performs the address matcher, address leads, and read/write tests.	DL:UC04
	5	Performs the unit identification matcher, address leads, and read/write tests.	DL:UC05
	6	Performs the data matcher, address leads, and read/write tests.	DL:UC06
	7	Performs the event and transfer trace counters and the read/write tests.	DL:UC07
	8	Performs the transfer trace access path unit identification buffers tests.	DL:UC08
	9	Performs the trace memory and read/write tests.	DL:UC09
	10	Performs the trigger function in freeze mode tests.	DL:UC10
	11	Performs the block address matcher adder tests.	DL:UC11
	12	Performs the trigger functions in run mode without match conditions.	DL:UC12
	13	Performs the access matcher run mode tests.	DL:UC13
	14	Performs the data matcher run mode tests.	DL:UC14
	15	Performs the address matcher virtual address leads (store address register), run mode tests.	DL:UC15
16	Performs the address matcher physical address leads cache address A bus - run mode tests.	DL:UC16	
17	Performs the address matcher physical address leads cache address B bus - run mode tests.	DL:UC17	
18	Performs the unit identification matcher and transfer trace run mode tests.	DL:UC18	
19	Performs the trigger functions in run mode with match conditions.	DL:UC19	
20	Performs the transfer trace run mode tests.	DL:UC20	
90	(Demand phase only). Tests the external output of trigger function 0. It also tests the external inputs to trigger functions 1, 2, and 3. To run this phase, clip pin 400 to pin 405 on the backplane at the UC slot.	DL:UC90	
91	(Demand phase only). Tests the external output of trigger function 1. It also tests the external inputs to trigger functions 0, 2, and 3. To run this phase, clip pin 401 to pin 405 on the backplane at the UC slot.	DL:UC91	
92	(Demand phase only). Tests the external output of trigger function 2. It also tests the external inputs to trigger functions 0, 1, and 3. To run this phase, clip pin 402 to pin 405 on the backplane at the UC slot.	DL:UC92	
93	(Demand phase only). Tests the external output of trigger function 3. It also tests the external inputs to trigger functions 0, 1, and 2. To run this phase, clip pin 403 to pin 405 on the backplane at the UC slot.	DL:UC93	
DISK FILE CONTROLLER	1	Tests the DMCH - DDSBS interface.	DL:DFC01

(DFC)	2	Tests the DDSBS - bus interface controller interface and bus interface controller circuitry. Excludes the PIC's interface.	DL:DFC02	
	3	Tests the bus interface controller - peripheral interface controller interface using peripheral interface controller resident firmware.	DL:DFC03	
	4	Tests the bus interface controller - peripheral interface controller communication.	DL:DFC04	
	5	Tests the peripheral interface controller microstore data validity and microstore parity checker.	DL:DFC05	
	6	Tests the peripheral interface controller microsequencer.	DL:DFC06	
	7	Tests the peripheral interface controller register and arithmetic logic unit.	DL:DFC07	
	8	Tests the peripheral interface controller source/destination decoders.	DL:DFC08	
	9	Tests the peripheral interface controller internal registers.	DL:DFC09	
	10	Tests the peripheral interface controller interrupt circuitry.	DL:DFC10	
	11	Tests the peripheral interface controller RAM memory and sequencer.	DL:DFC11	
	12	Tests parallel/serial data interface and MHD control source and destination decoders.	DL:DFC12	
	13	Tests MHD control requester	DL:DFC13	
	15	(Demand phase). Tests the interface with the off-line CU. The off-line CU must be specified as a helper unit, and it must be OOS and ATP.	DL:DFC15	
	DISK FILE CONTROLLER SMALL COMPUTER SYSTEM INTERFACE (DFC-SCSI)	1	DSCH—duplex dual serial bus selector interface.	DL:DFCS01
		2	Duplex dual serial bus selector—BIC interface and BIC circuitry excluding peripheral interface controller interface. No BIC FIFO testing.	DL:DFCS02
3		BIC—peripheral interface controller interface using peripheral interface controller resident firmware.	DL:DFCS03	
4		WE32100 CPU test.	DL:DFCS04	
5		Test ROM by verifying its content.	DL:DFCS05	
6		Test 1 MB SRAM.	DL:DFCS06	
7		Host Adapter register tests.	DL:DFCS07	
8		WE32104 DMAC test.	DL:DFCS08	
9		DUART test.	DL:DFCS09	
10		STC test.	DL:DFCS10	
11		SCSI Protocol Controller's test. Tests both SCSI buses.	DL:DFCS11	
12		Test (validate) only differential type devices attached to buses.	DL:DFCS12	
13		Test ability of SCSI devices to reorganize and acknowledge bus reset.	DL:DFCS13	
14		(Demand and DEX phase). Bit-wise independence test for HA FIFO.	DL:DFCS14	
15		(Demand-only phase). Tests the interface with the nonactive CU. The nonactive CU must be specified as the helper unit, and must be OOS and ATP prior to running this phase.	DL:DFCS15	
90	(Demand phase). Bus loop test. This phase requires that existing cables to the DFC be disconnected and the loop-around cable be connected between the two buses before running the phase.	DL:DFCS90		
DIRECT USER INTERFACE	1	Request isolate, control signal, and control signal	DL:DUIC01	

CONTROLLER (DUIC)		acknowledge from the peripheral interface controller.	
	2	Read/write access of dual access memory.	DL:DUIC02
	3	Dual access memory parity checker.	DL:DUIC03
	4	Microdiagnostic.	DL:DUIC04
	5	(Demand-only phase). Loopback mode. DUICs must be equipped.	DL:DUIC05
	6	(Demand-only phase). Send-frames mode. DUICs must be equipped.	DL:DUIC06
INPUT/OUTPUT PROCESSOR (IOP)	1	Tests the DSCH - DDSBS interfaces.	DL:IOP01
	2	Tests the DDSBS - bus interface controller interface and bus interface controller circuitry. Excludes the peripheral interface controller interface.	DL:IOP02
	3	Tests the bus interface controller - peripheral interface controller interface, using the peripheral interface controller resident firmware.	DL:IOP03
	4	Tests the bus interface controller - peripheral interface controller communications.	DL:IOP04
	5	Tests the peripheral interface controller microstore data validity and microstore parity checker.	DL:IOP05
	6	Tests the peripheral interface controller microsequencer.	DL:IOP06
	7	Tests the peripheral interface controller register and arithmetic logic unit.	DL:IOP07
	8	Tests the peripheral interface controller source/destination decoders.	DL:IOP08
	9	Tests the peripheral interface controller internal registers.	DL:IOP09
	10	Tests the peripheral interface controller interrupt circuitry.	DL:IOP10
	11	Tests the peripheral interface controller RAM memory and sequencer.	DL:IOP11
	12	Tests the I/O microprocessor interface hardware.	DL:IOP12
	13	Tests the I/O microprocessor interface power control circuitry peripheral controller community power converter/monitor.	DL:IOP13
	15	(Demand phase only). Tests the interface with the off-line CU. The off-line CU must be specified as a helper unit and it must be OOS and ATP.	DL:IOP15
	LINK NODE (LN)	1	Tests the Ring Interface 0 (UN122), Ring Interface 1 (UN123), IFB-P (TN915), IFB (TN918), and Ring Bus Cable.
2		Tests the Ring Interface 0 (UN122), Ring Interface 1 (UN123), IFB-P (TN915), IFB (TN918), and Ring Bus Cable.	iun02.1
10		Tests the Node Processor (TN913/TN922), Ring Interface 0 (UN122), and Ring Interface 1 (UN123).	iun10.1
11		Tests the Ring Interface 0 (UN122), Node Processor (TN913/TN922), and Ring Interface 1 (UN123).	iun11.1
12		Tests the Ring Interface 0 (UN122).	iun12.1
13		Tests the Ring Interface 1 (UN123).	iun13.1
20		Tests the Node Processor (TN913/TN922).	iun20.1
23		Tests the Node Processor (TN913/TN922).	iun23.1
24		Tests the Node Processor (TN913/TN922).	iun24.1
26		Tests the Node Processor (TN913/TN922).	iun26.1
27		Tests the Node Processor (TN913/TN922).	iun27.1
40		Tests the Node Processor (TN913/TN922), Link	CBph40.1

	41	Interface (TN916) - not encrypted, and Link Interface (TN917) - encrypted. Tests the Node Processor (TN913/TN922), Link Interface (TN916) - not encrypted, and Link Interface (TN917) - encrypted.	CBph41.1
	47	Tests the Node Processor (TN913/TN922), Link Interface (TN916) - not encrypted, Link Interface (TN917) - encrypted, and TN919 Data Sets and VFL.	CBph47.1
	48	Tests the Node Processor (TN913/TN922), Link Interface (TN916) - not encrypted, Link Interface (TN917) - encrypted, and TN919 Data Sets and VFL.	CBph48.1
MOVING HEAD DISK (MHD)	1	Tests the parallel/serial data interface and the MHD control source and destination decoders.	DL:MHD01
	2	Tests the MHD control register.	DL:MHD02
	3	Tests the parallel/serial data interface.	DL:MHD03
	4	Tests the MHD control, disk select, and driver enable.	DL:MHD04
	5	Tests the MHD clock.	DL:MHD05
	6	Tests the read/write circuitry and error correction circuitry. A fully formatted disk pack must be mounted and spinning on the drive under test.	DL:MHD06
	7	The same applies for phases 7 and 8. Tests the seek, seek error detection, servo offset, and fault detection circuitry of the drive. A fully formatted disk pack must be mounted and spinning on the drive under test. The same applies for phases 6 and 8.	DL:MHD07
	8	Tests the data transfer between CU and the drive. A fully formatted disk pack must be mounted and spinning on the drive under test. The same applies for phases 6 and 7.	DL:MHD08
MOVING HEAD DISK - SMALL COMPUTER SYSTEM INTERFACE (MHD-SCSI)	1	Diagnoses SCSI disk via device self-tests of SCSI device controller buffer and read/write access to the MHD maintenance area.	DL:MHDS01
MAGNET TAPE CONTROLLER (MTC)	1	Tests the request isolate control signal and the control signal acknowledge from the peripheral interface controller.	DL:MTC01
	2	Tests the read/write access of the dual-access memory.	DL:MTC02
	3	Tests the dual-access memory parity checker.	DL:MTC03
	4	Tests the microdiagnostic.	DL:MTC04
	5	(Demand phase only). Tests the tape transport. A fully formatted diagnostic test tape must be mounted on the tape transport under test.	DL:MTC05
MAINTENANCE TELETYPEWRITER CONTROLLER (MTTYC)	1	Tests the request isolate control signal and the control signal acknowledge from the peripheral interface controller.	DL:MTTYC01
	2	Tests the read/write access of the dual-access memory.	DL:MTTYC02
	3	Tests the dual-access memory parity checker.	DL:MTTYC03
	4	Tests the microdiagnostic.	DL:MTTYC04
RING PERIPHERAL CONTROLLER NODE (RPCN)	1	Tests the Ring Interface 0 (UN122), Ring Interface 1 (UN123), IFB-P (TN915), IFB (TN918), and Ring Bus Cable.	rpc01.1
	2	Tests the Ring Interface 0 (UN122), Ring Interface 1 (UN123), IFB-P (TN915), IFB (TN918), and Ring Bus Cable.	rpc02.1

	10	Tests the DDSBS (TN69B), DSCH (UN9), and 3B Interface (TN914).	rpc10.1
	11	Tests the 3B Interface (TN914) and DDSBS (TN69B).	rpc11.1
	12	Tests the 3B Interface (TN914), Node Processor (TN913/TN922), Ring Interface 0 (UN122), and Ring Interface 1 (UN123).	rpc12.1
	13	Tests the Node Processor (TN913/TN922) and 3B Interface (TN914).	rpc13.1
	14	(Demand phase only). Tests the DDSBS (TN69B) and the off-line DSCH (UN09).	rpc14.1
	20	Tests the Node Processor (TN913/TN922).	rpc20.1
	23	Tests the Node Processor (TN913/TN922).	rpc23.1
	24	Tests the Node Processor (TN913/TN922).	rpc24.1
	26	Tests the Node Processor (TN913/TN922).	rpc26.1
	27	Tests the Node Processor (TN913/TN922).	rpc27.1
	30	Tests the Node Processor (TN913/TN922), Ring Interface (UN122), and Ring Interface (UN123).	rpc30.1
	31	Tests the Ring Interface 0 (UN122), Node Processor (TN913/TN922), and Ring Interface 1 (UN123).	rpc31.1
	32	Tests the Ring Interface 0 (UN122).	rpc32.1
	33	Tests the Ring Interface 1 (UN123).	rpc33.1
SCANNER AND SIGNAL DISTRIBUTOR CONTROLLER (SCSDC)	1	Tests the request isolate control signal and the control signal acknowledge from the peripheral interface controller.	DL:SCSDC01
	2	Tests the read/write access of the dual-access memory.	DL:SCSDC02
	3	Tests the dual-access memory parity checker.	DL:SCSDC03
	4	Tests the microdiagnostic.	DL:SCSDC04
SYNCHRONOUS DATA LINK CONTROLLER (SDLC)	1	Tests the request isolate control signal and the control signal acknowledge from the peripheral interface controller.	DL:SDLC01
	2	Tests the read/write access of the dual-access memory.	DL:SDLC02
	3	Tests the dual-access memory parity checker.	DL:SDLC03
	4	Tests the microdiagnostic.	DL:SDLC04
TELETYPE-WRITER CONTROLLER (TTYC)	1	Tests the request isolate control signal and the control signal acknowledge from the PIC.	DL:TTYC01
	2	Tests the read/write access of the dual-access memory.	DL:TTYC02
	3	Tests the dual-access memory parity checker.	DL:TTYC03
	4	Tests the microdiagnostic.	DL:TTYC04
Notes:			
a. Any units that are causing external error signals should be repaired before running phase 59. Also, do not execute these tests unless all CU units have been diagnosed or the CU has been in service since the last time power was restored to the frame.			
b. Since this failure is indicated visually, phase 93 may run ATP in spite of display faults. All forced states on the EAI must be cleared before phase 93 is run. Do this by activating key ``14'' on the EAI page.			

5.1.1.1 Central Control Processor Unit (CPU) - J1C147BA-1

The Central Control Processor Unit (CPU) is a single-shelf unit with high-speed control functions required by the Administrative Module (AM).

All connections between the CPU and the I/O devices occur over the Central Control Input/Output (CCIO) bus, which connects the CPU to one or two Direct Memory Access Controllers (DMACs) and up to two other I/O positions.

The DMACs provide Direct Memory Access (DMA) to the main store, bypassing the CPU. The I/O positions do not use DMA and communicate with the Main Store (MAS) through the CPU using programmed I/O. The I/O can be Application Channel Interfaces (ACHIs) or Dual Serial Channels (DSCHs). Each DMAC can control two DSCHs by way of the Direct Memory Access Input/Output (DIO) bus. Each DSCH can control up to 8 devices.

The devices are dual ported to two dual serial channels by way of the Dual Duplex Serial Bus Selector (DSBS) to give each processor access to all other devices.

The CPU is located at location 60. Figure 5.1-3 illustrates the CPU and the respective circuit packs contained in the unit.

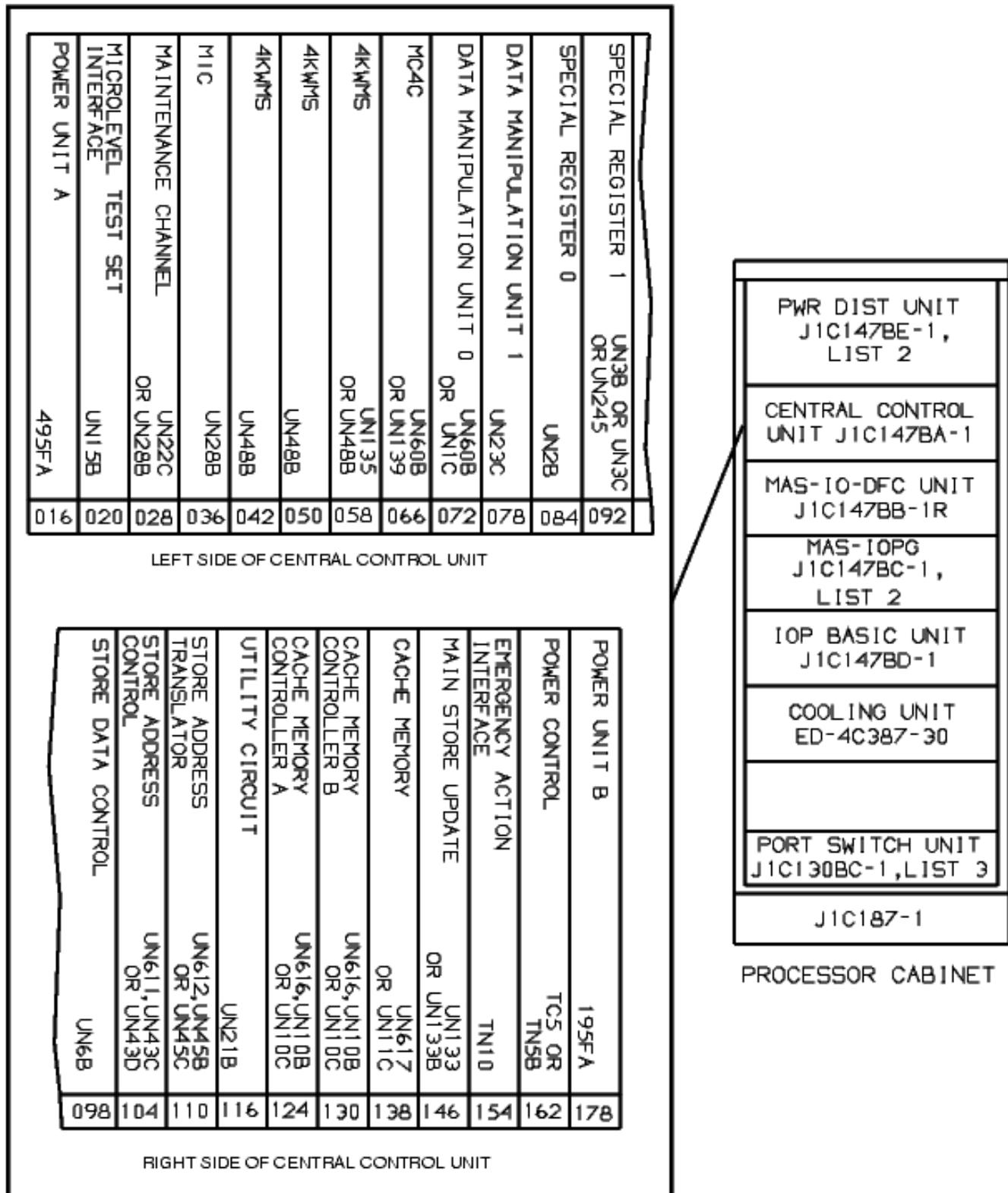


Figure 5.1-3 Central Processor Unit - J1C147BA-1

5.1.1.2 Cooling Unit - ED-4C387-30

Each Administrative Module Processor Control Unit (AMPCU) contains a cooling unit for air circulation for internal equipment (circuit packs, etc.). The cooling unit fans operate on inverted 120 V AC converted from -48 V DC which is supplied directly from the Power Distribution Unit. The input -48 V DC is converted to +5 V DC for alarm circuitry power requirements.

Turning on any of the power control circuit packs in the Processor Control Cabinet (PCC) starts the fans; they stop if all units in the PCC are powered down.

Fuses are fixed assigned to the power distribution unit in the top of the cabinet.

The cooling unit is alarmed by scan and single-distributor points on IOP units 0 and 1. If a single fan fails, a minor alarm is generated; and the failed fan alarm LED lights. The remaining three fans are sufficient to cool the cabinet until failure is corrected. If a multiple fan failure occurs, a major alarm is generated and the failed fan's alarm LEDs light. Fan failures do not automatically shut down the PCC.

Each cooling unit consists of two slide-out drawers, each of which contains two fans, a filter assembly and power and logic circuitry. The front panel of each drawer has two LEDs (one for each fan), an OFF pushbutton switch to power down both fans and an ON/RESET pushbutton switch to turn fans on or reset alarm conditions within the unit.

Figure 5.1-4 illustrates the cooling unit for the 3B20D (shown with a drawer partially opened) with details of the control panel.

Refer to SD-5D007-01 for dedicated coding scan and SD assignments.

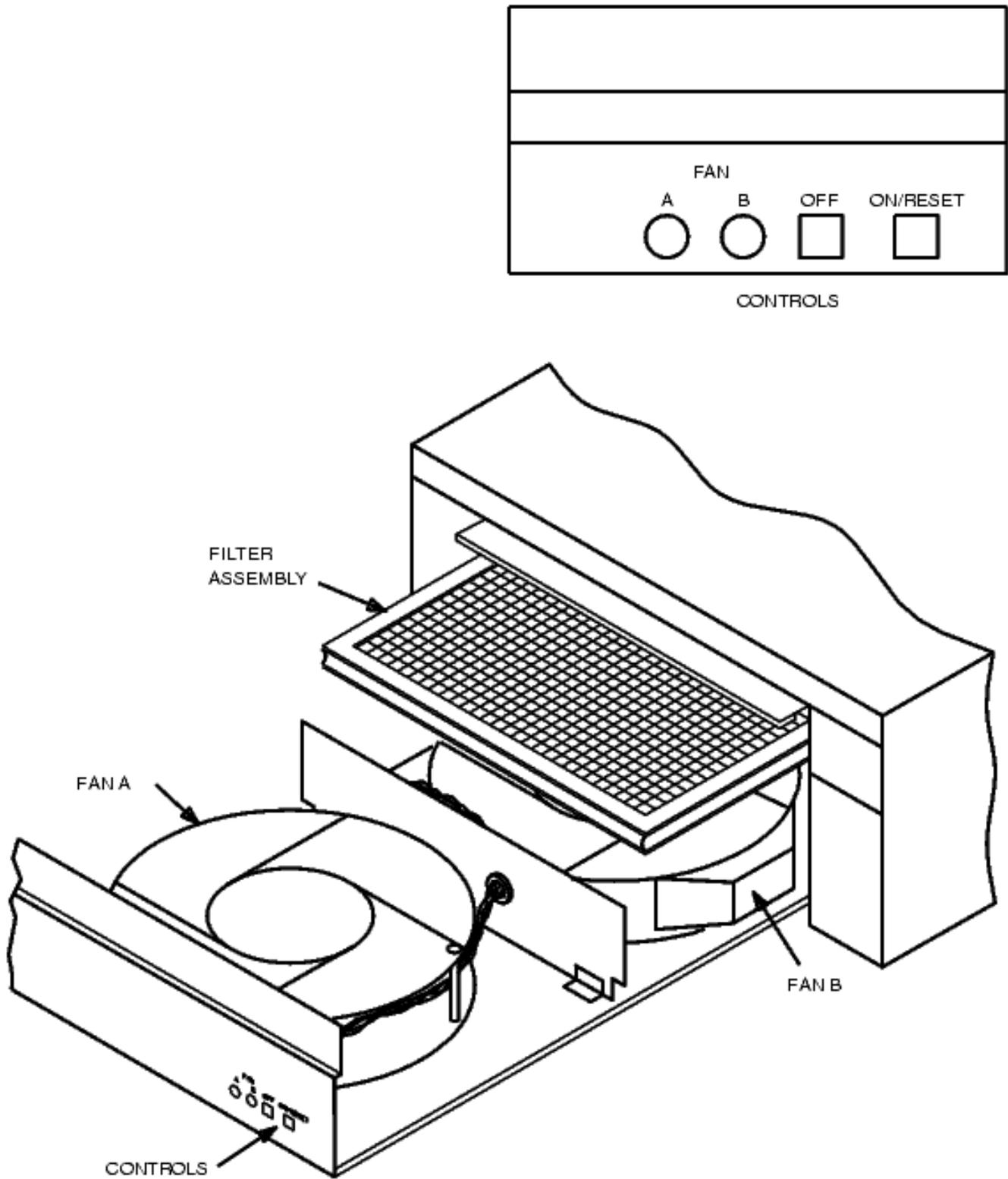


Figure 5.1-4 Cooling Unit - ED-4C387-30

5.1.1.3 Input/Output (Top) Basic Unit - J1C147BD-1

The IOP Basic Unit (IOPBU) is a processor used to control transfers between the Main Store (MAS) and peripheral equipment such as magnetic tape units, terminals and other slow- and medium-speed peripheral units requiring block transfers of data to and from the MAS. Local and remote terminals requiring connection to the exchange must get access through the IOPBU.

The IOPBU consists of a series of control packs (positions 110 - 175) and two communities [Community 0 (positions 072 - 102) and Community 1 (positions 032 - 042)].

The IOPBU can interface with up to four peripheral communities (0 and 1 on IOP Basic and 2 and 3 on IOP Growth units). Each community consists of four slots numbered 0-3.

The IOPBU is a single-shelf unit mounted at Bay 0 location 36. A duplicate is in Bay 1. Figure 5.1-5 illustrates the IOPBU and the respective circuit packs contained in it.

For assignments of IOP Layout, refer to Office Record T-XXXX-DX-3780.

NOTE: The XXXX variable in the "T" drawing number represents a specific number assigned to a local office.

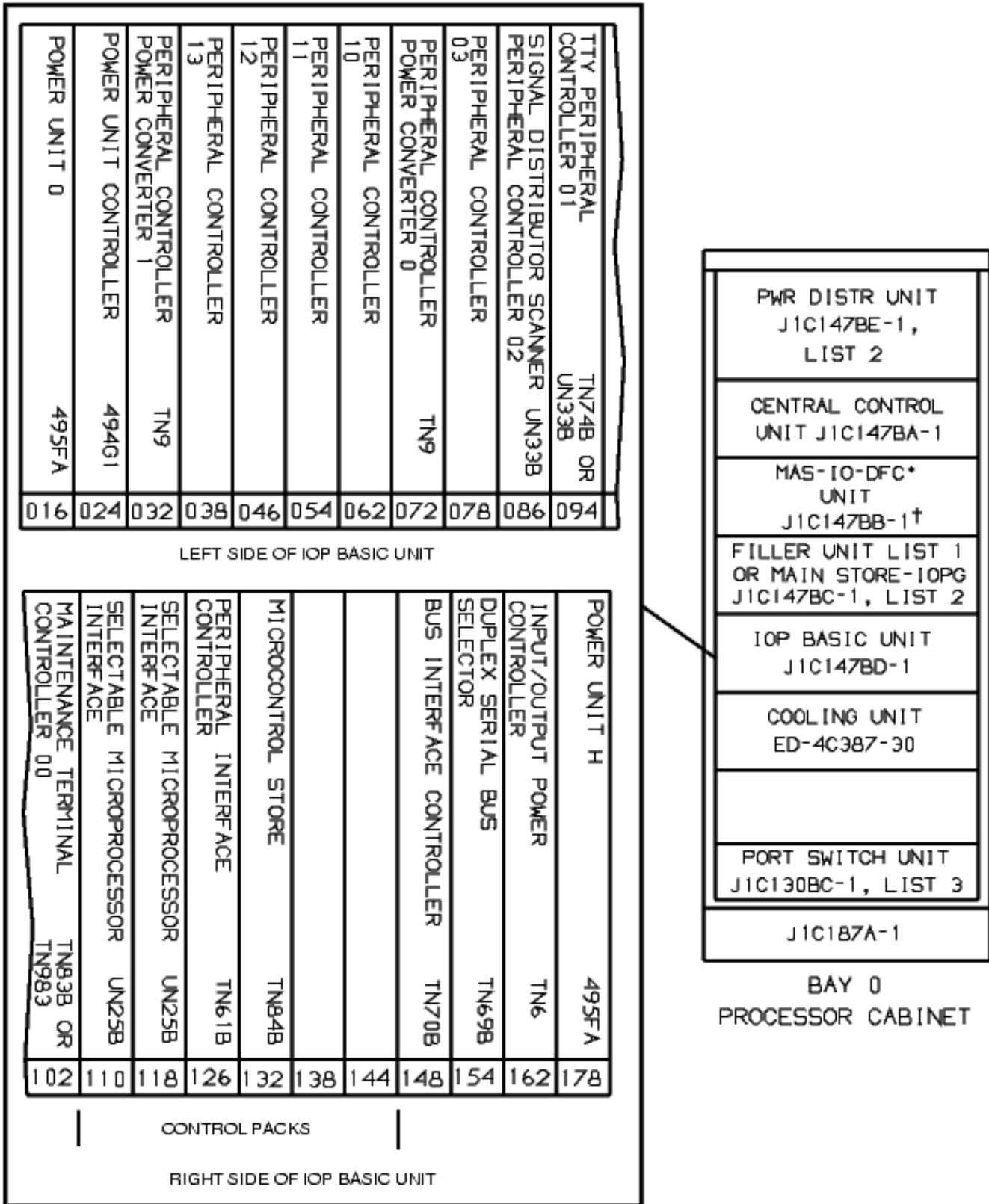


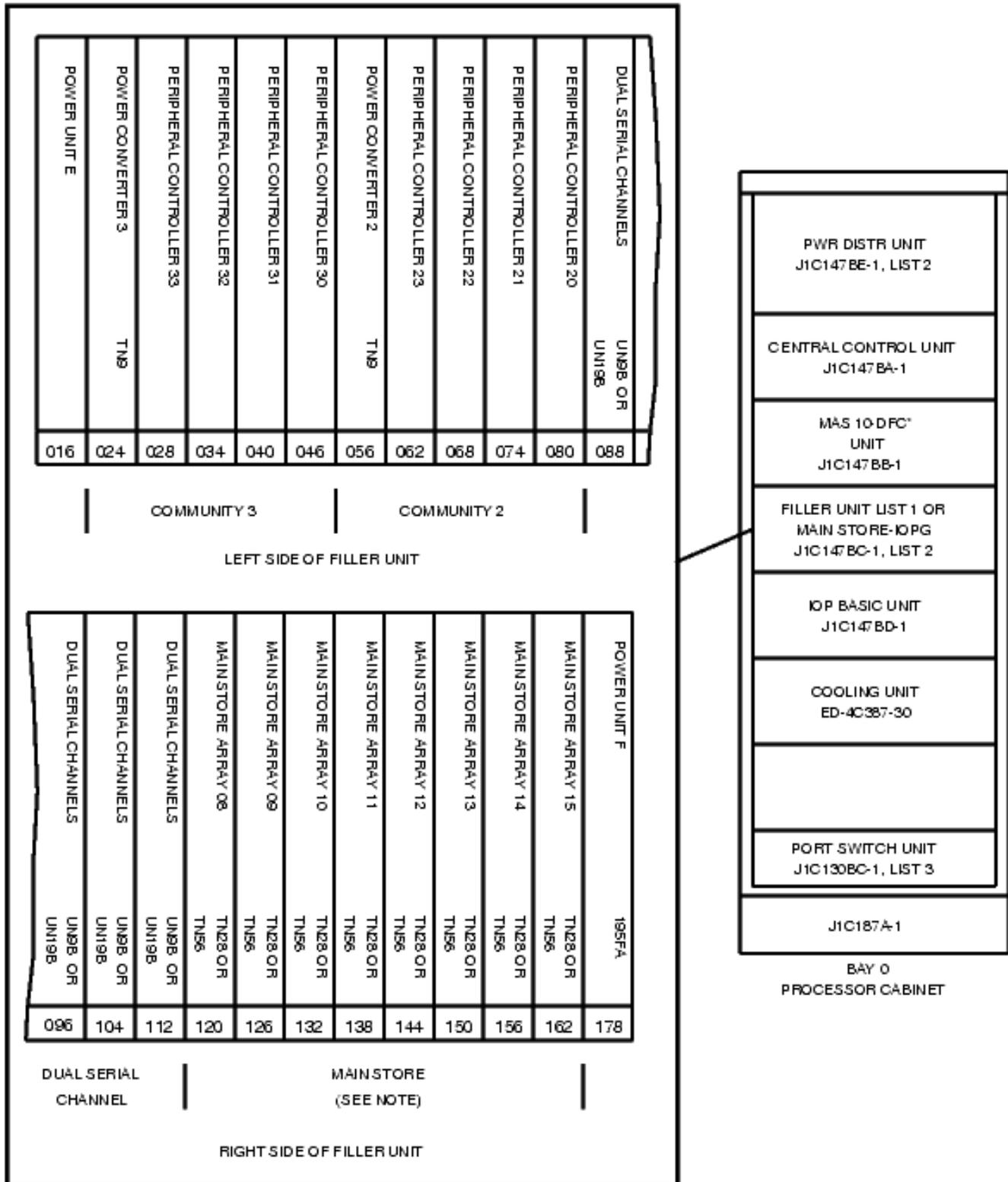
Figure 5.1-5 IOP Basic Unit - J1C147BD-1

5.1.1.4 Main Store Input/Output Growth Unit - J1C147BC-1

The Main Store Input/Output Growth Unit (MASIOPGU) is an optional unit, the need for which is dictated by the required number of addressable memory megabytes on a Main Store (MAS) main unit. The MASIOPGU is a single-shelf unit which mounts in location 42 in Bay 0 of the Administrative Module cabinet. A duplicate unit is mounted in the same location in Bay 1. If a MASIOPGU is not required, a plenum is closes the cabinet space.

The purpose of the unit is to expand the 16-MB capacity of the MAS main unit to a possible 32 megabytes in 2-MB increments. The growth unit has positions for eight additional 2- or 4-MB main store memory array circuit packs; mixing of the two types of memory arrays is not supported.

Figure 5.1-6 illustrates the MASIOPGU and the respective circuit packs contained within it.



NOTE: MAIN STORE IS NOT NORMALLY IN FOR 5E5 SOFTWARE RELEASE

Figure 5.1-6 Main Store, Input/Output, Growth Unit (3B20D) - J1C147BC-1

5.1.1.5 Main Store Input/Output Disk File Controller Unit (3V20D) - J1C147BB-1

The Main Store Input/Output Disk File Controller Unit (MASIOPDFCU) is a single-shelf unit mounted in location 51 in the Administrative Module (3B20D) cabinet, Bay 0. The unit is considered the main unit of the partitioned Main Store (MAS). A duplicate unit is at the same location in Cabinet 1.

The MASIOPDFCU contains the Main Store Controller (MASC) and eight Main Store Arrays (MASAs). The MASC controls access to the Main Store (MAS) and determines multiple store request priorities. It also performs hamming and parity checks.

Each MASA occupies one circuit pack (TN56) and contains two megabytes of addressable memory for a possible total of 16 MB per MAS. The capacity may be increased to 32 megabytes (in 2-MB increments) by the addition of a MAS Growth unit.

Figure 5.1-7 illustrates the MASIOPDFCU unit and its respective circuit packs.

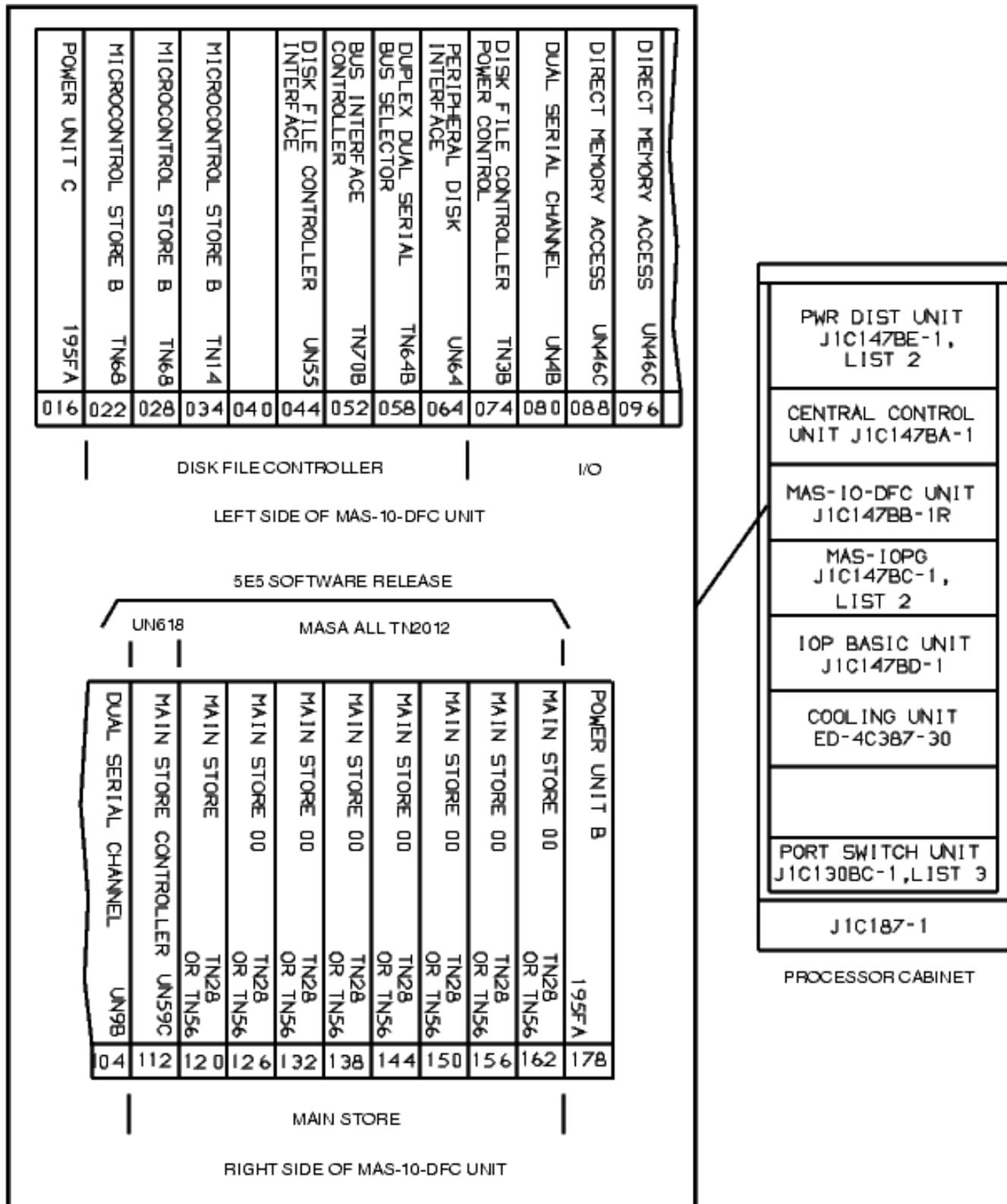


Figure 5.1-7 Main Store Input/Output Disk File Controller Unit (3B20D) - J1C147BB-1

5.1.1.6 Port Switch Unit - J1C130BC-1

The Port Switch Unit (PSU) is a single-shelf unit mounted in location 14 in the Administrative Module (AM) cabinet, Bay 0. A duplicate PSU in Bay 1 is not required.

The PSU is an interface between the Master Control Center (MCC) Teletypewriter (TTY) and printer and the MCC TTY controllers. It ensures that the MCC is always connected to the active controller. The PSU can be used to select states (ACTIVE or STANDBY) of the TTY controllers. Such selection is useful for testing TTY circuitry and it lets TTY devices operate if a TTY controller fails.

The PSU is equipped with two port-switch circuits, one serving the MCC video terminal and the other serving the MCC receive only printer (ROP). Each associated switch has three settings: 0, 1 or AUTO. Position setting 0 or 1 manually forces the MCC terminal to connect to controller 0 or 1 and the AUTO position setting keeps the terminal connected to the controller associated with the active (0 or 1) side.

Figure 5.1-8 illustrates the PSU and the respective circuit packs contained in the unit.

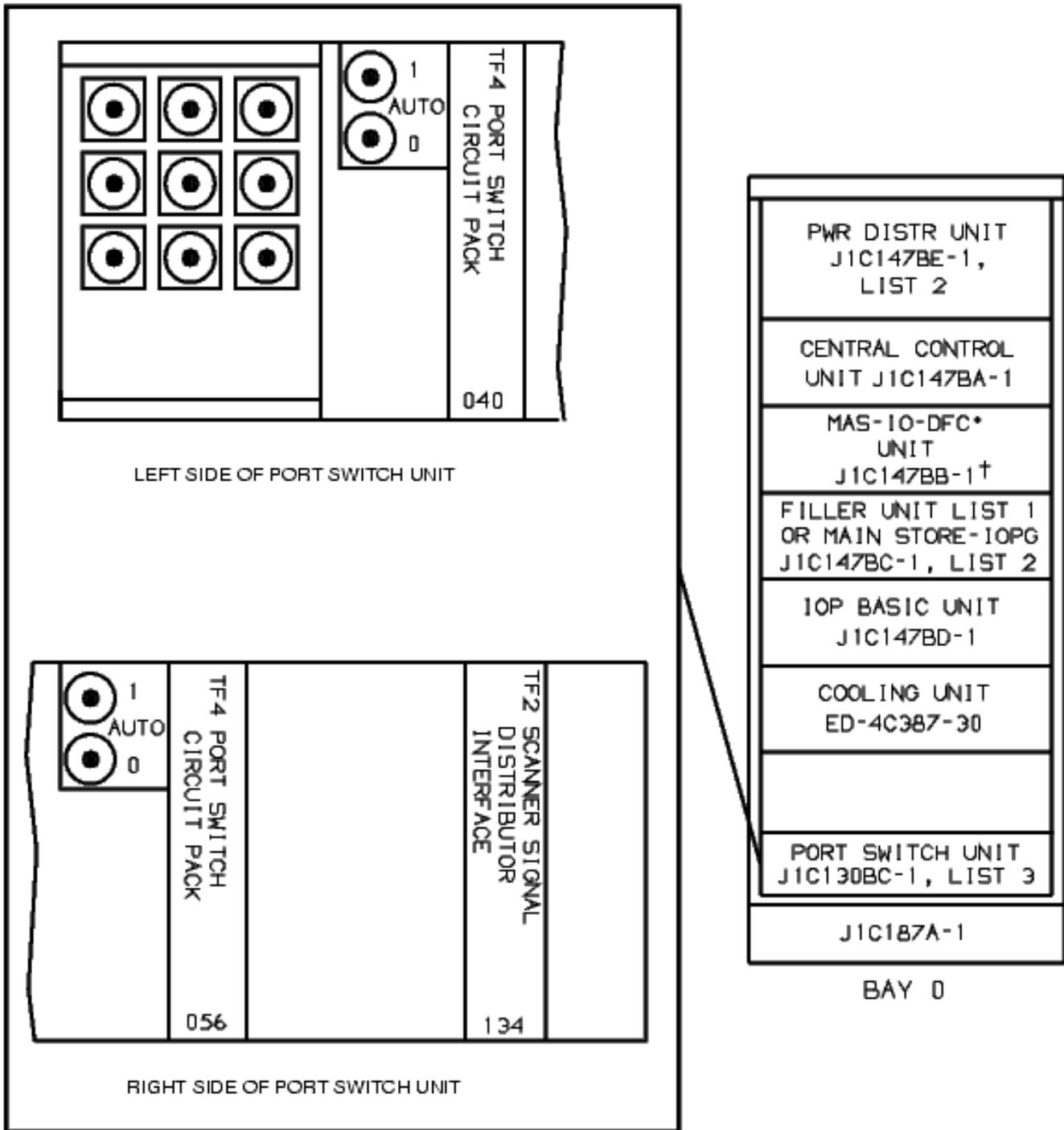


Figure 5.1-8 Port Switch Unit - J1C130BC-1

5.1.1.7 Power Distribution Unit (PDU) - J1C147BA-1

The Power Distribution Unit (PDU) is a single-shelf unit mounted in the top of Processor Cabinet Bays 0 and 1. It is an assembly of fuse blocks, input jacks and terminal blocks.

Power is routed from the Power Distribution Frame (PDF) on cable pairs into the PDU and distributed out through

fused circuits by way of terminal blocks feeding the processor cabinet units. Refer to ED-4C184-12 for details on running power feeders to AM cabinets.

The Port Switch Unit (PSU) in Bay 0 is supplied -48 V DC directly from Jack J in the PDU. In Bay 1, Jack J is not connected.

Specific fuse assignments are made at the local office as indicated in appropriate office records.

Figure 5.1-9 illustrates the PDU and its location in the processor cabinet. A rear view shows input/output provisions.

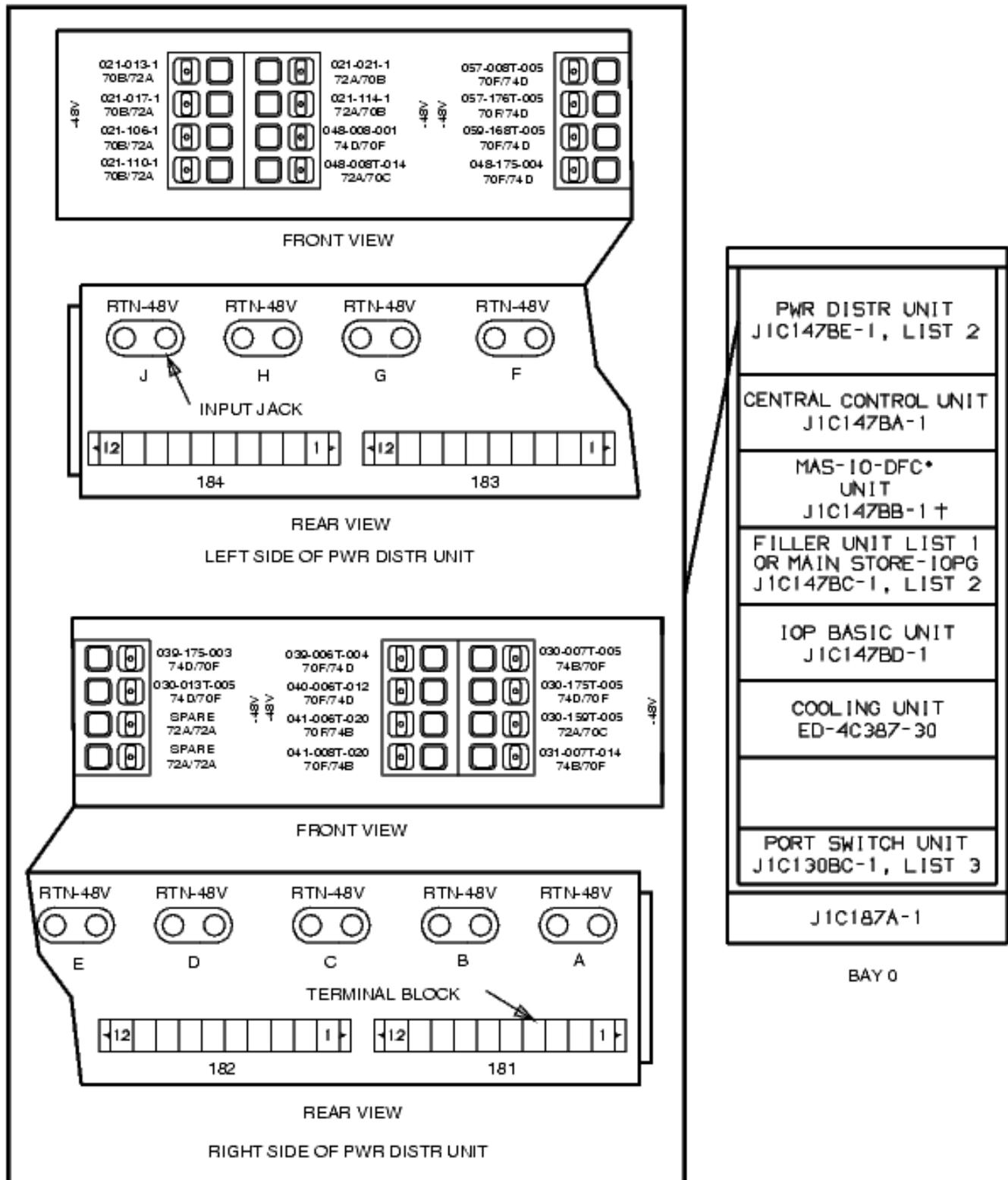


Figure 5.1-9 Power Distribution Unit - J1C147BA-1

5.1.1.8 Tape/Disk Cabinet - J1C192A-1

The Tape/Disk Cabinet contains tape units and disk drives as required for specific 5ESS®-2000 switch office configurations. A cabinet can contain a tape unit and four disk drives or no tape unit and up to eight disk drives for growth accommodation.

Streaming tape units are used in the computer. Two types are available: KS-22762, 1600 bits per inch (BPI) and KS-23113, 6250/1600 BPI. Each unit contains a tape transport and a power distribution unit. The units have a protective, plastic-hinged front cover with a cut-out for access to the control panel. A circuit breaker keeps the transport power supply from drawing more than 10 amperes of current. The breaker must be in the one position for unit operation.

Figure 5.1-10 illustrates the Tape/Disk Cabinet and the components in it.

Tape diagnostics, self (off-line) and system (on-line), are run on transports to ensure proper operation.

Self-diagnostics are run on the transport during normal operation and when requested from the operator control panel. Test result codes are shown on the digital display (Figure 5.1-11). When a fault occurs during normal operations, reference the displayed digital fault code to the functional fault recovery table (Table 5.1-2) to determine corrective action.

The operator initializes diagnostic test 01, which runs for about 10 minutes. Tests 02 and 03 are available to KS-trained (maintenance) personnel to analyze certain failures in test 01 and can give false indications if run at other times.

Run test 01 as follows:

PRESS POWER ON SWITCH.

LOGIC OFF indicator lights.

TOUCH LOGIC ON SWITCH.

LOGIC OFF indicator goes off. (Diagnostics include a power-on health check that runs when the LOGIC ON switch is touched. If the digital display indicates a fault, verify power to the unit, verify that the operation is legal or change the tape. If the fault does not clear, call KS maintenance.)

LOGIC ON indicator lights.

THREAD TAPE. [Do not move tape to Beginning of Tape (BOT).]

CLOSE DOOR.

TOUCH TEST SWITCH (Display reads 01)

TOUCH EXECUTE SWITCH.

Test proceeds with various motion and read/write exercises for about 10 minutes.

If the test is successful, the tape rewinds, the digital display reads 00 and the RESET indicator illuminates.

If the test fails, the diagnostic halts, the RESET indicator lights and a fault code (number) is displayed. Reference the fault code in Table 5.1-2 to determine corrective action.

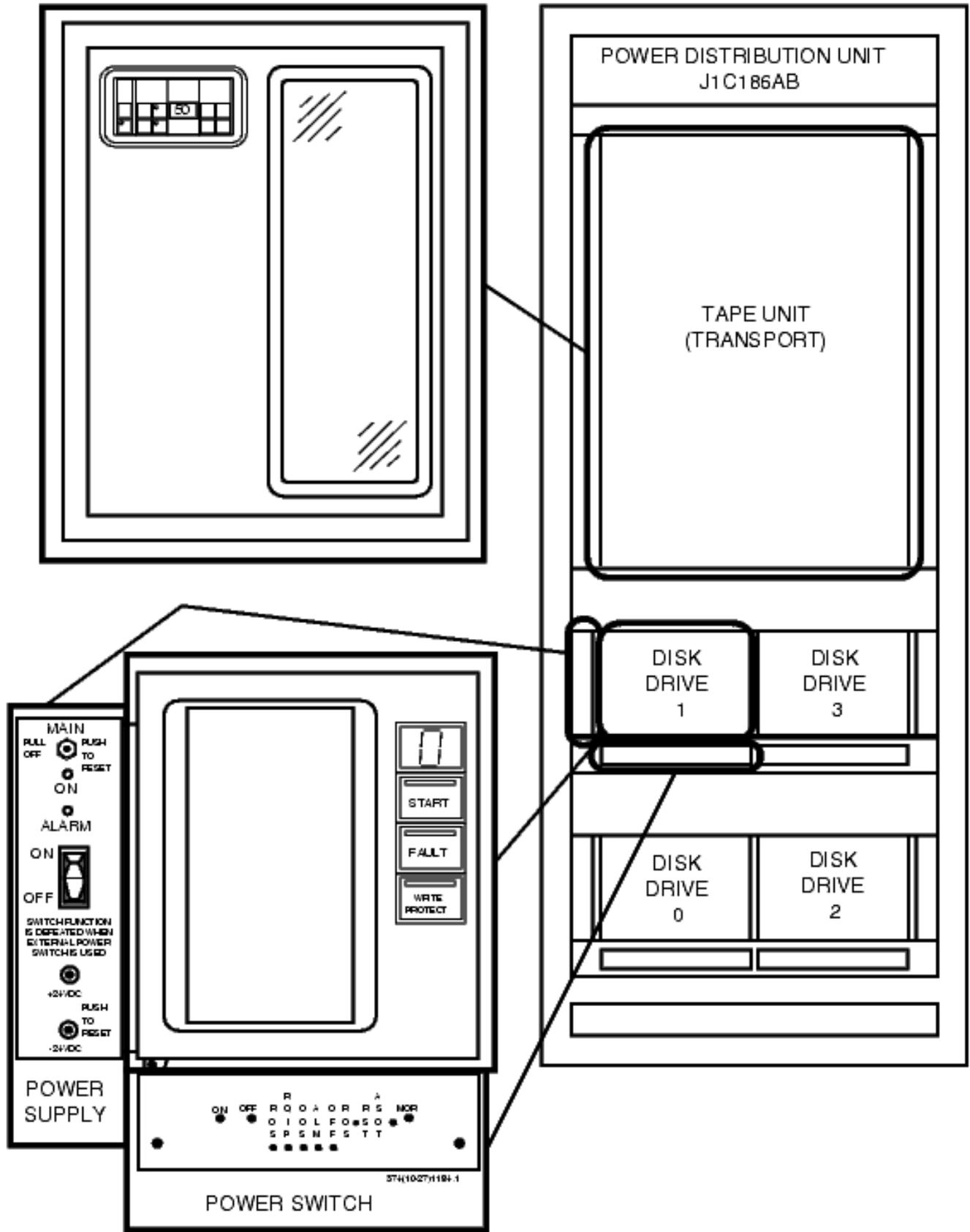


Figure 5.1-10 Tape/Disk Cabinet - J1C192A-1

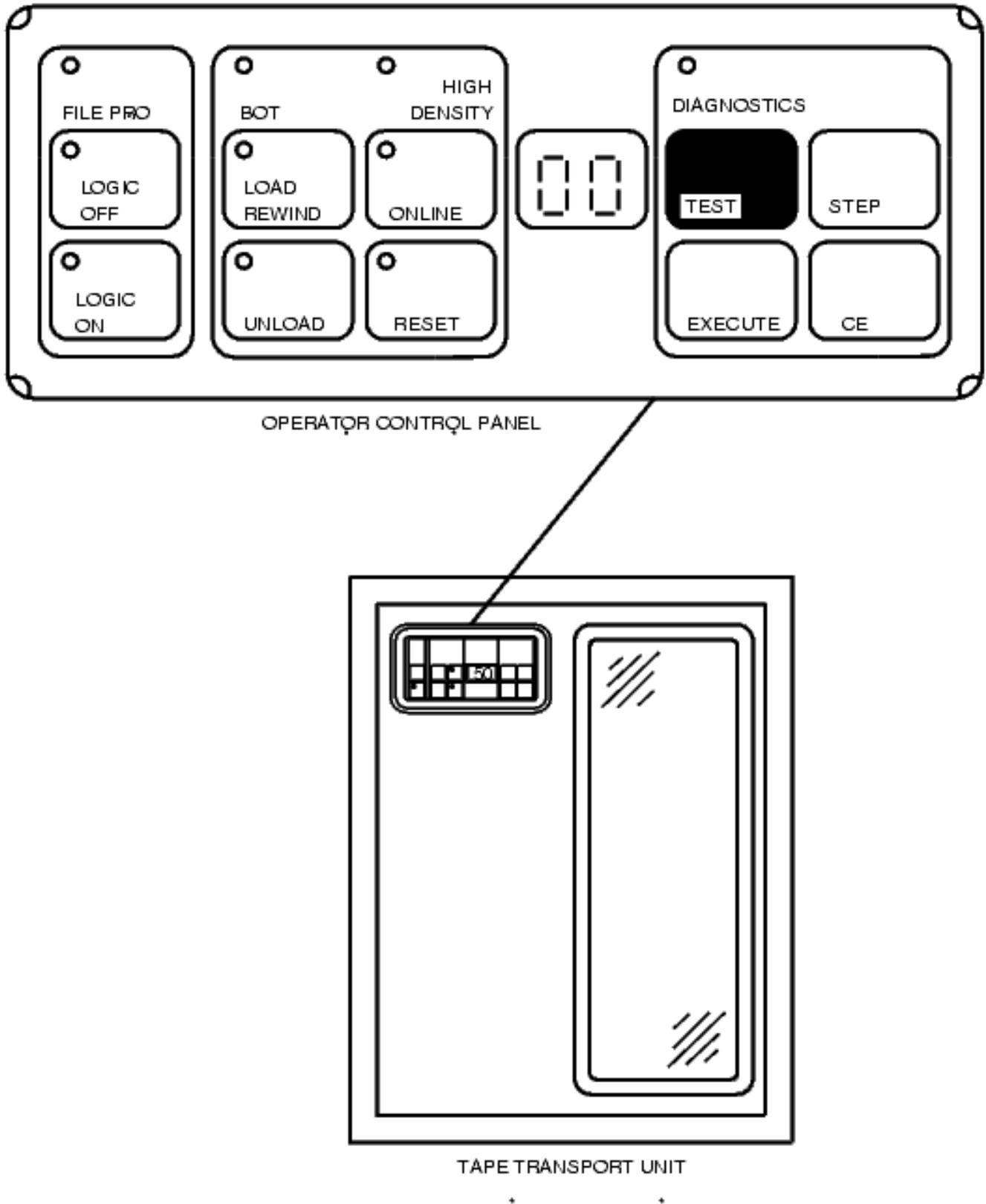


Figure 5.1-11 Operator Control Panel

Table 5.1-2 Operator Test 01 Fault Recovery

FAULT CODE	CAUSE OF FAULT	CORRECTIVE ACTION		
		1	2	3
01-09	Read/Write Errors	Clean Read/Write Head	Change Tape	Call Maintenance
10	Operator Door Open	Close Door	Call Maintenance	—
11	Tape Not Threaded	Thread Tape	Call Maintenance	—
12	Hub Not Latched	Latch Hub	Change Tape	Call Maintenance
13	Tape Incorrectly Threaded	Thread Tape Per Diagram	Call Maintenance	—
14	BOT Marker Fault	Check Location of Marker	Change Tape	Call Maintenance
15	Reset Switch Aborted Load/Unload	Retry Operation	Call Maintenance	—
16	Tape Not Write Enabled	Install Write Enable Ring	Call Maintenance	—
17	EOT Marker Fault	Check Location of Marker	Change Tape	Call Maintenance
18	Tape Already Loaded	Unload and Thread Tape	Call Maintenance	—
20-29	Tape/Unit Fault	Clean Read/Write Head	Change Tape	Call Maintenance
30-99	Unit Fault	Call Maintenance	—	—

5.1.2 3B21D COMPUTER SYSTEM - J3T061A-1

The 3B21D is a high-speed, fault-tolerant, high-reliability, duplex computer. Refer to Figure 5.1-2. The 3B21D is similar to 3B20D computer except for the following:

- Expansion slots in the 3B21D computer control unit complex
- Maximum main store memory configuration is increased from 64 MB to 128 MB
- Tape unit - connects to a Disk File Controller (DFC) via (SCSI) bus versus tape unit connects through input/output processor in the 3B20D computer.
- Disk file controller - supports up to three DFCs versus four in 3B20D computer. A minimum DFC consists of one disk file controller A, one SCSI host adapter and one power converter.
- Direct Memory Access (DMA) - supports up to 32 dual-serial channels versus 64 in the 3B20D computer.

The 3B21D computer system is packaged in one to three cabinets. Figure 5.1-12 depicts the two 3B21D cabinets. The cabinets are as follows:

- Processor cabinet - which is required at all times.
- First peripheral growth cabinets (J3T059A-1) - which are for the 9-track small computer systems interface (SCSI). Tape drives are required as part of the configuration. The first peripheral growth cabinet is located to the right of the processor cabinet. The 3B21D currently uses a 9-track tape unit for procedures such as downloading disks and for an AMA backup system. However, it can also support the Digital Audio Tape (DAT) units. These units are considerably smaller than the current 9-track units. The use of the DAT eliminates the need for a tape frame on the 3B21D AM, thus reducing it from a 2-frame to a 1-frame configuration.

Each cabinet measures 72 inches (182 cm) high by 30 inches (76 cm) wide by 24 inches (60 cm) deep. Figure

5.1-13 shows the layout of the processor unit cabinet. Figure 5.1-14 shows the layout of the growth unit cabinet.

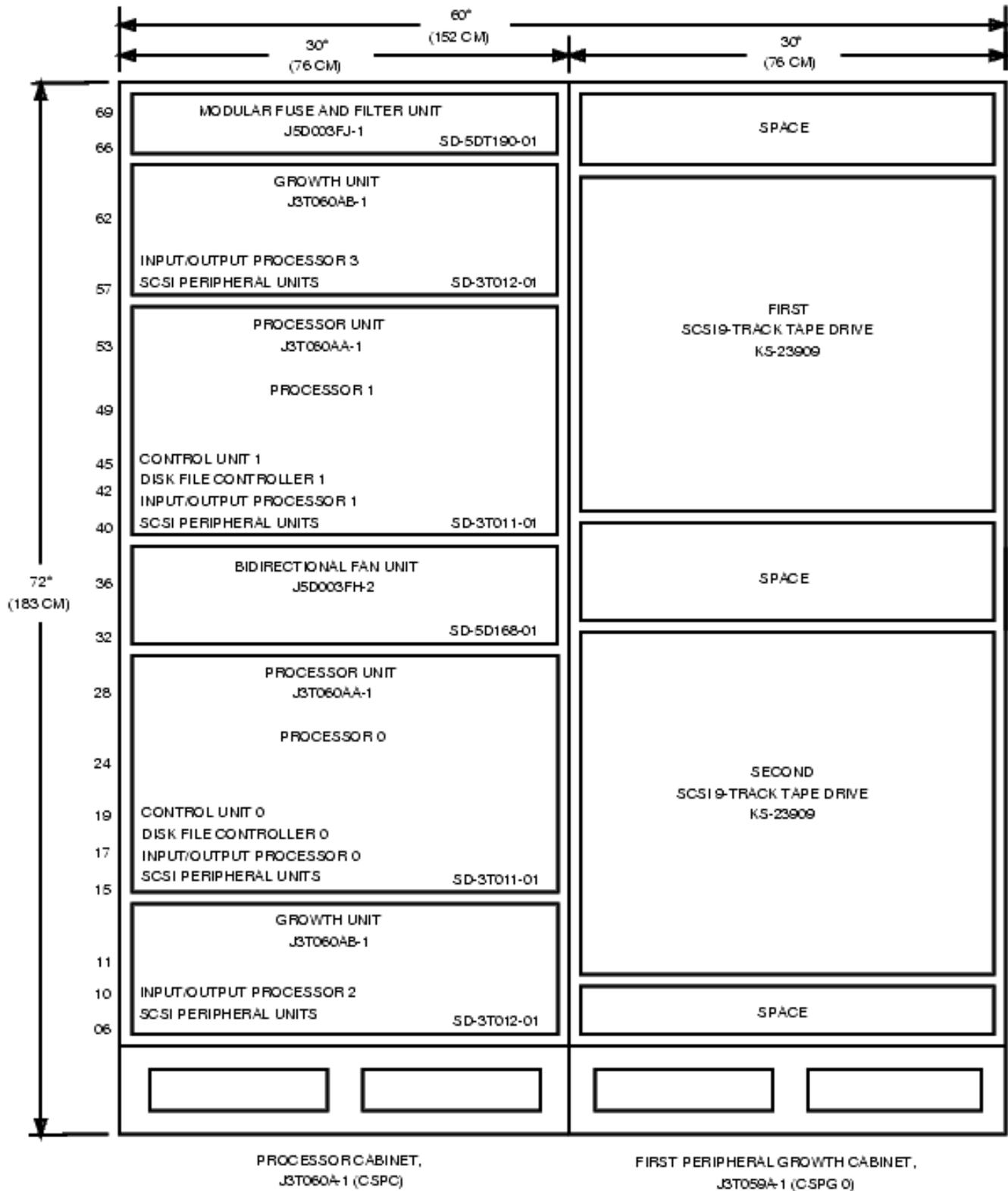


Figure 5.1-12 3B21D Computer

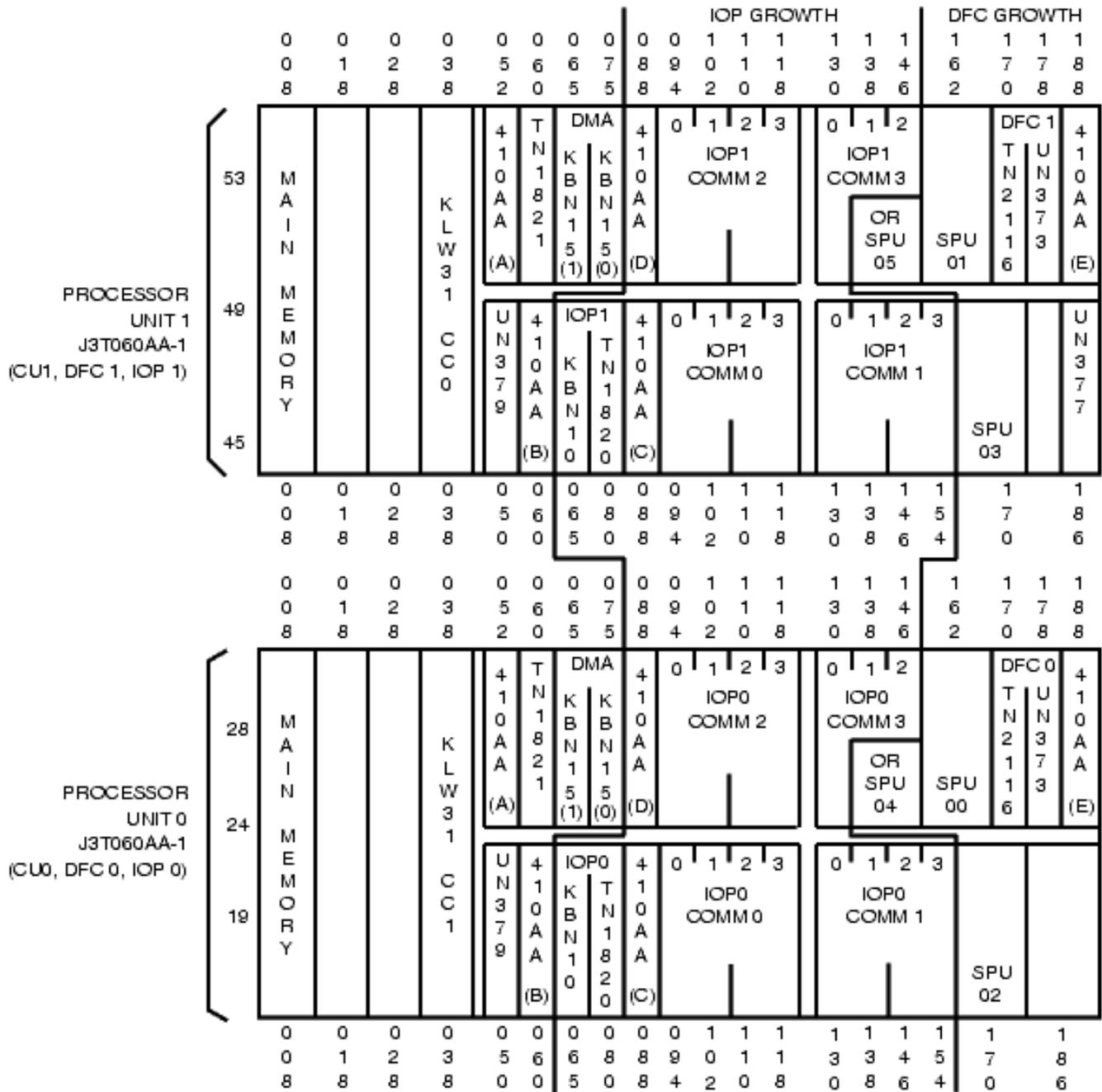


Figure 5.1-13 Processor Unit Shelf Layout - J3T060AA-1

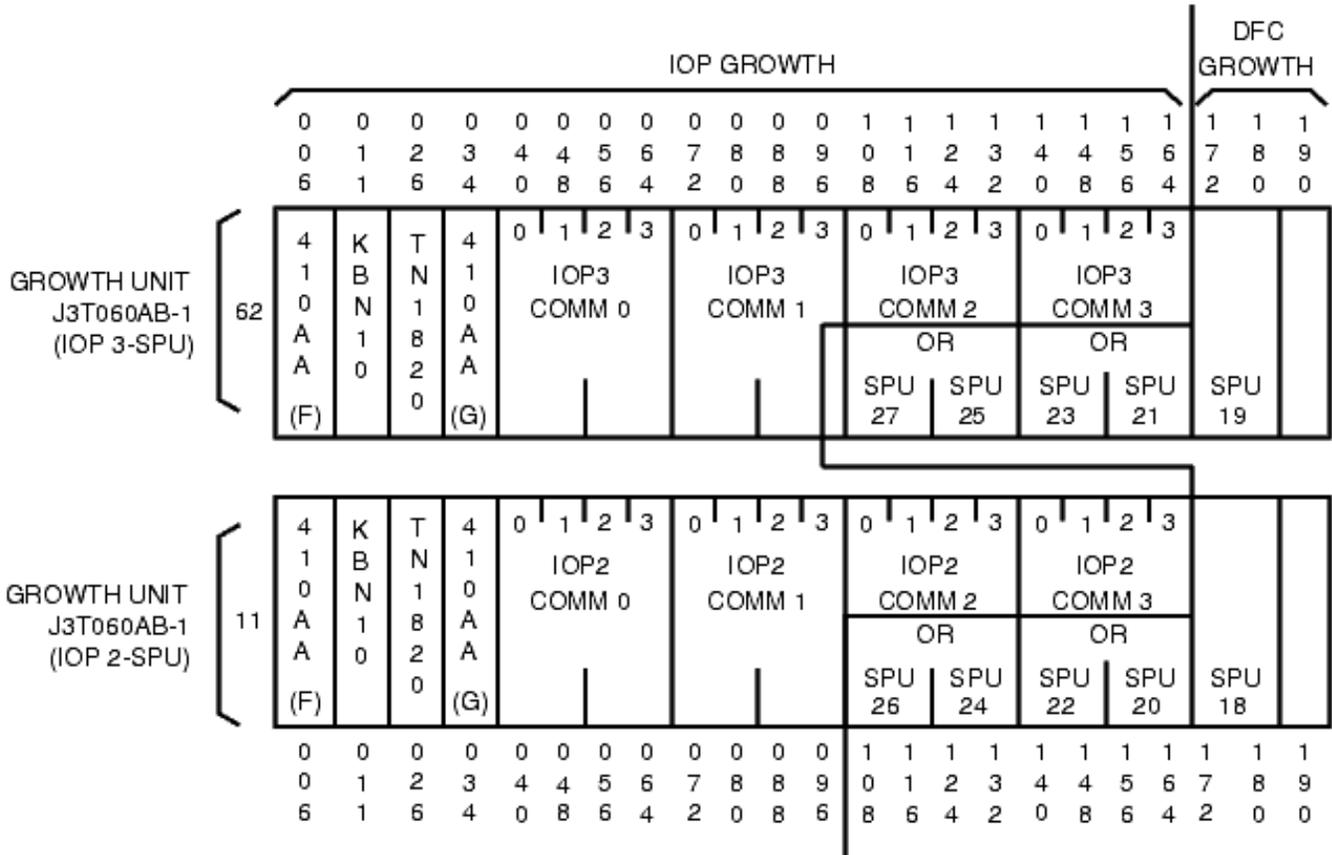


Figure 5.1-14 Growth Unit Shelf Layout - J3T060AB-1

5.1.2.1 Small Computer System Interface (SCSI)

The Small Computer System Interface (SCSI), used in the 3B21D, is an interface for computer input/output devices, primarily data storage units. The exchange uses a distributed-processing system, but the data storage remains centralized. The SCSI is designed for multiple access to a central mass data storage area.

The SCSI bus has 50 terminating leads in a 2-by-25-pin female connector. For administration module (AM) application, the SCSI bus is limited to five devices, four disk drives, the central processor unit (CPU) and the disk file controller (DFC).

The SCSI bus numbering is detailed in Table 5.1-3 .

In the AM the DFC serves as two SCSI host adapters, intelligent devices that direct data flow.

The SCSI bus interface has an arrangement for peripheral devices for the AM as it evolves.

The SCSI has the following:

- More disk space
- Increased reliability
- Lower floor space requirement
- Simpler DFC design incorporation.

Older disk systems needed up to three cabinets to house the maximum of 16 disks. The SCSI disk system contains up to 16 disk units in a single cabinet and can grow two additional disk file controllers providing up to 32 disk units housed in only two cabinets. Equipping the AM with SCSI disk units also reduces maintenance costs.

The SCSI disk units are configured with the same amount of memory capacity as the 340-MB storage module device (SMD) disk units. This configuration may change in the future to let the SCSI disk units take advantage of their entire memory spectrum.

Figure 5.1-2 illustrates the AM including SCSI.

Table 5.1-3 SCSI Peripheral Unit Controller and Bus Assignments

SCSI PERIPHERAL UNIT ^a		PROCESSOR CABINET CONFIGURATION			ADDITIONAL GROWTH (WITH REDUCED IOP CAPABILITY)
DESCRIPTION	LOCATION	BASIC	EXAMPLE 1 WITH GROWTH UNIT AT EQL 57	EXAMPLE 2 WITH GROWTH UNITS AT EQLS 57 AND 06	
	PROCESSOR CABINET				
SPU00	28-162	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 2 DFC 1/SBUS 3 DFC 0/SBUS 0 DFC 1/SBUS 1 DFC 0/SBUS 2 DFC 1/SBUS 3 DFC 0/SBUS 0 DFC 1/SBUS 1 DFC 0/SBUS 2 DFC 1/SBUS 3 DFC 0/SBUS 0 DFC 1/SBUS 2 DFC 0/SBUS 2 DFC 1/SBUS 3
SPU01	53-162	DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU02	19-170	DFC 0/SBUS 2	DFC 0/SBUS 2	DFC 0/SBUS 2	
SPU03	45-170	DFC 1/SBUS 3	DFC 1/SBUS 3	DFC 1/SBUS 3	
SPU04	28-146	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU05	53-146	DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU06	19-154				
SPU07	45-154				
SPU08	28-118				
SPU09	53-118				
SPU10	19-138				
SPU11	45-138				
SPU12	28-102				
SPU13	53-102				
SPU14	19-118				
SPU15	45-118				
SPU16	19-102				
SPU17	45-102				
SPU18	11-180			DFC 0/SBUS 2	
SPU19	62-180		DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU20	11-164			DFC 0/SBUS 0	
SPU21	62-164		DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU22	11-148			DFC 0/SBUS 2	
SPU23	62-148		DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU24	11-132			DFC 0/SBUS 0	
SPU25	62-132		DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU26	11-116			DFC 0/SBUS 2	
SPU27	62-116		DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU28	11-096				
SPU29	62-096			DFC 0/SBUS 0	
SPU30	11-080			DFC 1/SBUS 1	
SPU31	62-080			DFC 0/SBUS 2	
SPU32	11-064			DFC 1/SBUS 3	
SPU33	62-064			DFC 0/SBUS 0	
SPU34	11-048			DFC 1/SBUS 1	
SPU35	62-048			DFC 0/SBUS 2	
SPU54 (MT)	19-186	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 1/SBUS 3
	PERIPHERAL CABINET				
SPU56 (9-TRACK1)	10-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU57 (9-TRACK0)	42-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU58 (9-TRACK3)	17-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	
SPU59	42-XXX	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	DFC 0-1/ SBUS 0-3	

(9-TRACK2)		0-3	0-3	0-3	
Notes:					
a. An SCSI Peripheral Unit (SPU) can be any SCSI device such as 9-track tape, Digital Audio Tape (DAT), Moving Head Disk (MHD) drive, or magnetic tape (MT) unit.					

The SCSI disk unit (DU) consists of a disk drive and a power supply. The disk unit is an industry standard Winchester-type drive, supported by a built-in processor to accept instructions from the disk file controller (DFC) via the SCSI bus. The SCSI DFC controls the transfer of data between the CU and up to eight SCSI disk drives. The major subcircuits are as follows:

- Duplex Dual Serial Bus Selector (DDSBS) - TN69B — Connects the DFC to the DSCH.
- Host Adapter (HA) — Interfaces the DDSBS, intelligent control logic, and two different SCSI buses. The HA consists of a UN294 and TN2116 circuit pack.

The assembled housing for the Disk Unit Package (DUP) slides and locks onto a shelf that holds two DUPs. Refer to Figure 5.1-15 for an exploded view of the DUP components.

The DUP consists of the following components:

- Disk module
- Power supply board (CGG2)
- Power switch board (CGG1)
- Fan module
- Internal device selector microswitch and cable assembly
- Internal cable assemblies
- Internal power cable assemblies
- Housing and mountings.

The front panel of the DUP disk module has cutouts for access to the Internal Device (ID) selector switch, the operating controls and Light-Emitting Diode (LED) indicators. Figure 5.1-16 illustrates the DUP controls and indicators.

A fan module is on the unit chassis of each DUP for ventilation. The module contains a single fan with a panel for alarm and control mounting. For detailed fan replacement procedures, see 235-105-220. Figure 5.1-17 illustrates a rear view of the fan module.

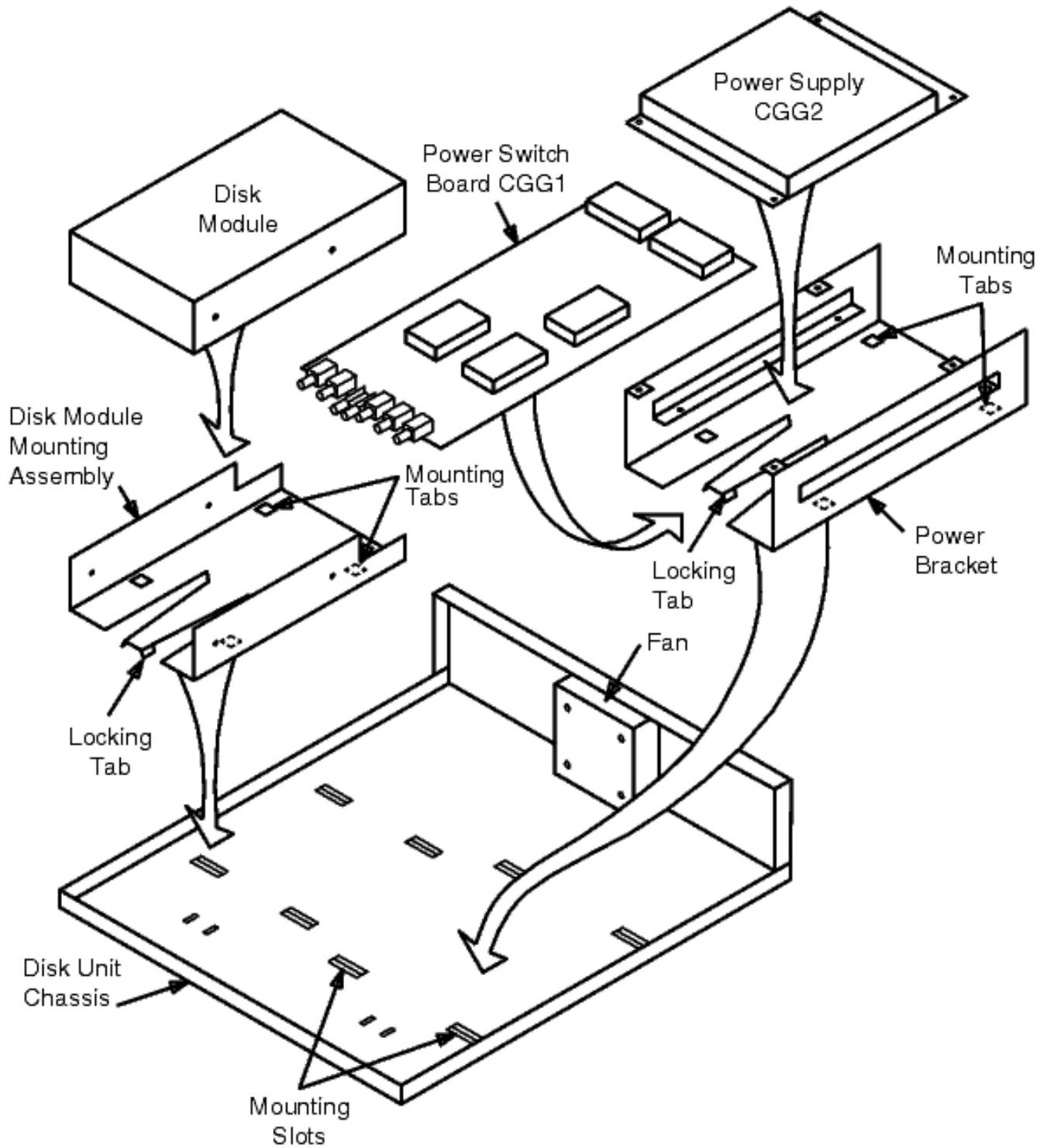


Figure 5.1-15 Disk Unit Package Components

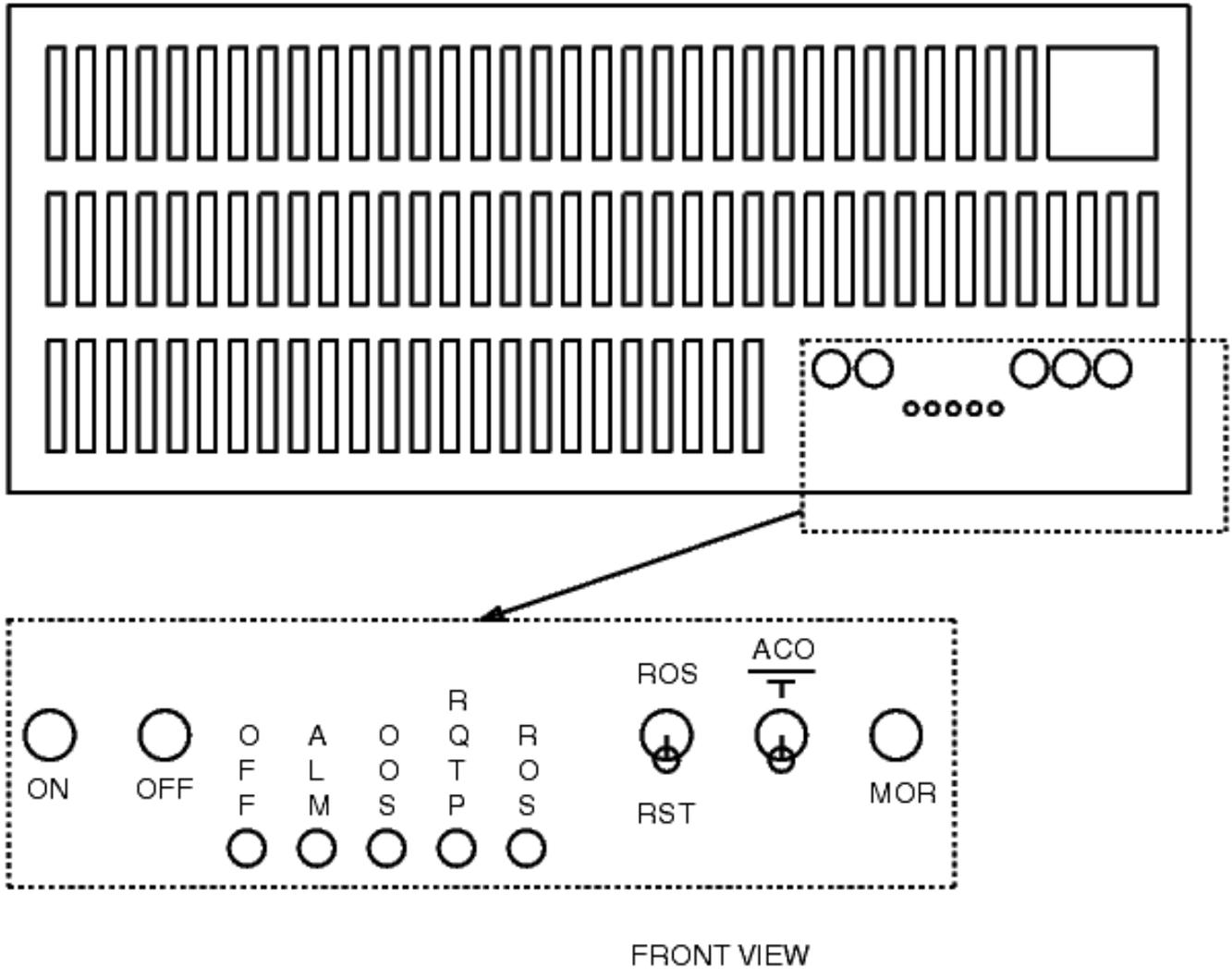


Figure 5.1-16 DUP Controls and Indicators

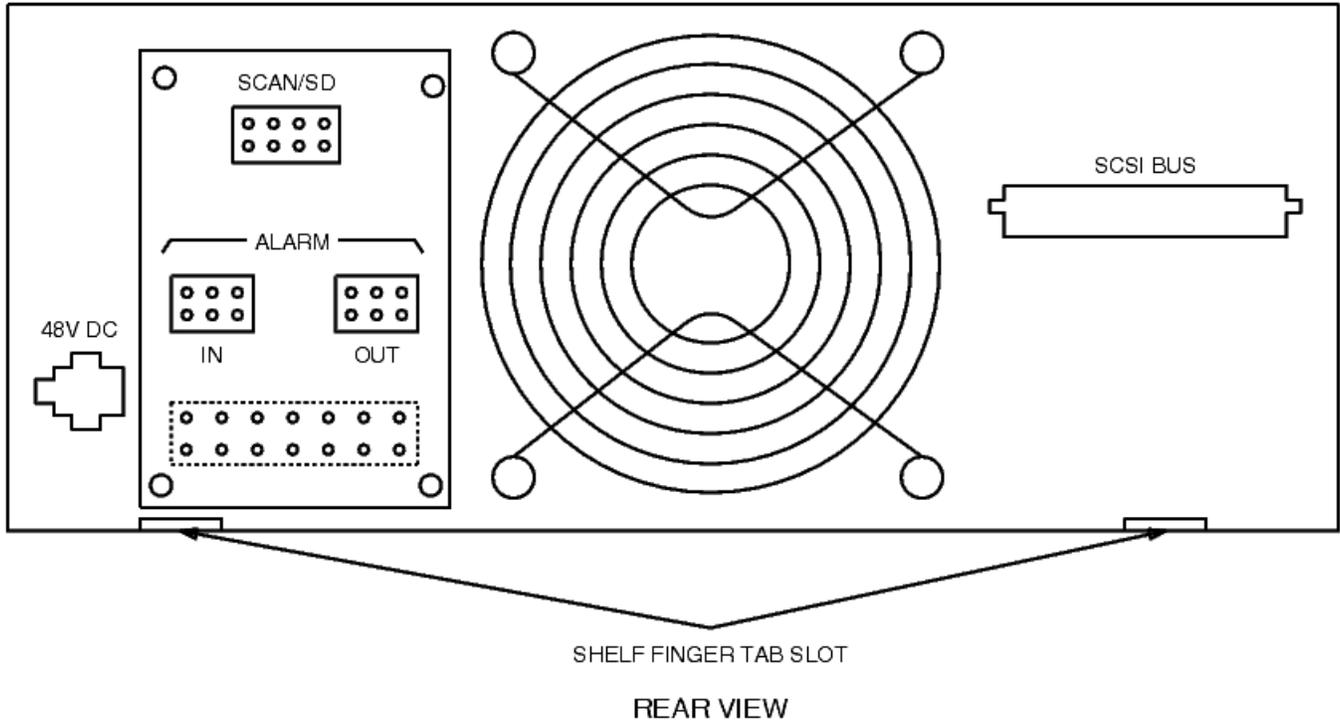


Figure 5.1-17 Fan Module

5.1.2.2 Digital Audio Tape (DAT) - UN376

The Digital Audio Tape (DAT) has a faceplate-mounted circuit pack, 3.5-inch, single-ended SCSI digital data storage (DDS) formatted DAT drive. The DAT drive uses 4-mm wide tape in 90-, 60- and 30-meter cartridges. The usable storage capacity of the DAT drive varies with the length of tape and recording mode. The usable storage capacity of the DAT drive varies with the length of the tape and the recording mode. In a noncompressed mode, the capacity is 650 MB for 30 M; 1300 MB for 60 M; and 2500 MB for the 90-M tape.

The SCSI device identification for the DAT drive is set to any available device address from 0 to 6, inclusive, using three SCSI device identification switches on the circuit pack.

Refer to 235-105-510 for additional information.

5.1.2.3 Processor Cabinet, Basic System - J3T060A-1

The basic system configuration consists of the Processor Cabinet equipped with the following major units:

- One Modular Filter and Fuse Panel Unit, J5D003FJ-1
- One Bidirectional Cooling Unit, J5D003FH-2
- Two Processor Units, J3T060AA-1.

The basic system configuration has the following equipment:

- Control Unit 0 and Control Unit 1 (CU 0 and CU 1).
- Direct Memory Access 0 (DMA 0) is part of the basic system. The DMA 1 is optional.

- Disk File Controller 0 (DFC 0) and DFC 1 supporting seven SCSI Peripheral Units (SPUs). An SPU slot can be equipped with a UN375 Moving Head Disk (MHD) circuit pack or a UN376 Digital Audio Tape (DAT) circuit pack. The DFC 0 supports four SPUs; DFC 1 supports three SPUs. There are five dedicated SPU slots in the basic units (Processor Unit 0 and 1). Optionally, two additional SPUs (SPU04 and SPU05) can be grown instead of equipping Input/Output Processor (IOP) Peripheral Controller (PC) Community 3 (PC31 and 32.) The PC30 slot in each Processor Unit is always available for use as a PC. One DAT drive (SPU54) is controlled by DFC 0.
- IOP 0 with Peripheral Communities 0, 1, 2 and 3.
- IOP 1 with Peripheral Communities 0, 1, 2 and 3.

5.1.2.4 Peripheral Growth Cabinet - J3T059A-1

The first Peripheral Growth Cabinet has one SCSI 9-track tape drive, KS-23909. This is the first 9-track tape drive (SPU57) in the 3B21D computer system.

A single SCSI bus cable connects a 9-track tape drive to any available SCSI bus (SBUS 0, 1, 2 or 3).

The 9-track tape drives are AC powered and plug directly into an AC power outlet. The drives can be configured to use either 50- or 60-Hertz power.

5.1.2.5 SCSI Peripheral Unit Controller

An SCSI peripheral unit (SPU) can be any device such as 9-track tape, digital audio tape, moving head disk or magnetic tape unit.

The naming convention for the two SCSI buses is "BUS A" and "BUS B." The 3B21D computer system designations for the SCSI buses are different, as follows:

- The SCSI BUS A and BUS B of DFC 0 are "SBUS 0" and "SBUS 2," respectively.
- The SCSI BUS A and BUS B of DFC 1 are "SBUS 1" and "SBUS 3," respectively.

A DFC includes a UN373 (DFCA), TN2116 (DFCB) and is powered by a 410AA (DC-to-DC converter). The equipment locations (EQLs) for DFC 0 and DFC 1 are as follows:

- DFC 0 is in the Processor Cabinet, Processor Unit 0, at 28-170 (TN2116), 28-178 (UN373) and 28-188 (CONVE).
- DFC 1 is in the Processor Cabinet, Processor Unit 1, at 53-170 (TN2116), 53-178 (UN373) and 53-188 (CONVE).

For more detailed information on the 3B21D computer, refer to 235-105-510.

5.1.3 Administrative Services Module (ASM)

The 5ESS Switch Administrative Services Module (ASM) integrates a commercial hardware and software platform into the 5ESS architecture. The ASM will enable service providers to offer switching features even faster. The ASM is a simplex Sun Netra t1120 server, running the Solaris 2.6 operating system. It is NEBS Level 3 compliant and has access to the Administrative Module (AM) of the Switch via Lucent Technologies' proprietary Dual Serial Channel Computer Interconnect (DCI) high-speed interface. This link will support multiple channels for parallel operations, providing high-speed DMA access to the Switch. The ASM will support a wide variety of commercially available

software and hardware for network access. Capabilities such as UUCP File Transfer Protocol with TCP/IP, and 10 BaseT Ethernet are included in the base configuration.

5.1.3.1 Power

The ASM is designed to be rack-mounted in a Miscellaneous Cabinet located no more than 100ft. from the AM and is powered by dual —48V DC battery feeds.

5.1.3.2 Configuration

The ASM is equipped with the following:

- Sun Netra t1120 server —NEBS Level 3 Certified
- Solaris 2.6 Operating System
- 256 Mb memory
- Single Processor
- CD-ROM (4x)
- Two RS-232 ports
- Cables
- One Ethernet port
- Four PCI slots
- 1 pair 18.2G mirrored disks
- DAT tape drive
- Alarm interface
- Optional Miscellaneous Cabinet

5.1.3.3 Functional Description

The SUN Netra t1120 server runs on the Solaris 2.6 operating system. It currently provides capacity for administering data changes on the switch, downloading software updates to the switch, and for evolving the switch database to a new software release.

5.2 COMMUNICATION MODULES

5.2.1 INTRODUCTION

This section contains information about Communication Modules (CMs) 1 and 2 (CM1, CM2 and CM2C). Typical CMs and their respective units are described and illustrated. The diagnostic phase descriptions for the CMs are also described in this section.

For diagnostic execution input message and POKE command source information, refer to the following documents:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-700, *Input Message Manual*
- 235-600-750, *Output Message Manual*.

5.2.2 COMMUNICATION MODULE MODEL 1 - J5D001C/J5D006C

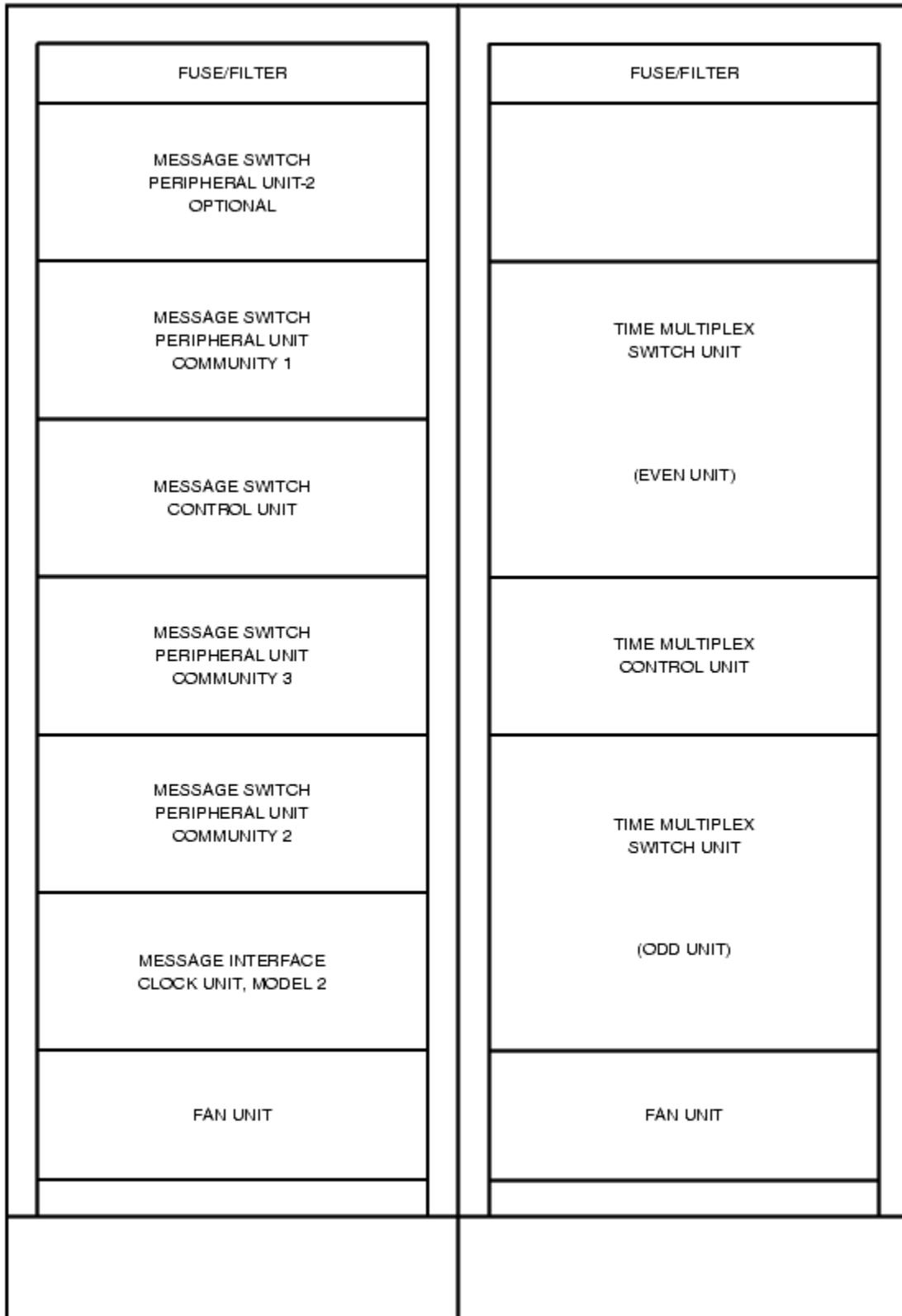
Communication Module Model 1 (CM1) consists of four cabinets. There are two Time-Multiplex Switch (TMS) cabinets, 0 and 1 and two Message Switch (MSGS) cabinets, 0 and 1. Equipment in TMS cabinet 0 and MSGS cabinet 0 is duplicated in TMS cabinet 1 and MSGS cabinet 1, respectively. The cabinets operate as active major and active minor.

The TMS units terminate Switching Module (SM) Network Control Timing links and are responsible for space switching the time slots.

The MSGS units have timing and process control messages for the SMs.

Figure 5.2-1 illustrates the CM1 cabinets and their contents.

A Communication Module Processor (CMP), in the form of two circuit packs, is added to the Community 1 Message Switch Peripheral Unit (MSPU).



MESSAGE SWITCH CABINET 1

TIME MULTIPLEX SWITCH CABINET 1

Figure 5.2-1 Communication Module Model 1**5.2.3 COMMUNICATION MODULE MODEL 2 - J5D020A-1**

Communications Module Model 2 (CM2) consists of at least two cabinets (5 and 6) and as many as 12 cabinets (0 through 11). Cabinets 5 and 6 represent the basic CM2 and are duplicates.

A CM2 complex is divided into Side 0 and Side 1; added CM2 cabinets must be supplied in duplicated pairs, one for Side 0 and one for Side 1. Any CM2 cabinets added to the basic complex are positioned adjacent to cabinets 5 and 6 with Side 0 cabinets descending in order from 4 to 0 and Side 1 cabinets ascending in order from 7 to 11.

The two basic cabinets (5 and 6) are J5D020A-1. Added cabinets (0 to 4 and 7 to 11) are J5D020B-1. Figure 5.2-2 illustrates the basic Communication Module 2 (cabinets 5 and 6) and the respective units contained in the Module.

Figure 5.2-3 illustrates the numbering scheme for a fully equipped CM2 configuration containing 12 cabinets (0 to 11).

A Communication Module Processor Unit (CMPU), in the form of CMPU units, is added to the CM2.

The optional Quad-Link Packet Switch (QLPS), release resides in CM2.

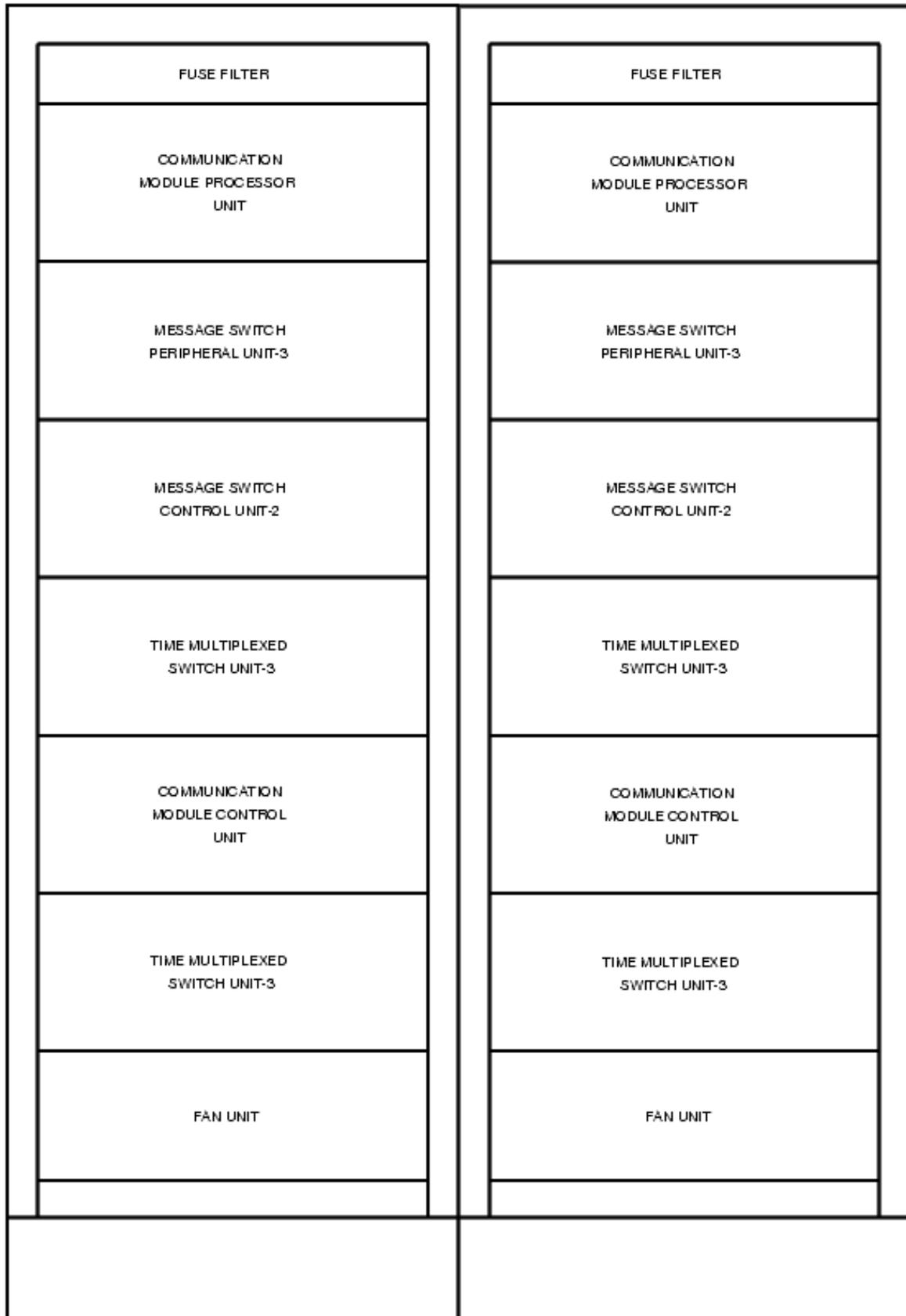


Figure 5.2-2 Communication Module Model 2 - J5D020A-1

EQL	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER	FUSE/FILTER
						CMPU	CMPU					
53	MSPU-3 COMM 15, 14	MSPU-3 COMM 13, 12	MSPU-3 COMM 11, 10	MSPU-3 COMM 6, 7	MSPU-3 COMM 4, 5	MSPU-3 COMM 2, 3	MSPU-3 COMM 3, 2	MSPU-3 COMM 5, 4	MSPU-3 COMM 7, 6	MSPU-3 COMM 10, 11	MSPU-3 COMM 12, 13	MSPU-3 COMM 14, 15
45	E BUS 010	E BUS 08	E BUS 06	E BUS 04	E BUS 02	MSCU-2	MSCU-2	E BUS 12	E BUS 14	E BUS 16	E BUS 18	E BUS 110
36	TMSU-3 010	TMSU-3 08	TMSU-3 06	TMSU-3 04	TMSU-3 02	TMSU-2 00	TMSU-2 10	TMSU-2 12	TMSU-2 14	TMSU-2 16	TMSU-2 18	TMSU-2 110
28	E BUS 011	E BUS 09	E BUS 07	E BUS 05	E BUS 03	CMCU	CMCU	E BUS 13	E BUS 15	E BUS 17	E BUS 19	E BUS 111
19	TMSU-3 011	TMSU-3 09	TMSU-3 07	TMSU-3 05	TMSU-3 03	TMSU-2 01	TMSU-2 11	TMSU-2 13	TMSU-2 15	TMSU-2 17	TMSU-2 19	TMSU-2 111
11	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT	FAN UNIT
	CABINET 0	CABINET 1	CABINET 2	CABINET 3	CABINET 4	CABINET 5	CABINET 6	CABINET 7	CABINET 8	CABINET 9	CABINET 10	CABINET 11
	← SIDE 0					SIDE 1 →						

GLOSSARY OF ACRONYMS:
 EBUS - EMITTER COUPLED LOGIC BUS
 CMCU - COMMUNICATION MODULE CONTROL UNIT
 COMM - COMMUNITY
 MSCU - MESSAGE SWITCH CONTROL UNIT
 MSPU - MESSAGE SWITCH PERIPHERAL UNIT

Figure 5.2-3 Communication Module Model 2 (Fully Equipped)

5.2.4 COMMUNICATION MODULE MODEL 2 COMPACT

The Communications Module Model 2 Compact (CM2C) consists of the following three shelves:

- Two Communications Module Units (CMU) shelves - J5D020AJ-5
- One Communications Module Processor Unit (CMPU) shelf - J5D020AF-1

Figure 5.2-4 illustrates the CM2C and its respective units.

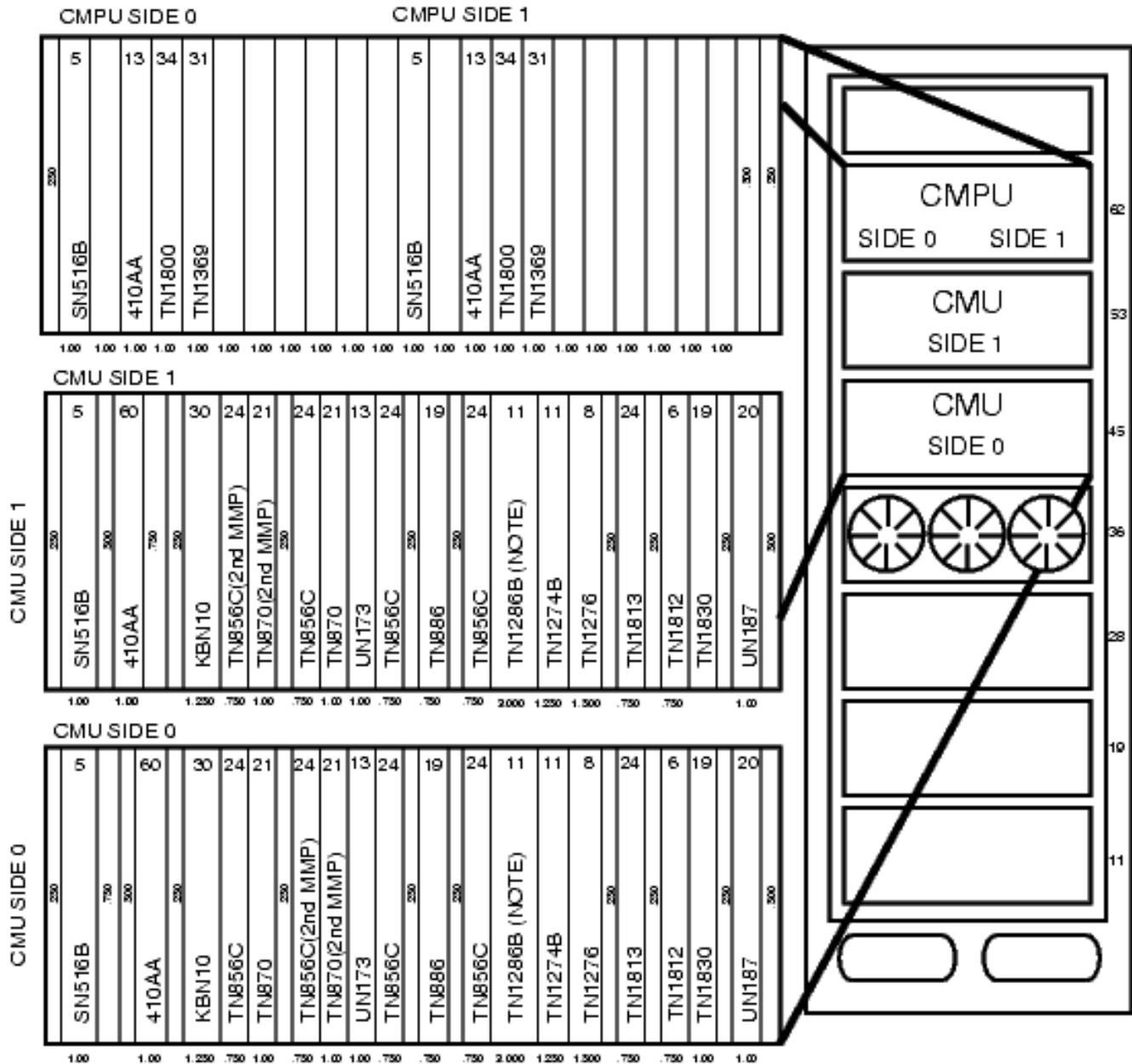
The CM2C shelves must be housed in either a Switching Module Controller (SMC) or a Link and Trunk Peripherals (LTPs) cabinet and the cabinet must be located immediately to the left of the Administrative Module (AM). Of the two Local Switching Modules that the CM2C may be equipped with, only one, at most, can be an SM-2000.

The CM2C has the following limitations:

- Supports a maximum of two Switching Modules: a Local Switching Module (LSM), a Host Switching Module (HSM), an Optically Remote Module (ORM) or a Two-Mile Optically Remote Module (TRM)
- Supports a maximum of six Remote Switching Modules (RSMs)
- Supports a maximum of two Module Message Processors (MMPs)
- Supports a maximum of three Network Clock (NCLK) references
- Supports a maximum of four Time-Multiplexed Switch (TMS) links
- Supports only one single fabric configuration
- Supports a maximum of one SM-2000
- Does not support the Quad-Link Packet Switch (QLPS).

The CM2C configuration requires a Lucent 3B21D computer in the AM.

CM2C DUAL MMP



NOTE:
OTHER CLOCK PACK OPTIONS ARE ALLOWED.

Figure 5.2-4 CM2C and CPU Cabinet

5.2.5 COMMUNICATION MODULE PROCESSOR UNIT - J5D020AF-1

The Communication Module Processor Unit (CMPU) is added to the Communication Module Model 2 (CM2). The CMPU is also part of the CM2C. Its major functions are to perform Recent Change and Call Processing in the Administrative Module.

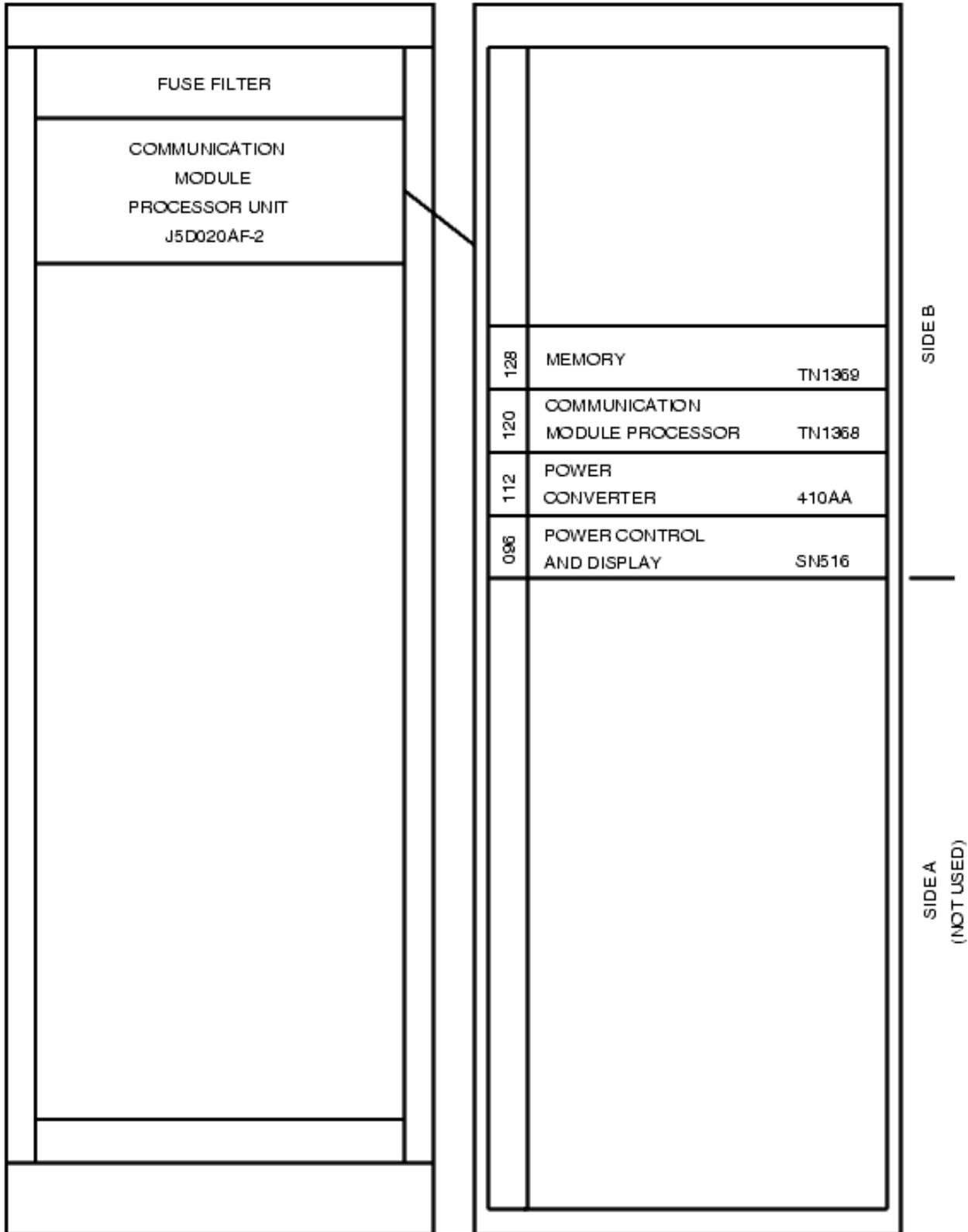
The CMPU is a single-shelf unit, one of which is located in CM2 Cabinets 5 and 6. Each unit is divided into Side A and Side B; each side supports up to two communities, 0 and 1. Only four circuit packs are used in the present configuration and they are in Side B for Community B0. In the CM2C, the CMPU is a single-shelf unit that contains both Side 0 and Side 1.

The CMPU is used in the CM2C. The CMPU Side 0 is in Community A0 and CMP Side 1 is in Community B0.

The Communication Module Processor (CMP) uses the TN1368 core circuit pack which contains 4 MB of Dual Dynamic RAM (DDRAM) and 0.75 MB of static RAM (SRAM). The TN1800 core circuit pack, which has 16 MB of DDRAM and 3 MB of SRAM replaces the TN1368 core circuit pack. TN1800 applies to both CM2/CM2C.

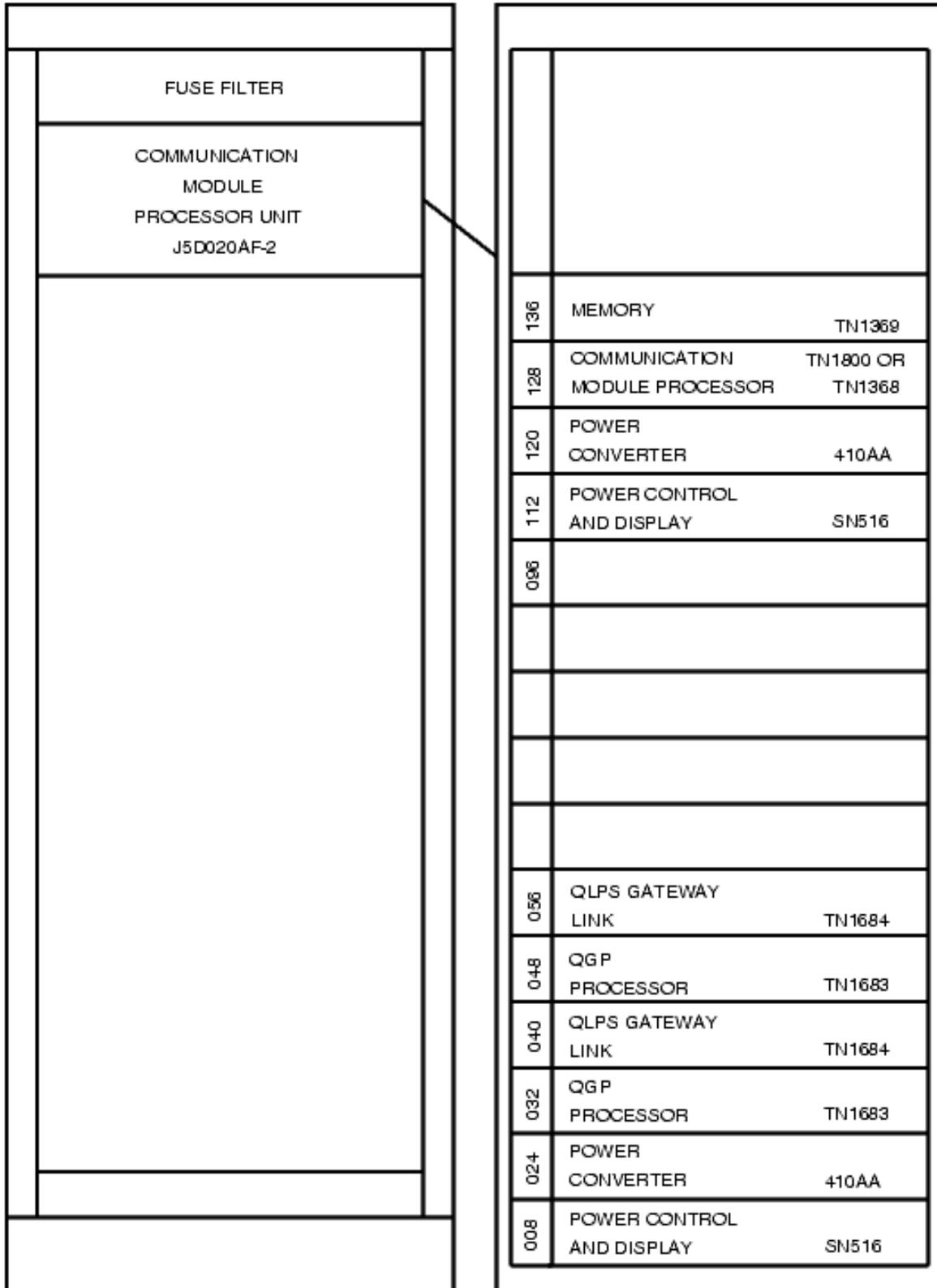
Figure 5.2-5 illustrates the location of the CMPU in the CM2 and the circuit packs in it. Refer to Figure 5.2-4 which illustrates the location of the CMPU in the CM2C and the circuit packs in it.

In the 5ESS[®]-2000 switch, the CMPU shelf has been divided into two communities, 0 and 8; 0 is the CMP side (Side B) of the shelf for CMPs and 8 is the QGP side (Side A) of the shelf for QLPS Gateway Links (QGPs.) The QGP community is optional. Figure 5.2-6 shows a typical QGPS (4QGP) network configuration.



tpa 760681/01

Figure 5.2-5 Communication Module Processor Unit, - J5D020AF-1



tpa 821749/01

Figure 5.2-6 Communication Module Processor Unit, with Optional QGP - J5D020AF-1

5.2.6 COMMUNICATION MODULE UNIT - J5D020AJ-5

The Communications Module Unit (CMU) is the basic unit of the CM2C. CMU sides 0 and 1 are located at EQL positions 45 and 53, respectively, in either the SMC or an LTP cabinet, which must be located immediately to the left of the AM.

The CMU consists of the following eight function blocks:

- The KBN10 board has message switch controller. This board is also used in the CM2s MSCU3.
- The TN856C and UN173 boards are foundation peripheral controllers. These boards are also in the CM2s FPC.
- The TN856C and TN886 boards are the pump peripheral controllers. These boards are the same ones used as the CM2's PPC.
- The TN856C and TN870 boards are the message module processor. These boards are the same ones that are used as the CM2s MMP.
- The UN187 board is the message interface controller. This board is the same one used in the CM2.
- The TN1276 and TN1274B, along with either the TN1284B or TN1286B boards are the Network Clock (NCLK). These boards are the same ones used as the CM2s NCLK2.
- The time-multiplexed switch function is provided by the TN1812, TN1813 and TN1830 boards. These boards are new with the CM2C.

All of the above mentioned units in the CMU are powered by a single power supply, except for the network clock oscillator (NCOSC) which has its own power supply as it does in the CM2.

5.2.7 COMMUNICATION MODULE CONTROL UNIT - J5D020AA-1

The Communication Module Control Unit (CMCU) is provided in only the two basic Communication Module cabinets 5 and 6 and are fixed located at EQL position 28. Unit 0 is in cabinet 5 and unit 1 is in cabinet 6.

The three main functions of the CMCU are as follows:

- (1) To provide timing for the switch. The type of oscillator pack (TN1284 or TN1286) and microcode of the TN1276 determines the type of office Network Clock as Stratum 2 or Stratum 3.
- (2) To control the switching of the Time-Multiplexed Switching Unit - Model 2 (TMSU2) fabric. EQLs 170 and 178 are used only in Dual Fabric arrangements.
- (3) To regulate the control time slots between the link interface packs of the TMSU2 or TMSU3 and the Module Message Processors (MMPs) located on the Message Switch Peripheral Unit Model 3 (MSPU3) or the Pump Peripheral Controller (PPC) located on the Message Switch Control Unit - Model 2 (MSCU2).

The Emitter-Coupled Logic Bus (EBUS) originates from the CMCU and provides the metallic path over which the CMCU communicates with every TMSU2. The EBUS (J5D020AE-1) is a single-shelf unit that distributes clock and data to/from all switch units in the TMS. The EBUS unit connects the TMSUs with the time-multiplexed switch controller circuit located in the CMCU.

The EQL 116 (TN310) is used only when no growth cabinets are supplied.

Figure 5.2-7 illustrates the location of the CMCU2 in the basic module and the circuit packs contained in the unit.

178	DUAL MESSAGE INTERFACE 2	TN 1034
170	DUAL MESSAGE INTERFACE 1	UN 186
162	DUAL MESSAGE INTERFACE 3	UN 187
154	DUAL MESSAGE INTERFACE 1	UN 186
146	DUAL MESSAGE INTERFACE 2	TN 1034
138	CONTROL INTERFACE BUS	
130	TIME MULTIPLEXED SWITCH CONTROLLER	TN 884
122	CONTROL INTERFACE	UN 183
116	TRANSMIT DATA	UN 310
112	CLOCK INTERFACE	TN 881
104	-2V POWER CONVERTER	495 MA
088	-5VA POWER CONVERTER	410 AA
070	DIGITAL PHASE LOCK LOOP	TN1276
058	SYNCHRONIZER	TN1274 B
048	OSCILLATOR	TN1286 OR TN1284
024	POWER CONVERTER +12V/+5V	495 KA
008	POWER CONTROL AND DISPLAY	SN516

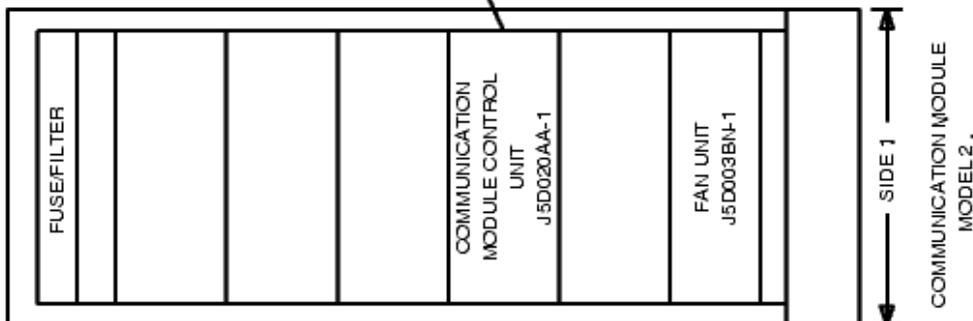


Figure 5.2-7 Communication Module Control Unit - J5D020AA-1

5.2.8 MESSAGE INTERFACE CLOCK UNIT - J5D006ED-1

The Message Interface Clock Unit (MICU) is a single-shelf assembly containing timing and control time slot interface circuit packs. The MICU can interface up to four communities of Module Message Processors (MMPs). Each community is cross-coupled to the mate MICU.

The network clock is configured in the active/standby arrangement. The standby clock receives timing from the active clock and the active clock receives timing from an oscillator board equipped within the MICU.

Figure 5.2-8 illustrates the MICU and the circuit packs in it.

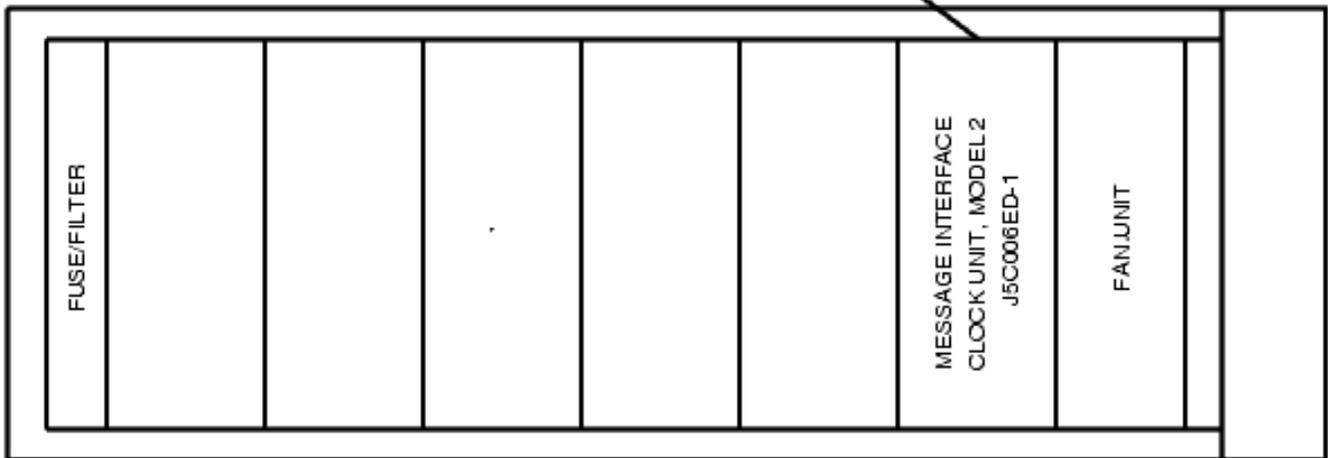
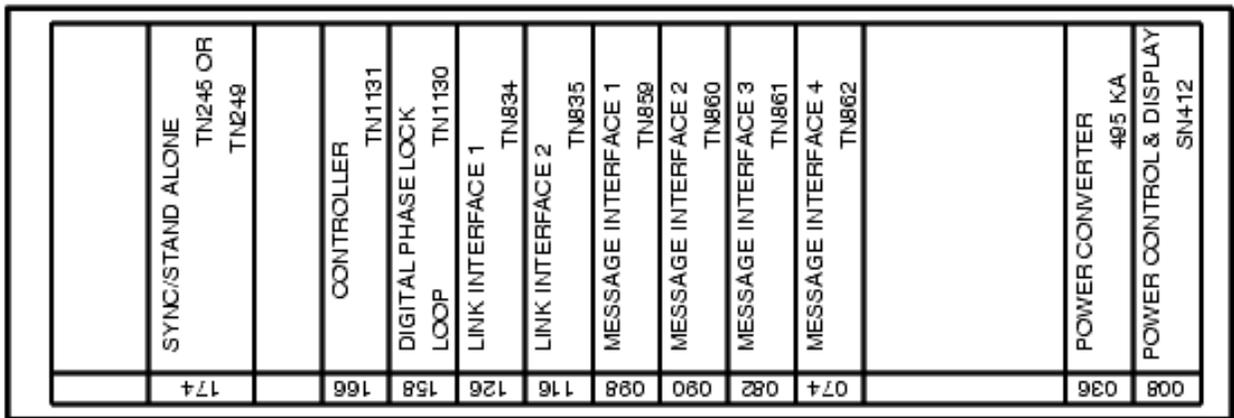


Figure 5.2-8 Message Interface Clock Unit - J5D006ED-01

5.2.9 MESSAGE SWITCH CONTROL UNITS

5.2.9.1 Message Switch Control Unit (MSCU) - J5D006AB-1

The Message Switch Control Unit (MSCU) is located at EQL 45 in the Communications Module 1 (CM1) Message

- Pumpable Micro Control Store
- Bus Interface Controller (BIC).

The unit provides four basic functions as described as follows:

- (1) Reformats data received from the Administrative Module (AM) or Communication Module Processor Unit (CMPU) and transmits it to the other units in the cabinet.
- (2) Reformats data received from other units in the cabinet and transmits it to the AM or CMPU.
- (3) Interprets destination codes of incoming control time slots and switches the control time slots to the AM or another Switching Module (SM).
- (4) Provides control of the other units in the CM2 cabinet.

Figure 5.2-10 illustrates the location of the MSCU2 in the Communication Module, Cabinets 5 and 6 and the respective circuit packs in the unit.

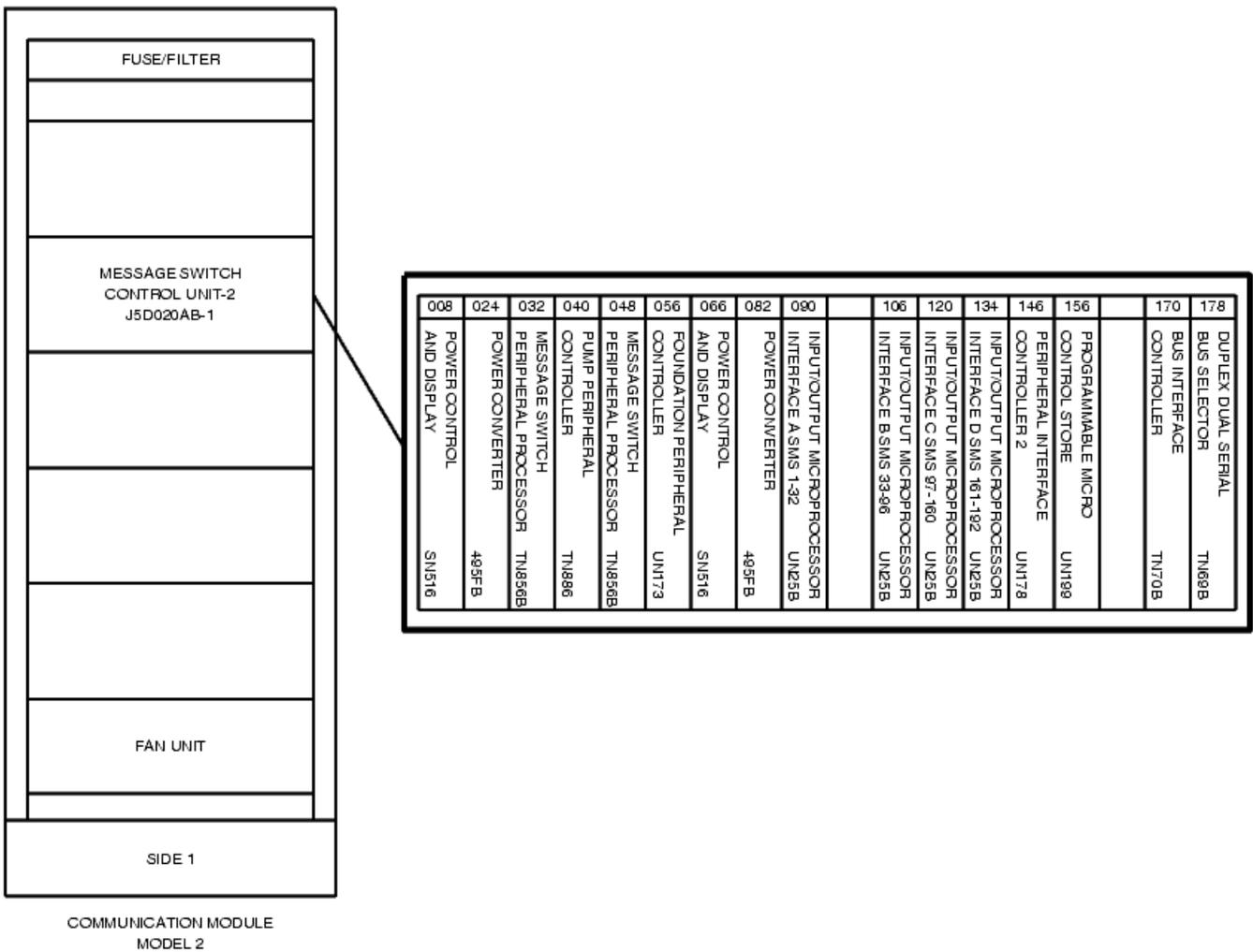


Figure 5.2-10 Message Switch Control Unit Model 2 - J5D020AB-1

5.2.9.3 Message Switch Control Unit Model 3 - J5D020AH-5

The Message Switch Control Unit Model 3 (MSCU3) controls message transfers among the Administrative Module (AM) and as many as 14 peripheral control communities, each consisting of one to four peripheral controls. A Peripheral Controller (PC) can be a Module Message Processor (MMP), Foundation Peripheral Control (FPC), Pump Peripheral Controller (PPC) or Communication Module Processor (CMP). The community with the FPC and PPC is limited to two PCs and is contained within the MSCU3. Message transfers are accomplished under the control of a bit-slice processor on the Input/Output Processor 2 (IOP2)/Message Switch Control 3 (MSC3) circuit pack.

The MSCU3 provides the following functions:

- Performs the serial-to-parallel conversion of data received from the AM and the parallel-to-serial conversion of data transmitted to the AM.
- Provides one to four Input/Output Microprocessor Interfaces (IOMIs) to interface the IOP2/MSC3 with the MMPs, FPC and PPC.
- Provides control to transfer data among MMPs or between the AM and MMPs.
- Provides control to transfer data between the AM and the FPC or PPC.
- Performs self-diagnostics that are resident in IOP2/MSC3 firmware.
- Provides control and diagnostic access for the Dual Message Interface (DMI), Network Clock (NCLK) and Time-Multiplexed Switch Model 2 (TMS2) via the FPC.
- Provides a PPC for loading the Switching Module (SM) with data at 192 kbps.
- Provides both manual and AM control of the MSCU3 from an in-service/ out-of-service point of view.

The MSCU3 can be equipped with up to three additional external IOMIs to provide additional communities.

5.2.9.3.1 Message Switch Peripheral Processor

The Message Switch Peripheral Processor (MSPP) is the controlling circuit pack of all message switch peripheral controller applications. It is a single-board processor with an interface through an IOMI bus to the IOP2/MSC3 as well as an interface to application boards needed for each specific function. The MSPP contains a 16-bit microprocessor, 128 KB of Dynamic Random Access Memory (DRAM), 8 KB of static RAM, 16 KB of EPROM and clock circuits to ensure its own sanity and to provide needed timing to application boards.

5.2.9.3.2 Foundation Peripheral Controller

The Foundation Peripheral Controller (FPC) provides the interface for rapid pumping on the SM. Data are pumped from the disk in the AM through the IOP2/MSC2 to the PPC through the on-board IOMI bus. The PPC then sends the data to the CMCU through a Message Interface Bus (MIB). The CMCU sends the data to the TMS2 where it is distributed to the destination SM via a Network Control and Timing (NCT) link.

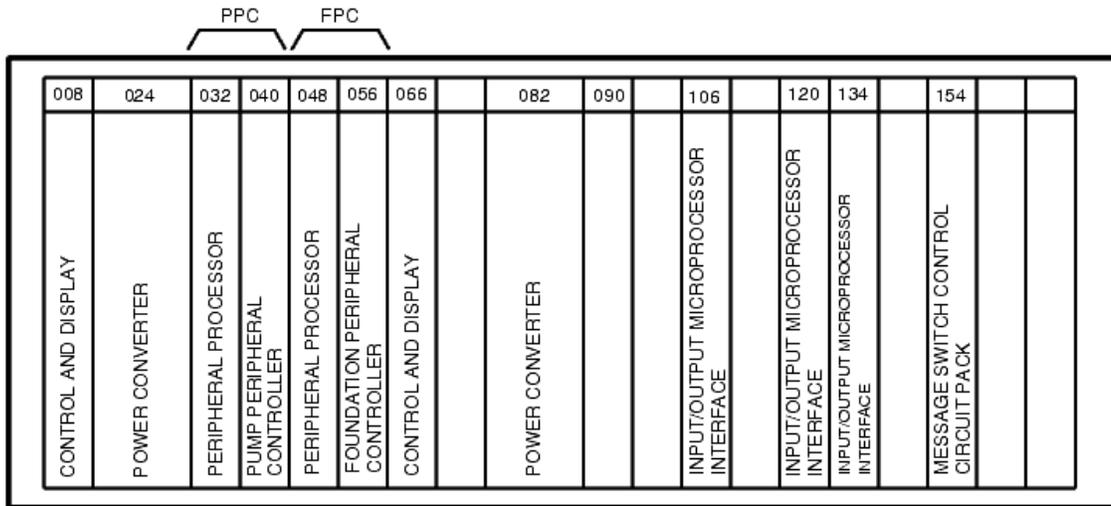
5.2.9.3.3 Control and Display

The Control and Display (C&D) circuit packs run in-service/out-of-service control and the alarming of the power converters. The MSCU3 uses two C&D packs; one provides manual and AM control of the FPC, PPC and their associated MSPPs and the other provides manual and AM control of the IOP2/MSC3 and the IOMIs. The AM monitors the CD packs for fuse alarms, power status (alarms, manual off and power on) and requests for OOS.

5.2.9.3.4 Power Converter - 495FB

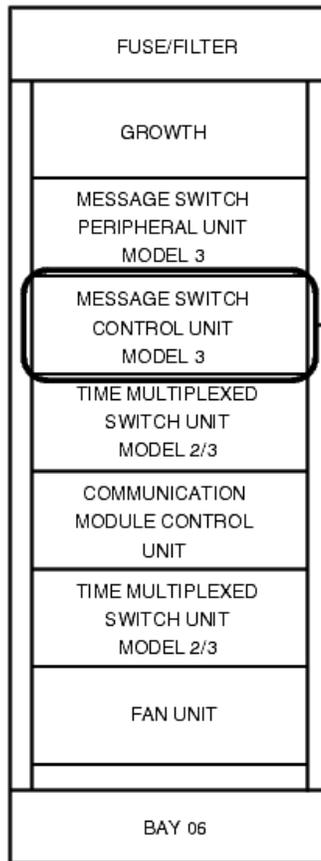
The converter changes a nominal -48 volt input to a well-regulated +5 volt output for applications in the MSCU3 circuits. The power unit is pulse-width controlled for regulation, self-oscillating and operates at a fixed frequency. The 495FB provides +5 volts at 250 watts. The MSCU3 uses two converters, one provides power for the FPC, PPC and their associated MSPPs and the other provides power for the IOP2/MS3 and the IOMIs.

Figure 5.2-11 shows the layout of the MSCU3 circuit packs.



MODEL 3 MESSAGE SWITCH CONTROL UNIT

Note: IOMIs are equipped according to size of the exchange. If there are less than 32 SM's, the IOMI function will be handled by the KBN10 circuit pack. If 33 to 96 SM's, 1 IOMI pack will be utilized. If 97 to 128 SM's, 2 IOMI's will be utilized. If 129 to 192, 3 IOMI's will be utilized.



COMMUNICATION MODULE 2 CABINET

Figure 5.2-11 Message Switch Control Unit Model 3 - J5D020AH-5

5.2.10 QUAD-LINK PACKET SWITCH (QLPS) NETWORK

A optional message switch, the Quad-Link Packet Switch (QLPS), is available to support the higher message traffic of the SM-2000 and the 5ESS[®]-2000 switch.

The QLPS is essentially a high-speed tandem message switch designed to support the increased message traffic from the SM-2000 and its Message Handler (MH) due to the higher volume of calls. The QLPS communicates with the existing 5ESS[®]-2000 switch Message Switch (MSGS) through a QLPS Gateway Link (QGP). The MSGS supports the SM and SM-2000 without QLPS, but to effectively use the higher call capacity of the SM-2000, the eventual addition of the QLPS is recommended.

The QLPS has two significant impacts:

- The QLPS enables a capacity increase of the 5ESS[®]-2000 switch to one million completed POTS calls per hour.
- It lets the 5ESS[®]-2000 switch handle the increased message traffic generated by the message-intensive, distributed-intelligence architecture of the Advanced Intelligent Network.

The QLPS network is an overlay network which provides high- bandwidth/low-latency message transport between an SM-2000 and other SM-2000s, between an SM-2000 and SMs, the Administrative Module (AM), Communication Module Processor (CMP), Direct Link Node (DLN) via the MSGS Peripheral Interface Controller (PIC) and the Foundation Peripheral Controller (FPC). The QLPS network increases the bandwidth for Operating System for Distributed Switching (OSDS) messages from 48 kbps to 896 kbps.

The QLPS network is composed of the following elements: Quad Link Packet Switch (QLPS), QLPS Gateway Link (QGP), QLPS-QGP Link (QGL) and the Quad-Link Interface Model 2 (QLI2). It also includes a new message handler used as a link to the SM-2000.

5.2.10.1 Quad-Link Packet Switch (QLPS)

The Quad-Link Packet Switch (QLPS) is the hub of a "star network." Its purpose is to assemble frames (encapsulate the actual Operating System for Distributed Switching CCS OSDS Messages) received from network endpoints, verify basic frame integrity, determine the destination and store those frames until delivery to the destination can be accomplished.

5.2.10.2 Quad-Link Gateway Processor (QGP)

The QLPS Gateway Processor (QGP) is a Message Switch (MSGS) subdevice, which provides access to/from an MSCU and the QLPS via a QLPS Gateway Link (QGL). The QGP provides QLPS with an interface to the existing 5ESS[®]-2000 switch communications foundation. Messages received at the QGP can be transmitted to the AM, CMP, DLN, FPC SMs or into the appropriately addressed QLPS network and the SM-2000.

NOTE: The QLPS network may be equipped with 0, 1 or 2 QGPs per MSGS side; depending on the QGP configuration, there may 0, 2 or 4 QGLs per QGP.

5.2.10.3 Message Handler

The Message Handler (MH) provides access from the SM-2000 CORE40 to the QLPS network. The connection between the MH and QLPS is via a nailed-up "pipe" through the TMS/TSI.

5.2.10.4 QLPS-QGP Link

The QLPS-QGP Link (QGL) provides the interconnection of the QGP and QLPS via dedicated electrical connections. Each complex of QGPs on a MSGS has four QGL connections, one to each QLPS.

The connection between the MH and the QLPS is via a nailed-up "pipe" through the TMS/TSI.

5.2.10.5 Quad-Link Interface Model 2

The Quad-Link Interface Model 2 (QLI2) circuit pack plugs into the Communications Module Model 2 and provides the network Control and Timing (NCT2) interface between the CM2 and the SM-2000. The QLI2s plug into any existing QLI slot in the TMS, except for the Foundation Link Interface (FLI) slot, which is reserved for the TN883. CM2s equipped with QLI2s support both single- and dual-fabric configurations.

5.2.11 MESSAGE SWITCH PERIPHERAL UNITS

5.2.11.1 Message Switch Peripheral Unit (MSPU) (Community 1) - J5D006AD-1

The Message Switch Peripheral Unit Model 2 (MSPU2) is in EQL 53 in all Communication Module Model 1 cabinets. The main function of the MSPU2 is to process the control time slots and send them to the Message Switch Control Unit (MSCU) for switching to the Administrative Module (AM) or to other Switching Modules (SMs). Each MSPU is identified by a unique community number, 1, 2 or 3, plus an optional MSPU if desired.

The Communication Module Processor Unit (CMPU) has been added in the form of two circuit packs, TN1369 and TN1368. Details for adding the CMP are shown in drawing ED-5D687-30.

Figure 5.2-12 illustrates the location of the MSPUs in the Communication Module Cabinet 1 and the respective circuit packs in the unit, including the CMP.

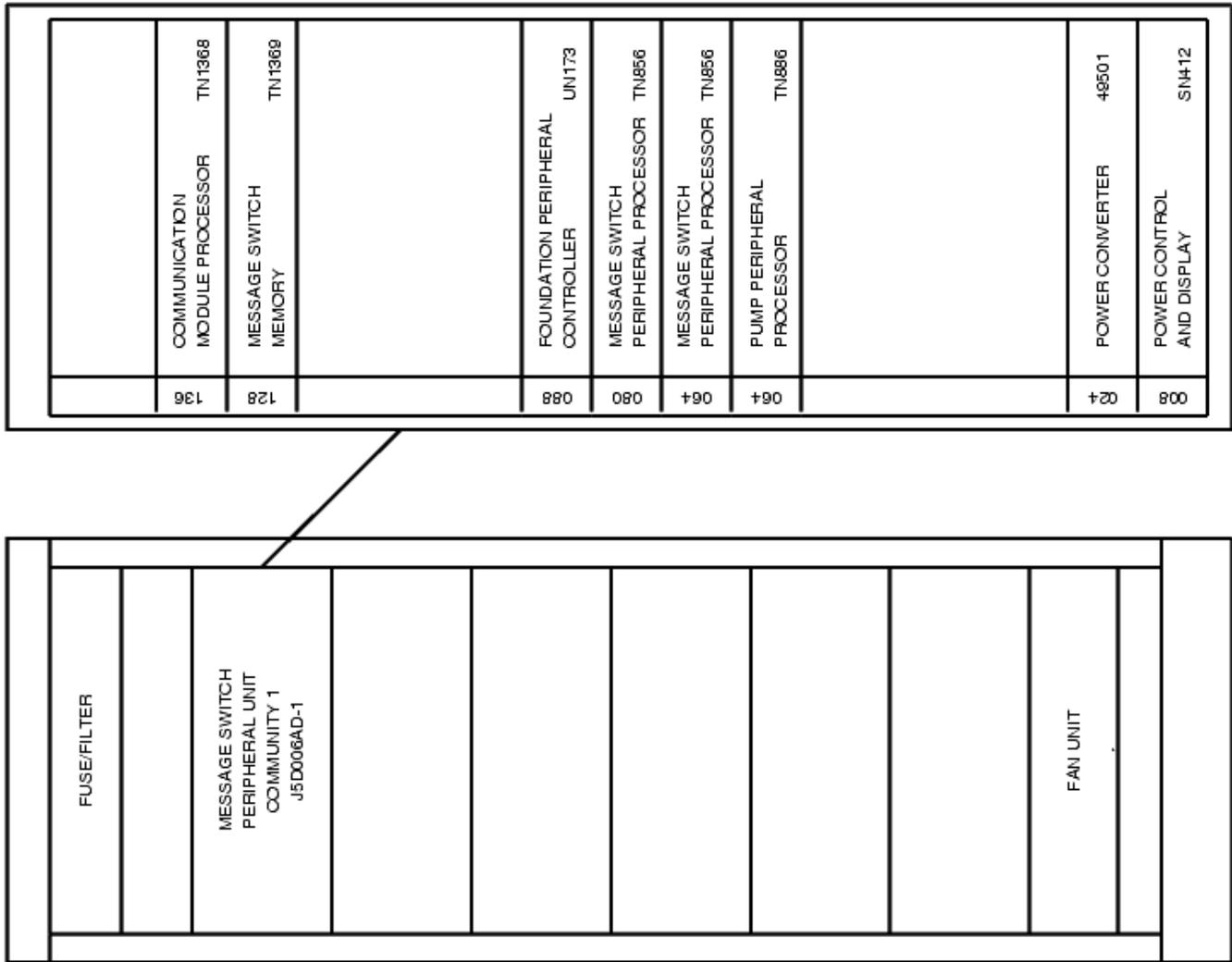


Figure 5.2-12 Message Switch Peripheral Unit Model 2 - J5D006AD-1

5.2.11.2 MSPU (Communities 2 and 3) - J5D006AB-1

The Message Switch Peripheral Units (MSPU) provided for Communities 2 and 3 are located in EQLs 28 and 36, respectively, in the Message Switch Cabinet.

The main purpose of the two MSPUs is to provide switching control for the Module Message Processors (MMPs) assigned to Switching Modules (SMs). The Community 2 MSPU handles even numbered MMPs (0, 2, 4 and 6) assigned to SMs 1 through 32. The Community 3 MSPU handles odd numbered MMPs (1, 3, 5 and 7) assigned to the same SMs.

The MSPU connects directly to the Input/Output Microprocessor Interface (IOMI) located in the MSCU and also with the Dual Message Interface (DMI) located in the CMCU.

Figure 5.2-13 illustrates the location of the MSPUs in the Communication Module Cabinet 1 and the respective circuit packs in the units.

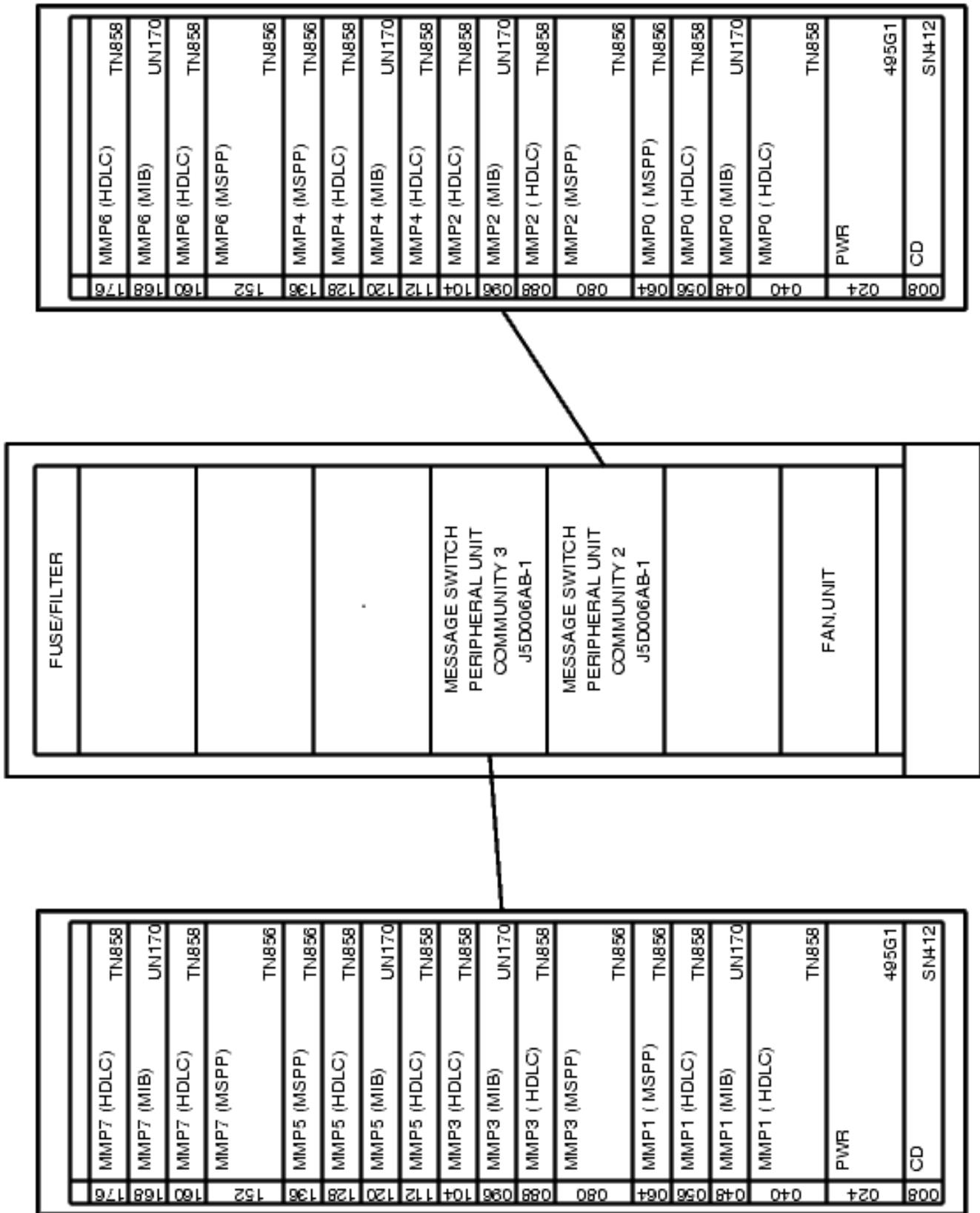


Figure 5.2-13 Message Switch Peripheral Unit - Communities 2 & 3 - J5D006AB-1

5.2.11.3 MSPU3 - J5D020AC-1

The Message Switch Peripheral Unit Model 3 (MSPU3) is fixed located in EQL 53 in all Communication Module Model 2 cabinets. The main function of the MSPU3 is to process the control time slots and send them to the Message Switch Control Unit Model 2 (MSCU2) for switching to the Administrative Module (AM) or to other Switching Modules (SMs). Each MSPU3 is identified by a unique community number.

Each community mounts four Module Message Processors (MMP). Each MMP processes control time slots for eight SMs. The MMPs can be equipped in Service Groups 0 and 1 (Dual MMP arrangement).

Table 5.2-1 identifies the community assignments to cabinets for a fully equipped, 12-cabinet office.

Figure 5.2-14 illustrates the location of the MSPU3 in the Communication Module Cabinets 5 and 6 and the respective circuit packs in the unit.

Table 5.2-1 Community/Cabinet Assignments

SIDE 0 DUAL				SIDE 1 DUAL			
CM2 CABI- NET	MSPU-3 COM- MUNI TY	SER- VICE GRO- UP	MMPs	CM2 CABI NET	MSPU-3 COM- MUNI TY	SERVICE GROUP	MMPs
5	2	0	00,02, 04,06	6	3	0	01,03, 05,07
	3	1	01,03, 05,07		2	1	00,02, 04,06
4	4	0	08,10, 12,14	7	5	0	09,11, 13,15
	5	1	09,11, 13,15		4	1	08,10, 12,14
3	6	0	16,18, 20,22	8	7	0	17,19, 21,23
	7	1	17,19, 21,23		6	1	16,18, 20,22
2	11	0	24,26, 28,30	9	10	0	25,27, 29,31
	10	1	25,27, 29,31		11	1	24,26, 28,30
1	13	0	32,34, 36,38	10	12	0	33,35, 37,39
	12	1	33,35, 37,39		13	1	32,34, 36,38
0	15	0	40,42, 44,46	11	14	0	41,43, 45,47
	14	1	41,43, 45,47		15	1	40,42, 44,46

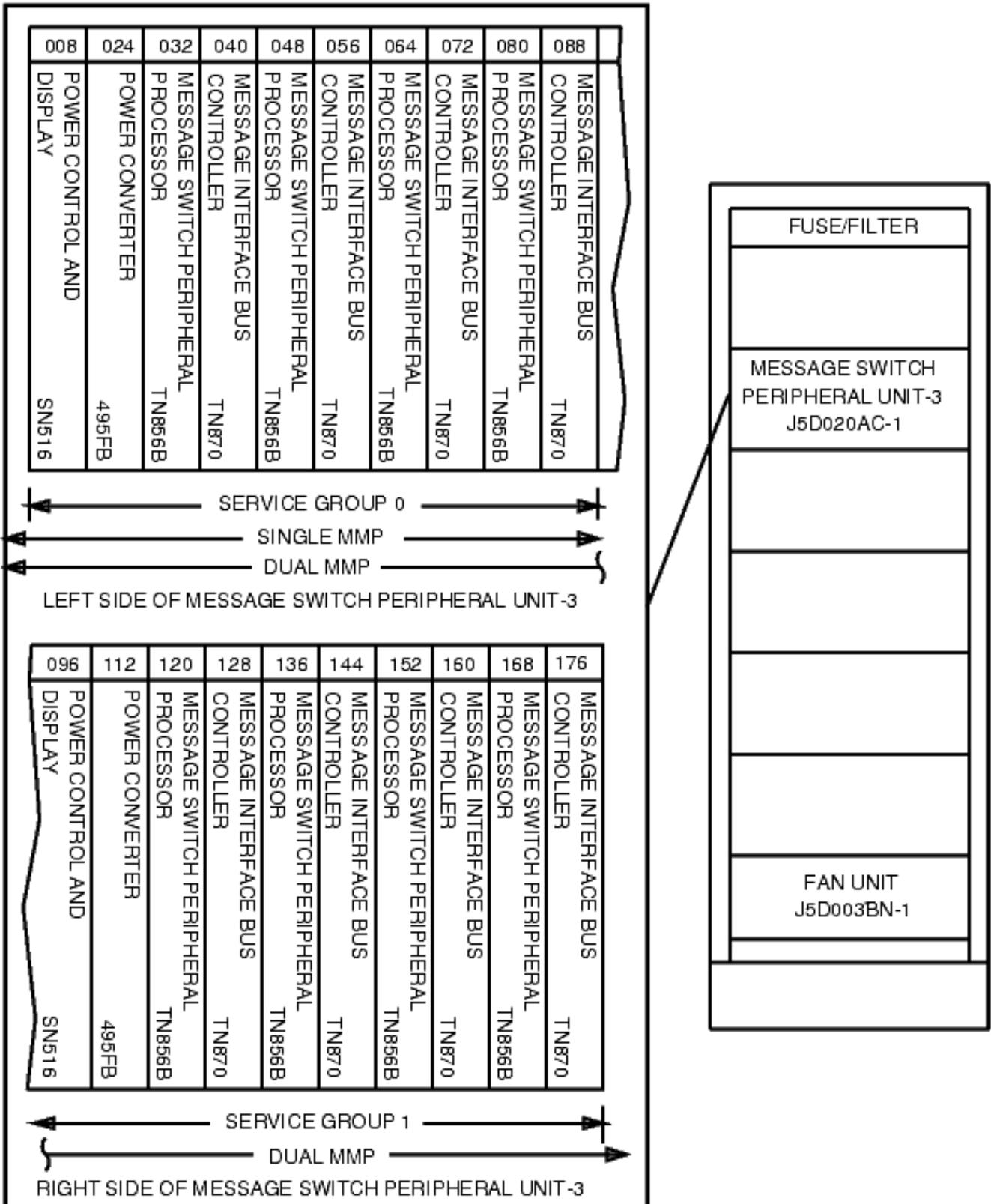


Figure 5.2-14 Message Switch Peripheral Unit - J5D020AC-1

5.2.12 TIME-MULTIPLEXED CONTROL UNIT - J5D001AA-1

The Time-Multiplexed Control Unit (TMCU) is a single-shelf assembly that terminates Network Control and Timing (NCT) links from the Message Interface Clock Unit (MICU) and is equipped with the overall control circuit packs for the Time-Multiplexed Switch (TMS). Positions are provided for seven control and interface packs in addition to space for two power converters.

Figure 5.2-15 illustrates the TMCU and its associated circuit packs.

178	POWER	495FB
096	CLOCK INTERFACE	TN270
086	MESSAGE LINK INTERFACE	TN252
076	TEST BOARD	TN267
068	TMS MAINTENANCE BOARD	TN265
060	TMS CONTROLLER (UP)	TN268
052	TMS INTERFACE	TN269
026	POWER	495FB
008	POWER CONTROL AND DISPLAY	SN412

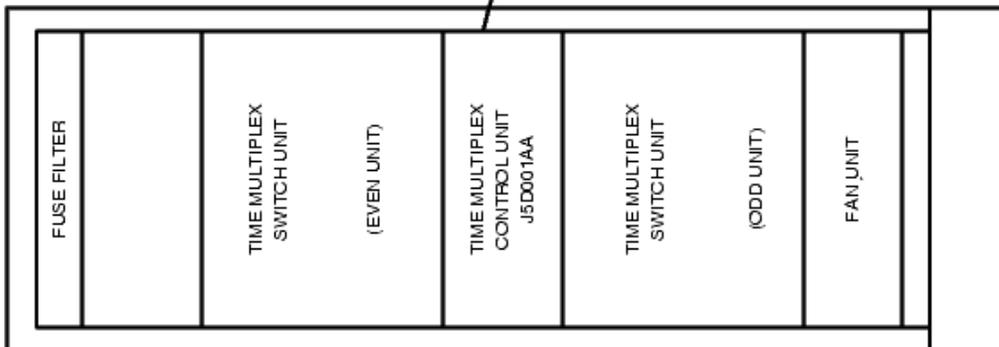


Figure 5.2-15 Time-Multiplexed Control Unit - J5D001AA-1**5.2.13 TIME-MULTIPLEXED SWITCH UNITS****5.2.13.1 Time-Multiplexed Switch Unit (TMSU) - J5D001AB-1**

The Time-Multiplexed Switch Unit (TMSU) is a 2-shelf assembly that contains the fabric, fanout and interface circuit packs to provide control and data paths to appropriate Switching Modules (SMs).

The TMSUs are arranged in an even and odd configuration to serve the associated Network Control and Timing (NCT) links. Positions are provided for 27 circuit packs in the TMSU. Four positions are provided for power converters.

Each link interface is capable of interfacing two NCT links and a fully equipped shelf unit can handle up to 32 links. The TMS fabric is expanded in 4-link increments that are implemented by inserting the 32 or 34 fabric boards. Two fully equipped shelves provide a 32-by-32 TMS.

Figure 5.2-16 illustrates the TMSU and its associated circuit packs.

178	POWER	495FB	178	POWER	495FB
156	L1 7	TN243	156	L1 7	TN243
146	L1 6	TN243	146	L1 6	TN243
136	L1 5	TN243	136	L1 5	TN243
126	L1 4	TN243	126	L1 4	TN243
116	FABRIC	TN242	116	FABRIC	TN242
108	FABRIC	TN242	108	FABRIC	TN242
098	FANOUT	UN74	098	FANOUT	UN74
088	FABRIC	TN242	088	FABRIC	TN242
080	FABRIC	TN242	080	FABRIC	TN242
			080	L1 0	
062	L1 1	TN243	072	L1 1	TN243
052	L1 2	TN243	052	L1 2	TN243
042	L1 3	TN243	042	L1 3	TN243
032	SHELF INTERFACE	TN244	032	SHELF INTERFACE	TN244
018	POWER	495FB	018	POWER	495FB

L1 = LINE INTERFACE

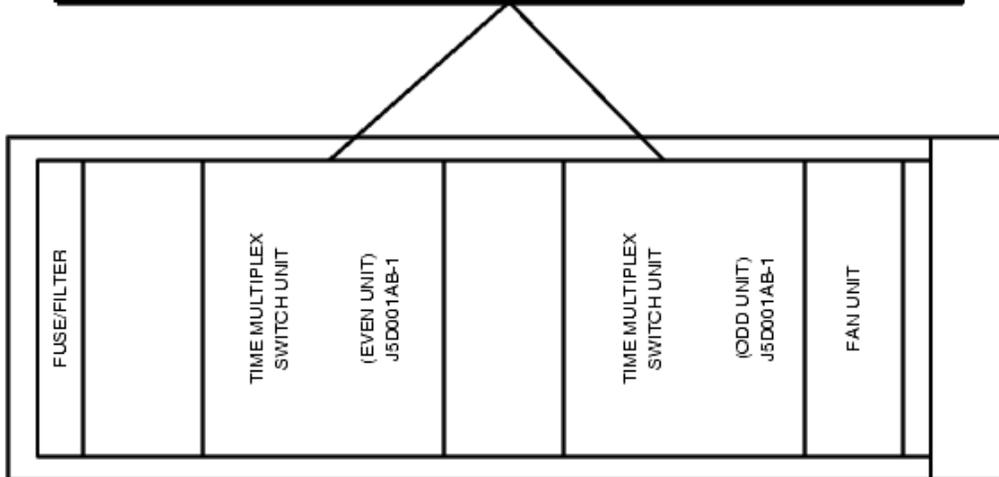


Figure 5.2-16 Time-Multiplexed Switch Unit - J5D001AB-1**5.2.13.2 TMSU Model 2 - J5D020AD-1 and Model 3 - J5D020AG-1**

A basic Communication Module contains at least one Time-Multiplexed Switch Unit Model 2 (TMSU2) or Model 3 (TMSU3) mounted at EQL 36. The TMSU2 and TMSU3 are functionally identical. The TMSU3 is functionally identical to the TMSU2, but has fewer physical components. If a second TMSU is required, mount it at EQL 19. Mount a plenum at EQL 19 if a second TMSU is not required. Side 0 and side 1 (Cabinets 5 and 6) are equipped identically. Figure 5.2-17 illustrates the TMSU2 unit and the circuit packs in it.

The TMSU primarily consists of the following circuit packs:

- Control and display
- Quad-Link Interface (QLI)
- Quad Link Packet Switch (QLPS)-
- Quad Link Interface, Model 2 (QLI2)
- Shelf utility board
- Fabric
- Fabric control

The number of TMSUs required depends upon the number of Switching Modules (SM) in the office and the TMSU arrangement as to single or dual fabric. Fabric arrangement determination is required in order to correctly assign SM links to the CM. Once the TMSU fabric structure is established (single or dual), all later added TMSUs must be of the same arrangement. A particular CM2 frame cannot mix TMSU2 and TMSU3 models; both TMSUs must have the same model number if they are mounted in the same cabinet.

One of the main functions of the TMSU is to terminate (switch) NCT links to and from SMs. Cables carrying input from SMs are connected to optical transceivers located in the line interface area, EQLs 032 through 088. The optical transceiver connectors mount on the TMSU backplane.

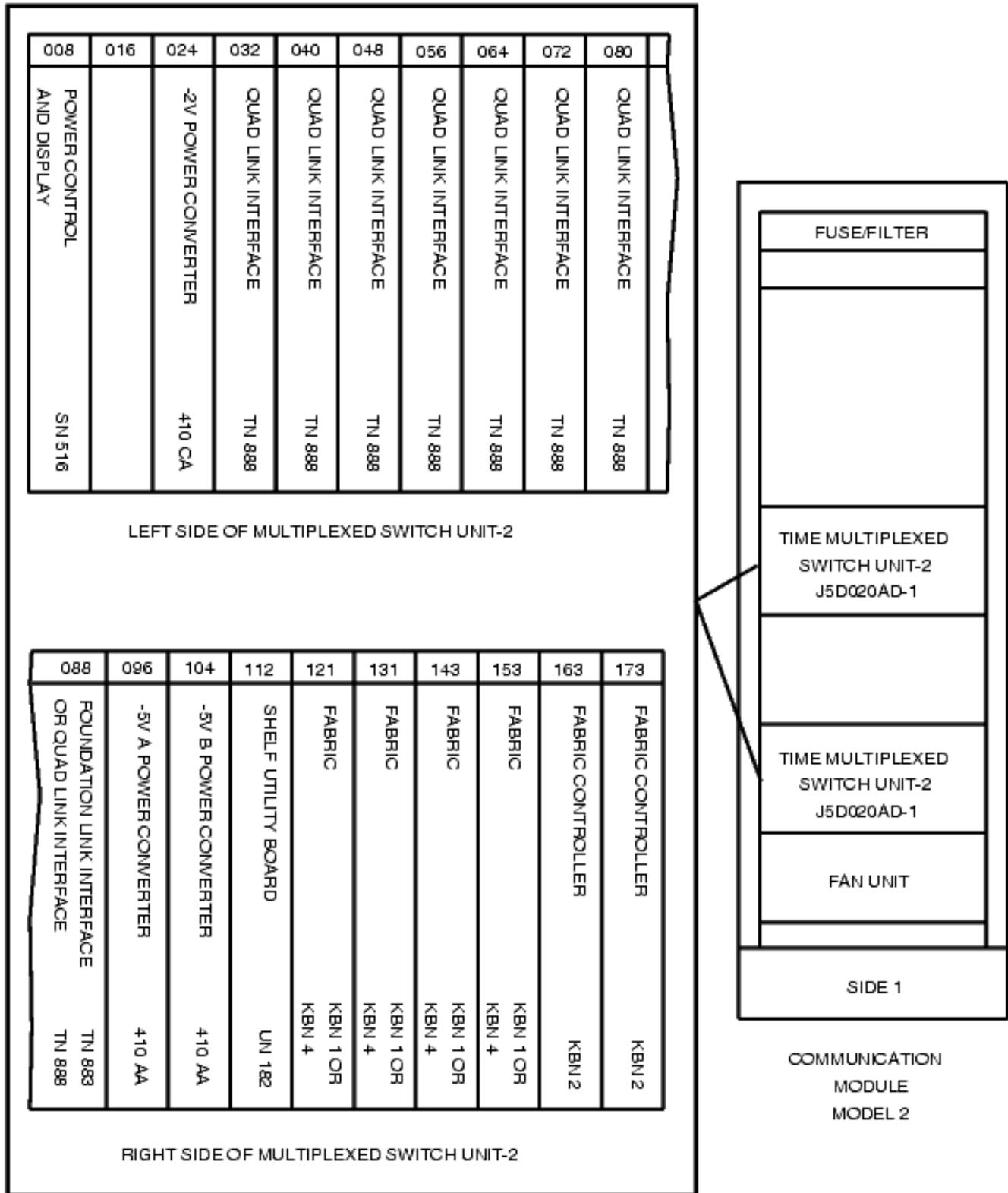
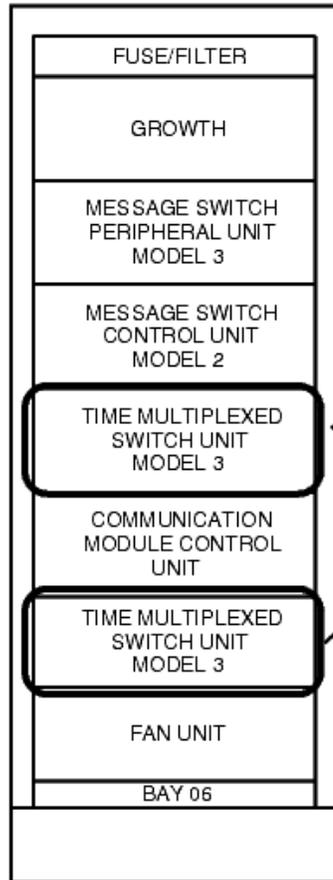


Figure 5.2-17 Time-Multiplexed Switch Unit Model 2 - J5D020AD-1

008	024	032	040	048	056	064	072	080	088	096	104	112	121	131	143	153	163	173
CONTROL AND DISPLAY	POWER CONVERTER	QUAD-LINK INTERFACE	SEE NOTE	POWER CONVERTER	POWER CONVERTER	SHELF UTILITY BOARD		FABRIC BOARD										

MODEL 3 TIME MULTIPLEXED SWITCH UNIT

NOTE:: Position 088 is equipped with a foundation link interface board when the TMSU is located in bay 5 or 6 of the CM2. Otherwise, position 088 is equipped with a quad-link interface board.



COMMUNICATION MODULE 2 CABINET

Figure 5.2-18 Time-Multiplexed Switch Unit Model 3 - J5D020AG-1

Figure 5.2-19 illustrates the interface between SMs and CMs by circuit pack functions.

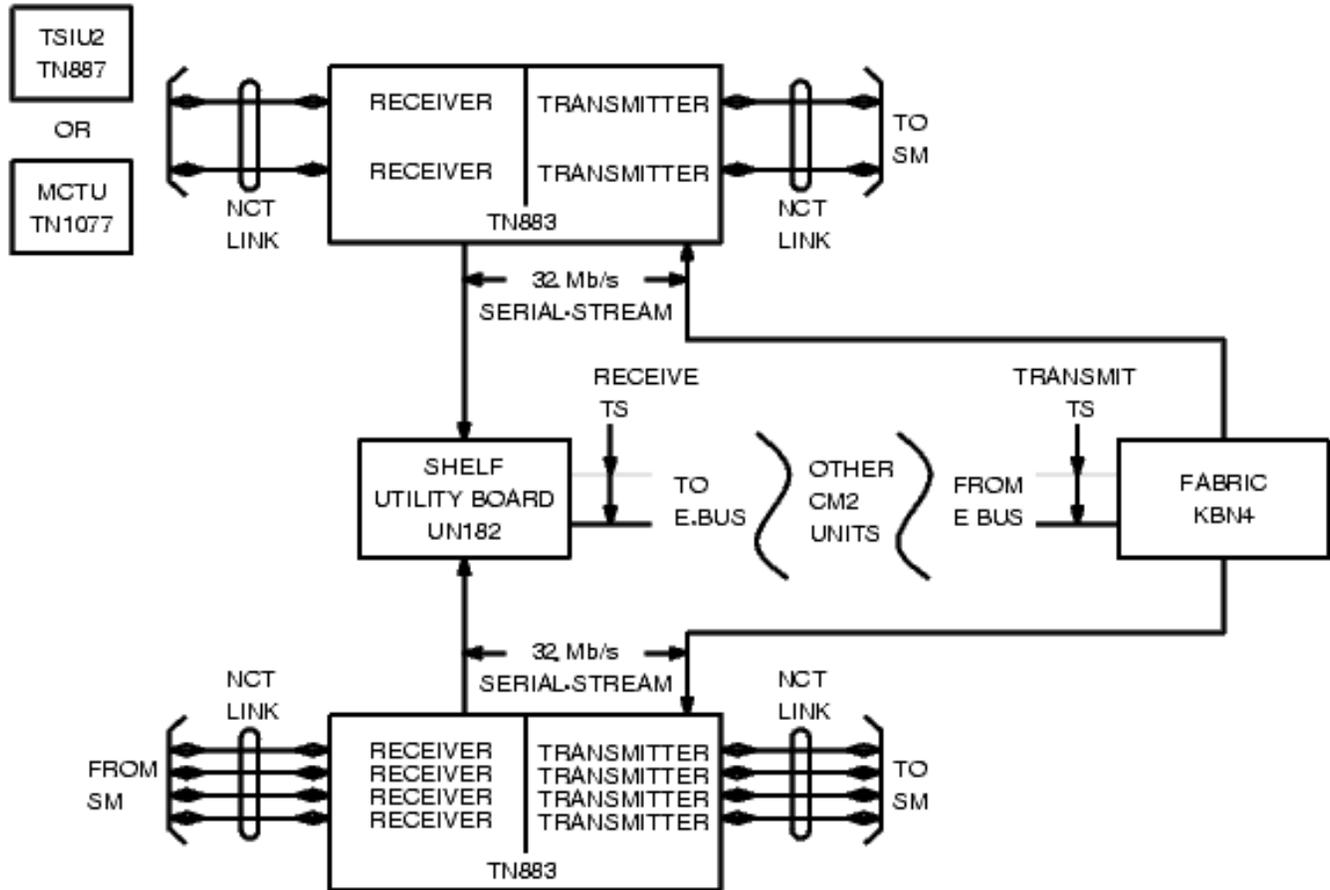


Figure 5.2-19 SM/CM Interface

5.2.13.2.1 Single Fabric Termination Arrangement

If the termination arrangement is Single Switching Fabric, up to 94 SMs can be terminated using six CM cabinets; 5, 4 and 3 on side 0, and 6, 7 and 8 on side 1. Table 5.2-2 lists the cabinet and shelf assignments for the 94 SMs.

Details on how to terminate NCT links from SMs to the TMSU2 for a single fabric arrangement are shown on ED5D500-21-Table AA. A portion of the table, listing up to 30 SMs, appears in Tables 5.2-3 and 5.2-4. Table 5.2-3 provides information for termination of NCT links on assigned SMs. The table is divided into half, with NCT links OA (even time slots) and OB (odd time slots) connected to CM2, side 1. The direct connections are between the selected SM Module Controller Time Slot Interchanger Unit (MCTU) Dual Link Interface (TN1077E) and transmitters and receivers at specific SM locations. Note that SM numbers are not entered on the table. These assignments are made locally. Table 5.2-3 shows the three most popular SMC units: TSIU2, MCTU and MCTU2.

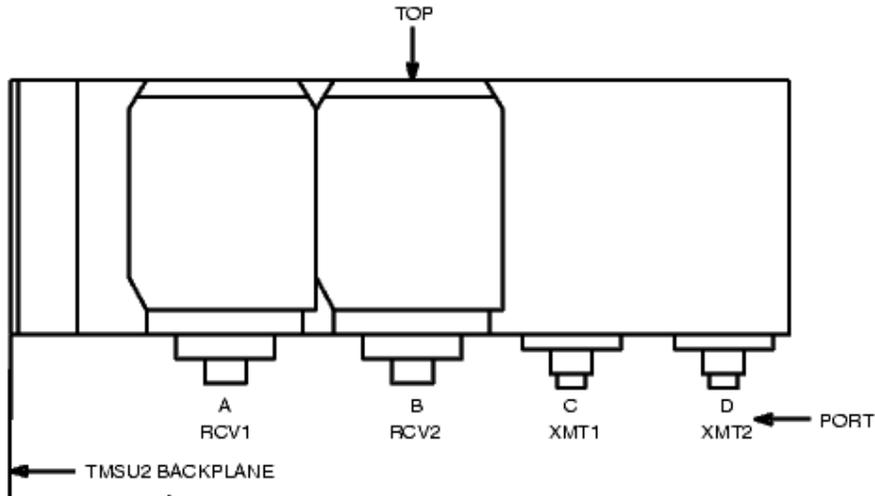
Table 5.2-4 shows how SM NCT links terminate on the TMSU transceivers. Looking at the table columns from the left, the first column shows SM numbering, the second column shows the 9-digit EQL identification for CM2 side 0 and the third column shows the EQL identification for CM2 side 1. The 9-digit EQL number is defined as follows:

- Digit 1 = CM2 cabinet number (can be two digits)
- Digits 2 & 3 = Inches shelf is from floor (36 or 19)

- Digits 4, 5, & 6 = Circuit pack position in unit (EQL) (088 to 032)
- Digit 7 = Column
- Digits 8 & 9 = Row.

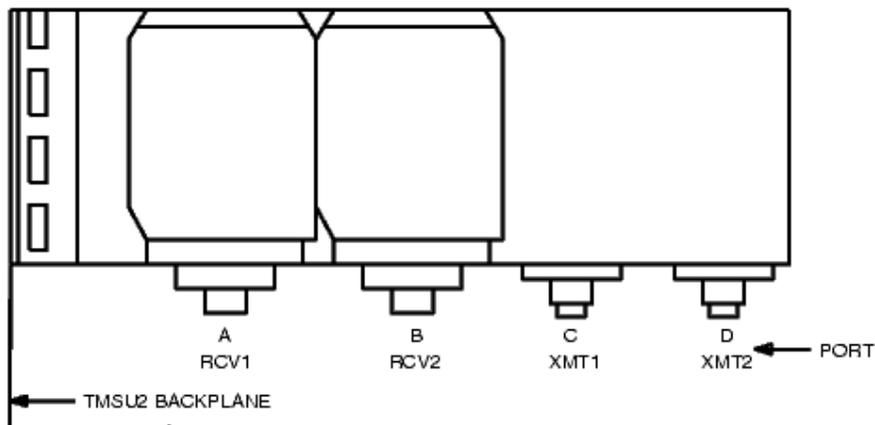
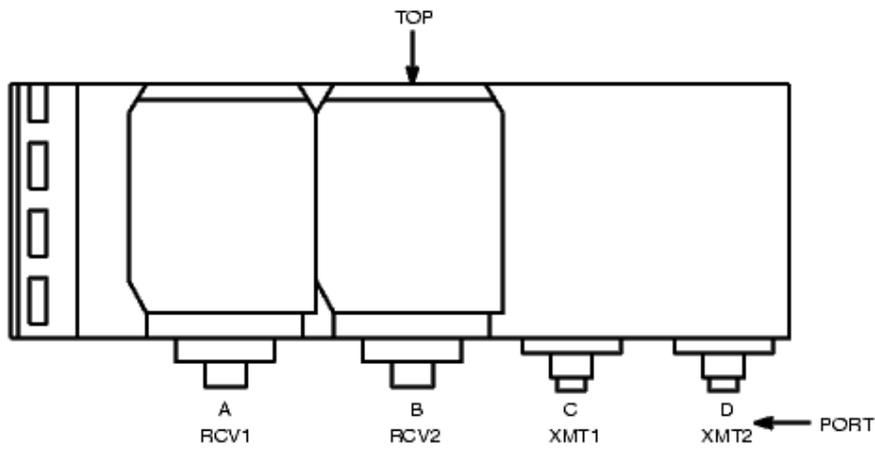
The top section of the table shows how the NCT links are connected to the transceivers. A designated cable connects an EQL in the SM to an EQL in the CM2.

The Foundation Link Interface (FLI) circuit pack (TN883) terminates SM1, with both odd and even NCT links connected to one 1A transceiver. A total of 512 time slots are handled. Quad Link Interface (QLI) circuit packs, TN888, can terminate four NCT links, both odd and even, and handle 1024 time slots through two 1A transceivers. The TN883 FLI circuit packs appear only in CM cabinets 5 and 6. Refer to Figure 5.2-20 for the termination to the 1A transceiver.



1A TRANSCEIVER

TN883 TERMINATES ONE 1A TRANSCEIVER



TN888 TERMINATES TWO 1A TRANSCEIVERS

Figure 5.2-20 1A Transceiver

Table 5.2-2 SM Cabinet and Shelf Assignments for the 94 SMs

CM2 CABINET	TMSU2 SHELF	SWITCHING MODULES
5 & 6	36	SM1 to SM15
5 & 6	19	SM16 to SM30
4 & 7	36	SM31 to SM46
4 & 7	19	SM47 to SM62
3 & 8	36	SM63 to SM78
3 & 8	19	SM79 to SM94

Table 5.2-3 NCT Link Terminations On SMS

Cable Desig	EVEN NCT LINK		ODD NCT LINK		EVEN NCT LINK		ODD NCT LINK	
	JL9	JL11	JL13	JL15	JL10	JL12	JL14	JL16
NCT Links	OA		OB		1A		1B	
	XMTR	REC	XMTR	REC	XMTR	REC	XMTR	REC
SM ()	145-	145-	145-	145-	145-	145-	145-	145-
SMC	084-	084-	084-	084-	100-	100-	100-	100-
TSIU2 (TN 877)	132	145	113	100	132	145	113	100
SM ()	136-	136-	136-	136-	136-	136-	136-	136-
SMC 1	084-	084-	084-	084-	098-	098-	098-	098-
MCTU (TN 1077)	332	345	313	300	332	345	313	300
SM ()	119-	119-	119-	119-	128-	128-	128-	128-
SMC 1	156-	156-	156-	156-	156-	156-	156-	156-
MCTU (TN 1077E)	332	345	313	300	332	345	313	300

Table 5.2-4 SM NCT Link Terminations On TMSU Transceivers

SM NO.	CM2 PORTS							
	CM2 "0" SIDE				CM2 "1" SIDE			
	REC1 A	XMT1 C	REC2 B	XMT2 D	REC1 A	XMT1 C	REC2 B	XMT2 D
SM1		536-088-145				636-088-145		
SM2		536-080-145				636-080-145		
SM3		536-080-113				636-080-113		
SM4		536-072-145				636-072-145		
SM5		536-072-113				636-072-113		
SM6		536-064-145				636-064-145		
SM7		536-064-113				636-064-113		
SM8		536-056-145				636-056-145		
SM9		536-056-113				636-056-115		
SM10		536-048-145				636-048-145		
SM11		536-048-113				636-048-113		
SM12		536-040-145				636-040-145		
SM13		536-040-113				636-040-113		
SM14		536-032-145				636-032-145		
SM15		536-032-113				636-032-113		
SM16		519-088-145				619-088-145		
SM17		519-080-145				619-080-145		
SM18		519-080-113				619-080-113		

SM19	519-072-145	619-072-145
SM20	519-072-113	619-072-113
SM21	519-064-145	619-064-145
SM22	519-064-113	619-064-113
SM23	519-056-145	619-056-145
SM24	519-056-113	619-056-115
SM25	519-048-145	619-048-145
SM26	519-048-113	619-048-113
SM27	519-040-145	619-040-145
SM28	519-040-113	619-040-113
SM29	519-032-145	619-032-145
SM30	519-032-113	619-032-113

5.2.13.2.2 Dual Fabric Termination Arrangement

If the termination arrangement is Dual Switching Fabric, up to 190 SMs can be terminated using 12 CM cabinets; 5 to 0 on side 0 and 6 to 12 on side 1. Table 5.2-5 lists the cabinet and shelf assignments for the 190 SMs.

Figure 5.2-3 illustrates the CM2 fully loaded with 12 cabinets.

Table 5.2-5 SM Cabinet and Shelf Assignments for the 190 SMs

CM2 CABINET	TMSU2 SHELF	SWITCHING MODULES
5 & 6	36 & 19	SM 1 to 30
4 & 7	36 & 19	SM 31 to 62
3 & 8	36 & 19	SM 63 to 94
2 & 9	36 & 19	SM 95 to 126
1 & 10	36 & 19	SM 127 to 158
0 & 11	36 & 19	SM 159 to 190

Even NCT links for each SM terminate on Shelf 36 and odd links terminate on Shelf 19. If QLPS is present, Network 0 is Shelf 36; Network 1 is located on Shelf 19. The QLPS circuit pack must be in the same slot number. A Foundation Link Interface (FLI) circuit pack (TN883) terminates even NCT links for SM1 and SM2 on two CM2 1A transceivers. The NCT links for the remaining SMs terminate on Quad Link Interface (QLI) circuit packs (TN888), with even links on Shelf 36 and odd links on Shelf 19. CM2 cabinets 5 and 6 can terminate up to 30 SMs in the dual fabric arrangement. Note that FLI packs appear only in cabinets 5 and 6.

Details on how to terminate NCT links from SMs to the CM2 TMSU2 are shown on ED-5D500-21, TABLES AB and AB-1. Portions of these tables appear in Tables 5.2-3 and 5.2-6. Contents of Table 5.2-3, describing Single Fabric assignments, also apply to Dual Fabric arrangements.

Table 5.2-6 is a two-part table, one part lists odd numbered SM to CM connections and the other part lists even numbered SM to CM connections.

5.2.13.2.3 CM Diagnostic Testing

Diagnostic phase descriptions for the CMs are in Table 5.2-7.

Table 5.2-6 Odd and Even Numbered SM to CM Connections

SM NO.	ODD NUMBERED CM2 PORTS			
	CM2 "0" SIDE		CM2 "1" SIDE	
	REC1 A AND XMT1 C	REC1 A AND XMT1 C	REC1 A AND XMT1 C	REC1 A AND XMT1 C
SM1	536-088-145	519-088-145	636-088-145	619-088-145
SM3	536-080-145	519-080-145	636-080-145	619-080-145
SM5	536-080-113	519-080-113	636-080-113	619-080-113
SM7	536-072-145	519-072-145	636-072-145	619-072-145
SM9	536-072-113	519-072-113	636-072-113	619-072-113
SM11	536-064-145	519-064-145	636-064-145	619-064-145
SM13	536-064-113	519-064-113	636-064-113	619-064-113
SM15	536-056-145	519-056-145	636-056-145	619-056-145
SM17	536-056-113	519-056-113	636-056-113	619-056-113
SM19	536-048-145	519-048-145	636-048-145	619-048-145

SM21	536-048-113	519-048-113	636-048-113	619-048-113
SM23	536-040-145	519-040-145	636-040-145	619-040-145
SM25	536-040-113	519-040-113	636-040-113	619-040-113
SM27	536-032-145	519-032-145	636-032-145	619-032-145
SM29	536-032-113	519-032-113	636-032-113	619-032-113
EVEN NUMBERED CM2 PORTS				
SM NO.	CM2 "0" SIDE		CM2 "1" SIDE	
	REC2 B AND XMT2 D			
SM2	536-088-145	519-088-145	636-088-145	619-088-145
SM4	536-080-145	519-080-145	636-080-145	619-080-145
SM6	536-080-113	519-080-113	636-080-113	619-080-113
SM8	536-072-145	519-072-145	636-072-145	619-072-145
SM10	536-072-113	519-072-113	636-072-113	619-072-113
SM12	536-064-145	519-064-145	636-064-145	619-064-145
SM14	536-064-113	519-064-113	636-064-113	619-064-113
SM16	536-056-145	519-056-145	636-056-145	619-056-145
SM18	536-056-113	519-056-113	636-056-113	619-056-113
SM20	536-048-145	519-048-145	636-048-145	619-048-145
SM22	536-048-113	519-048-113	636-048-113	619-048-113
SM24	536-040-145	519-040-145	636-040-145	619-040-145
SM26	536-040-113	519-040-113	636-040-113	619-040-113
SM28	536-032-145	519-032-145	636-032-145	619-032-145
SM30	536-032-113	519-032-113	636-032-113	619-032-113

Table 5.2-7 CM Diagnostic Phase Descriptions

DIAGNOSTIC ID	PHASE	DESCRIPTION/ WHAT IS TESTED	PR NAME
COMMUNICATIONS MODULE PROCESSOR (CMP) (CM)	1	Tests interface between the MSCU (IOMI) and TN1368 core board.	AM:DNC3BPIP1
	2	Tests IP side (including DAM, DRAMs) of TN1368 core board.	CMP:CMPPMSG
	3	Tests the AP side of the TN1368 core board.	CMP:CMPPMSG CMP:CMPP
	4	Tests AP-side interface of the TN1368 core board to the TN1369 external memory board.	CMP:CMPPMSG CMP:CMPP
	5	Tests memory pump of the TN1368 and TN1369.	CMP:CMPPMSG CMP:CMPP
	11	(Demand phase only). More exhaustive tests of memory devices on TN1368 and TN1369 boards. This phase should be run when there are reports of CMP memory errors but the normal CMP diagnostic phases above run ATP.	CMP:CMPPMSG CMP:CMPP
	12	(Demand phase only). This phase runs same test sequences as phase 2 except each sequence is run as a separate "segment" to provide more data on failures. This phase is expected to be used primarily in the factory where data may help in component-level fault isolation.	CMP:CMPPMSG CMP:CMPP
	13	(Demand phase only). This phase runs same test sequences as phase 3 except each sequence is run as a separate "segment" to provide more data on failures. This phase is	CMP:CMPPMSG CMP:CMPP

	14	expected to be used primarily in the factory where data may help in component-level fault isolation. (Demand phase only). This phase runs same test sequences as phase 4 except each sequence is run as a separate ``segment" to provide more data on failures. This phase is expected to be used primarily in the factory where data may help in component-level fault isolation.	CMP:CMPPMSGS CMP:CMPP
	15	expected to be used primarily in the factory where data may help in component-level fault isolation. (Demand phase only). This phase runs same test sequences as phase 5 except each sequence is run as a separate ``segment" to provide more data on failures. This phase is expected to be used primarily in the factory where data may help in component-level fault isolation.	CMP:CMPPMSGS CMP:CMPP
FOUNDATION PERIPHERAL CONTROLLER (FPC) (CM1 AND CM2)	1	Tests the interface between the MSCU and the microprocessor board of the FPC.	AM:DNC3BFPC1
	2	Tests the controller board (TN856) of the FPC.	FPC:DNCFP22-25
	3	Tests the application board (UN173) of the FPC.	FPC:DNCFP32-35
LINE INTERFACE (LI) (CM1)	1	Tests the communication interface between the FPC and LI, and the ability to read and write the LI control registers.	FPC:DNCL01
	2	Tests the A and B links framing, transmit and receive parity, the parity to/from the FPC, and the phase lock loop clock slip.	FPC:DNCL02
	3	Tests the A and B link receive message time slot parity, and the A and B link transmit message time slot parity.	FPC:DNCL03
MESSAGE INTERFACE (MI) (CM1)	1	Tests the interface from host FPC to MI under test, the major buses between MI boards, and the access of common registers.	FPC:DNCM01
	2	Tests the time slot switching functions of the TN861 board.	FPC:DNCM02
	3	Tests the CPI time slot matching functions of the TN861 board.	FPC:DNCM03
	4	Tests the clocking functions of the TN860 and TN859 boards.	FPC:DNCM04
	5	Tests the TN862 clocking, the TN861 gate array, the MI interrupt lead to the FPC, and the CDAL link to the opposite FPC.	FPC:DNCM05
	6	Tests the CPI loopback and MIBs from the PCs.	FPC:DNCM06
MESSAGE INTERFACE	1	Tests the interface from the host FPC to the MI under test and the	FPC:DNCDMI01

(MI) (CM2)	2	major buses between the MI boards and the access of source registers. Tests all clocks of the MI.	FPC:DNCDMI02
	3	Tests the time slot switching control and memory and the MIB parity by using associated PPC/MMPs as the host circuit.	FPC:DNCDMI03
	4	Tests the CPI time slot matching functions of the UN187 board.	FPC:DNCDMI04
	5	Tests the local transmission of the CPI diagnostic message.	FPC:DNCDMI05
	6	Tests the external transmission of CPI diagnostic messages using TMS loopback circuitry.	FPC:DNCDMI06
	7	(Demand phase only). Tests the MIBs by using the PPC/MMPs as host circuits.	FPC:DNCDMI07, MMP: DNC2MMP52-56
	MODULE MESSAGE PROCESSOR (MMP) (CM1)	1	Tests the interface between the MSCU PIC and the microprocessor board of the MMP.
2		Tests the controller board (TN856) of the MMP.	MMP:DNCMMP22-25
3		Tests the application board (UN170) of the MMP.	MMP: DNCMMP32-34
4		Tests the application board (TN858A) of the MMP.	MMP: DNCMMP42-44
5		Tests the application board (TN858B) of the MMP.	MMP: DNCMMP52-56
6		(Demand phase only). Tests the MMPs' interfaces to both sides of the ONTC (if in-service). Use this phase only when fault recovery reports troubles with the MMP, but normal diagnostic is ATP (all tests passed).	MMP: DNCMMP62-63
7		(Demand phase only). Tests the internal data transfer using DMA - SDLC. This is used to find intermittent failures of the DMA and SDLC chips.	MMP: DNCMMP72-73
MODULE MESSAGE PROCESSOR (MMP) (CM2)	1	Tests the interface between the MSCU PIC and the micro-processor board of the MMP.	AM: DNC3BMMP1
	2	Tests the controller board (TN856) of the MMP.	MMP: DNC2MMP22-25
	3	Tests the application board (TN870) of the MMP.	MMP: DNC2MMP32-36
	4	Tests the application board (TN870) of the MMP and the MIB from that MMP by looping data at the TMS.	MMP: DNC2MMP42-47
MESSAGE SWITCH CONTROLLER UNIT	1	Tests the interface between the Duplex Dual Serial Bus Selector (DDSBS) and the Dual Serial Channel (DSCH) - TN69 and UN9.	AM:DNCMSCU

(MSCU) (CM1)	2	Tests the interface between the Bus Interface Controller (BIC) and the DDSBS - TN70 and TN69.	AM:DNCMSCU
	3	Tests the BIC and BIC/PIC interface - TN70 and TN61.	AM:DNCMSCU
	4	Tests the Peripheral Interface Controller (PIC) - TN61, TN84A and B.	AM:DNCMSCU
	5	Tests the Input/Output Microprocessor Interfaces (IOMIs) - UN25, TN61, TN84A and B.	AM:DNCMSCU
	6	Tests the interface between the IOMIs and the PC communities - UN25 and TN 856.	AM:DNCMSCU
	MESSAGE SWITCH CONTROLLER UNIT (MSCU) (CM2)	1	Tests the power switch monitor (PSM) boards - SN516, 495FB, and UN33.
2		Tests the Duplex Dual Serial Bus Selector (DDSBS) TN69.	AM:DNCMSCU
3		Tests the Bus Controller Interface (BIC) - TN70.	AM:DNCMSCU
4		Tests the BIC and BIC/PIC interfaces - TN70 and UN178.	AM:DNCMSCU
5		Tests the Peripheral Interface Controller (PIC) - UN178 and UN199.	AM:DNCMSCU
6		Tests the interface between the Input/Output Microprocessor Interfaces (IOMIs) and the PIC and the power circuitry of the IOMIs - UN25 and UN178.	AM:DNCMSCU
7		Tests the interface between the IOMIs and the PC communities - UN25 and TN856.	AM:DNCMSCU
NETWORK CLOCK NC1 (CM1)	1	Tests the communication interface between the host FPC and NC, and the CLRT subunit on the controller board.	FPC:DNCN01
	2	Tests the CCB subunit on the controller board.	FPC:DNCN02
	3	Tests the microprocessor portion of the controller board.	FPC:DNCN03
	4	Tests the synchronizer board of the NC - (TN245 or TN249).	FPC:DNCN04
	5	Tests the DPLL board and the operation of the NC in its entirety.	FPC:DNCN05
NETWORK CLOCK NC2 (CM2)	1	Tests the communication interface between the host FPC and NC, and CLRT subunit on the controller board.	FPC:DNC2NC01
	2	Tests the CCB subunit on the controller board.	FPC:DNC2NC02
	3	Tests the microprocessor portion of the controller board.	FPC:DNC2NC03
	4	Tests the synchronizer boards (0 and 1) of the NC.	FPC:DNC2NC04

	5	Tests the DPLL board and the operation of the NC in its entirety.	FPC:DNC2NC05
NETWORK CLOCK (CM2)	1	Tests the communication interface between the host FPC and NC, and the CLRT subunit on the controller board.	FPC:DNC2NC01
	2	Tests the CCB subunit on the controller board.	FPC:DNC2NC02
	3	Tests the microprocessor portion of the controller board.	FPC:DNC2NC03
	4	Tests the synchronizer boards (0 and 1) of the NC.	FPC:DNC2NC04
	5	Tests the DPLL board and the operation of the NC in its entirety.	FPC:DNC2NC05
PUMP PERIPHERAL CONTROLLER (PPC) (CM1 and CM2)	1	Tests the interface between the MSCU PIC and the microprocessor board of the PPC.	AM:DNC3BPPC1
	2	Tests the controller board (TN856) of the PPC.	PPC:DNCPPC22-25
	3	Tests the application board (TN886) of the PPC.	PPC:DNCPPC32-38
	4	Tests the Metallic Interface Buses (MIBs) by looping data out of PPC via MIB through MI 0, LI 0, and TMS 0 and back.	PPC:DNCPPC42-43
QUAD-LINK PACKET SWITCH GATEWAY PROCESSOR (QGP) (CM2)	1	Tests power, the interface between the MSCU and QGP processor board, and RAM that both the MSCU and QGP can access (DAM).	
	2	Tests the QGP IP processor.	
	3	Tests the QGP AP processor.	
	4	Tests the interface between the QGP processor board and the QGP link board, and the QGP link board and the QGL cable.	
	5	Verifies that the QGP can be pumped.	
QUAD-LINK PACKET SWITCH (QLPS) (CM2)	1	Tests the interface between the TMS controller and the QLPS board, BIST, registers, and error propagation.	
	2	Tests error detection with and without sending packets through the TMS fabric.	
	3	Tests receive detection of Level 2 errors, QGL connectivity, packet RAM (PRAM), routing RAM (RR), stress testing (many packets), tests to check TMS fabric between the QLPS, all QLI/QLI2 boards in the TMS, and any miscellaneous boards that don't belong to any of the previous groups.	

TIME MULTIPLEXED SWITCH (TMS) (CM1)	1	Tests the power and access to the TMS interface and verifies communication to TMS through the TMS interface (TN269).	FPC:DNCTM01
	2	Tests the TMS controller boards (TN269, TN268, and TN265).	FPC:DNCTM02
	3	Tests the TMS controller's RAM memory, PROM memory, and microprocessor circuitry (TN268).	FPC:DNCTM03
	4	Tests the TMS maintenance board (TN265).	FPC:DNCTM04
	5	Tests the TMS interface to the host FPC and the interface to the microprocessor (TN269).	FPC:DNCTM05
	6	Tests the TMS interface (TN269), the TMS clock board (TN270), and the TMS maintenance flip-flop.	FPC:DNCTM06
	7	Tests the bi-directional serial data link and the error source lead between the TMS interface (TN269) and the test board (TN267).	FPC:DNCTM07
	8	Tests the test board (TN267) error source register and the test generating circuitry.	FPC:DNCTM08
	9	Tests the bi-directional serial data link and the error source lead between the TMS interface (TN269) and the message link interface (TN252).	FPC:DNCTM09
	10	Tests the message link interface's ability to detect control parity and bad board IDs - as flagged on the message link interface error source register.	FPC:DNCTM10
	11	Tests the bi-directional serial data link and the error source lead between the TMS interface (TN269) and the shelf interface (TN244).	FPC:DNCTM11
	12	Tests the TMS shelf interface (TN244).	FPC:DNCTM12
	13	Tests the bi-directional serial data link between the shelf interface (TN244) and the fabric (TN242) and the error source lead from the fabric to the shelf interface.	FPC:DNCTM13
	14	Tests the bi-directional serial data link between the shelf interface (TN244) and the link interface (TN243) and the error source lead from the link interface to the shelf interface.	FPC:DNCTM14
	15	Tests the error source registers, error source lead, and memory of the fabric (TN242).	FPC:DNCTM15
	16	Tests the link interface's (TN243) ability to detect control parity and bad board IDs.	FPC:DNCTM16

	17	Tests the message link interface (TN252) and link interface boards (TN254) by sending various data patterns via the test board (TN267).	FPC:DNCTM17
	18	Tests are the same as phase 17.	FPC:DNCTM18
	19	Tests are the same as phase 17.	FPC:DNCTM19
	20	Tests are the same as phase 17.	FPC:DNCTM20
	21	Tests the fabric data paths for switch half A - (TN252 and TN243).	FPC:DNCTM21
	22	Tests the fabric data paths for switch half B - (TN252 and TN243).	FPC:DNCTM22
	23	Tests the message link interface's (TN252) fabric (TN242) and fanout (UN74).	FPC:DNCTM23
	24	Tests the optical link receiver on the message link interface (TN252).	FPC:DNCTM24
	25	(Manual diagnosis only). Tests the NCT links to the local TRCU (TN1344) circuits that interface links to Optically Remote Modules (ORMs).	FPC:DNCTMS25
	27	(Demand phase for factory or growth testing only). Tests the NCT link receivers and transmitters. This phase requires fiber looparound straps installed either at the TMS end or the SM end of the NCT link.	FPC:DNCCLN3
TIME MULTIPLEXED SWITCH (TMS) (CM2) (CM2C)	1	Tests the Power Switch Monitor (PSM) boards and the interface between the FPC and the TMS2.	FPC:DNC2FMS01 TMS:DNC2TMS01
	2	Tests the operation of the TMS2 controller (TN884, UN183, and TN881) and tests the controller's CIC unit towards switching units.	FPC:DNC2FMS02 TMS:DNC2TMS02
	3	Tests communications between the controller and all UN182, KBN2, TN883, and TN888 boards and their registers. For the 5ESS [®] -2000 Switch CDX, the UN182, KBN2, TN1830, and TN888 boards are changed to the TN1812; TN1830 boards, for the CM2C.	FPC:DNC2FTMS03 TMS:DNC2TMS03
	4	Tests error detecting, propagational masking in KBN1/KBN5, KBN2, TN883, and TN884 boards. For the 5ESS [®] -2000 Switch CDX, the TN883 and TN884 boards are changed to the TN1813 and TN1830 boards for the CM2C.	FPC:DNC2FTMS04 TMS:DNC2TMS04
	5	Tests the access to all control registers of each FCB, QLI, and SUB board in switch units. Tests data paths in switch units using test function.	FPC:DNC2FMS05 TMS:DNC2TMS05
	6	Tests the operation of the FCB and FABs ESR/MSK. Tests AUTISS function, KBN2 sequencing, and all	FPC:DNC2FMS06 TMS:DNC2TMS06

11	fabric paths. (Demand phase for factory or growth testing only). Tests the NCT link receivers and transmitters. This phase requires fiber looparound straps installed either at the TMS end or SM end of the NCT link.	FPC:DNC2FMS11 TMS:DNC2TMS11
12	Tests the TMS fabric load/stress test.	FPC:DNC2FMS12 TMS:DNC2TMS12
13	(Demand phase for factory or growth testing only). Tests the NCT link receivers and transmitters. All links must have looparound straps installed either at the TMS or SM end of the NCT links. All links are tested concurrently. This phase is a more exhaustive test than Phase 11.	FPC:DNC2FMS13 TMS:DNC2TMS13
14	(Demand phase to be run when an earlier phase fails with Note No. 36 in its Suspected Faulty Equipment List). It does sectionalized testing of the E-bus circuits to produce a more accurate Suspected Faulty Equipment List.	FPC:DNC2FMS14 TMS:DNC2TMS14
15	A manual diagnostic phase that does NCT link looparound tests from the TMS link board (TN888) to the local TRCU (TN1344) circuits interfacing links to Optically Remote Modules (ORMs).	FPC:DNC2FMS15 TMS:DNC2TMS15

5.3 SWITCHING MODULES

5.3.1 INTRODUCTION

This section contains maintenance support information about the various switching module (SM) configurations. While there is no "typical" SM (because of differences among local office requirements), basic modules are presented to provide reasonable coverage. The diagnostic phase descriptions for the SM are also included in this section.

Figures 5.3-1 and 5.3-2 consecutively illustrate an SM and a loaded SM.

Units within the SM are identified by model numbers (J-drawings) usually stamped on the plastic strip mounted on the cabinet frame above the unit. If the number is not present, get it from office records and apply it to the strip for future reference.

For diagnostic execution input message and POKE command source information, refer to the following documents:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-700, *Input Message Manual*
- 235-600-750, *Output Message Manual*.

The change in standard media for the Program Listings from microfiche to on-line makes it necessary to clarify our terminology. The use of the PR FUNCTION NAME reference used in the microfiche listings does not apply to the on-line listings. When using the on-line listings, the FUNCTION NAME reference is used in conjunction with the search for information on specific functions.

The program listings available via networked service are referred to as the , 235-410-220, *Electronic Media Networked Service (EMNS) Access to On-Line Program Listings*. This "document" is actually a dial-up service that allows the user to choose from a menu of selections which includes queries that allow a user to view the source code in the 5ESS[®]-2000 switch. This access is proprietary and the appropriate nondisclosure agreements must be signed before it can be provided.

NOTE: Program listings were provided via microfiche and networked service. To print out pages, a viewer or a printer is required.

The on-line listings which record the software are similar to the microfiche listings but are *not* identical in format or content. The layout of the directory structure for the listings is similar to that used by the software developers. Breakpoints, disassemblies, and header files are left as individual files facilitating access via on-line editors. Authorized customers access the on-line listings via the EMNS and a login/password process. The on-line listings contain program listings for multiple software releases. The number of software releases available is consistent with the 5ESS[®]-2000 switch Software Support Product Policy.

NOTE: At the time of printing, there was no conversion for the AM diagnostic products. The following rules for using the on-line listings are for the SM and CM only.

The general rule to convert the PR name to the MODULE PRODUCT NAME is to remove the processor name and colon then make all characters lowercase except the first two. The processor being the first field (AM or CM or SM). This is true for SM products.

Example: SM:DNFABEX converts to DNfabex

CM diagnostic names are different, having DNC as the first three characters and, in this case, change all characters to lowercase except the first three. However, some CM products are 3B-related, in which case the first five characters are DNC3B, all in upper case.

Example: CM:DNC2NC03 converts to DNC2nc03
 AM:DNC3BFPC converts to DNC3Bfpc

Customers with login access to the on-line listings can refer to the 235-600-510, *Software Analysis Guide* for the login procedure and basic usage information. Customers can also call the Lucent Electronic Media Networked Service group at 800.225.4672 for assistance.

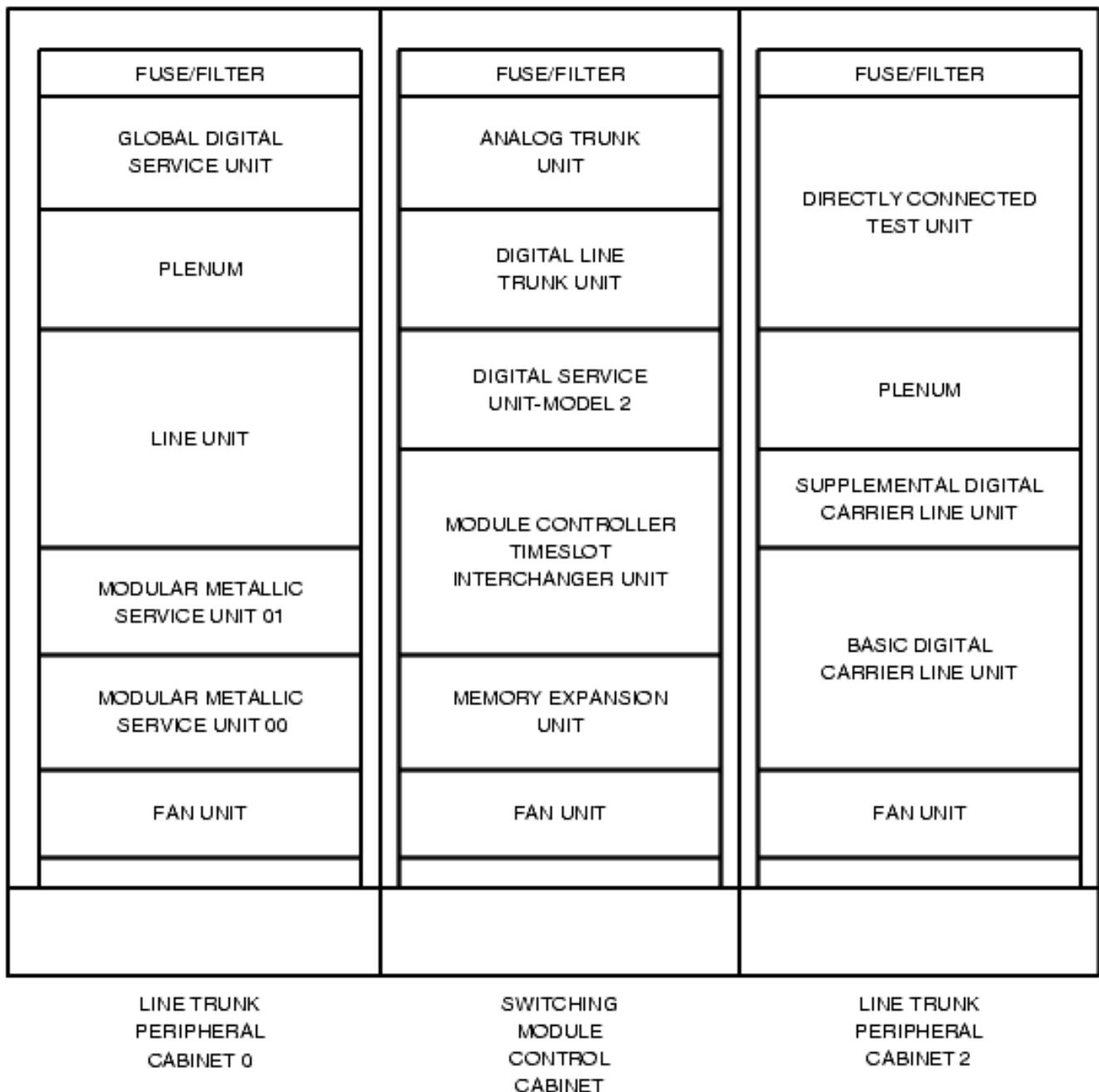


Figure 5.3-1 Switching Module

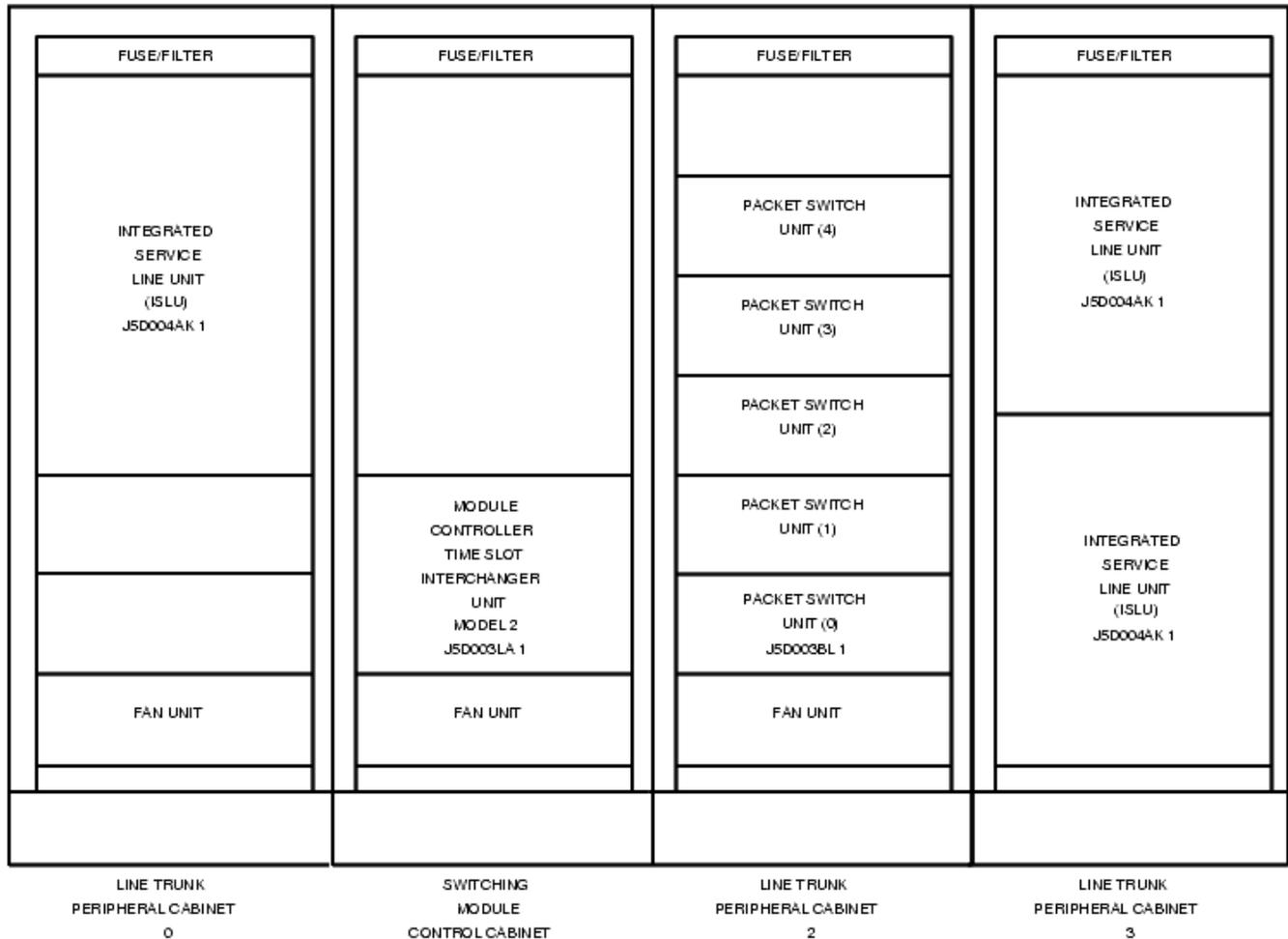


Figure 5.3-2 Loaded Switching Modules

5.3.2 SWITCHING MODULE-2000

The major component of the 5ESS[®]-2000 switch is the Switching Module-2000 (SM-2000). Architecturally identical to today's SM, the SM-2000 greatly expands the bandwidth available in the switch while providing additional call processing power and memory capacity needed for its effective use and the ability to terminate more peripherals than a SM.

The SM-2000 is required to permit the installation of SM peripherals in the aisles adjacent to the SMC cabinet. Because this increased capacity needs more power than a standard 48 kbps communications link can handle, the QLPS message network was designed to provide for the higher message capacity required by the SM-2000 and its peripherals. The following are the SM-2000 major components:

- A growable Time Slot Interchange Unit - Model 4 (TSIU4), can be grown to 30K time slots compared with 512 network timeslots of the existing SM. This enables enhanced support of the large-scale applications of wideband data switching, as well as continued support of narrowband services. Growth is in response to total bandwidth demand in increments of 3092 peripheral terminations (DSOs). Also, the fabric is configurable, providing additional network capacity toward the periphery of the switch or toward the internal network, as required. This flexibility permits a tailoring of bandwidth capacity. The internal network side of the TSI is served by expanded Network Control and Timing (NCT2) links. These NCT2 links grow with the TSI in increments of 1024 network terminations (DSOs) up to a maximum of 2048 network time slots per TSI slice (TSIS).

- The more sophisticated switching fabric of the SM-2000 is supported by a higher capacity Switching Module Processor (SMP). Based on the *Motorola*® *MC68040*TM microprocessor, the CORE40 has a significant increase in call processing capacity over the current SMP20. This means that the SM-2000 can support up to 27,520 (43 x 640) analog lines at 10:1 concentration or 10,752 digital trunk applications.
- The Switching Module Processor Unit - Model 4 (CORE40) complex also includes the Message Handler (MH), a separate processor responsible for all interprocessor messages for the SM-2000. Coupled with an expanded message channel on the NCT2 links of 800 kilobits per second (kbps), the MH comprises the SM-2000 portion of an enhanced message switching architecture.
- A larger Network Control and Timing Link (NCT2) which can be added incrementally to an individual SM-2000 and is fully compatible with the existing Communication Module (CM2) and NCT links on existing SMs. An SM-2000 can coexist on a switch with local and remote SMs.
- The Digital Service Unit - Model 3 (DSU3) is used to provide the local digital service unit function (LDSUF). The Global Digital Services Facility (GDSF) is also defined as the DSU3.

Peripheral units supported in SM-2000 are as follows:

- Digital Service Circuits (DSC3) - Local Digital Service Unit Function (LDSUF)
- Digital Line/Trunk Unit - Model 2 (DLTU2)
- Line Unit 3 (LU3)
- Digital Network Unit-SONET (DNUS)
- Modular Metallic Service Unit (MMSU) (EXM-2000 only)
- Directly Connected Test Units (DCTU) (EXM-2000 only)

Release 1(99-5E-1433) for the Switching Module - 2000 (SM-2000) provided 32 megabyte (MB) memory boards. With the 5E10 software release, the SM-2000 can also be equipped with new 64 MB boards (TN1806). These new memory boards can be used with the existing 32 MB boards on the same SM-2000, thus providing ease of maintenance and provisioning flexibility.

Figure 5.3-3 shows the basic SM-2000 frame and unit layout. Figure 5.3-4 illustrates the transmission interfaces for remote operation of the SM-2000. Figure 5.3-5 shows the TSI link to DX backplane connections, Figure 5.3-6 shows a backplane view of the TSIU4 and Figure 5.3-7 shows the layout of the DSU3.

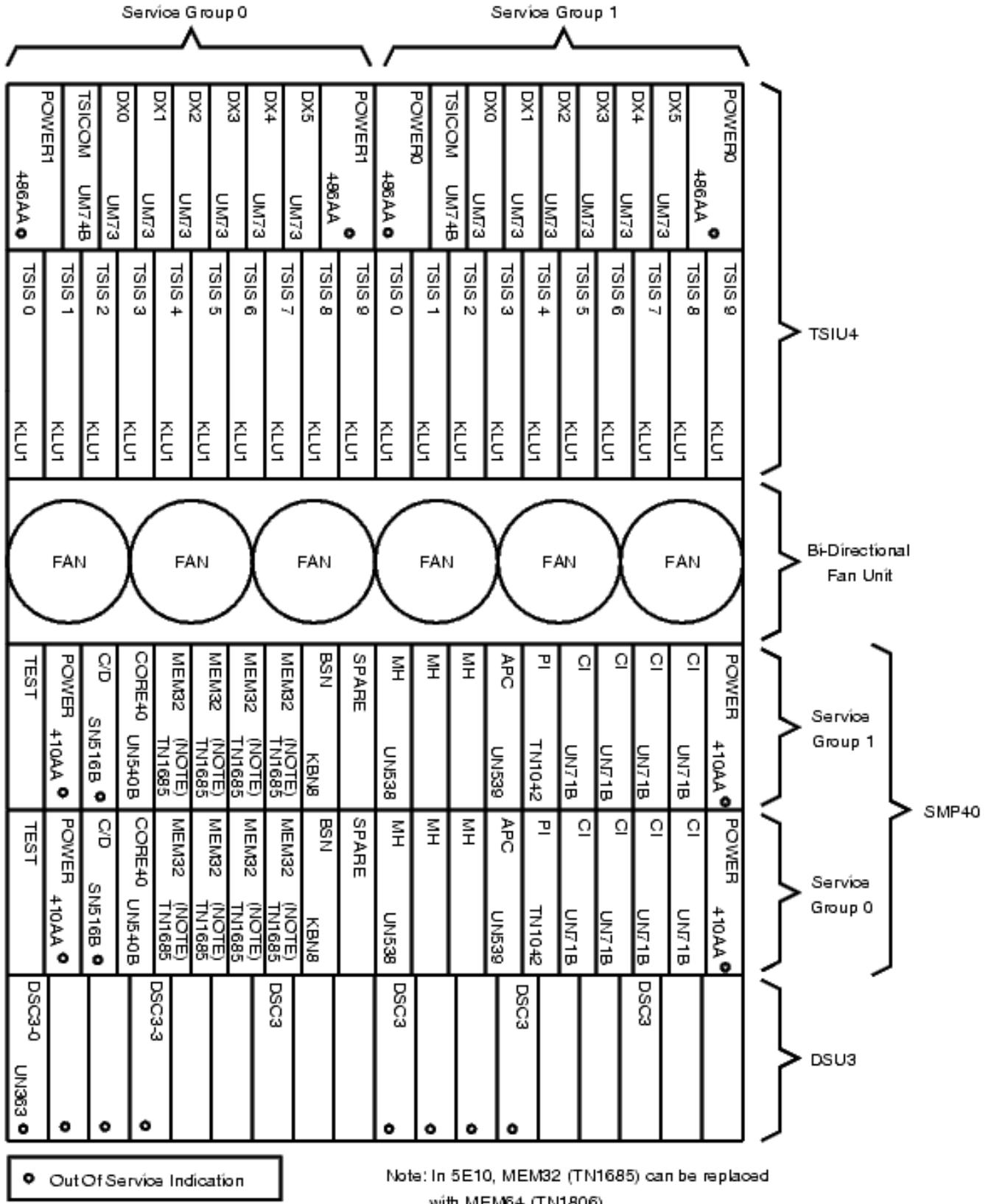


Figure 5.3-3 Basic SM-2000 Frame and Unit Layout Basic SM-2000 Frame and Unit Layout

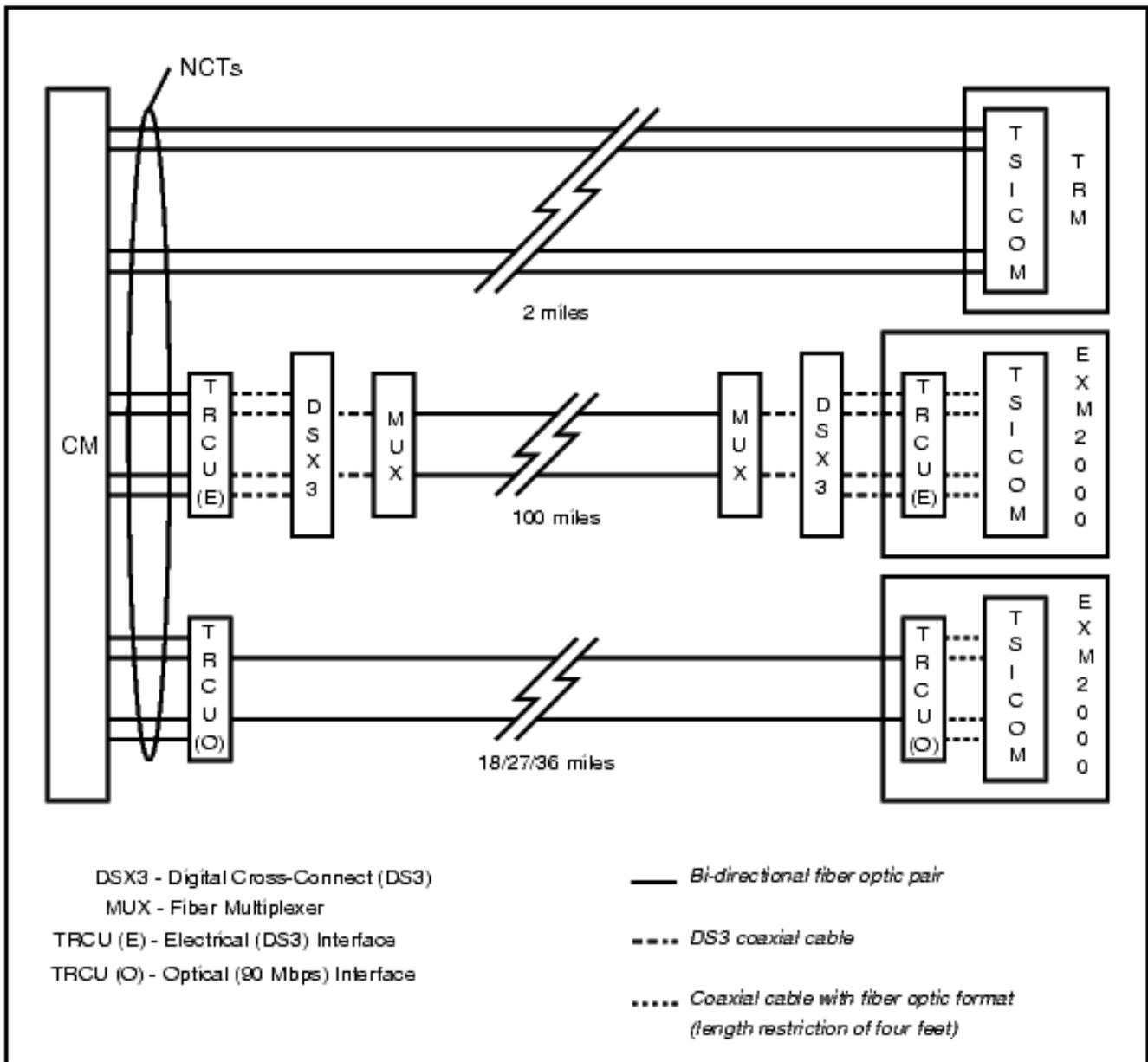


Figure 5.3-4 Transmission Interface for Remoting the SM-2000 Transmission Interface for Remoting the SM-2000

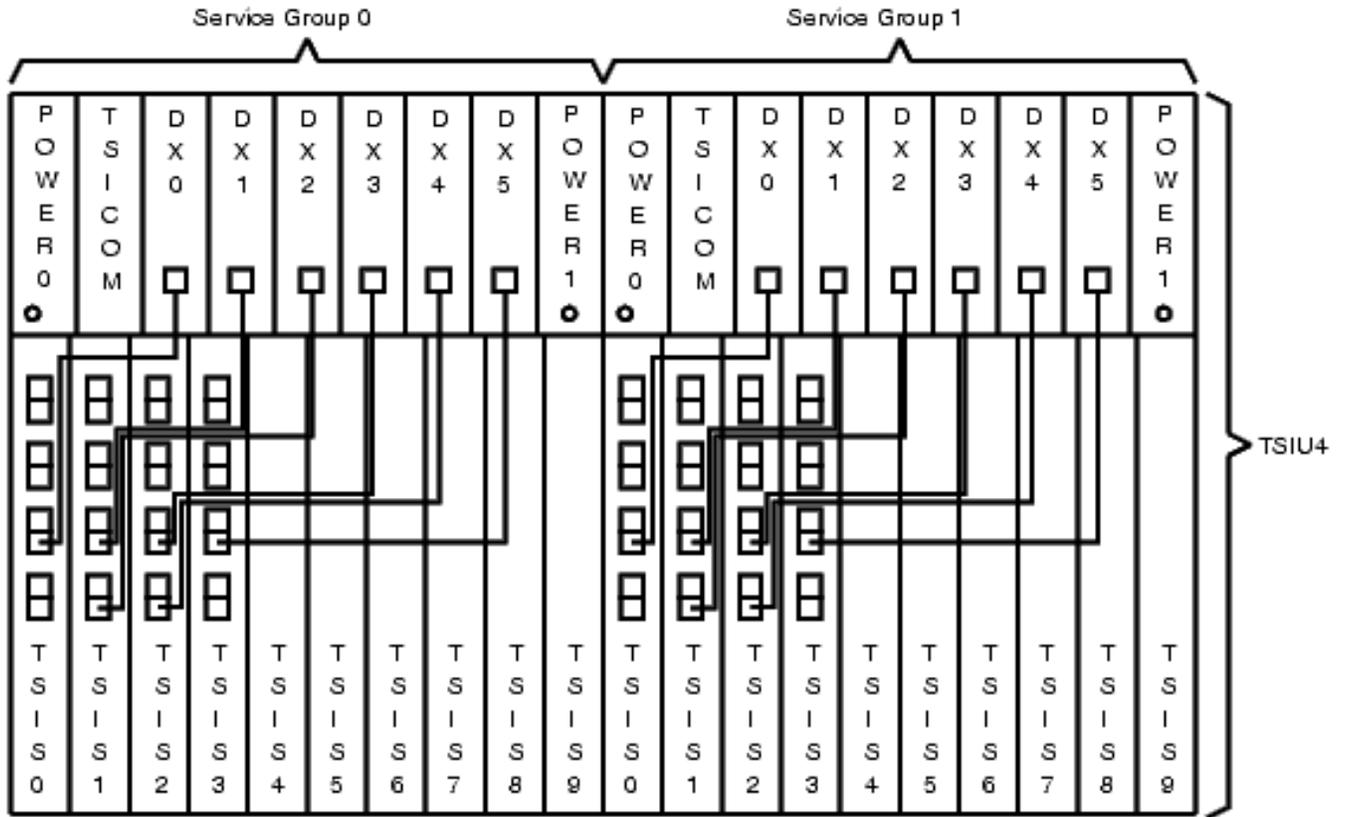


Figure 5.3-5 TSI Link to DX Backplane Connections TSI Link to DX Backplane Connections

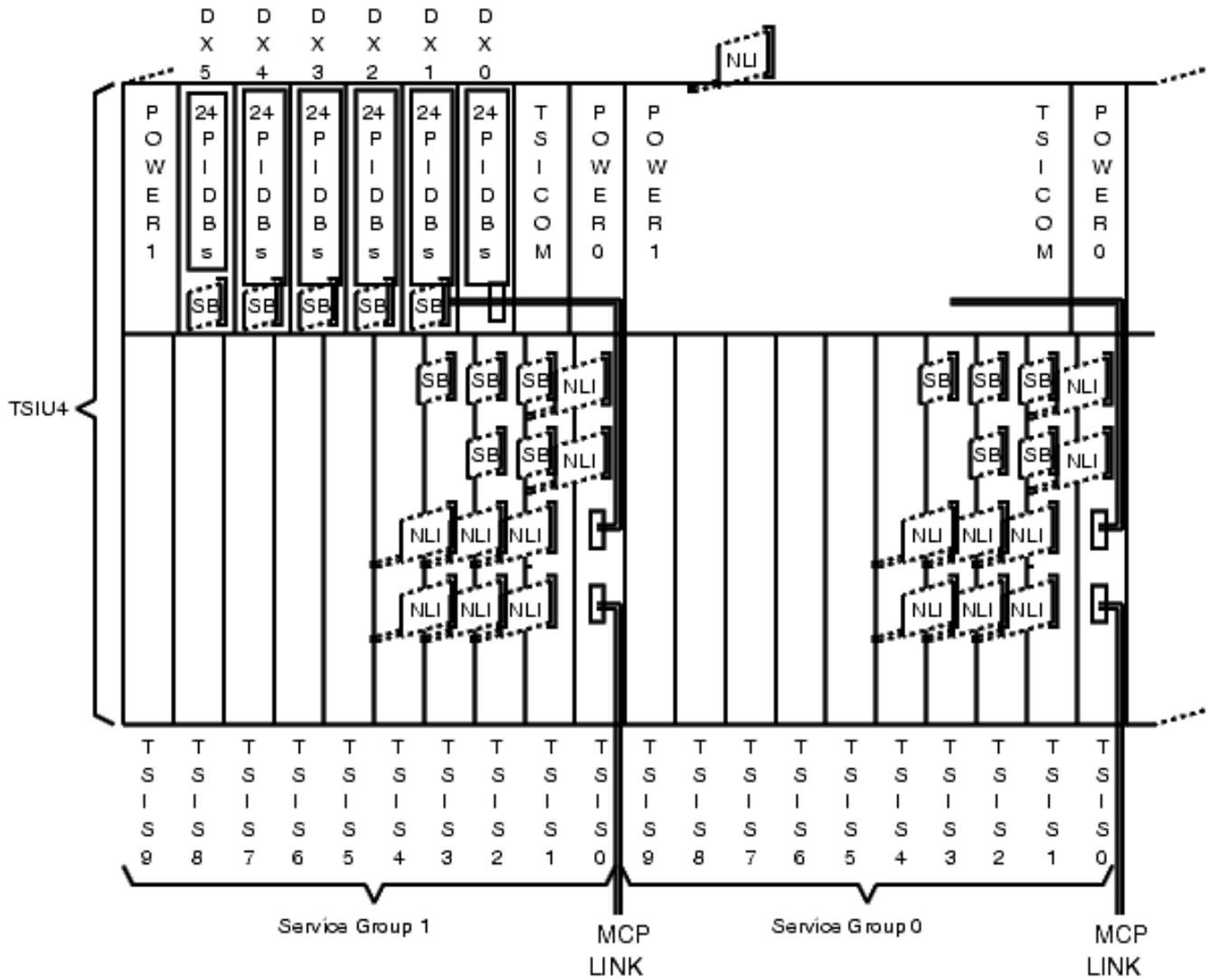


Figure 5.3-6 TSIU4 Backplane TSIU4 Backplane

Typical Placement of DSC3s for
Local Digital Services Function (LDSF)

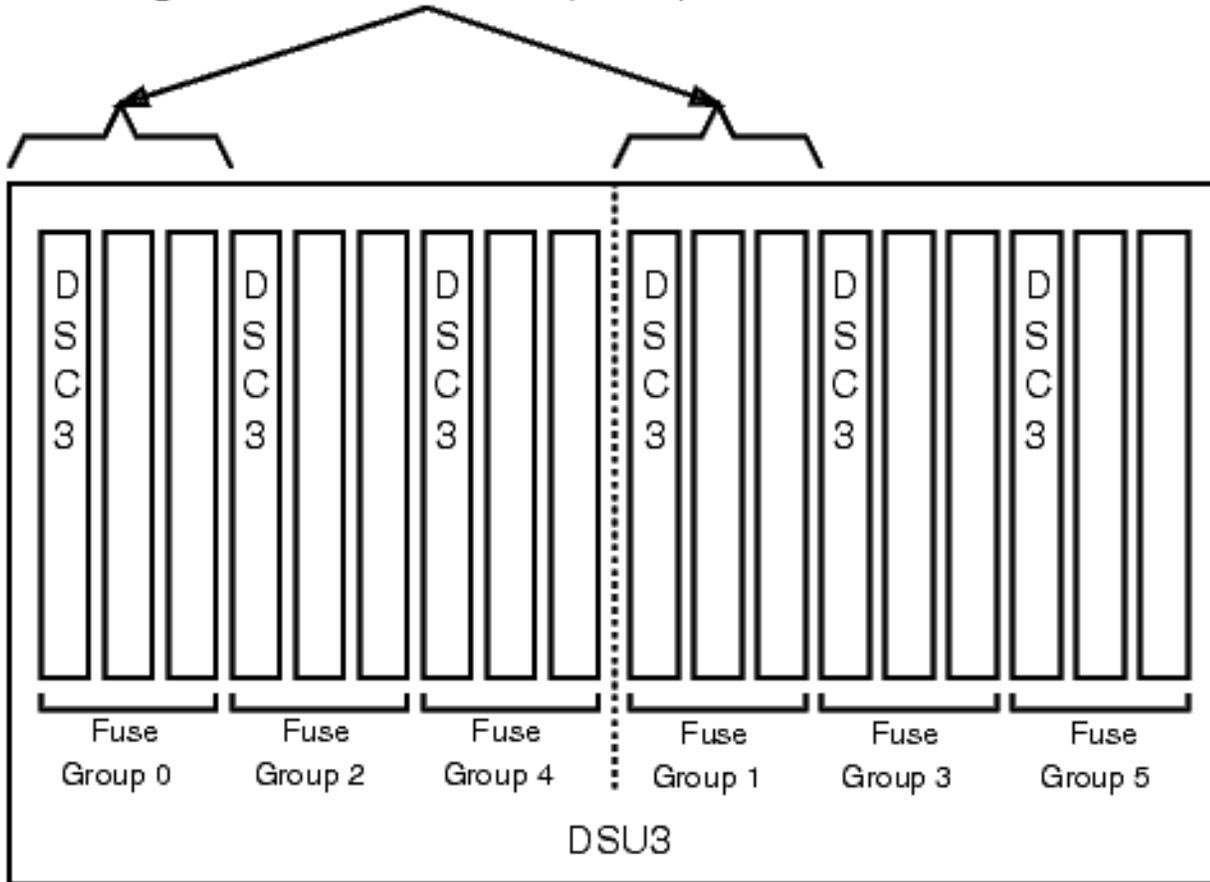


Figure 5.3-7 DSU3 Layout DSU3 Layout

5.3.2.1 TR303 on DNU-S

Previous generation Digital Loop Carrier (DLC) systems, designed to the TR-008 interface have supported a DS1 (Digital Signal Level 1) level interface to the Central Office Terminal. The DCLU (Digital Carrier Line Unit) and IDCU (Integrated Digital Carrier Unit) were developed to terminate DS1 based DLC systems directly on the 5ESS[®]-2000 switch.

Next Generation Digital Loop Carrier (NGDLC) systems that are being deployed today are being designed to the TR-303 interface. While they may still support DS1 access, SONET (Synchronous Optical NETWORK) OC-3 access is more common. In order to terminate an NGDLC system on an IDCU, the customer must either run copper to support a DS1 interface or provide a SONET multiplexer in the CO to extract DS1s from the OC-3.

The following two configurations are under consideration:

- 1) TR-303 through EC-1 intraoffice interfaces
- 2) TR-303 OC-3 interoffice interfaces over SONET rings.

In the two configurations, both asynchronous and byte synchronous mapped VTs (Virtual Terminals) are supported using the hybrid Time slot Management Channel / Embedded Operations Channel (TMC/EOC) for call processing and OAM&P control. Note that the Common Signaling Channel (CSC) implementation and DS1 protection switching

are NOT requirements for this feature.

This feature would provide a platform for future evolution of TR-303. In particular, TR-303 Feature Set C provides more integration of SONET compatible RDTs directly into the switch.

One DNU-S (TR303) will terminate SONET trunks and lines (both analog and ISDN). One DNU-S supports approximately 30,000 lines in an area (floor space) of 25 square feet (includes the SM-2000 cabinet).

5.3.2.2 Voice Frequency Data Enhancement — (VFDE)

The 5ESS-2000 Switch implementation of TR-303 utilizes the hybrid signaling method to detect off-hook, on-hooks and flashes along with standard TMC (Time-Slot Management Channel) message set for lines served by a TR-303 RDT (Remote Digital Terminal). This feature will enhance the TMC message set to contain non-standard messages that will be used to allow 64KB clear channel use of a DSO once a call has been set up. These new messages will be used to switch between clear channel mode and robbed bit mode for each individual call. This new messaging scheme will provide inter-operability with RDTs that do not support these new messages.

The VFDE is operational on both the IDCU, DNU-S and TR-303 platforms. When activated, the VFDE applies to all analog calls to/from single party Plain Old Telephone Service (POTS) Lines, Wide Area Telephone Service (WATS) Lines, and Ground Start Private Branch Exchange (PBX) Lines. This new signaling mechanism will be published in the 5ESS-2000 Switch TR-NWT-000303 Interface Specification document 235-900-308.

5.3.2.3 TSIU - Model 4

5.3.2.3.1 General

The TSIU4 consists of two shelves; an 8-inch high shelf which houses the power converters for the unit, the TSICOM circuit packs and the DX (PIDB Expansion) circuit packs plus a 16-inch high shelf which houses the TSIS circuit packs. This unit uses 9-inch deep boards for both shelves as opposed to the 13-inch boards used throughout the 5ESS[®]-2000 switch. This provides more space in the back of the unit for NLIs and ENLIs and forced air cooling of these boards without modifying the fan unit.

The TSIU4 uses a single backplane for the entire two-shelf, two service groups unit. Two power converters per TSI/DX service group are required. The second power converter needs to be installed whenever the number of TSIS circuit packs is four or more or whenever the number of DX circuit packs equals six. One TSICOM, 10 TSIS and six DX circuit packs are allowed per service group. TSI service groups are split left and right and a single backplane is used for both service groups of TSI/DX. The mapping of the TSI links to the DX.

5.3.2.3.2 Time Slot Interchange Common

The Time Slot Interchange Common (TSICOM) provides the control interface to the SMP and is responsible for the synchronization timing for the SM. The TSICOM contains a stratum 4 clock for the SM. This supports the digital trunks when the SM-2000 operates as a standalone unit.

5.3.2.3.3 DX - PIDB Expansion

The DX board converts one TSI link into 24 PIDBs using all the time slots of the TSI link. The DX is a standard board that inserts through the front of the TSI unit. A maximum of six boards is located in the shelf immediately above the TSISs. The TSI link for the DX may be connected either by a cable from the TSI or through the backplane traces and paddleboards.

5.3.2.3.4 Time Slot Interchange Slices

The Time Slot Interchange Slices (TSIS) occupy the second, double-grid shelf in the TSIU4. Each TSIS sends the data it receives from its TSI link to the first TSIS. The first TSIS stores all the time slots that arrive at the TSI in its

TSI RAMs and sends it to the second TSIS and so forth. The TSISs provide four duplex TSI links. The maximum number of TSISs that can be installed is 10. Each TSIS circuit pack terminates four TSI links.

5.3.2.4 TSIU4 (SM-2000) Version 2

The TSIU4 Version 2 provides exactly the same functionality as TSIU4, but in a different unit configuration. TSIU4-2 will still be a two shelf duplex unit, but will use two separate backplanes in place of a single, triple-high backplane. The upper shelf is a standard 8" high by 13" deep 132-type housing, which contain one Power Converter and up to six XDX (UN553) circuit packs per service group. The left side of the shelf is designated SG0 and the right side is designated SG1.

The lower shelf is a double high 500-type housing, 16" high and 10" deep, containing two Power Converters and two TSICOM packs (UM74C) stacked vertically on the left hand side of the unit, as viewed from the front. The lower pair is in service group 0, the upper pair in service group 1. The right side of the shelf contains up to 10 TSIS (KLU1B) packs per service group, with service group 0 to the left and service group 1 to the right of the center stiffing plate.

A minimally equipped TSIU4 Version 2 service group contains:

- One 410AA and one 486AA Power Converter
- TSICOM (UM74C)
- One TSIS (KLU1B)
- One XDX (UN553)
- Two CBT paddle boards
- One CTSNS paddle board.

5.3.2.6.3 Message Handler

The Message Handler provides access from the CORE40 to the QLPS network and can terminate several message links that consist of time slots embedded in the links which are used to carry messages to and from the SMP. The MH terminates 32 time slots for messages. The CTS and QLPS are the communication types to be handled by the MH and terminates HDLC-encapsulated messages carried in the payload time slots of the TSI.

5.3.2.7 Digital Service Unit - Model 3

5.3.2.7.1 General

This shelf houses the Digital Service Circuit - Model 3 circuit packs. There are a total of 18 slots in six fuse groups (of three boards each) in this unit. The unit's design provides backplane connections for all adjacent slots for multiple board services such as the RAF and announcement memory. For reliability, it is desirable to spread the DSCs across fuse groups to avoid the loss of all three DSC3s to a single fuse failure. Refer to Figure 5.3-7.

5.3.2.7.2 Digital Services Circuit - Model 3

The Digital Services Circuit - Model 3 (DSC3) provides four times the capacity of the DSC used in the SM. It also provides the Local Digital Service Function (LDSF). Each DSC3 circuit pack comprises a service group and has four duplex PIDBs for a total of 128 time slots of data and a duplex PICB for control. A minimum of two DSC3s is required for reliability. Each DSC3 circuit pack is powered separately through an on-board power converter. The DSC3 does not support the 5E10 implementation of the Service Announcement System (SAS). For the SM-2000, the SAS is on a DSU (Model 2) shelf.

5.3.3 SWITCHING MODULE PROCESSOR UNIT - MODEL 5

The Switching Module Processor Unit - Model 5 (SMPU5) implements the SM-2000 SMP functionality in a different unit configuration. The SMPU5 development consists of three basic pieces: a new backplane which integrates DSC3 functions into the unit; a CORE60 processor board with additional integrated DRAM; and a APC board. None of these changes affect any of the TSI, its interfaces, or the SU IO interfaces with the SMP. A detailed list of all the hardware changes follows.

5.3.3.1 Unit

The SMPU5 unit is capable of supporting all SM-2000 configurations supported by SMPU4, and in particular VCDX. The differences between SMPU4 and SMPU5 are the equipment locations which will change for most/all boards. SMPU5 uses a single, combined power/control and display board per side; there are DSC3 slots in SMPU5; and there are only 2 memory slots, per side, in SMPU5. Refer to Figure 5.3-9.

Two memory slots provide for sufficient memory growth given the currently available 32 Megabytes (MB) and 64 MB memory boards. With a 128M CORE60MM board and 2, 64M memory boards, a total of 256 MB could be equipped in the SMPU5 without further development. The SMPU5 developed in 5e11 will support CORE60 with 64 MB and CORE66 will support the faster version of CORE60 with 64 MB.

The CORE60 operating at 60MHz is designed to improve the processor performance and provide two CORE RAM memory configurations of either 64MB(UN594) or 128MB(UN588). The 64MB CORE60MM(UN594) is supported on SMPU4 for release 5E12. The 128MB CORE60MM(UN588) is supported on SMPU5 for release 5E12. The 128MB CORE60MM(UN588) will be used for all newly shipped SMPU5 offices.

5.3.3.2 Power, Control, and Display

The Power, Control, and Display (PCD) will provide a 5V output supply only. However, the SMPU backplane is designed to support boards which utilize on-board 3.3v power supplies. As 3.3v use becomes more prevalent on

the CORE and MEM boards, the need to tie these converters into the +5v alarm/detection and auto-shutdown capability provided by the PCD becomes apparent. Therefore, a single wire bus will be provided in the backplane from the PCD to the CORE and MEM slots. Future CORE and/or MEM designs may use this bus to indicate to the PCD that an internal 3.3v power failure has occurred so the PCD can report and act on the power fault appropriately. The initial PCD design will investigate design requirements needed to provide this function but will not be required to implement this capability. A combined PCD board developed for the SMPU5 cannot be used by the existing SM-2000 with SMPU5.

5.3.3.3 Cable

The current cables used for all SMPU5 shelf 0 to shelf 1 update bus interconnects (i.e. BSN and MH/MHEIB update bus cables) are integrated into the backplane.

5.3.3.4 CORE60MM

The CORE60MM design will be based on the UN560 (CORE60) design and will retain all of its functionality. As a goal, the new CORE60MM will have minimal impact to the 5ESS®-2000 switch. The primary switch impacting area of the new CORE60MM design will be the growth of the on-board memory to a maximum equipage of 128 megabytes.

Three board codes will be created from a single AM version of the CORE60MM: a 64M board, a 96M board, and a 128M board. A given board code will dictate the number of DRAMs which are populated on the board in order to attain that codes particular DRAM density. In addition, the hardware will indicate to switch the amount of on-board memory.

NOTE: The new CORE60MM will not be supported in 5e11 software releases.

5.3.3.5 Application Controller

The intent of the new Application Controller (APC-CR) hardware is to be fully interchangeable with the current versions of the UN560 and UN539 boards. This means that the new APC-CR boards can be equipped in the SMPU4, SMPU5, or ATM units. Likewise, the current versions of the UN560 and UN539 can be equipped in the SMPU5 unit.

014	022	032	042	052	061	072	080	088	096	106	114	122	130	138	146	156	166	176	
PCD	TEST UN364/UN561	CORE60 UN560	MEM32/64 TN1685/TN1806	MEM32/64 TN1685/TN1806	BSN KBN8B	APCX * EDUN555	MH/MHEIB UN538	NH UN538	NH UN538	APC UN539	PI TN1042B/UN395B	CI UN71C	CI UN71C	CI UN71C	CI UN71C	DSC3 SG19 PN1 UN363	DSC3 SG19 PN1 UN363	DSC3 SG19 PN1 UN363	
PCD	TEST UN364/UN561	CORE60 UN560	MEM32/64 TN1685/TN1806	MEM32/64 TN1685/TN1806	BSN KBN8B	APCX * EDUN555	MH/MHEIB UN538	NH UN538	NH UN538	APC UN539	PI TN1042B/UN395B	CI UN71C	CI UN71C	CI UN71C	CI UN71C	DSC3 SG19 PN1 UN71C	DSC3 SG19 PN1 UN363	DSC3 SG19 PN1 UN363	
014	022	032	042	052	061	072	080	088	096	106	114	122	130	138	146	156	166	176	

8"

8"

SERVICE GROUP1

SERVICE GROUP0

SMPU5

* APCX (available in international generics only)
 SG Service Group (unit offset)
 PN Pack Number

Figure 5.3-9 Switching Module Processor Unit - Model 5 Switching Module Processor Unit - Model 5

5.3.4 EXTENDED SWITCHING MODULE-2000

5.3.4.1 General

The Extended Switching Module-2000 (EXM-2000) feature provides optical remote control for an SM-2000 via Transmission Rate Conversion Unit - Model 2 (TRCU2) equipment. The EXM-2000 supports the same functions and operations as the local SM-2000.

The Extended Switching Module-2000 (EXM-2000) has a maximum of 24 Electrical Network Link Interfaces (ENLIs) per each side of the EXM-2000. An ENLI is the hardware which terminates Network Control and Timing links. A minimum of two primary ENLIs per EXM-2000 side (a total of four primary ENLIs per EXM-2000) must be installed. The ENLI can be terminated to up to six fully equipped TRCU2 units at each end. Each TRCU2 requires two ENLIs per EXM-2000. The ENLI terminates 256 time slots while an NLI terminates only 512 time slots.

5.3.4.2 Electrical Network Link Interface

The Electrical Network Link Interface (ENLI) terminates one bi-directional electrical link to the Transmission Rate Conversion Unit - Model 2 (TRCU2). This link is identical to that used between the DLI and TRCU2. It provides an optically remote SM-2000 without any modifications to the TRCU2.

5.3.5 TRANSMISSION RATE CONVERTER UNIT (TRCU3)

5.3.5.1 General

The TRCU3 supports the conversion of Network and Control Timing / Network and Control Timing Model 2 (NCT/NCT2) 5ESS Switch signals into SONET (STS1), and provides the capability to remote an EXM-2000 or an ORM for 5E applications. The TRCU3 is replacing TRCU2, and improving the available network timeslots for an EXM-2000. TRCU3 is being implemented using NCT packs for Optically Remoted Module (ORM) and NCT2 packs for EXM-2000 in a Digital Data Multiplexer 2000 (DDM-2000) shelf which occupy a DS3 function slot.

5.3.5.2 Detailed Description

The major difference with the EXM-2000 with the TRCU2 and the TRCU3 is the Network Components. The EXM-2000 with the TRCU2 network connection is limited to 512 TSs/ Network Link Pair. The TRCU connection provides network connection supports 1024 TSs/Network Links Pair. While the TSI has the same capacity, there are fewer Network side TSs available with the TRCU2. Both the TRCU2 and TRCU3 can be used to support an EXM-2000. When an existing EXM-2000 with TRCU2 needs to grow, it will be able to grow TRCU3s along side the existing TRCU2s. In a mixed configuration the TRCU2s must be equipped before the TRCU3s.

The TRCU3 is made up of the following:

- Synchronous Timing Generator (TGS) — Two circuit packs (4-inches high). Provides timing.
- Optical Line Interface Unit (OLIU) — Multiplexes STS-1 signals into OC-3/OC-12.
- NCT1 or NCT2 — Terminates NCT or NCT2 links from the 5ESS-2000, converts NCT/NCT2 signals into STS-1.
- Overhead Controller (OHCTL) — Provides SONET overhead to the OLIU.
- System Controller (SYSCTL) — Provides control of other circuit packs within the TRCU3.
- User Panel — Provides information and control functions.

5.3.5.3 Functional Description

The following functions are provided on the TRCU3:

- The TRCU3 unit equipped with the NCT packs will be used for remoting ORM.
- The NCT function pack terminates one 256 timeslot NCT link.
- The TRCU3 unit equipped with NCT2 packs will be used to remote EXM-2000s.

The units that make up the TRCU3 provide the following functions:

- TGS — Provides timing for the TRCU3 shelf. Also provides a reference signal for network synchronization.
- OLIU — Interface with the OC-3/OC-12 optical
- NCT1/NCT2 — Terminates one NCT or one NCT2 link per board from the TMS, ORM, or EXM-2000. Converts NCT or NCT2 signal into SONET STS-1.
- OHCTL — Used in conjunction with the SYSCTL circuit pack. Provides overhead channel interface for the system.
- SYSCTL — Main System Controller in the system. Used in conjunction with the OHCTL circuit pack. Control over all shelf functions and provides all user interfaces into the system.
- User Panel — Allows CIT tasks to be performed. Provides information and control functions.

5.3.5.4 Configuration

At the host office, the TRCU3 will reside in a miscellaneous cabinet next to the Communication Module 2 (CM2). At the remote location, the TRCU3 will reside in the Switch Module Cabinet (SMC) for an ORM and the Line & Trunk Peripheral (LTP) cabinet for an EXM-2000. Each of the new circuit packs provides termination for NCT/NCT2 links and maps NCT/NCT2 signals into STS-1, SONET. The following distinctions should be noted:

- The TRCU3 is equipped with NCT packs when used for remoting ORM
- The NCT function pack terminates (1) 256 timeslot NCT link.
- The TRCU3 is equipped with NCT2 packs when used to remote EXM-2000s.
- The NCT2 function pack terminates (1) 512 timeslot NCT2 link.
- The NCT packs will terminate NCT links from the CM2 or the ORM.
- The NCT2 packs will terminate NCT2 links from the CM2 or the EXM-2000.

5.3.5.5 Shelf and Pack Layout

The TRCU3 feature includes new circuit packs that will support the conversion of NCT/NCT2 5ESS Switch signals into STS1. These new circuit packs will be used along with packs derived from the DDM-2000 OC-3 multiplexer creating a new unit called TRCU3. The TRCU3 circuit packs consist of the following:

- NCT1/NCT2 Circuit Packs — The NCT1 (BNP1) or NCT2 (BNP2) circuit packs terminate the NCT or NCT2 links from the TMS, DLI, or NLI. The BNP1/BNP2 converts the NCT/NCT2 links into SONET STS-1 electrical signals. In the opposite direction, the SONET STS-1 electrical signals are converted to NCT/NCT2 links.
- OLIU — The OLIU multiplexes the SONET STS-1 electrical signals and SONET overhead signals into OC-3 or OC-12 transmission to the remote office which contains the ORM or EXM-2000. In the opposite direction, the OLIU demultiplexes the OC-3 or OC-12 signal back into SONET STS-1 and SONET overhead. Intra-shelf control is provided by SYSCTL.
- TGS — TGS provides timing to NCT1 (BNP1)/NCT2 (bnp2) and OLIU circuit packs. Control is provided by SYSCTL.
- SYSCTL — SYSCTL provides control and monitoring of all circuit packs in the TRCU3. It communicates with the OHCTL through a dedicated bus via dual port RAM. The SYSCTL provides front and rear S-232D interfaces to a Craft Interface Terminal (CIT) for local craft interface.
- OHCTL — OHCTL accesses the SONET Data Communications Channel (DCC) through the OLIU and processes the OSI 7-layer protocol as specified for the DCC. The OHCTL also provides an x.25/TL-1 gateway interface for access to remote Operation Support (OS) Systems and a 10-base LAN interface for extending the DCC to a co-located SNC-2000 EMS or to other co-located SONET network elements.

For each TRCU3 path, there is one additional timeslot required for special control purposes. One timeslot, referred to as the Control Time Slot (CTS) is used for messaging with ORM. The additional timeslot, referred to as the Transmission Control Time Slot (TCTS), is used with both ORMs and EXM-2000s. Because of the control timeslot, the number of ORMs in an office is limited to 120. As a result of these timeslot restrictions, an ORM can not use two traffic bearing timeslots with each link, and an EXM-2000 cannot use one.

The mapping of network control and timing signals are performed by the NCT/NCT2 circuit packs of the TRCU3 proceeds independently of the host or remoted switch. The TRCU3 circuit packs are listed in figure: 5.3-10

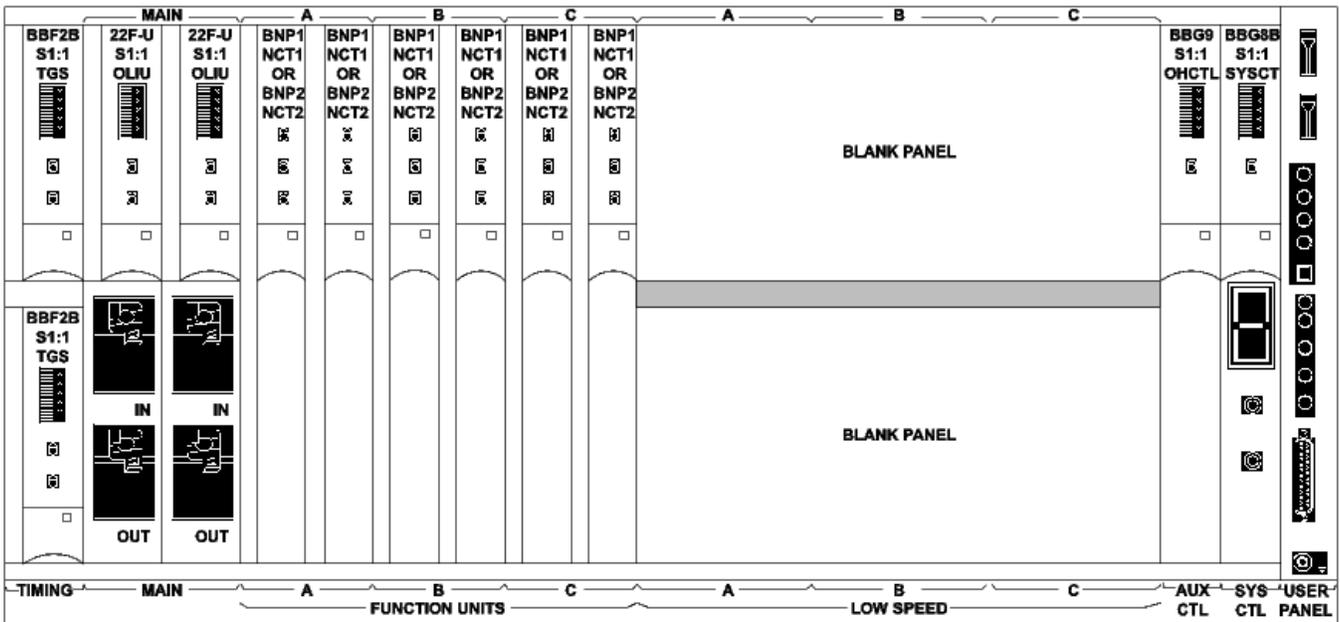


Figure 5.3-10 Transmission Rate Converter Unit Model 3 Transmission Rate Converter Unit Model 3

5.3.6 DIGITAL NETWORK UNIT-SONET - J5D003FR-1

5.3.6.1 General

The SM-2000 also supports, the Digital Network Unit-SONET (DNU-S), which provides an STSX-1 trunk interface. It is a high-capacity, digital, trunk-termination vehicle which can support up to 8,064 trunks via a new SONET STS-1 interface.

The DNU-S interface to the SM-2000 Time Slot Interchange (TSI) is via new optical Peripheral Control and Timing (PCT) links. These links are 65.536 Mbps and replace the Peripheral Interface Data Bus (PIDB) and Peripheral Interface Control Bus (PICB) interfaces currently used by existing Switching Module (SM) peripherals - for example, Line Units (LU)s, Digital Line and Trunk Units (DLTUs), etc.

The DNU-S interface to the network is via electrical STS-1 STSX-1 links. This interface is a standard SONET interface and, as such, is compatible with transmission equipment that supports the STS-1 interface, including the Digital Access and Cross Connect System IV - 2000 (DACS-2000) and the Dual Digital Multiplexer-2000 (DDM-2000).

The DNU-S, as a 5ESS[®]-2000 switch peripheral, provides complete Operations, Administration and Maintenance (OA&M) and Provisioning functions. This includes capabilities such as Recent Change/Verify (RC/V), Performance Monitoring, Call Trace, Alarming, etc.

Initially, the DNU-S is capable of supporting 12 STSX-1 high-speed trunk interfaces. Each STSX-1 can support 672 DSOs.

The DNU-S is in the Line Trunk Peripheral (LTP) cabinet of the SM-2000 and can accommodate two DNU-S units, one above and one below the center-mounted bidirectional fan unit.

The DNU-S is a double-high (16-inch) shelf unit which fits into the new 5ESS[®]-2000 cabinet. The DNU-S unit uses a single backplane for the entire unit and uses 16- by 13-inch KLV-coded circuit boards. Common Optical Termination (COT) and STSX-1 Link Interface (SLI) paddle boards connect to the rear of the backplane.

The unit is divided into two mirror-imaged data groups around the duplexed Common Control (CC) circuit packs located at the center of the unit. In simplex mode, each CC can control both data groups. Each data group contains duplexed Common Data (CD) and STSX-1 Facility Interface (SFI) packs and the engineered number of simplex service Transmission Multiplexer (TMUX) packs plus one spare TMUX (TMUX-S) for protection. The amount of TMUX packs used in each data group is dependent on the number of STX-1 transmission links that are terminated onto the DNU-S.

Table 5.3-1 provides the quantities of DNU-S components required.

Table 5.3-1 DNU-S Engineering Quantities

ELEMENT	MAX SERV EQUIP	MIN OPER EQUIP	MIN SERV EQUIP	DESCRIPTION
Message Handler	2	2 ^a	2	SM-200 Unit 32 Time Slots
DNU-S Unit	8 ^b	1	1	SM-2000 Peripheral Capacity: 8064 Trunks
PCT Links (Duplicated)	24	2	2	Interface to SM-2000 1-6 pair per Data Group
PCT Link Interface (PLI) (Duplicated)	24	2	2	Paddleboard on SM-2000. One per PCT link.
Common Control (CC) (Duplicated)	2	2	2	DNU-S Processor One pair per DNU-S Unit
Common Data (CD) (Duplicated)	4	2	2	One pair per Data Group
Common Optical	24	2	2	Termination (COT)

Paddleboard on DNU-S (Duplicated)				One per PCT link
Transmission Multiplexer (TMUX)	14	1	2	One Spare and 1-6 Active Per Data Group
STXS-1 Facility Interface (SFI) (Duplicated)	4	2	2	One pair per Data Group
STXS-1 Link Interface (SLI)	12	0	1	Paddleboard. One per STXS-1 Link
STXS-1 Link	12	0	1	Interface to Transmission 1-6 per Data Group
STE/STS-1	12	0	1	1 per STSX-1
VT1.5/DSI	28 x 12	0	1	1-28 per STSX-1
Notes:				
a. A second MH is required for DNU-S. If the SM-2000 does not support a DNU-S, it only needs one MH.				
b. Release 1 must support up to four DNU-Ss.				

5.3.6.2 Common Control

The DNU-S contains two CC circuit packs which implement a duplex unit controller that operates in an active/standby mode and performs the following functions:

- Terminates the communication and control channels that originate from the SM-2000 CORE40 and are interfaced via the PCT links and Common Data (CD) circuit packs.
- Supervises unit initialization, maintenance and diagnostics.
- Implements and handles the control interfaces to all DNU-S circuits.
- Provides non-volatile storage of CC and TMUX control programs in flash memory.

5.3.6.3 Common Optical Terminator

The Common Optical Termination (COT), 982TN, terminates the optical fibers for one side of a duplex PCT link and performs optical-to-electrical and electrical-to-optical conversion of data and control information received by and transmitted over the PCT link interface with the SM-2000. The DNU-S may be equipped with up to 24 COT paddle boards.

5.3.6.4 Common Data

The DNU-S may be equipped with either two or four Common Data (CD) packs with two packs in each data group. The two packs in each data group are designated as "mates". For example, CD00 and CD01 are

The mate CDs in each data group can terminate up to six duplicated PCT links with side 0 for each duplicated link terminating on one CD and side 1 terminating on the other CD. The mate CDs in each group operate active/standby.

The CDs logically terminate the PCT links and perform rate conversion, selection and multiplexing/demultiplexing functions that are associated with the passage of data and control information between the PCT links and internal interfaces with other packs in the unit.

The CD performs specific functions, which include:

- Interfaces with up to six normally active Transmission Multiplexer (TMUX) packs, where each terminates one STSX-1 link and mapping data and signaling information among the TMUXs and up to six PCT links with the STS-1 information for each TMUX mapped onto one PCT link.

- Interfaces with a spare TMUX pack and supports TMUX pack sparing capabilities.
- Converts data and signaling information between the PCT link format and the Bi-Peripheral Interface Data Bus (BPIDB) format used internal to the DNU-S to pass information between the TMUX and CD packs.
- Extracts and inserts unit control information on PCT link 000/001 and implements the Peripheral Control and Maintenance Bus (PCAMB) interface to the CCs (in CD data group 0 only.)
- Extracts and inserts the SONET Section Data Communications Channel (DCC), line DCC, section orderwire and low orderwire information on the PCTs.
- Derives system reference timing from the 5ESS[®]-2000 switch and sources synchronization timing to the rest of the DNU-S.

5.3.6.5 Transmission Multiplexer

The Transmission Multiplexer (TMUX) provides the format conversion of data between one STSX-1 link and 14 BPIDB structures, including the mapping of data time slots between the two formats and signaling bit conversion.

The DNU-S may be equipped with up to 14 TMUX packs. In each data group, the TMUXs implement an N+1 sparing arrangement with up to six active TMUXs and one spare that can be switched into service in place of any of the active TMUXs.

The TMUX also performs functions associated with terminating the STS-1 SONET and facility overhead, including the following:

- Terminates STS-1 line and section overhead.
- Terminates STS-1 path overhead and extracts Virtual Tributary (VT).
- Frames and extracts DS1.
- Detects DS1 facility alarms.
- Checks DS1 Cyclic Redundancy Code (CRC).
- Initial collection of STS-1 and DS1 performance monitoring data.
- Facilitates data alignment to the system clock.

5.3.6.6 STSX-1 Facility Interface

The DNU-S may be equipped with two to four STSX-1 Facility Interface (SFI) packs with two in each data group. Each SFI pack pair implements a duplicated electrical interface for six STSX-1 links. The SFI implements STSX-1 line drivers and receivers, Bipolar 3-Zero (B3SZ) encoding and decoding and connects each of the six STSX-1 links to either one active or the spare TMUX.

5.3.6.7 STSX-1 Link Interface

The DNU-S may be equipped with up to 12 SLI paddleboards with each board terminating one STSX-1 link. The SLI is a passive circuit that contains a splitting transformer for coupling the received STSX-1 signal to two SFI circuit packs and another transformer that couples the STSX-1 transmit signal from two SFIs to the facility.

Figure 5.3-11 shows the DNU-S in a cabinet with two units.

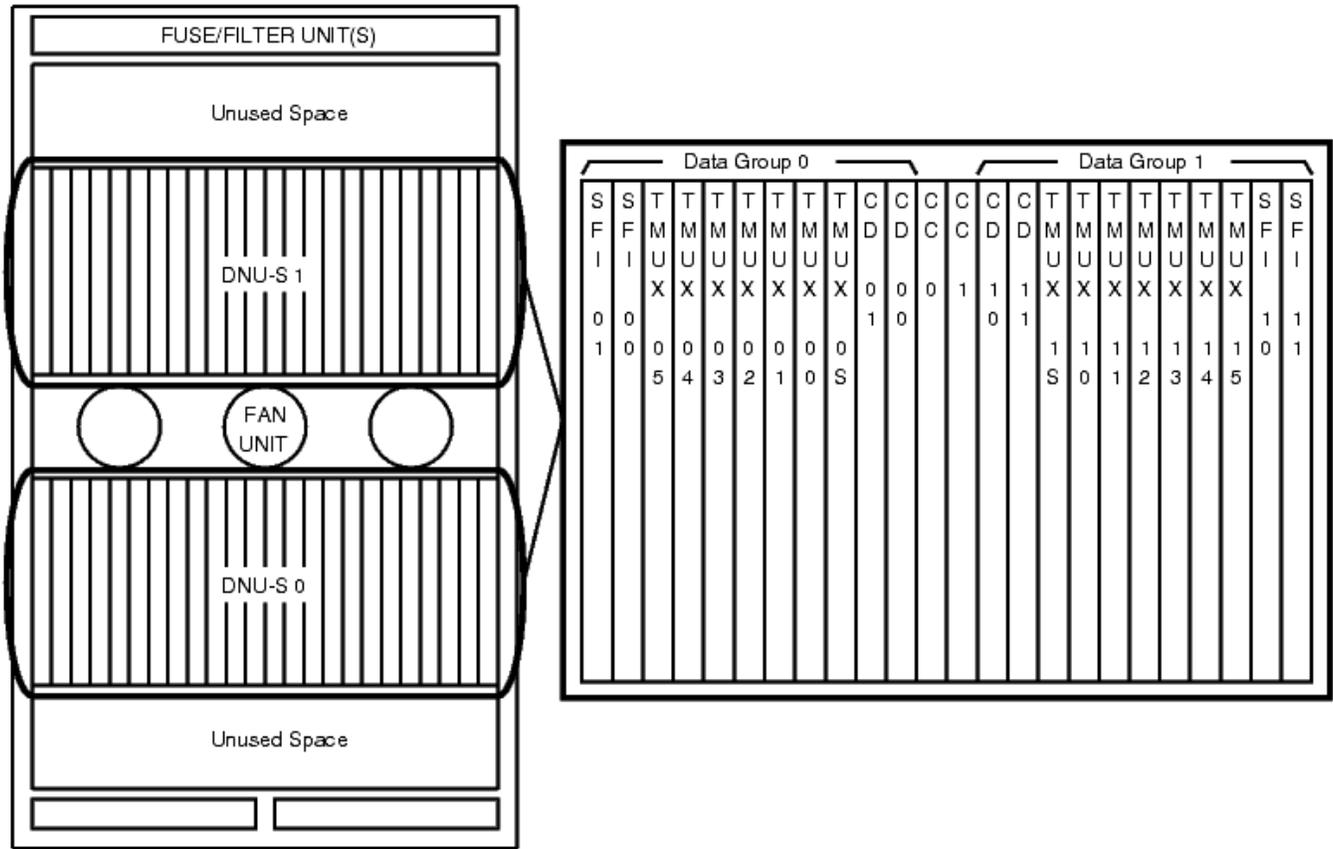


Figure 5.3-11 Digital Network Unit-SONET Physical Configuration with Two Units per Cabinet Digital Network Unit-SONET Physical Configuration with Two Units per Cabinet

5.3.7 ANALOG TRUNK UNIT - J5D003AC-1

The Analog Trunk Unit (ATU) is a single-shelf unit that can be mounted in any vacant shelf position in the Switching Module Control cabinet or any of the Line Trunk Peripheral cabinets. Functionally, it provides termination for interoffice trunks and trunks to operator positions and announcement machines.

The unit is divided into two service groups, 0 and 1, each group containing a Common Circuit Pack Area and a Trunk Circuit Pack Area. There are nine different trunk circuit packs available for use, depending on the trunk circuit functions. The packs are listed on Figure 5.3-12 .

Figure 5.3-12 shows where the ATU is located in the Switching Module Control Cabinet and its respective circuit packs in the unit.

Figure 5.3-12 Analog Trunk Unit - J5D003AC-1**5.3.8 COMMON SHELF UNIT (CSU) - J5D004AG-1**

The Common Shelf Unit (CSU) is a single-shelf unit located in the top of the Integrated Service Line Unit (ISLU). Its purpose is to support all the equipment mounted in the ISLU drawer shelf units. The CSU is divided into Service Group 0 on the left and Service Group 1 on the right. Normally, both sides are active except for the Common Control circuit packs which always operate in active/standby.

Figure 5.3-13 illustrates the location of the CSU and the respective circuit packs in the unit.

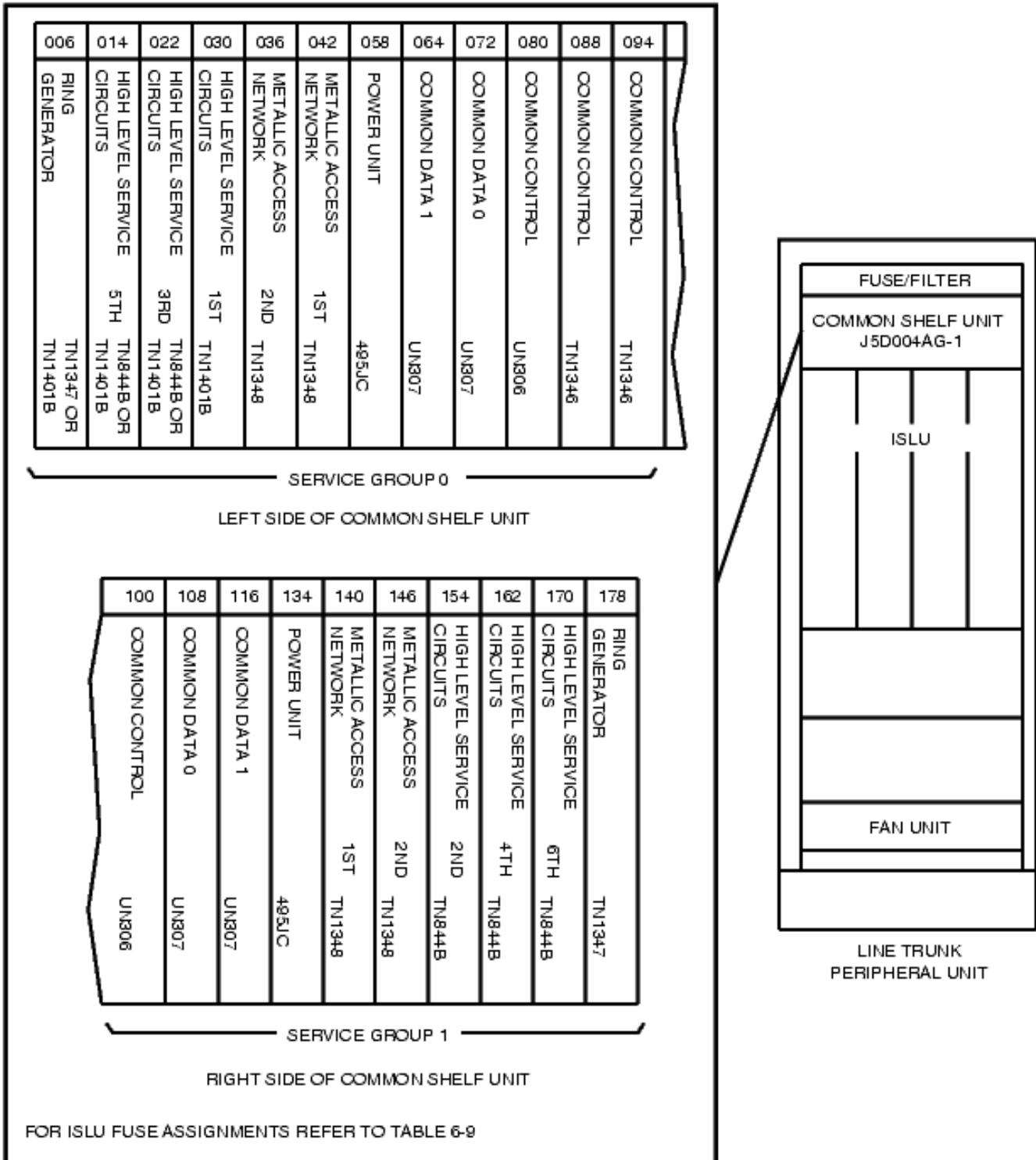


Figure 5.3-13 Common Shelf Unit - J5D004AG-1

5.3.9 DIGITAL CARRIER LINE UNITS - MODEL 2 - J5D003AR-2 (BASIC) AND J5D003AS-2 (SUPPLEMENTARY)

The basic Digital Carrier Line Unit (DCLU) is a 2-shelf unit used to interface with SLC[®] 96 carrier. It is divided into

Service Group 0 (lower shelf) and Service Group 1 (upper shelf).

The number of Digital Facility Interface (DFI) circuit packs (ANN4) required is variable depending on the number of SLC[®] carrier remote terminals involved and their use with SLC[®] carriers operating in Mode I or Mode II.

NOTE 1: Mode I (unconcentrated): Each SLC[®] carrier remote terminal requires five T1 lines; four working and one protecting. The 96 subscribers, at a remote location, are converted into a digital format and sent to the switch office by T1 lines. (24 channels x 4 T1 lines = 96 + 1 back-up T1 line.)

NOTE 2: Mode II (concentrated): Each SLC[®] remote terminal requires three T1 lines; two working and one protecting. The 96 subscribers, at a remote location, are converted into a digital format. These subscribers are also concentrated 2:1 and sent to the switch by T1 lines (24 channels X 2 T1 lines = 48 + 1 back-up T1 line).

The basic DCLU serves up to six concentrated (Mode II) SLC[®]-96 carrier remote terminals. When service for six unconcentrated (Mode I) terminals is required, use a supplementary DCLU.

The supplementary DCLU (J5D003AS-2) is a single-shelf unit which must be mounted directly above the basic DCLU.

The circuit packs ANN4 located in positions 027 through 067 (5) are associated with service group 0 and packs ANN4 in positions 129 through 169 (5) are associated with service group 1.

Figure 5.3-14 illustrates the location of the basic DCLU in the Switching Module Line Peripheral Unit and the respective circuit packs in the unit.

Figure 5.3-15 illustrates the location of the supplementary DCLU in the Switching Module Line Peripheral Unit and the circuit packs in it.

NOTE: SLC[®] Carrier Remote Terminals which are connected by fiber optic facilities do not require protect lines. Protection is built into the fiber optic facilities.

Table 5.3-2 lists equalizer circuit packs from which an appropriate selection can be made, dependent on hook-up distance to DXA and cable type.

Table 5.3-2 Equalizer Table

CIRCUIT PACK	DISTANCE TO DSX-1	DISTANCE TO DSX-1
	BAY 607C CABLE	BAY 1249 CABLE
SN215	001' to 133'	001' to 090'
SN216	134' to 267'	091' to 180'
SN217	268' to 400'	181' to 270'
SN218	401' to 533'	217' to 360'
SN219	534' to 665'	362' to 450'

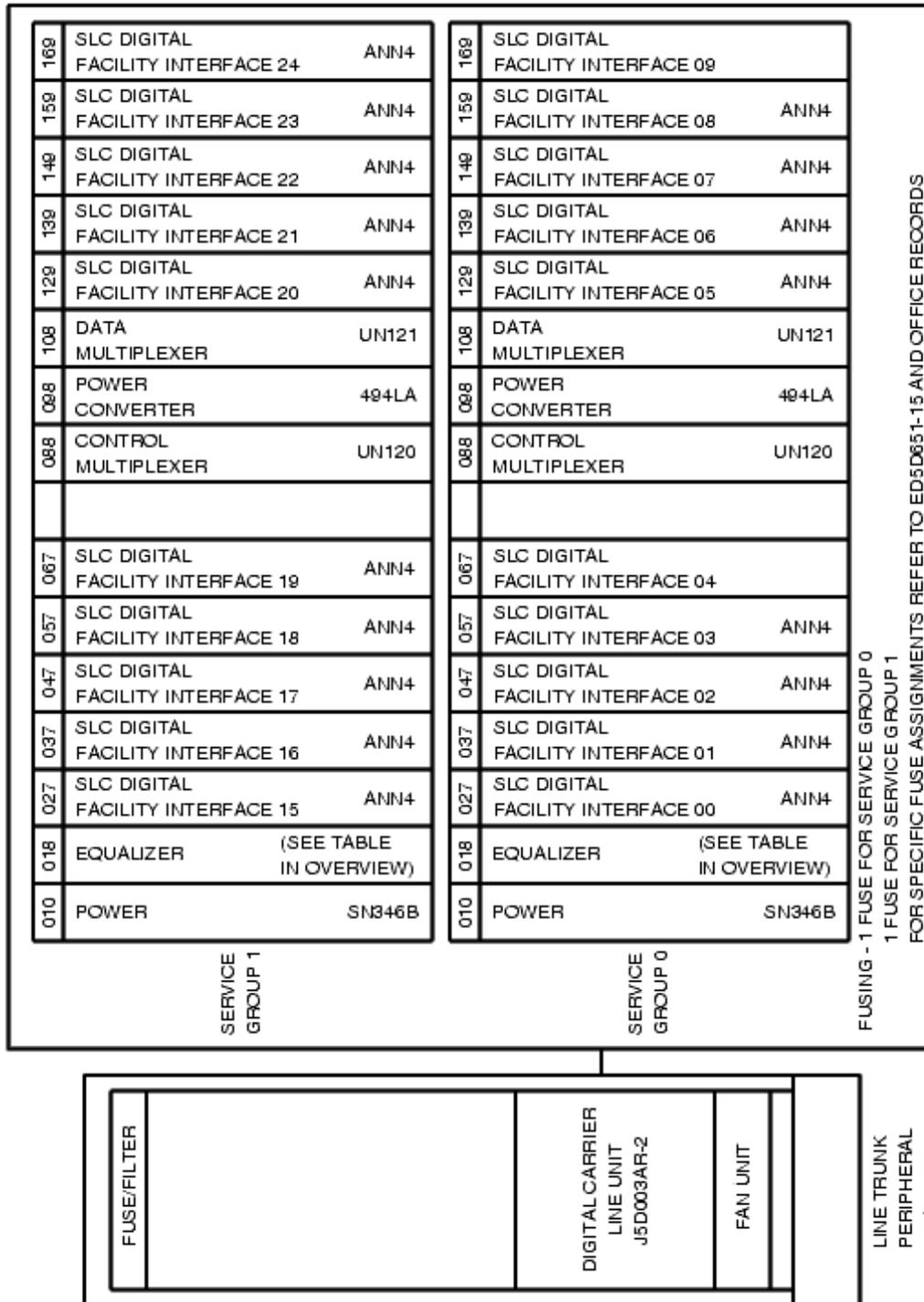


Figure 5.3-14 Basic Digital Carrier Line Unit - Model 2 - J5D003AR-2

SERVICE GROUP 1	169	SLC DIGITAL FACILITY INTERFACE 29	ANN4
	159	SLC DIGITAL FACILITY INTERFACE 28	ANN4
	149	SLC DIGITAL FACILITY INTERFACE 27	ANN4
	139	SLC DIGITAL FACILITY INTERFACE 26	ANN4
	129	SLC DIGITAL FACILITY INTERFACE 25	ANN4
SERVICE GROUP 0	067	SLC DIGITAL FACILITY INTERFACE 14	ANN4
	057	SLC DIGITAL FACILITY INTERFACE 13	ANN4
	047	SLC DIGITAL FACILITY INTERFACE 12	ANN4
	037	SLC DIGITAL FACILITY INTERFACE 11	ANN4
	027	SLC DIGITAL FACILITY INTERFACE 10	ANN4
	018	EQUALIZER	(SEE TABLE IN OVERVIEW)
	010	POWER	SN346B

FOR FUSE ASSIGNMENTS REFER TO ED5D651-15 AND OFFICE RECORDS

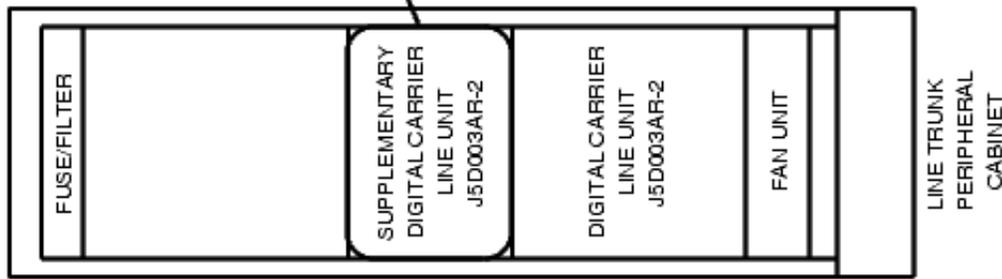


Figure 5.3-15 Supplementary Digital Carrier Line Unit - J5D003AS-2

5.3.10 DIGITAL LINE AND TRUNK UNITS

5.3.10.1 Digital Line Trunk Unit - J5D003AD-1

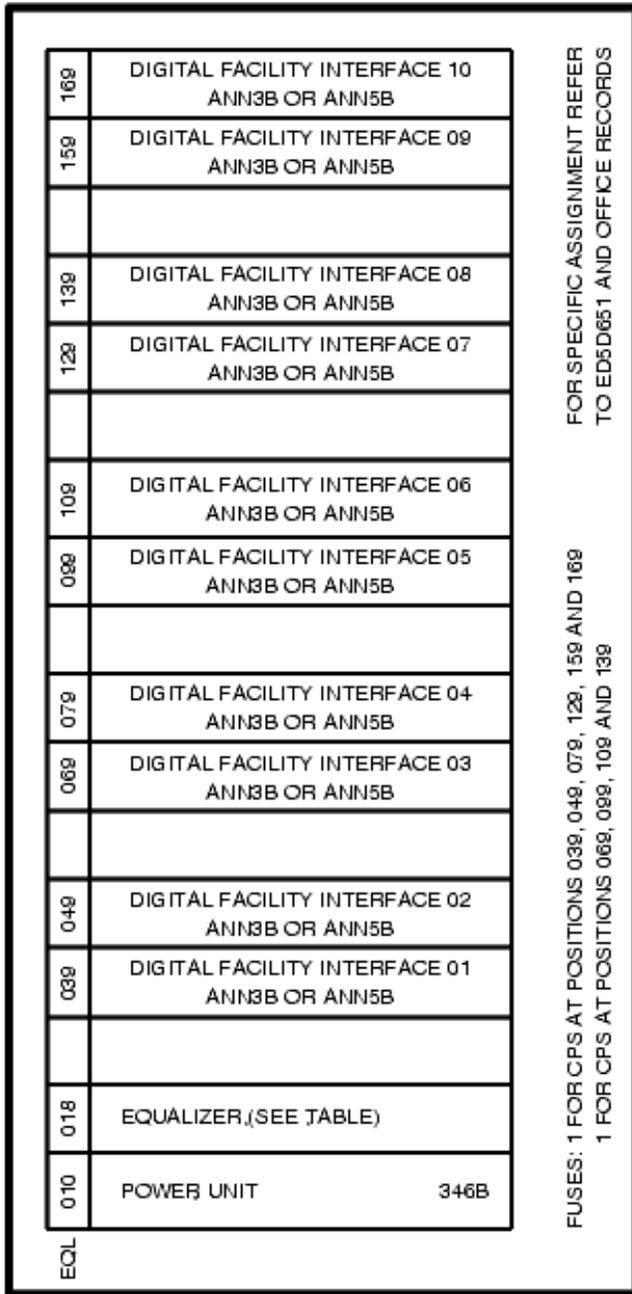
The Digital Line Trunk Unit (DLTU) is a single-shelf unit that can be mounted in any Line Trunk Peripheral cabinet in shelf position 1 through 6. It can also be mounted in any vacant shelf (1, 5 or 6) of the Switching Module Control cabinet.

The main function of the DLTU is to provide direct interfacing with digital transmission facilities. Because of time slot restrictions, a host switching module can have a maximum of two fully equipped DLTUs.

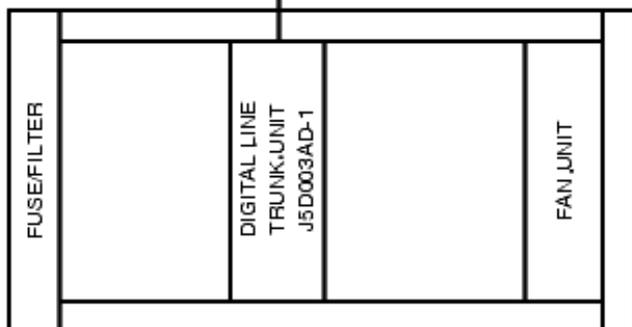
The DLTU can mount up to 10-digit Facility Interface packs, ANN3B or ANN5B.

The ANN3B pack must connect with other offices when using direct digital trunking (T1 facilities). Use the ANN5B pack when connecting to the umbilical T1 facilities of a remote switching module.

Figure 5.3-16 illustrates the location of the Digital Line Trunk Unit and the respective circuit packs in the unit.



EQUALIZER TABLE	
CIRCUIT PACK	DISTANCE TO DSX-1 BAY 607C CABLE
SN215	001' TO 133'
SN216	134' TO 267'
SN217	268' TO 400'
SN218	401' TO 533'
SN219	534' TO 665'



SWITCHING MODULE
CONTROL CABINET

Figure 5.3-16 Digital Line Trunk Unit - J5D003AD-1

5.3.10.2 Digital Line Trunk Unit - Model 2 - J5D024AA-1

The Digital Line Trunk Unit - Model 2 (DLTU2) is a single-shelf unit that can be mounted in any Line Trunk Peripheral cabinet in shelf position 1 through 6. It can also be mounted in any vacant shelf of the Switching Module Control cabinet.

The DLTU2 can mount up to 10 Digital Facility Interface (DFI) packs, TN1611 or TN1612, each capable of terminating two T1 lines. The TN1611 (DFI2-T) packs are used for trunks and the TN1612 (DFI2-R) packs interface with remote SMs.

The main function of the DLTU2 is to provide interfacing with digital transmission facilities. Because of time slot restrictions, a host switching module can have a maximum of one fully equipped DLTU2s.

Figure 5.3-17 illustrates the location of the DLTU2 and its respective circuit packs.

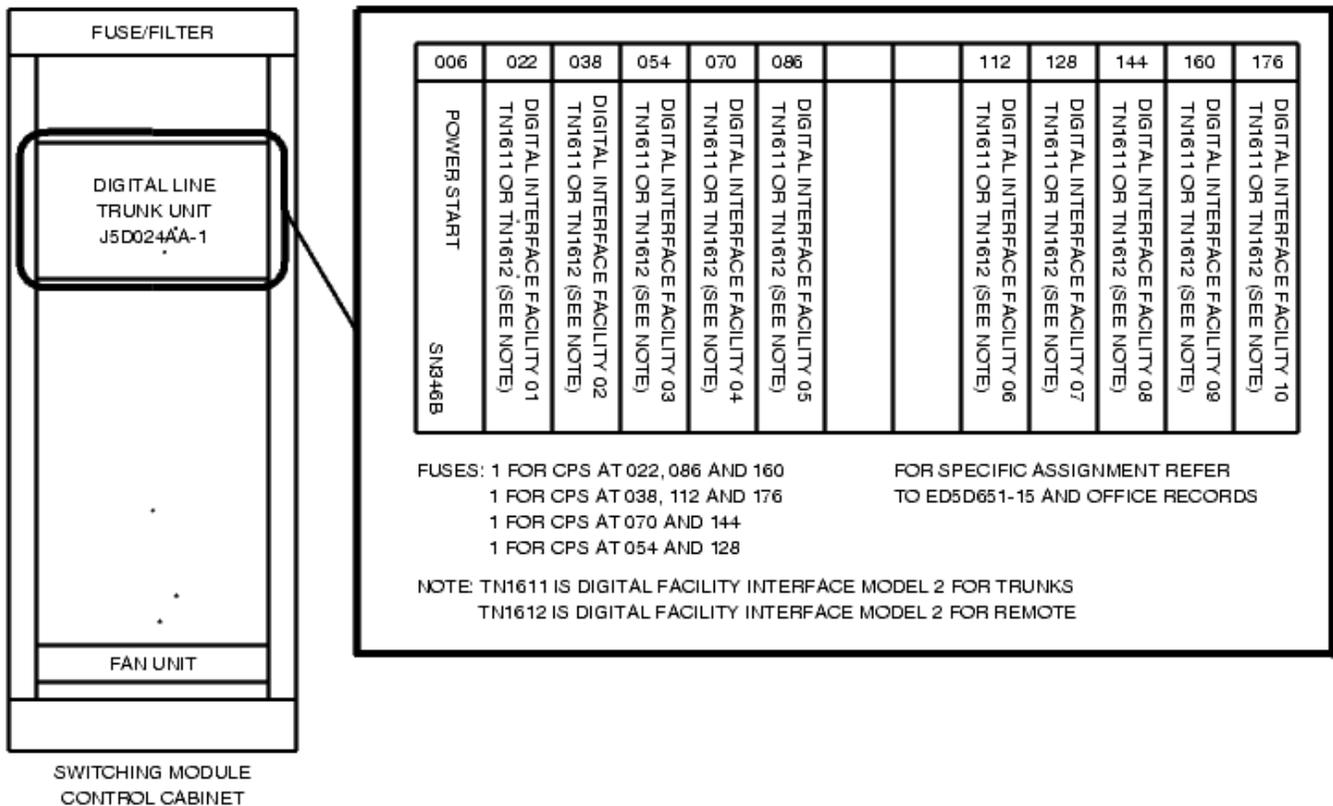


Figure 5.3-17 Digital Line Trunk Unit - Model 2

5.3.10.3 Echo Canceling Service Unit

The Echo Canceller exists on 30 channel export DFI facilities in International. Porting of Echo Canceller to the U.S. means it will be ported for 24 channel DFI/DF2 facilities. For dual facility DFIs, each facility has EC5 circuit pack associated with it.

5.3.10.3.1 Audits (AU)

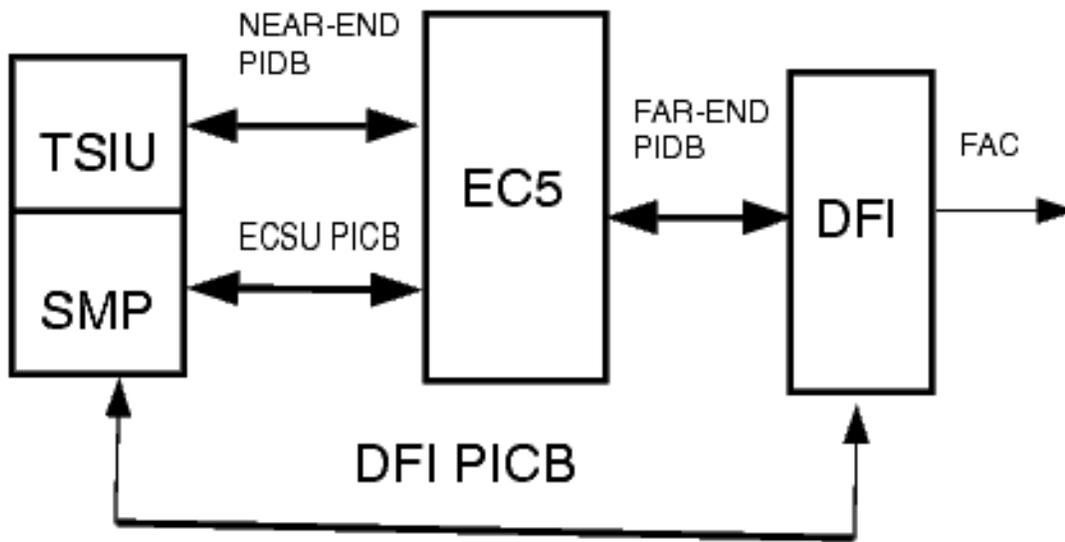
Audits (AU) will support the Echo Canceller Service Unit (ECSU) in the U.S. by porting changes to the CKTDATA,

CDBCOM, and SCNMSK audits. Changes to the CKTDATA, CDBCOM, and SCNMSK audits will include cases to audit the PCEC5 circuit type. Basically, the CKTDATA and CDBCOM audits do the same checks on the PCE5 circuit as the checks done for the PCTI_DFI circuit. The SCNMSK audit does the same checks on the PCE5 circuit as the checks done for the PCDFI circuit.

5.3.10.3.2 Peripheral Control

Peripheral Control (PC) will provide the same echo functionality to U.S. code as it is currently provided in the International code. The ECSU is the hardware that will provide the echo canceling in the 5ESS[®]-2000 switch for U.S. Generic 5E10. The signaling unit (CCITT5) part of the ESCU will not be supported in the U.S. code.

The ESCU occupies its own shelf space in the switching module. The ECSU is situated between the Time Slot Interchange Unit and the Digital Line Trunk Unit. An ECSU may contain several EC5 boards. Each EC5 interfaces with a DFI in the DLTU. A particular EC5 provides echo canceling for the channels of the interfacing DFI. Figure 5.3-18 shows the physical layout of an ECSU.



LEGEND

- TSIU - Time Slot Interchange Unit
- SWM - Switching Module Processor
- PICB - Peripheral Interface Control Bus
- PIDB - Peripheral Interface Data Bus
- EC5 - Echo Canceled Service Unit Circuit Pack
- DFI - Digital Facility Interface Circuit Pack
- FAC - Facility

Figure 5.3-18 Echo Canceled Service Unit

The ECSU and DLTU require the same service request treatment because EC5 has the same CCB structure as a DFI. They are companion circuits, and EC5 has the same CCB structure for Peripheral Fault Recovery (SMPFR) and unexpected activity or unused registers (SMERR). The canceler control code is comprised of the primitive

LPec_cntl() and the global header PCec_cntl, which is used to specify whether enabling or disabling of the echo canceler is desired.

If more information is required for the ECSU, refer to 235-200-100, *5ESS®-2000 Switch for AUTOPLEX® System 1000 Wireless Application*.

5.3.11 DIGITAL SERVICE UNITS

5.3.11.1 Introduction

The Digital Service Unit (DSU) was developed with flexible hardware so that both local and global DSUs are served by a common, optional plug-in unit. As a result of transitions brought about by software releases, there are at least five versions of the DSU in use, including Model 2.

Table 5.3-3 lists the versions by "J" drawing number.

Table 5.3-3 Digital Service Units

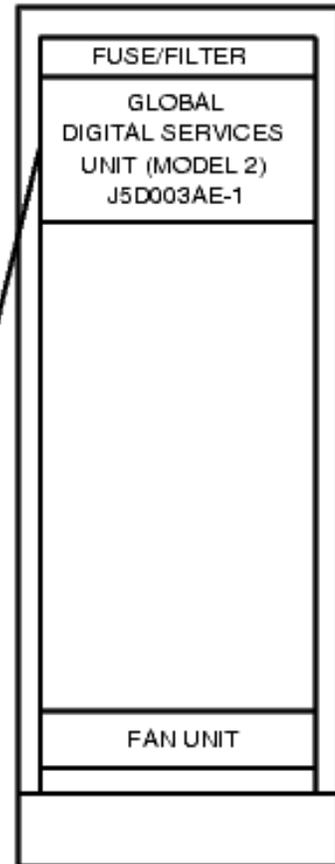
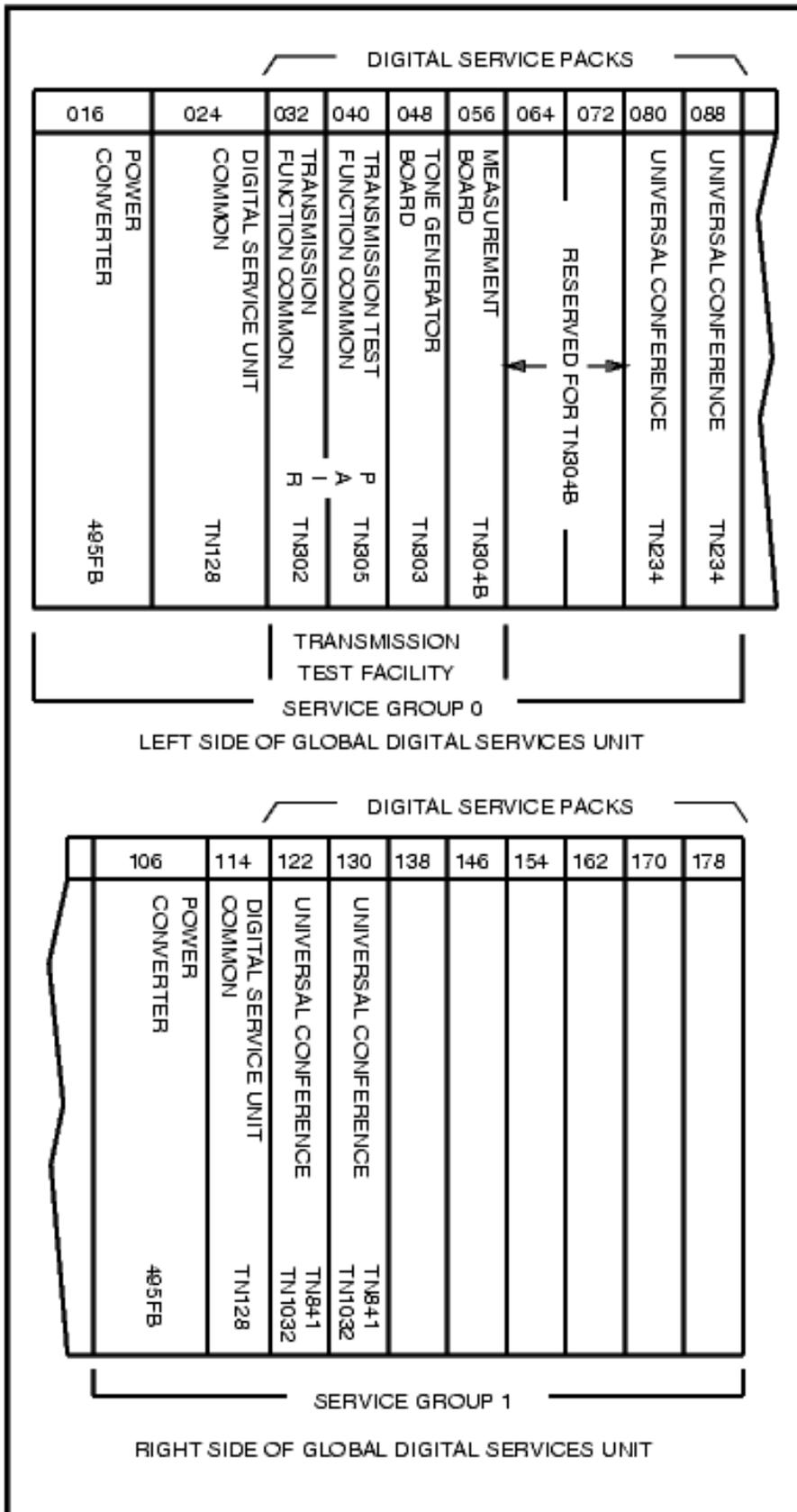
J DRAWING	FIGURE NUMBER	UNIT NAME
J5D003AE-1	5.3-19	GLOBAL DSU
J5D003AE-1	5.3-20	LOCAL DSU
J5D003AE-1	5.3-21	LOCAL DSU (modified)
J5D003EA-1	5.3-22	DSU-MODEL 2
J5D003EA-1	5.3-23	DSU-MODEL 2 (RAF)

5.3.11.2 Global Digital Service Unit - J5D003AE-1

The Global Digital Service Unit (GDSU) is a single-shelf unit that can be mounted in any vacant shelf position in the switching module control cabinet or any of the Line Trunk Peripheral cabinets. Functionally, it houses low-usage, low-level service circuits, Transmission Test Facility (TTF) and conference circuits.

The unit is divided into two service groups, 0 and 1, each independent of the other. A service group can mount up to eight digital service circuit packs.

Figure 5.3-19 illustrates the Global Digital Service Unit and the respective circuit packs in it.



FUSES:
 1 FUSE FOR SERVICE GROUP 0 -FOR SPECIFIC ASSIGNMENTS REFER TO ED5D651-15 AND OFFICE RECORDS. 1 FUSE FOR SERVICE GROUP 1

Figure 5.3-19 Global Digital Service Unit - J5D003AE-1**5.3.11.3 Local Digital Service Unit - J5D003AE-1**

The Local Digital Service Unit (LDSU) is a single-shelf unit that normally mounts directly above the Module Controller Time Slot Interchanger Unit in the Switching Module Control cabinet. The unit is divided into two service groups, 0 and 1, each independent of the other.

Functionally, the LDSU contains low-level service circuits that require high usage, such as audible ring, busy tone, high tone, multifrequency tones and touch tone.

Electronic offices sometimes connect with Panel and Crossbar offices. If this is the case, revertive pulsing may be required; replace the Digital Service Circuit (TN133) in locations 088 and 178 with a Revertive Pulsing Transceiver (TN853) pack.

Figure 5.3-20 illustrates the LDSU and the circuit packs in it.

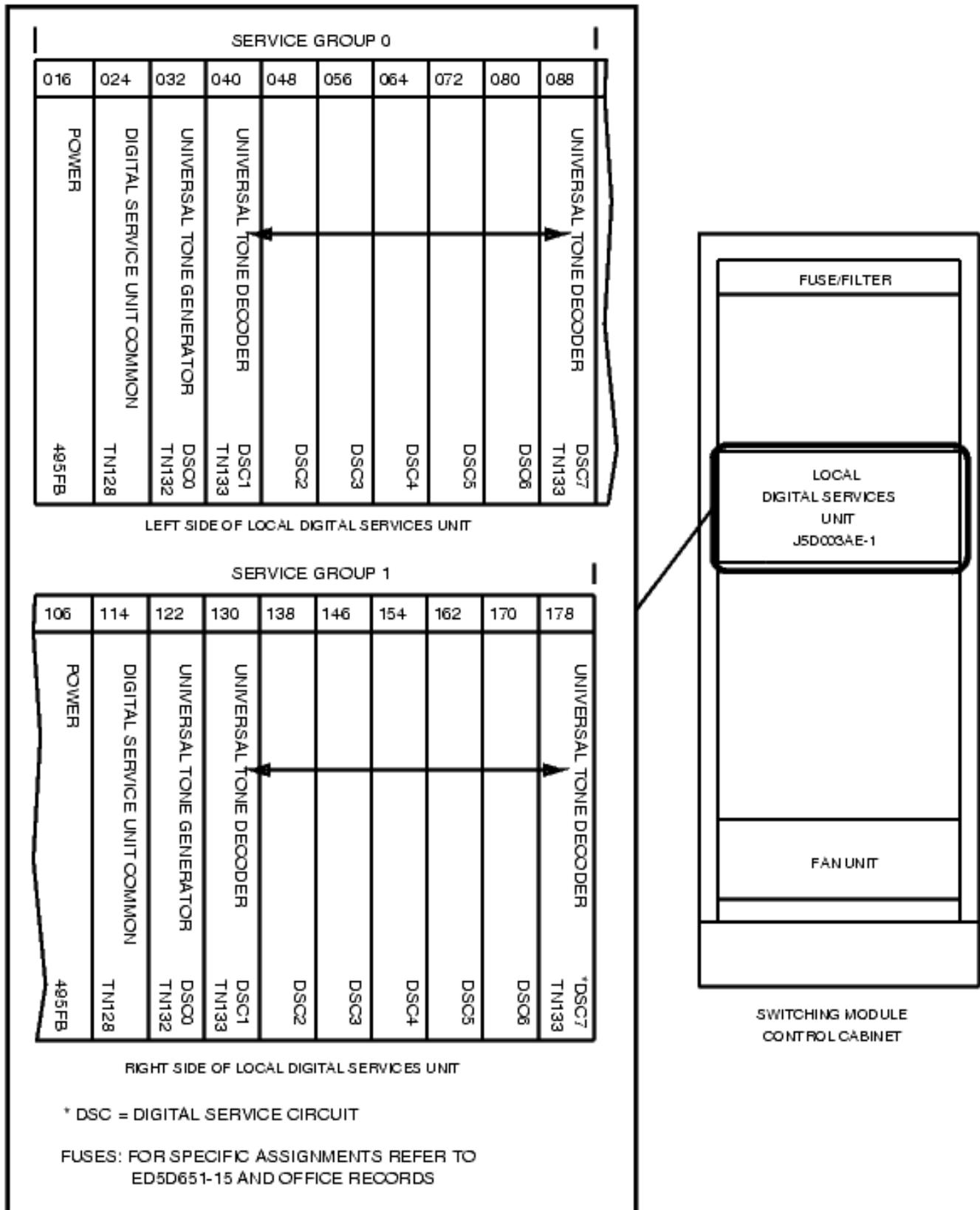


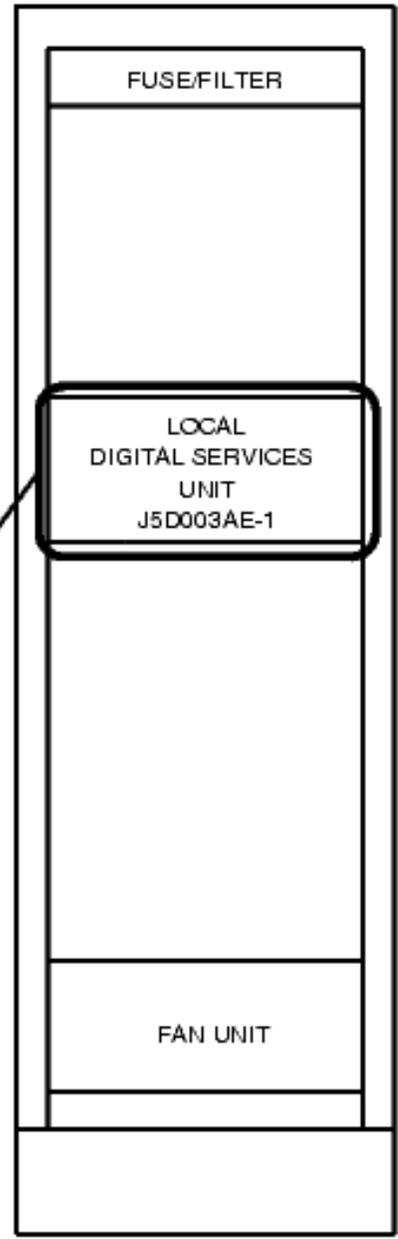
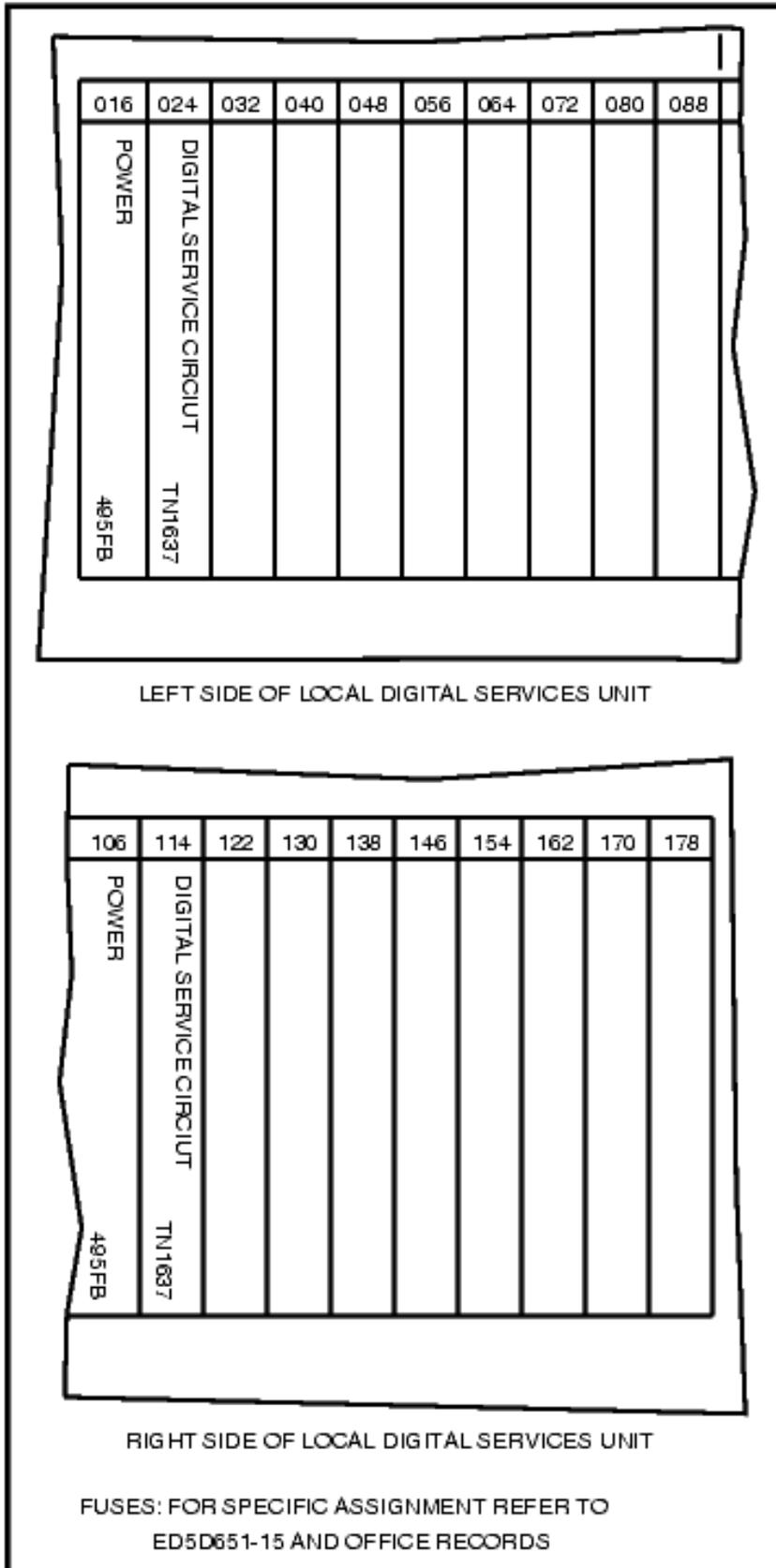
Figure 5.3-20 Local Digital Service Unit - J5D003AE-1

5.3.11.4 Local Digital Service Unit (Modified) - J5D003AE-1

The Local Digital Service Unit (Modified) (LDSUM) replaces all the Universal Tone Decoders (TN133), Universal Tone Generators (TN132) and Common Digital Service Units (TN128) in the LDSU with a single Digital Service Circuit (TN1637).

This version provides the LDSU with the functional capability supplied in the later available Model 2 DSU. Service groups 0 and 1 are still present, each independent of the other.

Figure 5.3-21 illustrates the LDSUM and its circuit packs.



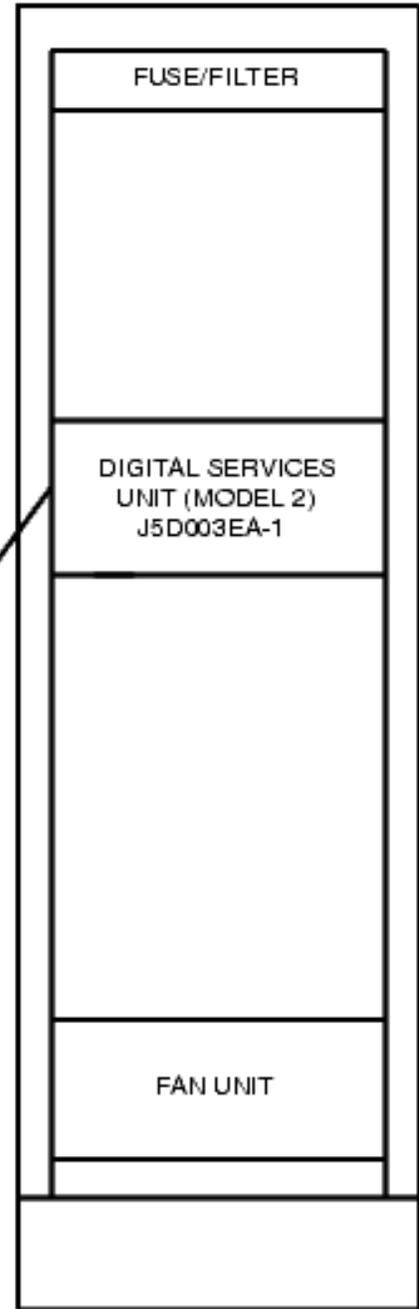
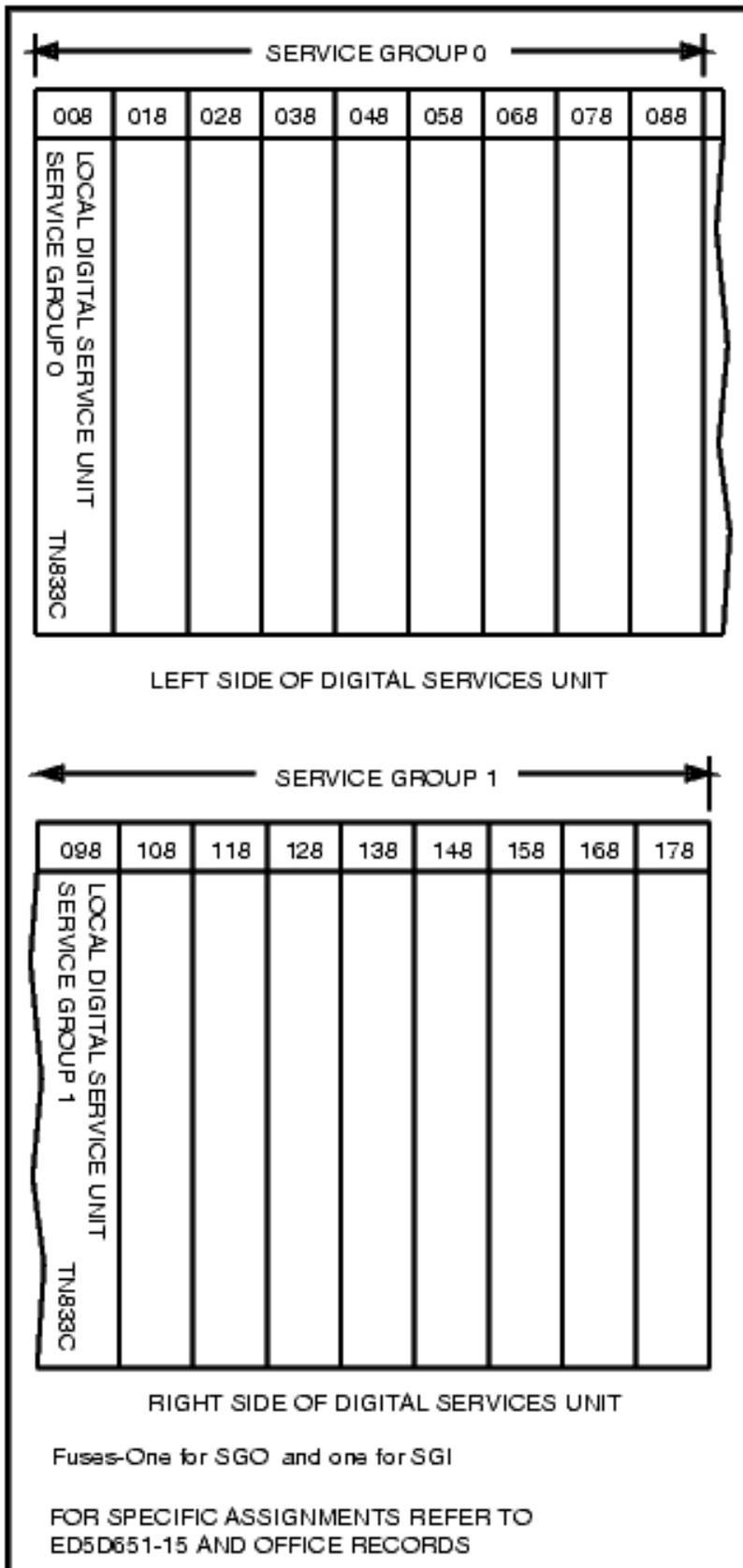
SWITCHING MODULE CONTROL CABINET

Figure 5.3-21 Local Digital Service Unit (Modified), - J5D003AE-1**5.3.11.5 Digital Service Unit - Model - J5D003EA-1**

The Digital Service Unit - Model 2 is a single-shelf unit divided into two service groups (0 and 1), each independent of the other.

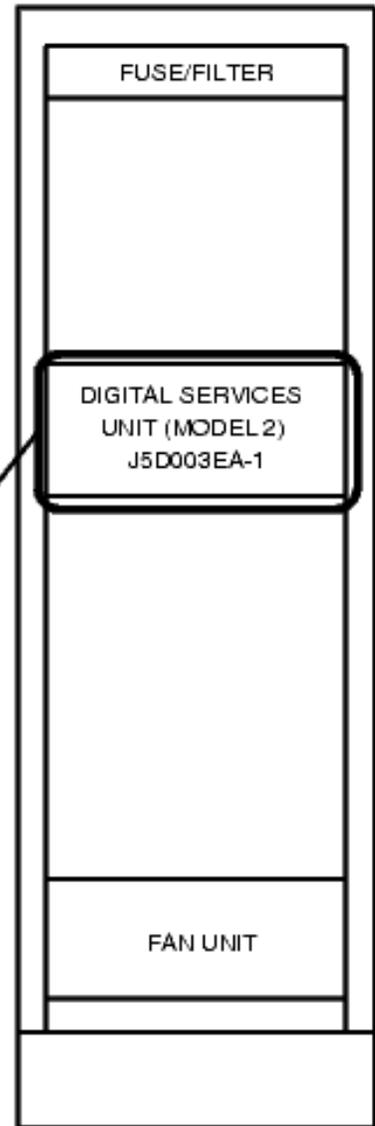
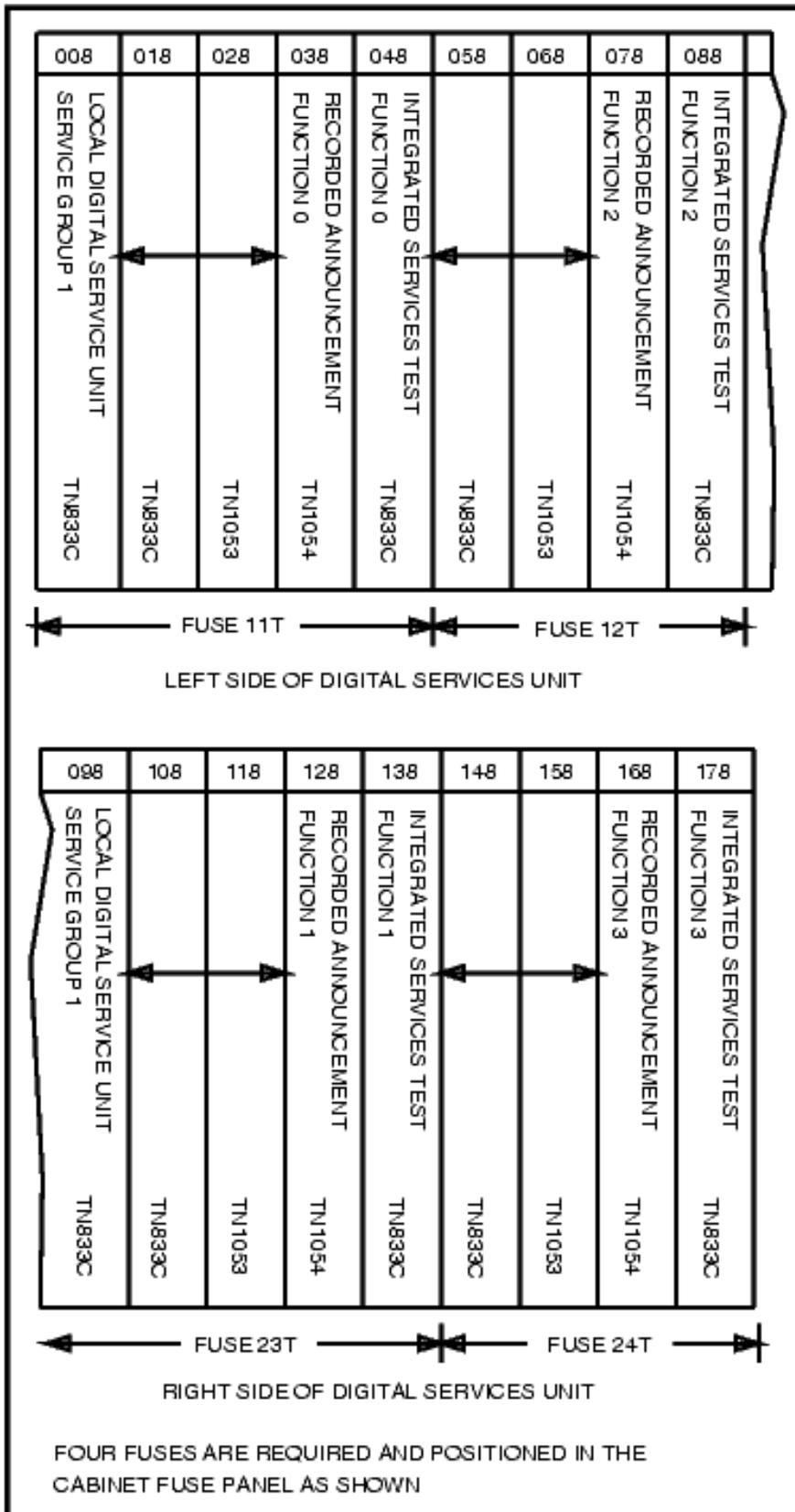
Figure 5.3-22 illustrates the location of the DSU2 and the respective circuit packs in the unit.

Figure 5.3-23 illustrates the ISDN-accommodated unit and the circuit packs in it.



SWITCHING MODULE CONTROL CABINET

Figure 5.3-22 Digital Service Unit - Model 2 - J5D003EA-1



SWITCHING MODULE CONTROL CABINET

Figure 5.3-23 DSU - Model 2 - Peripheral - J5D003EA-1**5.3.12 RECORDED ANNOUNCEMENT FUNCTION DSU2**

The Recorded Announcement Function (RAF) lets more than one caller be connected to a single RAF circuit that broadcasts a particular general recorded announcement (GRA). For each GRA announcement broadcast, at least one of the 32 circuits in a RAF unit is needed. If more callers are to be connected to the announcement than a single RAF circuit can handle, then more RAF circuits in the same or other RAF units must be assigned to broadcast the same announcement.

Figure 5.3-23 shows the location of RAF functions in the DSU2.

5.3.13 COMBINED SERVICE UNIT (CSU) - J5D003FS-1

For the 5E10 and later software releases, the Combined Services Unit (CSU) applies only to the SM (not the SM-2000). The CSU combines the DLTU2, MMSU, DSU2-SAS, and GDSF into one shelf.

The new CSU unit is compatible with existing DLTU2, DSU2-RAF2, and GDSU units in the same office, the same SM, or in different SMs. The MMSU in the repackaged version will have only one service group, thereby making it incompatible with the standard MMSU which has two service groups. Therefore, if office growth to conventional configurations necessitates greater metallic services, the standard MMSU will need to be provided and the MMSU portion of the repackaged shelf will have to be de-grown. Figure 5.3-24 illustrates the location of the CSU and the respective circuit packs in the unit.

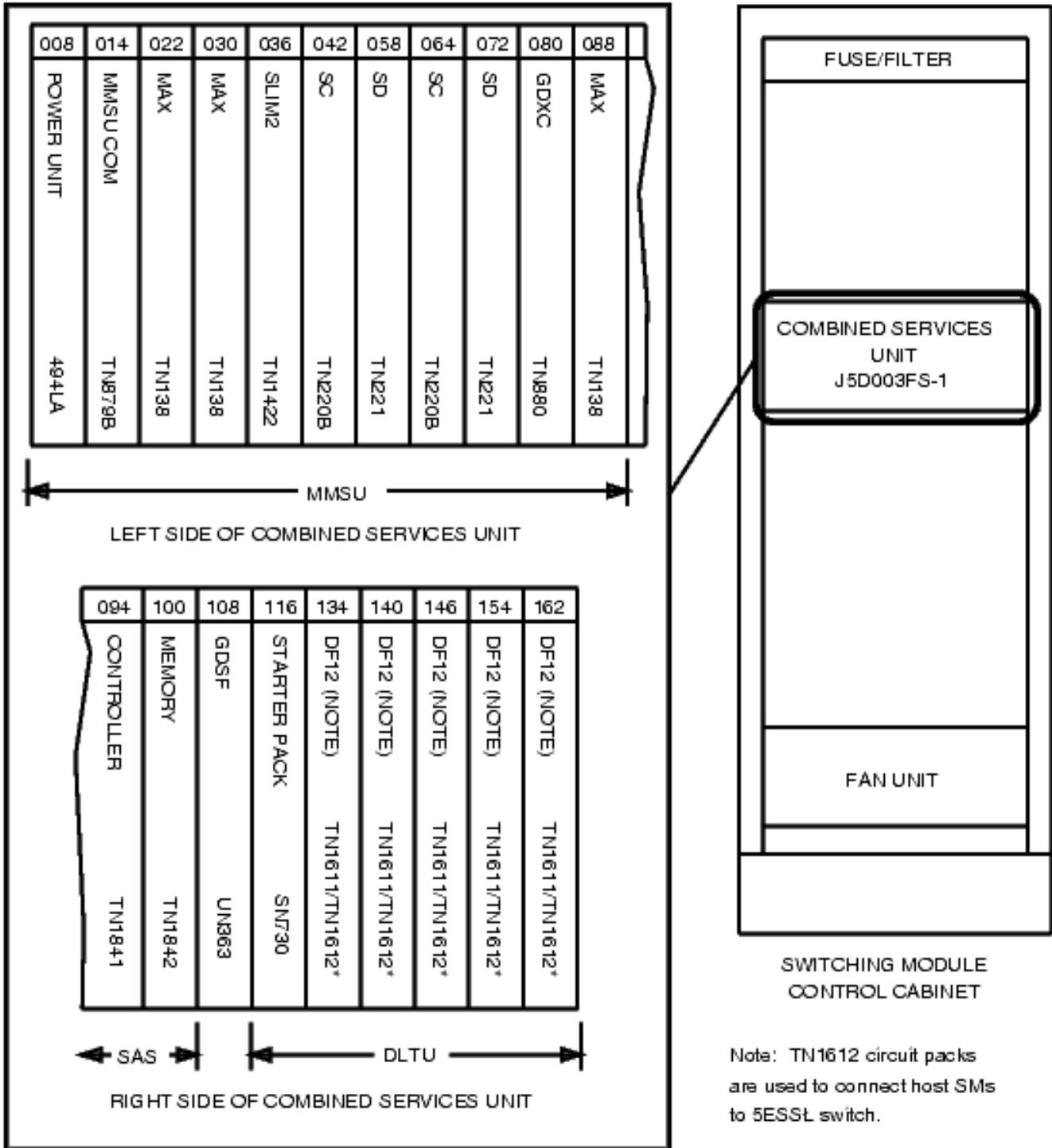


Figure 5.3-24 CSU - Peripheral - J5D003FS-1

5.3.14 SERVICE ANNOUNCEMENT SYSTEM

The Service Announcement System (SAS), and the RAF function operate in a similar way. The difference is that the SAS contains additional functions necessary to support features such as Automatic Collect Call (ACC). These new features require functions such as digit reception, and the recording and playback of a caller's name on a

per-call basis. The SAS provides these new functions in addition to all existing functions currently supported on the RAF.

An SAS unit consists of two major components: a controller board and up to four memory boards. These boards are plug-in compatible with the existing DSU2 and can be placed into any slot of the DSU2 except position 0. An SAS unit is created by placing a controller board in any slot position, except position 0, with at least one but no more than four memory boards in the slots immediately to the right of the controller board.

Like the RAF, the SAS is a global resource. A SAS unit located in a particular DSU2 is accessible from any other SM in the 5ESS®-2000 switch. An SAS unit may be mixed on the same physical DSU2 with other RAF, ISTF and TTF2 circuit packs.

SAS announcements are defined through Office Dependent Data (ODD) as a series of phrases. These phrases are stored on the memory board(s) in an SAS unit housed in a DSU2. The announcements can be changed by reconfiguring the ODD announcement definitions using the phrases already stored in the SAS unit. The memory board phrases are stored on flash memory devices.

Each SAS unit can provide up to 32 independently phased announcement channels; thus 32 separate announcements can be played or 32 copies of the same announcement can be played simultaneously. Access to any of the 32 channels of a SAS unit provides access to any of the stored announcements of an announcement set. Multiple SAS units can handle the traffic load to the announcements supported by the announcement set.

Figure 5.3-25 shows the co-existing SAS/RAF equipment locations and restrictions.

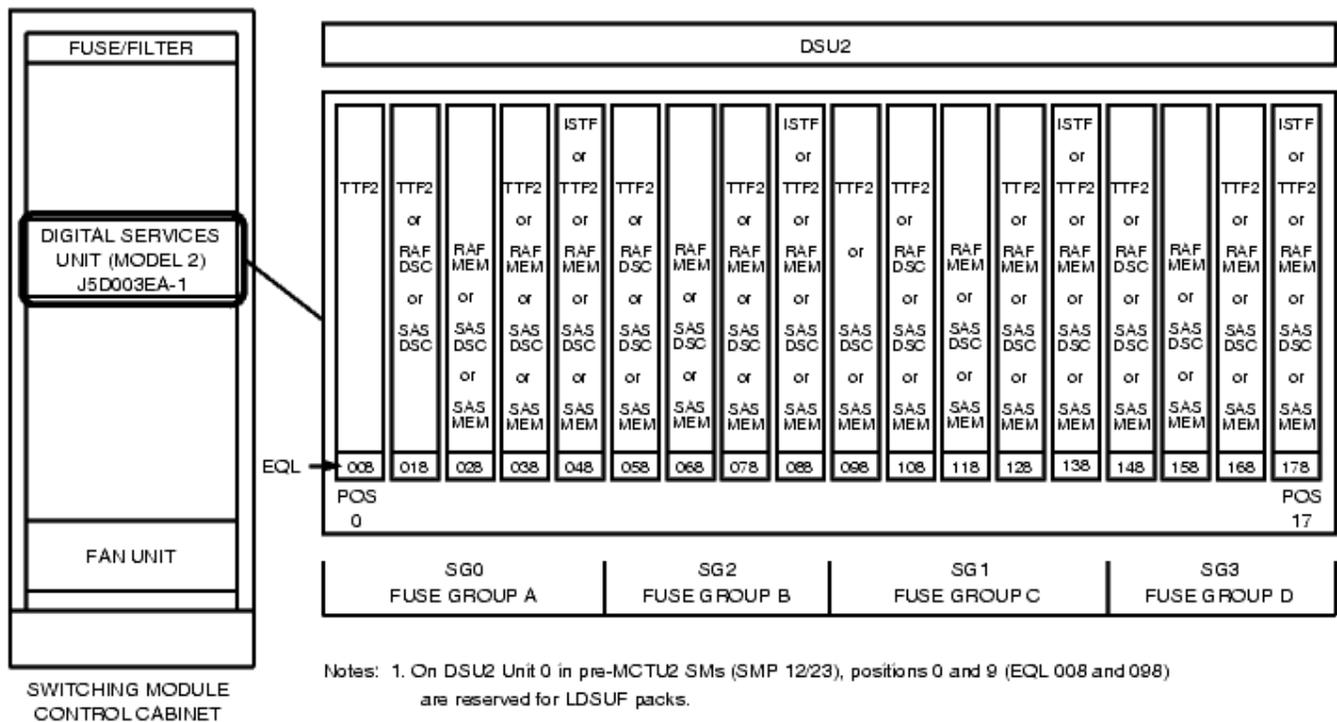


Figure 5.3-25 SAS Equipment Locations and Restrictions

Introduction of the SAS implementation in the 5E10 software release, is based on DSC3 boards. Each service group has one to four memory boards, each having slots for eight flash memory cards. These cards are PCMCIA standard memory cards, which may vary in capacity and can be used in any quantity from one through eight.

The SAS units for the 5ESS®-2000 switch are on the DSU2 units. The 5E10 units for the 5ESS®-2000 switch are

compatible with the SM-2000.

5.3.14.1 SAS Controller Board

The SAS Digital Circuit (SASDSC) controller board (TN1841) contains the Digital Signal Processors (DSPs) and provides the PICB and PIDB interface to the SM and the interface to the SAS memory board(s). Like the RAFDSC, the SASDSC can support up to 32 time slots.

5.3.14.2 SAS Memory Board

Up to four SAS Memory (SASMEM) boards (TN1842) can be installed in a SAS unit. Each SASMEM board can be equipped with up to eight PCMCIA flash memory cards of the same or varying capacity. The 4 MB flash cards provide 422 seconds of speech recording space per card, which yields 3367 seconds of recording space per memory board.

5.3.15 DIRECTLY CONNECTED TEST UNIT - J1P023AM-1

The Directly Connected Test Unit (DCTU) can be a two-, three- or four- shelf unit, depending on the size and needs of an office. The basic unit always has two shelves: the upper containing the DCTU controller, the control interface, the Equipment Access Network (EAN) circuits and the power converters; the lower containing the Precision Measuring Unit (PMU).

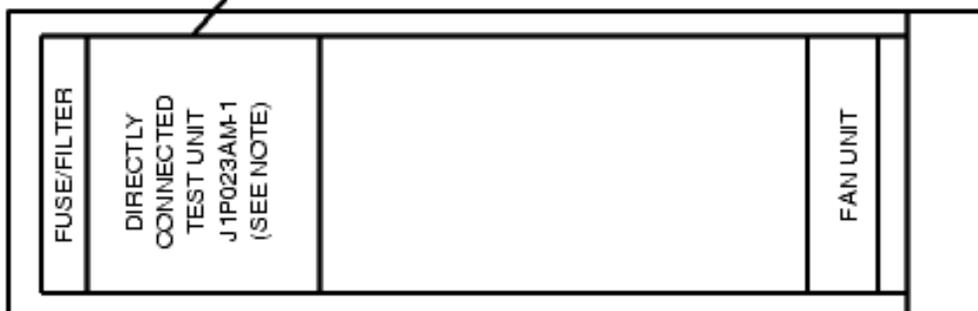
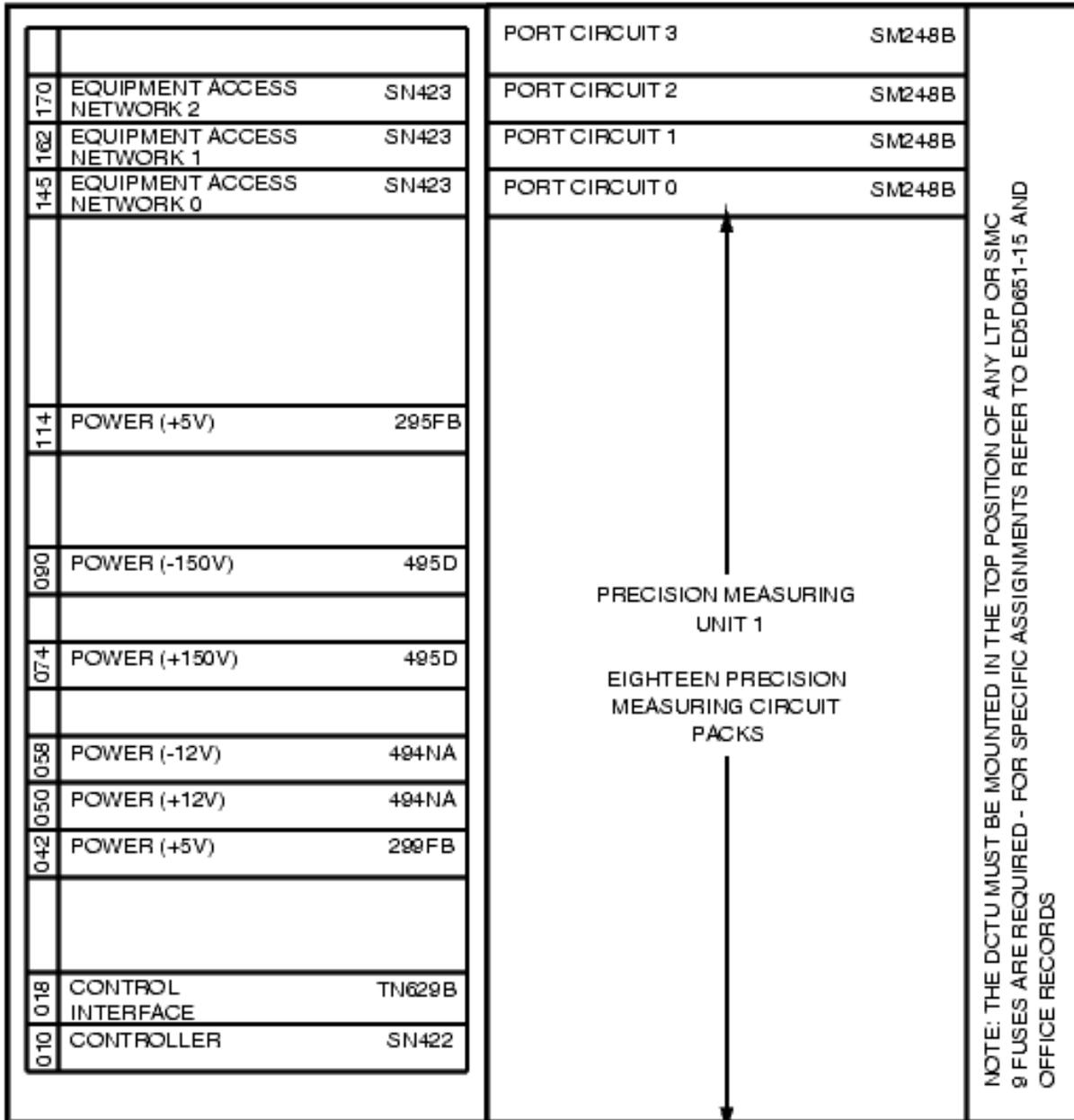
The DCTU must be mounted at the top of the cabinet. If only a basic unit is initially furnished, reserve space for two additional precision measuring units (PM02 and PM03).

The DCTU does the following:

- Performs testing of lines and trunks.
- Provides certain central office-related maintenance activities such as DC voltage, resistance and capacitance measurements, and low frequency readings of facilities.

The DCTU is dependent on the switch office for its control functions and metallic paths required to establish connections to facilities requiring the test functions.

Figure 5.3-26 illustrates the location of the Directly Connected Test Unit and the respective circuit packs in the unit.



LINE TRUNK
PERIPHERAL CABINET

Figure 5.3-26 Directly Connected Test Unit - J1P023AM-1

5.3.16 INTEGRATED SERVICES LINE UNIT

5.3.16.1 Integrated Services Line Unit (ISLU) - J5D004AK-1 SD5D089-01

The Integrated Services Line Unit (ISLU) is a three-and-one-half shelf unit that mounts in a Line Trunk Peripheral (LTP) cabinet at EQL 63 to 36. One or two ISLUs can be mounted in an LTP and one can be mounted in the top of the Switching Module Control (SMC) cabinet if space is available. If one ISLU is required in an LTP cabinet, a plenum is mounted in the remaining half space at EQL 36. If two ISLUs are located in an LTP, the second is mounted in EQL 36 to 11 and no plenum is provided. Also with two ISLUs present, no LTP fan unit is required, because each ISLU drawer contains its own fan drawer.

The ISLU provides customer interface to the switch for 2-wire analog and 2- or 4-wire digital lines. It supports coin lines with up to 1500Ω DC resistance and noncoin and PBX lines with up to 1600 Ω DC. The ISLU handles both analog and digital lines simultaneously.

The ISLUs are numbered 0 and up for each switching module (SM). Details for adding an ISLU to an SM are given on SD-5D5012-02, Figure AS 27.

An ISLU contains a Common Shelf Unit (CSU) and from one- to four- drawer shelf units. Figure 5.3-27 illustrates a "fully equipped" ISLU containing four-drawer shelf units.

Each drawer unit can mount up to four Line Groups (LGs), 00 through 15. A drawer does not have to contain four LGs before other drawers can be added. A cover is supplied for any ISLU drawer position not occupied.

Each drawer shelf unit is divided into two sides, left and right, when viewed from the front. In each drawer, the first two LGs are mounted on the left side and the next two on the right side. The backplane separates the two sides. Mounted on the front of each drawer is a label identifying the LGs in the drawer. In Figure 5.3-28, even-numbered LGs are in the lower part of the drawer and odd-number LGs are in the upper part.

Each LG comprises three basic areas, which are as follows:

- Line Cards (LC)
- Line Group Common Area
- Connector Area.

An LG can mount up to 32 Line Cards (00 to 31). Whether facing the left side or right side of a drawer unit, observe that LCs are ALWAYS numbered from left to right, with LCs 00 to 15 on the lower level and 16 to 31 on the upper level. There are three kinds of line cards that can be used and a line group can have a mix of all three. A label on the LC pull-out bar identifies each card.

When fully equipped with four LGs, a drawer has a maximum of 128 LCs, 64 on the left side and 64 on the right side. Table 5.3-4 lists the three types of line cards.

One LC is required for each subscriber.

Figure 5.3-28 illustrates the LC location layout within the Line Groups.

The Line Group Common Area consists of two types of circuit packs, the Line Group Controller (LGC) and the Line Group Power (LGP). The double-high packs are always required for each LG. Their location in the LG is illustrated in Figure 5.3-27.

Located near the rear of each ISLU Drawer Unit is a Connector Area used to terminate the flat umbilical cables from the ISLU Common Shelf. The area also terminates Line Card cabling from a connector panel on the rear of the Drawer Shelf Unit. Each drawer unit has four Connector Areas, one for each LG. Table 5.3-5 lists typical connector areas with jack number functions.

5.3.16.2 Integrated Services Line Unit 2 (ISLU2) - SD5D192-01

The operation of the ISLU2, introduced in software release 5E10, is identical to ISLU and transparent with respect to the operation of the ISLU. However, for service purposes, the two units are different. The ISLU2 contains individual line circuits in packs of 8 circuits apiece. Thus, at the pack level all eight lines must be installed or removed simultaneously. To work on individual circuits at the line level, the entire pack must be removed.

A simplified block diagram of the ISLU2 physical configuration is shown in Figure 5.3-29. The ISLU2 is configured with one common shelf and one, two, three, or four line shelves. A plenum is required when only one line shelf is equipped. As a four-shelf unit, ISLU2 consists of a common shelf and three line shelves. As a five-shelf unit, ISLU2 consists of a common shelf and four line shelves.

The ISLU2 common shelf contains the Common Control Processor (CCP), Common Control Interface (CCI), and Common Data (CD) circuit packs which control the flow of data and control information between the line circuits and the rest of the SM. There are two CCP/CCI pairs which form duplex Common Control (CC) service groups which operate in active/standby mode. There are two CD service groups, with two CD packs in each service group. The CD service groups may be operated in either active/active or active/standby modes.

The ISLU2 common shelf may also be equipped with zero through four Metallic Access Network (MAN) circuit packs, and zero through six High Level Service Circuits (HLSC). These circuit packs support metallic access to line circuits and subscriber lines for testing, and/or sparing.

The type and number of MAN, and HLSC circuit packs equipped in a unit are engineered according to the different types of lines and number of each type equipped, and the amount of traffic anticipated.

In ISLU2, the line circuits are partitioned into 16 line groups, with up to 64 lines in each group. From an exchange technician perspective, each line circuit in the unit is identified by a unique line group-line pack-line circuit designation. This designation is determined by the specific ISLU2 shelf and slot in which the line pack is plugged, and the relative position of the line circuit on the line pack.

In the ISLU2 design, eight line circuits and associated power and control circuitry are implemented on each pack. All line circuits equipped on a line pack are always the same type, i.e. U, T, or Z. W type line packs will be available for Wireless Centrex/Air Extension the first half of 1996 (1H96).

NOTE: At present, the Z interface line circuits are not supported in ISLU2.

Up to eight line packs of any type may be equipped in a line group in any combination. Since lines are equipped eight lines per pack, hardware growth/conversion must be done on an eight line basis. Note also that although the line group control architecture will support up to 64 lines of any type, care must be taken when equipping ISDN line cards to ensure that a line group is not overloaded in terms of traffic capacity.

NOTE: Cabling has to be compatible with the pack type. If the Technician is familiar with ISLU and has been equipping the cabling for T packs, then the packs can be mixed and matched on a single ISLU, with 100% utilization of Line Cards. In ISLU2 the packs cannot be interchanged without a coordinated cabling change. ISLU2 requires that specific cabling be engineered to support "U" or "T" DSLs.

5.3.16.3 Comparing ISLU2 to (R)ISLU

The ISLU2 hardware architecture is based in large part on the hardware architecture of the existing (R)ISLU. The ISLU2 differs from ISLU in the following key areas:

- The ISLU2 can support a maximum of 1024 lines, twice as many as ISLU. The line circuits are partitioned into 16 line groups. Each line group can be equipped with up to 64 lines, as compared to the 32 lines per line group maximum for ISLU.
- In ISLU2, all line group circuitry is implemented on N-sized circuit packs that are equipped in shelves, eliminating the drawer hardware and smaller KCB and KCD packs used in ISLU. In the present design eight line circuits are implemented on each pack. Line Group Control (LGC) and Line Group Power (LGP) functionality is distributed across the associated line packs. There are no separate LGC and LGP packs.
- In ISLU2, the Common Data (CD) circuit packs support a modified Line Interface Data Bus (LIDB) architecture, 64 lines per line group, and distributed LGC function.
- The Common Control Processor (CCP) and Common Control Interface (CCI) circuit packs are available for ISLU2. The ISLU2 CCP has a powerful microprocessor and more RAM than the CCP for ISLU. The ISLU2 CCI also supports the new Common Control (CC) processor bus structure. It will also have an additional Control Sequencer (CS) device that will be used in implementing control capabilities for handling up to 64 lines per line group.
- The Metallic Access Network (MAN) circuit pack is available for ISLU2. The metallic access structure implemented using the MAN pack supports the following enhanced capabilities:
 - A sparing architecture that provides less degradation in ringing and metallic testing capabilities when sparing is active, as compared to ISLU.
 - Cleaner metallic test access paths containing no active components and the ability to insert or remove additional capacitance.
 - Metallic access that supports testing at Digital Subscriber Line (DSL) transmission signal frequencies.
 - The ability to metallically isolate line packs from access buses for improved fault sectionalization.

Table 5.3-4 Line Card Characteristics

CARD	T	U	U 5E8 & LATER	Z
Circuit Pack	KCB7	KCB10	KCB17 ^a	KCB6 or KCB6B
Facility Type	4-Wire DSL	2-Wire DSL	2-Wire DSL	Analog
Line Format				Analog
Rate	144 kbps 64 kbps X 2 B Channels 16 kbps X 1 D Channel			
Switching Method	B Channel - Voice: Circuit Switched Only Data: Circuit or Packet Switched D Channel - Data: Packet Switched Only			Circuit Switched Only
Cable Loop Loss	6 dB @ 96 kHz	32 dB @ 80 kHz	42 dB @ 40 kHz	-
Outside Plant Protection	No	Yes	Yes	Yes
Standard	TSS	AT&T	ANSI [®]	AT&T
Notes:				
a. When a KCB17 Pack is mounted, the line group power pack must be A553B.				

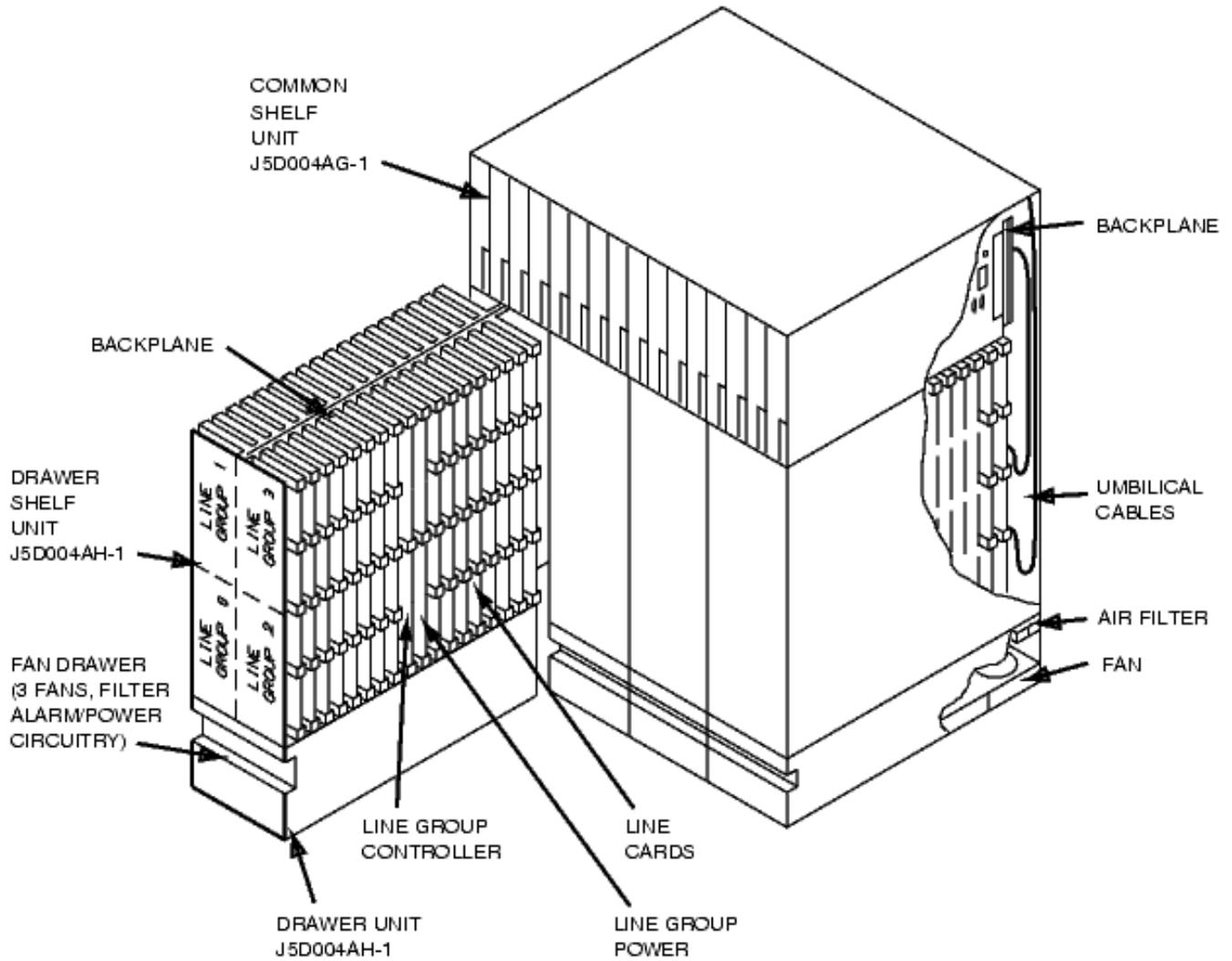


Figure 5.3-27 Integrated Service Line Unit - J5D004AK-1

LC 31	LC 15	LC 31	LC 15	178
LC 30	LC 14	LC 30	LC 14	170
LC 29	LC 13	LC 29	LC 13	163
LC 28	LC 12	LC 28	LC 12	155
LC 27	LC 11	LC 27	LC 11	148
LC 26	LC 10	LC 26	LC 10	140
LC 25	LC 09	LC 25	LC 09	133
LC 24	LC 08	LC 24	LC 08	125
LINE GROUP POWER		LINE GROUP POWER KCD2, 553A OR 553B		118
LINE GROUP KCD3 OR KCD3B CONTROLLER		LINE GROUP CONTROLLER		110
LC 23	LC 07	LC 23	LC 07	108
LC 22	LC 06	LC 22	LC 06	095
LC 21	LC 05	LC 21	LC 05	088
LC 20	LC 04	LC 20	LC 04	080
LC 19	LC 03	LC 19	LC 03	073
LC 18	LC 02	LC 18	LC 02	065
LC 17	LC 01	LC 17	LC 01	058
LC 16	LC 00	LC 16	LC 00	050

LC = LINE CARD

LG3

LG2

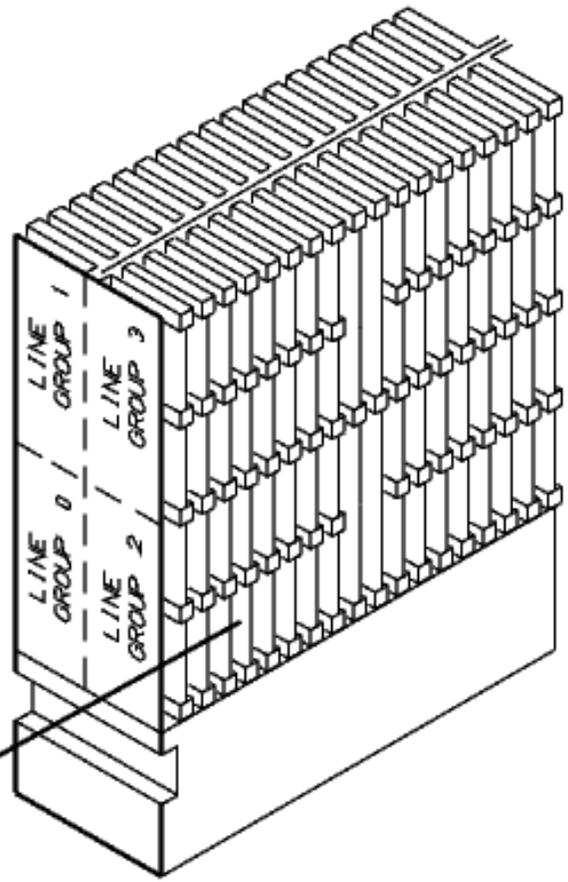


Figure 5.3-28 ISLU Line Group 2 & 3(Line Cards)

Table 5.3-5 ISLU Connectors

CONNECTORS	LINE CARDS	LEADS
J1 a	00 to 15	TIP & RING
J2 a	00 to 15	TIP1 & RING1
J3 a	16 to 31	TIP & RING
J4 a	16 to 31	TIP1 & RING1
J5	Metallic test bus leads, ringing leads and spare bus leads, (common shelf)	
J6	Line Interface Data Bus (LIDB) (common shelf)	
J7	Power leads and power distribution (common shelf)	
Loc 030 (Left Side)	Fan unit termination	
Loc 199	Fan unit termination	
Notes:		
a. Connectors J1 to J4 provide termination of the tip and ring cables for the line cards (LCs) to the connector panel located on the rear of the ISLU drawer.		

The Parallel Peripheral pump for all peripherals pumped through PICBs (Peripheral Interface Control Bus) are modified to take advantage of the multi-cast capability offered by the CI2 for peripherals behind the same CI2. For peripherals behind CI2 or multiple CI2s, asynchronous writes are used which allow the SMP to issue multiple CI orders to different CIs without waiting for the ASW. This allows the ASW to write a number of CI orders in the time it takes to write one currently. If these peripherals are equipped behind as few CI2s as possible, at most 6 CI2s are needed [for 62 ISLUs (Integrated Services Line Unit) or RISLUs (Remote Integrated Services Line Unit), with 11 ISLUs or RISLUs per CI2). Using the multi-cast and asynchronous I/O (Input/Output) all of these can be pumped in the time it takes to pump a single ISLU or RISLU, [approximately 14.1 seconds for ISLU(2) and 150 seconds for RISLU(2)s].

The peripheral offline pump is also modified to use multi-cast to improve its performance. Since multi-cast uses a special PICB number to perform CI operations, this should neither impact any operational actions nor cause side-effects from maintenance interrupts. However, asynchronous CI operations are not used by the peripheral offline pump to avoid any side effects resulting from e.g., maintenance interrupts.

5.3.18 LINE UNITS - MODEL 2 (J5D004AC-2) AND MODEL 3 (J5D004AD-2)

Line Units 2 and 3 are two-shelf units that can be located in any available shelf location in any Line Trunk Peripheral cabinet.

The Line Unit provides an interface between customer lines and the Time Division Switching Network. Its two main functions are to provide subscriber line concentration and "BORSCHT" functions. The functions are defined as follows:

- **Concentration:** Refers to a relationship between subscriber terminations and time slot assignments. A fully assigned grid serves for 64 subscribers, terminated in two, half-grid circuit packs, each pack serving 32 subscribers. The total number of subscribers assigned to a Line Unit is office engineered and dependent on the number of grids equipped. Line Units 2 and 3 can terminate up to 640 subscribers.

Table 5.3-6 illustrates the subscriber/time slot ratio.

- **BORSCHT:** Service group functions contained in this coded reference are described as follows:

B - Battery feed, including all needed DC-to-DC converters for generating required voltages.

O - Overvoltage protection for power crosses, lightning surges, etc.

R - Ringing, coin control and other high-level service circuit functions.

S - Supervisory functions, such as on-hook/off-hook detection, call origination, dial pulses, ring trip, etc.

C - CODE C or code/decode analog-to-digital and digital-to-analog conversion.

H - Hybrid or 2-wire to 4-wire coupling and vice versa.

T - Test access to the Metallic Test Bus (MTB).

Line Units, Models 2, 3, and 4 are illustrated in Figures 5.3-30, 5.3-31 and 5.3-32. Model 2 J5D004AC-2 has Subscriber to Time Slot ratios of 4:1, 6:1 and 8:1. Model 3 J5D004AD-2 has ratios of 4:1, 6:1, 8:1 and 10:1.

Half-grid circuit packs (such as TN1048) are selected locally to satisfy secondary protection needs. The three types that may be selected from are TN1048, TN838 and TN1058. Both TN1048 and TN838 are shown in the figures as typical.

The KTU4 (Common Control, Data and Power Board) replaces the 4996B and UN322 that are used in LU3, while

KTU6, an alternate to KTU4, provides an additional redundant 48 V power supply and acts as a single Line Unit from either feeder. This alternate circuit pack is helpful if the wrong fuse is accidentally pulled. The alternate KTU8 High-Level Service Circuit board has the functions of three TN844s; the KTU9 has the functions of two TN844s.

Table 5.3-6 Subscriber/Time Slot Assignments

NO. SUBS.	NO. GRIDS	TIME SLOTS OUT	RATIO
256	0 to 3	64	4:1
384	0 to 5	64	6:1
512	0 to 7	64	8:1
640	0 to 9	64	10:1

EQL		SERVICE GROUP 1												SERVICE GROUP 0													
		CONCENTRATION												CONCENTRATION													
008		POWER UNIT						494GB						008		POWER UNIT						494GB					
016		HIGH LEVEL SERVICE CIRCUI T 0						TN844						016		HIGH LEVEL SERVICE CIRCUI T 0						TN844					
024		HIGH LEVEL SERVICE CIRCUI T 1						TN844						024		HIGH LEVEL SERVICE CIRCUI T 1						TN844					
032		HIGH LEVEL SERVICE CIRCUI T 2 (OPTIONAL)						TN844						032		HIGH LEVEL SERVICE CIRCUI T 2 (OPTIONAL)						TN844					
038		ELECTRICAL-MECHANICAL INDUCTION SHIELD												038		ELECTRICAL-MECHANICAL INDUCTION SHIELD											
046		CHANNEL 0-7						TN335C						046		CHANNEL 0-7						TN335C					
054		CHANNEL 8-15						TN335C						054		CHANNEL 8-15						TN335C					
062		CHANNEL 16-23						TN335C						062		CHANNEL 16-23						TN335C					
070		CHANNEL 24-31						TN335C						070		CHANNEL 24-31						TN335C					
078		COMMON DATA						TN842B						078		COMMON DATA						TN842B					
086		COMMON DATA						TN843						086		COMMON DATA						TN843					
096		GATED DIODE CROSSPOINT ACCESS 31						TN831B						096		GATED DIODE CROSSPOINT ACCESS 31						TN831B					
104		GATED DIODE CROSSPOINT ACCESS 32						TN832B						104		GATED DIODE CROSSPOINT ACCESS 32						TN832B					
112		HALF-GRID 40						GRID 4						112		HALF-GRID 00						GRID 0					
120		HALF-GRID 41						GRID 4						120		HALF-GRID 01						GRID 0					
128		HALF-GRID 50						GRID 5						128		HALF-GRID 10						GRID 1					
136		HALF-GRID 51						GRID 5						136		HALF-GRID 11						GRID 1					
144		HALF-GRID 60						GRID 6						144		HALF-GRID 20						GRID 2					
152		HALF-GRID 61						GRID 6						152		HALF-GRID 21						GRID 2					
160		HALF-GRID 70						GRID 7						160		HALF-GRID 30						GRID 3					
168		HALF-GRID 71						GRID 7						168		HALF-GRID 31						GRID 3					

FUSING: 12 FUSES REQUIRED. FOR SPECIFIC ASSIGNMENTS REFER TO ED5D651-15 AND OFFICE RECORDS.

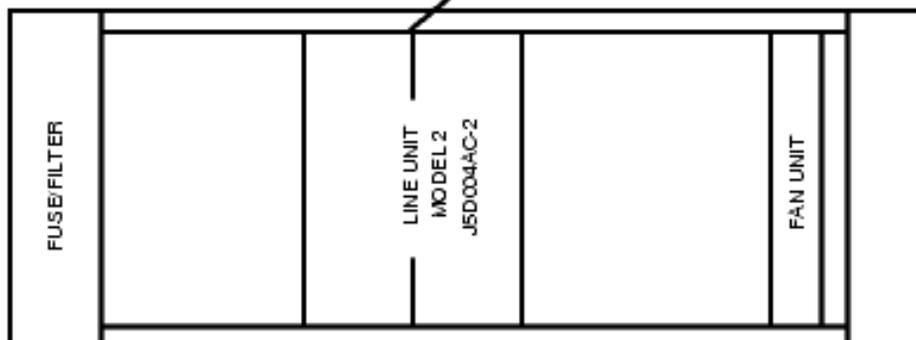
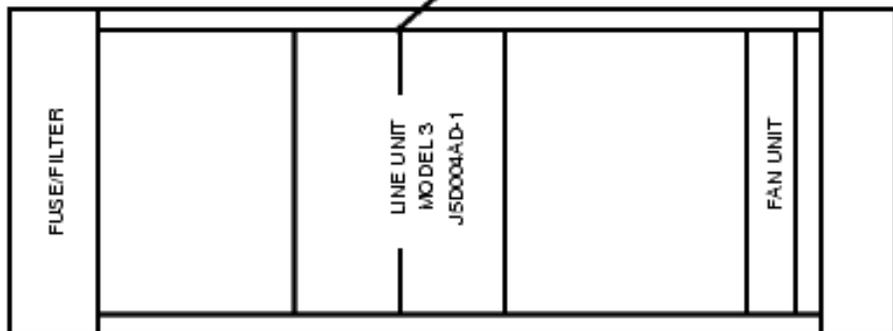


Figure 5.3-30 Line Unit Model 2 - J5D004AC-2

SERVICE GROUP 1		CONCENTRATION				SERVICE GROUP 0									
		1	100	108	116			124	132	140	148	156	164	172	
		HALF GRID 10	TN1048	HALF GRID 01	TN1048			HALF GRID 20	TN1048	HALF GRID 40	TN1048	HALF GRID 60	TN1048	HALF GRID 80	TN1048
		HALF GRID 11	TN1048	HALF GRID 00	TN1048			HALF GRID 21	TN1048	HALF GRID 41	TN1048	HALF GRID 61	TN1048	HALF GRID 81	TN1048
		GRID 1	TN1048	GRID 0	TN1048			GRID 2	TN1048	GRID 4	TN1048	GRID 6	TN1048	GRID 8	TN1048
		HALF GRID 30	TN1048	HALF GRID 20	TN1048			HALF GRID 40	TN1048	HALF GRID 60	TN1048	HALF GRID 80	TN1048	HALF GRID 90	TN1048
		HALF GRID 31	TN1048	HALF GRID 21	TN1048			HALF GRID 41	TN1048	HALF GRID 61	TN1048	HALF GRID 71	TN1048	HALF GRID 91	TN1048
		GRID 3	TN1048	GRID 2	TN1048			GRID 4	TN1048	GRID 6	TN1048	GRID 7	TN1048	GRID 9	TN1048
		HALF GRID 50	TN1048	HALF GRID 40	TN1048			HALF GRID 60	TN1048	HALF GRID 80	TN1048	HALF GRID 70	TN1048	HALF GRID 90	TN1048
		HALF GRID 51	TN1048	HALF GRID 41	TN1048			HALF GRID 61	TN1048	HALF GRID 81	TN1048	HALF GRID 71	TN1048	HALF GRID 91	TN1048
		GRID 5	TN1048	GRID 4	TN1048			GRID 6	TN1048	GRID 8	TN1048	GRID 7	TN1048	GRID 9	TN1048
		HALF GRID 70	TN1048	HALF GRID 60	TN1048			HALF GRID 80	TN1048	HALF GRID 90	TN1048	HALF GRID 70	TN1048	HALF GRID 80	TN1048
		HALF GRID 71	TN1048	HALF GRID 61	TN1048			HALF GRID 81	TN1048	HALF GRID 91	TN1048	HALF GRID 71	TN1048	HALF GRID 81	TN1048
		GRID 7	TN1048	GRID 6	TN1048			GRID 8	TN1048	GRID 9	TN1048	GRID 7	TN1048	GRID 8	TN1048
		HALF GRID 90	TN1048	HALF GRID 80	TN1048			HALF GRID 90	TN1048	HALF GRID 91	TN1048	HALF GRID 90	TN1048	HALF GRID 91	TN1048
		HALF GRID 91	TN1048	HALF GRID 81	TN1048			HALF GRID 91	TN1048	HALF GRID 91	TN1048	HALF GRID 91	TN1048	HALF GRID 91	TN1048
		SERVICE GROUP 1		082	GATED DIODE CROSSPOINT ACCESS			TN832B	082	GATED DIODE CROSSPOINT ACCESS	TN832B				
				084	GATED DIODE CROSSPOINT ACCESS			TN831B	084	GATED DIODE CROSSPOINT ACCESS	TN831B				
074	COMMON DATA COMMON CONTROL			UN322	074	COMMON DATA COMMON CONTROL	UN322								
066	CHANNEL 24-31			TN335C	066	CHANNEL 24-31	TN335C								
058	CHANNEL 16-23			TN335C	058	CHANNEL 16-23	TN335C								
050	CHANNEL 8-15			TN335C	050	CHANNEL 8-15	TN335C								
042	CHANNEL 0-7			TN335C	042	CHANNEL 0-7	TN335C								
038	GROUND SHIELD				038	GROUND SHIELD									
032	HIGH LEVEL SERVICE CIRCUIT 2			TN844	032	HIGH LEVEL SERVICE CIRCUIT 2	TN844								
024	HIGH LEVEL SERVICE CIRCUIT 1			TN844	024	HIGH LEVEL SERVICE CIRCUIT 1	TN844								
SERVICE GROUP 1		016	HIGH LEVEL SERVICE CIRCUIT 0	TN844	016	HIGH LEVEL SERVICE CIRCUIT 0	TN844								
		008	POWER UNIT	494GB	008	POWER UNIT	494GB								
		EQL		EQL											

FUSING: 14 FUSES REQUIRED. FOR SPECIFIC ASSIGNMENTS REFER TO EDS0651-15 AND OFFICE RECORDS.



LINE TRUNK PERIPHERAL CABINET

Figure 5.3-31 Line Unit Model 3 - J5D004AD-1

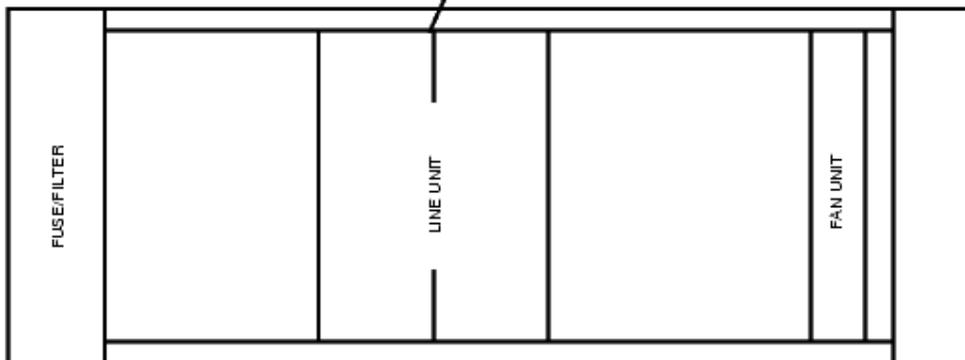
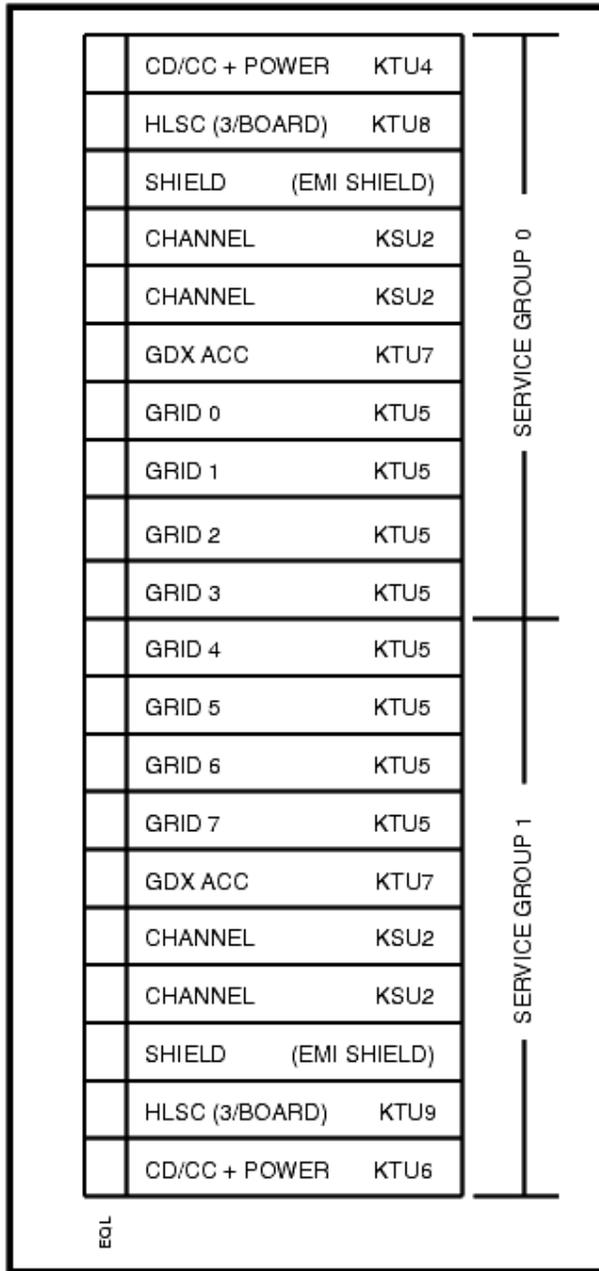


Figure 5.3-32 Line Unit Model 4 - J5D004AN-1 16-inch Shelf Unit

5.3.19 ACCESS INTERFACE UNIT

The AIU (Access Interface Unit) is a new unit that provides functionality found in Line Units and ISLUs previously described. All common equipment is centralized on a single COMDAC (COMMon DATA and Control) circuit pack, one for each service group. All remaining packs are Application Packs (APs). In the initial release of AIU the only application packs supported are Line Packs (LPs), Ringing Generators (RGs).

The COMDAC provides a control interface between the SMP and the application packs. In addition, the COMDAC contains a space switch providing a mapping and concentration function of the time slots from the application packs onto the PIDBs. The two COMDACs normally operate in an ACT-ACT mode, where each COMDAC serves half the APs. The APs provide the interface to subscriber lines. The AIU provides a LP for the analog (Z) interface and another LP for the analog interface with 12/16 KHz PPM. The POTS Z-pack supports 32 lines with per-line Codec functionality. The PPM AP supports up to 24 lines. Each of the LPs provides a time switch allowing any line circuit to be connected to any time slot on the AP-COMDAC data bus.

The ISDN "U" Application Pack provides Basic Rate Access (BRA)/Basic Rate Interface (BRI) and can be provisioned with up to two 64 Kbps "B channels" and one 16 Kbps "D channel".

5.3.19.1 Application Pack

Any type of Application Pack may be equipped in any Application Pack position within the unit. Thus the physical backplane interface is the same for each AIU Application Pack. Each type of Application Pack provides a self ID feature that contains the pack code and serial number.

5.3.19.2 Data Interface

The data interface format is 32 time slots of 16 bits each (4.096 MHz). This interface consists of a 4.096 MHz clock signal, a Frame sync, data up (towards the COMDAC) and data down (towards the Application Pack). Each Application Pack slot has its own data interface.

The Application Packs contain elastic stores (or their equivalent) to send and receive data to and from either COMDAC (both operating at the same frequency, but possibly at different phases) on any of the 32 time slots.

5.3.19.3 Control Interface

The control Interface for the Application Packs is through a 256K bit UART. The interface between the Application Pack and each COMDAC consists of the following signals:

- Clock
- Sync
- Data Up (toward the COMDAC)
- Data Down (toward the Application Pack)
- Control Up (toward the COMDAC)
- Control Down (toward the Application Pack)
- Select
- Reset

Application Packs have the capability to loop back any time slot for test purposes.

5.3.19.4 Ringing

The POTS analog line AP has two ringing inputs, selected by a register bit written through a UART (Universal Asynchronous Receiver Transmitter) message. Ring trip is per line.

NOTE: AIU does not support multi Party Ringing or Multi Party Lines. The reason the AIU does not support multi party lines is due to the way the ringing bus is designed.

5.3.19.5 Metallic Test

Application Packs have access to only one metallic test bus. Each COMDAC has an incoming MTB (Metallic Test Bus), but only one will connect its MTB to the internal general purpose bus. The POTS Line Pack hardware design supports both test-in and test out, which can be provided simultaneously with two general purpose buses for use in the *SLC*[®]-2000 application.

If the R/EAIU is beyond metallic testing range, (3000 Ohms), or no metallic pair is available, to test AP for the remote site should be considered. The AIU can be equipped with an Application Test Pack that performs SLIM-2 like test functions. It is controlled from the RCOMDAC and provides integrated testing with the rest of the *5ESS*[®]-2000 Switch. A Test Application Pack can provide testing capability for up to 8 RAIUs at the same logical remote site (the logical remote site is defined in the ODD). Only one Test Application pack may be equipped per logical remote site. Multiple logical remote sites may be physically co-located. If a test pack is not equipped, external test equipment may also be considered.

5.3.19.6 POTS

The Analog Line Packs provide a tip and ring interface to analog subscriber lines, which includes the BORSCHT functions. The BORSCHT functions provided by the line circuits are battery feed, overvoltage protection, ringing access and ring trip, supervision, CODEC (A-to-D and D-to-A conversion), hybrid (4-wire to 2-wire conversion), and loop testing access.

The Z Line Packs (POTS) support 32 subscriber line interface circuits per pack. If ISDN customers are supported, D Channel access and B Channel support must be provisioned before other customers will have access.

5.3.19.7 PPM

In addition to the POTS analog interface, special Line Packs to support 12 kHz and 16 kHz Periodic Pulse Metering (PPM) are provided. These packs generate the PPM tones, provide the capability to diagnose the PPM hardware, and support the same BORSCHT functions as the POTS lines.

Coin Pack terminate up to 16 analog coin or POTS customers. If more than one coin pack is equipped, balancing the coin packs between odd and even pack positions is recommended. This will equalize path hunting between major and minor (R)COMDAC.

Figure 5.3-33 illustrates the location of the Access Interface Unit in the Switching Module Control Cabinet and the respective Circuit Packs in the unit.

5.3.19.8 Power

Each AIU circuit pack converts -48 volts to +5 volts (or other required voltages) locally.

Each AIU circuit pack has a surface mount (non-field replaceable) fuse on its incoming -48 volts. This fuse is not intended to replace the fuse/filter unit, but only to prevent flame and smoke in case of a component failure on the

circuit pack.

AIU uses the standard 5ESS[®]-2000 Fuse/Filter Unit (FFU) to distribute -48 volts.

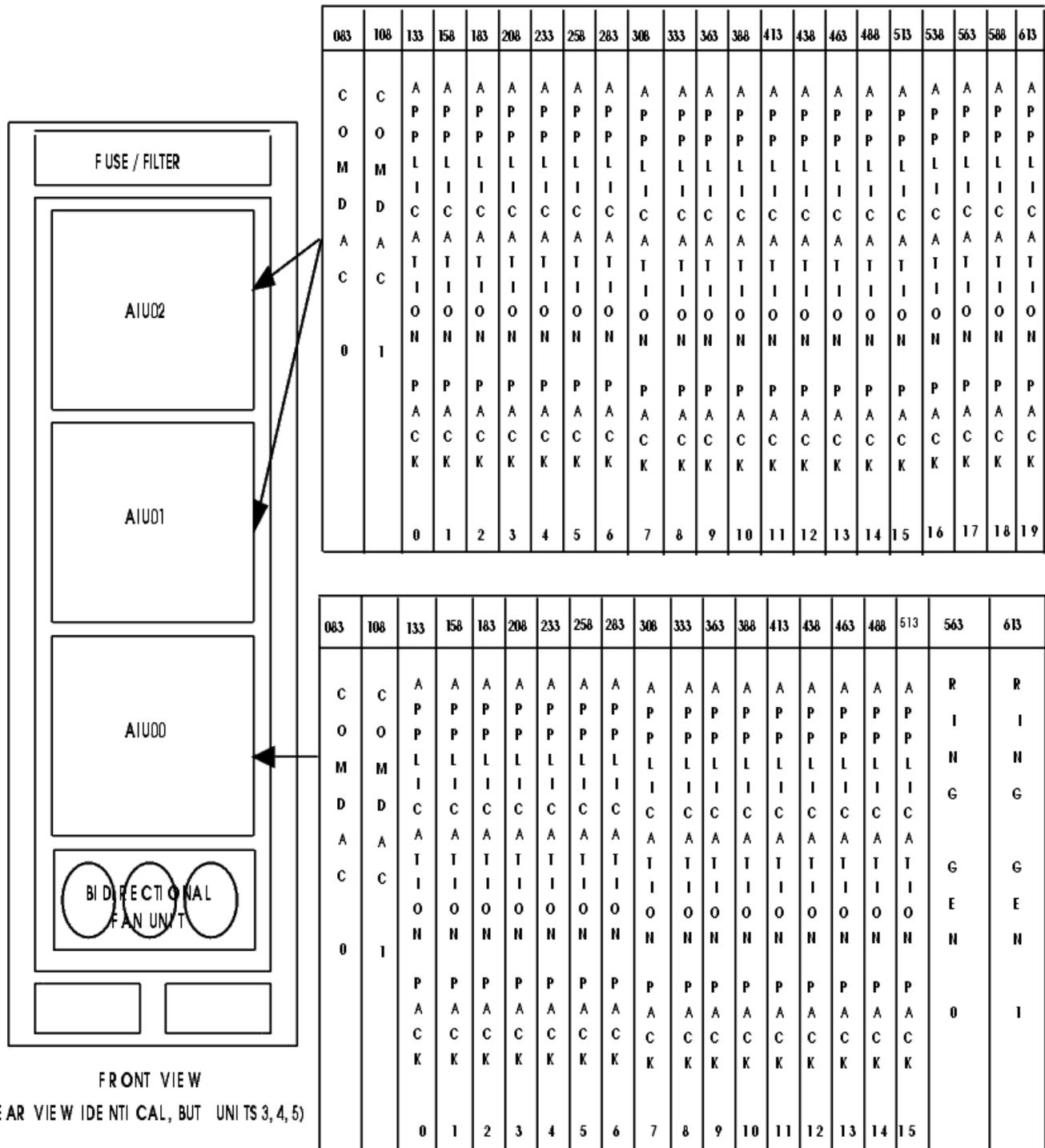


Figure 5.3-33 Access Interface Unit

5.3.20 Asymmetric Digital Subscriber Line (ADSL)

5.3.20.1 Basic Description

Asymmetric Digital Subscriber Line (ADSL) provides combined broadband data and narrowband telephony service for subscribers on the 5ESS-2000 switch by using the ANSI standard T1.413 ADSL Specification. This technique puts the broadband data on the same subscriber loop through the use of Discrete MultiTone (DMT) modulation at frequencies above 4 KHz. Splitters at both ends of the loop separate the narrowband and broadband signals. The broadband data is carried in the form of ATM cells on Permanent Virtual Circuits (PVCs).

5.3.20.2 Configuration

The AIU cabinet has space for six shelves, three in the front and three in the back. The configuration chosen for ADSL has two OEM ADSL shelves and one Lucent POTS shelf in the front of the cabinet, and three OEM ADSL shelves in the back. The ADSL shelf has 18 slots for line cards, but only 16 are used. Two slots are left empty. The OEM shelf provides terminations for alarms (6 outputs and 2 inputs), but these are not used. All alarm information is transported through the Element Manager.

The top shelf is identical to the middle shelf with respect to the circuit pack configurations. It should be noted that the ADSL unit is dedicated to the ADSL application described. This means that it can not be converted to a full AIU (non-ADSL) application by only changing out the AP types. The tip/ring cabling to the MDF is different between the types of units and is not easily interchangeable. A cabling harness, connected between the MDF cable and circuit packs is also required in the ADSL application.

5.3.21 EXPANSION ACCESS INTERFACE UNIT — (EAIU)

5.3.21.1 General

The Expansion Access Interface Unit (EAIU) is similar to the AIU except it can be co-located with the Host SM/SM-2000, ORM/EXM2000 or it can be remotely located by itself. The distance between the EAIU and the SM-2000 can be up to 300 miles. The actual distance will vary depending on the transmission equipment used for remoting.

5.3.21.2 Detailed Description

The Expanded Access Interface Unit (EAIU) has the same major components as the AIU, except it uses a Remote COMMon Data and Control (RCOMDAC DAC624) pack.

The EAIU performs its function by multiplexing the DS1 signals from the RCOMDAC pair into the STS1 (Synchronous Transport Signal Level 1) signal. Testing capabilities are provided through connection to Metallic Test Bus.

5.3.21.2.1 Components for EAIU

RCOMDAC EAIU — The RCOMDAC provides DS1 signal over the T1 facilities that is multiplexed into a STS-1 signal. Each RCOMDAC can have up to 6 T1 facilities (12 T1s per EAIU). The STS-1 from the T1 facility is terminated to a DNU-S [Digital Network Unit-Sonet (Synchronous Optical Network)] associated with the SM-2000.

Subscriber Lines — The APs provide the interface for analog and ISDN subscriber lines and ringing generators. Any type of AP can be installed in any AP slot to provide a flexible mixture of analog and ISDN lines, if necessary. This arrangement also makes it easy for subscribers to migrate from an analog to an ISDN line. Each type of Application Pack will provide a self ID feature that will contain the pack code and serial number.

The types of APs used in the AIU or the EAIU area:

- LPZ100: Provides Plain Old Telephone Service (POTS) Z interface for up to 32 analog subscriber lines.

- LPC100: Provides Coin Phone or POTS interface for up to 16 analog subscriber lines.
- LPU116: Provides ISDN ANSI U interface for up to 16 digital Subscriber lines.
- RGP100: Provides ringing generation for analog subscriber lines. Two packs service up to three AIUs.
- TAP100: Provides integrated metallic testing (that is, SLIM functionality) at remote sites (EAIU) more than 3000 ohms from the Modular Metallic Service Unit (MMSU).

5.3.21.3 Functional Description

The Access Interface Unit (AIU) and Expansion Access Interface Unit (EAIU) consists of two types of Circuit Packs:

- Common Data and Control (COMDAC) — provides common control functions and the interface to the switch.
- Application Packs — provide the interface to the subscriber lines. The interface to the subscriber lines can be provided by using the appropriate application pack. The Application packs differ for digital, analog, or coin.

The COMDAC and various combinations of Application Packs are combined to provide local customers interface to the 5ESS-2000 switch switching module for analog and 2-wire ISDN lines. The AIU terminates up to 640 analog lines or 320 two-wire ISDN lines. It concentrates these lines based on the customer traffic load, the method of engineering, and the engineered blocking factors that have been applied.

In addition to terminating lines and providing line concentration, the unit performs origination scanning, BORSCHT functions (battery feed, overvoltage protection, ringing, supervisory functions, Analog/digital [CODEC] conversion, 2-wire to 4-wire conversion [hybrid], test access), and accepts voice and data connections simultaneously over the same telephone lines.

Each of the line packs provide a time switch allowing any line circuit to be connected to any time slot on the Application Pack-COMDAC to connect the data bus to on a per time slot basis.

5.3.21.3.1 RCOMDAC Circuit

The RCOMDAC (DAC624) circuit provides a Digital Signal Level 1 (DS1) between the AIU and the switch. Each RCOMDAC circuit provides up to six duplicated DS1 signals, therefore a RCOMDAC pair (DAC624 0 and 1) will provide up to 12 DS1 signals per EAIU. The DS1 signals are multiplexed into a STS-1 signal. Up to 28 DS1 signals can be multiplexed into a STS-1 signal. The STS-1 signal is terminated on a Digital network Unit —Sonet (DNU-S). The DNU-S provides a Peripheral Control and Timing link interface to SM-2000 Module Controller/Time Slot Interchanger (MCTSI). The EAIU control channel is bundled with 23 other data channels to make up the 24 channel DS1-0 signal. The PCT link delivers the DS1 signal to the TSI link and the TSI. At the TSI, the control channel is routed to the Message Handler 1 (MH-1) where the control information is formatted into a pseudo-PICB and routed to the Switching Module Processor (SMP).

5.3.21.3.2 Application Packs

The line Application Packs are common to the AIU and the EAIU.

The following functionality is common to all application packs providing line terminations.

The data interface format for application packs consists of 32 time slots of 16 bits each. The interface between the Application Packs and the COMDAC consist of the following signals:

- PCM Clock

- PCM Synchronization
- PCM Data (AP up/down to COMDAC)
- AP Control (AP up/down to COMDAC)
- AP Select
- AP Reset

The SM selects the time slot to be used and then sets up the COMDAC and the Application Packs. The COMDAC concentrator connects a given time slot from any Application Pack to the same time slot on any of the Time Slot Groups (TSGRPs). The Application Packs can connect any incoming line to any of the 32 time slots.

Application Packs have one red LED located on the faceplate. This red LED is used as a diagnostic tool to announce various conditions of Self-Test. Such a Reset, Power-Up, and Software Control. A constant Lit LED (no flashing) means a fault condition exists with the pack.

5.3.21.4 Configuration

The Access Interface Unit (AIU) is a simplex unit made up of two service groups. Each service group has a Common Data and Control (COMDAC) pack.

The AIU is engineered for a line concentration ratio of anywhere from 2:1 to 10:1.

The COMDAC packs operate in ACTIVE/ACTIVE mode to share the call load.

The even numbered application packs are assigned to COMDAC 0 and the odd numbered application packs are assigned to COMDAC 1. However, each application pack has access to both COMDACs should one COMDAC become overloaded or go out of service.

Should one COMDAC go out of service, the line concentration ratio would double.

5.3.21.5 Shelf and Pack Layout

AIU's/EAIU are housed in a dedicated Line Trunk Peripheral (LTP) cabinet. No other units are installed in a cabinet housing AIU's/EAIU's. AIU's/EAIU's are installed in standard building blocks of two or three AIU's/EAIU's mounted one above the other. One AIU/EAIU building block fits into a Standard LTP Cabinet. Two AIU/EAIU blocks fit into a Front Access Cabling (FAC) Cabinet, one facing the equipment aisle and one facing the wiring aisle.

5.3.22 MEMORY EXPANSION UNIT - J5D003BH-1

The Memory Expansion Unit (MEU) is a single-shelf unit which MUST be mounted in the Switching Module Control (SMC) cabinet, shelf 1. The unit is divided into two Module Controller Time Slot Interchange (MCTSI) controllers, 0 and 1, with 0 to the left and 1 to the right.

The main function of the MEU is to expand the memory area of the MCTU. Addition of the MEU increases the maximum MCTU memory capacity from 10 to 16 MB. Since the SMP12 or SMP23 units can be equipped with either 2MB (TN56) or 4MB (TN2012) memory boards, the MEU increases the maximum MCTU memory capacity to 24MB (12 * 2MB)(TN56s) or 32MB (12 * 4MB - but limited to a maximum addressability of 32MB (TN2012).

The type and number of memory circuit packs (TN56 or TN2012) depends on the processor in the MCTU. The memory packs in the MEU must be the same as the memory boards in the MCTU. The MEU is only valid on MCTU's which supports SMP12 or SMP23 Module Processors. The MEU is not supported on MCTU's with SMP23CDM Module Processors.

Figure 5.3-34 illustrates the location of the Memory Expansion Unit in the Switching Module Control Cabinet and the respective Circuit Packs in the unit.

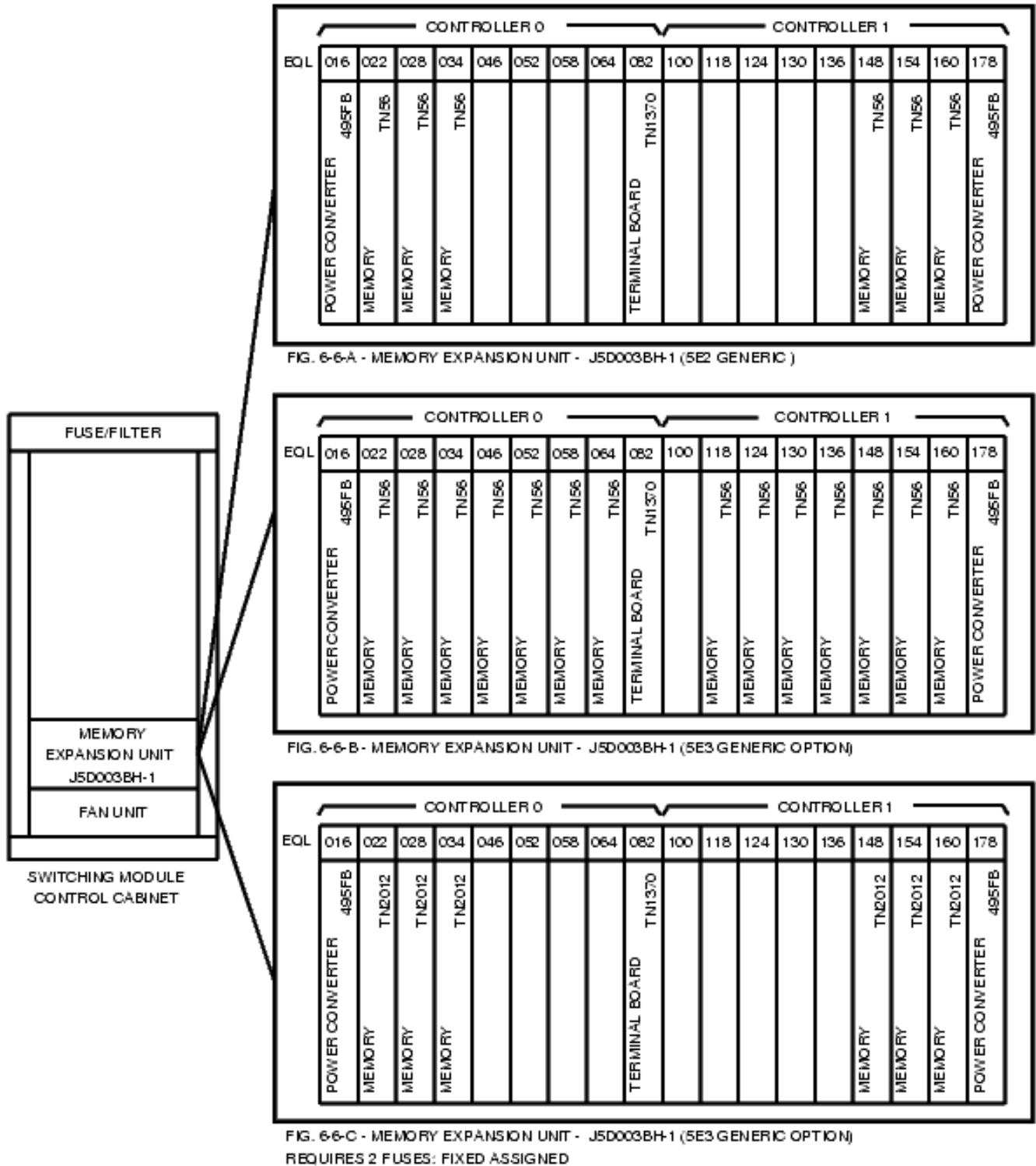


Figure 5.3-34 Memory Expansion Unit - J5D003BH-1

5.3.23 SMP23 WITH CORE DRAM

The SMP23CDM core board (TN1423) can be used in SMP23 or SMP12 units to replace the TN1407(B) or TN1397 microprocessor core boards, respectively. The TN1423 provides 32MB of DRAM on the microprocessor core board, which removes the need of using an MEU shelf and extra memory boards to reach maximum equipment. The SMP23CDM is introduced as part of the 5E10 software release. Although the SMP23CDM core board is capable of addressing up to 128MB, the bootstrapper board and the size of the update bus currently limit duplex operation of the MCTSI to 32MB.

The SMP23CDMX is an extension of the SMP23CDM processor. The conversion of a SMP23CDM to a SMP23CDMX involves adding an Update Bus Cable, a new bootstrapper board, the code to support it, and possibly changing the Memory Controller boards. The SMP23CDMX is introduced as part of the 5E12(1) software release and as a software update in 5E10(1) and 5E11(1). The SMP23CDMX supports 32MB of DRAM on the microprocessor core board and up to 5 4MB (TN2012) on the MCTU shelf. This means that the maximum memory equipment of a SMP23CDMX is 52MB (32MB DRAM + (5 * 4MB)). Table 5.3-7 shows the configuration of the component boards.

Table 5.3-7 SMP23 Components

FUNCTION	SMP23CDM	SMP23CDMX
Micro processor core board	TN1423(B)	TN1423(B)
Communications boards	TN1617/TN872	TN1617/TN872
Processor core support board	TN1533	TN1533
RAM/ROM board	TN874B	TN874B
Bootstrapper board ^a	TN878	TN1418
Memory controller board	TN1408(B)/TN1527	TN1408(B)
Non-Core Board Memory Board	NONE	TN2012
Notes:		
a. The TN878 can only be used for applications requiring 32 Mbyte or less of memory.		

5.3.24 MODULE CONTROLLER TIME SLOT INTERCHANGER UNITS

5.3.24.1 Module Controller Time Slot Interchanger - J5D003EC-1

The Module Controller Time Slot Interchanger Unit (MCTU) is a two-shelf unit fixed located on shelf 2 and 3 of the Switching Module Control cabinet. It is divided into two sections with controller 0 at the left and controller 1 at the right. The controllers operate in an active/standby mode with circuit packs duplicated in the two controllers. All circuit packs in Module Controller 0 are duplicated in Module Controller 1 except the bootstrapper pack (TN878 or TN1418).

The MCTU does the following:

- Provides interfaces with Network Control and Timing (NCT) links.
- Provides an interface with the intra-switching module to transmit control information from the Switching Module Processor.
- Provides an interface with the intra-switching module for pulse-code modulation (PCM) data.
- Provides call processing, call supervision and maintenance functions.
- Provides Switching Module Processor controlled time-division switching.
- Provides an interface between the Switching Module Processor and the Network Control Timing links message time slots.
- Preprocesses signaling and control bits of time-slot data and provides Switching Module Processor access to

the bits.

The TN874B Module Processor pack is software-release sensitive.

Figure 5.3-35 illustrates the location of the Module Controller Time Slot Interchanger Unit and the respective circuit packs in the unit.

MODULE CONTROLLER 1		
180	POWER CONVERTER	410AA
172	CONTROL AND DISPLAY	SN516
162	CONTROL INTERFACE 1	UN71B
	CONTROL INTERFACE 0	UN71B
148	DATA INTERFACE 1	TN876
140	DATA INTERFACE 0	TN876
122	TIME SLOT INTERCHANGER SIGNAL PROCESSOR	TN1086B
114		
098	DUAL LINK INTERFACE 1	TN1077C
084	DUAL LINK INTERFACE 0	TN1077C
070		
MODULE CONTROLLER 0		
062	TIME SLOT INTERCHANGER SIGNAL PROCESSOR	TN1086B
048	DATA INTERFACE 0	TN876
040	DATA INTERFACE 1	TN876
030	CONTROL INTERFACE 0	UN71B
022	CONTROL INTERFACE 1	UN71B
016	CONTROL AND DISPLAY	SN516
008	POWER CONVERTER	410AA

MODULE CONTROLLER 1		
178	POWER CONVERTER	410AA
162	MEMORY TN56	TN2012
156	MEMORY TN56	TN2012
150	MEMORY TN56	TN2012
144	MEMORY TN56	TN2012
138	MEMORY TN56	TN2012
132	MODULE PROCESSOR	TN875C TN1527
126	MODULE PROCESSOR	TN874B
120	MODULE PROCESSOR	TN872
114	MODULE PROCESSOR	TN873 TN1533
108	MODULE PROCESSOR	TN871B TN1397
100	BOOTSTRAPPER	TN878
090		
082		
076	MODULE PROCESSOR	TN871B TN1397
070	MODULE PROCESSOR	TN873 TN1533
064	MODULE PROCESSOR	TN872
058	MODULE PROCESSOR	TN874B
052	MODULE PROCESSOR	TN875C TN1527
046	MEMORY TN56	TN2012
040	MEMORY TN56	TN2012
034	MEMORY TN56	TN2012
028	MEMORY TN56	TN2012
022	MEMORY TN56	TN2012
MODULE CONTROLLER 0		
016	POWER CONVERTER	410AA

FUSING - REFER TO ED5D661 AND OFFICE RECORDS FOR SPECIFIC FUSE ASSIGNMENTS

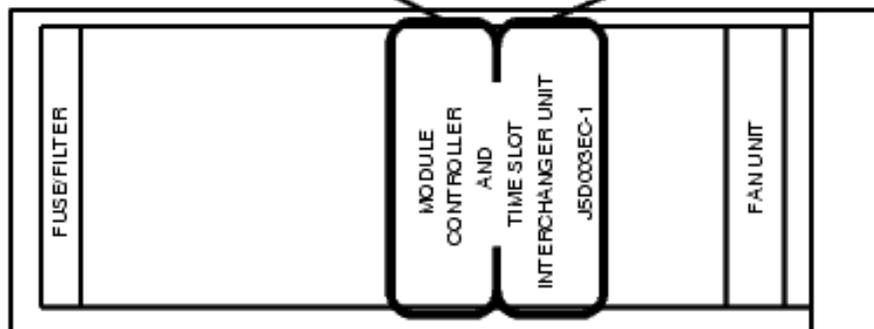


Figure 5.3-35 Module Controller Time Slot Interchanger - J5D003EC-1**5.3.24.2 Module Controller Time Slot Interchanger - Model 2 - J5D003LA-1**

The Module Controller Time Slot Interchanger Model 2 (MCTU2) is a two-shelf unit fixed located on shelves 1 and 2 of the Switching Module Control cabinet. It is divided into two sections with controller 0 at the bottom and controller 1 at the top. The controllers operate in an active/standby mode with circuit packs duplicated in the two controllers. All circuit packs in Module Controller 0 are duplicated in Module Controller 1.

The TN833 circuit pack located at EQL 168 handles the Local Digital Service Unit functions. This eliminates a need for 003EAI DSU2 serving local functions for a DSU2 shelf.

The MCTU2 does the following:

- Interfaces with Network Control and Timing Links.
- Sends/receives control orders from the peripheral units in the SM, using the PICB bus information from the Switching Module Processor.
- Sends/receives pulse-code modulation data from the peripheral unit in the SM, using the PICB bus.
- Preprocesses signaling and control bits of time-slot data and provides Switching Module Processor access to the bits. Memory unit assignments are sensitive toward software releases.
- Provides interface with the PSU.

Figure 5.3-36 illustrates the location of the Module Controller Time Slot Interchanger - Model 2 and the respective circuit packs in the unit.

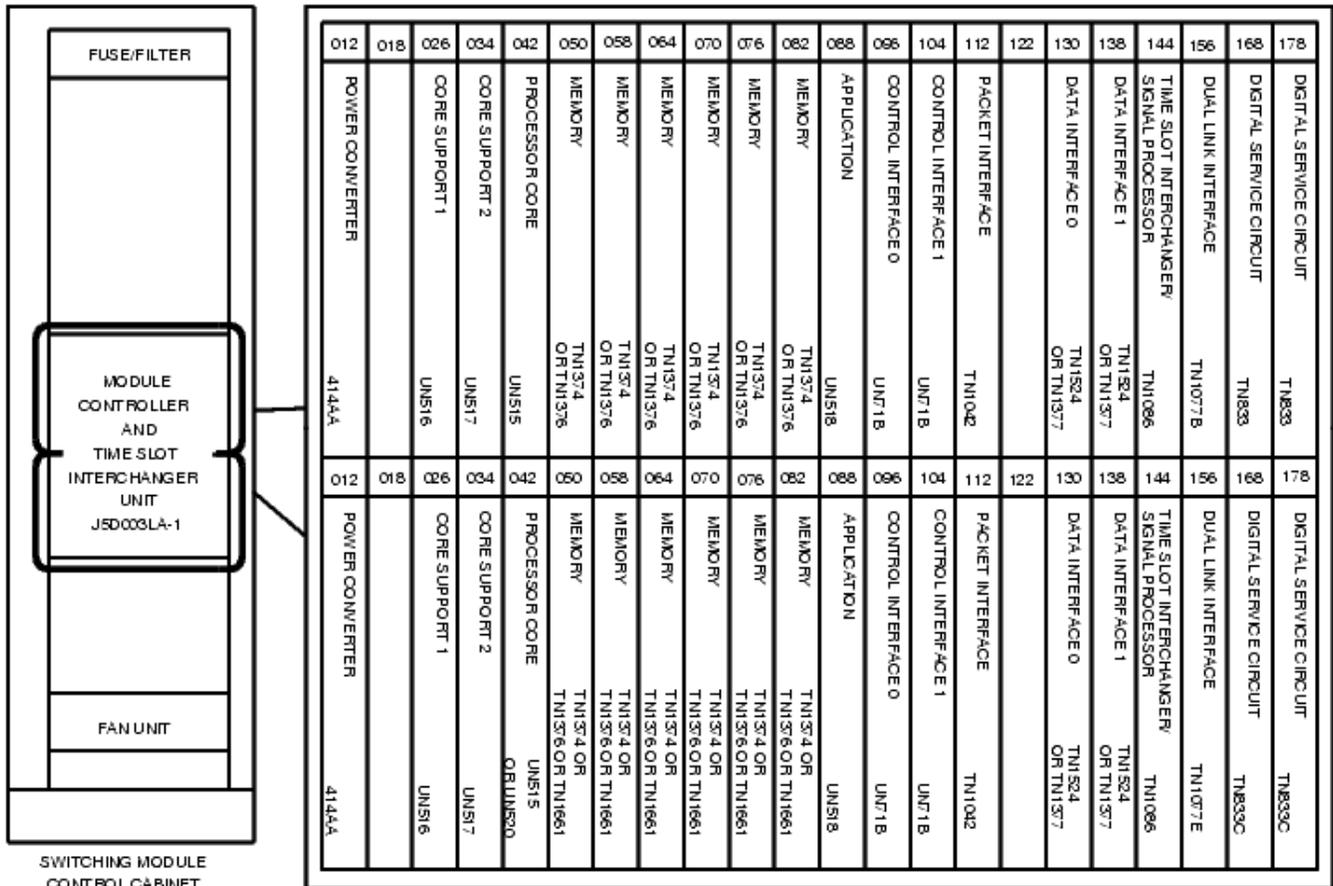


Figure 5.3-36 Module Controller Time Slot Interchanger - Model 2 - J5D003LA-1

5.3.24.3 Module Controller Time Slot Interchanger - Model 3 - J5D003LB-1

The Modular Controller/Time Slot Interchange Unit, Model 3 (MCTU3) combines several circuit packs into one and reduces the MCTU2 from two shelves to one. The MCTU3 will require a new shelf/backplane, a new core board (SB20CORE), and a new combined power control and display pack. The existing TSIU3 together with the DIs, CIs or the new CI2s and peripherals will be used. All SM configurations including Local Switching Module (LSM), RSM, ORM for 5ESS®-2000 switch and 5ESS®-2000 switch CDX will be supported. The MCTU3 feature is particularly beneficial to the 5ESS®-2000 VCDX because the SB20CORE board contains most of the hardware to support the Ethernet® interface. A paddle board located on the backplane of the MCTU3 will provide the physical interface to the Ethernet® interface and handles the CPI message interface between the workstation and the SB20CORE.

The functionality of the MCTU3 is identical to MCTU2 with customer benefits listed below:

- The MCTU3 provides a more than 10% increase in SM Processor capacity without the need of a Data Cache (UN520 as required by MCTU2).
- MCTU3 consumes 50% less power than MCTU2.
- MCTU3's predicted reliability is 35% better than MCTU2.
- The reduction in circuit pack codes means that fewer codes need to be spared.
- MCTU3 fits in one shelf, MCTU2 requires two shelves.

Figure 5.3-37 illustrates the location of the Module Controller Time Slot Interchanger - Model 3.

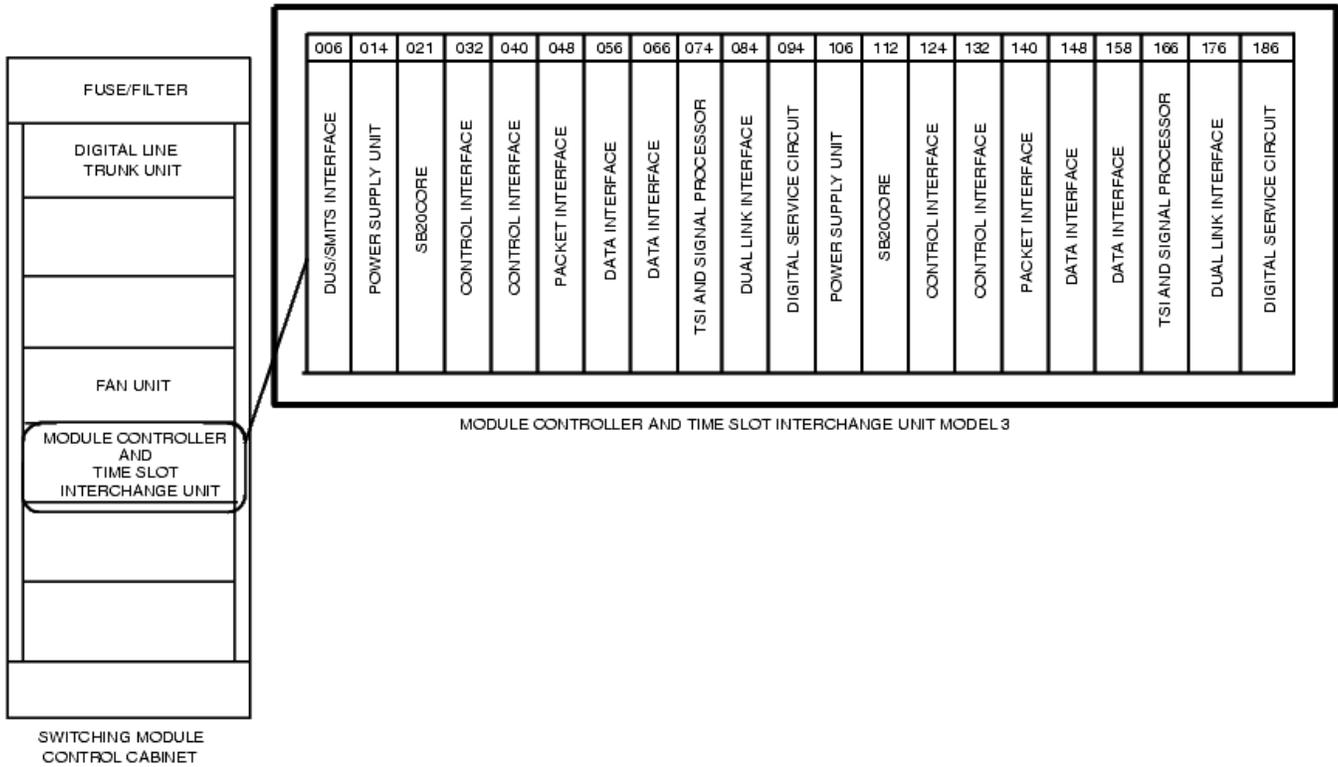


Figure 5.3-37 Module Controller Time Slot Interchanger -Model 3 - J5D003LB-1

5.3.25 MODULAR METALLIC SERVICE UNIT - J5D003BD-1

The Modular Metallic Service Unit (MMSU) is a one- to four-shelf unit that can be located in shelf positions 1 through 6 in a Line Trunk Peripheral (LTP) cabinet. Put the basic MMSU in shelf space 1 to 3, with supplemental units (up to 03) mounted above in ascending order. The MMSU may also be mounted in any available vacant location in the Switching Module Control cabinets.

Each unit is divided into two duplicate Service Groups, SG0 and SG1. Each shelf requires two power units (494LA) at locations 010 and 098, respectively. Only the basic shelf requires common packs TN879B at positions 018 and 106.

Each service group can mount up to 32 service packs (Service Group 0 - EQL 026 to 081 and Service Group 1 - EQL 114 to 170). The type of pack in each position varies from office to office.

One of the main functions of the MSSU is to establish a metallic test path through the office, thereby connecting lines or trunks to test positions and designated test equipment.

When a TN138 pack is mounted in Service Group 0 (at 026, 034 and 042) and Service Group 1 (at 114, 122 and 130), an additional TN138 pack is required at 090 and 178. When there are no TN138 packs in a service group, position 090 contains a ground shield.

Circuit packs assigned to Automatic Line Insulation Tests are selected to accommodate local area humidity conditions. The packs available are TN328B, TN329B and TN330B. The packs are located at EQL 050 and 138.

For software release 5E10 and later, a SLIM(2) board (TN1422) is an optional board to insert in the MMSU. The

SLIM(2) is designed to do measurements on analog and digital subscriber lines as well as analog trunks. It will measure the metallic characteristics of the line/trunk such as voltages, insulation resistances, and capacitances. SLIM(2) can be operated in both Operator Mode (TLWS 5700 page, similar to the DCTU page) and Routine Mode (recent change driven, similar to the ALIT).

Figure 5.3-38 illustrates an example location of the SLIM(2) board in the Modular Metallic Service Unit area of the Line Trunk Peripheral Cabinet, and location of the respective circuit packs in the unit. The MMSUs and associated growth units are engineered to specific office requirements, therefore, the configurations are typical and nonrestrictive.

SERVICE GROUP 1				SERVICE GROUP 1			
178	METALLIC ACCESS	MTIB ONLY	TN138	178	METALLIC ACCESS	MTIB ONLY	TN138
170				170	DISTRIBUTING FRAME TEST ACCESS CIRCUIT		TN1040
162				162	SIGNAL DISTRIBUTOR		TN221
154				154	SCAN		TN220B
146				146	GATED DIODE CROSSPOINT COMPENSATOR		TN880
138				138	AUTOMATIC LINE INSULATION TEST		
130	METALLIC ACCESS 10		TN438	130	METALLIC ACCESS 2		TN438
122	METALLIC ACCESS 9		TN438	122	METALLIC ACCESS 1		TN438
114	METALLIC ACCESS 8		TN438	114	METALLIC ACCESS 0		TN438
106				106	COMMON		TN879B
098				098	POWER UNIT		494LA
090	METALLIC ACCESS	MTIB ONLY	TN138	090	METALLIC ACCESS	MTIB ONLY	TN138
082				082	DISTRIBUTING FRAME TEST ACCESS CIRCUIT		TN1040
074				074	SIGNAL DISTRIBUTOR		TN221
066				066	SCAN		TN220B
058				058	GATED DIODE CROSSPOINT COMPENSATOR		TN880
050	SLIM2		TN1422	050	AUTOMATIC LINE INSULATION TEST		
042	METALLIC ACCESS 10		TN438	042	METALLIC ACCESS 2		TN138
034	METALLIC ACCESS 9		TN438	034	METALLIC ACCESS 1		TN138
026	METALLIC ACCESS 8		TN438	026	METALLIC ACCESS 0		TN138
018				018	COMMON		TN879B
010	POWER UNIT		494LA	010	POWER UNIT		494LA
E O L				E O L			
MMSU 01 (GROWTH UNIT)				MMSU 00 (BASIC UNIT)			

FUSES: TWO PER SERVICE GROUP. FOR SPECIFIC LOCATION ASSIGNMENTS, REFER TO EDS0651-15 AND OFFICE RECORDS.

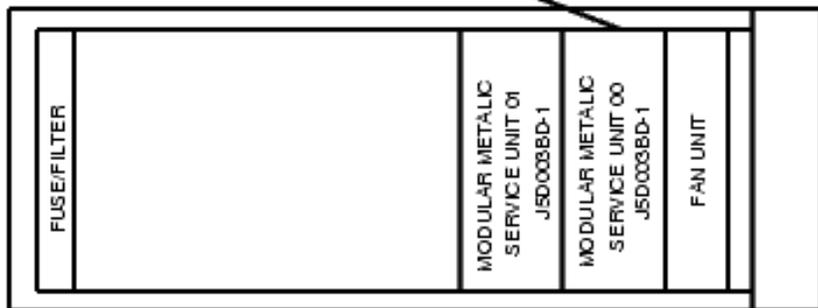


Figure 5.3-38 Modular Metallic Service Unit - J5D003BD-1

5.3.26 PACKET SWITCH UNIT - J5D003BL-1

The Packet Switch Unit (PSU) is made of one to five shelf units mounted in any Line Trunk Peripheral (LTP) cabinet. The PSUs can also be mounted in Switching Module Control (SMC) cabinets, but only in shelves 3 and 4 when the space is available.

The primary function of the PSU is to provide processing to support packet signal messages, Operator Services Position System (OSPS) operator data messages and packet data switching.

The basic PSU (00) is always required in an SM containing an Integrated Service Line Unit (ISLU) that services digital subscribers. The basic PSU is also required for SMs that mount a Digital Line Trunk Unit (DLTU) connected to T1 lines that handle Integrated Services Data Network (ISDN) traffic (primary rate users).

The assignment of Protocol Handler circuit packs (up to 16) is software-release sensitive. The Protocol Handler communicates over the packet bus to the SMP and to other protocol handlers and provides a local environment to support distributed processing.

The basic PSU always mounts in vertical location 19 in an LTP cabinet and can support four additional growth units. The growth units are mounted above the basic unit in ascending numerical order from 01 through 04. The number of PSU shelves for an office is determined by the number of digital subscribers present. Only one PSU can mount in an SM.

Figure 5.3-39 illustrates the location of the Packet Switch.

Table 5.3-8 identifies the respective circuit packs in it.

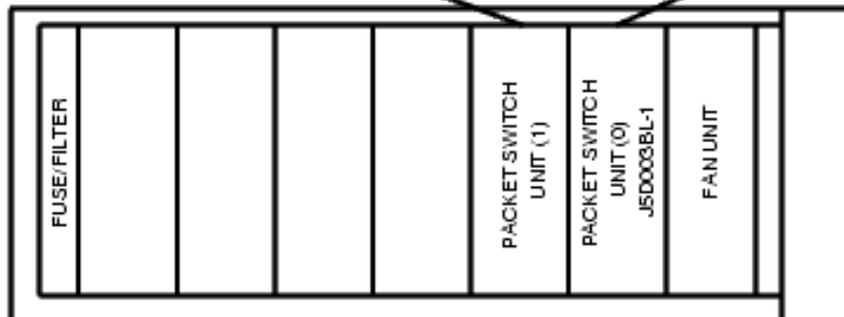
NOTE: In the 5E10 software release, if the SM requires a PSU, either a PSU or PSU2 can be used. In the 5E10 software release, if the SM-2000 requires a PSU, only a PSU2 can be used. A single Packet Switch Unit Model 2 (PSU2) unit can physically support up to a combination of 80 Protocol Handler 4's (PH4s), Protocol Handlers for Voice (PHVs) and spares. However, time slot engineering may limit specific configurations to less than 80. To support a large community of PH4s and PHVs, a multiple community of PH4s and PHVs, a multiple PSU2 configuration is required. Refer to 235-200-100, *5ESS®-2000 Switch Autoplex 1000 Wireless Applications*, for additional information on the PSU2 units.

178	16TH PROTOCOL HANDLER
170	15TH PROTOCOL HANDLER
162	14TH PROTOCOL HANDLER
154	13TH PROTOCOL HANDLER
146	12TH PROTOCOL HANDLER
138	11TH PROTOCOL HANDLER
130	10TH PROTOCOL HANDLER
122	9TH PROTOCOL HANDLER
114	
106	PACKET FANOUT
098	DATA FANOUT
090	DATA FANOUT
080	PACKET FANOUT
072	
064	8TH PROTOCOL HANDLER
056	7TH PROTOCOL HANDLER
048	6TH PROTOCOL HANDLER
040	5TH PROTOCOL HANDLER
032	4TH PROTOCOL HANDLER
024	3RD PROTOCOL HANDLER
016	2ND PROTOCOL HANDLER
008	1ST PROTOCOL HANDLER (SEE TABLE)

PACKET SWITCH 1 (GROWTH)

178	16TH PROTOCOL HANDLER
170	15TH PROTOCOL HANDLER
162	14TH PROTOCOL HANDLER
154	13TH PROTOCOL HANDLER
146	12TH PROTOCOL HANDLER
138	11TH PROTOCOL HANDLER
130	10TH PROTOCOL HANDLER
122	9TH PROTOCOL HANDLER
114	CONTROL FANOUT
106	PACKET FANOUT
098	DATA FANOUT
090	DATA FANOUT
080	PACKET FANOUT
072	CONTROL FANOUT
064	8TH PROTOCOL HANDLER
056	7TH PROTOCOL HANDLER
048	6TH PROTOCOL HANDLER
040	5TH PROTOCOL HANDLER
032	4TH PROTOCOL HANDLER
024	3RD PROTOCOL HANDLER
016	2ND PROTOCOL HANDLER
008	1ST PROTOCOL HANDLER (SEE TABLE)

PACKET SWITCH UNIT 0 (BASIC)



LINE TRUNK
PERIPHERAL CABINET

Figure 5.3-39 Packet Switch Unit - J5D003BL-1

Table 5.3-8 PACKET SWITCH UNIT— CIRCUIT PACKS

PROTOCOL HANDLER	CIRCUIT PACKS
PSU	TN1366, TN1367, TN1081
PSU2	TN1844, TN1856, TN1862, TN1845, TN1367C, TN1867, TN1846
FANOUT	CIRCUIT PACKS
PSU1	Control Fanout TN1082/MC5D102A1, TN1082B/MC5D102A1B, TN1082B/MC5D123A1B
PSU2	TN1843, UN399, UN348B, UN348/MC5X701A1, UN592

5.3.27 SS7-PSU ON SM/EXM-2000

The introduction of SM-based SS7 (Signaling System 7) signaling on the SM-2000/ EXM-2000 allows basic subscriber features and services that require SS7 signaling to continue intra-module operation in the event that the SM-2000/EXM-2000 loses communication with the host and goes in to stand-alone operation (if provisioned for stand-alone). The SM-based SS7 signaling platform is provided by the addition of an SS7 Packet Switch Unit (PSU) to the switching module. For switching modules like the SM-2000 and EXM-2000, an SS7 PSU can be added and SS7 signaling links terminated to it to provide stand-alone processing if desired.

This feature consists of the following core elements:

- (1) It provides the SM-based SS7 Message Transfer Part (MTP) and Signaling Connection Control Part (SCCP) signaling platform (SS7-PSU) on the SM, RSM ORM (Optically Integrated Remote Switching Module), (local) SM-2000 and EXM-2000 switching modules in the 5ESS[®]-2000 switch.
- (2) It allows both the (AM-based) CNI (Common Network Interface) and (SM-based) SS7-PSU signaling platforms to co-exist in the same host office.

Those switching modules equipped with an SS7 PSU and terminating SS7 signaling links are designated as Global Switching Modules (GSMs). All SS7 signaling on the GSM is handled by its SS7 PSU. In this phase of bringing SM-based signaling to the 5ESS[®]-2000 switch, the SS7 PSU supports only trunk groups terminated on the GSM. In essence, the GSM emulates a single SM office, and up to sixteen GSM are supported per 5ESS[®]-2000 switch.

The SM-based SS7 signaling is necessary for VCDX offices since CNI, AM, and CM do not exist. CNI and SS7 on PSU may co-exist. 5ESS[®]-2000 Switch, employs PH3 to terminate the SS7 signaling links onto the VCDX, and non-VCDX offices. A signaling link arrives as a timeslot either on a 24-channel T1 facility terminating in a Digital Line and Trunk Unit 2 (DLTU2) or on a Digital Networking Unit-Sonet (DNU-S). The SS7 on PSU provides:

- Transaction Capabilities Application Part (TCAP)
- Integrated Services User Part (ISUP)

On the non-VCDX offices, if a Switching Module is equipped as a Global SM (GSM), an ISUP trunk group or TCAP service can be provisioned by the customer to use either Common Network Interface (CNI) or an SS7 PSU for message transport. This will provide a means for the service provider to transition signaling from CNI to the SS7 PSU for normal and standalone operation over time rather than being flash cut.

5.3.28 INTEGRATED DIGITAL CARRIER UNIT

5.3.28.1 Integrated Digital Carrier Unit - J5D003FL-1

The Integrated Digital Carrier Unit (IDCU) is an interface on the SM that provides integrated access to digital loop

carrier (DLC) systems. In addition to terminating TR-008 systems (POTS and other switched services), the IDCU supports TR-303 integrated DLC (IDLC) systems (POTS, switched and ISDN), as well as PUB 43801 (non-switched and non-locally switched services) interfaces. The initial offering of this hardware provides the first phase of a TR-303 implementation.

The IDCU provides an open interface as described in Bellcore TR-TSY-000303 to support concentrated Integrated Services Digital Network (ISDN). This feature supports the following Remote Terminals (RTs):

- **SLC[®] 96 Carrier System Remote Terminals**
 - Mode I
 - Mode II.
- **SLC[®] Series 5 Carrier System Remote Terminals**
 - Feature Package 303G (FP303G): TR-008 Mode I, TR-008 Mode II or TR-303 interface (with concentrated ISDN)
 - Feature Package B (FPB)
 - Enhanced Feature Package B (FPB+) Mode I
 - Enhanced Feature Package B (FPB+) Mode II.
- **Large Remote Digital Terminals**
 - TR-008 Mode
 - TR-303 Mode.
 - TR-008 Compatible RTs
- **TR-303 Compliant RTs.**

IDCU TR-303 Industry Standard 96 Line RDT Interface was the 5ESS[®]-2000 switch's first Product Release of the TR-303 Industry Standard 96 Line RT Interface. It implements the IDCU with the SLC[®] Series 5 carrier system remote terminal equipped with FP303. The 5ESS[®]-2000 switch's implementation of TR-303 is described in 235-900-308, *Integrated Digital Carrier Unit TR-TSY-000303 Interface Specification*. The TR-303 options implemented with the IDCU are identified and the implementation details needed to build the interface (matched to Bellcore's Revision 4 of TR-303), are included in this document.

If an IDCU interfaces with TR-303 RDTs, the IDCU requires a PSU(2). If an IDCU only interfaces with TR-08 RDTs, a PSU(2) is not required. See section 5.3.20 for more information on PSU(2).

The IDCU TR-303 Large RDT interface can support up to 2048 lines. This is significantly larger than the small RDT interface which supports up to 96 lines. Additionally, the Large RDT interface can support up to 28 DS1 interfaces compared with the 5 DS1 interfaces supported in the small RDT interface. The 5E10 software release supports both the small and large TR-008 and TR-303 interface.

The Integrated Digital Carrier Unit (IDCU) is a single-shelf peripheral unit. The IDCU shelf is divided into two service groups (SGs) [that is, SG 0 and SG 1] that operate in an "active/standby" configuration. Figure 5.3-40 shows the IDCU shelf layout. The IDCU contains four or five duplicated circuit packs (that is, power control/display and power

converter (PCDC), common control processor (CCP), PIDB transmission interface (PTI) and loopside interface (LSI0, LSI1). The IDCU also contains one or two common packs, electrical line interface (ELI0 and ELI1). The LSI1 and ELI1 are optional.

The IDCU connects within the SM via peripheral interface control bus (PICB), peripheral interface data bus (PIDB) and directly connected interface data bus (DPIDB). The DS1 cables connect to it from the DSX bay. The SM-2000 supports up to 34 IDCU peripheral units with unit numbers from 0 to 42. This maximum number can only be reached if other peripherals are not also maximally installed.

The IDCU diagnostics are divided into the following phases:

- Phases 1 through 4, 7, 8, and 10 are CCP test.
- Phases 5, 6, and 9 are PTI tests.
- Phases 21 through 27 are LSI/DLP tests.
- Phases 28 through 30 are demand phases used during factory and installation testing.

5.3.28.2 PIDB Transmission Interface

The PIDB Transmission Interface (PTI) contains a time slot interface that can connect any DS1 time slot to any time slot on the PIDBs, to the SM TSIU, or on the DPIDBs to the PSU. The PTI provides a signal processing function which monitors incoming signaling to detect originations and transmits idle signaling.

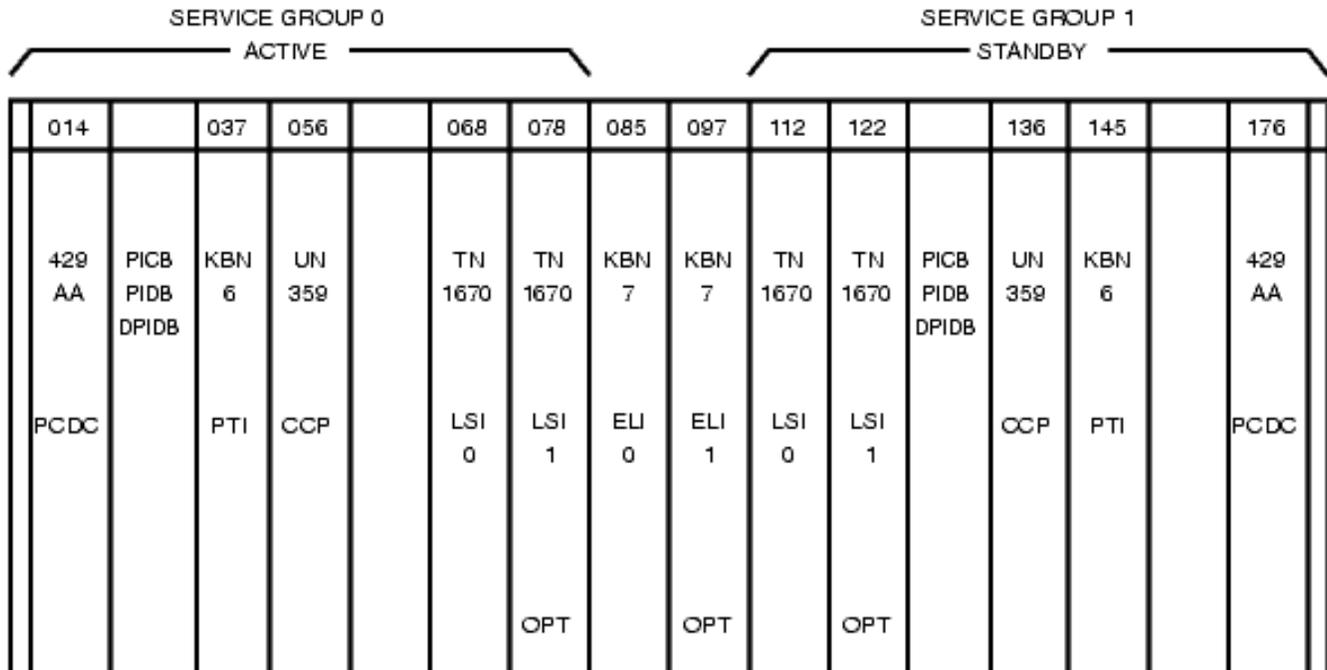
5.3.28.3 Loopside Interface

Each Loopside Interface (LSI) terminates 20 DS1s. Two fully duplicated LSIs are required to equip an IDCU. The LSI frames on each of the DS1s convert it to a PIDB-like format on the internal bus to the PTI. It also collects DS1 performance-monitoring data and detects DS1 failures and alarms.

5.3.28.4 Electrical Line Interface

The Electrical Line Interface (ELI) splits the received DS1 signals to active/standby LSIs and combines the transmitted DS1 signals; each ELI can handle 20 DS1s. The units are not duplicated because they contain only passive components and a single fault can affect only one DS1.

See Table 5.3-9 for detailed information on diagnostic phases for IDCU.



NOTE: Optional LSI1 and ELI1 circuit packs are equipped if more than 20 IDCU facilities are required. An IDCU facility number greater than 19 is assigned. IDCU PIDB ports 9 and up are assigned.

Figure 5.3-40 IDCU Shelf Layout - J5D003FL-1

Table 5.3-9 Switching Module Diagnostic Phase Descriptions

DIAGNOSTIC ID	PHASE	DESCRIPTION/ WHAT IS TESTED	PR NAME
ACCESS INTERFACE UNIT (AIU)	1	Tests the control/data integrity to each equipped and ACT AP. If an AP is OOS, the tests for that AP are skipped. This phase also runs the COMDAC resident diagnostics.	
	2	Verifies the control data flow between the RG(AP) and both COMDACs and runs the RG firmware diagnostics.	
	3	Verifies the RG's isolation relay, programmability, and the ringing bus connections to each AIU it is assigned. At least one in-service COMDAC is required for this phase or the phase completion status is NTR (no tests run).	
	4	Verifies the control data flow between the AP and both COMDACs and runs the AP resident diagnostics.	
	5	Verifies the PCM data paths between the AP and both COMDACs.	
	6	Verifies the AP metallic test buses and associated relays including the paths	

		(GPB0/1) from the COMDAC to the AP. Note: The AP metallic bus structure is likely to vary between specific AP types.	
	7	Run for Z-POTS circuit packs only. Verifies the AP's connection to the RG buses. Also verifies that the AP can be isolated from the RG buses.	
	8	Verifies the LC functionality by requesting the AP firmware to run tests on the circuits, including PCM path tests between the LC and the controlling COMDAC.	
AUTOMATIC LINE INSULATION TESTING (ALIT)	1	Tests receive control orders from the MSUCOM sanity test and calibration test.	SM:DNALIT
APPLICATION (Z-INTERFACE) (AP)	1	Verifies the control data flow between the AP and both COMDACs (Common Data and Control Controllers) and runs the AP resident diagnostics.	
	2	Verifies the PCM data paths between the AP and both COMDACs.	
	3	Verifies the AP metallic test buses and associated relays including the paths (GPB0/1) from the COMDAC to the AP. NOTE: The AP metallic bus structure is likely to vary between specific AP types.	
	4	Run for Z-POTS circuit packs only. Verifies the AP's connection to the RG (ring generator) buses. Also verifies that the AP can be isolated from the RG buses.	
BOOT-STRAPPER (BTSR)	1	Tests access to the BTSR board, verification of registers, and executes internal self-diagnostic of the BTSR.	SM:DNBTSR
	2	Functional test of the BTSR (attempts to pump to mate MCTS's memory).	SM:DNBTSR
COMMON CONTROL (CC) (DNU-S)	1	Performs PCT loopback at PCTLI and serial PCAMB loopback at CC. PCT loopback is performed using the PCT loopword time slot. The PCT link loopword time slot is looped back at PCTLI. The PCAMB	SM2K:DNUSCC1
	2	Tests the HIFI device's processor-side interface, loopback, internals, and interrupts.	SM2K:DNUSCC1
	4	Verifies operation of the DNU-S CCP processor that includes timers, sanity timer, interrupt priority encoder, and the NMIs. It also tests EPROM, I/O write protection, memory write-protection circuits, and address and data parity generators and checkers.	SM2K:DNUSCC1
	5	Tests the operation of the two control	SM2K:DNUSCC1

	7	interface (CI) devices on the CC pack. Tests the mate bus, ICB interface and mate hashsum. If there is no active CC, this phase falls into NTR. The mat bus is tested from the active CC towards the CC under test. The CC under test is initialized into DGN mode before the active CC tests it.	SM2K:DNUSCC1
	8	Tests the mate access circuit from the CC under test to the active CC. It verifies that the CC under test can detect mate errors by putting the OOS CC in hold and forcing the mate errors.	SM2K:DNUSCC1
	9	Requests the DNU-S' CC to run on a ROM-based memory test for the CC memory.	SM2K:DNUSCC1
COMMON DATA (CD) (DNU-S)	1	Tests the PCT link(s) between the SM and the DNU-S. This phase of the CD diagnostic is a common product shared by all PCT-based peripherals.	SM2K:DNUSCD1
	2	Tests the Peripheral Control and Maintenance Bus (PCAMB) interfaces to active and OOS/SBY CC. Both the serial and parallel buses are tested as well as the fuse/fan alarm and the IF sink/source registers that access the PCTLIs. The clock tracking and generating circuits are also tested.	SM2K:DNUSCD2
	3	Tests the Internal Control Bus (ICB) and Peripheral Control Interface (PCI) devices and their interfaces to the ON-LINE and OOS/SBY CC. Also tests the general registers and their interface to the PCIBUS.	SM2K:DNUSCD2
	4	Tests the six PCTLI devices on the CD pack.	SM2K:DNUSCD2
	5	Tests the BPIDBs to the TMUXs.	SM2K:DNUSCD2
CONTROL AND DATA INTERFACE (CDI) (TRUNK UNIT)	1	Tests loopback register, service request register, all seems well (ASW) register, and error source register.	SM:DNCDI
	2	Tests clock errors, data path integrity, and data delay circuits.	SM:DNCDI
	3	Tests the interface with the mate MCTSI. If MCTSI is not ACT/STBY it completes CATP.	SM:DNCDI
COMMON DATA AND COMMON CONTROLLER	1	Tests the PICB (Control) interface.	
	2	Tests circuitry on the COMDAC.	
	3	Tests the control/data integrity to each equipped and ACT application pack. If an application pack is OOS, the tests for that application pack are skipped. This phase also runs the COMDAC resident diagnostics.	
DIRECTLY CONNECTED	1	Tests the CI/CLRT integrity.	SM:DNDCTC
	2	Runs DCTU special diagnostic: CPU test, RAM/ROM tests, GPIB loopback,	SM:DNDCTC

TEST UNIT (DCTU)	3	and arithmetic processor. Tests the CI/CLRT integrity to mate MCTSI.	SM:DNDCTC
DIRECTLY CONNECTED TEST UNIT PORT (DCTU PORT)	1	Runs Group J DCTU tests.	SM:DNPORT
DIGITAL FACILITY INTERFACE (ANN3,ANN5)	1	Tests the active side CI-CLRT. The functions that are verified: 1. Serial transmission capabilities including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities including the subaddresses register, the 4 subaddress registers, and the Peripheral Control Link (PCL) exercise register. 3. CLRT clear capabilities including output-piso, the 4 subaddress registers, and PCL exercise clear. 4. ASW integrity which includes a check for ASW response and an exercise to check the checker. 5. Status latch control which verifies status-reread and explicit clear capabilities as well as a status-latch exercise. 6. PSR test which checks the PSR function and a PSR exercise. ^a	DNec5_1
	2	Tests the mate CI-CLRT communication paths and provides a comprehensive system test for the CLRT. The functions that are verified: 1. Serial transmission capabilities including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities including the subaddress Control Link (PCL) exercise register. 3. CLRT clear capabilities including output-piso, the 4 subaddress registers, and PCL exercise clear. 4. ASW integrity which includes a check for ASW response and an exercise to check the checker. 5. Status latch control which verifies status-reread and explicit clear capabilities as well as a status-latch exercise. 6. PSR test which checks the PSR function and a PSR exercise. ^a	DNec5_1
	3	Tests the integrity of the CCB interface.	DNec5_1

The functions verified by this phase are:

1. The integrity of the transmission path between CLRT & CCB.
2. The CCB Data Ram is accessible both for reading and writing.
3. The Flag Ram is accessible both for reading and writing.
4. The decision tree for pinpointing raised flags works (activity flags, summary flags).
5. All error reporting mechanisms are in working order (address matching, parity errors).
6. That the clear operation visibly works. ^a

4

This phase insures that the up can be brought up from a cold start and that the firmware enters its process schedule routine. The functions that are verified in this phase are:

1. Partial check of up to CCB data access and flag protocol.

DNec5_2

2. Sanity time-out indicator (shows that the firmware is cycling in process scheduler). ^a

5

This phase tests the PMTG parity walker and the firmware parity error reporting mechanism. It also verifies that the PMTG does not corrupt data passed through it on the active or mate PIDB. The functions verified by this phase are:

1. The circuit's ability to pass PCM and signaling information at the circuit interface is verified by looping through the PMTG over the active and mate PIDBs.
2. The firmware error reporting mechanism is enabled and verified by detecting transmit and receive errors with the PMTG.
3. The circuit's ability to pass PCM and signaling information through the circuit is verified by looping PCM and signaling information through the companion DFI over the far-end active and mate PIDBs.
4. The PMTG parity walker circuitry is verified by forcing the companion DFI to loose synchronization. ^a

DNec5_2

6

The functions verified by this phase are: 1. That the LST can both transmit and receive 2400 HZ, 2600 Hz and 2400/2600 Hz combined tones for all

DNec5_2

7	30 channels. ^a This phase verifies that echo cancellation can be disabled using the 2100Hz disabling tone. This phase verifies: 1. The 2100Hz tone recognition and echo cancellation control circuitry. 2. Echo Cancellation and Voice Path Assurance tests. ^a	DNec5_2
9	This phase initializes and tests the CI-CLRT communication paths and provides a comprehensive system test for the CLRT. ^a	DNuci
10	This segment clears all CCB latches and registers except the flag and data registers.	DNuci
11	This phase insures that the uC can be brought up from a cold start and that the firmware enters its process schedule routine. The DFI is automatically looped on itself by the firmware as part of the initialization process.	DNuci
12	This phase provides a comprehensive check of the Maintenance Buffer and its internal latches.	DNdfig1
13	This phase writes various exercise patterns to the control streams of each of the three LSI devices and checks for the correct response. Interaction among the MB, TF, RS, FR, CCB and the firmware is quite extensive, so this phase should give a good indication of the health of the LSI.	DNdfig1
14	Like the previous phase, this phase writes exercises to the LSI devices. However, these exercises bring up facility alarms that are service affecting. Hence, these exercises must be run out-of-service. Also note that the facility response register in the CCB contains the exercise response.	DNdfig1
15	This phase checks the address and data bus of the uC as well as the integrity of the firmware via the firmware fault flag.	DNdfig2
16	This phase verifies the integrity of the signaling and PCM data paths in the DFI. Both the active and mate PIDB's are checked.	DNdfig2
17	This phase tests the mate-side CI by running the same tests as in Phase 1. The only difference is that the CLRT is now accessed via the mate CI.	DNdfig3
18	Tests the XPC-8 Protocol Controller chip, the Dual Port Ram (DPR), and the internal Facility Data Link (FDL)	DNdfig3

DIGITAL FACILITY INTERFACE (DFI) (TN1611 or TN1612) or (TN1618 or TN1619 in future)	19	path. This phase uses the active and standby FIU to test the operation of the T1 Clock and T1 Status leads from the RSM DFI to both FIU sides.	DNdfig3
	20	This phase loops PCM and Signaling data from the Active TSI to the looped RSM DFI.	DNdfig3
	1	Tests the active side CI-CLRT. The functions that are verified: 1. Serial transmission capabilities including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities including the subaddress register, the 4 subaddress registers, and the Peripheral Control Link (PCL) exercise register. 3. CLRT clear capabilities including output-piso, the 4 subaddress registers, and PCL exercise clear. 4. ASW integrity which includes a check for ASW response and an exercise to check the checker. 5. Status latch control which verifies status-reread and explicit clear capabilities as well as a status-latch exercise. 6. PSR test which checks the PSR function and a PSR exercise.	DNec5_1
	2	Tests the mate CI-CLRT communication paths and provides a comprehensive system test for the CLRT. The functions that are verified: 1. Serial transmission capabilities including the PICB transmission paths, order start code, order parity, and serial loop back checks. 2. Parallel loop back capabilities including the subaddress register, the 4 subaddress registers, and the Peripheral Control Link (PCL) exercise register. 3. CLRT clear capabilities including output-piso, the 4 subaddress registers, and PCL exercise clear. 4. ASW integrity which includes a check for ASW response and an exercise to check the checker. 5. Status latch control which verifies status-reread and explicit clear capabilities as well as a status-latch exercise.	DNec5_1

3	<p>6. PSR test which checks the PSR function and a PSR exercise. Tests the integrity of the CCB interface. The functions verified by this phase are:</p> <ol style="list-style-type: none"> 1. The integrity of the transmission path between CLRT & CCB. 2. The CCB Data Ram is accessible both for reading and writing. 3. The Flag Ram is accessible both for reading and writing. 4. The decision tree for pinpointing raised flags works (activity flags, summary flags). 5. All error reporting mechanisms are in working order (address, matching, parity errors). 6. That the clear operation visibly works. 	DNec5_1
4	<p>This phase insures that the uP can be brought up from a cold start and that the firmware enters its process schedule routine. Functions that are verified in this phase are:</p> <ol style="list-style-type: none"> 1. Partial check of up to CCB data access and flag protocol. 2. Sanity time-out indicator (shows that the firmware is cycling in process scheduler). 	DNec5_2
5	<p>This phase tests the PMTG parity walker and the firmware parity error reporting mechanism. It also verifies that the PMTG does not corrupt data passed through it on the active or mate PIDB. The functions verified by this phase are:</p> <ol style="list-style-type: none"> 1. The circuit's ability to pass PCM and signaling information at the circuit interface is verified by looping through the PMTG over the active and mate PIDBs. 2. The firmware error reporting mechanism is enabled and verified by detecting transmit and receive errors with the PMTG. 3. The circuit's ability to pass PCM and signaling information through the circuit is verified by looping PCM and signaling information through the companion DFI over the far-end active and mate PIDBs. 4. The PMTG parity walker circuitry is verified by forcing the companion DFI to loose synchronization. 	DNec5_2
6	<p>The functions verified by this phase</p>	DNec5_2

	are: 1. That the LST can both transmit and receive 2400 Hz, 2600 Hz and 2400/2600 Hz combined tones for all 30 channels.	
7	This phase verifies that echo cancellation can be disabled using the 2100Hz disabling tone. This phase verifies: 1. The 2100 Hz tone recognition and echo cancellation control circuitry. 2. Echo Cancellation and Voice Path Assurance tests.	DNec5_2
9	This phase verifies the PICB interface between the active/standby MCTSI and the DFI control interface. The PICB interface circuits (parity check, start code check, and ability to force ASW errors) are verified. If the MCTSI is not duplex (ACT/STBY), only the interface to the active processor is tested and the phase completes CATP.	SM:DNUCI
10	This phase tests interface functions which are accessible through the module processor (MP) port. This includes testing of the first in - first out (FIFO) registers RAM, RAM parity checker/generator, summary scan registers, error source registers, mailbox registers, and mask registers.	SM:DNUCI
11	This phase tests the interface between the MP and local processor (LP) via the universal control interface (UCI) device. The specific tests are summary scan, interrupts and masks for the LP, access to registers, and interrupt in the hardware error source register (ESR) for errors on the LP.	SM:DNUCI
12	This phase tests that the uP can be brought up from a cold start and that the firmware enters its process scheduler routine. The sanity time-out indicator is verified which shows that the firmware is cycling in the process scheduler. A check of the equalizer value leads to the digital signal interface (DSI) is also performed.	SM:DNDFID1
13	This phase checks the response of firmware that runs EPROM and RAM diagnostics.	SM:DNDFID1
14	This phase verifies the integrity of the transceiver (XCVR) uP interface. The transmitter, receive synchronizer, and framer functions are checked via demand exercises performed in firmware. This phase also checks the XCVR framer, remote frame alarm,	SM:DNDFID2

	15	remote multiframe alarm, and receive synchronizer counter functions. The XCVR RAM is checked by running facility side for all the above tests. This phase verifies the integrity of the signaling and PCM data paths in the DFI. Both the active and standby MCTSI PIDs are checked. The alternate data RAM is used to source 8-bit PCM data toward the DFI. Signaling bits are supplied by the SP. Since the DFI is looped on itself, the data and signaling bits are sent back to the alternate data RAM where they are verified.	SM:DNDFFID3
DIGITAL FACILITY INTERFACE HOST (DFIH)	16	(TN1612 only). This phase tests the XPC (X.25 protocol controller) by writing different patterns to the talk-back channel and verifies a response pattern. With both paths of the RSM DFI looped at the far-end, the talk-back channel is used as a means of checking the XPC.	SM:DNDFFID3
	17	(TN1612 only). This phase sends PCM data and signaling from the MCTSI to the looped RSM DFI. A single time slot is sourced from the MCTSI and sent through the FIU-DLI to the DFI. Both active and mate FIU-DLI paths are verified.	SM:DNDFFID3
	18	(TN1612 only). This phase tests the operation of the T1 status leads from the RSM DFI to both FIU sides of an RSM.	SM:DNDFFID3
	1	This phase, if the HDFI is the H1DFI, verifies the PICB interface to the unified control interface (UCI) from the ACT/STBY MCTSI.	SM:DNUCI
	2	This phase on the H1DFI verifies operation of the UCI chip from the SMP end.	SM:DNUCI
	3	This phase on the H1DFI tests the logical port (LP) of the UCI. It also verifies communication between the SMP and the LP via the UCI and the associated interrupts to the LP.	SM:DNUCI
	4	This phase on the HDFI initializes and tests the CI/CLRT communication paths and provides a comprehensive system test for the CLRT.	SM:DNDFFR1
	5	This phase on the HDFI ensures the following: (1) The integrity of the transmission path between the CLRT and the CCB. (2) That the CCB data RAM and CCB flag RAM are	SM:DNDFFR1

	accessible both for reading and writing.	
	(3) That the decision tree for pinpointing raised flag works. (4) That all error reporting mechanisms are in working order. (5) That the clear operation visibly works.	
6	This phase ensures that the uP can be brought up from a cold start and that the firmware enters its process schedule routine on the HDFI. It partially checks the uP to CCB data access and flag protocol, sanity time-out indicator, and loop monitor indicator.	SM:DNDFR11
7	This phase provides a comprehensive check of the maintenance buffer and its internal latches including the report synchronizer, transmit formatter, framer control and report stream registers, register clear register, error source register, and general purpose latch on the HDFI.	SM:DNDFR11
8	This phase writes various exercise patterns to the control streams of each of the three LSI devices on the HDFI and checks for the correct response. Interaction among the MB, TF, RS, FR, CCB, and the firmware is extensive, so this phase gives a good indication of the health of the LSI.	SM:DNDFR12
9	This phase, like phase 8, writes exercises to the LSI devices. However, these exercises bring up facility alarms that are service affecting. The TF does not have any facility alarm exercises.	SM:DNDFR12
10	This phase checks facility alarm reporting on the HDFI in an indirect manner by taking advantage of the fact that the uP, when functioning properly, reports facility alarms routinely (via firmware). Hence, this phase checks the address and data bus of the uP as well as the integrity of the firmware via the device summary register.	SM:DNDFR12
11	This phase verifies the integrity of the signaling and PCM data paths in the HDFI. Both the ACT and STBY PIDBs are checked.	SM:DNDFR12
12	This phase tests the standby side CI by running the same tests as in Phase 4. The only difference is that the CLRT is now accessed via the standby CI.	SM:DNDFR12
13	This phase tests the XPC protocol controller in the HDFI. It tests the XPC by writing different patterns to talk-back channel and verifying a response of a	SM:DNDFR12

	<p>true data pattern. In H1s, this test is performed for the different number time slots that can be used for the control channel in the DLI.</p>	
14	<p>This phase checks uP EPROM and RAM on the HDFI.</p>	SM:DNDFRI2
15	<p>This phase ensures that the uP can be brought up from a cold start and that the firmware enters its process schedule routine on the RDFI. It partially checks uP (R1, R2) to CCB (H1, H2) data access and flag protocol and sanity time-out.</p>	SM:DNDFRI2
16	<p>This phase provides a comprehensive check of the SM:DNDFRI3 maintenance buffer and its internal latches including receive synchronizer, transmit formatter, and framer control and report stream registers, register clear register, error source register, and general purpose latch on the RDFI.</p>	SM:DNDFRI3
17	<p>This phase writes various exercise patterns to the control streams of each of the three LSI devices on the RDFI and checks the correct response. Interaction among the MB, TF, RS, FR, CCB, and the firmware is quite extensive, so this phase gives a good indication of the health of the LSI.</p>	SM:DNDFRI3
18	<p>This phase, like phase 17, writes exercises to the LSI devices. However, these exercises bring up facility alarms that are service affecting. The TF does not have any facility alarm exercises.</p>	SM:DNDFRI3
19	<p>This phase checks XPC function in the RDFI. It also checks facility alarm reporting in an indirect manner by taking advantage of the fact that the uP, when functioning properly, reports facility alarms routinely (via firmware). Hence, this phase checks the address and data bus of the uP as well as the integrity of the firmware via the device summary register.</p>	SM:DNDFRI4
20	<p>This phase verifies the integrity of the signaling and PCM data paths in the RDFI. Both the ACT and STBY PIDBs are checked. For one segment, the remote DFI is looped on itself. The looping takes place in the PMTB so that time slot 7 is returned directly to the transmit formatter. For another segment, the RDFI is unlooped and a CD is looped.</p>	SM:DNDFRI4
21	<p>This phase checks the uP EPROM and</p>	SM:DNDFRI4

	22	RAM on the RDFI using on-board test routines. This phase checks the PMTG functions on the RDFI including the walking parity mask and error registers, control register, and remote loss of clock register.	SM:DNDFRI4
	23	This phase checks the operation of the control interface (CI) in the R1DFI. The primary responsibility of the CI is to recreate the PICB interface at the remote site in a manner similar to that in the non-remote application.	SM:DNDFRI4
	24	This phase tests the communication between the SMP and the H1DFI through the PICB bypass FIFO circuit by writing data in various RAM locations in the UCI and verifying that the same data is returned in the corresponding locations.	SM:DNDFRI4
DIGITAL FACILITY TEST ACCESS CIRCUIT (DFTAC)	1	Verifies board ID and basic register operation.	SM:DNDFTAC
	2	Tests junctor network and monitor and talk circuits.	SM:DNDFTAC
DIST (SM)	1	Tests send and receive data via MSUCOM operation of relay drivers.	SM:DNDIST
DATA LINK INTERFACE HOST SM	1	Active MP to DLI communication and interface tests.	SM:DNDLI1
	2	Performs DLI internal function tests (I). Performs DLI internal function tests (II). Performs active TSI to DLI interface tests.	SM:DNDLI1
	3		SM:DNDLI1
	6		SM:DNDLI2
	7	Performs standby MP to DLI interface tests.	SM:DNDLI2
	8	Performs standby MP SDLC to DLI interrupt and data tests.	SM:DNDLI2
	9	Performs standby TSI to data loopback interface (DLI) tests. Also tests the standby TSI to TRCU loopback tests in	SM:DNPDLI3
	10	Optically Remote Modules (ORM). Performs switch/monitor tests.	SM:DNPDLI3
11	Performs the TMS NCT link tests.	SM:DNPDLI3	
EQUIPMENT ACCESS NETWORK (EAN)	1	Runs Group H DCTU tests.	SM:DNEAN
GLOBAL DIGITAL SERVICE UNIT COMMON (GDSSUCOM)	1	Tests control interface with the active MCTSI. Will complete CATP if the MCTSI is not ACT/STBY	SM:DNGDSC1
	2	Tests control interface with the mate MCTSI. Will complete NTR if the MCTSI is not ACT/STBY.	SM:DNGDSC1
	3	Tests the TSSR.	SM:DNGDSC1
	4	Tests the parity checkers and	SM:DNGDSC2

	5	generators. Tests interrupt registers, DSC parity error, DSC fault, and summary scan.	SM:DNLDSC2
	6	Tests data links to/from active and mate MCTSIs (if mate MCTSI is OOS - executes CATP).	SM:DNLDSC2
GATED-DIODE CROSSPOINT ACCESS (GDAXS)	1	Tests initialization. SM: DNAXS1 (for LU1) or SM: DNCAXS1 (for LU2&LU3).	SM:DNAXS1 (LU1) SM:DNCAXS1 (LU2&LU3)
	2	Verifies crosspoints that make up the 6-by-6 test access network. If cannot test access to all HLSCs (HLSC is busy), completes CATP.	SM:DNAXS1 (LU1) SM:DNCAXS1 (LU2)
	3	Verifies operation of crosspoints which make up the 32 by 8 B-LINK access network. If cannot test access to all HLSCs (HLSC is busy), completes CATP.	SM:DNAXS2 (LU1) SM:DNCAXS1 (LU2&LU3)
	4	Verifies operation of crosspoints of the 32 forward/reverse networks associated with the channel circuits in this service group.	SM:DNAXS3 (LU1) SM:DNCAXS2 (LU2&LU3)
	5	Verifies access network crosspoints which connect B-LINKS to the GDAX linearization circuit.	SM:DNAXS4 (LU1) SM:DNCAXS2 (LU2&LU3)
	6	Verifies operation of the GDAX linearization circuit.	SM:DNAXS4 (LU1) SM:DNCAXS2 (LU2&LU3)
GATED-DIODE CROSSPOINT COMPENSATOR	1	Tests receive control orders from the MSUCOM and performs a compensation.	SM:DNMCOMP
GATED-DIODE CROSSPOINT CONCENTRATOR	1	Tests the load and read data from the source gate array and the alarm mask destination.	SM:DNGCTR
	2	Tests the enable checking and reporting circuits.	SM:DNGCTR
	3	Tests the power alarm reporting, storing, and inhibiting circuits.	SM:DNGCTR
	4	Tests transmission, loading, and reading of data to the concentrator line groups.	SM:DNGCTR
	5	Tests circuits which inhibit writes and reads to the concentrator when a multiple enable is detected.	SM:DNGCTR
	6	Turns on the network controller lamp for one second, then off for one second. Test is repeated seven times, and then the lamp is left on.	SM:DNGCTR
GRID/ GRID BOARD	1	Tests the grid alarm status, verifies the loopable test bit positions of both grid destination gate arrays, initializes all grid crosspoints to their off state, and verifies the pseudo alarm capability of the grid to both SG network controllers.	SM:DNGRD (LU1) SM:DNCGRD (LU2&LU3)
	2	Verifies the ability to write and read the state of each crosspoint control latch for the scan cutoff crosspoints in the	SM:DNGRD (LU1) SM:DNCGRD (LU2&LU3)

	3	grid. The actual connect/disconnect state of the crosspoints are not verified. Verifies the ability to write and read the state of each crosspoint control latch for the second stage crosspoints in the grid. The actual connect/disconnect state of the crosspoint are not verified. Also, crosspoint address decoding is tested for the possibility of stuck bits of "do not care" states which cause erroneous or multiple operation of crosspoints.	SM:DNGRD (LU1) SM:DNCGRD (LU2&LU3)
	4	Verifies the ability to write and read the state of each crosspoint control latch for the first stage crosspoints in the grid. The actual connect/disconnect states of the crosspoints are not verified.	SM:DNGRD (LU1) SM:DNCGRD (LU2&LU3)
	5	Checks the operation of the summary scan transition latch programming on the grid.	SM:DNGRD (LU1) SM:DNCGRD (LU2&LU3)
GRID/ GRID BOARD EXERCISE	1	Tests the scan cutoff crosspoints and associated scan circuitry on each of the ports.	SM:DNFABEX (LU1-LU3)
	2	Tests the first stage crosspoints along the A-LINKS.	SM:DNFABEX
	3	Tests the second stage crosspoints along with the B-LINKS.	SM:DNFABEX (LU1-LU3)
GRID/ GRID BOARD PATH TEST	1	Tests grid portion of the path for a resistive leak to ground.	SM:DNLUP2 (LU1) SM:DNLUP3 (LU2&LU3)
	2	Tests the path (grid and loop facility) for a dangerously high voltage (AC and/or DC).	Same as 1
	3	Tests the path (grid and loop facility) for an extraneous voltage. Also tests loop facility for a resistive leak and short between TR leads.	SM:DNLUP2 (LU1) SM:DNLUP3 (LU2&LU3)
	4	Verifies the scan origination circuit's ability to detect off-hook for 200- and 2500-Ω loops and tests the scan cutoff crosspoints for stuck open failures.	Same as 3
	5	Tests scan cutoff crosspoints for stuck closed failures.	Same as 3
	6	Tests the first stage crosspoint of the path for stuck open failures. Tip, ring, or failures on both leads are specifically indicated.	Same as 3
	7	Tests the first stage crosspoint of the path for stuck closed failures. Tip, ring, or failures on both leads are specifically indicated.	Same as 3
	8	Tests the second stage crosspoint of the path for stuck open failures. Tip, ring, or failures on both leads are specifically indicated.	Same as 3
	9	Tests the second stage crosspoint of	Same as 3

		the path for stuck closed failures. Tip, ring, or failures on both leads are specifically indicated.	
	94	Reverse channel battery is applied, scan cutoff crosspoints are open and first and second stage crosspoints are closed.	Same as 3 b
	95	Forward channel battery is applied, scan cutoff crosspoints are open and first and second stage crosspoints are closed.	Same as 3 b
	96	First and second stage crosspoints are closed. Both tip and ring scan crosspoints are open.	SM:DNLUP2 (LU1) SM:DNLUP3 (LU2&LU3) b
	97	Ring scan and first and second stage crosspoints are closed. Tip scan crosspoint is open.	Same as 96 b
	98	Tip scan and first and second stage crosspoints are closed. Ring scan crosspoint is open.	Same as 96 b
	99	Both tip and ring scan crosspoints and the first and second stage crosspoints are closed.	Same as 96 b
HOST DIGITAL FACILITY INTERFACE	1	Tests the CI/CLRT integrity.	SM:DNDFIG1
	2	Tests the CCB integrity.	SM:DNDFIG1
	3	Tests the μ C integrity.	SM:DNDFIG1
	4	Tests maintenance buffer integrity.	SM:DNDFIG2
	5	Tests LSI exercises I.	SM:DNDFIG2
	6	Tests LSI exercises II.	SM:DNDFIG3
	7	Tests facility alarm check.	SM:DNDFIG3
	8	Tests transmit and receive signaling and PCM data paths.	SM:DNDFIG3
	9	Tests mate CI/CLRT check.	SM:DNDFIG3
	10	Tests DPR, XPC, FDL integrity.	SM:DNDFIG4
INTEGRATED DIGITAL CARRIER UNIT (IDCU)	1	Verifies the PICB interface from the active and standby MCTSI.	SM:DNUCI
	2	Verifies operation of the Common Control Processor (CCP) Unified Control Interface (UCI) chip from the SMP end.	SM:DNUCI
	3	Tests the Local Processor (LP) of the CCP UCI. The module controller (MC) sends messages through the UCI for the LP, which upon receipt of the messages, performs the required reads and writes to the UCI, and internal reads and writes to verify interrupts to the LP.	SM:DNUCI
	4	Verifies operation of the timers, sanity timer, processor interrupts, and NMIs. It also tests EPROM, I/O write protection circuits, and address and data parity generators and checkers.	SM:DNIDCOM
	5	Verifies the control interface between the PTI (PIDB Transmission Interface) control logic and all PTI VLSI devices: PRF (PIDB Receive Formatter), TSI	SM:DNIDCOM

	(Time Slot Interchanger), SP (Signal Processor), and CI (Control Interface). The VLSI devices are tested to the extent possible (for example, alarms, BIST, etc.) without using the data paths. The interrupt masking and clock selection/detection circuitry is also tested.	
6	Verifies the functionality of the PTL internal data paths and interconnection of the PRF, SP, and TSI devices.	SM:DNIDCOM
7	This phase tests the mate access bus by verifying communication from the ACT CCP to the CCP under test with the side under test in hold.	SM:DNIDCOM
8	This phase tests the mate access bus by verifying communication from the CCP under test to the ACT CCP with the ACT CCP put in hold.	SM:DNIDCOM
9	This phase verifies all (D)PIDB connections and associated (D)PIDB interface circuitry.	SM:DNIDCOM
10	This phase runs a memory test on the CC memory (RAM).	SM:DNIDCOM
21	Verifies the ICB (Internal Control Bus) interface from the PTI to the LSI (Loop Side Interface) pack.	SM:DNLSI1
22	Verify operation of the LSI UCI chip from the PTI end.	SM:DNLSI1
23	Tests the LP of the LSI. The CCP sends messages through the UCI for the LP, which upon receipt of the messages, performs the required reads and writes to the UCI, and internal reads and writes to verify interrupts to the LP.	SM:DNLSI1
24	This phase runs a memory test on all of the LSI memory (RAM).	SM:DNLSI1
25	Verifies the LSI processor, processor clock, interrupts, timers, sanity timer, 4-MHz clock detector circuit, and EPROM. It also verifies communication from LSI to DLPs (Data Link Processor) and functionality of the DLP, DLP RAM, DLP timers and interrupts, and control to SCC (Serial Communication Controller) devices. Lastly it verifies control to the rest of the devices on the pack such as the transceivers and the time slot multiplexer/	SM:DNLSI1
26	demultiplexer. Verifies the functionality of the LSI internal data paths and interconnection of the time slot multiplexer/ demultiplexer, transceiver, SCC,	SM:DNLSI1

		and DSI (digital signal interface) devices.	
	27	Verifies all Internal Data Bus (IDB) connections and associated IDB interface circuitry.	SM:DNLSI1
	28	(Demand phase only for factory and installation use). Verifies the LSI switch circuitry mainly that on the DSI device and the sync signals between the two SGs. The LSIs in both SGs must be in the growth state.	SM:DNLSI2
	29	(Demand phase only for factory and installation use). Verifies the DSI output drivers and the data paths between the LSI and ELI (Electrical Line Interface) along with the output of the ELI. This phase requires a special loopback connector on the backplane. The LSIs in both SGs must be in the growth state, of the unit must be duplex failed.	SM:DNLSI2
	30	(Demand phase only for factory and installation use). Verifies a HITLESS switch can be performed. This phase requires a special loopback connector on the backplane. The LSIs in both SGs must be in the growth state.	SM:DNLSI2
INTEGRATED SERVICE LINE UNIT COMMON CONTROL	1	Verifies the PICB interface from the ACT and STBY MCTSI.	SM:DNUCI
	2	Verifies operation of the UCI chip from the SMP end.	SM:DNUCI
	3	Tests the LP of the UCI. The module controller (MC) sends messages through the UCI for the LP, which upon receipt of the messages, performs the required reads and writes to the UCI, and internal reads and writes to verify interrupts to the LP.	SM:DNUCI[
	4	Verifies operation of the timers in the CC uP, sanity timer, PIC, and NMIs. It also tests EPROM, I/O write protection circuits, and address and data parity generators and checkers.	SM:DNICC
	5	Verifies operation of the control sequencer on the CC under test. This includes the CS register, the sync circuitry, the CS memory, the CS memory parity generators and checkers, the 2-MHz interface and its error detection and propagation, and the 4-MHz interface and its error detection and propagation.	SM:DNICC
	6	Verifies the interface between the CC and peripheral boards. It also verifies operation of the enable controller,	SM:DNICC

	7	ASW controller, and the service request controller. This phase verifies operation of the mate access bus from the ACT CC to the CC under test. It also verifies peripheral select bit and the CIDB interface to the ACT CD.	SM:DNICC
	8	This phase verifies operation of the mate access bus from the CC under test to the ACT CC.	SM:DNICC
	9	This phase runs memory test on the CC memory (RAM).	SM:DNICC
INTEGRATED SERVICE LINE UNIT COMMON DATA (ISLUCD)	1	Verifies the interface between the CD under test and the ACT and STBY CCs. It also tests the peripheral register access controller's service request register and its mask register.	SM:DNICD
	2	Tests the parity generators and checkers used in the PCM - MUX for its different control memory banks (A, B, and T).	SM:DNICD
	3	This phase runs a memory test on all of the CDs in the PCM-MUX control memory.	SM:DNICD
	4	Tests the CIDB interface to the ACT and STBY CC from the CD under test and the corresponding configuration bits. This phase does not perform any test if the CCs are not duplex.	SM:DNICD
	5	Verifies multiplexing function of the CD between all PIDBs and equipped LGCs by looping data at the LGC, using on-board signature only.	SM:DNICD
	6	Verifies data interface between the CD packs and the ACT/STBY DI and the ACT/STBY DFs.	SM:DNICD
INTEGRATED SERVICE LINE UNIT HIGH-LEVEL SERVICE CIRCUIT (ISLUHLSC)	1	This phase verifies communication between the ACT/STBY CCs and the HLSC. Also, it tests the ability to shut down the power converter on the HLSC and ring tip service request. Finally, it verifies the firmware version.	SM:DNIZHSC
	2	This phase tests the internals of the HLSC with self-test routines.	SM:DNIZHSC
	3	This phase tests the HLSC buses 0 and 1 output relays. It also verifies the ring tip function and the ability of the HLSC to supply DC voltages.	SM:DNIZHSC
INTEGRATED SERVICE LINE UNIT LINE CARD (ISLULC) T-CARD	1	Verifies the control interfaces to the line card, the function of the maintenance circuitry and its masks, and the directed scanning and isolation functions.	SM:DNITC
	2	Verifies a test for single-bit errors in the time slot comparator and parity of the B	SM:DNITC

INTEGRATED SERVICE LINE UNIT LINE CARD (ISLULC) U-CARD ^c	3	and D channels. It also tests the ability of the T-Card to communicate over a path to the TSI. [A duplex path (two time slots at the TSI, the same time slot number on LIDB sides 0 and 1 to the card under test) is set up between the active TSI and the T-Card under test. The dual upstream mode of the card is also tested over this duplex path]. This phase only runs on ISLULC diagnosis with LC option requested. It verifies the time slot comparator, the origination and fault scan operation, and the broadcast mode operation.	SM:DNITC
	1	This phase is concerned with the control access to the line card through primitive reads and writes provided by ISLU base software. This phase checks the control path to the line card. This test checks for proper register access as a foundation to other tests. It also verifies that all error register flags operate correctly. It also verifies the time slot selection feature of the line card.	SM:DNISUC
	2	This phase runs for all sources. This phase is concerned with the various channels' mode of operation. The group interface data bus (GIDB) path, e-bit control, and data parity are examined. Also, this phase checks local loopback of data, U-K logic, and verification of the echo canceler. Finally, this phase checks the operation of the spare U-DSL card and the U-DSL card crosspoints via the line group bus, and the ability to spare the line card is examined via the spare bus.	SM:DNISUC
	3	This phase can only be run if the ISLULC is OOS. To run this phase you must run the ISLULC diagnostic with the LC option. This phase checks the broadcast features of the LC and performs fault and summary line group scan tests. It also does a full test of the B and D time slot comparator.	SM:DNISUC
	4	(Demand phase only). For the AMI U-Card, this phase examines the upstream responses to changes in the downstream N-channel signaling using the NT1. For the ANS [®] U-Card, this phase examines the upstream response to the downstream EOC messages sent to the NT1. For both	SM:DNISUC

	5	<p>the AMI and ANS[®] U-Cards, this phase verifies that each channel can transmit and receive without data corruption through loopbacks and a digital source. Each channel is also checked for data integrity. This phase also does a Metallic Mismatch test to check for a mismatch between the LC/NT1 installed and the ODD and also a check for a T/R open or short. For AMI it checks for a T/R reversal. [PR Name=SM: DNISUC]. This phase is used only by the ANS[®] U-Card. This phase runs for all sources except Automatic which is called by Fault Recovery. This phase performs tests to check the PM circuitry. [PR Name=SM: DNISUC].</p>	SM:DNISUC
<p>INTEGRATED SERVICE LINE UNIT LINE CARD (ISLULC) Z-CARD</p>	1	<p>This phase verifies the control interface to the line card. It also verifies the function of the maintenance circuitry and its masks. It also tests the digital circuitry to the MCTSI and e-bit control.</p>	SM:DNIZC1
	2	<p>This phase tests the DC portion of the line card which can be tested without closing the tip/ring crosspoints. It also tests spare bus continuity if the card is a spare card.</p>	SM:DNIZC1
	3	<p>This phase tests the remaining DC portion of the line SM:DNIZC1 card through metallic access buses 0 and 1.</p>	SM:DNIZC1
	4	<p>This phase tests the ring tip circuit on the line card.</p>	SM:DNIZC1
	5	<p>This phase performs basic transmission testing within the ISLU.</p>	SM:DNIZC3
	6	<p>(Demand phase only). This phase performs comprehensive transmission tests including auto-out, idle channel noise, receive and transmit filters, balance network, and gain states.</p>	SM:DNIZC2
	7	<p>This phase performs basic time slot comparator check.</p>	SM:DNIZC3
	8	<p>(Demand phase only). This phase runs the tests that may interfere with a private branch exchange (PBX) if the line is a PBX line.</p>	SM:DNIZC2
	9	<p>This phase runs only if the ISLULGC diagnostic is requested with the LC option. This phase tests the summary scan, fault scan, and performs comprehensive time slot comparator check.</p>	SM:DNIZC2
<p>INTEGRATED SERVICE</p>	1	<p>Verifies the interface to the LGC from the ACT/STBY major and minor CD. It</p>	SM:DNLGC

LINE UNIT LINE GROUP CONTROLLER (ISLULGC)	2	also tests the internal logic and bit decoding, and verifies the ability to communicate with a line card over both GIDBs. Verifies the interface from the LGC to each equipped line card in the SG - not OOS due to a faulty condition. Also, each line card in an OOS faulty condition is verified that no directed scan is detected when it is isolated.	SM:DNLGC
	3	Verifies the directed, faulty, and summary scan from each equipped line card in the SG - not OOS due to a faulty condition.	SM:DNLGC
	4	Verifies operation of the loopback mode for the LGC. In this mode, data and control are looped back to the STBY CC from the LGC under test.	SM:DNLGC
	1	This phase verifies communication between SM:DNMAN ACT/STBY CCs and the MAN circuit pack. It also verifies the reset function that de-energizes all relays and associated latches.	SM:DNMAN
INTEGRATED SERVICE LINE UNIT METALLIC ACCESS NETWORK (ISLUMAN)	2	This phase tests the MTB relays, test termination relays, ringing generator maintenance relays, and spare relays. Also, it tests protocol circuit, MTB protection circuit, and verifies that the MAN circuit pack is disconnected from mate MAN circuit pack on spare bus.	SM:DNMAN
	3	This phase tests all RG relays on the MAN circuit pack.	SM:DNMAN
	4	This phase tests all relays on the MAN circuit pack associated with HLSCs.	SM:DNMAN
	5	(Demand phase only). This phase verifies that there are no foreign tip/ring shorts and/or voltage potentials connected to the MAN circuit pack and more testing is done on the MTB relays.	SM:DNMAN
	1	This phase verifies communication between ACT/STBY CCs.	SM:DNIRG
INTEGRATED SERVICE LINE UNIT RING GENERATOR (ISLURG)	2	This phase tests the RG voltages and four different modes. Namely, the modes are as follows: (1) Earth backed with ring on tip lead (2) Earth backed with ring on ring lead (3) Battery backed with ring on ring lead (4) Battery backed with ring on tip lead. It also tests the sources of service	SM:DNIRG

	3	request on the RG and verifies that the RGs ringing frequency agrees with that of ODD. This phase verifies that the RG can output its ringing voltage to each of the 4 metallic access network (MAN) CPs. In addition, the bus connect fault (BCF) service request is also tested.	SM:DNIRG
INTEGRATED SERVICES TEST FACILITY (ISTF)	1	Same as Phase 1 LDSU (SM).	SM:DNUCI
	2	Same as Phase 2 LDSU (SM).	SM:DNUCI
	3	Same as Phase 3 LDSU (SM).	SM:DNUCI
	4	Same as Phase 4 LDSU (SM).	SM:DNDSU2
	5	Same as Phase 5 LDSU (SM).	SM:DNDSU2
	6	Same as Phase 6 LDSU (SM).	SM:DNDSU2
	8	Performs memory test, and operational image pump verification.	SM:DNDSU2
	LINE CIRCUIT (LC)	1000	Verifies the LC functionality by requesting the application pack firmware to run tests on the circuits, including PCM path tests between the LC and the controlling COMDAC.
Local Digital Service Unit (LDSU)	1	Tests CI with ACT and STBY MCTSI. If STBY MCTSI is OOS, then CATP completes	SM:DNUCI
	2	Tests the internal functions of the UCI chip on the LDSU.	SM:DNUCI
	3	Tests the LP - UCI interface.	SM:DNUCI
	4	Tests LDSU interface to DSU2.	SM:DNDSU2
	5	Performs LP tests-interrupt controller, timers, parity, and write protect	SM:DNDSU2
	6	Tests DSPs, SDI, and data to/from LDSU bus.	SM:DNDSU2
	8	Performs memory test and operational image pump verification.	SM:DNDSU2
LOCAL DIGITAL SERVICE FUNCTION (LDSF)	1	Verifies the PICB interface from the ACT and STBY MCTSI.	SM:DNUCI
	2	Verifies operation of the UCI chip from the SMP end.	SM:DNUCI
	3	UCI tests the interface to the LP side. The MC sends messages through the UCI for the LP, which, upon receipt of the messages, performs the required reads and writes to the UCI and internal reads and writes to verify interrupts to the LP.	SM:DNUCI
	4	Phase 4 of the DSC3 diagnostic. Verifies all hardware of the circuit pack and its interface to PICBs and PIDBs. All segments which are executed entirely by resident software have the "LP" prefix; all others use the resident software indirectly.	DNds3_4
LOCAL	1	Tests control interface with active and	SM:DNUCI

DIGITAL SERVICES UNIT (LDSU)		mate MCTSI. If mate MCTSI is OOS, CATP runs.	
	2	Tests the internal functions of the UCI chip on the LDSU.	SM:DNUCI
	3	Tests the local processor (LP) - UCI interface.	SM:DNUCI
	4	Tests LDSU bus interface to DSU2.	SM:DNDSU2
	5	Performs LP tests - interrupt controller, timers, parity and write protect.	SM:DNDSU2
	6	Tests digital signal processors (DSPs), serial data interface, and data to/from LDSU bus.	SM:DNDSU2
	8	Performs memory test.	SM:DNDSU2
	LOCAL DIGITAL SERVICES UNIT COMMON (LDSUCOM)	1	Tests control interface with the active MCTSI. If the MCTSI is not ACT/STBY, CATP runs.
2		Tests control interface with the mate MCTSI. If the MCTSI is not ACT/STBY, NTR runs.	SM:DNLDSC1
3		Tests the TSSR.	SM:DNLDSC1
4		Tests the parity checkers and generators.	SM:DNLDSC2
5		Tests the interrupt registers, DSC parity error, DSC fault and summary scans.	SM:DNLDSC2
6		Tests data links to/from active and mate MCTSI (if mate MCTSI is OOS - CATP runs).	SM:DNLDSC2
LINE UNIT CHANNEL CIRCUIT/ LINE UNIT CHANNEL BOARD	1	Tests control to the channel circuit.	SM:DNCHN (LU1) SM:DNCCHNI (LU2&LU3)
	2	Tests DC portion of the channel circuit - battery feed, cutoff, scan encoding, loop bias, and power up/down. Initializes all GDX crosspoints associated with the channel under test.	SM:DNCHN (LU1) SM:DNCCHN1 (LU2&LU3)
	3	Tests AC portion of the channel circuit - parity bit, CODEC power down, CODEC circuit, hybrid gain, idle channel noise, and CODEC filter balance network. Will complete CATP if either the mate MCTSI or the TTFCOM is OOS.	SM:DNCHN (LU1) SM:DNCCHN1 (LU2 & LU3)
	4	Performs more exhaustive test of CODEC. Will complete CATP if either the mate MCTSI or the TTFCOM is OOS.	SM:DNCHN (LU1) SM:DNCCHN1 (LU2&LU3)
	5	Checks the crosspoints associated with the path to the channel being tested.	SM:DNCHN (LU1) SM:DNCCHN1 (LU2 & LU3)
LINE UNIT COMMON DATA AND CONTROL (LUCOMC) LINE UNIT 1	1	Tests control interface with the MCTSI. Will complete NTR if the MCTSI is not ACT/STBY.	SM:DNCD
	2	Tests the remaining control to registers on the COMDAC. Reports CI errors - does not check interface to the COMDAC subtending circuits.	SM:DNCD
	3	Tests control interface with the mate	SM:DNCD

	4	MCTSI. Will complete NTR if the MCTSI is not ACT/STBY. Verifies operation of the common data circuit. Will complete NTR if the MCTSI is not ACT/STBY.	SM:DNCD
	5	(Demand, automatic, or growth phase). Tests the interface of COMDAC and its subtending circuits.	SM:DNCD
LINE UNIT COMMON DATA AND CONTROL (LUCOMC) LINE UNITS 2, 3, 4	1	Tests control interfaces with MCTSI, peripheral sequencer and maintenance register. Will complete CATP if MCTSI is not ACT/STBY.	SM:DNCCD1
	2	Tests service request controller.	SM:DNCCD1
	3	Tests board - enable multiplexer.	SM:DNCCD1
	4	Tests ASW controller.	SM:DNCCD1
	5	Tests control interface with mate	SM:DNCCD2
	6	MCTSI. Will complete NTR if MCTSI is not ACT/STBY. Tests PIDB interface with active and mate MCTSI. Will complete CATP if MCTSI is not ACT/STBY.	SM:DNCCD2
	7	(Demand, automatic, or growth phase only). Tests interface of COMDAC with its subtending circuits.	SM:DNCCD2
LINE UNIT HIGH-LEVEL SERVICE CIRCUIT (LUHLSC) LINE UNIT 1	1	Verifies basic functional operations - control of power converter, bridge switch, amplifier detect overcurrent, operation of overvoltage protection and output reversal.	SM:DNHLSC1
	2	Test operation of the metallic access buses.	SM:DNHLSC1
	3	(Demand phase only). Generates and detects DC voltages and operation of the voltage flip-flop.	SM:DNHLSC2
	4	(Demand phase only). Tests filtered current crosspoints, reset time constant, ring flip-flop, and ring tip ringing generator.	SM:DNHLSC2
	5	(Demand phase only). Performs DC current generation and detection, using several current levels and the current sensing modes single-ended, differential, and single-ended-times-four.	SM:DNHLSC3
LINE UNIT HIGH-LEVEL SERVICE CIRCUIT (LUHLSC) LINE UNITS 2, 3, 4	1	Tests control interface to HLSC, runs firmware self-tests, and verifies the microcode version for HLSC boards (two or three circuits per board) are not microcoded so the microcode test is skipped.	SM:DNCHLSC1
	2	Tests HLSC output connections through A and B relays.	SM:DNCHLSC1
METALLIC ACCESS (MA)	1	Tests send and receive data with MSUCOM, generates interrupt to MSUCOM, and operation of relay drivers.	SM:DNMAXS

	2 3	Tests MTBs to far-end units. (Demand phase only) Tests the MTBs for <i>SLC</i> [®] 96 carrier RTs.	SM:DNMAXS SM:DNMAXS
	102	Tests the MTBs for proper operations. This phase test and checks the following: <ul style="list-style-type: none"> Relay operations in the MA circuit pack that are connected to the MTB. <p>Connections to the TBCU for integrated subscriber loop carriers.</p>	SM:DNMAXS
	103	Tests ingegrated subscriber loop carrier terminations on each RT connected to the MTB.	SM:DNMAXS
METALLIC ACCESS BUS (MAB)	1	Tests access bus and all connecting relays in MSU shelf.	SM:DNJUNC
MODULAR CONTROLLER TIME SLOT INTER- CHANGER (MCTSI) SMP12/23/ 23CDM(X)	1	Tests static RAM, PICs address, data latches access to all boards of IMP and all equipped memory boards in SMP12/23/23CDM(X). Skips PIC test if either DLI is OOS, and completes CATP.	SM:DNMP1
	2	Processor sanity test, test dormant logic and parity checkers on TN871/ TN1397/ TN1407/ TN1407B/ TN1423(B) in SMP 12/23 ^d .	SM:DNMP2
	3	Tests ROM checksum, write protect, stack protect, address decoder, and microcode number on TN874 in SMP12/23/ 23CDM(X).	SM:DNMP3
	4	Tests error source registers, sanity and I/O timers, reset handling circuits, status registers, bus control register and its shadow register, subunit mismatch error detection, and address decoders on the TN873/ TN1533 in SMP12/23/ 23CDM(X).	SM:DNMP4
	5	Tests the SDLC and DMA circuits, and the DLI interface on the TN872 in SMP12/23/ 23CDM(X). Completes CATP if either DLI is OOS.	SM:DNMP5
	6	Tests the TN875/ TN1527 and all memory boards — row and column parity, hamming and a 2-pass memory test in	SM:DNMP6

	7	SMP12/23/ 23CDM(X). (Demand phase only). Memory tests — a more exhaustive (8-pass) memory test in SMP12/23/ 23CDM(X). Use when suspected marginal memory board, but normal MCTSI is ATP.	SM:DNMP6
	8	Tests the power alarm circuitry on the TN874B and ASC in SMP12/23/ 23CDM(X).	SM:DNMP7
	9	Tests the CPI in SMP12/23/ 23CDM(X). Will not perform test if either DLI or any TMS link is OOS and complete CATP.	SM:DNMP7
	10	Performs update bus test for SMP12/23/ 23CDM(X).	SM:DNMP8
	11	Performs the Subunit access test for SMP12/23/ 23CDM(X).	SM:DNMP8
	90	(Demand phase only.) Tests the TN874. Primary use is during software update when TN874 has been changed on one side of the MCTSI and needs to be tested (including the EPROM microcode number and checksum over the code in the EPROMs).	SM:DNMP8
MODULAR CONTROLLER TIME SLOT INTERCHANGER (MCTSI) SMP20 (SM)	1	Tests the active processor's ability to write and read the mate via the update bus, the interconnections between circuit packs, and the dynamic memory in an SMP20.	SM:DNMC2_1
	2	Verifies sanity for off-line execution, tests mate module controller, interrupt controller, 10-ms timer, ability for mate to be awakened and put to sleep, reset and total hold masks, sanity maze, address and data parity checkers, Shadow Operation Register, internal and external cache, Processor Performance, and cross coupled interrupts/DLI interrupts in SMP20 (UN516/ UN520).	SM:DNMC2_2
	3	Tests the UN517 board, 10-ms timer, stack protect, billing counter, and verifies the microcode number in SMP20.	SM:DNMC2_2
	4	Tests all circuitry on UN516 CS1 board not previously tested in SMP20. Tests ASR, PSRs 1&2, SPR ``A" FF, 8255 Port Hardware, Software and Global memory ESRs, Sanity and I/O timer,	SM:DNMC2_3

		reset handling circuitry, BCR, shadow BCR, and MPF circuitry.	
	5	Tests applications board (UN518), SDLC and DMA circuitry in SMP20.	SM:DNMC2_4
	6	Tests the dynamic memory boards, EDC circuits, write protect circuits, memory refresh circuits, dynamic RAM devices, and memory self-test in SMP20 (TN1374, TN1376, and TN1661).	SM:DNMC2_5
	7	(Demand phase only). Tests dynamic memory boards by doing reads and writes from software in addition to self-tests in SMP20 (TN1374, TN1376, and TN1661).	SM:DNMC2_6
	8	(Demand phase only.) Tests RSM lamp circuitry on UN516 (CS1) board and the ASC in SMP20.	SM:DNMC2_6
	9	Tests CPS HW in SMP20.	SM:DNMC2_5
	10	Tests the OOS processor's ability to access the active side over the update bus, as well as local and mate side pump DMA activity to memory in SMP20.	SM:DNMC2_5
	11	Tests SIB in SMP20.	SM:DNMC2_5
	66	Tests interface to the B TSR circuit on the UN518 - the PIDB interface from the DI, and level 6 interrupt to UN516 in SMP20.	SM:DNMC2_66
MODULAR CONTROLLER TIME SLOT INTERCHANGER (MCTSI) SMP1/12/20/23	31	Tests TSI — MP interface, TSI control circuitry, control RAMs A-E, ADR, and RCV and TMT TSIs, attenuator ROM, E-bit buffer, and TSI data paths.	SM:DNTSI1
	32	Tests TSI — DLI interface. Will complete NTR if either DLI is OOS.	SM:DNTSI2
	51	Tests the SP — mode latch, RAM, ignore RAM, and immediate access RAM.	SM:DNSP
	52	Tests the SP — FIFO, parity check circuits, error source register, interface to programmable interrupt controller on the TN872, and ready time-out error.	SM:DNSP
	61	Tests the DI circuits.	SM:DNDI
	62	(Demand phase only.) Tests the DI parity check from peripheral.	SM:DNDI
	63	Tests the DI fanout on TN1377.	SM:DNDI
	66	(SMP20 only). Tests interface to the B TSR circuit on the UN518 — the PIDB interface from the DI and Level 6 interrupt to UN516.	SM:DNMC2_66
	71	Tests CI — MP interface and CI register access.	SM:DNCI1
	72	Tests the CI — CI transmit/receive sequencers.	SM:DNCI1
	73	(Demand phase only.) CI — tests integrity of PICB paths to/from	SM:DNCI1

	81	peripherals. Verifies SUIB interface of the PI. Fundamental communication and error reporting are verified. The port processor and DARAM are not accessed except to initialize them into a noninterfering configuration.	SM:DNPI1
	82	Verifies access to full range of DARAM from SUIB side of PI. A complete memory test is provided from port processor side of PI. This phase is only used to verify addressing, the ability to reset memory, the write protect of memory, and auto increment of address register when reading or writing data to the DARAM.	SM:DNPI1
	83	Verifies operation of the error correction and detection circuits from SUIB side of DARAM. Also verifies ability to detect and correct single-bit errors and to detect and report multiple bits errors.	SM:DNPI1
	84	Verifies port processor side of the PI. The PI is reset and pumped. Basic communication of PB is verified. If communication looks good, a sanity maze and memory test are run. This phase does not continue its operation if the initial pump fails or if setup of PB from on-line PSUCOM fails. Port processor is in a diagnostic mode.	SM:DNPI1
	85	Verifies packet bus from PI to standby side of PSUCOM. This phase only attempts test if PSUCOM is in standby mode. If PSUCOM is in OOS mode, test reports a CATP. The port processor in the PI is in a diagnostic mode during this phase.	SM:DNPI1
	90	Tests the TN874. Primary use is during software release update when TN874 has been changed on one side of the MCTSI and needs to be tested (including the EPROM microcode number and checksum over the code in the EPROMs).	SM:DNMP8
MCTSI (SM-2000) 5EE9.1	1	Verifies the sanity of the OOS MCTSI for power (410AA/UN589), SMP state, SMP equipage with respect to the database, ability to perform the accesses across the SMP update bus to the I/OS on CORE (UN560), BSN (bus service node) (KBN8/KBN8B), equipped external memory boards (TN1685/TN1806), APC (application controller) (UN539). It also verifies parity checkers and	DNMC4_1

		generators connected to the update bus, interconnections between circuit packs, and SMP error source hierarchy. Tests the external memory and its initialization using onboard self-tests. In the case of the UN560, it tests the internal timer and on -CORE memory & external cache using self-test.	
	2	Tests circuits on CORE & BSN. Verifies power-up reset (exception 0) circuit to and from the OOS SMP, cross coupled processor status signals between the ACTive and OOS SMP, ability to wake-up and stop the OOS processor for the off-line execution. Verifies sanity and mate lockout, short ready timeout, A-FF and loss of clock detector, sanity maze, cache, SPFMR operation, parity checkers and generators on the Local System (LS) bus, conditional suspend timer, processor performance, and CRC checks of the generic firmware. Tests the UN560 external cache maintenance modes, internal timers, lock protocol, loss of synchronization and write posting buffer.	DNMC4_2
	3	Tests the circuits on CORE & BSN. Verifies processor status registers, PICs, to/from mate interrupt signals between the ACT and OOS SMPs, control/display circuits (SN516/UN589), sanity timer, I/O timers, bus error circuits, and MPF circuits for the ACT and OOS SMPs.	DNsmPMC3.out
	4	Tests the circuits on BSN: the interfaces between the LS, RS (remote system) bus and SMP update bus. Verifies bus control circuits and shadow bus control, address, data, control shadow registers, BSN write protects, matchers, shadow circuits, parity checkers and generators on the RS bus, and hardware reset strobe on CORE.	DNsmPMC4.out
	5	Tests the circuits on APC (UN539). Verifies address decoders on APC, stuck at faults on the APC I/Os, the BDL (bootstrapper DLI interface circuit), BTR-DMA (bootstrapper direct memory access) circuits, SUIB (subunit interface bus), and the hardware delay register.	DNsmPMC5.out
MCTSI (SM-2000) 5E11	1	Verifies the sanity of the OOS MCTSI for power 410AA/UN589 ^d , SMP state,	DNsmPMC1.out

	<p>SMP equipage with respect to the database, ability to perform the accesses across the SMP update bus to the I/OS on CORE (UN540/UN540B/UN560), BSN (bus service node) (KBN8/KBN8B), equipped external memory boards (TN1685/TN1806), APC (application controller) (UN538).</p> <p>It verifies parity checkers and generators connected to the update bus, interconnections between circuit packs, and SMP error source hierarchy. Tests the external memory and its initialization using on-board self-tests. In the case of the UN560, it tests the internal timer and on-CORE memory & external cache using self-test.</p>	
2 d	<p>Tests circuits on CORE & BSN. Verifies power-up reset (exception 0) circuit to and from the OOS SMP, cross coupled processor status signals between the ACTive and OOS SMP, ability to wake-up and stop the OOS processor for the off-line execution. Verifies sanity and mate lockout short readytimeout, A_FF and loss of clock detector, sanity maze, cache, SPFMR operation, parity checkers and generators on the Local System (LS) bus, conditional suspend timer, processor performance, and CRC checks of the generic firmware. Tests the UN560 external cache maintenance modes, internal timers, lock protocol, loss of synchronization and write posting buffer.</p>	DNsmPMC2.out
3	<p>Tests the circuits on CORE & BSN. Verifies processor status registers, PICs, to/from mate interrupt signals between the ACT and OOS SMPs, control/display circuits (SN516/UN589), sanity time, I/O timers, bus error circuits, and MPF circuits for the ACT and OOS SMPs.</p>	DNsmPMC3.out
4	<p>Tests the circuits on BSN: the interfaces between the LS, RS (remote system) bus and SMP update bus. Verifies bus control circuits and shadow bus control, address, data, control shadow registers, BSN write protects, matchers, shadow circuits, parity checkers, and generators on the RS bus, and hardware reset strobe on</p>	DNsmPMC4.out

5	<p>CORE. Tests the circuits on APC (UN539). Verifies address decoders on APC struck at faults on the APC I/Os, the BDL (bootstrapper DLI interface circuit), B TSR-DMA (bootstrapper direct memory access) circuits, SU IB (subunit interface bus), and the hardware delay register.</p>	DNsmPMC5.out
6	<p>Tests the circuits on the external memory boards and the circuits associated with on-CORE (UN560) memory. For the TN1806, verifies memory equipage, address decoder and I/O registers, different size memory accesses, refresh circuit, corr-bit counter and threshold circuits, EDC (error detection and correction) circuits, memory self-test logic including the comparators, pattern matchers, system address leads, different self-test modes and its interaction with HW reset, and NMI (non-maskable interrupt). For the UN560, tests the on-CORE memory circuit, scrubbing, and address comparators on dynamic ram controller.</p>	DNsmPMC6.out
7	<p>Tests the circuits on the external memory boards and the circuits associated with on-CORE (UN560) memory. Verifies self-test inhibit circuit, which prevents the running of the memory board self-test on the ACT side. This phase is a demand phase which typically would only be executed on those occasions where the memory self-test is suspect of not finding fault memory boards or when new memory boards are being grown in the unit. For the UN560, tests the above memory functionalities for on-CORE memory.</p>	DNsmPMC7.out
8	<p>Verifies the ASU (alarm status unit) equipage and then tests the RSM sanity and stand-alone indicator logic on the BSN, ASU paddle board (9822DU), and SAM (stand-alone monitor) circuit in the ASU. This is a demand phase.</p>	DNsmPMC7.out
9	<p>Tests the CPI (central processor intervention) circuit on the BSN and, for AWS exchanges, on the CPI paddle board (982YN).</p>	DNsmPMC8.out
10	<p>Tests the SMP update bus circuits on CORE and BSN. Verifies the update bus status signals, parity, ability to</p>	DNsmPMC8.out

	drive address, data, control signals, and various access modes from the OOS to ACTIVE SMP. Tests the operation of mate ready time out & internal global system ready timeout circuits.	
21	Tests local processor of MH (UN538), RAM, and BRIPIT devices. Tests OOS MH interfaces to ACTIVE SMP and ACTIVE MH.	
22	Tests the SPYDER-T (synchronous/asynchronous protocol data formatter) device functions of all equipped MH boards (UN538).	
23	This phase is used with the MCTU4 only. Sets up SMP initialization. For exchanges equipped with a UN538, no tests are performed. Phase stops and indicates ATP. For exchanges with a UN584, tests are performed on the MH. Also reserved for future releases for exchanges equipped with multiple MHS.	
24-32	These phases are not used for MCTU4 testing.	
33	Tests all circuits of TSICOM circuit packs (UM74/UM74/UM74C): TSICOM version check, SMP to TSICOM interfaces via UN539, interrupt hierarchy, clock control register, TSIU4 unit equipage, and for AWS switches, the BIST device test. Also tests TSLIU4 board equipage and all registers on all equipped TSIS (KLU1) boards. Segments 2-9 (2-11 for AWS switches) test the TSICOM. Segments 20-49 test the TSIS boards.	DNts_33
34	Tests each equipped TSIS (KLU1) board. Segments 2-80 test TSIS diagnostic control and ESR functions, TSILS CRC error propagation, and TSIS link equipage and version. Segments 100-149 are BSM and BS based interconnect/cluster tests. Segments 160-169 are device BIST tests. Segment 171 tests the CTS number registers. Segments 300-309 test the active signal from the SMP.	DNts_34
35	Performs more exhaustive functional tests of TSIS (KLU1) boards. Segments 400-409 are board-level BIST tests.	DNts_35
36	Tests TSIS (KLU1) board interfaces: to	DNts_36

	APC (UN539) MCP link in segment 10, to reference clock interface in segments 50-52 (either CM sourced or externally sourced), and to (E)NLI interface in segments 60-69.	
37	Reserved demand phase. Currently performs no tests.	
38	Performs additional TSIS (KLU1) functional unit-level BIST tests, concentrating on inter-TSIS board connections.	DNts_38
39-43	These phases are not used for MCTU4 testing.	
44	Tests all internal circuits of equipped DX (UM73)/XDX (UN553) boards. Included are initial access test of control RAMs, board configuration, and inter-board crosstalk tests (segments 9,10,11), TSICOM to DX/XDX communication tests (segments 20,21), control RAM tests of parity, rd/mod/write masking and memory tests (segs 30-32) and board reset, device BIST tests (segments 40-43).	DNdx_44
45	Tests further the DX/XDX boards individually and in looped back configurations. These tests include TSI-link CRC tests (segment 50), PIDB parity buffer tests (segment 51), fanout-fanin tests (segment 60), PIDB monitoring of active/standby peripheral sides for valid parity (segment 70), and a multi-access board PCM looping test at the DX PIDB outputs (segment 9975).	DNdx_45
46	Demand phases are not available to craft (requires additional test equipment).	
47-65	These phases are not used for MCTU4 testing.	
66	Tests circuits on CORE, BSN, APC, and MH-APC interface. Verifies pump data assembler circuit on APC, billing counter clock input, pump circuits on APC-MH interface, and APC_MH SPYDER interface.	DNMC4_66
67-70	These phases are not used for MCTU4 testing.	
71	Tests parity on PICBs from PUs. Verifies receivers on PICB links. Tests CI-MP interface and CI (UN71/UN71B) register access.	DNCI1
72	Tests CI-CI transmit and receive sequencers (UN71B).	DNCI1
73	CI - tests integrity of control paths to and from all equipped peripherals (UN71/UN71B).	DNCI1

	75-80	These phases are not used for MCTU4 testing.	
	81	Verifies SUIB interface of PI. Verifies fundamental communication and error reporting. Verifies all register functions, excluding memory and error correction.	DNPI1
	82	Verifies access to full range of DARAM from SUIB side of PI. A complete memory test is provided from port processor side of PI. This phase is only used to verify addressing, ability to reset memory, write protect of memory, and auto increment of address register when reading or writing data to DARAM.	DNPI1
	83	Verifies operation of error correction and detection circuits from SUIB side of DARAM. Verifies ability to detect and correct single bit errors and to detect and report multiple bit errors.	DNPI1
	84	Verifies port processor side of PI. The PI is reset and pumped. Verifies basic communication of PB. If communication looks OK, a sanity maze and memory test are run on PI. This phase does not continue its operation if initial pump fails or if setup of PB from on-line PSUCOM fails. Port processor is in diagnostic mode during this phase.	DNPI1
	85	Verifies packet bus from PI to standby side of PSUCOM. This phase only attempts test if PSUCOM is in STBY mode. If PSUCOM is in an OOS mode, test reports CATP. Port processor in PI is in diagnostic mode during this phase.	DNPI1
	86	PI2 tests	
	87	PI2 tests	
	88-89	These phases are not used for MCTU4 testing.	
MSUCOM (SM)	1	Tests the control interface with the MCTSI.	SM:DNMSC
	2	Tests the control interface with the mate MCTSI. SM: DNMMSC (for multimodule office).	SM:DNMMSC SM:DNMSC
	3	Tests the remote interrupt mask and scan registers, interrupt latches and interrupt polarity bit. SM: DNMMSC (for multimodule office).	SM:DNMMSC SM:DNMSC
METALLIC TEST INTERCONNECT BUS (MTIB)	1	Performs end-to-end protocol test of complete interconnect bus.	SM:DNMTIB
	2	Performs step-by-step verification of interconnect bus interfaces to MSU shelves.	SM:DNMTIB
METALLIC TEST	1	Tests send and receive data switch	SM:DNMTAC

INTERCONNECT BUS ACCESS (MTIBAX)	2	with MSUCOM, interrupts, and operation of relay drivers. Tests relay connections to all MTIBs.	SM:DNMTAC
NETWORK LINK INTERFACE (NLI)	1	Phase 1 of the LI diagnostic. Verifies the interface of the LI to the active and mate side Time Slot Interchangers as well as the functionality of various error checks.	DNnli_1
	2	Phase 2 of the LI diagnostic. Verifies the interface of the LI to the ONTC TMS. In the case of an ORM ENLI, the TRCU looparound test is performed.	DNnli_2
PRECISION MEASUREMENT UNIT (PMU)	1	Runs Group D DCTU tests.	SM:DNPMU1
	2	Runs Group E DCTU tests.	SM:DNPMU2
	3	Runs Group F DCTU tests.	SM:DNPMU3
	4	Runs Group G, Series A through I - DCTU tests.	SM:DNPMU4
	5	Runs Group G, Series J through O - DCTU tests.	SM:DNPMU5
PROTOCOL (PROTO)	1	Tests operation of the protocol circuit to a termination circuit.	SM:DNPROTO
PACKET SWITCH UNIT COMMON (PSUCOM)	1	Tests the peripheral interface control bus (PICB) communication between the control interface (CI) and the unified control interface (UCI) chip on the control fanout (CF).	SM:DNUCI
	2	Tests the UCI chip on the CF.	SM:DNUCI
	3	Tests the logical port (LP) of the CFs UCI chip. The switching module processor (SMP) sends messages for the LP, and when the LP sees the messages, performs the required reads and writes (to verify interrupts to the LP).	SM:DNUCI
	4	Tests the CFs LP error source registers and CRC in ROM.	SM:DNPS1
	5	Tests the control interface bus (CIB) between the CF, packet fanout (PF), and the data fanout (DF).	SM:DNPS1
	6	Tests the packet bus (PB) between the CF and the packet interface (PI), and the Packet Interconnect Bus (PIB) between the CF and PF.	SM:DNPS1
	7	(Demand phase for factory and growth testing only). Tests all dual universal asynchronous receiver transmitters (DUARTS) in the CF for unequipped shelves.	SM:DNPS1
	8	(Demand phase for factory and growth testing only). Tests the internal CF interfaces to all unequipped PFs.	SM:DNPS1
	9	(Demand phase for factory and growth testing only). Tests the OOS lamps on equipped and growth CFs, PFs, and DFs. The diagnostic cycles through five times, starting by turning all lamps off. NOTE: This manual test requires a	SM:DNPS1

	11	visual check of the lights. Tests the communication between the CI and the PF via the CF. It also determines that a bad parity error can be detected at a CF and a PF.	SM:DNPS2
	12	Tests the LPs ROM and the ability of the PF to be reset.	SM:DNPS2
	13	Tests the communication between the PF and each of the equipped and growth protocol handlers (PHs).	SM:DNPS2
	14	Tests the packet bus arbiter and the packet bus connections through the PF to each equipped PH.	SM:DNPS2
	15	(Demand phase for factory and growth testing only). Tests the internal communication path on the PF for each unequipped PH.	SM:DNPS2
	16	(Demand phase for factory and growth testing only). Tests the packet bus arbiter and the packet bus connections interval to the PF and the CF.	SM:DNPS2
	21	Tests the communication path between the CI and DF, via the CF. It also determines that a bad parity error can be detected at DF.	SM:DNPS3
	22	Tests the LPs CRC in ROM and the ability of the DF to be reset.	SM:DNPS3
	23	Performs reads and writes on the DFs 8751 bus. This verifies the accessibility of the DF control and error reporting registers.	SM:DNPS3
	24	Provides a memory test for the DFs parity error buffer.	SM:DNPS3
	25	Performs a test on the DFs TSI chip register access and the TSI RAM self-tests are exercised in this phase.	SM:DNPS3
	26	Tests the data paths on the DF such as PHDBs to PHs, PIDBs to TSIU and DPIDBs to ISLU.	SM:DNPS4
	27	(Demand phase for factory and growth testing only). Tests the data paths between the DF and the TSIU (both active and standby) over the PIDBs and DF and ISLU over the DPIDBs. This phase is virtually shipped for the DFs without flex capability.	SM:DNPS4
PACKET SWITCH UNIT PROTOCOL HANDLER (PSUPH)	1	Tests the interface between the active PF and PH under test (TN1081 or TN1367). This includes the control bus (CB), and the CB and PB leads.	SM:DNPH1
	2	Tests the application processor (AP) side of the PH board.	SM:DNPH1
	3	Tests the Input Output processor (IP) side of the PH board.	SM:DNPH1
	4	This phase tests the IP processor side interface with the active and standby	SM:DNPH2

	5	DF over the PHDB. Tests the interfaces between the standby PF and PH under test.	SM:DNPH2
	90	(Demand phase only). Tests the full range of memory using a	SM:DNPH2
	91	high-coverage memory algorithm. (Demand phase only). More exhaustive test of the SPORT chips on the PH circuit pack.	SM:DNPH2
	92	(Demand phase only). This phase runs the same test sequences as phase 2 SUPER sequence except each sequence is run as a separate ``segment'' to provide more data on failures. This phase is expected to be used primarily in the factory where the additional data may help in component-level fault isolation. This phase only applies to a TN1367 PH. Request for it on a TN1081 PH	SM:DNPH2
	93	produces an NTR result. (Demand phase only). This phase runs the same test sequences as phase 3 SUPER sequence except each sequence is run as a separate ``segment'' to provide more data on failures. This phase is expected to be used primarily in the factory where the additional data may help in component-level fault isolation. This phase only applies to a TN1367 PH. Request for it on a TN1081 PH produces an NTR result.	SM:DNPH2
RECORDED ANNOUNCE- MENT FUNCTION (RAF)	1	Tests control interface with active and mate MCTSI. Will CATP if mate MCTSI is OOS.	SM:DNUCI
	2	Tests the internal functions of the UCI chip on the LDSU.	SM:DNUCI
	3	Tests the LP - UCI interface.	SM:DNUCI
	4	Tests LDSU bus interface to DSU2.	SM:DNDSU2
	5	Performs LP tests - interrupt controller, timers, parity, and write protect.	SM:DNDSU2
	6	Tests DSPs, serial data interface, and data to/from LDSU bus.	SM:DNDSU2
	7	Tests RAF memory.	SM:DNDSU2
	8	Performs memory test.	SM:DNDSU2
REMOTE REAL CLOCK (RRCLK)	1	This phase checks CI/CLRT through the DFI - RCLK PICB, the CCB, the microprocessor talk-back and sanity timer. Diagnostics are resident in the R1DFI firmware.	SM:DNRRCLK
	2	This phase runs RCLK diagnostics which are resident in the RCLK firmware. The RAM and EPROM, the control latches, reference phase registers, DCO, clock generator, and interrupts are checked.	SM:DNRRCLK
	3	This phase tests the RCLK energy	SM:DNRRCLK

		detector circuitry with diagnostics resident in the RCLK firmware. It also tests the clock reference from each R1DFI and XCPL wires connecting the RCLKs.	
REVERTIVE PULSING TRANSCEIVER (RVPT)	1	Tests failure alarm circuits on the RVPT board.	SM:DNRPT1
	2	Tests the TSSR of the RVPT pack.	SM:DNRPT1
	3	Tests the parity checker and parity generator of the RVPT.	SM:DNRPT1
	4	Tests the summary scan register on the RVPT.	SM:DNRPT2
	5	Performs run on-board self tests, test overflow bit, and test I/O address and data leads.	SM:DNRPT2
	6	Performs loop test calls through RVPT pack.	SM:DNRPT2
SERVICE ANNOUNCEMENT SYSTEM (SAS)	1	Verifies control interface with active and mate MCTSI. Will CATP if mate MCTSI is OOS.	SM:DNUCI
	2	Verifies all functions of the SASDSC UCI device that are accessible from the MCTSI Module Controller and Time Slot Interchanger.	SM:DNUCI
	3	Tests the SASDSC LP-UCI interface. In Phase 3, the diagnostic code is downloaded to the SASDSC via the PICB.	SM:DNUCI
	4	Tests all the hardware components of the SASDSC.	SM:DNDSC3
	5	Tests SAS memory.	SM:DNDSC3
	6	Verifies programmability of SASMEM flash cards in SAS PSG under test.	SM:DNDSC3
SCAN POINTS (SCAN)	1	Tests the MSU scan pack with exception of actually closing the scan points.	SM:DNSCAN
	2	(Demand phase only). Tests low state of scan points with no backplane connections.	SM:DNSCAN
STSX-1 FACILITY INTERFACE (SFI) (DNU-S)	1	Tests the Internal Control Bus (ICB) from both CCs to the SFI, Peripheral Control Interface (PCI) device, the ability to read and write the general registers, the ability to detect PCIBUS errors, and the operation of each SFI reset mode.	SM2K:DNUSFF11
	2	Tests the TSCs, drivers, encoders, receivers, upstream LOS detectors, upstream spare selection and early loopbacks to the spare and service TMUXs. This phase also contains one task dedicated to duplicating the tests performed under PIST. This allows any PIST failures to be reproduced by OOS diagnostics.	SM2K:DNUSFF11
	3	Tests the upstream and downstream relays, downstream LOS, SLI LOS and	SM2K:DNUSFF11

SUBSCRIBER LOOP CARRIER DIGITAL FACILITY (SDFI)	9	facility loopbacks. Tests the upstream relay, secondary downstream relay, the service TIDB and the facility loopback capability for facilities in the GROW state using an external loopback manually applied to the SLI.	SM2K:DNUSSF11
	1	Tests the CI/CLRT integrity.	SM:DNDFIS1
	2	Tests CCB integrity.	SM:DNDFIS1
	3	Tests μ C integrity.	SM:DNDFIS1
	4	Tests maintenance buffer integrity.	SM:DNDFIS2
	5	Tests LSI exercises I.	SM:DNDFIS3
	6	Tests LSI exercises II.	SM:DNDFIS3
	7	Tests facility alarm clock.	SM:DNDFIS3
	8	Tests TSI integrity.	SM:DNDFIS4
9	Tests signaling and PCM data path test.	SM:DNDFIS4	
TEST ACCESS CIRCUIT (TAC) (SM)	1	Seizes CDI and finds active data side. Interconnect loop outgoing and loop incoming test circuits, normal battery loop open, E&M signaling test. Trunk access network is tested in groups of four. Facility test network is tested.	SM:DNTAC
	2	Tests initialization of the T and A destination register and analog termination segment. The D/A converters are tested; the test reference and detector are tested; and a test for shorts between the maintenance leads is performed.	SM:DNTAC
TRANSMISSION MULTIPLEXER (TMUX) (DNUS)	1	Verifies the ICB interface (physical connection) from the CC to the TMUX. The ICB interface circuits (parity check, start code check, ability to force ASW errors) and the ability of the mate CC to access the TMUX are verified.	SM2K:DNUSTX1
	2	Verifies that all functions within the UCI on the TMUX which are accessible via the CC. This includes the FIFO circuitry, RAM, RAM parity checker/generation, and summary scan/error source/mailbox/ mask registers.	SM2K:DNUSTX1
	3	Verifies the TMUX interface to the UCI. This includes the summary scan interrupts and masks, access to registers and interrupts in the hardware ESR for errors on the TMUX accesses.	SM2K:DNUSTX1
	4	Verifies the microprocessor-related circuitry on the TMUX including byte enables, timers, maskable interrupts and priority encoder, sanity timer, NMI circuitry, bus error circuitry, I/O write protection, RAM write protection, data parity checkers/generators and on-chip	SM2K:DNUSTX1

	9	cache.	
	11	Verifies the RAM on the TMUX. Verifies the individual SONET devices for read/write parity and protocol errors and the connections of the STS-1 level devices to the VT level devices.	SM2K:DNUSTX1 SM2K:DNUSTX2
	12	Devices that have a Built-In Self-Test (BIST) are also run. Verifies the transmission of SONET payloads through the SONET devices on the TMUX. The C1 overhead byte is used first to verify basic connections between devices. Then, different payloads with different signaling modes are looped through both the transmit and receive portions of each device and verified for accuracy.	SM2K:DNUSTX2
	14	Verifies the BPIDB connections to the CD packs and the TDIB connections to the SFI packs. Parity generation/checking is verified for each link.	SM2K:DNUSTX2
TRUNK EQUIPPED NUMBER/ TRUNK UNIT CIRCUIT BOARD	1	Performs signaling test for the trunk circuit under test (for example, SN102, SN103, SN104, SN105, and etc.).	d
	2	Performs transmission tests of the trunk circuit. Verifies correct operation of the CODEC, filter, and transformer. Will complete CATP if either the mate MCTSI or the TTFCOM is OOS.	d
TRANSMISSION TEST FACILITY COMMON (TTFCOM)	1	Tests failure alarm and system maintenance functions associated with the interface board.	SM:DNTFC1
	2	Tests failure alarm and system maintenance functions associated with the processor board.	SM:DNTFC1
	3	Tests failure alarm and system maintenance functions associated with the tone generator DSP board (TN304 or TN304B).	SM:DNTFC1
	4	Tests failure alarm and maintenance functions associated with the measurement DSP board. Will fail if DIP switches on TN304 or TN304B are configured incorrectly.	SM:DNTFC1
	7	Tests parity check circuit on the interface board.	SM:DNTFC1
	8	Tests firmware's ability to generate a summary scan interrupt.	SM:DNTFC2
	9	Tests write/read of the firmware's pseudo TSSR.	SM:DNTFC2
	10	Tests parity generator.	SM:DNTFC2
	11	Tests the reset function and verifies the TTF's reports.	SM:DNTFC2
	12	Tests the TTF tone sources - looped	SM:DNTFC2

		back to the TTF responder. Dummy test - if the CLI is equal to 0. Tests send and receive paths of each responder and port-to-CAROT (PTC) tone detector in the TTF. Dummy test - if the CLI is equal to 0.	SM:DNTFC2
	13		
		Tests AGC function of the PCT tone detector and the operation of the call disposition analysis (CDA) tone detector. Dummy test - if the CLI is equal to 0.	SM:DNTFC2
	14		
		Tests receive path of each Touch-Tone test function in the TTF. Dummy test - if the CLI is equal to 0.	SM:DNTFC2
	15		
UNIVERSAL CONFERENCE CIRCUIT (UCONF)	1	Tests failure alarm circuits.	SM:DNCONF1 (3-port) SM:DN6CONF1 (6-port)
	2	Test the TSSRs.	SM:DNCONF1 (3-port) SM:DN6CONF1 (6-port)
	3	Tests the parity checker.	SM:DNCONF1 (3-port) SM:DN6CONF1 (6-port)
	4	Tests the parity generator.	SM:DNCONF2 (3-port) SM:DN6CONF2 (6-port)
	5	Performs functional tests, using static data sent from the TSI alternate data RAM.	SM:DNCONF2 (3-port) SM:DN6CONF2 (6-port)
UNIVERSAL TONE DECODER (UTD)	1	Tests failure alarm circuits associated with the UTD.	SM:DNCUTD1
	2	Tests the TSSR.	SM:DNCUTD1
	3	Tests the parity checker.	SM:DNCUTD1
	4	Tests summary scan register, tone decoder, and read and write control registers.	SM:DNCUTD2
	5	Performs functional tests with tones from the UTG looped back to the UTD.	SM:DNCUTD2
UNIVERSAL TONE GENERATOR (UTG)	1	Tests the failure alarm circuits.	SM:DNUTG1
	2	Tests the TSSR.	SM:DNUTG1
	3	Tests the parity generator.	SM:DNUTG1

Notes:

- a. The first eight test phases are associated with the ECSU. Phase 9 is a demand phase and is only used when DFI under test is equipped with an ECSU.
- b. Phases 94-99 hold a path up to 15 minutes allowing testing of grid and loop characteristics with special instrumentation or procedures. The HLSC is never used in the hold tests, but the channel battery is used for some phases.
- c. Unless otherwise specified, these descriptions are for both the AMI and ANS[®] U-Cards. The segment numbers for the AMI Cards begins with 4000 and the segment numbers for the ANS[®] Cards begins with 5000.

- d. The PR name for Phases 1 and 2 depends on the type of trunk as follows:
- TRUNK TYPE - PR NAME
 - Loop Start Input - SM:DNLIN
 - Loop Start Output - SM:DNLOUT
 - 2-Wire E & M - SM:DN2EM
 - 4-Wire E & M - SM:DN4EM
 - Toll Loop Start Input - SM:DNTLI
 - Toll Loop Start Output - SM:DNTLO
 - Toll 2-Wire E & M - SM:DNT2EM
 - Toll 4-Wire E & M - SM:DNT4EM
 - Test Trunk - SM:DNTST

5.4 COMMON NETWORK INTERFACE

5.4.1 INTRODUCTION

This section describes the Common Network Interface (CNI) ring in the 5ESS[®]-2000 switch. There are several CNI configurations in each of its two technologies; Small Scale Integration (SSI) and Integrated Ring Node Version 2 (IRN2). The SSI technology has been the standard for all installing rings. The new IRN2 technology was deployed which provides higher reliability and more link terminations. Figure 5.4-1 shows the topology of a typical SSI-based ring

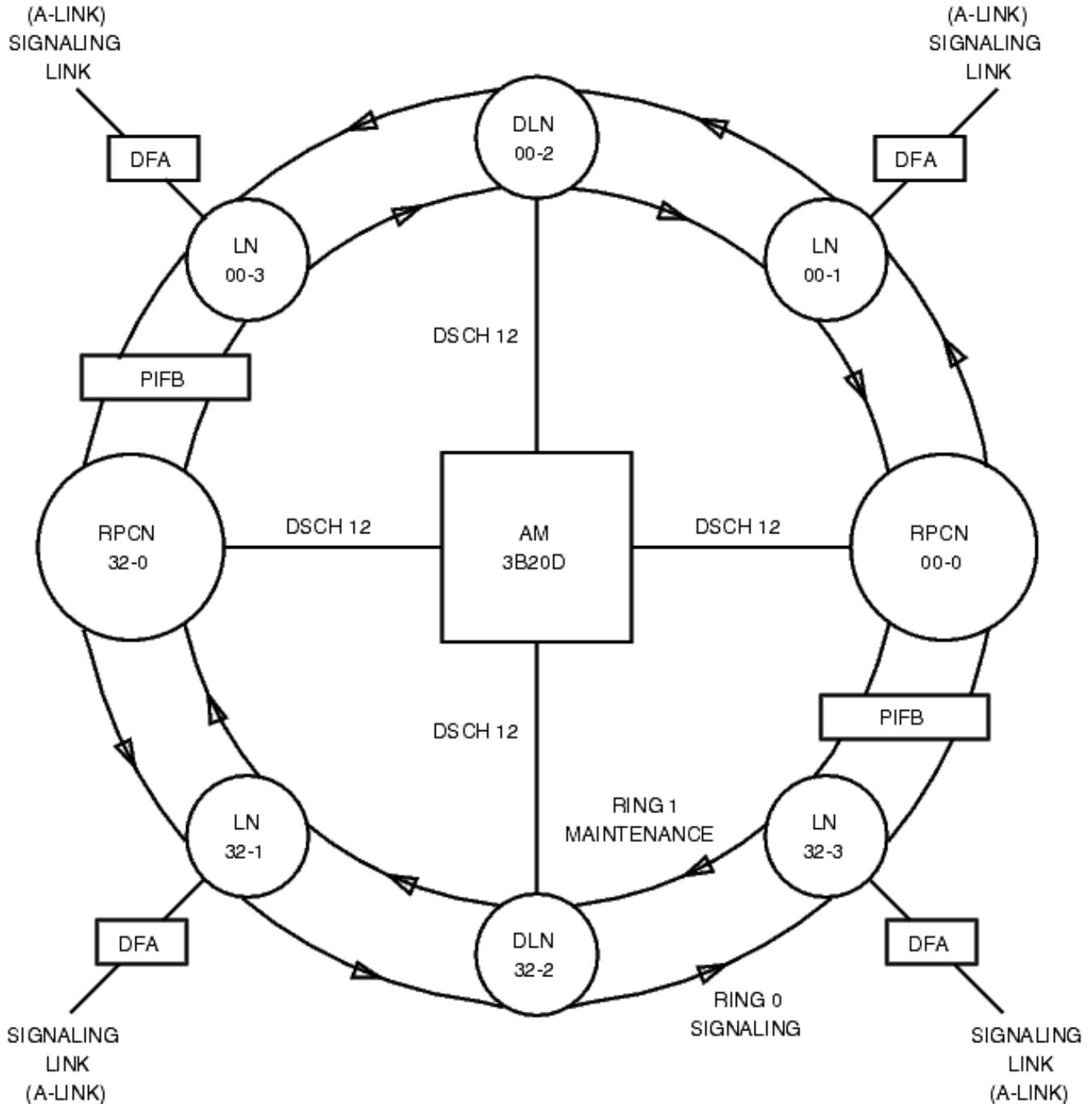


Figure 5.4-1 SSI CNI Configuration

Refer to 235-190-120 for additional information about CNI.

Diagnostic phase descriptions for CNI are provided in Table 5.4-1 .

For diagnostic execution input message and POKE command source information, refer to the following documents:

- 235-105-110, *System Maintenance Requirements and Tools*
- 235-105-210, *Routine Operations and Maintenance Procedures*
- 235-105-220, *Corrective Maintenance Procedures*
- 235-600-700, *Input Message Manual*
- 235-600-750, *Output Message Manual*.

5.4.2 SSI RING NODE CABINET

The Ring Node Cabinet is a single cabinet containing a power panel, control panel, shelves for ring nodes and a fan assembly. There are two types of SSI cabinets. The J3F011C-1 is the original cabinet used for installing offices. The latest cabinet, J3F011C-2, uses the same shelving arrangements but has a different fan unit and alarming capabilities. The following text and figures show the J3F011C-1.

The cabinet is divided into two groups, ring groups 00 and 32, which must be configured identically to provide redundancy.

There are only two types of shelves provided for ring node assignment: J3F011AA and J3F011AC.

There can be up to six shelves equipped, shelves 0-5, configured as follows:

- Shelf positions 0 and 3 always contain a J3F011AA shelf, normally equipped with one Ring Peripheral Controller Node (RPCN) and one Link Node (LN).
- Shelf positions 1 and 4 may contain an optional J3F011AA shelf, equipped to hold one Direct Link Node (DLN) and one LN.
- Shelf positions 2 and 5 may contain an optional J3F011AC shelf, equipped with three LNs numbered from right to left.

Power is fed to each shelf-mounted node through the J5D003AU-02 fuse/filter panel and is controlled by a 495 FA converter provided for each node except for LN5 which is controlled by packs adjacent to LNs 4 and 6.

A 3-fan assembly is mounted at the bottom of the cabinet for equipment ventilation.

Figure 5.4-2 illustrates a fully equipped CNI cabinet and how the shelves are configured with the optional DLN configurations.

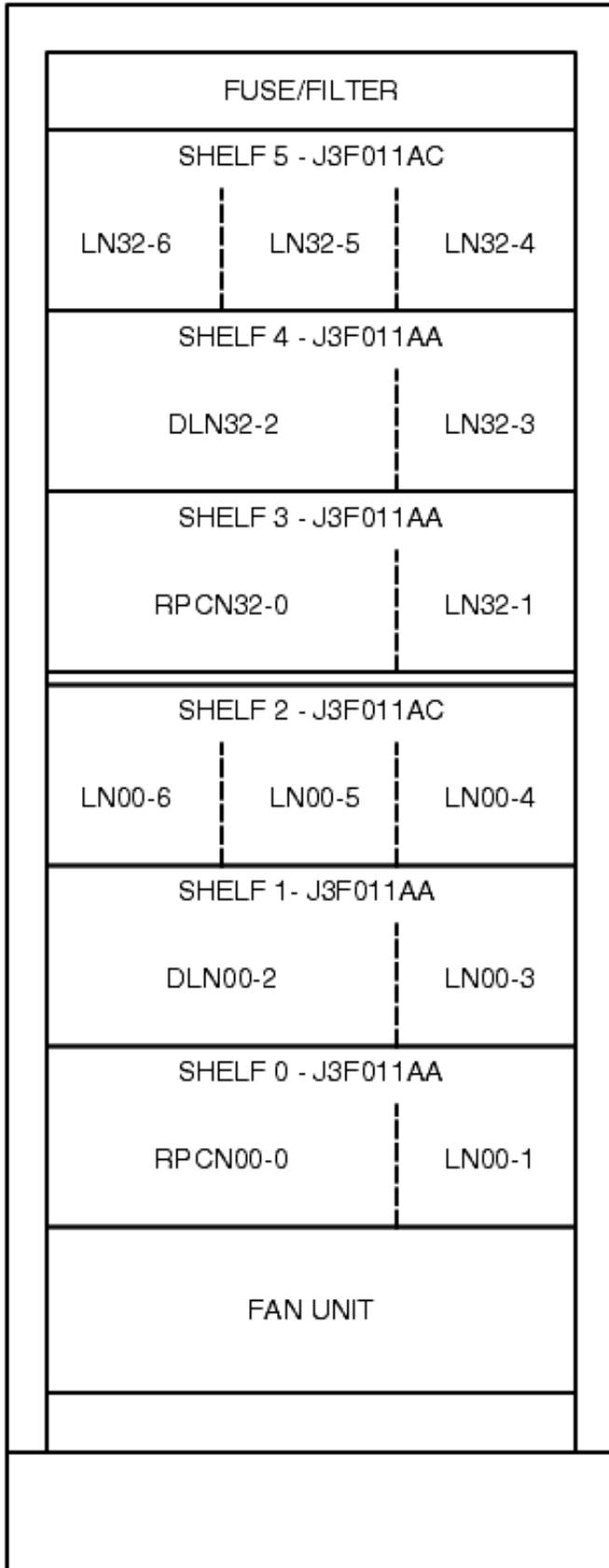


Figure 5.4-2 Fully Equipped SSI CNI Cabinet With Optional DLNs

5.4.3 SSI CNI NODES

Only three kinds of CNI nodes are available for the 5ESS[®]-2000 switch. There is an optional fourth ring processing node to provide for increased CCS capacity requirements. The nodes are described as follows:

- **Ring Peripheral Controller Node (RPCN):** Provides communication between the ring and the Administrative Module (AM). There is an RPCN placed in position 0 of each ring group. Two are always used in the 5ESS[®]-2000 switch CNI application.

The RCPN and its circuit packs are illustrated in Figure 5.4-3 .

- **Link Node (LN):** Provides communication between the CNI ring and the CCS network. The LN data speed can be 4.8 kb/s or 56 kb/s. These can be either encrypted or not encrypted. From 2 to 10 LNs can be used in the 5ESS[®]-2000 switch CNI application.

The LN and its circuit packs are illustrated in Figure 5.4-4 .

- **Interprocess Message Switch User Node (IUN):** This is not recommended for 5ESS[®]-2000 switch. This is an active node on the CNI ring, but it performs no signaling or processing. One use of the IUN, in the 5ESS[®]-2000 switch application, is to electrically hold a place for a future DLN or LN and provide the foundation of common circuitry on which the DLNs or LNs are built. This avoids ring cabling at the time of growth. The IUN may control an adjacent interframe buffer that is used to connect ring nodes across a physical frame boundary; it is generally a temporary filler during growth or reduction periods. The IUN is not illustrated.

- **Direct Link Node (DLN):** The DLN, an optional node, is for 5ESS[®]-2000 switches equipped with Communication Module 2 (CM2). The DLN relieves the AM of some signaling message processing to support greater CCS processing capacity. When DLNs are used, there are always two required for the 5ESS[®]-2000 switch.

The DLN and its circuit packs are illustrated in Figure 5.4-5 .

The 5ESS[®]-2000 switch CCS7 capacity improvement - DLN30 capability was developed. This CCS7 capacity improvement increases the call capacity in the 5ESS[®]-2000 switch by replacing the existing Small Scale Integration (SSI) nodes on the Common Network Interface (CNI) ring with the newer technology Integrated Ring Nodes (IRN)s.

With this capability, the DLN capacity no longer matched the capacity of the switch. Therefore a new DLN, DLN30 was developed. The DLN30 includes a *Motorola*[®] MC68030[™] processor and the integrated ring node.

The capability requires a DLN-AP30 replacement for a DLN-AP and a conversion from an SSI based technology to IRN technology for all the CNI nodes - DLNs, LNs and RPCNs. It also requires a new IRN eight-node third shelf.

The following DLN30 hardware changes are required to support this feature:

- An AP30 processor board with the *Motorola*[®] MC68030[™] chip. It has 16 MB of fixed resident memory that cannot be reengineered.
- A single IRN2 circuit pack which has the current NP, RI0 and RI1 board functions.
- A 3B20D Interface (3BI) board.
- A Duplex Dual Serial Bus Selector (DDSBS) board.

018	POWER	495FA
026	INTERFACE BUFFER	TN915
034	NODE PROCESSOR	TN922
058	RING INTERFACE 0	UN122C
068	RING INTERFACE 1	UN123B
078	3B20D COMPUTER INTERFACE	TN914
086	DUPLEX DUAL SERIAL BUS SELECTOR	TN69B

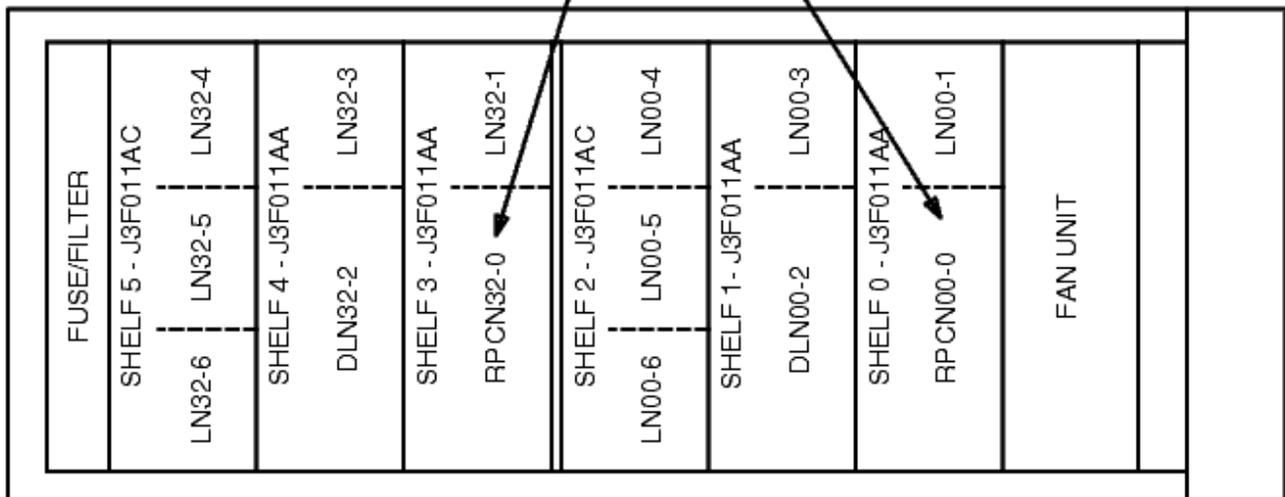


Figure 5.4-3 SSI Ring Peripheral Controller Node

178	POWER	495FA
162		
152	RING INTERFACE 1	UN123B
142	RING INTERFACE 0	UN122C
134	LINK INTERFACE	TN916 OR TN917
118	NODE PROCESSOR	TN922

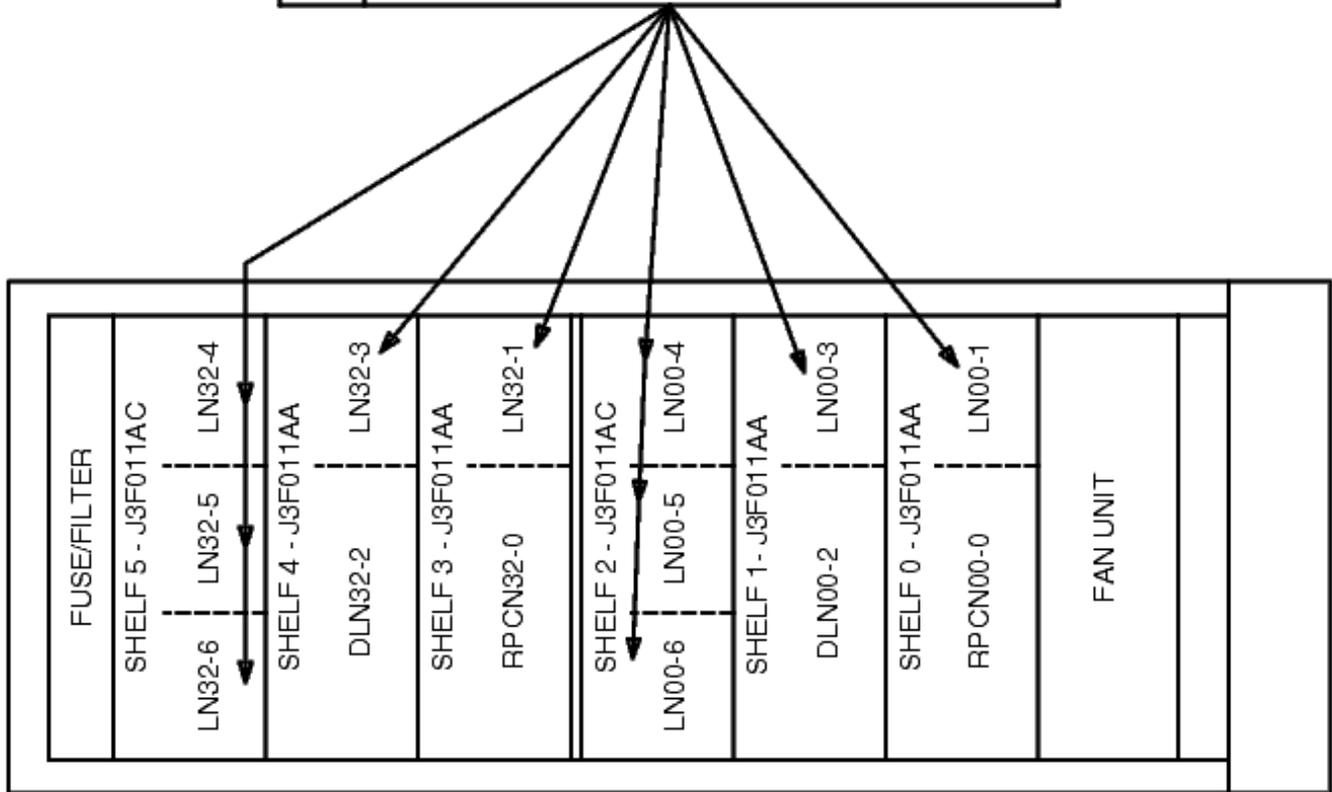


Figure 5.4-4 SSI Link Node

086	DUPLEX DUAL SERIAL BUS SELECTOR	TN69B
078	3B20D COMPUTER INTERFACE	TN914
068	RING INTERFACE 1	UN123B
058	RING INTERFACE 0	UN122C
042	ATTACHED PROCESSOR	TN134O
034	NODE PROCESSOR	TN922
026	INTERFRAME BUFFER*	TN918
018	POWER	495FA

* NOT PRESENT IN ALL RN CABINET CONFIGURATIONS

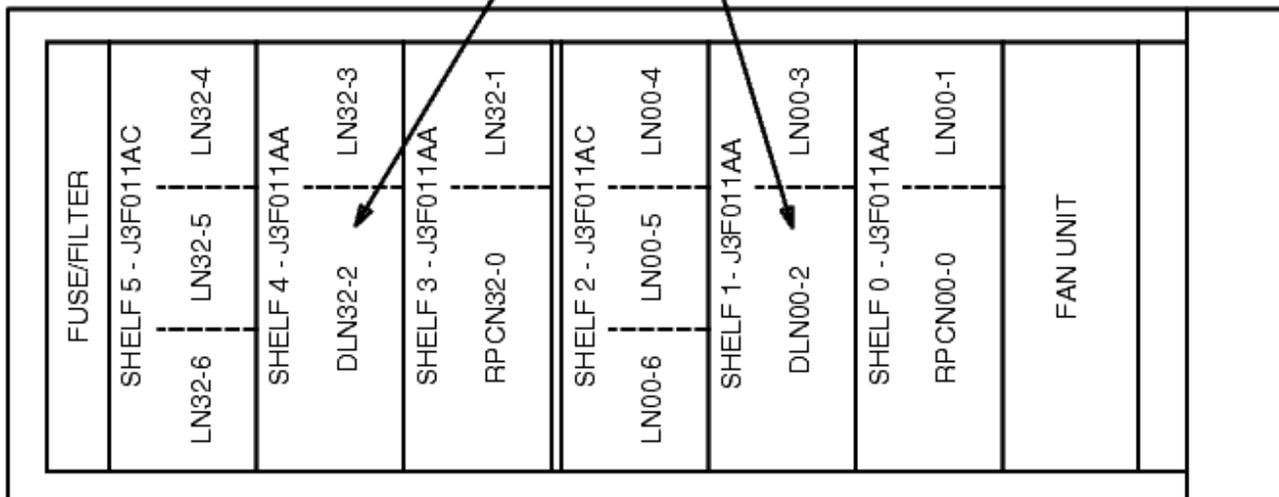


Figure 5.4-5 SSI Direct Link Node

5.4.4 IRN2 RING NODE CABINET

The ring node cabinet is a single cabinet containing a power panel, control panel, shelves for ring nodes and fan assembly. The IRN2 ring is placed in the J3F011C-2 frame and is only available to offices.

The cabinet is divided into two halves, each containing three groups. Groups 01, 01 and 02 in one half, and groups 32, 33 and 34 in the other half. These two halves must be equipped identically for redundancy.

There are two types of shelves provided for this cabinet; J3F011GC and J3F011GD. The cabinet accommodates up to six shelves and is configured as follows:

- Shelf positions 0 and 4 always contain J3F011GD. This shelf must have the RPCN and LN4 installed. It may have up to three Link Nodes (LNs) and one Direct Link Node (DLN).
- Shelf positions 1, 2, 5 and 6 have the J3F011GC shelf. This shelf is optional and is needed only when the existing J3F011GD has been filled. The J3F011GC shelf can contain up to eight LNs.

The Modular Fuse Filter Unit (MFFU) provides power to the cabinet and to the 410AA Power Converters. There are two power converters per shelf. On the J3F011GD the left-hand converter powers the RPCN and LN-1, while the right converter powers DLN2, LN3 and LN4. For the J3F011GC shelf, the power is split down the middle so that the left-hand converter powers nodes LN1 through LN4 and the right one powers LN5 through LN8. Figure 5.4-6 shows the J3F011GC shelf layout and Figure 5.4-7 shows the J3F011GD shelf layout.

A six-fan assembly is mounted in the middle of the cabinet with three fans pulling air up for the lower three shelves and three fans pushing air up for the upper three shelves. Figure 5.4-8 illustrates a fully equipped IRN2 CNI cabinet and how the shelves are arranged.

178	POWER	410AA	
170	IFB	TN1803	
162	LI	TN916	LN-4
152	IRN2	UN304B	
144	LI	TN916	LN-3
126	IRN2	UN304B	DLN
118	DDSBS	TN69B	
110	3BI	TN914	LN-1
102	AP	TN1630B	
			LN-1
084	IRN2	UN304B	
076	LI	TN916	LN-1
058	IRN2	UN304B	LN-1
050	DDSBS	TN69B	
042	3BI	TN914	RPCN
024	IRN2	UN304B	RPCN
016	IFB	TN1803	
008	POWER	410AA	

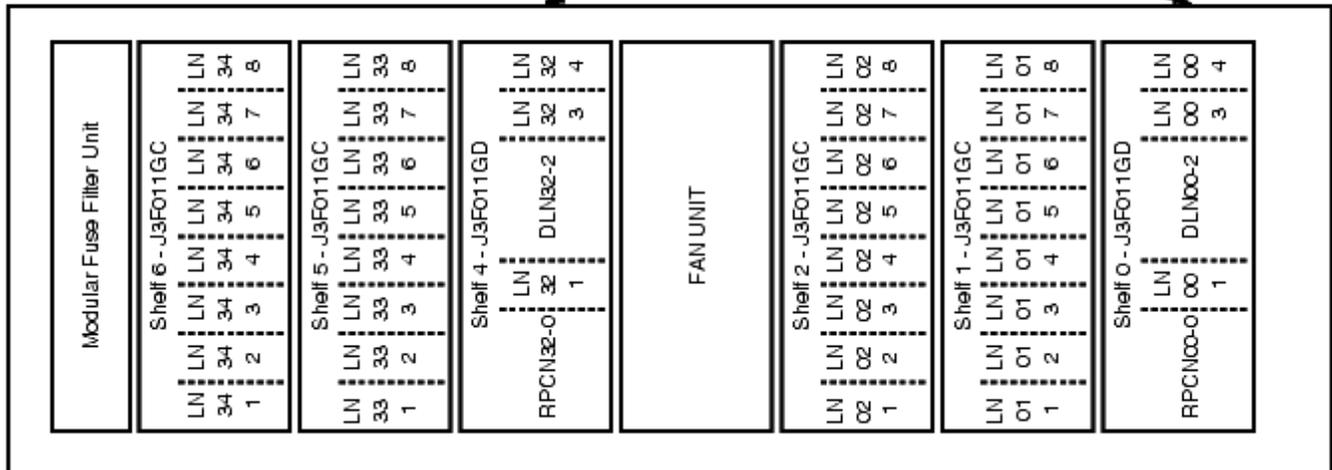


Figure 5.4-7 IRN2 J3F011GD Shelf Unit

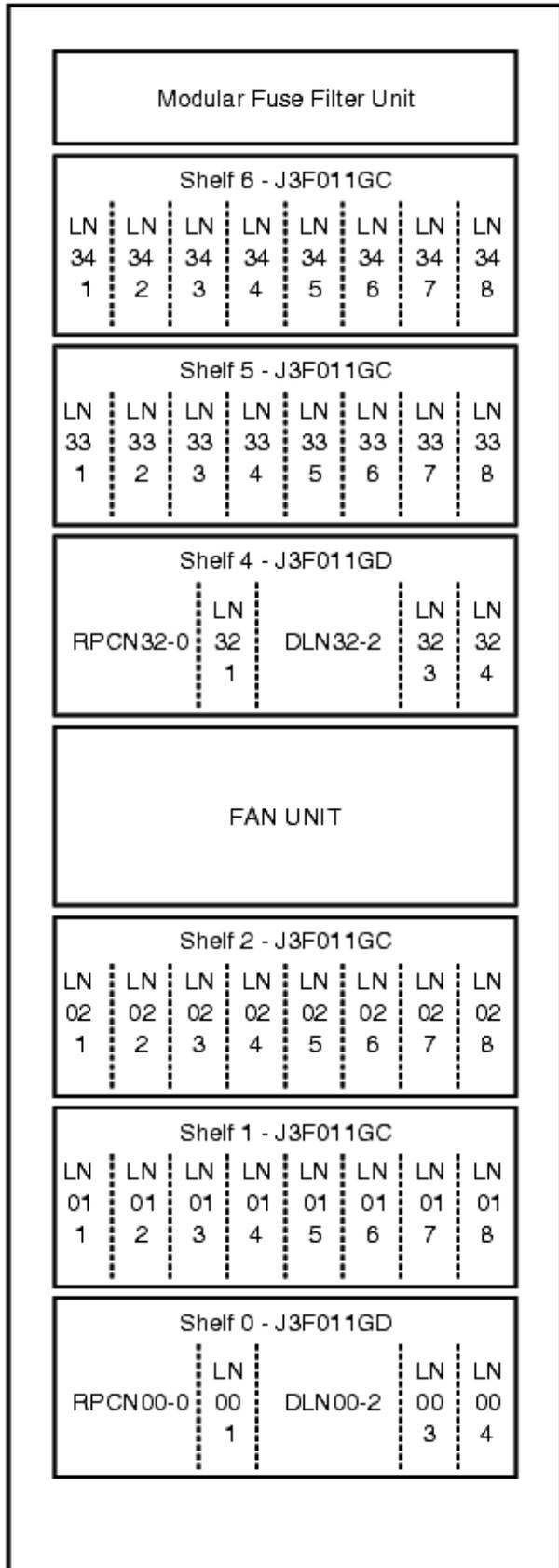


Figure 5.4-8 Fully Equipped IRN2 CNI Cabinet

5.4.5 IRN2 CNI NODES

There are four types of nodes available on the CNI ring. The nodes are described as follows:

- **Ring Peripheral Controller Node (RPCN):** There are only two RPCNs per CNI ring. These nodes provide the communication interface to the AM processor through the Duplex Dual Serial Bus Selector (DDSBS).
- **Link Node (LN):** The LNs provide communications to the CCS7 signaling. The IRN2 ring uses only TN916 CCS7 nonencrypted links, of which it can support 19 pair.
- **IMS User Node (IUN):** The IUN is used only as a "place holder" in a live ring to prevent recabling when added signaling capacity is expected in the future. In the SSI ring this was needed because of DLN growth. For IRN2 rings it is only allowed in the LN-4 position on the J3F011GD shelf and only for rings which converted from SSI to IRN2.
- **Direct Link Node (DLN):** The DLN is used to handle CCS7 call processing instead of the AM. The DLN can handle several times the amount of traffic of the AM thus increasing office capacity. There are two DLNs (also known as DLN30s) in a ring. They are required if more than two pair of signaling links are to be installed but cannot be equipped with just one pair.

Table 5.4-1 CNI Diagnostic Phase Descriptions

PHASE	PHASE DESCRIPTION	PACKS TESTED
SSI LN Node Diagnostic Phases		
01	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC0. Phase 1 also tests that a message can be relayed from the BISO node to the EISO node via the isolated segment over ring 0, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibits the proper data storage capacity.	UN122 UN123 TN915/TN918
02	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC1. Phase 2 also tests that a message can be relayed from the EISO node to the BISO node via the isolated segment over ring 1, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibits the proper data storage capacity.	UN122 UN123 TN915/TN918
10	Tests part of both RAC circuit packs and the RAC to the NP interface. It also partially tests the interface between both RACs and the ring bus.	UN122 UN123 TN922
11	Makes additional tests of the interface between both RACs and the ring bus. Checks the capacity of the interframe buffers associated with the node under test.	UN122 UN123 TN922
12	This phase verifies that RAC0 can detect bad parity in a ring message.	UN122 UN123 TN915/TN918
13	This phase verifies that RAC1 can detect bad parity in a ring message.	UN122 UN123 TN915/TN918
20	Tests NP RAM memory.	TN922
23	This phase tests the NP parity checker and generator circuitry.	TN922
24	This phase tests the NP programmable master and slave interrupt controllers and associated circuitry.	TN922
26	This phase tests the NP programmable Direct Access Memory Controllers and associated circuitry.	TN922
27	This phase tests the NP programmable interval timer circuitry.	TN922
40	Tests hardware in the Line Interface (LI) board or the LI-NP interface.	TN922 TN916/TN917

41	This phase tests the sanity of the microprocessor and the ROM. (Phase 41 will sometimes fail when the node is looped back.)	TN922 TN916/TN917
47	Tests the 2.4 and 4.8 data service units along with their respective VFLA or DSA units. The CCS7 will ATP by default.	TN922 TN916/TN917 DSA/DSU
48	This phase ensures that the firmware and hardware on the LI board will function as a whole.	TN922 TN916/TN917 DSA/DSU
SSI RPC Node Diagnostic Phases		
01	Tests that a message can be relayed from the BISO node to the EISO node via the isolated segment over ring 0. Phase 1 also tests that any interframe buffers and all SSI boards in the isolated segment are equipped in accordance with ECD data, and that any interframe buffers in the isolated segment exhibit the proper data storage capacity.	UN122 UN123 TN915
02	Tests that a message can be relayed from the EISO node to the BISO node via the isolated segment over ring 1. Phase 2 also tests that any interframe buffers and all SSI boards in the isolated segment are equipped in accordance with ECD data, and that any interframe buffers in the isolated segment exhibit the proper data storage capacity.	UN122 UN123 TN915
10	Tests the interface between the Dual Serial Channel (DSCH) and the Duplex Dual Serial Bus Selector (DDSBS).	TN69B UN09 (on 3B)
11	Tests between the DDSBS and the 3BI.	TN914, TN69B
12	Verifies that RAC0 can detect bad parity in a ring message.	TN914, TN922
13	Verifies that RAC1 can detect bad parity in a ring message.	TN914, TN922
14	Off-line CU to DDSBS tests (Demand phase only)	TN69B UN09 (off-line 3B)
20	Tests the associated NP RAM memory, NP parity checker, and generator circuitry.	TN922
23	This phase tests the NP parity checker and generator circuitry.	TN922
24	This phase tests the NP programmable master and slave interrupt controllers and circuitry.	TN922
26	This phase tests the NP programmable Direct Memory Access Controller and associated circuitry.	TN922
27	This phase tests the NP programmable interval timer circuitry.	TN922
30	Tests part of both RAC circuits and the RAC to the NP interface. Partially tests the interface between both RACs and the ring bus.	UN122 UN123 TN922
31	Makes additional tests of interface between both RACs and the ring bus.	UN122 UN123 TN922
32	This phase verifies that RAC0 can detect bad parity in a ring message.	UN122 UN123 TN915
33	This phase verifies that RAC1 can detect bad parity in a ring message.	UN122 UN123 TN915
SSI DLN Node Diagnostic Phases		
01	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC0. Phase 1 also tests that a message can be relayed from the BISO node to the EISO node via the isolated segment over ring 0, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibits the proper data storage capacity.	UN122 UN123 TN918
02	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC1. Phase 2 also tests that a message can be relayed from the EISO node to the BISO node via the isolated segment over ring 1, and that any interface buffers in the isolated segment are equipped in accordance with ECD data and exhibits proper data storage capacity.	UN122 UN123 TN918
10	Tests part of both RAC service packs and the RAC to the NP interface. It also partially tests the interface between both RACs and the ring bus.	UN122 UN123 TN922
11	Makes additional tests of the interface between both RACs and the ring bus. Checks	UN122

	the capacity of the interframe buffers associated with the node under test.	UN123 TN922
12	This phase verifies that RAC0 can detect bad parity in a ring message.	UN122 UN123 TN918
13	This phase verifies that RAC1 can detect bad parity in a ring message.	UN122 UN123 TN918
20	Tests the NP RAM memory.	TN922
23	This phase tests the NP parity checker and generator circuitry.	TN922
24	This phase tests the NP programmable master and slave interrupt controllers and associated circuitry.	TN922
26	This phase tests the NP programmable Direct Memory Access Controllers and associated circuitry.	TN922
27	This phase tests the NP programmable interval timer circuitry.	TN922
30	Tests interface between the DSCH and the DDSBS.	TN69B UN09 (on 3B)
31	Tests interface between the DDSBS and the 3BI.	TN914 TN69B
32	Test ability of NP to go "insane" and set the "Interrupt Request Flag" when the 3BI has an error.	TN914 TN922 UN122 UN123
33	Tests the interface between the 3BI and the NP	TN914 TN922
34	Off-line CU to DDSBS tests. (Demand phase only)	TN69B UN09 (off-line 3B)
35	Cooperates with the 3B20D/3B21D driver to test the DMA capability via the 3BI.	TN914 TN922
40	Tests the AP Dual Port Memory from the NP side.	TN1340
41	Tests the AP and sends the results back to the 3B20D/3B21D computer.	TN1340
42	Tests interface between DMA and 3BI.	TN922 TN1340
IRN2 RPC Node Diagnostic Phases		
01	Test that a message can be relayed from the BISO node to the EISO node via the isolated segment over ring 0. Phase 1 also tests that any interframe buffers and all IRN boards in the isolated segment are equipped in accordance with ECD data, and that any interframe buffers in the isolated segment exhibit the proper data storage capacity.	UN304B TN1803
02	Tests that a message can be relayed from the EISO node to the BISO node via the isolated segment over ring 1. Phase 2 also tests that any interframe buffers and all IRN boards in the isolated segment are equipped in accordance with ECD data, and that any interframe buffers in the isolated segment exhibit the proper data storage capacity.	UN304B TN1803
10	Tests the interface between the Dual Serial Channel (DSCH) and the DDSBS.	TN69B UN09 (on 3B)
11	Tests interface between the DDSBS and the 3BI.	TN914 TN69B
12	Verifies that RAC0 can detect bad parity in a ring message.	TN914 UN304B
13	Verifies that RAC1 can detect bad parity in a ring message.	TN914 UN304B
14	Off-line CU to DDSBS tests. (Demand phase only)	TTN69B UN09 (off-line 3B)
20	Tests the NP RAM memory, NP parity checker, and generator circuitry.	UN 304B
30	Tests part of both RAC circuits, and the RAC to the NP interface. Partially tests	UN304B

	interface between both RACs and the ring bus.	
32	This phase verifies that RAC0 can detect bad parity in a ring message.	UN304B TN1803
33	This phase verifies that RAC1 can detect bad parity in a ring message	UN304B TN1803
IRN2 LN Node Diagnostic Phases		
01	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC0. Phase 1 also tests that a message can be relayed from the BISO node to the EISO node via the isolated segment over ring 0, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibits the proper data storage capacity.	UN304B TN1803
02	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC1. Phase 2 also tests that a message can be relayed from the EISO node to the BISO node via the isolated segment over ring 1, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibits the proper data storage capacity.	UN304B TN1803
10	Tests part of both RACs, the RAC to the NP interface, and the interface between both RACs and the ring bus. Checks the capacity of the interframe buffers associated with node under test.	UN304B
12	This phase verifies that RAC0 can detect bad parity in a ring message.	UN304B TN1803
13	This phase verifies that RAC1 can detect bad parity in a ring message.	UN304B TN1803
20	Tests the NP RAM memory, NP parity checker and generator circuitry.	UN304B
40	Tests hardware in the LI board or the LI-NP interface.	TN916 UN304B
41	This phase tests the sanity of the microprocessor and the ROM.	TN916 UN304B
47	The CCS7 will ATP by default.	None
48	This phase insures that the firmware and the hardware on the LI board will function as a whole.	UN304B TN916 DSA/DSU
IRN2 DLN (DLN30) Node Diagnostic Phases		
01	Tests that each node in the isolated segment is able to set and clear its data selector via hardware commands at RAC0. Phase 1 also tests that a message can be relayed from the BISO node to the EISO node via the isolated segment over ring 0, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibit the proper data storage capacity.	UN304B
02	Tests that each node in the isolated segment is able to set and clear data selector via hardware commands at RAC1. Phase 2 also tests that a message can be relayed from the EISO node to the BISO node via the isolated segment over ring 1, and that any interframe buffers in the isolated segment are equipped in accordance with ECD data and exhibit the proper data storage capacity.	UN304B
10	Tests part of both RACs, the RAC to the IRN2 interface, and the interface between both RACs and the ring bus.	UN304B
12	This phase verifies that RAC0 can detect bad parity in a ring message.	UN304B
13	This phase verifies that RAC1 can detect bad parity in a ring message.	UN304B
20	Tests the IRN2 RAM memory, IRN2 parity checker and generator circuitry.	UN304B
30	Tests interface between the DSCH and the DDSBS.	TN69B UN09 (on 3B)
31	Tests interface between the DDSBS and the 3BI.	TN914 TN69B
32	Tests ability of NP to go "insane" and set the "Interrupt Request Flag" when the 3BI has an error.	TN914 UN304B
33	Tests the interface between the 3BI and the NP.	TN914 UN304B
34	Off-line CU to DDSBS tests. (Demand phase only)	TN69B UN09 (off-line 3B)

35	Cooperates with the 3B20D/3B21D driver to test the DMA capability via the 3BI.	TN914 UN304B
40	Tests the shared static memory in the AP30 from the IRN2 side.	TN1630B
41	Tests the shared static memory from the AP30 side, the local parity error snapshot register, and the main 16 Megabytes of DRAM on the AP30.	TN1630B
42	Tests the DMA capability via the 3BI. The DMA is from the 3B20D/3B21D to/from the AP Dual Port Memory (DPM).	TN1630B
43	Tests the 4 D-channel data links on the AP30. (Demand phase only)	TN1630B

6. POWER DISTRIBUTION

6.1 DESCRIPTION

The Power Control Fuse Distribution (PCFD) provides primary power distribution (-48V DC to all cabinets in the 5ESS[®]-2000 switch) from whatever source is established.

Secondary distribution (-48V DC to individual units within cabinets) is provided through cabinet fuse and filter panels to the various units.

Circuits within the units convert the input voltage to the various levels required for system operations (tertiary distribution).

It is a general practice to supply duplicated system components within the switch with power from separate buses to establish independent power supplies for operating reliability.

Secondary power distribution in the Administration Module (AM) is unlike that in the Communication Module (CM) and Switching Module (SM). The AM contains a Power Distribution Unit (PDU) for extra control and protection, while the CM and SM filter and fuse panels distribute the fused power routinely.

Figure 6-1 illustrates the PCFD power distribution.

CAUTION: When performing maintenance procedures on, or affected by, the PCFD, maintenance personnel MUST be alert to any effects on switch operation integrity. Do not attempt "short cut" maintenance procedures. Refer to documents that provide detailed procedures for routine maintenance (235-105-210) and corrective maintenance (235-105-220).

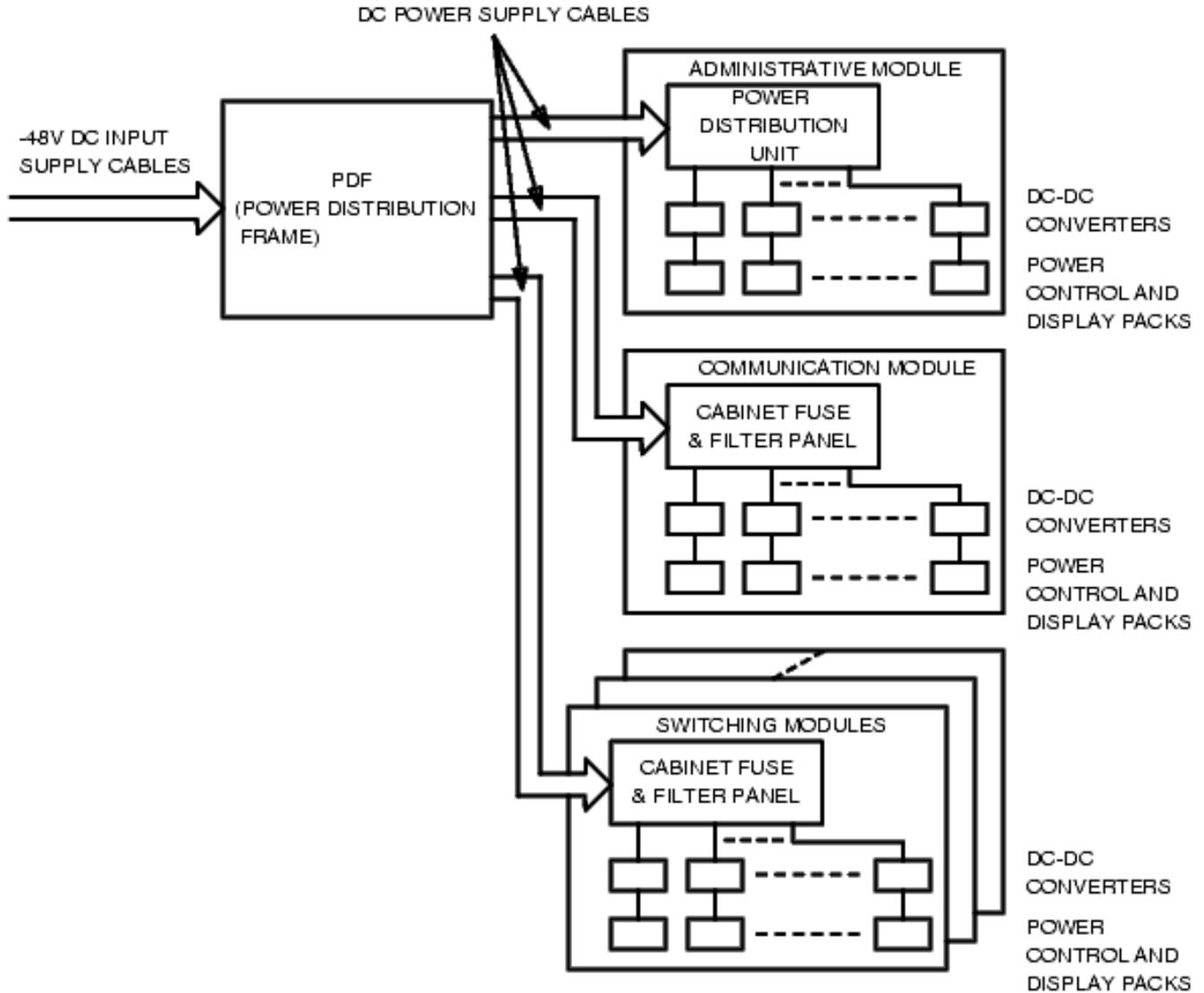


Figure 6-1 PCFD or GPDF Power Distribution

6.2 POWER DISTRIBUTION FRAME - J86334E-1

The Power Distribution Frame (PCFD) provides redundant, protected direct current to power the switch. The PCFD receives its power from two to four independent buses terminated at the back of PCFD frame.

The PCFD contains a control panel and from one to four distribution panels. The distribution panels may consist of any combination of fuse panels (pop-up type or high-current type).

Figure 6-2 illustrates a typical PCFD and its components.

The control panel contains an alarm circuit module, two alarm circuit module protection fuses, a charge circuit protection fuse and a capacitor charge circuit with a charging probe.

A pop-up fuse panel has 48 load fuse positions and associated alarm-indicating fuses and an energy storage capacitor bank (three capacitors per bus) to minimize voltage transients after load fuse operations.

Figure 6-2 illustrates the Control Panel and a pop-up fuse panel.

When a blown fuse is to be replaced, the power supply capacitor associated with the blown fuse must be charged before a new fuse is installed. Charging the capacitor prevents a sudden high-current surge which may blow the new fuse immediately.

A high-current fuse panel has eight load fuse positions and associated alarm indicating fuses (four load and four alarm indicating per bus), and a filter capacity bank (three capacitors per bus).

Figure 6-3 illustrates the high-current fuse panel.

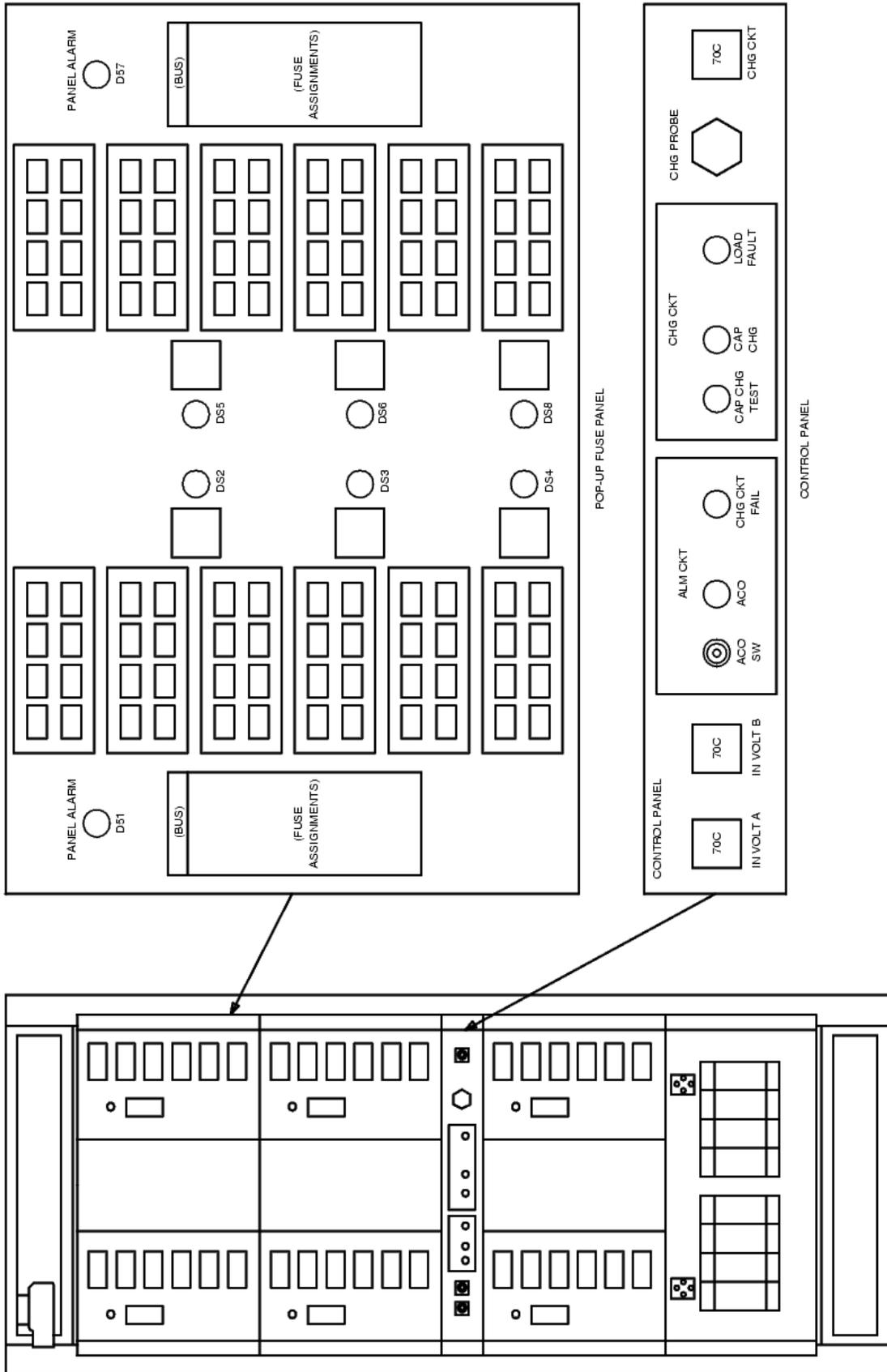


Figure 6-2 Power Distribution Frame

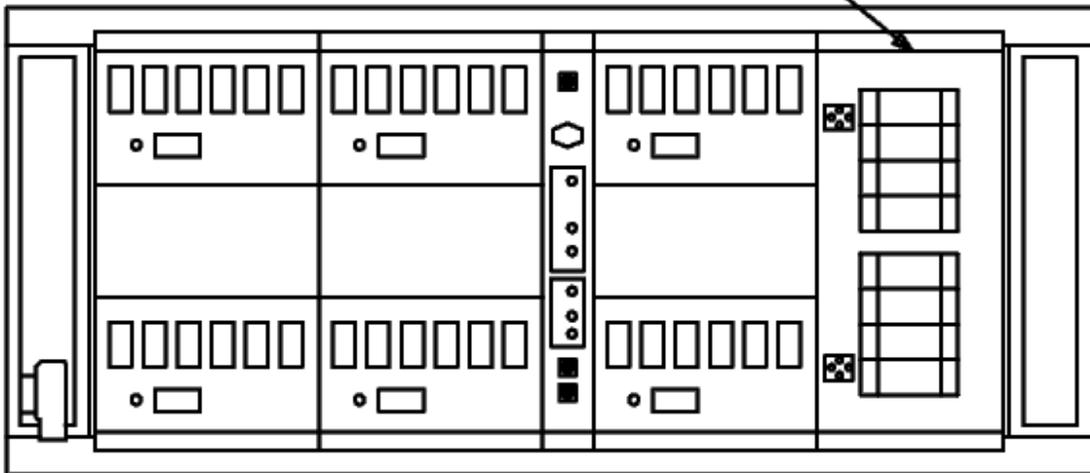
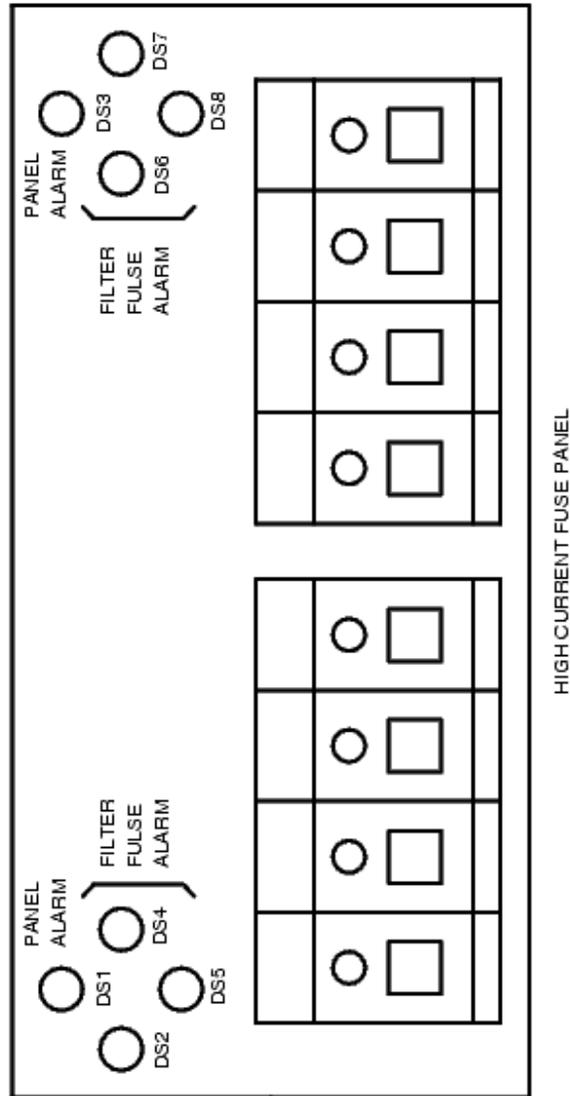


Figure 6-3 High-Current Fuse Panel

6.3 GLOBAL POWER DISTRIBUTION FRAME - J86334E-1

The Global Power Distribution Frame (GPDF) provides redundant, protected direct current to power the 5ESS[®]-2000 switch). The GPDF receives its power from two to eight independent buses that are terminated at the back of the GPDF frame.

Figure 6-4 illustrates a typical GPDF and its components.

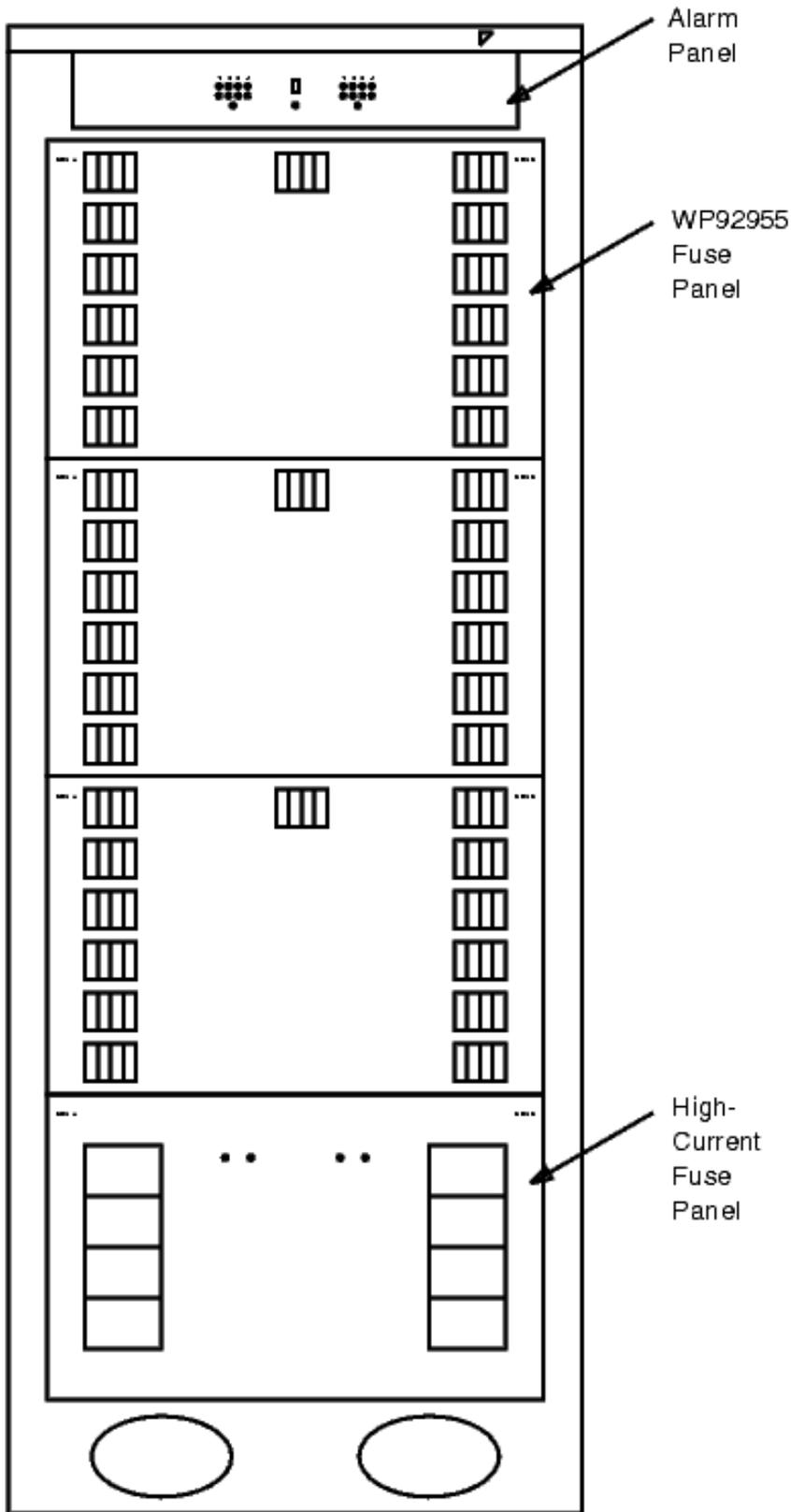
A WP92955 (ED83133-30) fuse panel has 48 load fuse positions and associated alarm-indicating LEDs and an energy-storage capacitor bank (two capacitors per bus) to minimize voltage transients after load-fuse operations.

Figure 6-5 shows the alarm panel and WP92955 fuse panel.

Note that when a blown fuse has to be replaced that the power supply capacitor associated with the blown fuse does **not** have to be charged before a new fuse is installed. The GPDF and WP92955 fuses are specially designed to withstand inrush currents.

A high-current fuse panel has eight load fuse positions and associated alarm-indicating fuses (four load and four alarm indicating per bus) and a filter capacity bank (two capacitors per bus.)

Figure 6-6 shows the high-current fuse panel.



tpa 831109/01

Figure 6-4 Typical Global Power Distribution Frame

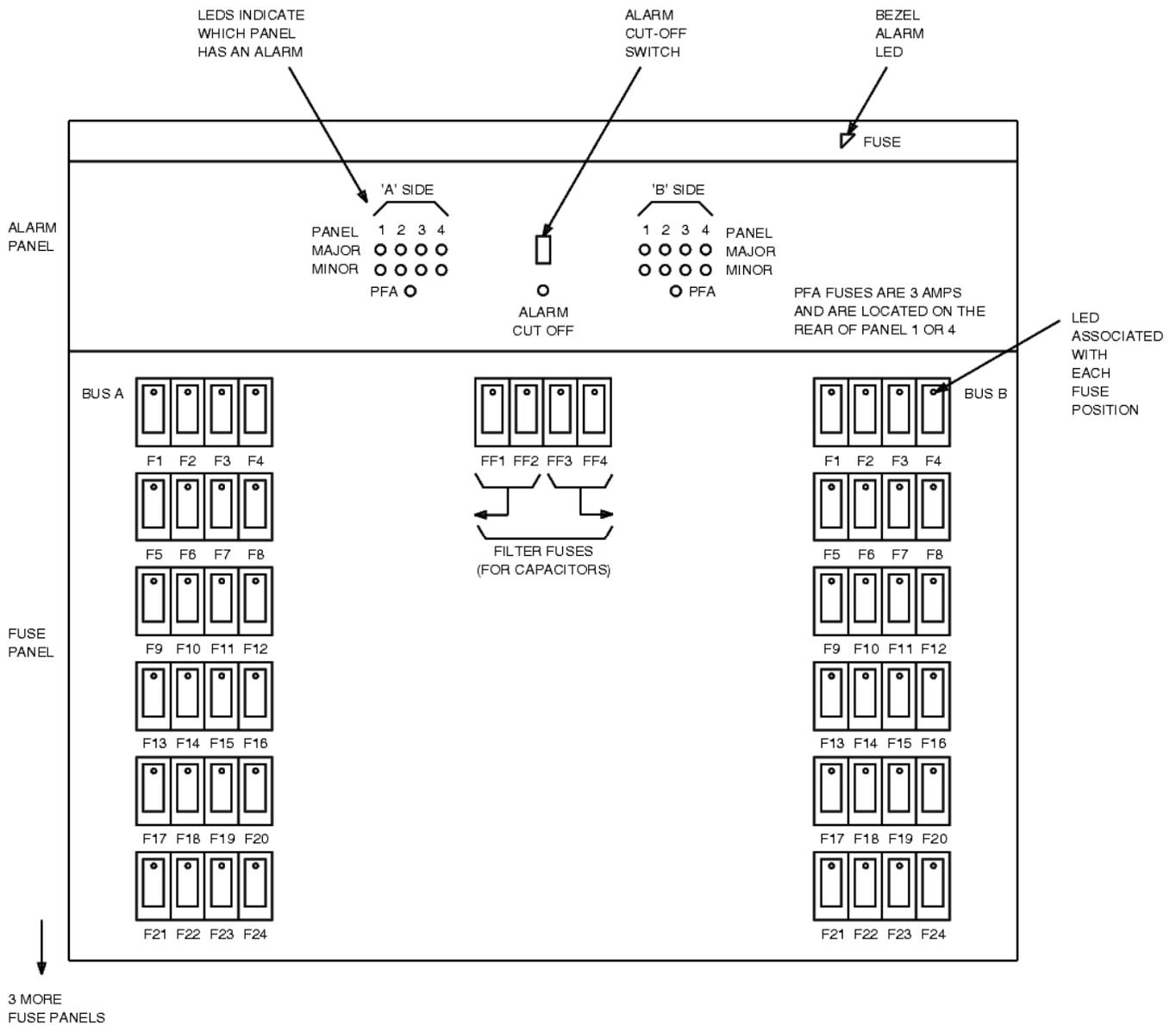
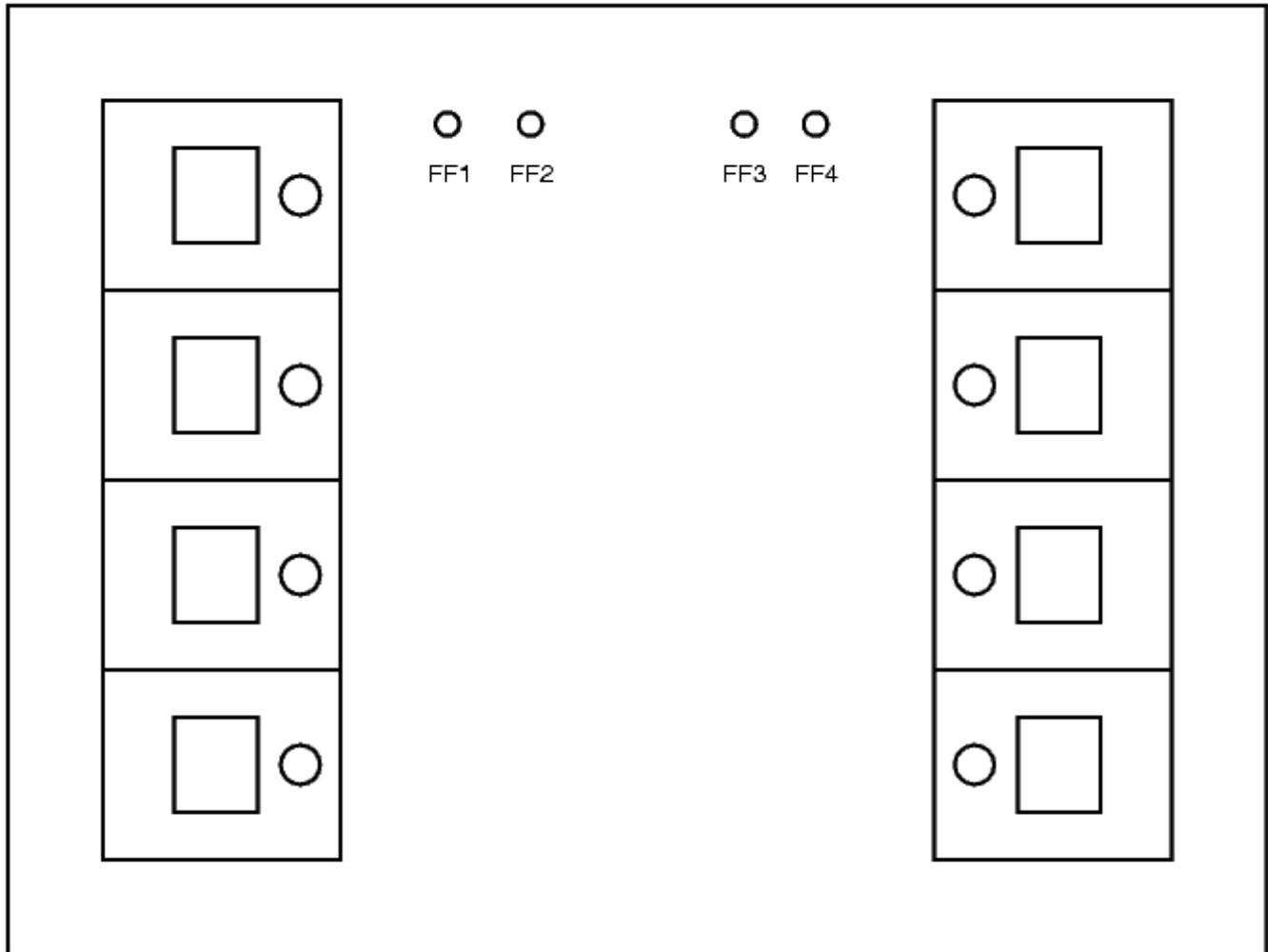


Figure 6-5 Alarm Panel and WP92955 Fuse Panel

pa 830876.01



FRONT

pa 830877/01

Figure 6-6 High-Current Fuse Panel (Front View)**GLOSSARY****A-Link**

The A-link connects the first- and second-stage switches of the line unit or access link from end office to STP.

Access Editor (ACCED)

The Access Editor is an administrative memory module function that controls the freeing and use of terminating number assignments.

Access Tandem (AT)

An *ESSTM* switch used to provide carrier access to end offices and possibly to colocated stations to directly control, in stages, the routing of an outgoing tie trunk call through the originating and intermediate switches. The user is said to "cut-through" these offices. These trunks are referred to as "nonsender" or "tandem" tie trunks.

Administration

Administration consists of related functions with the objective of ensuring the overall provision of switch service.

Administration includes the assignment of lines and trunks to the system, memory management, collection of traffic and plant data, provisions for additions and modifications to the switch, service evaluation and capabilities to control and manage the switch. The primary objective of administration is to assure that the switch delivers a high level of quality service to the subscribing customers. This is accomplished by monitoring and evaluating system performance. Potential problems that cause service deterioration are identified.

Administrative Module (AM)

The part of the 5ESS[®]-2000 switch which performs call processing, administration and maintenance which cannot be economically distributed to the switching modules. The AM consists of the processor, disk storage and tape backup units. The AM processor performs the central processing functions, controls the high-speed tape and the flow of data between the other dedicated processors distributed throughout the remaining units. The processor functions are fully duplicated (except for the port switch) to assure continued processing capability.

Analog Interface Unit (AIU)

The AIUs are hardware such as the LUs and TUs that connect wires from the MDF to peripheral interface control and data buses to the module processor and TSI.

Automatic Line Insulation Test (ALIT)

An OA&M feature enabling routine testing of analog line appearances that terminate directly on the switch. It runs tip-to-ring, tip-to-ground and ring-to-ground leakage tests.

Automatic Message Accounting (AMA)

This is a procedure in which the RAO processes the automatic accumulation of call data such as calling number, called number, date, time, duration, etc., to render a customer's telephone bill. Magnetic tapes and disks store the information from local and toll calls for billing purposes.

Automatic Message Accounting Teleprocessing System (AMATPS)

A billing system feature where the switch forwards billing information over a data link to a central AMA data collection system. The AMA data collection system interfaces with an RAO.

Automatic Number Identification (ANI)

A feature of a local switching office that automatically identifies the calling party without operator intervention.

Analog Trunk Unit (ATU)

The Analog Trunk Unit is a single-shelf unit in the Switching Module Control or Line Trunk Peripheral cabinets. It provides termination for interoffice trunks and trunks to operator positions and announcement machines.

Attempt

This is a peg count of an effort to use a facility or a circuit. An attempt may be a success or a failure.

Attribute

This is the title of a column in a data table having a unique name.

B-Link

A B-link is the output from 16 line unit (LU) half-grids that are multiplied onto 64 different paths.

BORSCHT

Battery feed, Overvoltage protection, Ringing, Supervision Coding and decoding, Hybrid (2-wire, 4-wire conversion) and Testing. This is a series of test routines provided with and run in the LU.

BRCS Feature Grouping (BFG)

The BFG function provides group feature assignment to lines. A BFG is a group of features and parameters. A BFG is not a group of DNs, terminals or MLHG members, but a BFG may be assigned to any number of DNs, terminals or MLHG members.

BX.25

This is the Lucent Technologies version of the Telecommunication Standardization Sector protocol X.25. This protocol is used for exchanging messages between the MSGS and the SM.

Basic Rate Interface (BRI)

The customer line's interface to the ISLU that combines two B-channels and one D-channel.

Bi-Peripheral Interface Data Bus (BPIDB)

The Bi-Peripheral Interface Data Bus is a data transfer point within the DNU-S unit.

Bootstrap

An initialization action which results in a memory reload and software initialization. The effect is the same as shutting a unit down and restarting it.

Bootstrapper (BSTR)

A part of the "fast pump" data link that works with the processor update bus to gain access to SM processor memory (see also Bootstrap).

Broadcast Warning Message (BWM)

This is an obsolete term. See Software Update.

Bus Interface Controller (BIC)

A unit which interconnects a duplex bus selector to the microprogrammer controller of the PIC.

Business and Residence Custom Services (BRCS)

The 5ESS[®]-2000 switch software that makes revenue generating features available to both business and residential customers.

Byte

Eight binary digits, or bits; the byte is the basic unit for measuring a computer's memory and storage capacity. Equivalent decimal values are 0 - 255.

Carrier Group Alarm (CGA)

This feature lets the local switching system infer the failure of a carrier group from observed call failures on only a few trunks in the trunk group.

Carrier Interconnect (CI)

This feature provides an interface between the local exchange and the interexchange carrier.

Central Control Input/Output (CCIO)

The CCIO is an interface that connects the CPU to up to two Direct Memory Access Controllers and up to two additional I/O peripherals.

Central Office (CO)

The central office is the switching equipment in a building that provides exchange telephone service for a given location. In some cases, there is more than one central office serving the same area. A central office may include more than one central office code.

Central Office Terminal (COT)

Hardware on the backplane of the DNU-S that change electromechanical signals to analog signals.

Central Processor (CP)

The central processor provides the primary control for operating the equipment that directs calls through the central office and aids in detecting and analyzing any faulty equipment involved in this task. In the switch, the AM is the central processor.

Central Processor Unit (CPU)

In general terms, the CPU is the area where all calculations take place. In a microcomputer, this is usually the microprocessor chip. In the 5ESS[®]-2000 switch, it is the Administrative Module. Other components may have their own independent CPUs.

Central Trunk Test Unit (CTTU)

An OS providing central trunk maintenance through a data link. This lets switching control center maintenance personnel perform remote trunk testing from a work station on a local switching office.

Circuit Pack

A circuit pack is a plug-in unit used as a convenient means for assembling, on a single mounting, one or more components such as capacitors, inductors, diodes, resistors, transistors, etc. The components are interconnected to perform one or more circuit functions, such as amplification, gating, timing, etc., required in a circuit. Typically, each circuit pack is an FRU.

Common Channel Signaling (CCS)

An operating capability of the software release that is compatible with the CCIS6, ECIS6, DSIS6, CCS7 and TSS message protocols and permits the switch to reach the No. 2 STP network.

Common Control (CC)

Two circuit packs in the DNU-S which implement a duplex unit controller that operates in active/standby mode. The primary functions of the CC include the termination of message and control channels originating from the SM-2000 CORE40 and interfaced via the PCT links and Common Data (CD) circuit packs; supervision of unit initialization, maintenance and diagnostics; implementation and handling of the control interfaces to all circuits in the DNU-S and non-volatile storage of CC and TMUX control programs in flash memory.

Common Control Switching Arrangement (CCSA)

switching arrangement is groups of trunks and one or more switching machines used to switch calls in a private leased network. All stations connected in the private network may call one another without using the public toll facilities. In addition, CCSA provides access to a DDD network for network inward calling to the centrex group, directs outward dialing to the DDD network and other features to the exchange network.

Common Data (CD)

The CD boards are located in the DNU-S and logically terminate the PCT links and perform rate conversion, selection and multiplexing/demultiplexing functions associated with passing data and control information between the PCT links and internal interfaces with other packs in the unit.

Common Network Interface (CNI)

The CNI functions as a packet switching system in the signaling network. The CNI is not a stand-alone switching system but requires configuration to an application such as the 5ESS[®]-2000 switch. The CNI consists of several peripheral processors (RPCs and LNs) serially interconnected and a central processor that performs the basic operating system duties in a distributed I/O processing architecture.

Common Network Interface/Interprocess Message Switch (CNI/IMS)

The CNI/IMS consists of a single switch cabinet that provides two types of ring nodes: RPCs and LNs. The CNI/IMS is connected to the AM by way of a dual serial channel and also interfaces with DDS facilities.

Common Optical Termination (COT)

These are paddle boards located on the back of the DNU-S board. The COT terminates the optical fibers for one side of a duplex PCT link and performs optical-to-electrical and electrical-to-optical conversion of data and control information received and transmitted over the PCT link interface with the SM-2000.

Common Shelf Unit of ISLU (CSU)

Supports all the equipment mounted in the ISLU drawer shelf units.

Communication Link (CLNK)

Logical path of control messages to/from DLI in SM from/to MMPs in AM.

Communication Module (CM)

Hardware that provides the interface between the AM and the SM(s). In a multimodule office, the CM consists of the message switch and the TMS.

Communication Module Control Unit-2 (CMCU2)

An updated version of the CMCU that is physically smaller but has an increased call handling capacity (see also CM2).

Communication Module Processor (CMP)

This unit can also be added to the CM2C. It is also referred to as the CMPU (Communication Module Processor Unit)

Communication Module Unit (CMU)

The Communications Module Unit is the basic FRU (circuit pack) of the CM2C.

Communications Module 2 (CM2)

An updated version of the CM that is physically smaller but has an increased call handling capacity. This has been accomplished by use of the new operationally larger TMS2 and MSG2, now housed in the CM2 cabinet instead of separate TMS and MSGS cabinets.

(Communications Module Control Unit (CMCU)

The CMCU, a part of CM2, provides message interface and timing facilities used to synchronize the time division network in the TMS via the TMSU. The CMCU consists of a DMI, NCLK2, TMS controller and metallic interface. The CMCU is not used in the CM1 configuration (see MICU).

Component

A server such as a trunk, tone decoder or service circuit that is a shared resource as opposed to being dedicated.

Concentration Ratio

The ratio of the number of lines terminated on the LU to the time slots available for the LU (64 time slots per LU).

Concentrator

A digital switching entity that permits more customers to share common output lines (for example, a 2:1 concentrator permits 48 customers to share the 24-channel capacity of a single T1 line)

Concentrator Group (CG)

Synonymous with LU pair of concentrators. There may be 4, 6, 8 or 10 concentrators to an LU.

Constructed Feature

Feature defined by a switch user (such as the service provider) for their particular needs.

Control Interface (CI)

A subunit of the TSIU, the control interface provides an interface and monitors communications between the SM processor and the interface units and reports errors detected; receives, latches and reports service requests from interface units to the SM processor; distributes control and clock signals to the module PUs via the peripheral interface control bus.

Control Interface Bus (CIB)

The bus carrying the control messages between the control fanout and the data fanout.

Control Time Slots (CTS)

The transmission periods for control signals during multiplexing or demultiplexing.

Control Unit (CU)

See Central Processor (CP).

Control and Data Interface (CDI)

The circuit providing the TU service group interface through the PICB and PIDB to the MCTU.

Customer Premises Equipment (CPE)

Telephone equipment located on the customer's premises.

Cyclic Sequential Search (CSS)

A path hunt used in the switch call processing software.

DS3

A transmission medium that can be fiber-optic or digital radio at a rate of 44.736 Mbps.

Data Base Manager (DBM)

Provides interfaces and access mechanisms between software systems and data in the data base.

Data Fanout (DF)

Data Fanout.

Data Interface

A subunit of the TSIU that provides the interface for the PCM data, signaling bits and the clock and time-slot synchronization between the TSI and the interface units.

Data Link Processor (DLP)

Data Link Processor.

Defense Switched Network (DSN)

A private 4-wire telecommunications network used for official business of the Department of Defense and military installations. The DSN incorporates unique features specific to government applications, including the use of 5ESS[®]-2000 switches as multifunction switches. The DSN has control to permit or limit access to commercial telephone company central office and trunk lines and to restrict commercial access to the DSN as deemed necessary. The terms DSN, AUTOVON, and DSN/AUTOVON are interchangeable when referring to this network.

Derived Data Links (DDL)

Data links used to communicate with other RSMs in a Multimodule Remote Switching Module (MMRSM) when in a stand-alone mode.

Dial Pulse (DP)

Method of transmitting digits (address information) between telephone customers and the central office or between central offices. It consists of DC pulses caused by momentarily opening the loop (usually at 10 "opens" per second). The numerical value of each digit is represented by the number of opens in a train of pulses.

Dial Tone Delay (DTD)

This is the time it takes the switching system to return dial tone to an originating line after the subscriber goes off-hook.

Dictionaries

A data base in the 5ESS[®]-2000 switch that provides information such as access type, relation and attribute identifications, number of subattributes, domain identifications, etc., in the memory structure.

Digital Carrier Line Unit (DCLU)

This unit terminates the T1 carrier from the SLC[®] 96 carrier systems to the switch.

Digital Line Trunk Unit - Model 2 (DLTU2)

Digital Line Trunk Unit — Model 2.

Digital Cross-Connect (DSX)

An internal interface that acts as a central point for cross-connecting, rearranging, patching and testing digital equipment and facilities.

Digital Equipment Number (DEN)

A 7-digit number used in translation to identify the location of a DLTU channel so that it may be used.

Digital Facilities Access (DFA)

This is an entry point for digital facilities in a 5ESS[®]-2000 switch.

Digital Facility Interface (DFI)

The circuitry in a DLTU that terminates a single T1 span line from a T-carrier RSM.

Digital Line Trunk Unit (DLTU)

This is hardware that terminates digital trunks with SMs by way of T1 lines.

Digital Network Unit - SONET (DNU-S)

An SM-2000 peripheral unit which provides an optical trunk interface. Its primary function is to terminate SONET facilities and overhead. It converts data and signaling information between SONET and PCT link format. It provides the 5ESS[®]-2000 switch interface for interoffice circuit switched trunks (inband and CCS), TR303 digital loop carriers and RSMs.

Digital Ordering and Planning System (5 DOPS)

The standard engineering ordering and pricing vehicle for the 5ESS[®]-2000 switch.

Digital Service Unit (DSU)

A functional part of the SM that generates and decodes tones, tests ISDN lines and CCS trunks and provides recorded announcements for the OSPS.

Digital Service Unit Bus (LDSUB)

A data connection terminating the time slot interchanger in the MCTU and the serial data interface circuit on the DSC pack. The LDSUB is the path over which digital tone samples pass to and from the DSU2.

Digital Signal Processor (DSP)

A special microprocessor that performs signal processing operations in the universal tone decoder, universal conference circuit and transmission test facility.

Digital Universal Conference Service (DUCS)

A 3-port or 6-port conference circuit capable of conferencing up to three or six parties, respectively.

Direct Link Node (DLN)

A node on the CN1 ring for signaling message processing normally done by the AM. The DLN is connected with other nodes on the ring by way of the dual ring bus.

Direct Memory Access (DMA)

Provides direct access to the main store by peripheral units without involving the AM.

Directly Connected Test Unit (DCTU)

A unit connected to each line and trunk to provide a number of required facility tests.

Directory Number (DN)

A 7-digit telephone number made up of a 3-digit central office code and a 4-digit station number. It is also called TN.

Disk Drives

Memory storage hardware that uses magnetic recording on rotating disks. Disk drives provide reliable and flexible mass memory storage for infrequently used programs and data. A single drive, with its controller, makes up a Disk Unit.

Disk File Controller (DFC)

A microprocessor-controlled unit that is programmed to accept tasks from the AM and then assigns each task to a disk drive work queue.

Disk Unit (DU)

See Disk Drives.

Disk Unit Package (DUP)

See Disk Drives.

Dual Link Interface (DLI)

This is a connection from the TSI to the NCT links which inserts control messages between the module processor and the AM or other module processors, providing buffering and timing.

Dual Multimodule Processor (DMMP)

An optional feature for hardware expansion, providing greater reliability for full message transfer capacity in CM2 equipped offices.

Dual Serial Channel (DSCH)

A bus in the CNI that provides packet data transfer between the RPCs, LNs and the AM.

Dual Tone Multifrequency (DTMF)

Method of transmitting digits (address information) from telephone customers to the central office. It consists of sending a simultaneous combination of one of a lower group of frequencies and one of a higher group of frequencies to represent each digit (1 through 0), and symbols (* and #).

Duplex Dual Serial Bus Selector (DDSBS)

A channel which permits the connection of two dual serial channels to a single I/O device.

Duplex Message Interface (DMI)

Circuitry terminating the message interface fuses from the module message processors.

Duplex Multienvironment Real-Time (DMERT)

The software operating system program used by the AM.

Dynamic Memory

The equipment used to magnetically store information which is changed frequently, such as equipment and work status, work queues, etc. Dynamic memory, dynamic data and dynamic ODD are used interchangeably.

E&M Signaling Leads

A signaling system that derives its name from historical designations of the signaling leads on the circuit drawings covering these systems. The M-lead carries supervisory (and sometimes dial pulse) signals from the switching equipment to the signaling/transmission equipment. The E-lead carries supervisory signals from the signaling/transmission equipment to the switching equipment. As a result, signals from office A to office B leave on the M-lead at office A and arrive on the E-lead at office B.

Electrical Line Interface (ELI)

Splits the received DS1 signals to active/standby LSIs and combines the transmitted DS1 signals. Each ELI

can handle 20 DS1s.

Electrical Network Line Interface (ENLI)

Terminates one bi-directional electrical link to the Transmission Rate Conversion Unit model 2 (TRCU2).

Electronically Erasable Programmable Read-Only Memory (EEPROM)

A type of EPROM which can be erased electronically and rewritten without removing the chip or component from its surroundings.

Emergency Action Interface (EAI)

The interface connecting craft input to the central control for certain maintenance functions.

Emitter-coupled Logic Bus (EBUS)

The EBUS is the communications path between the CMCU and the TMSU2.

End-of-Period (EOP)

A statistical term used in engineering that denotes the end of a predetermined engineering period. It is the time between scheduled phases of equipment growth or modification operations.

Engineering and Administration Data Acquisition System (EADAS)

An automated traffic data collection system which collects and summarizes data obtained from central office switches to be used for administrative and engineering purposes.

Enhanced Private Switched Communications Service (EPSCS)

A private switched network of dedicated facilities providing full duplex communication on all connections. It provides a center from which the customer can exercise, monitor and control functions relative to the performance of the network.

Equal Access End Office (EAEO)

An *ESSTM* switch used to provide carrier access to collocated stations.

Equal Access Signaling (EAS)

A signaling method introduced by the carrier interconnect feature.

Equipment Access Network (EAN)

A circuit pack which is a distribution node in the upper equipment shelf of the Directly Connected Test Unit (DCTU).

Equipment Location (EQL)

The Equipment Location is expressed as a 9-digit index used to identify the location of a component. Refer to figure 4-1 for more detailed information.

Erasable, Programmable, Read-Only Memory (EPROM)

A type of read-only-memory (ROM) that can be erased and rewritten.

Erlang

A measure of communications traffic intensity representing the full-time use of a communications facility. One Erlang equals 36 ccs.

Extended Switch Model-2000 (EXM-2000)

An optically remoted SM-2000 that provides the capability to deliver SM-2000 functions at a remote location. The EXM-2000 has the functions provided by local SMs during normal operations. When an EXM-2000 is isolated from the host switch, only optical standalone functions are available.

Extreme Value Engineering (EVE)

A method of engineering a switching system based on the extreme (that is, most space required, most lines

needed)expected use parameters.

Facilities Interface Unit (FIU)

Used between the RSMs and the host SMs and connects the T1 format to the NCT format.

Field Replaceable Unit (FRU)

An FRU is a single component of a system (such as a circuit pack) that can be replaced on the spot by a field technician. The FRU is generally the smallest level of item that can be replaced at the customer's site. Board- and chip-level repairs usually involve shipping a defective FRU to a maintenance depot.

Firmware

Firmware is software contained on a non-volatile medium (for example ROM, PROM, EPROM, EEPROM), as part of the on board operating components of a circuit pack or FRU.

Foreign Exchange Service (FX)

A provider of customer access to a distant central office by (FX) trunks. Incoming foreign exchange calls are placed to the listed (FX) directory number and answered by the attendant. Outgoing calls may be made on an attendant basis and/or on a station user direct-dial basis.

Foundation Link Interface (FLI)

A circuit pack (TN883) which is installed in SM cabinets 5 and/or 6, which serves as a terminator.

Foundation Peripheral Controller (FPC)

A peripheral control in the input/output processor used to provide an AM interface to the TMS and maintenance access to the message switch. The FPC issues time slot path requests to the TMS and acts as an interface between the peripheral subunits and the MSGS. In the CM1 configuration, the FPC is part of the MSPU. Under direction of the AM processor, the FPC controls the configuration of hardware in the MICUS. In the CM2 configuration, the FPC is part of the MSCU2. Under direction of the AM processor, the FPC controls the configuration of hardware in the MSCU2s.

Gated-Diode Crosspoint (GDX)

Electronic devices used to pass current in either direction and used in the LU line concentrator.

Global Digital Service Unit (GDSU)

A part of an SM that provides up to eight digital service circuits for low usage functions such as 3-port and 6-port conferences, test tones, responses to test tones and processing test responses.

Global Power Distribution Frame (GPDF)

Provides redundant, protected direct current to power 5ESS[®]-2000 switching system equipment.

Growth

The systematic modification of central office equipment to provide increased call-handling capacity and improved service. Growth is required so a switch may evolve economically over a wide range of services and traffic needs.

Half-Call

The establishment of a path between a peripheral unit and the TSI. The terminating part of a call represents a half-call and the originating part of the call represents the other half-call. Each half-call generates a terminal process.

High-Level Service Circuit (HLSC)

A service circuit in the LU used to perform all line service circuit functions which cannot be provided through the TSI.

Host Office Collector (HOC)

A central AMA data collection system which collects AMA data over data links from several telephone switching

offices.

Host Switching Module (HSM)

The SM in the host office terminating umbilicals from one or more RSMs.

IOP Basic Unit (IOPBU)

Processor used to control transfers between the main store (MS) and peripheral equipment.

IOP Disk File Controller Unit (IOPDFCU)

This is a generic name for the type of device typified by the Main Store Input/Output Disk File Controller Unit (MASIOPGU).

IOP Growth Unit (IOPGU)

This is a generic name for the type of device typified by the Main Store Input/Output Growth Unit (MASIOPGU).

Input/Output (I/O)

Input/output is the process of transmitting information from an internal source to an external destination and vice versa.

Input/Output Microprocessor Interface (IOMI)

A unit that provides the interface between the 16-bit PIC and up to 16 of the 8-bit MMPs.

Input/Output Processor (IOP)

The IOP controls transfers between the MAS of the AM and the MCC, operation and maintenance center and remote terminals. The IOP provides interfaces to visual display units and hard-copy printers in the MCC and other work stations and magnetic tape drives.

Integrated Digital Carrier Unit (IDCU)

This unit provides a nonproprietary integrated interface with subscriber loop carrier systems. The IDCU provides the same functions as the DCLU but provides analog and ISDN interface to customers on the remote terminal.

Integrated Services Digital Network (ISDN)

An international plan originated by the Telecommunication Standardization Sector representing the latest step of the evolution of the analog telephone to an all-digital network. Digital voice, circuit-switched and packet-switched data may be transmitted simultaneously over the same interface.

Integrated Services Line Unit (ISLU)

This unit houses the Basic Rate Interface (BRI) cards in the SM and provides analog and digital services to subscribers by support of the following interfaces: ISLU-T, a 4-wire BRI that provides the basic Integrated Services Digital Network 2B+D access over a range of up to 1,900 feet; ISLU-U, a 2-wire BRI that provides the basic ISDN 2B+D access using echo-canceled hybrid technology appropriate for all carrier serving area nonloaded loops; ISLU-Z, for analog lines (that is, POTS, coin-first coin lines, party lines, etc.) which normally terminates on the analog-concentrated line unit. The ISLU-Z interface can have a concentration ratio of up to 8:1.

Integrated Services Test Function (ISTF)

A group of diagnostic functions, originally native to the DSU2 unit; also, a general term for diagnostic functions native to any FRU.

Inter-RSM Communications Links (ICL)

The links that interconnect SMs in a multimodule RSM.

Interface Unit (IU)

A component that provides customer terminations.

International Telegraph and Telephone Consultative Committee (CCITT)

Currently known as Telecommunication Standardization Sector.

Interprocess Message Switch User Node (IUN)

In the 5ESS[®]-2000 switch, the IUN is a component which has no function other than to occupy a position reserved for future growth. As such, it is a temporary filler component.

Interprocessing Message Switch (IMS)

Hardware and software in the SM used to support OSPS, BRCS, CSDSCII and the ICLID for interoffice calls and 16 kb/s intraoffice packet switching.

Key

Designation assigned to one or more data base attributes that provides access to a particular tuple.

Key Service Indicators

These indicators give the administrator a quick view of the overall quality of service being provided to the subscribers.

Kilobyte (kB)

1024 bytes (by analogy with the metric prefix "kilo-", 1,000).

Line Equipment Number (LEN)

An 8-digit number used in translations to identify a customer's line.

Line Group (LG)

A general term for a circuit pack installed in a drawer in a Common Shelf Unit of an ISLU. Up to 16 can be installed in each drawer.

Line Group Controller (LGC)

The interface between switched information on the group interface data bus and the link interface data bus.

Line Group Power (LGP)

A circuit pack located adjacent to the Line Group Controller (LGC) in the Line Group Common Area. See Section 5.3.

Line Information Data Base (LIDB)

A 32-time slot bus that connects the Line Group Controllers (LGC) and the common data boards in the ISLU.

Line Trunk Peripheral (LTP)

Consists of the LU, TU, MSU, DCLU, FIU, and the modular metallic service unit.

Line Unit (LU)

An interface unit between the analog (subscriber) lines and the SM.

Link Nodes (LN)

A part of the CNI that performs the message handling protocol, control functions and self-diagnostics. The LN establishes the connection to the signaling network by way of A-links.

Local Digital Service Unit (LDSU)

A part of the SM that provides high-usage service circuits such as tone decoding, tone generation, conferencing and voice-frequency testing.

Local Digital Service Unit (Modified) (LDSUM)

A single circuit pack (TN1637) which replaces tone decoding and generating equipment and Common Digital Service Units in the LDSU.

Local Digital Service Unit Function (LDSUF)

The part of the DSU2 that generates and decodes tones.

Local Test Desk (LTD)

The local test desk provides equipment that performs local primary line testing. It may be used to test parts of the toll plant.

Loop Side Interface (LSI)

Frames on each of the DS1s and converts it to a PIDB-like format on the internal bus to the PTI and collects DS1 performance-monitoring data and detects DS1 failures and alarms.

Machine Load and Service Summary (MLSS)

A report which provides cumulative service year to date and additional capacity information for each SM.

Main Distributing Frame (MDF)

This is a connection system that interfaces between loop cable pairs and switching equipment.

Main Store (MAS)

The MAS is RAM (16 megabytes) in the AM that contains data needed for operating the switch, such as the software release for AM functions, translations, call processing registers and billing registers. The MAS is duplicated for reliability.

Main Store Array (MASA)

A circuit pack (TN56) which contains a series of up to eight 2-megabyte RAM modules which extend the MAS from 16 to up to 32 megabytes. See also MASIOPDFCU.

Main Store Controller (MASC)

The MASC controls access to the MAS and MASA, determines memory priorities, and checks memory.

Main Store I/O Disk File Controller Unit (MASIOPDFCU)

An optional unit needed to expand the 16 MB capacity of the MAS main unit to a possible 32 MB by increments of two.

Main Store I/O Growth Unit (MASIOPGU)

Main Store I/O Growth Unit.

Main Store Update (MASU)

See MAS.

Maintenance Teletypewriter (MTTY)

The human-machine interface to the administration module.

Master Control Center (MCC)

The local human-machine interface to the switch including system status displays, hard-copy printers and manual controls over system operations.

Mechanized Loop Testing System (MLT)

An external operations system for testing of the customer lines (loops) in the 5ESS[®]-2000 switch.

Megabyte (MB)

A unit of data storage or memory capacity; it is 1,048,576 bytes or 1,024 kB (kilobytes).

Memory Expansion Unit (MEU)

Hardware that provides additional memory capacity for SMs and/or RSMs.

Message Handler (MH)

The Message Handler is an independent processor unit which manages all data traffic among the various SM-2000 subprocessors.

Message Interface Bus (MIB)

A channel for data transfer, such as that between the Pump Peripheral Controller (PPC) and the Communication Module Control Unit (CMCU).

Message Interface Clock Unit (MICU)

This is a unit in a message switch which consists of the network clock and the NCT link interface from the message switch.

Message Switch (MSG/MSGS)

This is the unit that performs internal interprocessor message switching, provides terminations for common channel signaling (CCS) and contains the message interface clock unit.

Message Switch Control Unit (MSCU)

The MSCU is a part of the CM and is responsible for handling control information between the AM and module processors.

Message Switch Control Unit - Model 2 (MSCU2)

This circuit pack reformats data received from the AM or CMPU and transmits it to the other units in the cabinet and vice versa; interprets destination codes of incoming control slots and switches the control time slots to the AM or another SM and provides control of the other units in the CM2 cabinet.

Message Switch Control Unit - Model 3 (MSCU3)

A unit which controls message transfers between the AM and as many as 14 peripheral control communities. It performs serial-to parallel and parallel-to-serial conversion of data received from/transmitted to the AM; provides control to transfer data between the AM and FPC or PPC; provides manual and AM control of the MSCU3 from an in-service/out-of-service perspective.

Message Switch Peripheral Processor (MSPP)

The controlling circuit pack of all message switch peripheral controller applications.

Message Switch Peripheral Unit (MSPU)

Hardware unit of the CM that switches interprocessor messages on the control time slots.

Message Switch Peripheral Unit - Model 2 (MSPU2)

This is the particular model of MSPU which is mounted in EQL 53 of all Communication Module Model 1 cabinets.

Message Switch Peripheral Unit - Model 3 (MSPU3)

This is the particular model of MSPU which is mounted in EQL 53 of all Communication Module Model 2 cabinets.

Message Waiting Indicators (MWI)

An ISDN feature informing a customer of a message waiting. Three types of indicators are provided:

- (1) **Audible Message Waiting Indicator:** Provides a tone when the customer goes off-hook.
- (2) **Electronic Billboard:** Provides name of person having messages.
- (3) **Visual Message Waiting Indicator:** Activates a message waiting lamp on the station set.

Metallic Access (MA)

Connection with metallic wires as opposed to connection with fiber-optics or other types of connections.

Metallic Service Unit (MSU)

A unit which provides an access network which connects analog facilities and DC test equipment; provides scan and distribute functions, metallic access, automatic line insulation testing and gated-diode crosspoint compensation.

Metallic Test Bus (MTB)

The bus connecting the modular metallic service unit to the test access circuit within each trunk unit. This bus is used for maintenance and routine test activities.

Metallic Test Interface Bus (MTIB)

See MTB.

Micro Code (MC)

Software written in a low-level computer language, typically an Assembler language program. Also, an identifying code on a circuit pack label identifying the revision level of the on-board firmware.

Modular Controller Time Slot Interchanger (MCTSI)

An alternate designation for MCTU.

Modular Metallic Services Unit (MMSU)

Provides metallic access, miscellaneous scanning and distributing functions, automatic line insulation test, and gated-diode crosspoint compensation.

Module Controller and TSI Unit (MCTU)

A component which provides a variety of interface functions between the Switching Module (SM) and other components and modules in the 5ESS[®]-2000 switch.

Module Controller and TSI Unit - Model 2 (MCTU2)

The MCTU2 is a modified but equivalent version of the regular MCTU.

Module Message Processor (MMP)

Circuitry in the MSPU that handles control message protocol on the link to the SMs.

Module Processor Interface (MPI)

Module Processor Interface.

Moving Head Disk (MHD)

A high-capacity, random-access digital data storage device the AM uses to store infrequently used programs and data.

Multi-Module Remote Switching Modules (MMRSM)

The MMRSM consists of one to four RSMs interconnected by dedicated T1 links. Each RSM is also connected to an SM at the switch by dedicated T1 links.

Multiline Hunt Group (MLHG)

A group of customer facilities which are identified as a group in translations. When calls are placed to the MLHG, the switch hunts for an idle member of the group beginning with the dialed DN.

Network Administration Center (NAC)

A work group attached to the Switching Control Center System (SCCS) and designated to automatically receive the following: 15-minute traffic reports; 5-minute, 1-hour, 24-hour and monthly plant reports; and 30-minute traffic reports on request.

Network Clock (NCLK)

The digital reference clock for the Lucent network.

Network Control and Timing (NCT)

A fiber-optic path which connects an SM to the TMS, provides time-slot paths for network connections, carries a control time slot to the SM and distributes timing to the SM.

Network Link Interface (NLI)

Terminates one bi-directional optic link (two physical fibers) to the CM.

Nonredundant Office Dependent Data (NRODD)

Office dependent data that is not backed up (call processing data, for example).

ODD (Static)

Data that establishes the types and amounts of various equipment that comprise the office (lines, trunks, equipment, etc.). The protected area of memory.

Office Data Base (ODB)

The ODB is a store of information specific to the particular office or location served by a 5ESS[®]-2000 switch. Also called Office Dependent Information.

Office Data Base Editor (ODBE)

A feature of the 5ESS[®]-2000 switch memory management that lets technicians change data base information.

Office Dependent Data (ODD)

Equivalent to ODB; a data base specific to a particular office.

Office Monitoring System for the 5ESS[®]-2000 Switch (OMS5)

A tool or program that assists the maintenance personnel in the performance of the daily preventive maintenance of the switch.

Office Records

Office records are tabular listings of the actual inventories and assignments of the data base and serve as a means for administering the office. An explanation of the form entries is included in the translation guide TG-5.

Office Repeater Bay (ORB)

A bay in the office, usually near the digital system cross-connect bays, that houses the digital repeaters used to regenerate the PCM data for a T1 line.

Operating Telephone Company (OTC)

Telephone Company owning a 5ESS[®]-2000 switch.

Operational Capacity

This capacity is the indefinitely sustainable operation point while processing calls with an ideal, fault-free exchange and an unlimited supply of internal resources and external facilities.

Operational Support System (OS)

Computer systems which may be used to provide additional administrative support (for example, EADAS, COER, SCCS).

Operations, Administration and Maintenance (OA&M)

This is a series of functions run by the DNU-S unit which provide, among other things, verification, monitoring, tracing and alarms.

Operator Services Position System (OSPS)

The OSPS uses features provided by a host 5ESS[®]-2000 switch and dedicated peripheral equipment to support operator and attendant services.

Optically Remoted Switching Module (ORM)

A type of remoted SM that is interfaced to the switch through the CM instead of a host SM. This is done by way of DS3 transmission or T1 facilities (fiber-optic, digital radio, cable or T1) at a rate of 44.736 MB/s.

Outgoing Trunk (OGT)

An outgoing trunk is a 1-way trunk where only originating traffic can reach a distant office to complete telephone calls. Originating traffic in the distant office cannot reach this trunk.

PIDB Transmission Interface (PTI)

Provides a signal processing function which monitors incoming signaling to detect originations and transmits idle signaling.

Packet

A group of bits that is switched as an integral unit. Typically, packet contains data, destination and origination information, and control information, arranged in a particular format.

Packet Bus (PB)

The packet interface between the PSU and the MTCU.

Packet Interface Bus (PIB)

Packet bus internal to the PSU; that is, the interface between the packet fanout and the control fanout circuitry.

Packet Switch Unit (PSU)

The PSU contains circuitry that provides a central high bandwidth interface to support packet signal messages and packet data switching. The PSU is a part of the SM and occupies from one to five equipment shelves in a single cabinet.

Path Hunting

This is a routine the switch uses to select the A- and B-link that connect a given line with an available channel circuit. In addition to finding this path, the path hunt software updates the A- and B-link status maps.

Peg Count

A cumulative count of the number of times a specified event occurs during a given time interval. In some cases, the event may be an attempt to take some action, not necessarily a successful attempt.

Peripheral Control and Timing (PCT)

An interface between the DNU-S and SM-2000 which replaces the Peripheral Interface Data Bus (PIDB) and Peripheral Interface Control Bus (PICB).

Peripheral Controller (PC)

Circuitry in the input/output processor that connects to peripherals outside the AM.

Peripheral Interface Control Bus (PICB)

A duplex set of wires carrying control information between the module controller and an interface unit on the SM.

Peripheral Interface Controller (PIC)

The PIC controls the movement of commands and data between the AM processor and the peripheral controllers.

Peripheral Interface Data Bus (PIDB)

A duplex set of wires providing 32 time slots between the data interface and interface units.

Peripheral Unit (PU)

Equipment such as the LU, TU, DLTU, DCLU and GDSU that works with but is not a part of the AM, CM or SM. Peripheral units reside in the SM.

Plain Old Telephone Service (POTS)

Basic voice service by way of telephone.

Plant Measurements

These measurements provide data to evaluate equipment and craft performance.

Poisson Capacity Table

A statistical table, based on a theoretical mathematical formula, that is used to estimate the types and amounts of telecommunications equipment required to provide certain levels of service to a known or projected number of subscribers.

Port Switch Unit (PSU)

The interface between the master control center (MCC), teleprinter and printer.

Power Distribution Unit (PDU)

The Power Distribution Unit is based in processor cabinet bays 0 and 1; it routes power from the Power Distribution Frame (PDF) to other components.

Preconstructed Feature

Feature defined by Lucent and is available to all switch users (service providers).

Primary Rate Interface (PRI)

An ISDN feature supporting digital interface to digital PBX on a primary rate carrier (1.544 MB/s). It supports twenty-nine 64 kbps B-channels, plus one 64 kbps D-channel.

Private Branch Exchange (PBX)

A switching system installed on a customer's premises.

Private Facilities Access (PFA)

This feature lets subscribers have dial access to various types of public and private switching arrangements.

Process Identification (PID)

A number assigned to the running of a program for reporting and tabulating purposes.

Protocol

An agreed-on procedure for transmitting information between two or more entities.

Protocol Handler Data Bus (PHDB)

Data bus internal to the PSU that is the interface between the PH and the data fanout circuitry.

Protocol Handler (PH)

Circuitry that switches control messages between the Basic Rate Interface (BRI) and the MCTU.

Pulse Code Modulation (PCM)

A technique for coding analog signals for transmission on a digital circuit.

Pump Peripheral Controller (PPC)

Circuitry in the MSGS that is responsible for rapid reinitialization in case of total failure of the SM.

QLPS Gateway Link (QGL)

The 32-time slot/2-Mbps metallic link between a specific QGW and QLPS. Each QGW has four QGLs, each multiplexed into an associated QLNK stream. Each QLPS may have 0, 2 or 4 QGLs equipped, depending on the number of QGWs equipped.

QLPS Gateway Processor (QGP)

A device which provides an interface between the QLPS and the 5ESS[®]-2000 switch communications

foundation.

Quad-Link Interface (QLI)

A reconfigurable connection to a TMS fabric port (256 timeslot access). Each QLPS has four QLPS links.

Quad-Link Packet Switch (QLPS)

An optional message switch, QLPS is a high-speed subswitch which supports the increased call capacity of the 5ESS[®]-2000 switch.

REORG

A memory reorganization that may be needed when the processing speed is reduced.

Random Access Memory (RAM)

A type of memory that can be both read from and written to. It can contain resident information (static) or transient information (dynamic).

Read-Only Memory (ROM)

Memory whose data content is preset by the manufacturer. Data content in ROM does not change even if power to memory is removed. See also PROM, EPROM and EEPROM.

Receive-Only Printer (ROP)

The printer used only for receiving messages at the MCC.

Recent Change (RC)

This is the ability to change the system data base to reflect changes in customer or system capabilities.

Recorded Announcement Function (RAF)

A feature that provides independent playback of prerecorded, variable length and variable content Operator Services Position System (OSPS) announcements.

Recorded Announcement Unit (RAU)

A totally electronic storage device (no moving parts) which uses magnetic bubble memory to store recorded messages in digital form. Using a maximum of four 13A announcement machines, the RAU provides up to 32 channels of recorded messages.

Redundant Office Dependent Data (RODD)

Office dependent data that is backed up.

Regional Technical Assistance Center (RTAC)

The RTAC is the technical support office assigned to your part of the country. The phone number for RTAC information is **1.800.225.RTAC (7822)**.

Relation

A rectangular data table (matrix) that has rows called tuples and columns called attributes.

Remote Integrated Services Line Unit (RISLU)

The RISLU terminates digital and analog lines. It consists of an ISLU and a DLTU-R, and it is connected to a host SM by T1 carrier. The RISLU may be located up to 175 miles from the host switch. The RISLU is a remote version of the central office equipment and provides analog and digital services (including some switch features) to remote subscribers. The RISLU provides up to 496 terminations for remote operations over 24- and 30-channel pulse code modulation (PCM) facilities. The RISLU provides the same three types of interfaces (T, U and Z) as the ISLU.

Remote Memory Administration System (RMAS)

An operational support system used to load translation changes into the switch.

Remote Switching Module (RSM)

This is a type of SM that is located away from the switch. The RSM provides the switching capabilities of the 5ESS[®]-2000 switch to areas that cannot economically support an ESSTM switch.

Remote Terminal (RT)

A software release term denoting the remote vehicle in any pair gain or remote switch system.

Revenue Accounting Office (RAO)

A telephone company central computation center where per-message charges are calculated from Automatic Message Accounting (AMA) billing data, combined with other fixed monthly charges and prepared for delivery to telephone customers.

Revertive Pulse (RP)

A signaling pulse made by an LDSU transceiver to another LDSU transceiver on the same line. The LDSU2 does not provide RP transceivers.

Ring Peripheral Controller (RPC)

A part of the CNI that transports signaling messages and internal control CNI/IMS messages between the AM processor and the ring by way of a dual serial channel. The RPC node does not provide network connection. The switch uses two RPCs.

Ring Peripheral Controller Node (RPCN)

The Ring Peripheral Controller Node is a circuit pack that manages communications between the Ring and the Administrative Module. Two RPCNs are always used in the 5ESS[®]-2000 switch Common Network Interface (CNI) application.

Route Index

A code used in selecting the path a call takes through an office.

SAS Digital Service Circuit Controller (SASDSC)

A controller board (TN1841) with a variety of interface functions for the SM, PICB, PIDB and SAS memory.

SAS Memory Board (SASMEM)

A board which uses PCMCIA flash memory cards to support speech recording at a rate of 422 seconds of speech per 4 megabytes of memory.

SLC[®] 96 Carrier

A digital loop carrier pair gain system used as a supplement or replacement for cable. It serves up to 96 subscribers over T1 transmission facilities.

SLIM(2) Board

For software release 5E10 and later, a Subscriber Line Instrument Measurement (SLIM) (2) board (TN1422) is an optional board to insert in the MMSU. The SLIM(2) is designed to do measurements on analog and digital subscriber lines as well as analog trunks. It will measure the metallic characteristics of the line/trunk such as voltages, insulation resistances, and capacitances. SLIM(2) can be operated in both Operator Mode (TLWS 5700 page, similar to the DCTU page) and Routine Mode (recent change driven, similar to the ALIT).

STSX-1

An electrical interface that has STS-1 format conforming to SONET standard.

STSX-1 Facility Interface (SFI)

SFI pairs in the DNU-S implement a duplicated electrical interface for six STSX-1 links. The SFI implements STSX-1 line drivers and receivers, implements Bipolar 3-Zero Substitution (B3ZS) encoding and decoding, and interfaces each of the six STSX-1 links to either one service TMUX or the spare TMUX.

STXS-1 Link Interface (SLI)

A passive circuit containing a splitting transformer for coupling the received STXS-1 signal and two SFI circuit packs and another transformer that couples the STXS-1 transmit signals from two SFIs to the facility. It also implements a Ling Build Out (LBO) function on short links.

Screening

A translation process to determine what type of treatment to give a line. Screening information is used in the routing process.

Service Announcement System (SAS)

A feature that supports automatic collect call and requires speech recognition, digit reception, call progress monitoring and the recording and playback of a caller's name on a per-call basis. Each SAS unit can provide up to 32 independently phased announcement channels.

Service Group (SG)

The maximum set of resources which can be affected by a single hardware fault.

Service Measurements

These measurements provide data used to evaluate the quality of telephone service to the customer.

Signal Processor (SP)

Circuitry in the SM that performs supervisory scanning. It also detects incoming bylink pulses from step-by-step offices.

Small Computer System Interface (SCSI)

An industry standard interface between a central processor (in 5ESS[®]-2000 switching units this is the AM) and peripherals (that is, hard disk drives) which also conform to the SCSI standard.

Software Change Administration and Notification System (SCANS)

A dial-up system which uses a 2048 data set to distribute software changes in stored program control programs to the telephone company in the form of software updates. SCANS serves the responsible Switching Control Center System (SCCS).

Software Release

The software release is a fixed software program that makes up the basic operating system and is the same in all switch offices with the same program name and issue. It uses individual office translations to accommodate custom features for different installations.

Software Update

A electronic message containing a software release ``fix" or update that is disseminated on a priority or urgent basis.

Space Division

Space division is a method of serving a number of simultaneous calls by assigning different physical transmission paths through a switching network to those calls. In the 5ESS[®]-2000 switch, the TMS does space division switching.

Static Memory

Equipment used to store information which is changed infrequently, such as, characteristics of a particular telephone office (types and amounts of equipment, lines, trunks) and features associated with telephone numbers. Static memory, static data and office dependent data (ODD) are used interchangeably.

Subscriber Loop Interface Module (SLIM)

Replaces the standard office repeater bay used in direct mode I or II interfaces and terminates T-carrier from mode III shelves in D4 format.

Supplementary Trunk Line Work Station (STLWS)

Additional (one or more) trunk test facilities (digital), usually in larger offices, that provide access to the Trunk and Line Work Station (TLWS) by way of the Master Control Center (MCC). The STLWS need not be physically close to the MCC.

Switching Control Center (SCC)

A central location from which the operations for one or more switches can be monitored and controlled.

Switching Control Center System (SCCS)

A system that centralizes control, administration and maintenance of the switching systems for several central offices.

Switching Delay

This is the time from arrival of sufficient address information until the exchange starts sending a seizing signal on an outgoing circuit, a calling signal on a subscriber line or another appropriate indication (for example, congestion tone).

Switching Module (SM)

The SM connects all external lines and trunks to the switch and handles most of the call processing tasks. The SM converts signals received from the lines and trunks into internal digital time-division format of the office.

Switching Module Processor (SMP)

The SMP is a part of the SM that performs call-processing functions for lines and trunks terminating on the SM and maintenance functions for the SM equipment. There are two SMPs (an active and standby) in each SM. Each SMP is augmented by a separate signal processor located in the Time Slot Interface Unit (TSIU).

Switching Module Processor Unit (SMPU)

The SMPU is a part of the SM and consists of a duplicated SM processor (model 2) and the bootstrapper.

System Process

Software process that exists as long as the switch is functioning. System processes are associated with non-call-processing tasks such as maintenance and billing functions.

T1

A 24-channel PCM channel wire or cable transmission medium operating at a rate of 1.544 MB/s.

TMS NCT Link (TMSLNK)

See NCT.

Telephone Number (TN)

A 7-digit telephone number made up of a 3-digit central office code and a 4-digit station number. It is also called a Dialing Number (DN).

Telephone Equipment Order (TEO)

The order to Lucent specifying equipment required to construct the desired switch office.

Teletypewriter (TTY)

An output device used to print information within the switch in a legible form. It is an outmoded term from a time when teletypewriters were the only visual output device.

Teletypewriter Controller (TTYC)

The output port that sends data to the TTY device.

Terminal Equipment Number (TEN)

A 7-digit number used in translation to identify the location of a DCLU channel or trunk circuit.

Terminal Process

A software process in the SMP which controls a terminal (line, trunk or channel) during a call or call attempt. The terminal process is created and exists only as long as the terminal it controls is active.

Time Division

A method of serving a number of simultaneous calls by assigning different time slots through a switching network to those calls. The TSI does time division switching.

Time Slot Interchanger (TSI)

An equipment arrangement in the SM that takes information coming to it or from the TMS and switches it onto the time slot corresponding to the line or trunk involved in the call.

Time Slot Interchange Unit (TSIU)

The TSIU is the part of the SM that performs time slot switching. The TSIU consists of a TSI, data interface, dual link interface, control interface and signal processor.

Time-Multiplexed Control Unit (TMCU)

The Time-Multiplexed Control Unit (TMCU) is a single-shelf assembly that terminates Network Control and Timing (NCT) links from the Message Interface Clock Unit (MICU) and is equipped with the overall control circuit packs for the Time-Multiplexed Switch (TMS). Positions are provided for seven control and interface packs in addition to space for two power converters.

Time-Multiplexed Switch (TMS)

The TMS, one of two switches that comprise the CM1, performs the time-shared space division switching such as voice and data between any two SMs or between an SM and the AM. The MSGS is the other switch in CM1.

Time-Multiplexed Switch Unit (TMSU)

Circuitry within the TMS that terminates 30 NCT links and performs space switching of the time slots received.

Time-Multiplexed Switch Unit Model 2 (TMSU2)

This is a version of the TMSU which breaks down further into replaceable FRUs. TMSU2 units cannot be mixed with TMSU3 units in the same cabinet.

Time-Multiplexed Switch Unit Model 3 (TMSU3)

This is a version of the TMSU which is functionally identical to the TMSU Model 2, but has fewer physical components. TMSU3 units cannot be mixed with TMSU2 units in the same cabinet.

Tone Decoder (TD)

The TD resides in the LDSU of the SM and performs digit reception and decoding functions for dial pulse and touch-tone originating calls from lines.

Traffic Measurements

These measurements provide the current status of the 5ESS[®]-2000 switch as well as indications to support the switching system with additional resources.

Transmission Multiplexer (TMUX)

The TMUX performs the format conversion of data between one STSX-1 link and 14 BPIDB structures, which includes the mapping of data time slots between the two formats and signaling bit format conversion. It also performs functions associated with terminating the STS-1 SONET and facility overhead which include: STS-1 line and section overhead termination; STS-1 path overhead termination and Virtual Tributary (VT) extraction; DS1 framing and extraction; detection of DS1 facility alarms; DS1 Cyclic Redundancy Code (CRC) checking; DS1 Facility Data Link (FDL) extraction; initial collection of STS-1 and DS1 performance monitoring data and facility data alignment to the system clock.

Trunk

The facility between two different entities, such as central offices and sections of the same switching system, that is used for transmission and/or signaling.

Trunk Circuit

The trunk circuit of a switching system is used to supervise a connection within the system and/or to associate the system with a transmission facility or another switching entity.

Trunk Unit (TU)

Hardware that terminates 64 local or toll interoffice analog trunks without concentration. A minimum of one is required for each office.

Trunk and Line Work Station (TLWS)

Provides local access for lines and trunks, an interface for circuit administration and supports portable testing equipment for the switch.

Tuple

A row in a data table (relation).

Two-Mile Optically Remoted Module (TRM)

An SM located up to 2 miles from the CM and connected by a multimode optical fiber that serves as an extended NCT link.

Two-Party Service

Provides telephone service to a maximum of two customers on a common terminal appearance on the network.

Uniform Call Distribution (UCD)

A type of line hunting providing an even distribution of incoming calls among the available members of a hunt group.

Universal Conference Circuit (UCC)

A service circuit (3- or 6-port) used to connect 3 to 6 customers for service features.

Universal Tone Decoder (UTD)

Decodes dial pulse, multifrequency and touch-tone signals.

Universal Tone Generator (UTG)

Creates digital tones for touch-tone, busy tone, dial tone, and multifrequency.

Video Display Terminal (VDT)

A VDT is a nonmechanical output device, such as a Cathode Ray Tube (CRT) monitor or Liquid Crystal Diode (LCD) screen common to personal and laptop computers.

Voice Path Assurance (VPA)

A test providing a voice path for common channel signaling trunks. This test ensures the integrity of the voice path since the voice and signaling paths are separated on CCS trunks.

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