

**200-LINE SWITCH UNIT
DESCRIPTION OF SYSTEM OPERATION
NO. 101 ELECTRONIC SWITCHING SYSTEM**

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D. Duplication of Line and Attendant Number Translators	49	1.02 The major functional requirements of the switch unit are to provide:	
E. Scanner Circuit Duplication and Switching	49	(a) Suitable terminations for station lines and the various types of trunks.	
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down in response to directions received from the control unit. The control unit is guided in its actions by messages received from the switch unit whenever a line or trunk changes its supervisory state from on- to off-hook or vice versa. In the initial stage of a station originated call, dial pulses are transmitted as transients through a time division channel set up temporarily to a digit trunk where they are converted to tone spurts for retransmission to one of the centralized digit receivers at the control unit. TOUCH-TONE signals traverse a similar path without alteration. Ringing voltage, when required, is applied in the station line circuit under control of a signal received over a time division connection from a source provided for this purpose.

1.04 Speech transmission for the attendant is provided by a time division connection in the usual way. Signals for controlling her console lamp indications are derived from data messages received from the control unit. Console key operations are detected and treated as off-hook supervisory signals and transmitted to the control unit for interpretation.

1.05 The time division network, as a whole, has a capacity for 50 time slots. Thus, if traffic requires it, 50 simultaneous connections could be established for serving a maximum of 200 stations. The network is divided into two parts, each containing a time division bus so that, in case of trouble, the affected half can be taken out of service. Service will be maintained by the other half on a reduced traffic capacity basis for the duration of the difficulty. Each line, trunk, etc, has access to each of the two time division buses.

1.06 The service status of the two parts of the switching network, as well as that of certain other redundant features, is under direct control of a transfer and alarms circuit. This circuit can effect service-maintaining changes when it receives certain local indications of trouble or when it receives a message from the control unit. The latter continually establishes various test call connections at the switch unit and is immediately informed of any difficulty in the common equipment of the switch unit.

2. CIRCUITS AND METHOD OF OPERATION

A. Basic Circuit Elements and Purposes

2.01 The basic organization of switch unit circuits is shown in Fig. 1. In general, this is limited to a *half system*, that is, it shows one time division bus and one set of controls for it, one scanner circuit, etc. A similar layout is referred to later showing the complete dual system (Fig. 13). The functions of the major circuits are as follows.

2.02 *Line Circuit:* The circuit known as the line circuit or station line circuit consists of line transformers, low-pass filters, talking gates, ringing gates, and scanning gates. The line transformers serve to connect the balanced subscriber lines to the unbalanced switching network and to provide a method of feeding subset direct current to the lines. Talking gates respond to pulses from line number and attendant number translators and close a low impedance path from the low-pass filters to the common talking buses. Ringing gates apply 20-cycle ringing signals to the tip side of the line in response to a small positive dc signal received over the time division switch. Scanning gates measure the level of direct current in the subscriber loop in response to interrogation pulses sent to it by the scanner circuit. Thus, the scanning gate indicates whether that station is off- or on-hook.

2.03 *Switch Store and Clock:* To set up a conversation between two subscribers, the two line circuit time division gates associated with one of the talking buses are operated simultaneously and repetitively for short intervals during one time slot interval. This is done by writing the numbers of the selected gates side by side in one word in a high speed sequential access memory, the switch store. This memory device is a magnetic type (ferrite core) storage array using coincident flux for reading and writing. As the two line numbers are read out of the memory, they are translated as pulses onto the proper A (calling party) and B (called party) leads to actuate the line circuit talking gates. Additional line-to-line conversations may be provided for by having other pairs of gate (line circuit) numbers written into other words (time slots) of the switch store. The clock drives the

switch store through its cycling (reading time slots in sequence) and provides timing for other circuits.

2.04 Line Number Translator: The translation of line numbers as they are read out of the switch store is accomplished by the line number translators in two stages. First the 8-bit binary A party or B party numbers are each split into 4-bit numbers. Then each 4-bit group is translated to 1-out-of-16 possible leads going to a separate vertical and horizontal access row of 16 by 16 diode matrices. At the intersections within the matrices, connections are made to the time division gates of various circuits (line, trunk, etc). A signal on one horizontal and one vertical is required to close the time division gate at a cross point.

2.05 Data Distributor and Data Receiver: The data distributor is a shift register which receives information from the data receiver serially in binary form. Its function is to transfer the information in parallel paths to other switch unit circuits, namely, the switch store, the attendant circuit, or the transfer and alarms circuit. The data receiver, which furnishes this message, is an FM detector used to demodulate messages received from the control unit and convert them to dc pulses for use by the data distributor.

2.06 Scanner and Data Transmitter: The scanner circuit is a high speed monitoring circuit which interrogates the supervisory states of lines, trunks, attendant pushbuttons, and alarms. It reports to the control unit any changes in the states of these circuits. The comparator circuit in the scanner is a device which indicates when a difference in state exists between any two successive scans of the same line, trunk, etc, circuit. It is the output from the comparator which causes the scanner to make up a message giving the control unit a report on off-hook and on-hook activities in the switch unit. This message, in binary form, is sent to a data transmitter which is a frequency shift keying modulator where the dc pulses are converted to FM signals for transmission to the control unit.

2.07 Ring-Ringback Logic: This is a circuit composed of pulse-combining gates to produce a variety of pulses used to time ringing and ringback signals. Groups of staggered sig-

nals, needed to produce four phases of "1 second on, 3 seconds off" ringing periods, are developed by combining slow (15 and 30 ipm) pulses from an interrupt generator with fast (12.5 kc) pulses from the switch store binary counter. The staggered signal is combined with a binary bit of ringing information (continuous or interrupted ring) from the switch store, another pulse from the binary counter, and a timing pulse from the clock circuit. The output leads control the ring-ringback drivers in the line number translator circuit. These drivers close time division gates to connect the ring and ringback signals to the B and A parties, respectively, during the assigned time slot interval. Other output leads control the main function of the line number translator circuit; ie, the translator talking path function is disabled when the ring bit is present and enabled when the ring bit is not present. The ring and ringback connections are made on alternate read outs from the switch store to eliminate the need to occupy two time slots.

2.08 Digit Trunk: The digit trunk circuit serves to connect its associated digit pair to any station for digit signaling to the control unit. This is accomplished by making the digit trunk circuit a part of the time division switching network. The digit trunk number, assigned by the control unit, appears in the B party portion of the stored message in the same time slot occupied by the calling A party. TOUCH-TONE stations pulse directly through the digit trunk circuit on a time division basis, and, after filtering, on to the digit pair. However, rotary dial station dc pulses, after filtering, are converted to a pair of tones before transmission to the control unit on the digit pair. This particular pair of tones is recognized by the control unit where the tone bursts are counted rather than decoded as in the case of TOUCH-TONE dialing.

2.09 Central Office Trunks: These are similar to line circuits in that they serve to connect the balanced central office trunk pair to the unbalanced switching network and convert voice signals into time division pulses. However, there is no requirement for ringing. Scanning supervision is also similar to the line circuit operation except that an incoming central office call causes the control unit to place dc on both tip and ring of the incoming trunk pair to the switch unit. This is equivalent to a line circuit going off-hook.

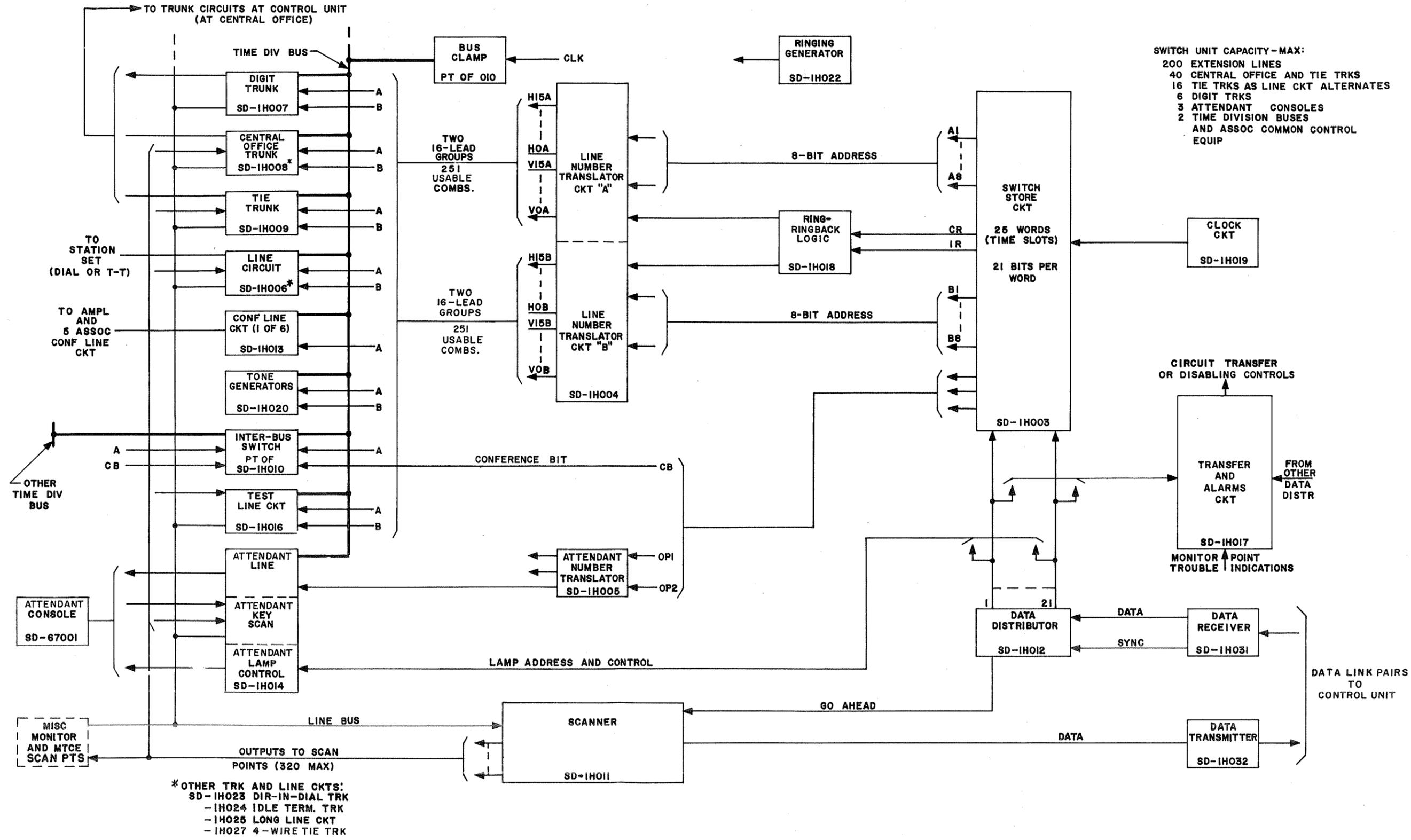


Fig. 1 - Switch Unit Block Diagram

2.10 Attendant Circuit and Translator: The attendant circuits provide the memory and translations required to light lamps on the attendant console. In addition, talking (line) circuits are provided for each of the attendants to permit time division connections to the talk buses. Scan point networks monitor the state of all console keys. Interrupt generators provide fast flashing, normal flashing, and winking pulses to drive the lamps and audible tones. The attendant number translator is much simpler than the circuitry and operation of the line number translator since it must only make a 1-out-of-3 choice of attendants from two binary bits. Only a single stage of translation is needed for this simple function.

2.11 Transfer and Alarms Circuit: The function of the transfer and alarms circuit is to activate and deactivate (under certain cases of equipment failure) various switch unit circuits by putting them under the control of messages received from the control unit. It also transmits alarms by way of the scanner circuit. Indicator lamps are provided to display the status of various on-line (in service) or off-line (out of service) equipment. Keys are also provided to permit manual simulation of transfer messages in order to conduct local maintenance test routines.

B. General Method of Operation

2.12 A brief description is given here of circuit operations. A more detailed study of the circuits will be undertaken in the following subdivisions of this section.

2.13 In Fig. 1, all line circuits, trunk circuits, etc (located in a vertical column at the left) have access to each other through the common time division bus. These are constantly interrogated for changes in their supervisory state by a scanner circuit. This is done through the scanner output connections to 320 points as shown. A common return connection is made to the scanner from each of these circuits over the line bus. The circuits are scanned sequentially at approximately 40 times per second.

2.14 In a station-to-station call (A party to B party) the A party in originating a call causes the following series of events:

- (1) The scanner, while looking at all of its monitored circuits one by one, detects the receiver off-hook condition and stops.
- (2) During this pause, a message is made up by the scanner to give the central office control unit identification of the line circuit and the off-hook state. This message is passed to the data transmitter where it is sent over the data link pair to the control unit.
- (3) A reply message from the control unit is received by the data receiver and fed into the data distributor. The message includes the address of the A party and the address of an idle digit trunk circuit.
- (4) The data distributor distributes parts of the reply message to the switch store for use by the line number translators.
- (5) The data distributor writes the A party number and the digit trunk number into the chosen time slot in the switch store.
- (6) The line number translators cause the calling line and the digit trunk to be connected together in the same time division bus.
- (7) At the control unit, a digit receiver is connected to the digit trunk. This supplies dial tone to the digit trunk.
- (8) The A party now hears dial tone and dials his desired destination using a rotary or TOUCH-TONE dial set.
- (9) Translation of the dial pulses at the control unit causes another message to be formed which is transmitted by the control unit to the switch unit data receiver. It then fills the data distributor and passes on to the same switch store time slot as the previous message occupied.
- (10) In the new message, the call processor of the control unit replaces the digit trunk address with that of the called station (B party).
- (11) Included in this message is additional information which activates the ring-ringback logic circuit and provides B party ringing and A party audible ringback signals on alternate passes through the time slot. Both signals are activated by a tone generator circuit which is also a source of busy tone.

(12) In answering an incoming ring, the B party's off-hook electronically opens the ringing generator lead within its own line circuit, thereby removing the 20-cycle ringing voltage from its line loop. At the same time, the scanner detects this off-hook, stops, and transmits a message to notify the control unit that an off-hook has occurred.

(13) From information in its memory, the control unit notes that a complete talking condition is to be satisfied. In its reply message to the switch unit, the ringing bits are removed. All other message information remains intact. Now the line number translators cause the A and B party line circuits to be connected together in the time division bus. Thus, both parties have their time division gates closed simultaneously and the talking connection is complete. The switch store continues to provide both line addresses to the line number translators to keep them linked by time division switching throughout the remainder of the talking connection.

(14) At the termination of a call, both station line circuits, upon hanging up, cause scan point changes. This results in two scanner messages notifying the control unit of these changes. Interpreting the changes as on-hooks by both parties, the control unit reply message will cause the switch store time slot to be wiped clean. This completes the disconnect operation.

C. Important Auxiliary Features

2.15 The operation of other types of switching circuits such as the central office trunks, the various tie trunks, long line circuits, and test line circuits, involves similar action by the controlling circuits just covered in the station-to-station call.

2.16 The attendant circuit performs four major operations.

- (1) Selects attendant key position (loop) for display of visual signals.
- (2) Activates common lamps to cause attendant actions.
- (3) Enables the attendant line circuit (talking connection).

(4) Creates primarily off-hook signals in response to the operation of the attendant keys, each of which changes the condition of an assigned scan point.

2.17 The attendant number translator will select one of the three possible attendant consoles as directed by the control unit just as the line number translator selects one of the many line or trunk circuits.

3. LINE CIRCUIT SIGNALING FEATURES

A. General

3.01 The fundamental signaling features in the switch unit may be understood with the help of Fig. 2. Only three of the circuits already mentioned are shown: line circuit, digit trunk circuit, and tone generator circuit. These particular circuits are directly related to station ringing, digit signaling (dialing), and ring enabling and audible ringback tone, respectively.

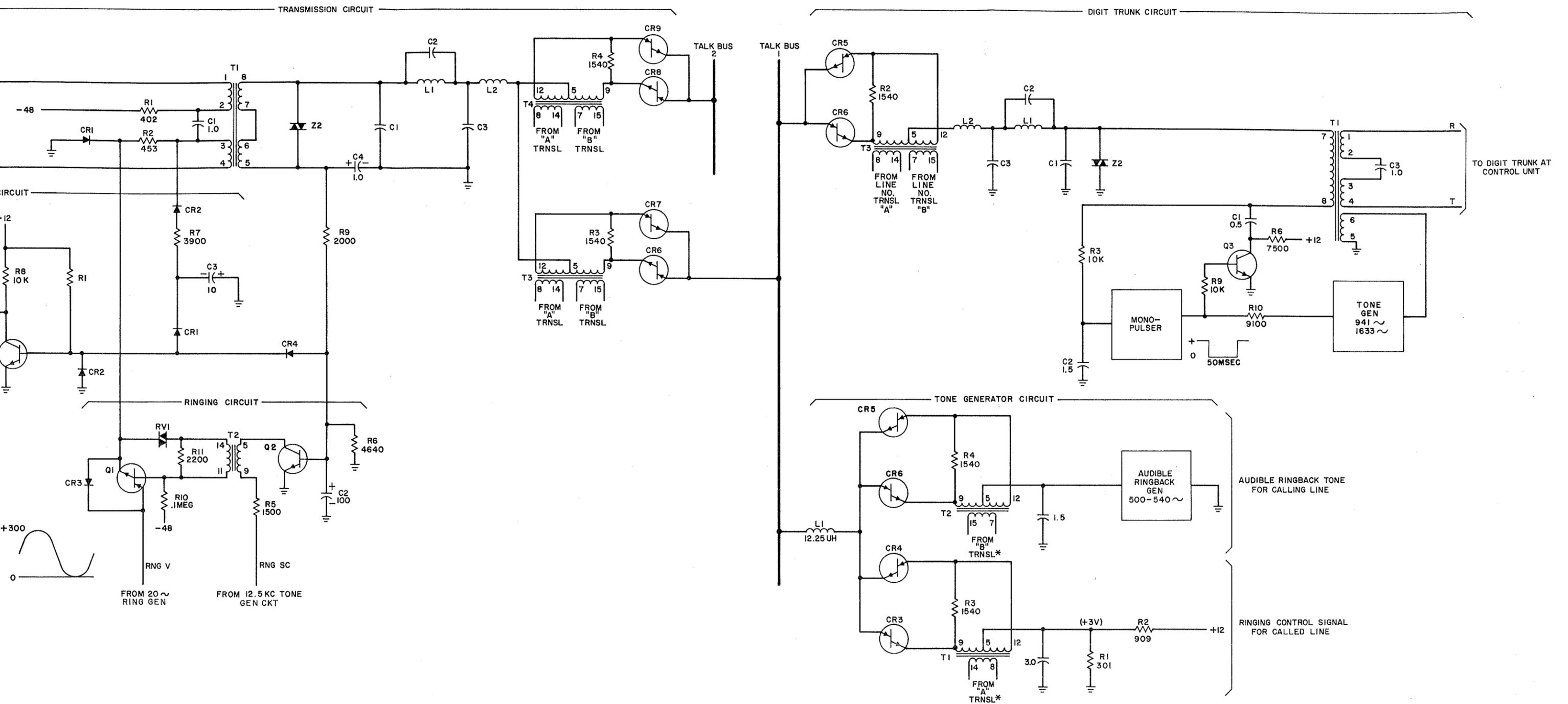
3.02 The transmission circuit shown in Fig. 2 is connected to talk bus 1 through the time division gate comprised of CR6 and CR7 and through pulse transformer T3. This connection is duplicated by CR8, CR9, and T4 to talk bus 2. The digit trunk and tone generator circuits also have duplicate gates and transformers which are not shown in this figure. This feature of equipment duplication will be discussed in 11. **DUPLICATION OF CONTROL CIRCUITS.**

3.03 In discussing signaling details, a study of the various sections of the circuits in Fig. 2 will be helpful. The circuit functions are comprised of five major parts which are listed below and expanded in paragraphs to follow.

- (1) Transmission.
- (2) Supervision
- (3) Ringing
- (4) Dialing
- (5) Tones

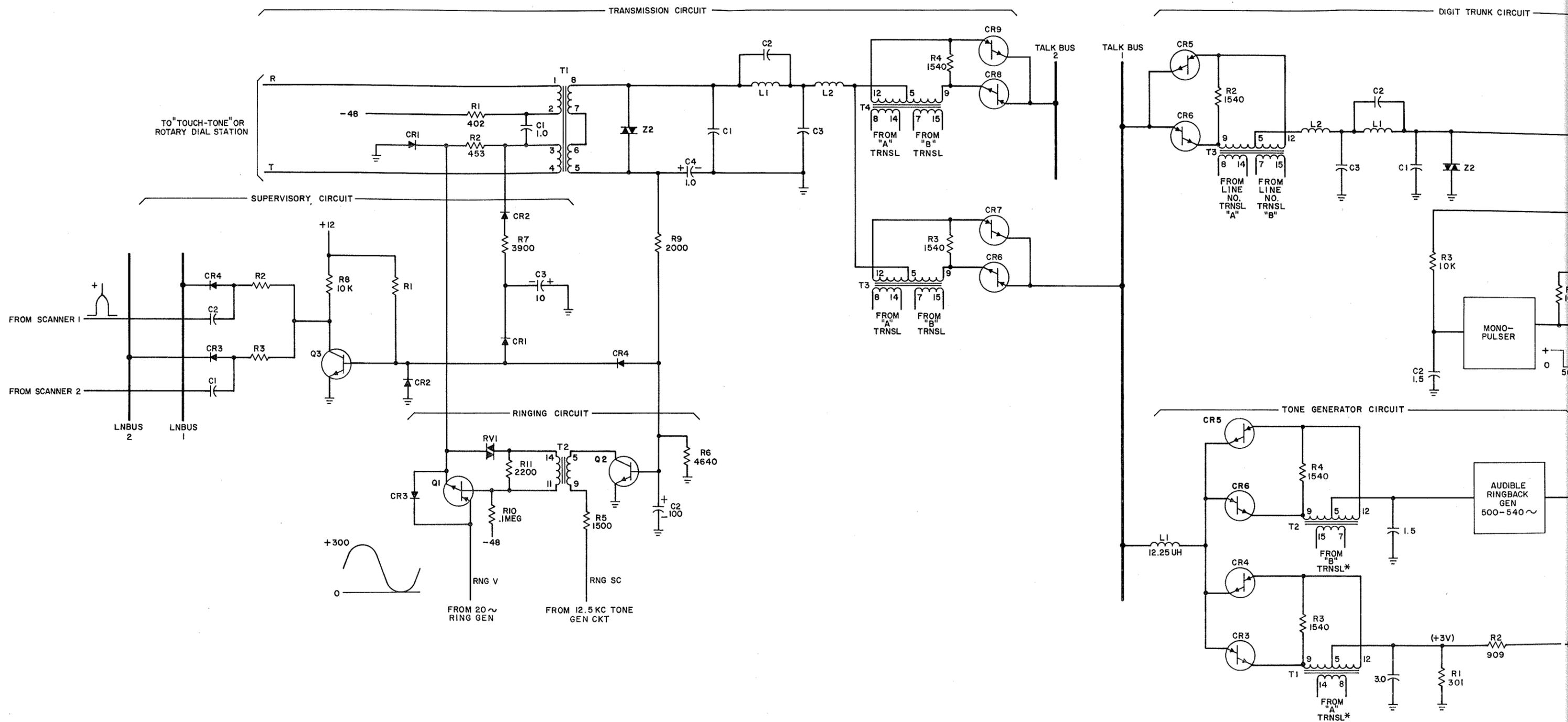
B. Transmission

3.04 The transmission circuit connected to talk bus 1 consists of a loop network and matching transformer (T1), a low-pass filter



* NOTE: THE TONE AND DC RINGING CONTROL SIGNALS ALTERNATE IN THEIR USE OF THE TIME SLOT ASSIGNED FOR THE "RINGING" FUNCTION.

Fig. 2 - Line Circuit Signaling Detail



* NOTE: THE TONE AND DC RINGING CONTROL SIGNALS ALTERNATE IN THEIR USE OF THE TIME SLOT ASSIGNED FOR THE "RINGING" FUNCTION.

(L1, L2, C1, C2, and C3), and a pair of fast switching diodes (CR6 and CR7) which are energized by a pulse transformer (T3). The low-pass filter, switching diodes, and pulse transformer are the basic components used in the principle of time division switching which is treated in more detail in other practices.

3.05 In Fig. 2 the line circuit receives dial tone which is supplied to the digit trunk circuit over the digit pair from the control unit. In return, the dial pulses from the line circuit station are transferred to the digit trunk circuit. Both signals are exchanged by time division switching facility.

C. Supervision

3.06 The supervisory circuit provides a means by which the condition of a line loop (whether it is in the on-hook or off-hook state) may be observed by a monitoring circuit, the scanner. A diode network CR4, C2, and R2, which is called the scan point, connects the line circuit with the scanner memory array. (See Fig. 3.)

3.07 The condition of the supervisory transistor (Q3) is determined by the on-hook or off-hook condition of the line. The absence of a voltage drop across resistor (R2) in the transmission circuit (on-hook condition) will bias the transistor (Q3) into conduction and block the flow of an interrogating pulse from the scanner through the scan point. The success or failure of the passage of this pulse allows the scanner to know whenever a change of state occurs in the line loop.

D. Ringing

3.08 The time division gates are not designed to pass ringing power; therefore, a method of connecting the ringing supply directly to the line circuit was devised. A special triode switch (Q1) is used to gate the 20-cycle generator to the line loop. Since the time division gates will pass a direct current signal of sufficient potential to trigger the transistor (Q2) into conduction, a dc potential (+3V) is time division-connected (via CR3 and CR4 of the tone generator circuit) to the line circuit when ringing is required.

3.09 With the transistor (Q2) conducting, transistor (Q1) is also turned on by the ring synchronizer (RNG SC) signal from the tone generator circuit as shown in the ringing circuit section. The transistor (Q1) is triggered by the induced voltage across the transformer (T2). This voltage has as its source the 12.5-kc oscillator (not shown) in the tone generator circuit. This 12.5-kc tone, rather than a dc signal, is used to trigger transistor (Q1), because an ungrounded switch is required. As the closure is made through transistor (Q1), a 20-cycle generator is connected to the tip side of the called party loop to ring the subset. A 1-second ringing, 3-second pause is the ring cycle used.

E. Dialing

3.10 Stations having either standard rotary dials or TOUCH-TONE dial sets may be used with No. 101 ESS switch units.

3.11 When a rotary dial is used, the dc pulses in the primary winding of transmission circuit transformer (T1) induce transient pulses into the secondary winding where they are shaped properly and time division-connected to the digit trunk circuit. Here the pulses are stretched (in the monopulser) and converted into two special (MF) audio tones (using the generator frequencies of 941 and 1633 cycles). This is the special pair of tones which the digit receiver recognizes as coming from a rotary dial.

3.12 In the case of a TOUCH-TONE dial set, each of the dial buttons activates a different combination of two audio tones which, although they are time division-connected to the digit trunk circuit, are induced directly from T1 of the transmission circuit through T1 of the digit trunk circuit on to the control unit without appreciable loss.

F. Tones

3.13 An audible ringback tone is time division-connected to the calling party. This is alternated with the dc ringing control signal to the called party. These two operations occur in the same assigned time period but during every other cycle of that time period. In other words, at a first sampling of the time slot (as the assigned time period is called), the called party will be connected with the dc ring enabling sig-

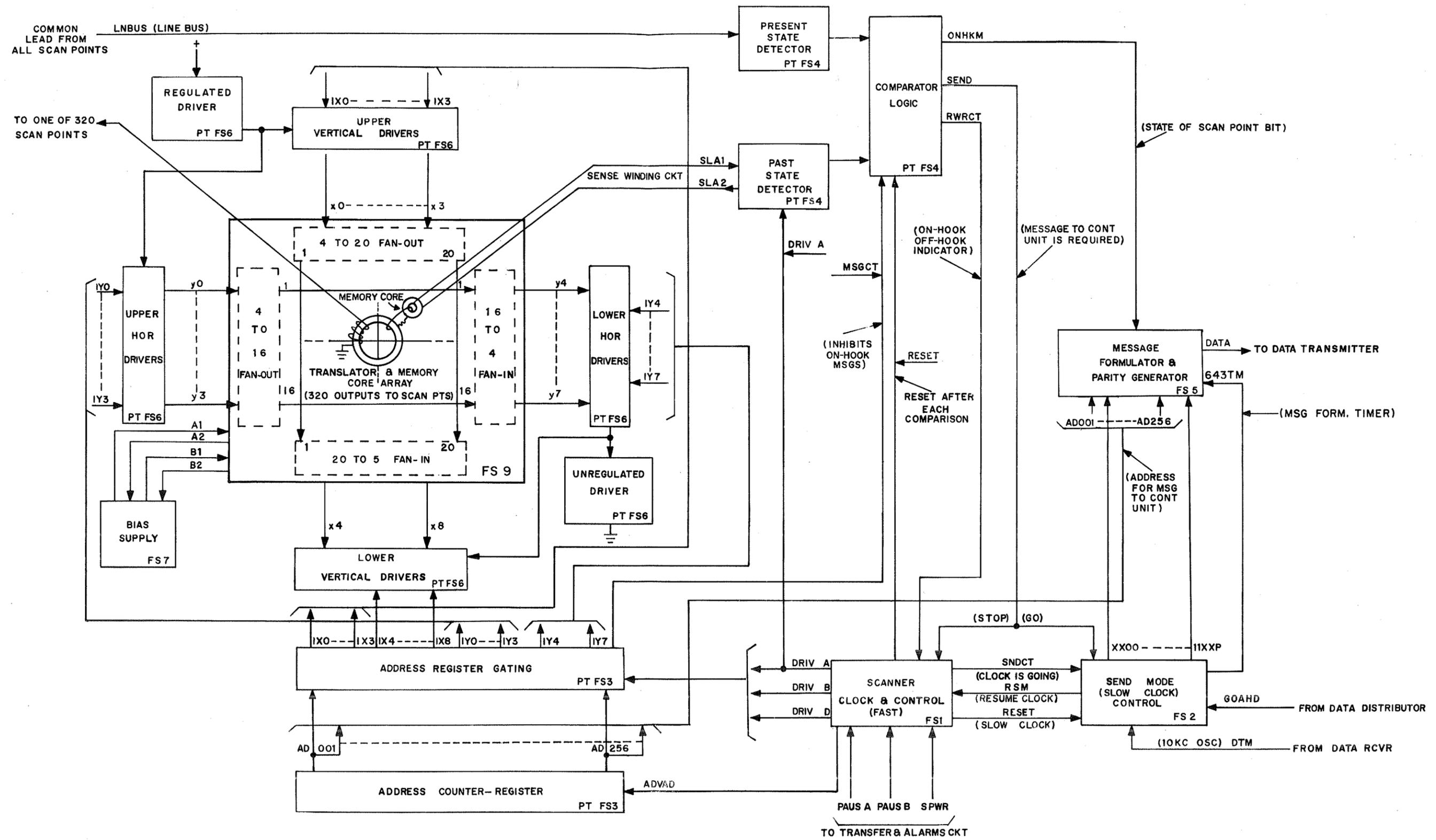


Fig. 3 - Scanner

nal. At the next sampling of the time slot the calling party will be connected with an audible ringback tone. This interchange of signals is controlled by the ring-ringback logic circuit acting through the line number translator circuit. Further details of these operations will be forthcoming under the headings indicated.

3.14 The digit control circuit in the control unit distinguishes between TOUCH-TONE and rotary dialing, but as far as the switch unit is concerned either type dial may be used without modification to the switch unit circuitry.

3.15 Not shown in Fig. 2 is a section of the tone generator which is devoted to the production of a busy tone. This portion of the tone generator consists of oscillators producing 500-cycle and 620-cycle tones combined to give the effect of a 500-cycle tone modulated by a 120-cycle note. This portion also consists of a gate to control the output with a pair of time division switches to couple to the talk buses for connection to circuits requiring a busy tone. The interrupt gating signals (60 or 120 ipm) for this busy tone are obtained from the interrupt generator in the attendant circuit.

4. SCANNER CIRCUIT

A. General Description

4.01 The scanner circuit can be considered as the eye of the switch unit. It continually monitors the on-hook or off-hook status of all line, central office, and tie trunk scan points as well as attendant operations and alarm circuits in the switch unit. It formulates and sends to a data transmitter serial messages concerning any change in state of 320 scan points. Two identical but independent scanner circuits are provided in each switch unit. The output of one or the other can be selected by messages from the control unit.

B. Memory

4.02 The scanner contains a memory array composed of a translator and a memory core for each of 320 individual scan points as indicated in Fig. 3. In order to have current flow in the vertical direction through any given

translator core, both corresponding upper and lower vertical drivers must be turned on. Similarly, horizontal current flow requires turning on both upper and lower horizontal drivers. Fig. 4 shows a slightly more detailed sketch of the scanner memory module. The drawing does not show that the drive and bias windings are four turns each while the output winding to the scan point is six turns. Sufficient drive must be applied to overcome the bias on any translator core so that it can be switched. The flux change in the translator core being switched is coupled via a one-turn winding to the associated memory core, causing it to switch if the previous state had been a 1 or to be undisturbed if the previous state had been a 0. At the same time that the translator core is switched, transformer action produces an 8-volt interrogation pulse at the output winding. All 320 translator-memory cores are accessed sequentially by providing the proper combinations of inputs to 17 drivers.

4.03 All but a few of these memory cores must be capable of being set to a 1 (off-hook) or a 0 (on-hook). The cores which are not allowed to store a 1 will be discussed later. If the memory must have a 0 written into a particular core, the upper Y driver is turned off first by DRIVA, then the upper X driver by DRIVB, and the lower X and Y drivers are turned off last by the normal change of state of the address counter register as it advances to the next address. This allows the translator core to lose drive current slowly. The flux change will be correspondingly slow and will not develop a large enough current pulse to set the memory core to a 1. If the memory must have a 1 written, all lower drivers are simultaneously turned off before the upper drivers by an overriding pulse called DRIVD. This pulse will be present only when writing or rewriting a 1. When all drive currents abruptly stop, the translator core returns to its normal bias state quite rapidly. The resulting rapid flux change couples a large current pulse to the memory core, overcoming the bias in its sense winding and causing it to switch to a magnetic 1 state.

C. Clock, Address Counter-Register, and Address Register Gating

4.04 In Fig. 3, the scanner clock (multivibrator) operates at a base frequency of 75 to 80 kc. The output is shaped in a squaring gate

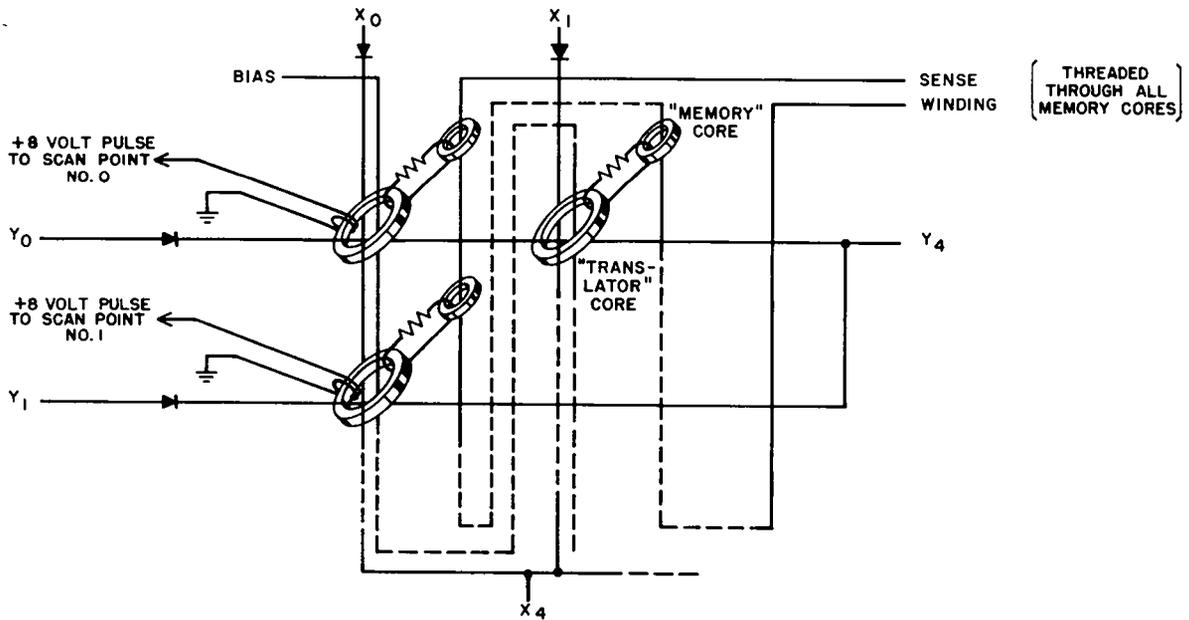
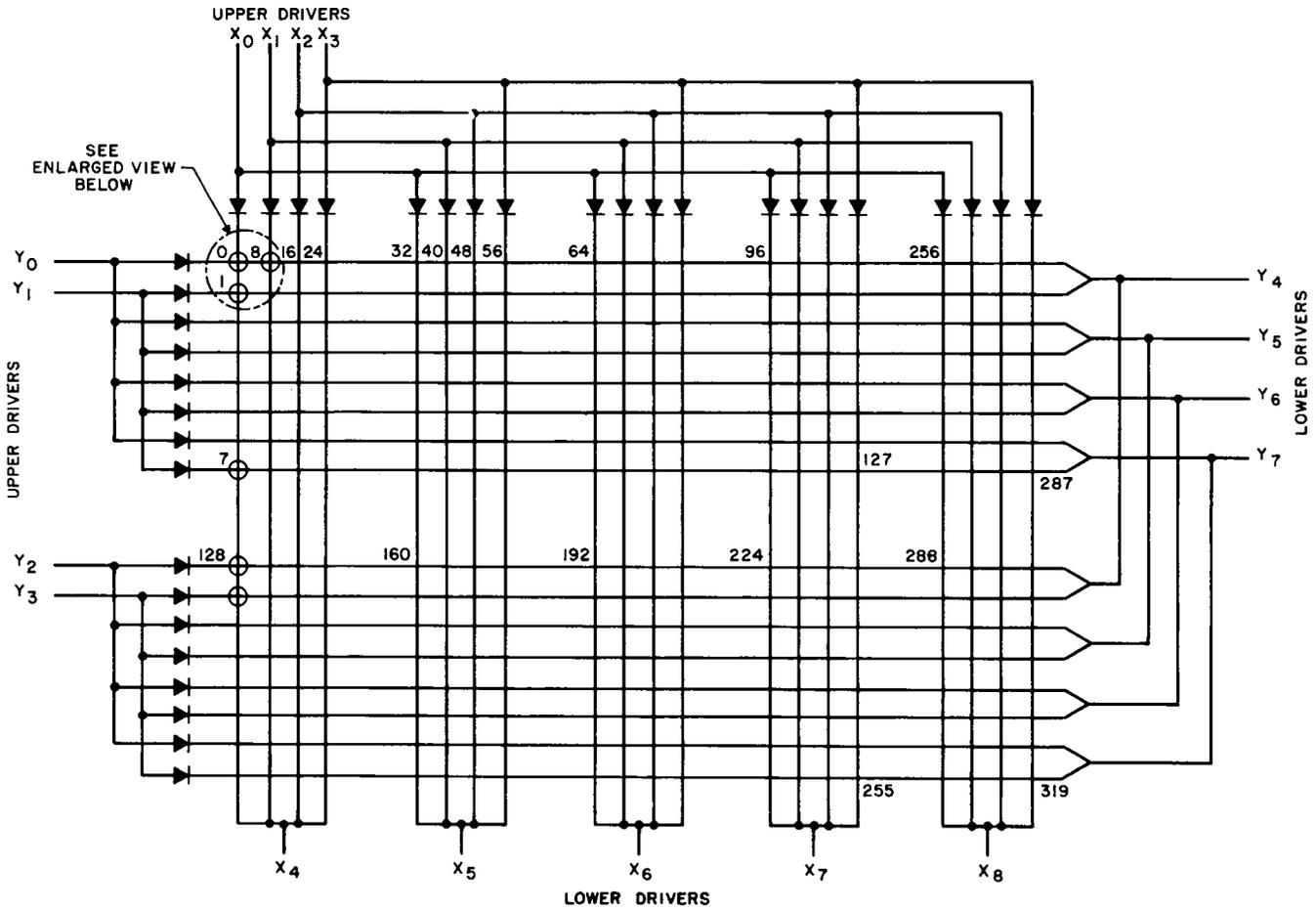


Fig. 4 - Memory Array Detail

which can be inhibited when it becomes necessary to stop the clock. This will occur whenever a message is to be sent to the control unit or when a transfer from one scanner to the other is demanded by the control unit. A 2-stage binary counter produces the outputs required to develop all of the scanner timing pulses. One of the timing pulses (ADVAD) is taken from the output of the second binary counter and therefore has a rate of approximately 20 kc. It is used to advance a 9-stage binary counter in order to sequentially address each scan point. The outputs of the counter are the logic inputs to the ADDRESS REGISTER GATING which translate to 4-out-of-17 for each of the memory addresses. Additional inputs to the register gates are the timing pulses DRIVA, DRIVB, and DRIVD.

D. Past and Present State Detectors

4.05 These two circuits will be described under one main heading since the concept of their operation depends upon an understanding of the timing of their respective inputs and consequently of their outputs which are compared in the comparator. Basically, the two circuits operate the same. They both develop output pulses only for off-hook inputs. Recall that whenever a translator-memory core combination is accessed, two simultaneous outputs are produced (to the scan point and to the memory core). The translator core output is sent to its associated scan point, and a signal will return on the scanner line bus only if the scan point is off-hook (Fig. 2 and 3). Assume it is off-hook and that it has been for at least the previous scanner cycle. Therefore, the memory core output pulse on the sense winding is present, indicating an off-hook state for the previous look at the scan point. This pulse appears on the input to the past state detector at the same time that the interrogation pulse appears at the present state detector. The outputs of the two circuits will occur simultaneously. The DRIVA input to the past state detector enables it only during the times when each sense core in the memory module is about to be read out in order to prevent random noise from producing false ones (1s).

E. Comparator

4.06 This circuit compares the outputs of the present and past state detectors. The comparator will detect a match or mismatch between

the outputs of the present and past state detectors for each scan point as the scanner cycles through its memory. It is reset just prior to accessing each scan point to allow successive comparisons. The comparator produces three outputs relating to any scan point state. Output lead RWRCT will go to ground only when the present state detector indicates off-hook. This allows DRIVD in the clock to pulse and, as explained earlier, DRIVD will override DRIVA and DRIVB causing a 1 to be written into the memory core. Whenever a scan point changes from on-hook to off-hook, lead ONHKM will go to ground. Conversely, if a scan point changes from off-hook to on-hook, lead ONHKM will be positive. If the comparator matches, no messages will be sent, but if a mismatch is produced between the past and present states of any scan point, the SEND lead will go to ground causing the scanner clock to stop. This will stop the address counter-register which will then contain the scan point address where the mismatch occurred. The scan point address in binary is fed from the address counter-register to the message formulator which also receives the state of the scan point (on-hook or off-hook) from the comparator via the lead ONHKM.

4.07 The message control (MSGCT) lead performs an inhibiting function. As mentioned earlier, a few scan points are inhibited from sending on-hook messages. Examples are: attendant console keys, clock failure, ring generator failure, blown fuse, parity failure alarms, and transfer verify indicator. When these *momentary impulse* scan points are addressed, the MSGCT lead is made positive. This is necessary because the operation of a nonlocking key at the attendant console (as an example) will, at one instant, give the scanner an off-hook indication and at the next instant (when the key is released) give an on-hook signal. It is this change to the on-hook condition that is not desired and therefore inhibited. A translation of the scan point binary number results in a positive signal on the MSGCT lead for those scan points not requiring on-hook messages. This translation takes place in the scanner address register.

F. Message Formulator

4.08 This circuit consists of 12 gates combined in an *or* function. The inputs of 9 of these gates are the leads which define the binary ad-

dress of the scan point. The tenth lead is ONHKM. One gate is used to gate a message start pulse and one is used to provide proper parity (odd). Parity is determined by counting the number of ones in any message as it is being sent. If the total number is even, a parity bit is generated. If the total number is odd, the binary counter will inhibit sending a parity bit.

G. Send Mode Control

4.09 This circuit requires several inputs in order for it to operate. The SEND lead which stops the scanner clock also removes an inhibiting potential to this circuit. In addition, the lead SNDCT must be at ground, indicating that the scanner clock has stopped. The go-ahead (GOAHD) lead goes positive as a result of a message sent from the control unit, indicating that the last message sent was received. In the event that the previous message was lost, the function of GOAHD would be assumed by a less frequent pulse from a built-in long period timer (1/2 second). When all input conditions are met, the send mode control circuit provides 11 binary counter outputs to the message formulator and parity generator. The binary counter is driven by a 10.294-kc reference frequency from the data receiver. A logical translation of the signals on the output leads is done in the message formulator causing serial messages to be sent at a bit rate of 643 cps.

5. DATA DISTRIBUTOR CIRCUIT

A. General Description

5.01 The data distributor (Fig. 5) is basically a shift register which receives a 47-bit serial message from the control unit.

B. Data Sequence Circuit

5.02 Data messages entering the distributor are in serial form. The incoming bit rate is 735 cps. A 5- μ sec synchronizing (SYN) pulse developed from the frequency shift data messages received by the data receiver also appears at the input to the distributor. One SYN pulse is present during each 1.360-msec bit period. It is this shift pulse which gates the serial message from stage to stage in the shift register.

5.03 The ones in all incoming messages are regenerated by a 50- μ sec monopulser as a requirement to the proper operation of the shift register stages. The regenerated message is then fed directly to the last stage of the register. The arrival of the first two bits (always ones) of all messages at the first and second stages of the register indicates that the first 32 bits of the 47-bit message fully occupy all 32 stages. At this time the sequence circuit begins a delay period of 100 μ sec. If the contents of the register, for one reason or another, have not been accepted (by the switch store or attendant circuit, etc) within 100 μ sec, the shift register will be reset in a special mode to accept the last 15 bits of the incoming message. This is done by inserting two new start bits and a time slot address of 0 into the shift register 15 stages from their final positions. When the last 15 bits of the message shift 15 stages into the register, all desired bits will be in the appropriate stages. At this time the 100- μ sec delay period starts again and at its conclusion all shift register stages are reset to 0.

5.04 The data sequence circuit also counts parity of all incoming messages. If the parity of any incoming message is even, the message will not be allowed to proceed to its destination. Instead, the data sequence circuit will cause the shift register to be reset to 0, thereby dumping the bad parity message.

C. Shift Register

5.05 The shift register is composed of 32 stages. It is possible to use a 32-stage shift register to receive a 47-bit message because of the character of all messages. The first 32 bits of all messages contain information destined for one of three major units.

- (1) The switch store
- (2) The transfer and alarms circuit
- (3) The attendant circuit

The last 15 bits of an incoming message always contain attendant console lamp information. There is sufficient time in a bit interval (1.360 msec) to distribute and use the first 32 bits, clear the register, and still accept bit number 33 into the shift register.

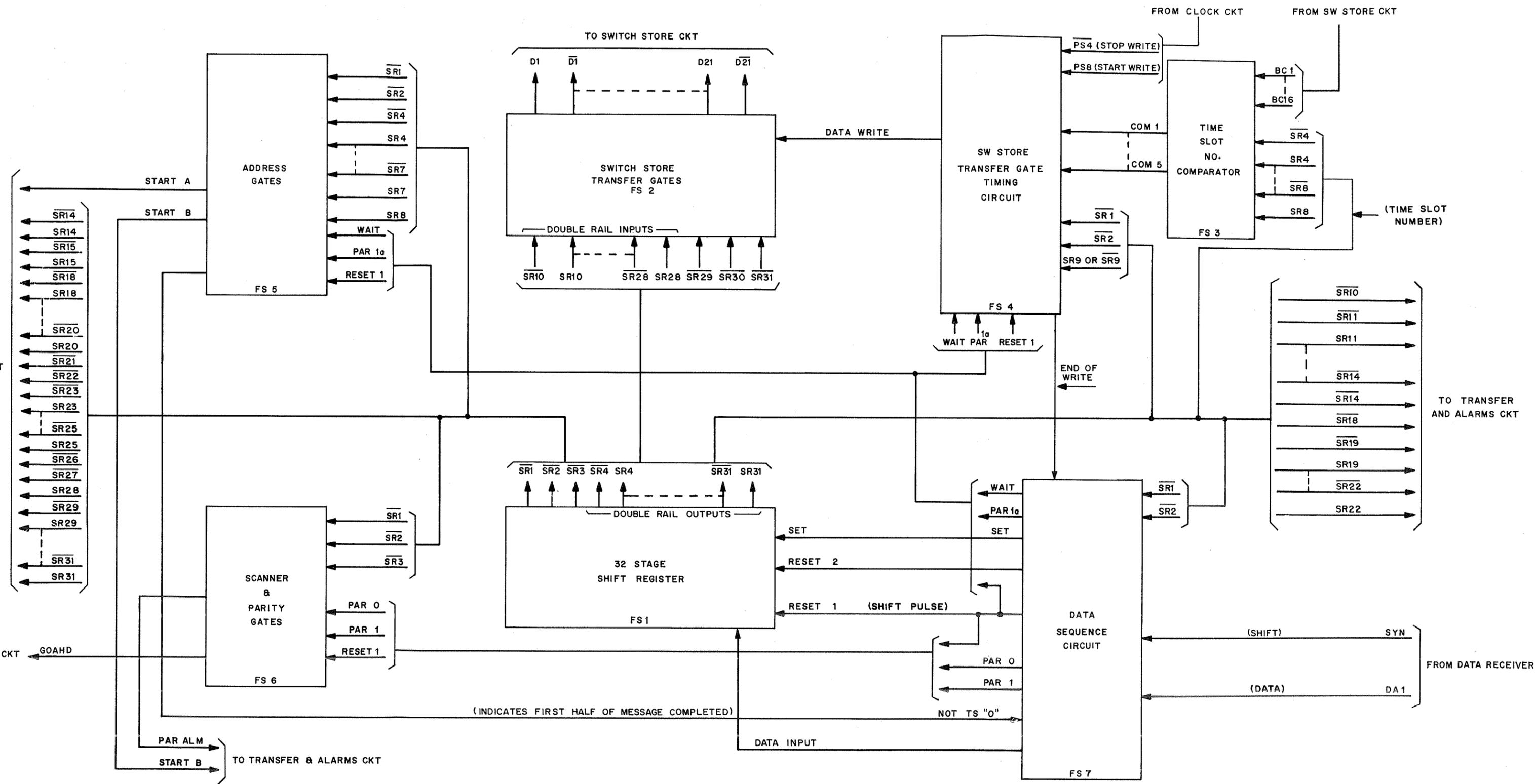
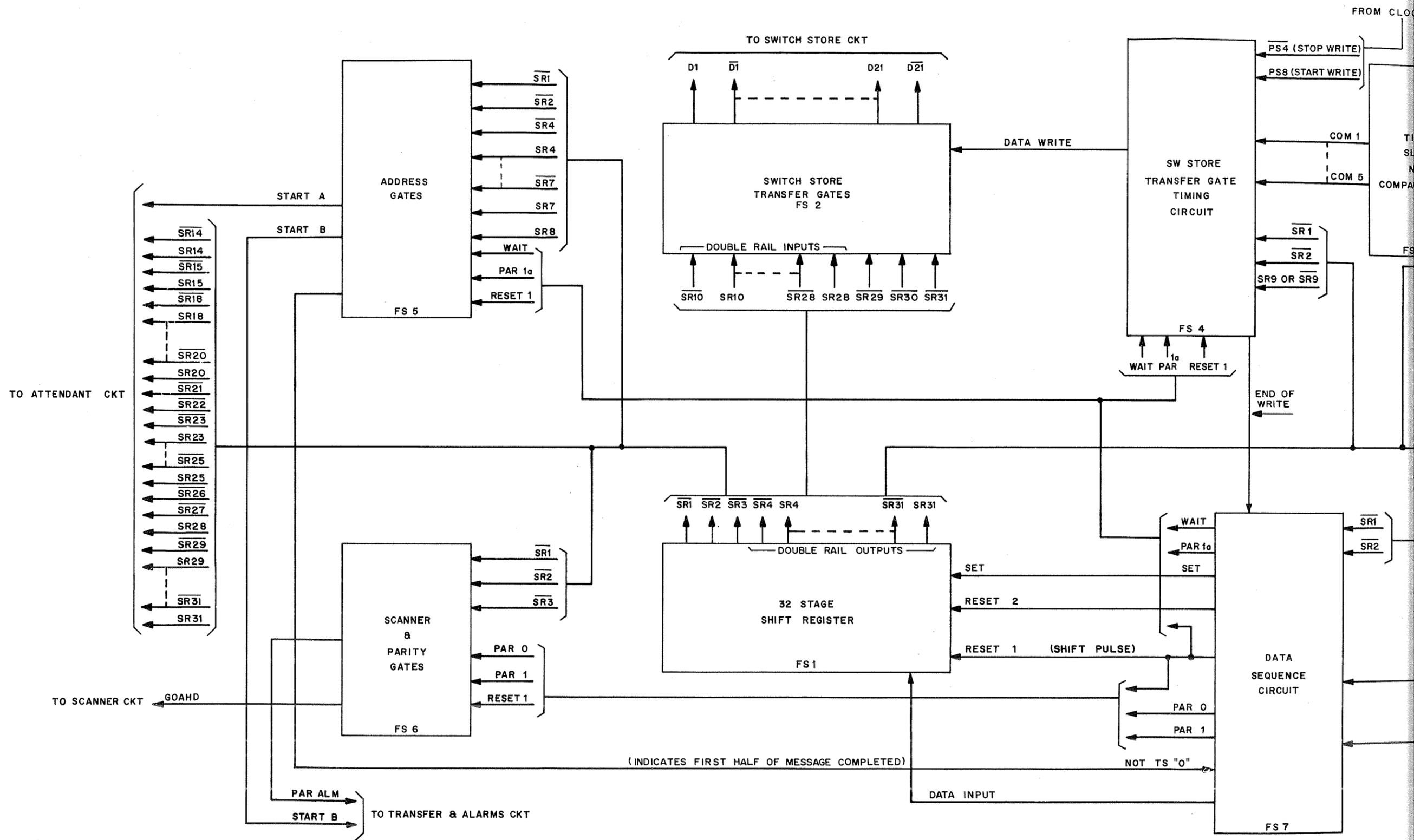


Fig. 5 - Data Distributor



D. Scanner and Parity Gates

5.06 This circuit has inputs from the shift register and the data sequence circuit. Its operation is a simple logic translation. A positive GOAHD signal to the scanner will be generated only if the first three bits of any message are present and if the message parity is correct (odd). A parity alarm signal will be generated only if the first two bits are present and parity is wrong (even). The RESET 1 lead is used to prevent any action until all shift register stages have settled to a quiet state.

E. Address Gates

5.07 This circuit produces three unique outputs, none of which can occur simultaneously. This circuit is used to steer the incoming message. If the number in the time slot address (bits 4 through 8) is 30, a transfer and alarm start pulse (START B) is generated and the shift register outputs are allowed to perform their function in the transfer and alarms circuit. If the number in the time slot address is 0, an attendant circuit start pulse (START A) is generated and the shift register outputs are allowed to perform their function in the attendant circuit. If the time slot is any number other than 0, a pulse on (NOT TS "O") lead is generated which allows the shift register contents to be gated to the switch store.

F. Time Slot Number Comparator

5.08 The time slot number contained in any incoming message will occupy five shift register stages (SR 4, 5, 6, 7, and 8). The outputs of the five shift register stages are double-rail coupled to the comparator. A second and corresponding group of inputs to this circuit is the output of the switch store horizontal address binary counter which determines the time slot in the switch store to be addressed. When the two binary numbers match, the DATA WRITE lead is energized and the appropriate shift register outputs are gated to the switch store.

G. Switch Store Transfer Gates

5.09 The A and B party, conference, continuous ring, interrupted ring, and two operator bits are double-rail gated to the switch store through these gates at the correct moment. The correct moment is defined as the time when the DATA WRITE lead goes to ground.

H. Switch Store Transfer Gate Timing Circuit

5.10 This circuit develops two outputs: DATA WRITE and END OF WRITE. It is an *and* gate which is not enabled until all of the following conditions are met.

- (1) Time slot in the switch store and in the data distributor are identical (COM1 to COM5, all at ground).
- (2) Shift register is fully loaded (SR1 and SR2 are 1s).
- (3) No reset pulse is present. (RESET 1 is ground.)
- (4) Parity is correct. (PAR 1 is ground.)
- (5) A 10- μ sec interval has passed since the last SYN (shift) pulse was received. (WAIT is ground.)
- (6) The data distributor for the switch unit half involved is handling its own message. (SR9 or SR9 is ground.)

When the above conditions occur simultaneously, the output, DATA WRITE, goes to ground and the contents of the transfer gates are gated to the switch store. Both data distributors receive every incoming message. Each data distributor drives an associated switch store, but the incoming message is addressed to one store or the other, never both. A single bit (bit 9) determines which switch store is the destination. If the bit is not present, data distributor 1 will generate DATA WRITE and data distributor 2 will not. If bit 9 is contained in the message, the opposite is true. Upon completion of the DATA WRITE cycle in the switch store, the END OF WRITE lead goes positive informing the data sequence circuit that it may begin to reset the shift register for the second half of the message.

6. SWITCH STORE CIRCUIT AND CLOCK**A. General Description**

6.01 The switch store is the circuit which retains in its memory the records of all telephone calls being controlled by the switch unit. It is composed of a 25-word, 21-bits per word, 3-hole ferrite core memory and its associated access circuitry.

B. Memory Array

6.02 The memory and its access circuits and sense gates are shown in Fig. 6. A more detailed drawing of the memory array itself is shown in Fig. 7.

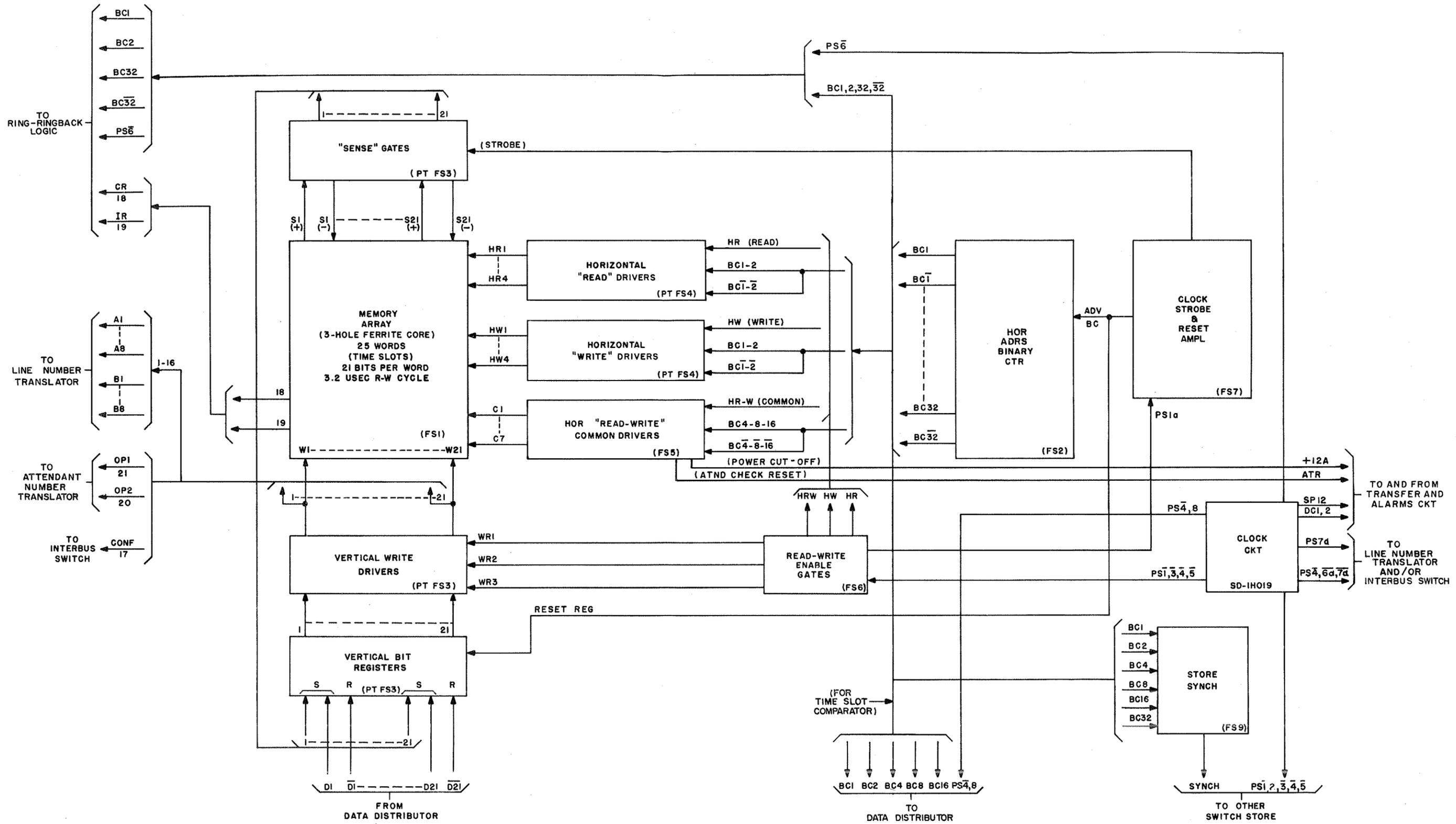


Fig. 6 - Switch Store and Clock

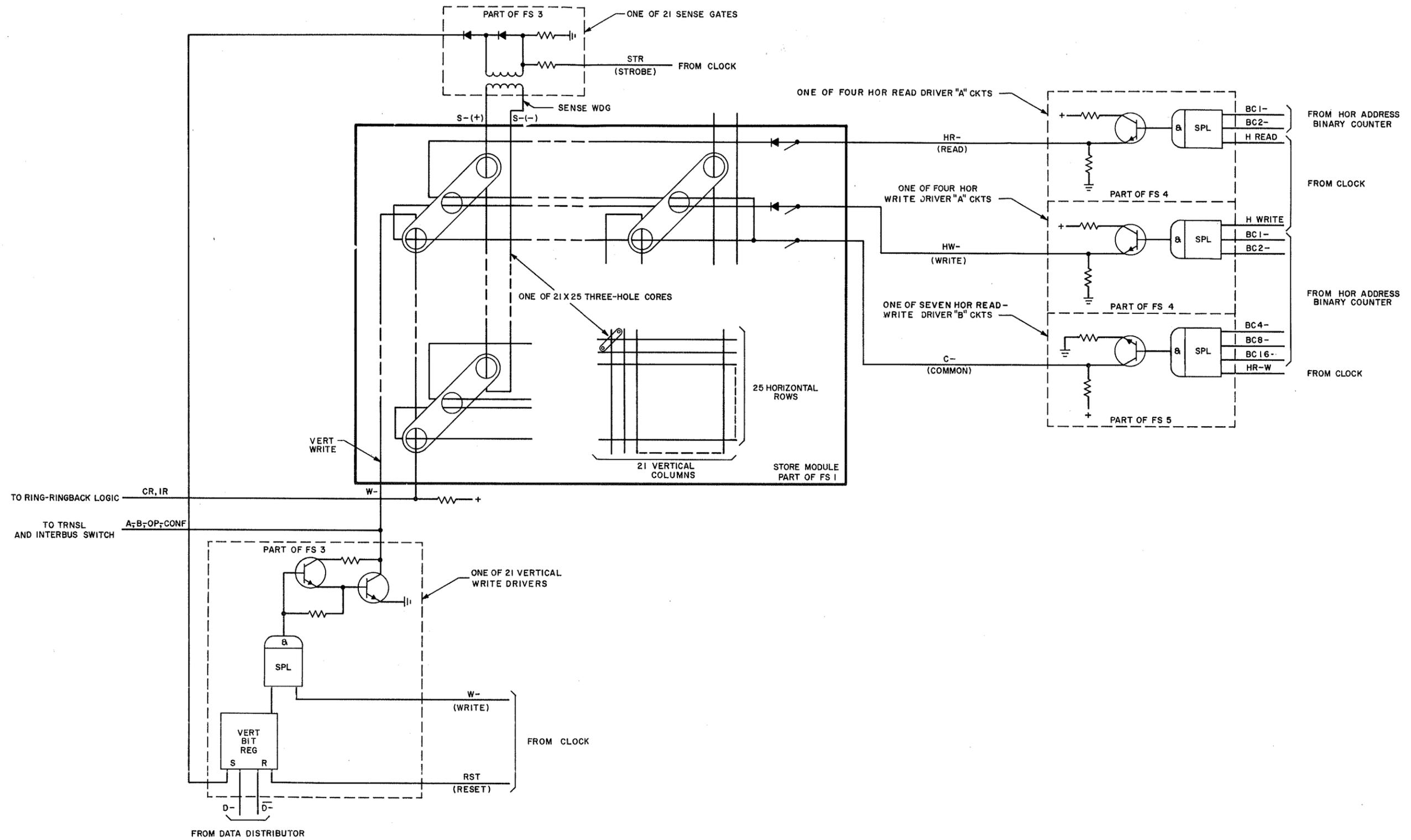


Fig. 7 - Memory Module and Access Circuitry

6.03 In order to read out or make use of an information bit that is stored in any particular core, the horizontal driver for that horizontal row will be pulsed through the center hole. This will cause the upper end of the core to be switched to a 0 if it contained a 1, destroying the contents of the core. In this process of destructive read out, however, a sense winding will couple the current surge of the core being reset (switched to 0) to a sense gate and back down to a vertical bit register. This register in the set state will cause its vertical write driver to write the original 1 back into the memory core by way of the vertical write lead. This re-write process requires coincidental current pulses from the vertical write and the horizontal write drivers which are timed for writing by the clock circuit.

6.04 As the vertical write driver output is placed on the vertical write lead to set the memory core, it also enables the appropriate line number translator, attendant number translator, ring-ringback circuit, or interbus switch.

6.05 Recall (see 6.03) that the manner of making use of a particular bit in a particular horizontal of the memory array considered only one of the horizontal cores. Actually, all of the cores (21) in a particular row are simultaneously accessed in exactly the same way since the HR lead is series wound through all core center holes in each horizontal row. The action just described (read out, sense, reregister, and vertical rewrite) for one particular core may occur in any of the 21 cores when its associated vertical bit register stage is found in the set state during the write interval.

6.06 When no information bits are stored in the memory array, there are no outputs to the sense windings, therefore, no change in the reset condition (needed for the writing in the original 0) of the vertical bit register. When the contents of this register are gated out, a zero (0) appears at the input to the translators, ring-ringback logic, interbus switch, and the memory array.

C. Clock

6.07 Each of the two identical clocks contains a quartz crystal oscillator (312.5 kc). The output of the oscillator is shaped to provide posi-

tive output pulses approximately $1/2 \mu\text{sec}$ wide and occurring at the 312.5-kc clock frequency. The oscillator output drives a 3- μsec multistap delay line. The outputs of this delay line are used to set and reset high speed flip-flops in order to generate timing pulses. In addition to driving the switch store, the clock generates timing pulses for use by the bus clamp, interbus switch, line number translator, ring-ringback logic, data distributor, and transfer and alarms circuits.

6.08 The two clocks are wired so that oscillator 2 is not normally used. The clocks are interconnected in a manner that allows clock 1 to bypass the oscillator in clock 2 and perform its function. If clock 1 should fail, oscillator 2 is wired to take over immediately. Both clock oscillator outputs are wired to the transfer and alarms circuit to continually indicate their status.

D. Horizontal Address Binary Counter

6.09 This circuit consists of a 6-stage binary counter. The first five stages of the counter are recycled at the count of 25 while the sixth stage is allowed to run uninterrupted. The counter is driven by the lead called ADV BC which is the output of an emitter follower called the RESET AMPL. The input to the RESET AMPL is, effectively, clock pulse PS1 since it passes through only one stage of inversion in the READ-WRITE ENABLE GATES circuit.

6.10 The output of the binary counters provides the desired inputs to the horizontal read and write drivers to address the time slots and also to the ring-ringback, transfer and alarms, data distributor, and store synch circuits.

E. Horizontal Read, Write, and Read-Write Drivers

6.11 This circuit translates the binary counter inputs in order to turn on the drivers in sequence. Timing and width of the output pulse of each of the READ drivers are determined by the HR gating pulse. Similarly, the output of each of the WRITE and READ-WRITE drivers is controlled by gating pulses HW and HR-W, respectively.

F. Read-Write Enable Gates

6.12 This circuit is composed of amplifiers required to fan out to the many current drivers since the clock circuit output does not have high fan out drive capability.

G. Sense Gates, Vertical Write Drivers, and Vertical Bit Registers

6.13 These circuits will be described together since they are all part of the same general vertical write circuit. Fig. 7 should be referred to during the description.

6.14 As mentioned in Section B, Memory Array, the memory core output pulses (approximately 180 mv) appear on the 21 vertical sense windings in the memory array during the destructive read pulse. One of the sense windings (bit position) will be described since they are all identical. Each word may or may not contain a 1 and therefore a 1 will appear on the sense winding only at times corresponding to the read out time for the word containing a 1. The positive bit pulses (1s) are transformer coupled (20:1 step up) to the sense gates which are enabled only during the strobe (STR) interval, located in the middle of the read out time for each word. This prevents the detection of noise pulses during the write intervals. The vertical register may be set by recirculating bits, as described, or by new information coming from the data distributor. The discussion will now be narrowed to a single bit of only one word and how it is read out and rewritten into the memory or how it is changed by new information available from the data distributor. A number of circuit operations will be listed in the time sequence in which they occur in the store.

6.15 The bit is read out (sensed) and sets (or does not set in the case of 0) the vertical bit register. This removes the bit from the memory core.

6.16 Now new information from data distributor is allowed to change the state of the bit register or keep it the same. If no new information is present, both inputs from the data distributor remain at ground and the bit register retains the 1 or 0 information provided by the sense winding.

6.17 The WRITE pulse is provided from the clock to allow the contents of the register to be written into the memory core. If a 1 is to be written, current will flow (during write time) from +24 volts through a current limiting resistor ahead of the write winding, then through the winding to the vertical access driver, and then to ground. If a 0 is to be written, no write current will flow. It should now be evident that writing requires the simultaneous operation of a horizontal write driver, a common write driver, and a vertical access driver, while reading requires only a horizontal and a common driver.

H. Memory Outputs to Other Circuits

6.18 During the writing of any word, the collectors of the 21 vertical drivers will swing from +24 volts to near ground while writing a 1 or remain at +24 volts for a 0 (as required). This voltage change is coupled away from the collectors to the proper destinations as shown in Fig. 6. The exceptions are the CR and IR bits which are taken from the voltage source side of the memory.

7. LINE NUMBER TRANSLATOR CIRCUIT**A. General Description**

7.01 This circuit performs the task of translating the output of the switch store which retains the records of all calls being handled by the switch unit at any one time. The translated output is used to trigger matrix drivers in the right combinations to maintain time division telephone connections. It also performs ringing and ringback functions as dictated by the ring-ringback logic circuit. Fig. 8 should be referred to during the description of all major blocks.

B. Memory Output Register

7.02 The switch store provides parallel bit information to this circuit which is composed of 16 register stages. A definite relationship exists between the input bits and the many line and trunk circuits within the switch unit. Cross points, representing line and trunk circuits, are physically located in 16 horizontal rows and 16 vertical columns, a 16 by 16 matrix. Bits A1 to A8 define the horizontal row (A1

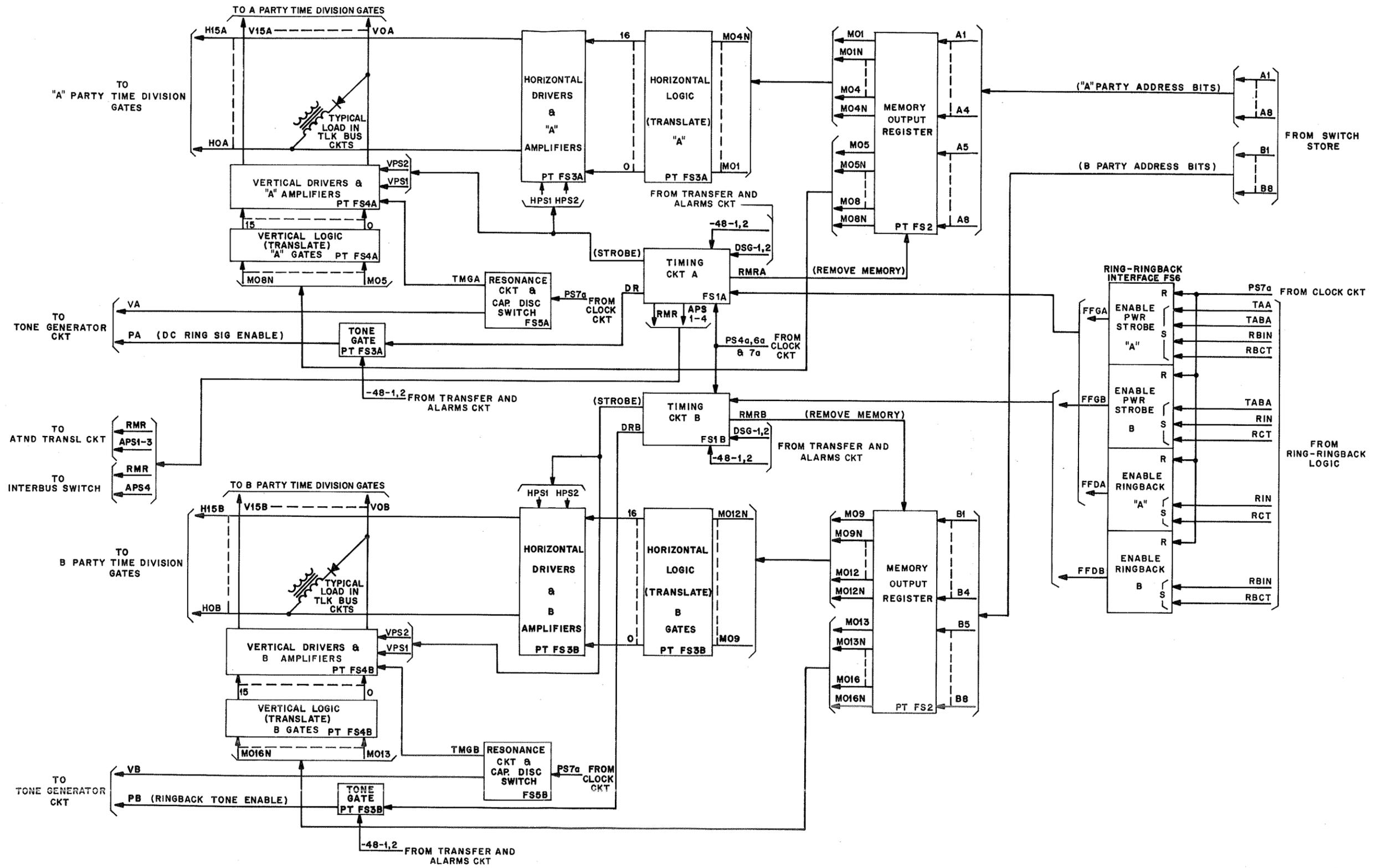


Fig. 8 - Line Number Translator

to A4) and vertical column (A5 to A8) of the A (calling) party in binary form while bits B1 to B8 correspondingly define the B (called) party cross point. A typical arrangement of the binary input information is shown below.

A (Calling) Party									
HORIZONTAL ROW	VERTICAL COLUMN								CROSS POINT
Input	1	0	1	0	0	1	1	1	0
Bit No.	A1	A2	A3	A4	A5	A6	A7	A8	= H10 V6
Weight	8	0	2	0	0	4	2	0	

B (Called) Party									
HORIZONTAL ROW	VERTICAL COLUMN								CROSS POINT
Input	0	1	1	1	1	1	0	1	
Bit No.	B1	B2	B3	B4	B5	B6	B7	B8	= H7 V13
Weight	0	4	2	1	8	4	0	1	

Each group of four bits will have 16 possible combinations from H0, V0 through H15, V15.

7.03 The memory registers serve to temporarily store the bits of each word at the time the word is written into the switch store memory. The outputs of the register provide the inputs to the horizontal and vertical logic translators.

C. Horizontal and Vertical Logic Translators

7.04 The operation of these two circuits is identical. The A party horizontal and vertical translators shown in the upper portion of Fig. 8 accept the stored bit contents of the register and translate to 1-out-of-16 horizontal drivers and 1-out-of-16 vertical drivers. The B party horizontal and vertical translators (lower portion of the figure) perform an identical translation. Each word contained in the store will cause the line number translator to turn on four matrix drivers. Two of these will close time division gates to connect an A party to the talking bus, and two will connect the B party to the bus at the same time.

D. Horizontal and Vertical Drivers

7.05 The inputs to these circuits may not arrive simultaneously due to differences in transistor switching speeds in the preceding cir-

cuits. The drivers are therefore gated on and off by strobe pulses HPS1, 2 and VPS1, 2. All matrix driver current pulses follow a path from ground through a common resonant timing circuit (described later) and then through the vertical drivers, matrix, and horizontal drivers to -48 volts which is supplied from the transfer and alarms circuit. Disabling the drivers of an entire line number translator is accomplished by removing the -48 volt source.

E. Resonant Timing Circuit

7.06 Each of the 25 time slots is divided into two periods. The first 2- μ sec period is used for the actual transfer of energy between two stations. The last 1.2 μ sec is a rest period required to allow the drivers to recover and to discharge a capacitor in this circuit which charges during every 2- μ sec timing period. During the rest period it is necessary to eliminate any energy remaining on the talking bus. This is accomplished by the bus clamp circuit which provides a low impedance path between the talking bus and ground during the last 1.2 μ sec of each time slot. The bus clamp detailed circuit description is covered by another document.

7.07 The current path in the resonant timing circuit follows a series path through a capacitor, an inductor, and a diode. The natural resonant frequency of the series LC circuit determines the current pulse duration and therefore the period of time during which two parties will be connected in any time slot.

F. Capacitor Discharge Switch

7.08 Clock phase PS7a which occurs during the last 1.2 μ sec of each time slot drives this circuit *on* to provide a low impedance path to ground in order to discharge the resonant circuit capacitor discussed in the preceding section.

G. Timing Circuits and Tone Gates

7.09 Clock phases PS4a and PS7a are supplied to the timing circuit and *anded* to generate a pulse used to reset the memory registers just prior to the time when the bits of the next memory word are fed to the inputs of the registers. The same pulse is also used to reset the memory registers in the attendant number translator circuit.

7.10 Clock phases PS6a and PS7a are used to generate the STROBE pulse discussed in Section D. Horizontal and Vertical Drivers. The two clock pulses operate an *and* gate which also has inputs from the ring-ringback interface circuit. Timing circuit A receives pulses FFGA and FFDA while timing circuit B is wired to pulses FFGB and FFDB. A fourth input to the *and* gate is provided from the transfer and alarms circuit and goes to ground to disable the timing circuits when required by the control unit.

7.11 A discussion of the timing of pulses FFGA, FFDA, FFGB, and FFDB is necessary to understand how these pulses from the ring-ringback circuit control the operation of the line number translator during any time slot containing ringing information. Assume that only one talking connection exists on the bus. Normally the horizontal and vertical drivers required for that connection are allowed to operate once every 80 μ sec (normal sampling). In this case the inputs from ring-ringback do not exercise any control, and driver timing depends on the input clock phases. When a ringing connection is desired in any time slot, it becomes necessary to provide (on the bus) a ringing signal to the B (called) party and an audible ringback tone to the A (calling) party. If both types of signals were connected to the bus at the same time, the effect would be an application of ring voltage to both phones and the audible ringback tone would not be able to perform its function. Additionally, the calling party would naturally be off-hook and would hear ringing voltage in the receiver. To avoid this the ring-ringback logic performs several functions. It will only allow ringing and ringback to occur alternately in the same time slot. For example, when the time slot is first sampled, the ring-ringback logic circuit will inhibit the A party matrix drivers (FFGA remains at ground) but will allow the B party to be connected to the talk bus (with a positive pulse on FFGB). The B party alone on the bus, however, is not enough. A ring-the-phone signal must also be connected to the bus at the same time. This is done by pulse FFDA which controls (by way of DR lead) a special driver called TONE GATE in the A section of the translator. At the same time, pulse FFDB inhibits (by way of DRB lead) the special driver in the B section. This prevents connecting audible ringback to the talk bus. At the next time slot sampling, the situa-

tion is reversed, ie, the A party is connected and receives an audible ringback tone from the TONE GATES in the B section while the B party matrix drivers are inhibited. The tone gates are equivalent to matrix drivers. Their output current pulses follow a path through the resonant circuit to leads VA and VB, through the ring and ringback sources respectively, and back to the tone gates on leads PA and PB.

H. Ring-Ringback Interface

7.12 Four flip-flops are used in each of the enable power and enable ringback sections shown in Fig. 8. They act as buffers and perform *or* logic on the input signals. The functions performed on the line number translator by each of the input signals are described in the discussion of the ring-ringback logic circuit. Clock phase PS7a is used to reset the flip-flops at the end of each sampling period so that they can assume new states for each time slot.

8. RING-RINGBACK LOGIC

A. General Description

8.01 In the No. 101 ESS, line ringing and ringback are connected alternately to the calling and called parties. This circuit also provides the interruption rates required to cause ringing and ringback to be applied to the stations for 1 second out of 4. Fig. 9 shows the block outline.

B. Staggered Interrupt (1 Second) Timing

8.02 Ringing capacity within the switch unit is limited. The single 100-milliampere ring generator provided is capable of ringing approximately eight stations simultaneously. For this reason, the ring-ringback logic is designed to provide a 4-phase output. Each phase permits ringing to occur on any phone assigned to one of six or seven nonadjacent time slots. For example, phase 1 (group A) allows ringing during time slots 1, 5, 9, 13, 17, 21, and 25 (seven total), while phase 2 (group B) controls slots 2, 6, 10, 14, 18, and 22 (six total). Phases 3 and 4 (groups C and D) begin with time slots 3 and 4 respectively and each controls a total of six slots. This portion of the ring-ringback logic develops a combined output at the interrupt (INT) gate. The output will pulse (for 1

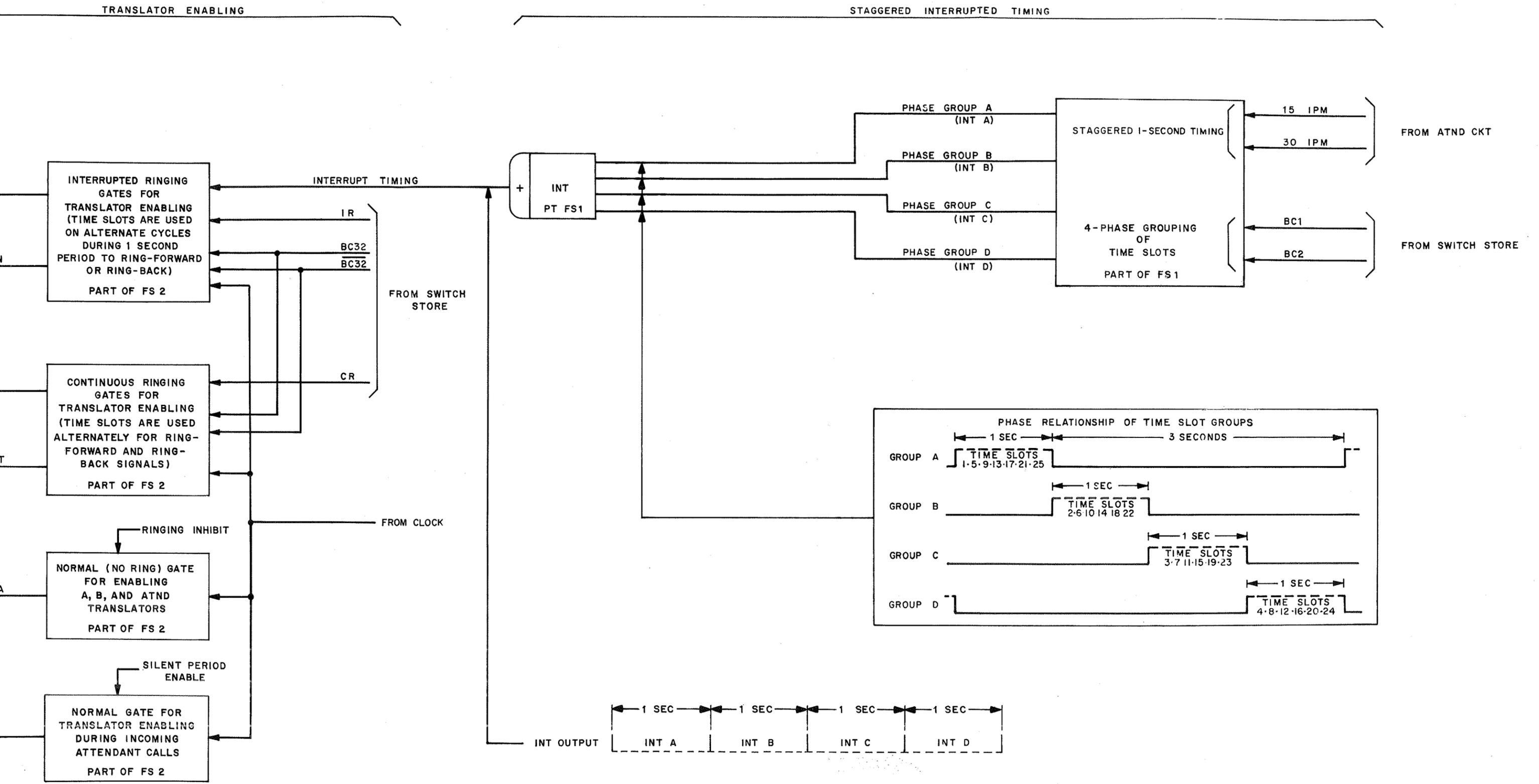
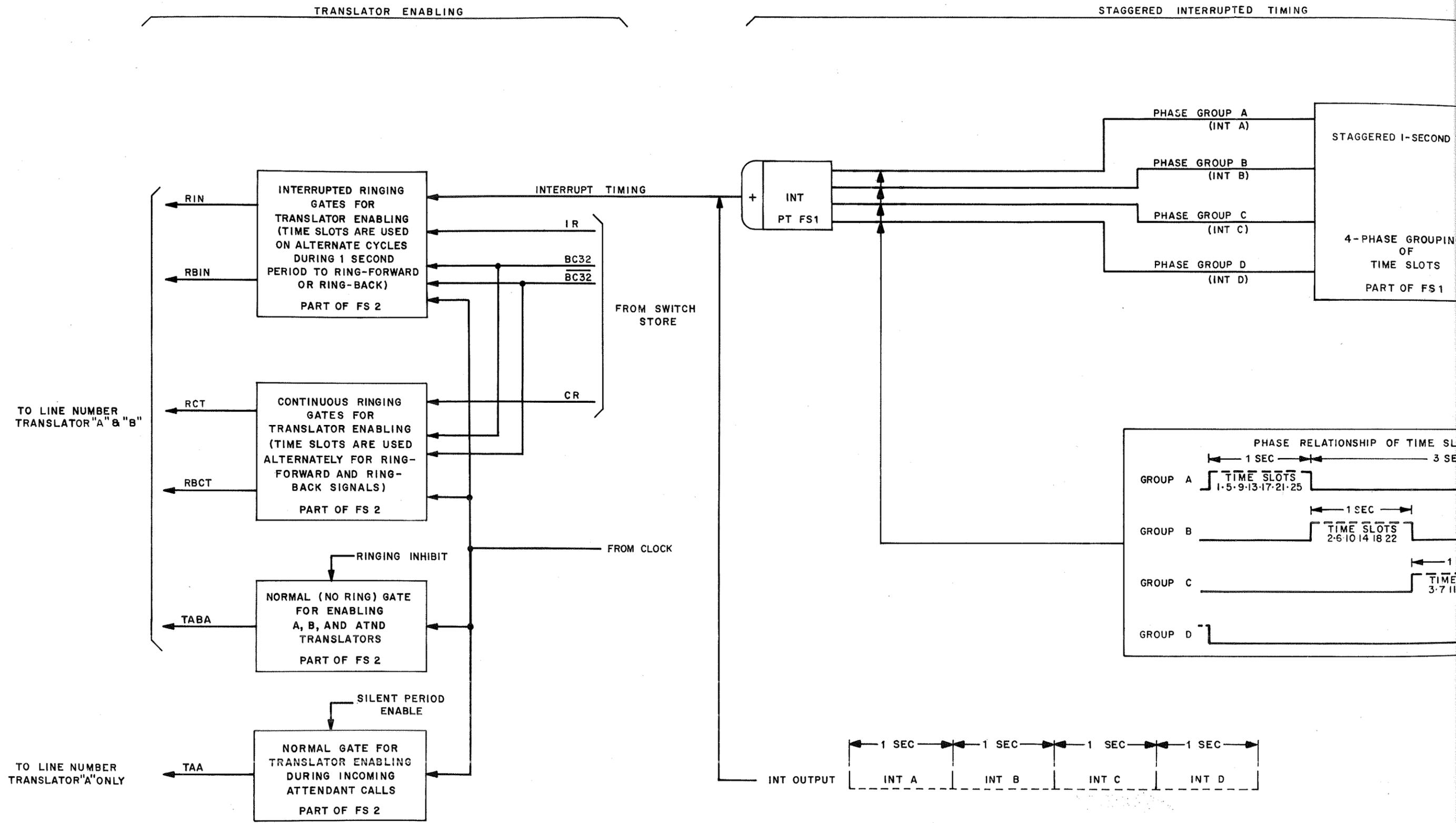


Fig. 9 - Ring-Ringback Logic



second) during the time slots affected by phase 1. During the next 1-second period, the output will change to a pattern of pulses which occur during the time slots controlled by phase 2. One second later the sequence will change to phase 3, and 1 second after that to phase 4.

C. Interrupt and Continuous Ring Gates

8.03 The description of these circuits will be restricted to a discussion of the characteristics of the output pulses and the functions they perform on the line number translator.

8.04 Output pulses RCT and RBCT will alternately go to ground once every 160 μsec for any time slot containing continuous ring bits from the switch store. These two pulses cause special ring and ringback drivers in the line number translator to operate alternately and uninterrupted until the continuous ring bit is removed from the switch store. Normally the control unit sends two messages when ringing a station. The first message sets up a continuous ring (which provides the immediate ring feature); and the second message, which follows by approximately 1 second, changes the ring connection to interrupted by erasing the continuous ring bit and replacing it with an interrupted ring bit. These gates are also fed by a clock pulse which determines the output pulse width (0.5 μsec).

8.05 Output pulses RIN and RBIN alternately go to ground once every 160 μsec for all time slots that have interrupt ring bits provided by the switch store. The interrupt timing input determines the phase during which the pulses will occur and that they will be present for only 1 second out of 4 (normal ring mode). The pulses will alternate since the RIN and RBIN output gates are also controlled by opposite phases of BC32 (changes state every 160 μsec). These two pulses perform the same function as RCT and RBCT in the line number translator. The clock input to these gates determines the output pulse width.

8.06 The output pulse on TABA normally goes to ground every 3.2 μsec . This pulse performs the function of allowing the line number translator matrix drivers to pulse once during every 80 μsec for each time slot occupied by a time division connection. If, however, a

ringing connection is to be set up in a time slot, this pulse will not go to ground during that time slot but will continue inhibiting the A and B matrix drivers normally fired during that time slot. Instead, the special driver (ring or ringback depending on the A or B translator section) will be fired by pulses RCT and RBCT or RIN and RBIN as discussed earlier.

8.07 The pulse on TAA is connected to the A party section of the line number translator. Its function is to enable firing the A matrix drivers to allow talking during the nonringing period of a ringing connection only when a conference or attendant bit is present.

9. ATTENDANT NUMBER TRANSLATOR

A. General Description

9.01 Incoming messages which call for the connection of one of three possible attendants to either a trunk circuit or a line circuit require that the attendant lines have access to the talking buses. The function of this circuit is to decode incoming messages containing operator bits and to properly set up a time division connection from an attendant to the talking bus. Two translators are provided in each switch unit to permit access to both buses. (See Fig. 10).

B. AMRO and AMR1 Circuits

9.02 These two circuits are flip-flop memory registers which temporarily store the OP1 and OP2 bits provided by the switch store in any time slot. Both registers are reset by pulse RMR from the line number translator.

C. Attendant Translator Gates

9.03 This circuit contains only three *and* gates which perform a 1-out-of-3 logic translation of the outputs of the AMR0 and AMR1 registers.

D. Driver Circuits

9.04 The three current drivers, which comprise this circuit, operate, when required, from the three outputs of the attendant translator gates. Their function is to provide the drive current required to maintain a time division connection between the talking bus and one of the

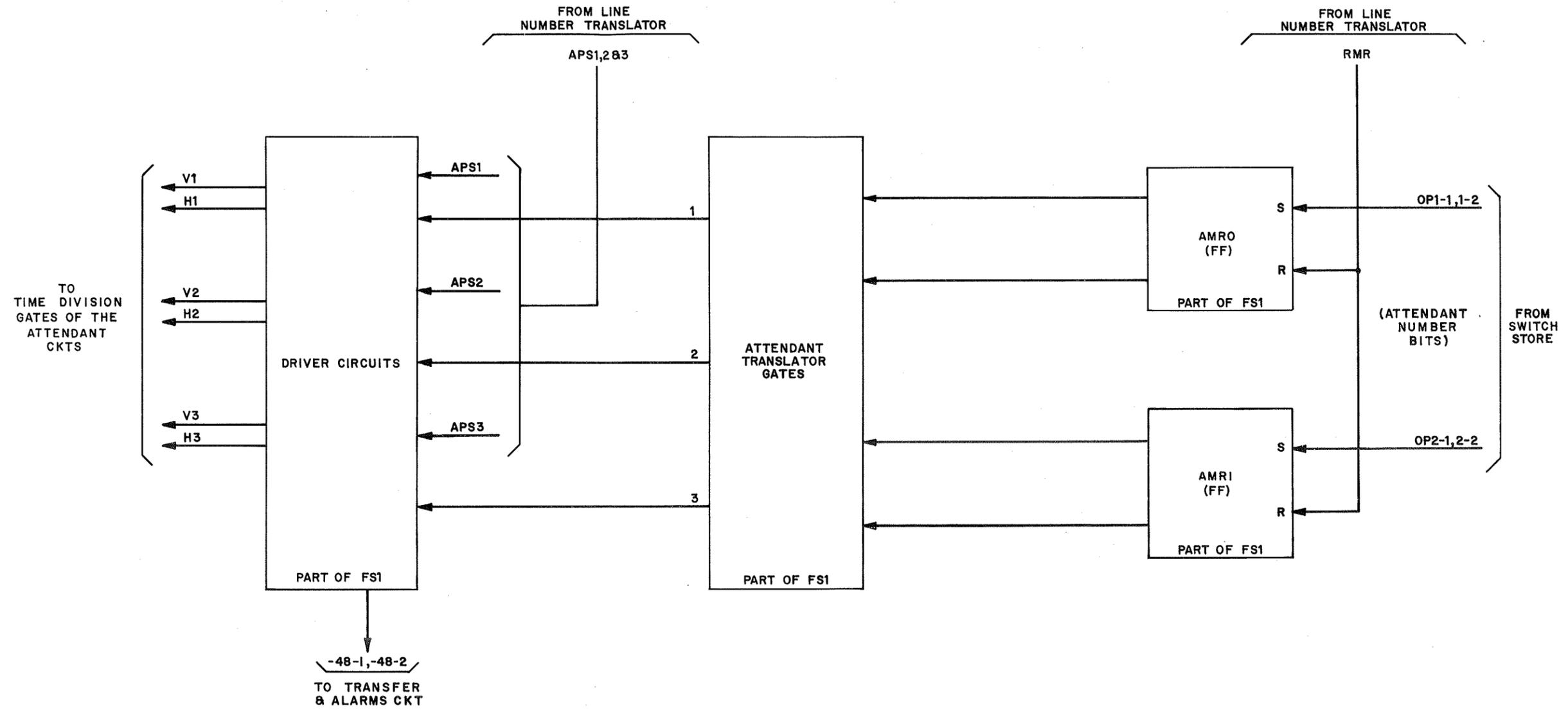


Fig. 10 - Attendant Number Translator

P. 39 Missing

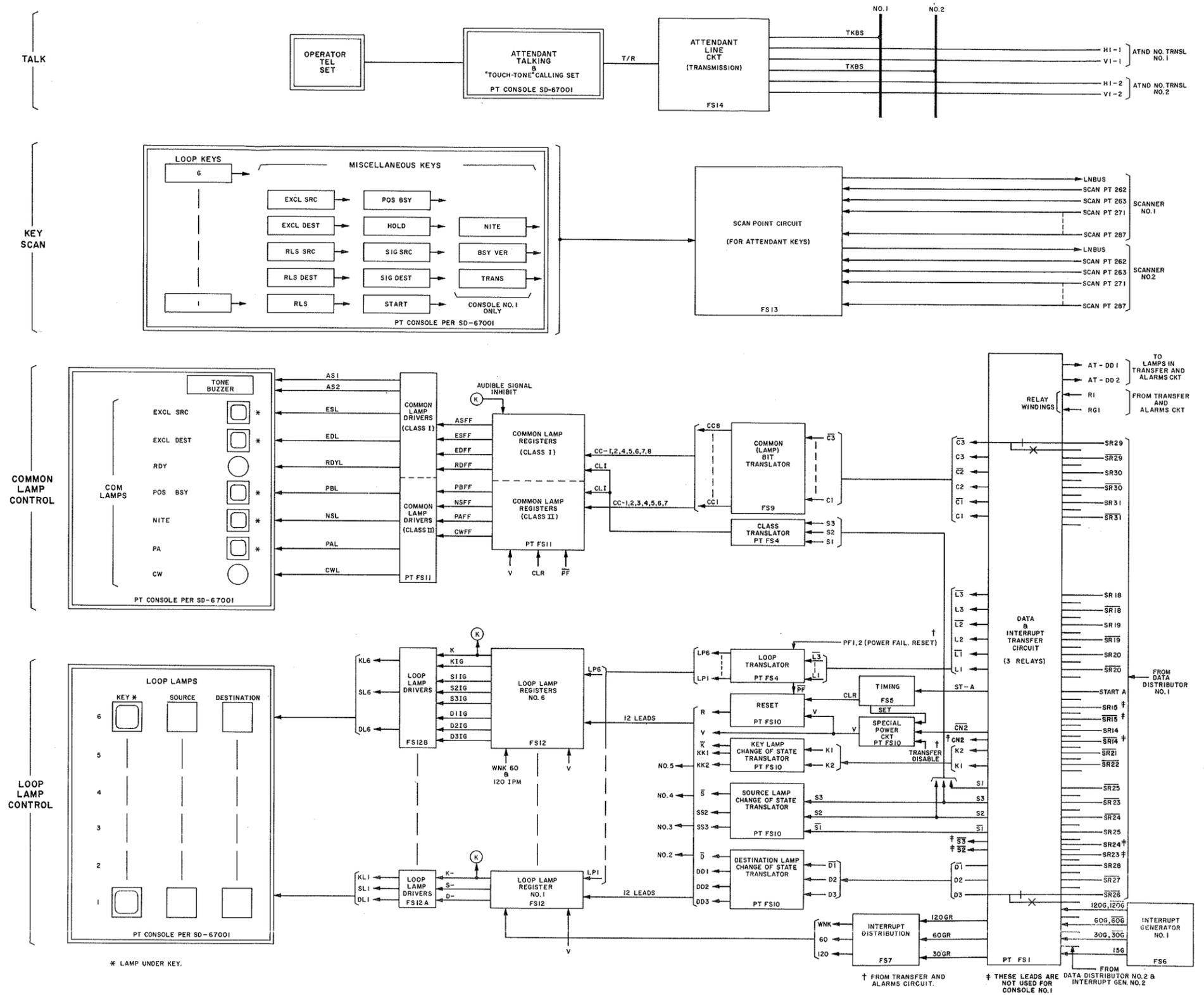


Fig. 11 - Attendant Circuit, Console No. 1

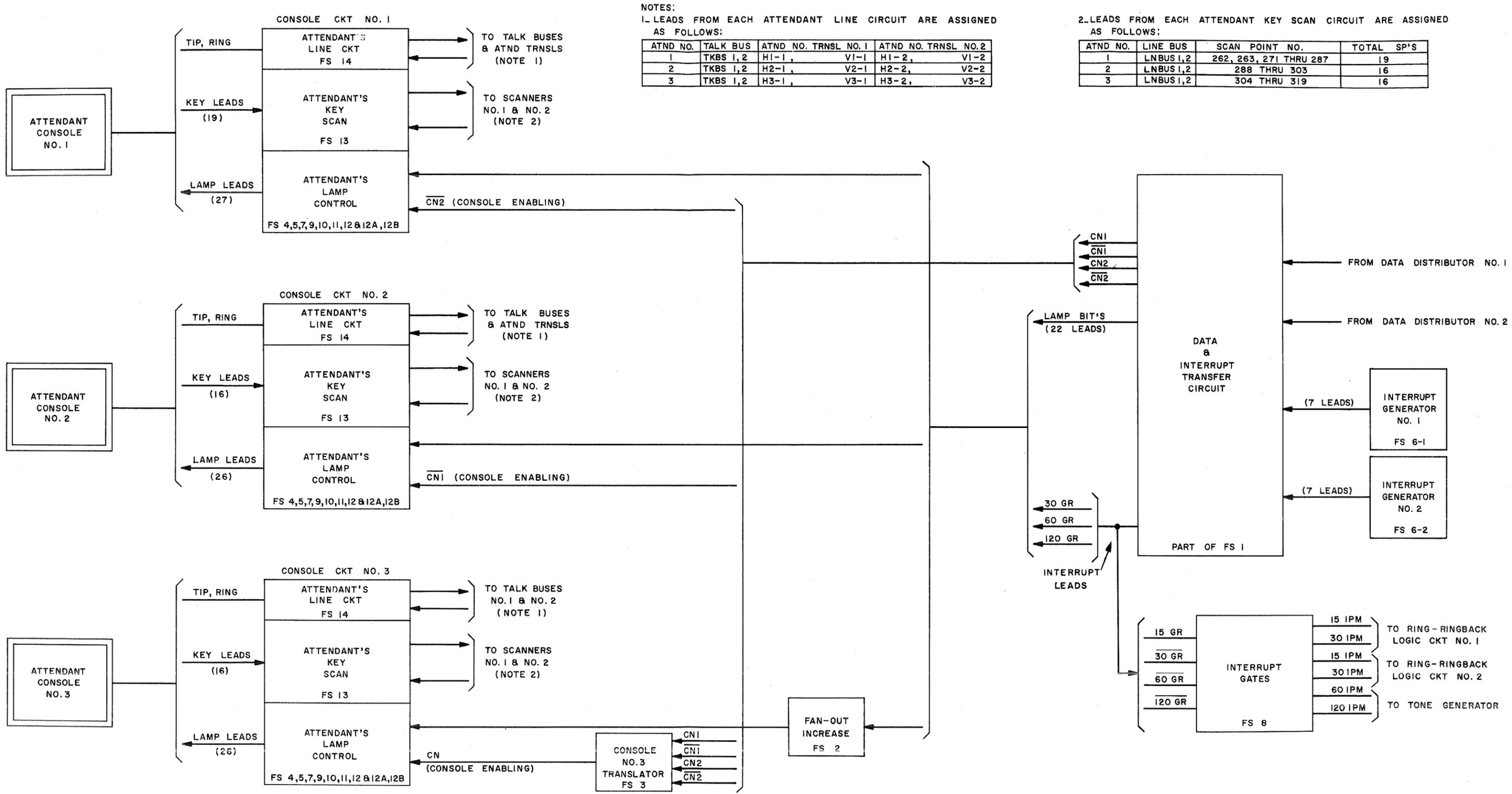


Fig. 12 - Attendant Circuit, Multiple Connection of Consoles

clear pulse is allowed to pass through this circuit to perform its clearing function. If any power should fail, the power failure (PF) leads will go positive and will cause the output of the reset circuit to remain at ground. This will cause all loop and source lamps to be turned off and all destination lamps to wink in unison. If a total power failure occurs, all lamps go out; but when power is restored, the same lamp action (winking) will take place due to the fact that when power is restored the transfer and alarms circuit will continue to provide a power failure alarm for the first 800 msec. This allows sufficient time to reset all flip-flops to the power failure state.

J. Key, Source, and Destination Lamp Translators

10.10 Key, source, and destination lamp information is translated by this circuit to provide single-rail outputs to the key, source, and destination lamp control circuits to be described later. One, two, or three complete and identical circuits are provided depending upon the number of consoles provided at the switch unit. Their inputs are driven in common from the transfer relays. Incoming messages will be one of two types. The message may contain information to change the state of one or more of the key, source, or destination lamps associated with a particular loop (class I message), or it may be intended to change the state of one or more of the common lamps (class II message). Assume a class I message commanding a change in state of a particular loop source lamp has been provided to the attendant circuit. The input gates will decode the change of state and provide one or more outputs which will set flip-flops in the source lamp register associated with the affected loop only. Since the message contained no information to change the state of either the key or destination lamps in the same loop, this circuit will produce two *no change* outputs which will inhibit any change in state of the flip-flops in the key and destination lamp registers.

10.11 In addition, a *no change* output to inhibit the source lamp register from changing state will result when the three message bits for this lamp are all ones. In this instance, all of the common lamp bits become effective since this code (all ones to the source lamp translator) labels the message as a class II message.

K. Loop Lamp Registers

10.12 The signals from the key, source, and destination lamp translators are fed single rail to this circuit and are gated to the lamp registers when special power is applied. Six identical circuits are provided, one for each loop. Three *and* gates in each of these six circuits perform inhibiting functions on the key, source, and destination registers whenever a *no change* command appears from the translators. One common input to the three gates allows one or more (depends on additional inputs) of these gates to reset those registers to be changed at the same time that the new register information is attempting to jam set the registers. The new information is present for a longer period than the reset and therefore will properly jam set the flip-flops. A second and common input to the three gates pertains to a specific loop and will allow resetting the registers of that loop. The corresponding leads to the other five loops will inhibit resetting their lamp registers since any incoming message affects only one loop. The output stages are *and* gates fed by the lamp registers and by the interrupt distributor which provides 120-ipm, 60-ipm, and a 30-ipm signal. Proper combinations of the register outputs allow the output stages to be turned on, off, or to be governed by the three interrupt rate inputs, thus providing fast flash (120 ipm), flash (60 ipm), and wink rates.

L. Loop Lamp Drivers

10.13 A total of 18 lamp drivers (6 loops, 3 lamps per loop) is provided for each console at the switch unit. The gates perform a translation of the outputs of the lamp register circuit in order to actually turn the lamps on and off at the desired rate (combining the flash or wink inputs from the loop lamp registers).

M. Common (Lamp) Bit Translator

10.14 The three inputs to this circuit from the data distributor can have eight possible combinations. This circuit translates the combinations and provides eight single-rail outputs to the common lamp registers.

N. Common Lamp Registers and Common Lamp Drivers

10.15 These circuits maintain on or off indications of the common lamps and audible signal on the console as determined by the inputs from the common bit translator. One of each of these circuits (except the night service lamp circuit which is only provided for console 1) is required per console. The circuit is enabled for class I and II messages by a single lead (CLI) from the class translator which remains positive (inhibiting) for all class II messages and goes to ground (gating) during class I messages. The eight inputs are gated to the lamp registers when special power is applied. The audible signal register is reset when the attendant depresses any loop key in response to the audible signal. A power failure will cause all common lamp registers to be reset (lamps out).

O. Scan Point Circuit

10.16 The pushbuttons and keys of each console are connected to individual scan points. The scanner circuit constantly interrogates these scan points in order to inform the control unit of the actions of one or more attendants. Depressing a console button will cause +12 volts to appear at the scan point associated with that button. This will allow the scanner interrogation pulse to pass through the scan point circuit and appear on the scanner line bus (off-hook signal).

P. Talking Circuit

10.17 Each console requires an attendant line circuit. It is the circuit controlled by the attendant number translator which allows an attendant to be time division-connected to either talking bus. It supplies talking battery to the attendant telephone sets.

Q. Multiple Connection of Consoles

10.18 Fig. 12 shows that all input information to each of three possible consoles is coupled in parallel directly to the various circuits associated with consoles 1 and 2. Fan out capability of the data distributors would be exceeded if a third console is bridged on the data transfer circuit, and for this reason the fan out increase circuit is included in all switch units having a third attendant console. Only one difference ex-

ists between the inputs to the three consoles. Leads CN1 and CN2 and their complements are the bits which determine the selection of a particular console by an incoming message. Whether these leads are at ground (enable console) or battery (inhibit console) depends upon the binary digit 1, 2, or 3 derived from bits CN1 and CN2. For example, if CN1 is present in an incoming message, console 1 will be enabled while consoles 2 and 3 will be inhibited. Similarly, if both CN1 and CN2 are present, the only console which will be enabled will be console 3.

11. DUPLICATION OF CONTROL CIRCUITS

A. General

11.01 Switch unit design philosophy specifies that a single malfunction within any major circuit should not be allowed to cause a total inability to process telephone calls. For this reason important blocks of circuits are duplicated to permit disabling troublesome circuits. Fig. 13 shows the circuit duplication and how all major units are interconnected.

B. Incoming Message Flow

11.02 A single data link provides identical input information through a splitting pad to two data receivers which, in turn, allow all incoming messages to be sent to both data distributors. Both data distributors are wired to permit any incoming message to be sent to the associated switch store, to the transfer and alarms circuit, or to the attendant circuit. The destination is determined by the address contained in the message itself.

C. Functions of the Switch Stores

11.03 Each store with its associated memory independently controls the periodic time division connection of switching circuits to the 25 time slots on each of two separate talking buses. Therefore, the loss of either bus, due to a failure in any circuit associated with that bus, will cause a loss of only half the system capability. A defective half system can be removed from service by the transfer and alarms circuit.

11.04 A benefit derived by the division of the system into halves is that corresponding numbered time slots can be electronically

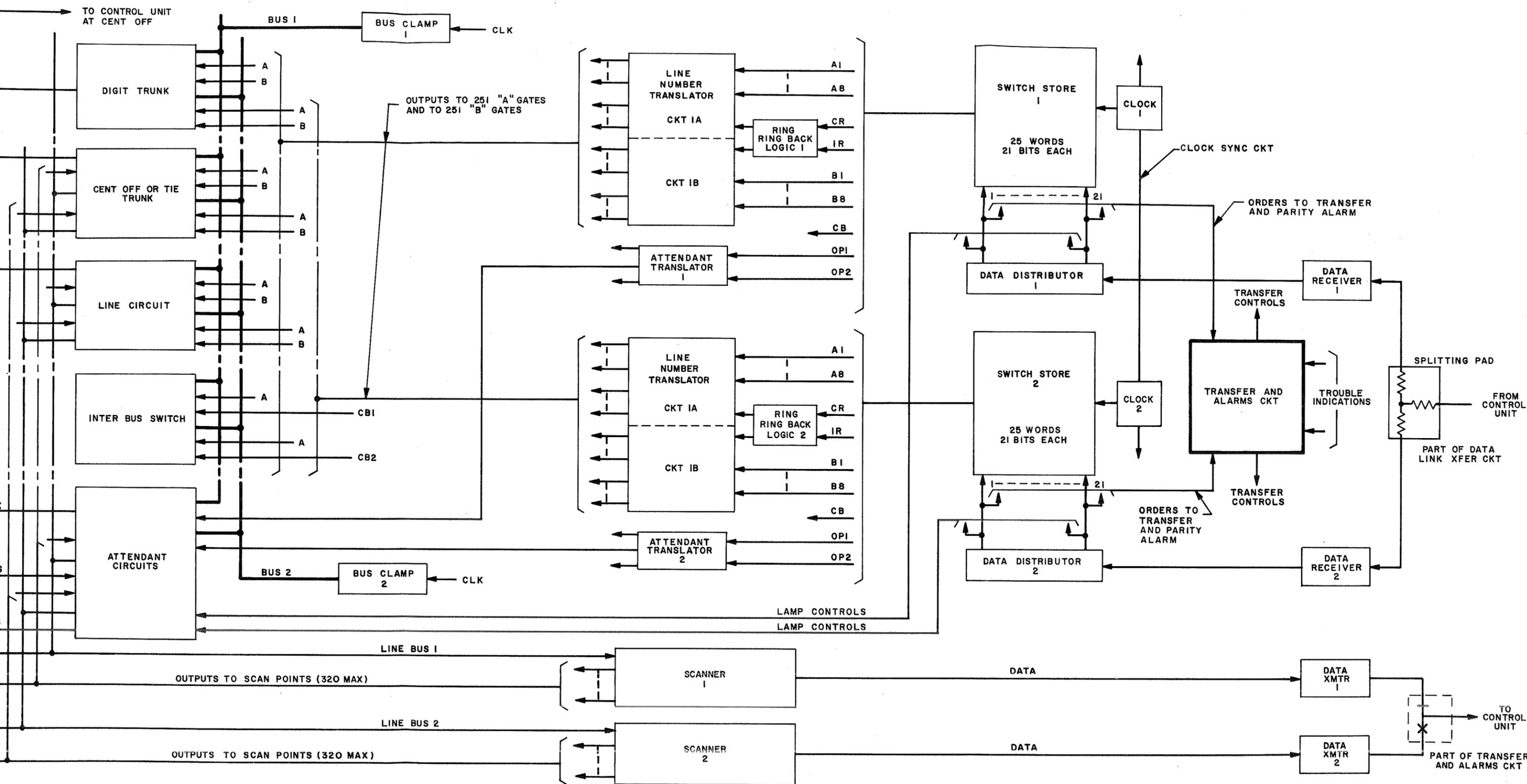
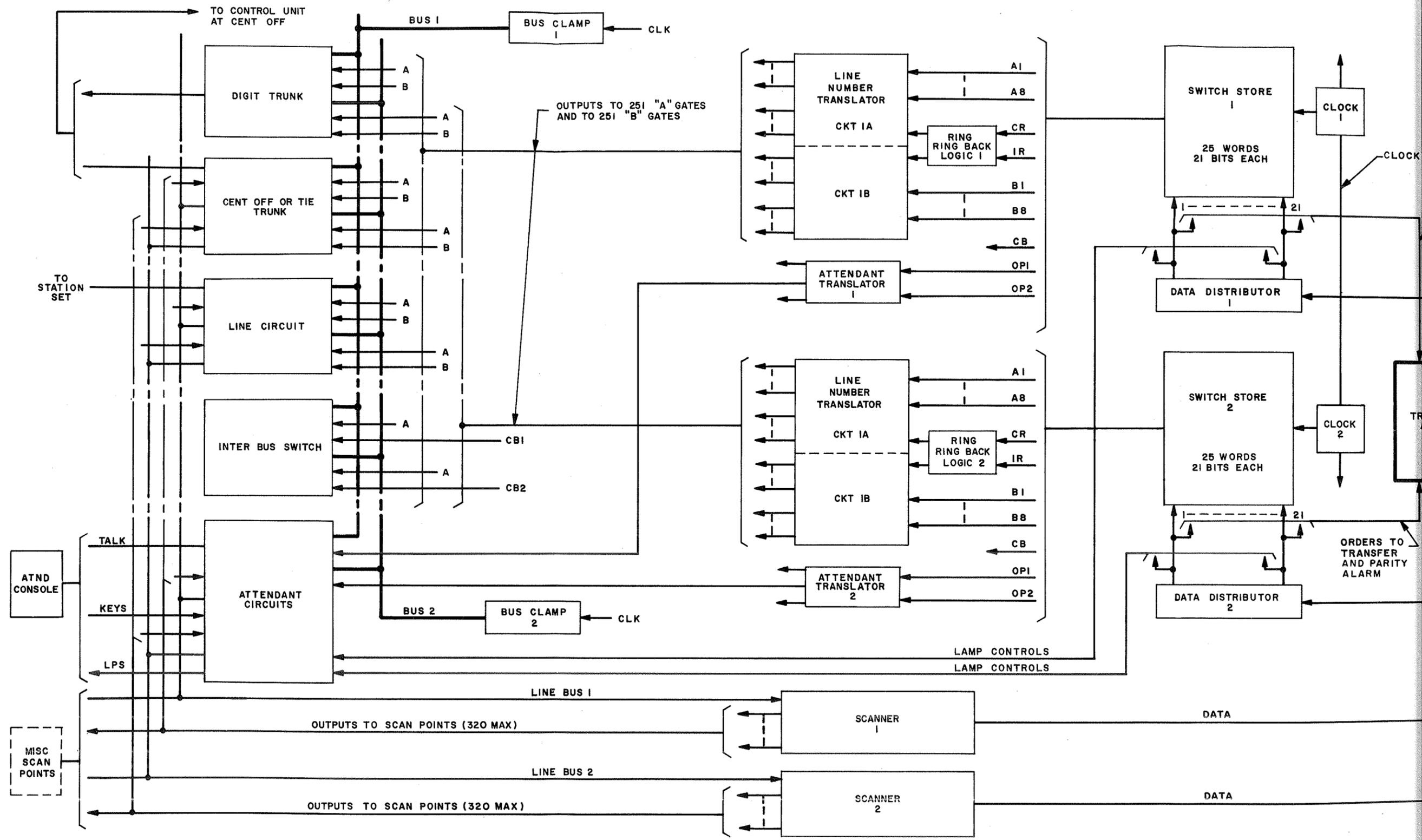


Fig. 13 - Duplication of Switch Unit Control Circuits



P. 49 Missing

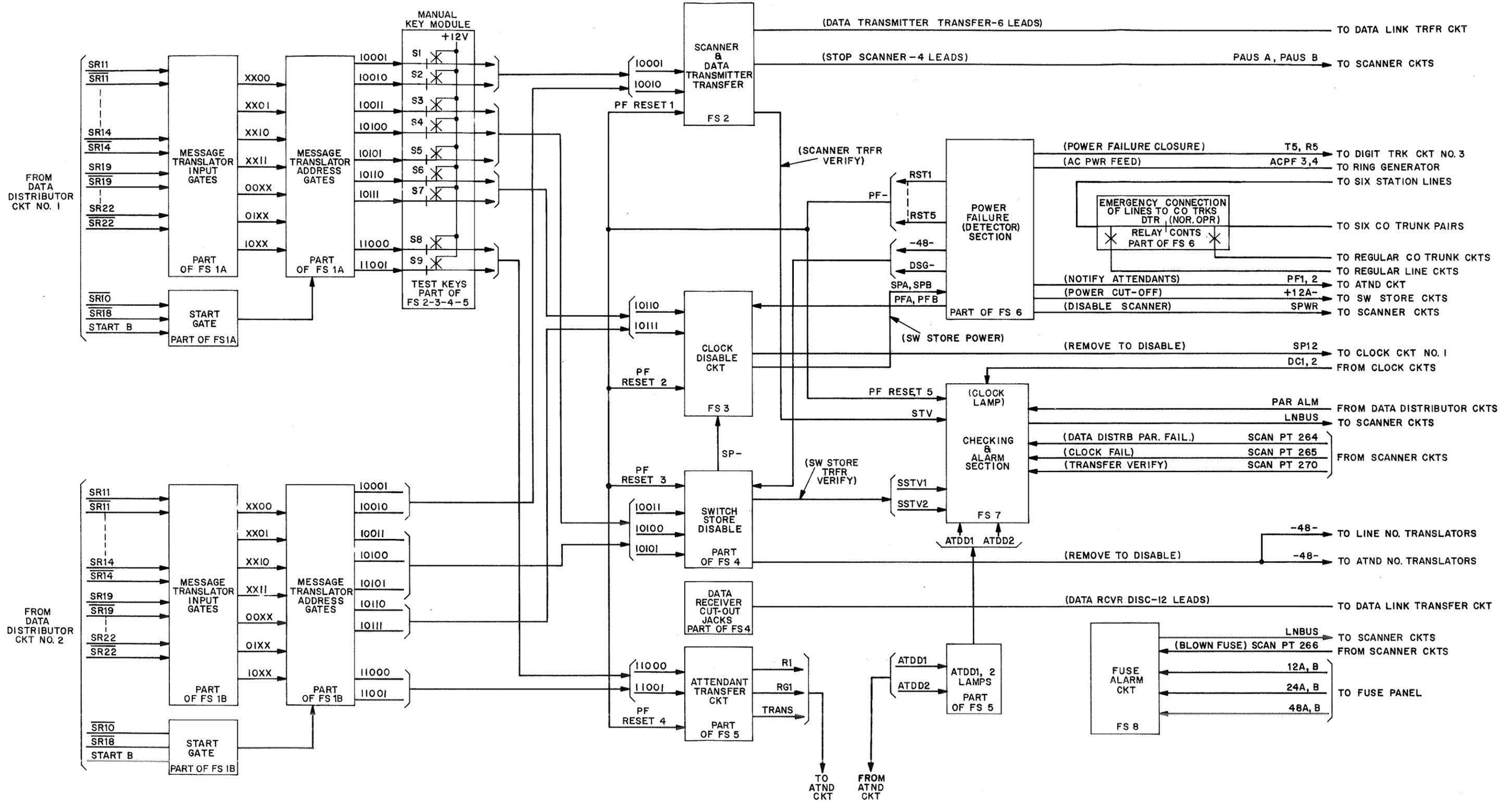


Fig. 14 - Transfer and Alarms Circuit

alarms circuit requires only a 5-bit input word in an incoming message to define all of its designed transfer functions. In order to provide the greatest defense against mutilated incoming messages, the 5-bit word is contained twice within the transfer and alarms circuit message. That is, the 47-bit incoming message will have bits 10 through 14 the same as bits 18 through 22. This circuit will not properly translate to 2-out-of-7 unless the two 5-bit words agree perfectly.

C. Start Gates

13.04 A signal called START B is sent to two identical START GATES from each data distributor when an incoming message is addressed to the transfer and alarms circuit. These pulses are combined with the first bit of both 5-bit words (mentioned in Section B. Message Translator Input Gates) in *and* circuits of both start gates. The outputs of the START GATES trigger the movement of the contents of both MESSAGE TRANSLATOR ADDRESS GATES to various disabling circuits.

D. Message Translator Address Gates

13.05 This circuit, composed of nine *and* gates, performs a 1-out-of-9 translation from the 2-out-of-7 code produced by the input gates. The output leads of this circuit are shown designated in binary in Fig. 14. This circuit is also duplicated. Each input gate circuit feeds a different address gate circuit to override the partial disabling effect of a single internal failure. Only one of the nine output leads of each of the address gates will go positive in response to one incoming message.

E. Manual Key Module

13.06 Complete manual control of all transfer functions is accomplished by connecting a positive voltage potential through the nine transfer keys of this circuit. It should be noted that since both address gates perform the same function on the common disabling or transfer circuit, it is not necessary to provide a duplicate set of manual keys.

F. Scanner and Data Transmitter Transfer

13.07 When the lead 10001 goes positive, it will cause a relay to operate which will connect the output of data transmitter 1 to the data pair going to the control unit. Since the output of

scanner 1 is permanently connected to data transmitter 1, scanner 1 will be in use. When lead 10010 goes positive, the relay will be released and data transmitter 2 will be connected to the data pair; ie, scanner 2 is in use.

13.08 During the actual operate time of the relay, no messages are allowed to be sent. This is done by stopping both scanner clocks which prevents them from sending messages. However, since one of the scanners is always in use, sufficient time must be allowed to let a message in progress be transmitted.

13.09 The leads PAUS A and PAUS B to each scanner are the leads which stop each scanner at the right times. During any scanner transfer the scanner not in use is stopped first (PAUS A and PAUS B to that scanner go to ground). The scanner in use at the time of transfer is allowed to run for 70 msec (PAUS A and PAUS B to that scanner go to ground after 70 msec). Approximately 25 msec later the relay is allowed to operate or release depending on the direction of transfer. An additional 200 to 300 msec is allowed before both scanners are permitted to proceed (both sets of PAUS A and PAUS B go positive). This long quiet period is necessary to allow the new data transmitter in use to settle to a stable state since it might be triggered by relay transients and contact chatter.

13.10 When the relay operates in either direction, the SCANNER TRFR VERIFY lead will go positive during the transfer time of the relay armature, providing an indication to the checking circuit (to be described later) that the relay actually operated or released.

G. Clock Disable Circuit

13.11 If clock 1 (normally in use) should fail, clock 2 will immediately take over without any assistance from the transfer and alarms circuit. The failure will cause an alarm (ie, scan point off-hook) to be generated in the checking and alarm circuits (discussed later). The control unit will be informed of the failure through normal scanner operation and will respond with a message which causes lead 10110 to go positive. This will cause lead SP12 supplying power to clock 1 to go to ground, thereby completely disabling clock 1. Leads SPA and SPB which feed special power to both switch stores through

the power failure section of the transfer and alarms circuit go to ground when any clock disabling or enabling action occurs in order to prevent losing information stored in memory registers during possible skips in the clock frequency. Leads SP-, PFA, and PFB also cause leads SPA and SPB to go to ground whenever a switch store is disabled or a power failure occurs. Lead PF RESET 2 presets this circuit to order clock 1 in use when power is first applied or restored to the switch unit.

H. Switch Store Disable

13.12 A positive signal on lead 10011 will remove -48 volts from the -48-1 lead which goes to switch store 1. A positive signal on lead 10100 will similarly remove power from the -48-2 lead which feeds power to switch store 2. A positive signal on lead 10101 will restore -48 volts to both -48-1 or 2 leads. The design of this circuit will not allow the removal of power from both -48-1 or 2 leads at once for this would disable both switch stores simultaneously. The removal of power involves the use of two relays which have contacts wired to produce a positive voltage during the transfer time of the relay armature on leads SSTV1 and SSTV2. Lead PF RESET 3 presets this circuit to apply power to both switch stores when power is first applied or restored to the switch unit.

I. Attendant Transfer Circuit

13.13 A positive pulse on lead 11001 will cause the attendant circuit to select its input from data distributor 2 by applying voltage to lead R1. A positive pulse on lead 11000 will cause the attendant circuit to select its outputs from data distributor 1 by removing voltage from lead R1. Leads R1 and RG1 are a source of +24 volts and a ground return path respectively and control the operation of 3 parallel-connected transfer relays within the attendant circuit.

13.14 The input lead PF RESET 4 is used to preset the attendant circuit to select the outputs of data distributor 1 whenever a power failure occurs.

J. Power Failure Detectors

13.15 The switch unit power supplies provide ac monitoring power to the transfer and alarms circuit via the ring generator on leads

ACPF 3 and ACPF 4. Special detectors in this circuit are satisfied only if the input voltage to the switch unit is above 95 volts ac. The dc outputs of the +12, +24, and -48 volt power supplies are also monitored by this circuit. Low ac or missing dc is sufficient to cause a power failure indication. When a failure occurs, four relays are released transferring six preselected stations to direct wire connections with the central office to provide emergency communication. The four relays are symbolized by the contacts shown in the block of Fig. 14 called Emergency Connection of Lines to CO trunks. The same released relays also provide +12 volts (if a partial power failure occurred) on leads RST1 to RST5 and remove voltage on leads +12A-1 or 2, -48-1 or 2, and SPWR in order to completely disable the switch stores, line and attendant number translators, and scanners respectively. Additionally, a 400-ohm connection between leads T5 and R5 (tip and ring of digit trunk 3) is closed. This informs the control unit of a power failure at the switch unit by causing a relay connected between tip and ring of digit trunk No. 3 cable pair at the control unit to operate. A power failure signal is also sent to the attendant circuit on leads PF1, 2.

K. Checking and Alarm Circuit

13.16 Three major functions are performed by this circuit. The outputs, in the form of three separate off-hook scan points (264, 265, 270), serve to inform the control unit via the scanner of any change in the inputs to this circuit.

13.17 The input PAR ALM is a dual input. Each data distributor will generate an output pulse on a PAR ALM lead whenever the number of bits in any message to it is even. Since both leads are connected to this circuit and perform the same function, a single parity failure in either path will activate the circuit. A positive pulse on PAR ALM will cause scan point 264 (both scanners) to go off-hook. If a switch store is disabled for any reason, the PAR ALM lead from the corresponding data distributor will be grounded to prevent unintentional generation of parity alarms.

13.18 If clock 1 fails, lead DC1 will go positive. Similarly, DC2 will go positive if clock 2 fails. A positive potential on either lead will cause scan point 265 to go off-hook, thereby

informing the control unit of the failure. A transfer verify indication is also given (scan point 270).

13.19 Any transfer function performed by the transfer and alarms circuit will directly or indirectly cause positive voltage to appear on leads STV, SSTV1, SSTV2, ATDD1, ATDD2, DC1, and DC2. These inputs drive an *or* circuit, the output of which causes scan point 270 to go off-hook. The control unit is thus informed of all transfer verify actions performed by the transfer and alarms circuit.

13.20 The lead PF RESET 5 will cause a parity alarm to be sent to the control unit when a partial power failure occurs or when power is restored after a complete power failure. This is done to override the signals on the two PAR ALM leads since the distributors may generate erroneous parity alarms during a power failure condition.

L. Fuse Alarm Circuit

13.21 This circuit monitors the normally floating state of the +12, +24, and -48 volt fuse alarm buses in both halves of the switch unit. Each switch unit half is fused separately. If any fuse blows, one of the three voltages will be applied to this circuit which responds by causing scan point 266 to go off-hook and to remain so until the fuse is replaced.

M. ATDD1, ATDD2 Lamps

13.22 The same relay which causes the attendant circuits to select their inputs from data distributor 1 or 2 also applies a ground to one of the lamp leads ATDD1 or ATDD2. This provides a visual indication of which data distributor is being used by the attendant circuits for their input information.

N. Visual Indicators

13.23 Several other visual indications in addition to the attendant status lamps are provided in the transfer and alarms circuit. Since they are controlled directly by this circuit (except the clock alarms) and not by the circuits with which they are associated, they

will be discussed in this one section. Fig. 14 does not show the lamps listed below.

LAMP	INDICATION (Illuminated)
S1	Scanner 1 in use
S2	Scanner 2 in use
SS1	Switch store 1 disabled
SS2	Switch store 2 disabled
CLKD1	Clock 1 disabled
CLKD2	Clock 2 disabled
FA1	Blown fuse switch unit half 1
FA2	Blown fuse switch unit half 2

O. Data Receiver Cutout Jacks

13.24 Both data receivers are driven from the same incoming message through a splitting pad and then through these individual jacks in order to permit monitoring the frequency shift input to both data receivers. Caution must be observed in the use of either of these jacks because they will interrupt the input signal when both switch stores are operating. If switch store 1 is disabled, however, jack J1 may be used at any time for monitoring since in this case the jack will be bridged across the signal pair. Similarly, J2 may be used at any time if switch store 2 is disabled.

14. CENTRAL OFFICE TRUNKS, TIE TRUNKS, AND SPECIAL TRUNKS

A. General

14.01 Up to this point in the discussion of the switch unit, little emphasis has been placed on trunk circuits which permit the switch unit to communicate with a central office or another private branch exchange. Selected subscribers, as in any PBX, may be allowed access to the telephone systems outside their own local system. Central office trunks provide a communication link with local central offices. Tie trunks of several types are required to permit communicating with other private branch exchanges. The following paragraphs describe the functions of these circuits. More detail is provided in Section 240-107-101.

B. Central Office Trunk

14.02 A subscriber who dials 9 or who requests an outside line through one of the attendants will be time division-connected to one

of the central office trunks in the switch unit. The output of the central office trunk is wired to the control unit where it connects to another circuit also known as a central office trunk circuit. This is primarily a relay control circuit which provides a talking path and dialing capability to a local central office. A normal central office call proceeds as follows: subscriber goes off-hook and is connected to a digit trunk, subscriber dials 9, control unit acknowledges the request for an outside line and retains the subscriber connection to the same digit trunk so that the outside number to be dialed will be sent to the control unit, control unit also reserves a central office trunk for use on this call. Upon completion of the first three digits of a possible 10-digit number, the control unit begins to outpulse the digits on the reserved control unit central office trunk. When the last digit has been dialed by the subscriber, the control unit erases the connection between the subscriber and digit trunk and connects the subscriber to the switch unit central office trunk circuit. A talking path is thereby set up to the local central office.

C. Tie Trunk and Idle Terminated Trunk

14.03 Both of these trunks perform the same function. The tie trunk, however, is used on trunk circuits which are not equipped with line repeaters. Idle terminated trunks present a load impedance of 900 ohms during idle periods as well as active periods. This permits them to be used on long trunk circuits containing repeaters which will sing (howl) if not properly terminated.

14.04 These types of trunks are a combination of a line circuit and a central office trunk having a common tip and ring feed. Their operation is as follows: a subscriber at another PBX is connected to a pair which terminates at the switch unit in an idle terminated or tie trunk, and the scan point of the central office portion of the trunk will respond by going off-hook. Therefore, the control unit is informed that an incoming call is present and will respond by ordering a time division connection between the line circuit portion of the trunk and one of the switch unit attendants. The attendant will answer and transfer the call to the desired extension.

D. Long Line Circuit

14.05 The long line circuit is used to extend the signaling range. Normal line loops are less than about 300 ohms and are ordinarily confined to an office building. Longer loops sometimes leave a local area and are subject to signaling difficulties. This circuit is designed to prevent interference with the normal operation of the supervisory portion of the circuit, and for long loops, is used in place of a standard line circuit.

E. DID Trunk

14.06 The switch unit end of a DID trunk circuit is like a line circuit without the ringing section. When the control unit end of a DID trunk is seized by an incoming call, the switch unit end of the DID trunk circuit scan point is made to transmit an off-hook indication. A series of bidirectional switch unit-to-control unit messages establishes a time division connection between the switch unit DID trunk and a digit trunk. This permits the central office to pulse the desired switch unit station number through the DID trunk-digit trunk connection and back to a control unit digit receiver. There, call processing will follow the normal programming given to the standard method of connecting an A party (incoming call) to a B party (called switch unit station).

F. 4-Wire Trunk Circuit

14.07 Simplex signaling on 4-wire trunks in some installations appears at the control unit. The trunks are carried to the switch unit as 4-wire circuits. At the switch unit the 4-wire trunk circuit converts the simplex signaling to ordinary 2-wire signaling. Incoming calls on this type of trunk are then handled as if the call were being made locally; ie, the trunk looks like another switch unit extension.

15. TEST LINE CIRCUIT

A. General Description

15.01 Periodically the control unit plays question and answer with the switch unit. Maintenance messages direct the switch unit to set up periodic test calls. Over an extended time, test calls will be made in all time slots on both talking buses in every switch unit operating from the common control unit. The results of the test calls (good or bad) are detected by the

scanner and returned to the control unit. Since establishing telephone calls requires the normal operation of nearly all major units within the switch unit, a test call failure will provide an indication of system abnormality.

B. Test Line A

15.02 This circuit performs three functions.

When it is time division-connected to either talking bus, it applies a 500-cps signal to the bus during one time slot. This circuit also counts the number of times its time division gates are pulsed by the line number translator in any 80- μ sec period (normal sampling rate). If the gates are pulsed no more than once within 80 μ sec, its scan point (7) is caused to produce an off-hook indication. The third function of test line A is to periodically check that the switch unit is capable of ringing stations. It does this by detecting the presence of a signal-to-ring (3 volts dc) on the talking bus when an incoming message directs the test line to be called. The ring signal appearing on the bus causes a second scan point (6) in the circuit to go on-hook. This scan point is normally held in an off-hook state by the presence of both +24 volts and -48 volts. These special voltage leads are routed (interlock fashion) through the other printed circuit cards which comprise the over-all test line circuit. If any one of the test circuit cards is pulled, scan point 6 will go on-hook and will remain so until the card is replaced. This is effectively an answer to a question not asked by any maintenance message. The maintenance program of the control unit will accept this as an indication that a test line card has been pulled and will not initiate any orders to begin transferring equipment in an effort to find a working mode.

C. Test Line B

15.03 This test line is the listener. It can be time division-connected as party A or B to either talking bus in any time slot by the line number translator as directed by an incoming maintenance message. If it is connected by itself in the time slot, it listens for noise on the bus. Excessive noise will cause its scan point (248) to go off-hook. Test line B can also be time division-connected to test line A by a maintenance message. In this case, test line B should respond to the 500-cps signal supplied by line A by going off-hook. This is an indication that the

transmission loss encountered by the 500-cps signal is not excessive.

D. Test Calls

15.04 The switch unit maintenance program in the control unit expects to receive the correct answers (scan points on-hook or off-hook) when it originates various types of test calls. The table shown below lists some of the test calls which are made and the answers expected.

A PARTY	B PARTY	TEST	SCAN POINT RESPONSE
None	Line B	Crosstalk (noise)	SP 248 no change
Line A	Line B	Transmission	SF 248 off-hook
Line A	Line B	Sampling Rate	SP 7 off-hook
Line B	None	Crosstalk	SP 248 no change
Line B	Line A	Transmission	SP 248 off-hook
Line B	Line A	Sampling Rate	SP 7 off-hook
Ring Sig	Line A	Ring	SP 6 on-hook
Ring Sig	Line A	Sampling Rate	SP 7 off-hook
Line B	Ringback Sig	Ringback	SP 248 off-hook
Line A (bus 1)	Line B (bus 2)	Conference	SP 248 off-hook

16. SWITCH UNIT TEST SET

A. General

16.01 Circuit malfunctions within the switch unit are detected by the failure of periodic test calls made by the maintenance program of the control unit. The defective major section or sections of the switch unit will be removed automatically, and an alarm will be generated at the control unit indicating the general area of trouble. The subsequent repair (by package replacement) of the fault depends upon the ability of the repairman to localize the trouble within a major section of the switch unit. The test set shown in Fig. 15 aids in

localizing faulty circuits by employing a 2-bit comparator, a message detector, and a frequency indicator.

B. 2-Bit Comparator

16.02 This circuit aids in shooting troubles which may occur somewhere within one of the duplicated sections of the switch unit. Since many of the duplicated circuits operate synchronously, individual stages within these circuits can be compared.

16.03 The outputs of stages to be compared are connected individually to inputs A and B of the 2-bit comparator. Input C is used to derive a strobe pulse. This allows pulse comparisons to be made only during specific times. The outputs of gates GA and GB will both be ground as long as both inputs are either positive or ground. Under these conditions, FF3 will be reset and the OK lamp will be illuminated. If a difference of polarity exists between inputs A and B, the three inputs of either GA or GB will be at ground. The output of that gate is positive which sets FF3 to illuminate the ER-ROR lamp.

16.04 A pulse from the switch unit known to occur before or during the time a comparison is to be made is connected to the input (C) of TRIG. Its output triggers a series of four stages (MP1, INV5, MP2, INV6) which function to produce a positive 0.250- μ sec pulse from MP2 delayed by MP1. The ground going output of INV6 gates the contents of GA and GB to FF3.

C. Message Detector

16.05 Special test messages can be sent to the switch unit from the control unit on request. These messages are repeated about every second and can be directed to either switch unit half. The IN1 to IN32 inputs of the message detector can be connected to the 32 output stages of either data distributor; and the test set can be preset, by means of 32 switches, to agree with a known incoming message. If the data distributor fails to catch the test message, the message indicator (MSG IND 1) lamp will not light.

16.06 Inputs IN1 through IN32 connect to 32 message detector circuits, each of which generates a positive output only when the input

agrees with the corresponding switch setting. Each switch has a third neutral position, do-not-care (DC), which permits a positive output regardless of the input. All 32 outputs are then *anded* at the input of THRESHOLD GATE 1, provided the separate-input, combined-input (SEP IN-COMB IN) switch is in the latter position. If one or more of the inputs to the *and* gate is at ground indicating a mismatch between the switch settings and the inputs, its output will be ground, thereby inhibiting the set pulse to FF1 and causing MSG IND 1 to remain extinguished (previously extinguished by RST 1). THRESHOLD GATE 2, INV2, and FF2 perform the same function on the last eight input signals provided the circuit is set for SEP IN and detector (DETR 2) operation. The reason for the division of the 32 inputs into two groups (24 and 8) is to permit the test set to be used in different portions of the switch unit where all 32 inputs are not required.

D. Frequency Indicator

16.07 Any individual stage within the switch unit which generates a periodic output pulse can be checked by this portion of the test set.

16.08 A periodic pulse is connected to input C of the test set which is switched to operate in the pulse frequency (PULSE FREQ) position. The input pulse triggers MP1, and its output pulse will cause the meter rectifier containing an RC time constant to develop an average output voltage which is proportional to the input frequency. The rotary switch allows a wide range of frequencies to be read by changing the MP1 output pulse width.

E. High Voltage Interface

16.09 An auxiliary circuit called HIGH VOLTAGE INTERFACE is provided to reduce the amplitude of the 48-volt switch unit translator driver output signals to normal logic levels. The horizontal-normal-vertical (H-N-V) switch allows the interface circuit to accommodate both ground-going or negative battery-going pulses. The output signals at jack M5 are of proper amplitude to drive the frequency indicator portion of the test set via input C.

16.10 Inverting gate INV7 is used to correct the polarity of one switch unit signal before comparing it to another in the 2-bit com-

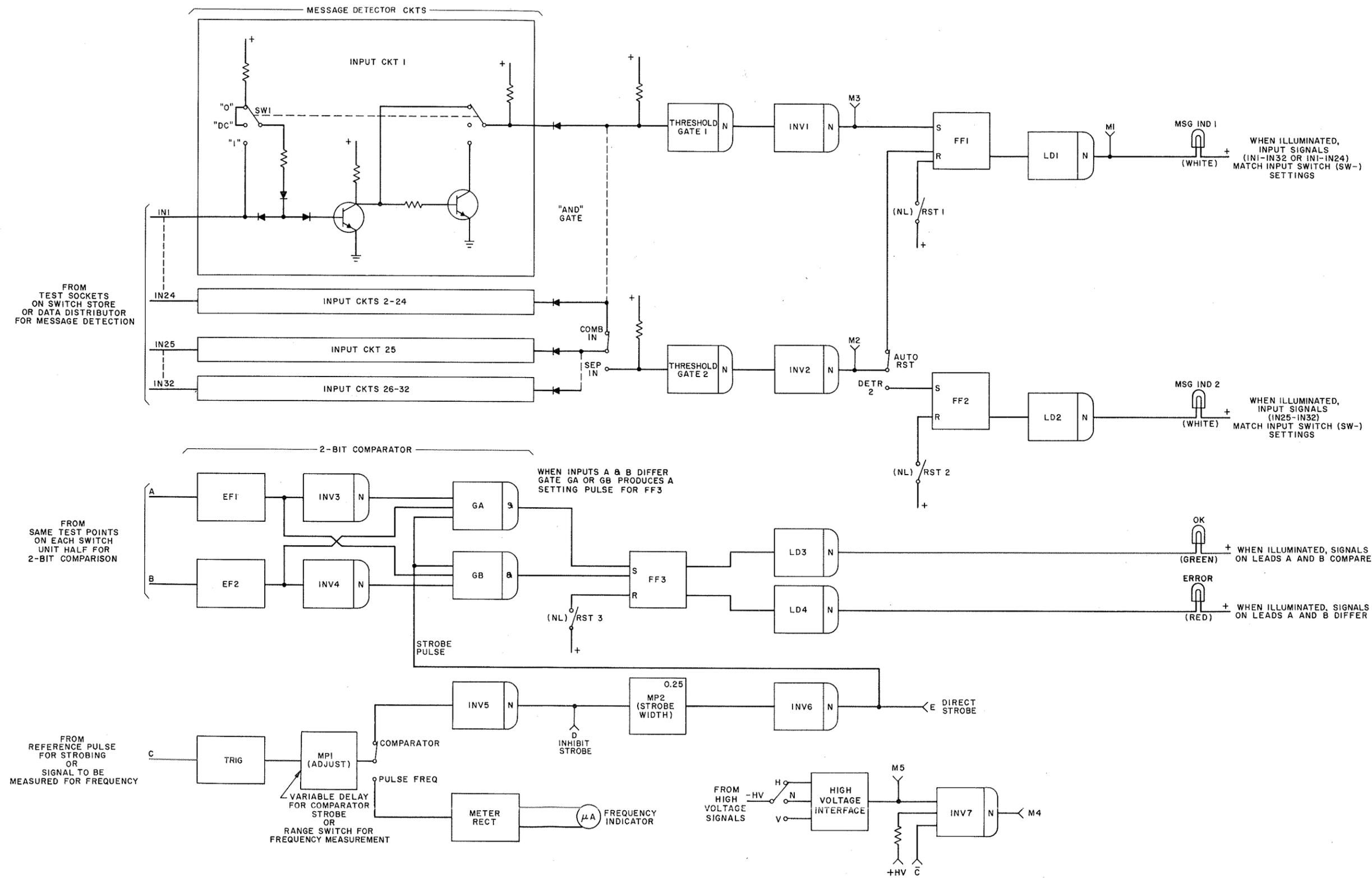


Fig. 15 - Switch Unit Test Circuit

parator. An added input, jack +HV, accepts 24-volt positive battery pulses and reduces them to normal logic levels for use in other parts of the test set.

17. DRAWING REFERENCES

17.01 The following SD drawings and associated circuit descriptions (CDs) give additional information. These are not attached.

Switch Store Circuit for Switch Unit	SD-1H003-01	Conference Circuit for Switch Unit	SD-1H013-01
Line Number Translator Circuit for Switch Unit	SD-1H004-01	Attendant Circuit for Switch Unit	SD-1H014-01
Attendant Number Translator Circuit for Switch Unit	SD-1H005-01	Test Line Circuit for Switch Unit	SD-1H016-01
Line Circuit for Switch Unit	SD-1H006-01	Transfer and Alarms Circuit for Switch Unit	SD-1H017-01
Digit Trunk Circuit for Switch Unit	SD-1H007-01	Ring-Ringback Logic Circuit for Switch Unit	SD-1H018-01
Central Office Trunk Circuit for Switch Unit	SD-1H008-01	Clock Circuit for Switch Unit	SD-1H019-01
Tie Trunk Circuit for Switch Unit	SD-1H009-01	Tone Generator Circuit for Switch Unit	SD-1H020-01
Bus Clamp and Interbus Circuit for Switch Unit	SD-1H010-01	Data Link Transfer Circuit for Switch Unit	SD-1H021-01
Scanner Circuit for Switch Unit	SD-1H011-01	Ringing Generator Circuit for Switch Unit	SD-1H022-01
Data Distributor Circuit for Switch Unit	SD-1H012-01	Direct-In-Dialing Trunk Circuit for Switch Unit	SD-1H023-01
		Idle Terminating Trunk Circuit for Switch Unit	SD-1H024-01
		Long Line Circuit for Switch Unit	SD-1H025-01
		4-Wire Tie Trunk Circuit for Switch Unit	SD-1H027-01
		Data Receiver Circuit for Switch or Control Unit	SD-1H031-01
		Data Transmitter Circuit for Switch or Control Unit	SD-1H032-01
		Switch Unit Test Set	SD-1H070-01