3A SWITCH UNIT

DESCRIPTION OF SYSTEM OPERATION

NO. 101 ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

1.01 This section describes the 3A basic switch unit (J1H013A, J1H013B, and J1H013C), the auxiliary line group unit (J1H013D), and the auxiliary time division control circuits unit (J1H013E). The purpose of this section is to provide information concerning the theory of operation and functional description of the switch unit circuitry.

1.02 The 3A switch unit is a part of the No. 101 Electronic Switching System (ESS). The

No. 101 ESS is a distinct departure from any previous PBX system in that it provides service to a multiplicity of PBX subscribers, employs stored program control in lieu of wired logic, and radically reduces the amount of equipment on subscriber premises. This reduction of equipment stems from the use of ***time division switching*** in the switch unit for the talking connection and from the remote common control organization.

1.03 Fig. 1 is a block diagram of the No. 101 ESS which consists of one control unit and one or more switch units. The control unit is generally located at the central office. The switch unit associated with a given customer is generally located on the customer premises. The switch unit establishes talking connections between PBX station, trunks, and attendant consoles in accordance with information provided by the control unit. The exchange of information between the switch unit and control unit, and vice versa, is accomplished by a 2-way voice frequency data link.

1.04 The control unit consists of input-output circuits and a call processor. The input-output equipment receives supervisory data and dialed digits from the switch unit for storage until requested by the call processor. The call processor works with one switch unit at a time and on one call at a time. The call processor is the program controlled decision making portion of the control unit, which arranges for setting up and supervising calls at all of its switch units and provides output information for the input-output circuits and the switch units.

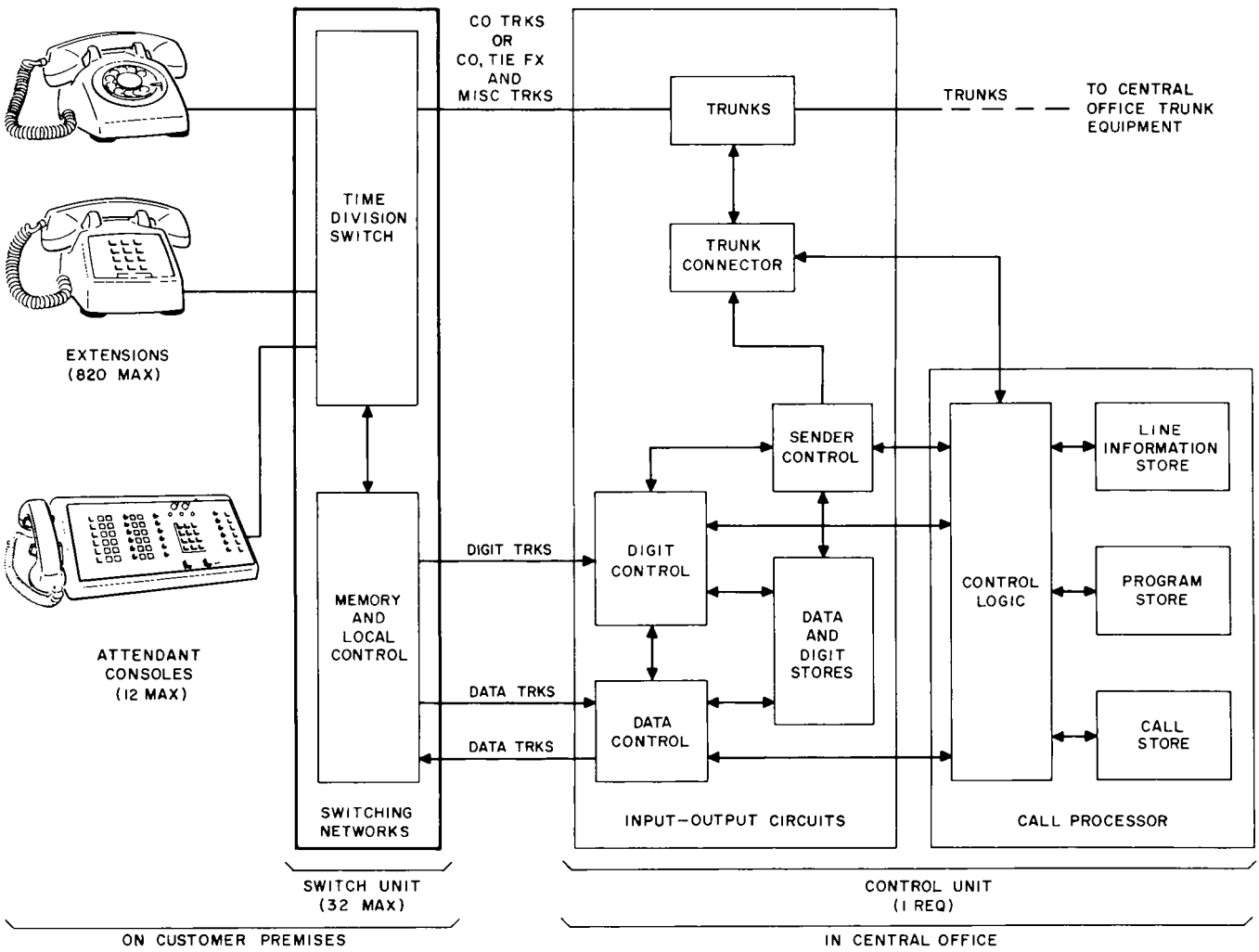


Fig. 1—No. 101 Electronic Switching System—Block Diagram

The output information includes data messages for transmission to switch units and digits to be out-dialed over trunks to a central office or another PBX. The sender control provides the out-dialing function for trunks. Thus the information from the call processor is routed to the proper destination by the input-output equipment. The input-output equipment is capable of working with all the switch units simultaneously.

1.05 The 3A switch unit passes information and is controlled by the control unit by means of data messages sent over data trunks, one for each direction of data transmission. Supervisory ***change information*** at the switch unit is transmitted to the control unit. Information for establishing time division connections, performing maintenance functions, and lighting attendant lamps is transmitted from the control unit to the switch unit.

1.06 The switch unit can be equipped to serve up to 820 PBX extensions and 112 trunks where maximum lines are required; 696 extensions and 220 trunks can be served where maximum trunks are required. Provision is made for up to 12 attendant consoles. The switch unit is designed to support the overall system objective of concentrating the call processing work in the common control unit with the least possible amount of work being done in the customer switch unit.

1.07 The major functional requirements of the switch unit are to provide:

(a) Suitable terminations for station lines and the various types of trunks

(b) Means for detecting changes in supervisory states of lines, trunks, attendant console keys, and maintenance scan points

(c) Means for communicating with the control unit

(d) Means for receiving information from the control unit

(e) Means for storing information received from the control unit

(f) A switchable network for connecting transmission paths for lines, trunks, attendants, lamps, and tone sources

(g) Means for controlling circuitry for maintenance purposes.

TRANSMISSION AND CONTROL

1.08 The 3A switch unit employs ***time division switching*** as opposed to a space division switching network. Time division switching utilizes the principle of speech sampling to establish a number of simultaneous conversations over a transmission path. The talking connection is not established continuously, but is made for extremely short intervals repeated at a high enough rate to give the effect of a continuous connection.

1.09 The time division switching network in the basic switch unit as a whole has a capacity for 120 time slots. Thus, if required by traffic, 120 simultaneous connections could be established by the basic switch unit for serving a maximum of 820 stations. The network in the switch unit is divided into two parts called time division control units, each containing a time division bus so that, in case of trouble, the affected half can be taken out of service. Service will be maintained by the other half on a reduced traffic capacity basis (60 talk connections maximum) for the duration of the trouble. The two time division buses are provided for reliability. One or two additional time division control units may be employed to produce a maximum of 180 or 240 simultaneous talk connections when the additional traffic handling capability is required. Each line and trunk has access to each of the time division buses.

1.10 The switch unit employs a store memory unit to store the talk connection information originated in the control unit. The memory words are 32 bits in length; 60 words are allocated in the memory unit of each time division control unit to contain the talking time slot information. The talking time slot words contain the binary address of the lines to be interconnected and are delivered from the memory on a per-time-slot basis. The words are read and translated, producing operation of the appropriate switches to provide the required pattern of talk paths between different line circuits. Other information translated from the talking time slot word is associated with attendant facilities, ring-ringback circuitry (continuous or interrupted), conference calls, trunk gain switching, and maintenance functions.

1.11 Speech transmission for the attendant is provided by time division switching connections similar to the transmission connections for lines or trunks. Signals for controlling the attendant console lamp indications are derived from data messages received from the control unit. Console key operations are detected and treated as off-hook supervisory signals and transmitted to the control unit for interpretation.

1.12 All lines and trunks are continuously scanned to detect changes in supervisory status. When a change of status (on-hook to off-hook, for example) is detected, a data message is sent to the control unit to notify it of the change. The control unit receives this information, processes it, and when appropriate, sends a message to the switch unit which contains the information required to establish a time division connection.

1.13 In the initial stage of a station originated call, the switch unit is instructed to temporarily produce a time division connection between the calling party line circuit and a specified digit trunk for out-dialing. All dialing is transmitted from the switch unit over digit trunks to the control unit as audible tones. TOUCH-TONE® signals are transmitted without modification, but if the dialing originates from a rotary station, the line-break signals are converted to audio frequency tone bursts for transmission over the digit trunk.

1.14 When dialing is completed, the control unit sends a talking time slot message to disconnect the digit trunk and connect the called party. The talking time slot message also contains information which prescribes the type of ringing signals to be applied to the line circuit of the called station.

1.15 When the called party answers (goes off-hook), the ringing operation is terminated by the line circuit ringing relay; the control unit responds to the change in supervisory state with a new talking time slot message in which the ringing bit has been removed. The time division connection, thus established between the calling and called parties, continues in operation until a change in the supervisory state of one or both parties causes one or two data messages to be sent to the control unit. The control unit processes these messages and sends one or two messages to the switch unit to terminate or modify the connections.

MAINTENANCE

1.16 The switch unit is highly reliable due to duplicated circuits and the ability to transfer control, by control unit command, to the duplicate circuit in case of a malfunction. The extensive use of plug-in circuit packages with their rapid repair-by-substitution capability reduces the maintenance effort appreciably. The control unit automatically prepares and types a trouble message on a teletypewriter (TTY) in the central office as a guide to maintenance.

1.17 Message and hardware control circuits of the maintenance and attendant circuit provide direct control over the service status of the two parts of the switching network as well as that of certain other redundant features. The control unit continually establishes various test call connections at the switch unit and is rapidly informed of any difficulty in the switch unit. When switch unit trouble conditions arise, the maintenance circuits provide a means of switching the redundant portions of switch unit circuitry in and out of service to maintain a satisfactory working mode. The maintenance and attendant circuits provide the following four maintenance circuits:

- Message controlled
- Hardware controlled
- Checking and alarm
- Power failure.

EQUIPMENT ARRANGEMENT

1.18 Fig. 2 is the basic 3A switch unit equipment arrangement. The basic switch unit consists of three frames (J1H013A, J1H013B, and J1H013C). The J1H013A frame provides fuses, alarms, transfer, storage, and control circuits for the line, trunk, and special groups of the J1H013B and J1H013C frames. The special group consists of tone generators, tone switches, digit trunk circuits, attendant lamp power supply, and attendant line circuits. Four line or trunk circuits are provided per circuit package and the circuit packages are arranged in groups of 16 to accommodate up to 64 lines or trunks. The basic switch unit cabinet provides up to 9 groups (0-3 and 5-9) which may be equipped with up to 436 lines and 112 trunks where maximum lines are required or 312 lines and 220 trunks

where maximum trunks are required. The J1H013C cabinet also contains the intergroup switch circuit and data transmitter and receiver circuitry. The intergroup switch circuit provides a time division switched transmission path between line or trunk groups.

1.19 Fig. 3 is the equipment arrangement for the auxiliary units and optional feature unit. The J1H013D auxiliary line group cabinet provides 6 additional line circuit groups (10-15) with up to 384 additional lines which would bring the total to 820 lines when equipped for maximum lines. The J1H013E auxiliary time division control cabinet may be equipped with circuit 2 or circuits 2 and 3 to increase the traffic handling capacity.

1.20 Additional equipment may be provided in the optional feature cabinet (J1H013F) shown in Fig. 3. This cabinet and additional wall cabinets may be provided to accommodate such special features as attendant direct station selection (ADSS), trunk repeaters, recorded telephone dictation circuits,

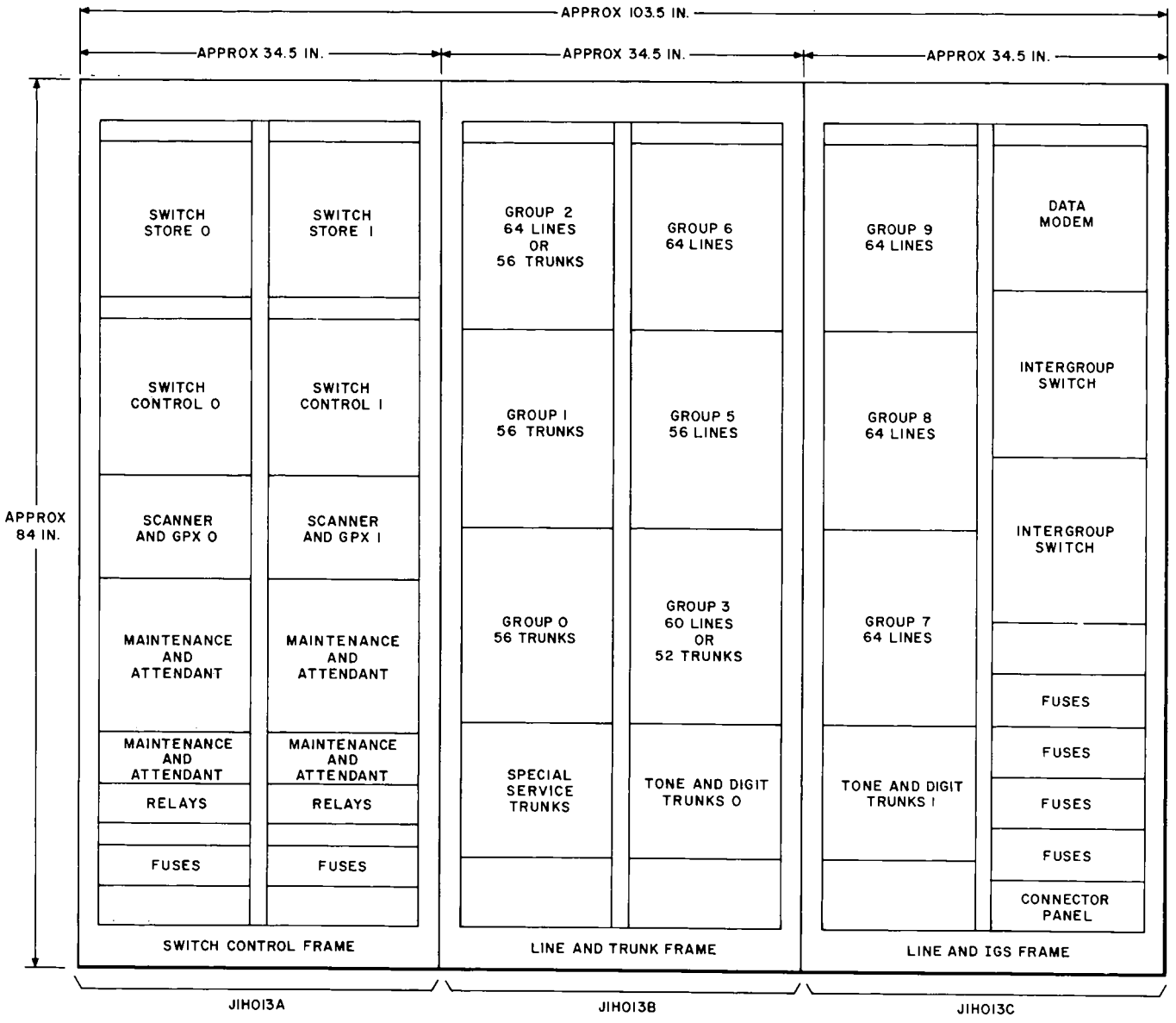


Fig. 2—Basic 3A Switch Unit Equipment Arrangement

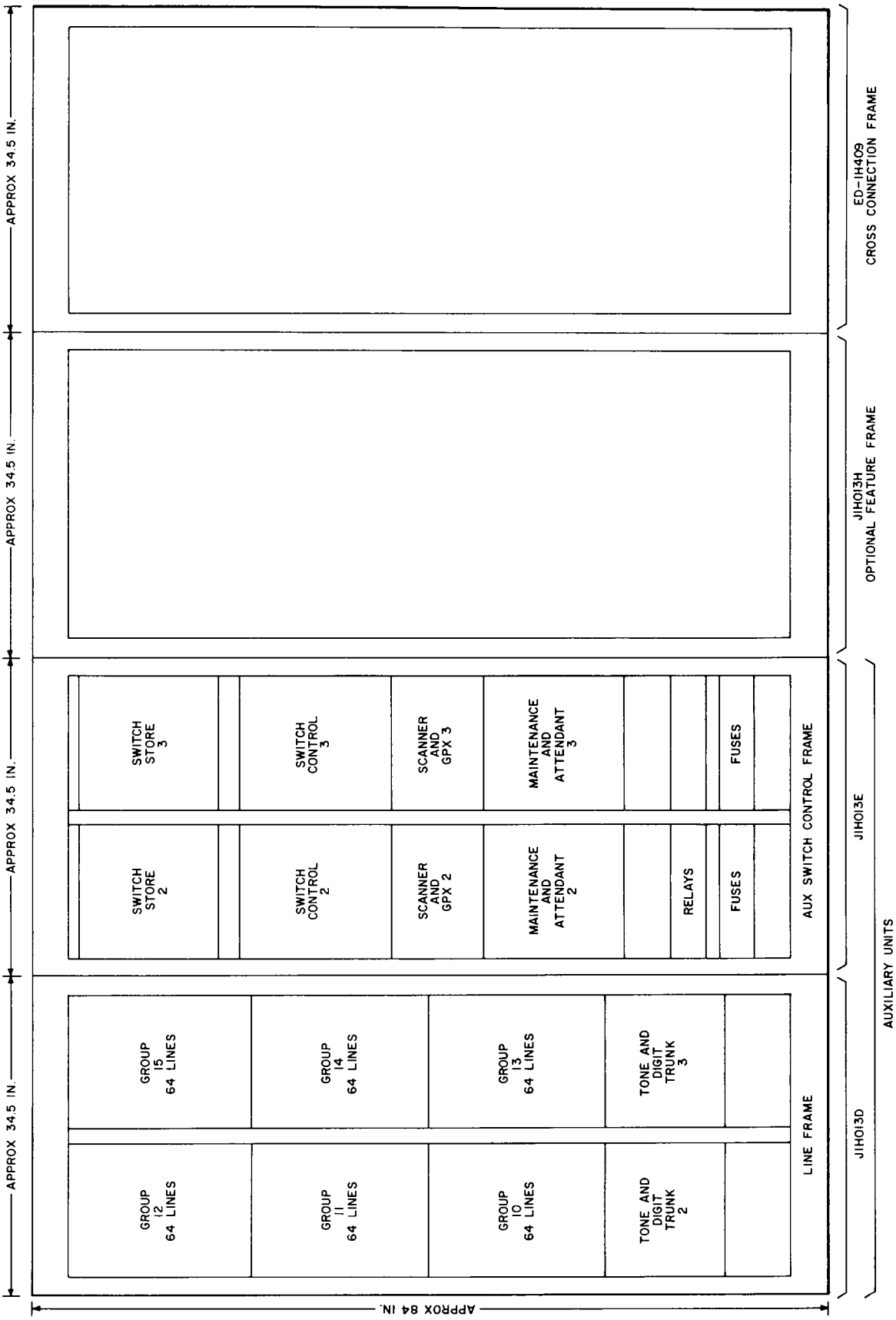


Fig. 3—Auxiliary Units and Optional Feature Unit Equipment Arrangement

code call circuits, key telephone units, station line transfer relays, or emergency power.

2. SWITCHING NETWORK

2.01 Fig. 4 is a simplified block diagram of the 3A switch unit consisting of the switching network portion which produces time division connections under control of the memory and local control portion. The switching network portion consists of the time division switch (line, trunk, intergroup, attendant, and tone), common bus (group, intergroup, and special group), and tone generator circuits. The memory and local control portion consists of the switch store, switch control, scanner, attendant, data receiver, data transmitter, and maintenance circuits. Although two, three, or four network control and intergroup switch circuits may be provided, only one circuit is illustrated for the sake of simplicity.

CALL ORIGINATION

2.02 A request for service is produced when the calling party goes off-hook. In an off-hook condition the subset presents a low-impedance path for line current, which produces a positive dc voltage across the line supervisory circuit. The line supervisory circuit is part of the line circuit unit which, if off-hook when interrogated by the scanner circuit, produces a pulse output.

2.03 The scanner compares the present-look status with the last-look data recorded for the line. Since a change in the supervisory status is noted (on-hook to off-hook), the scanner will signal the outgoing message control circuit to send a message to the control unit at the central office. The control unit recognizes the received message as a dial tone request. An idle time slot and digit trunk are selected, and a message containing the requesting line number as the calling party and the digit trunk number as the called party is sent to the switch unit. The message address indicates the idle time slot number.

2.04 The incoming 47-bit serial message at the switch unit is loaded into two temporary storage words a bit at a time. After the parity is successfully checked by the incoming message control circuit, the message relocation circuit transfers a portion of the message into the addressed time slot. After the message is loaded into the assigned talking time slot word, the information is used to establish a time division connection between the calling party and the digit trunk. The digit trunk is always treated as the called party. The calling party receives dial tone over the digit trunk and through the switch unit transmission connection.

2.05 The digit trunk is used to transmit dialed digits to the control unit. When the calling party uses a TOUCH-TONE telephone set, the signals are transmitted through the time division transmission path to the digit trunk without alteration. When the calling party uses a rotary dial telephone set, the dial pulses are sampled by the line supervisory circuit, which passes the information via the scan bus to the digit trunk circuit. The digit trunk circuit converts the dial pulse information to tone bursts which are transmitted to the control unit over the digit trunk. After dialing is complete, the control unit sends a 47-bit message to the switch unit, containing the number of the calling party, the number of the called party, and the address for the time slot originally assigned. The message also contains ringing instruction bits for signaling the called party. The ringing information in the data message causes the switch unit to apply immediate, then interrupted ringing, via the line circuit to the line of the called party. Ringback signals are supplied to the time-shared bus for the calling party. When the called party answers (off-hook), a data message is sent to the control unit; the control unit then sends a message to the switch unit, which is used to terminate the ring-ringback operation.

2.06 Incoming or outgoing calls are set up in a manner similar to line-to-line calls. Tandem trunk calls are similarly treated.

NETWORK CIRCUITS

A. Line Circuits

2.07 Each extension line has access to the talking buses through a line circuit. Four line circuits are provided on each line circuit pack. Fig. 5 is a block diagram of a line circuit showing the transmission, supervisory, and ringing functions for the associated extension. The transmission portion consists of a high-speed solid-state sampling switch, a low-pass filter, and a line transformer. Trunk circuits are quite similar to line circuits in arrangement and function; only the line circuit will be described in this part.

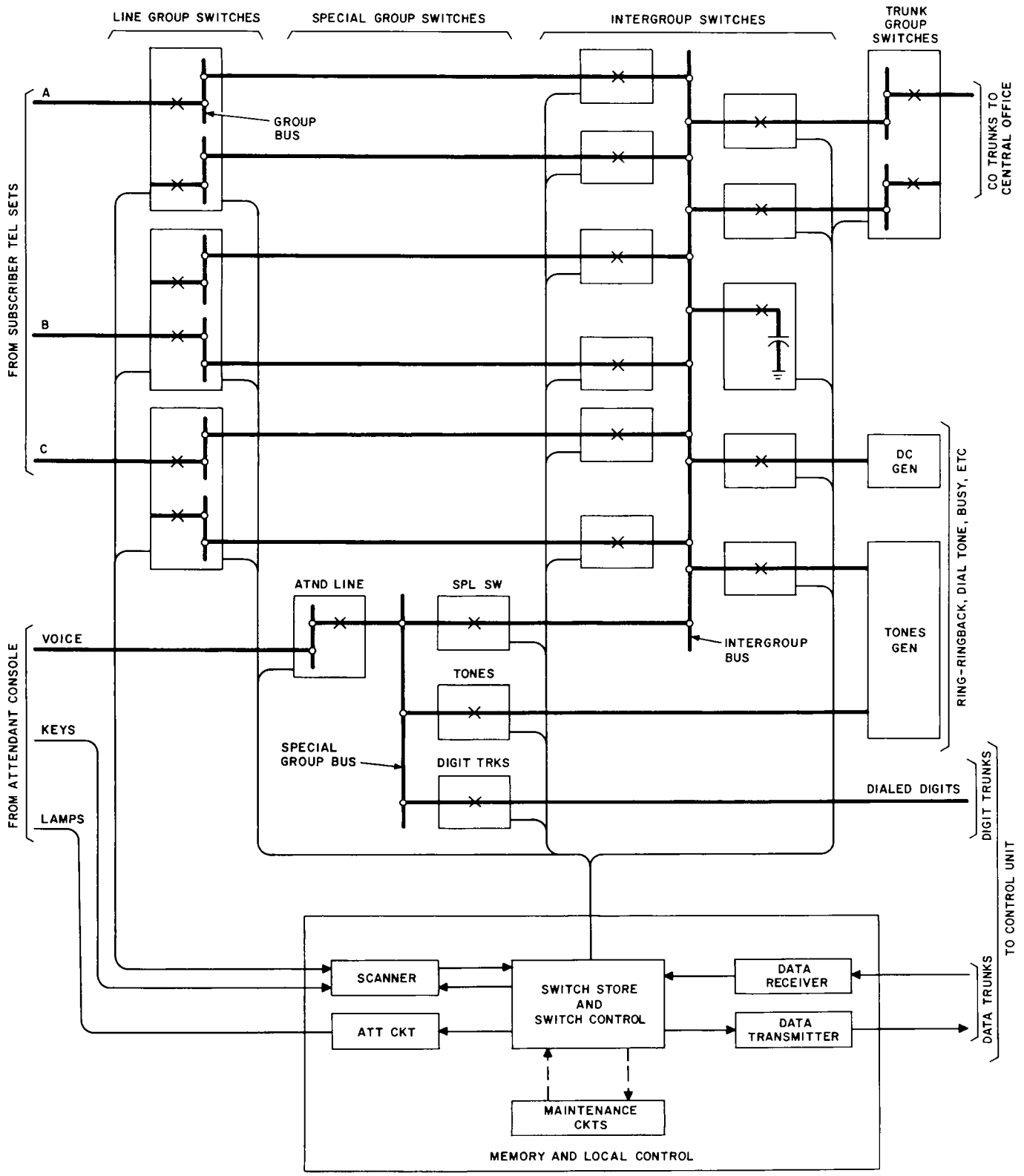


Fig. 4—3A Switch Unit—Simplified Block Diagram

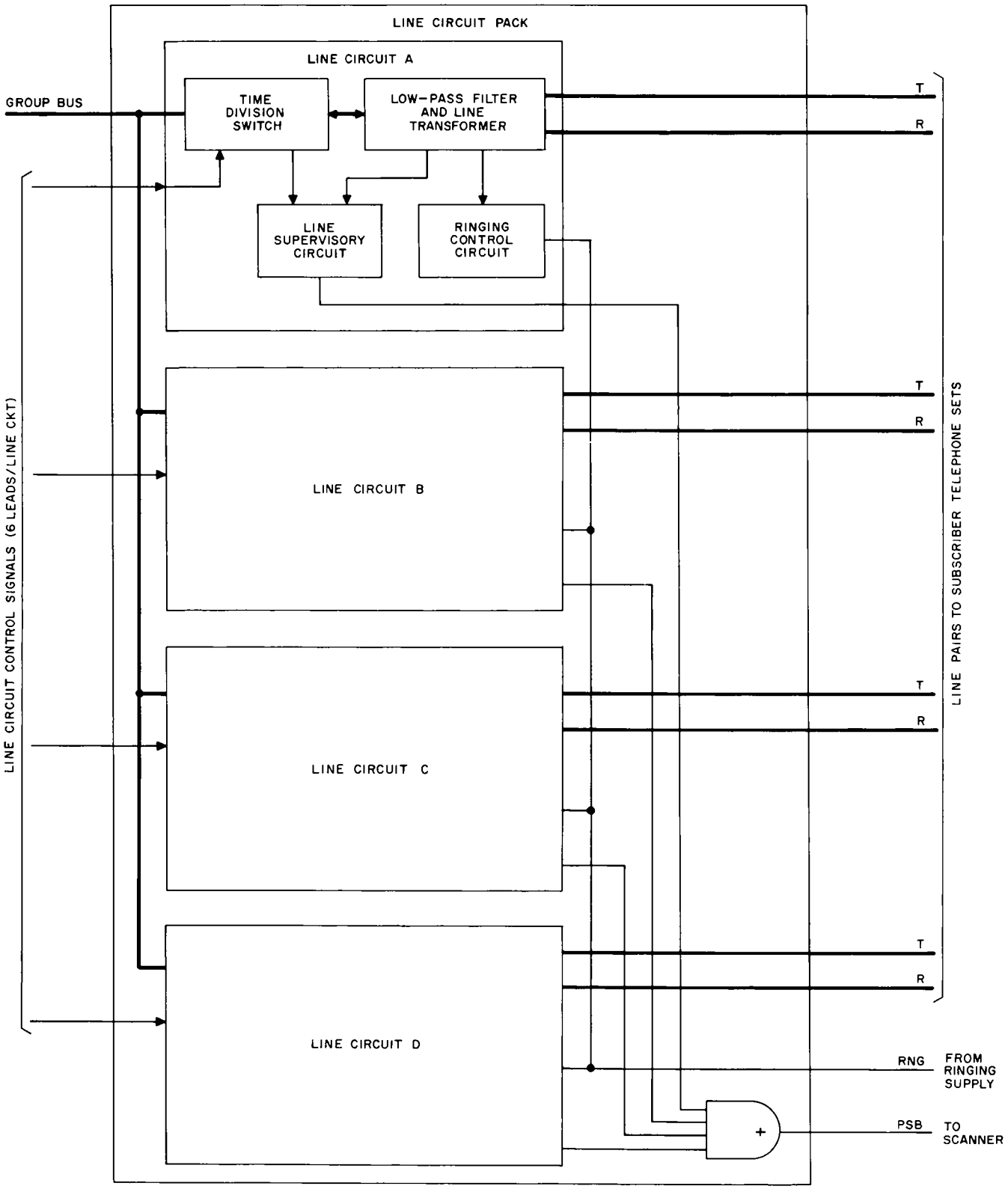


Fig. 5—Line Circuit Pack—Block Diagram

2.08 Fig. 6 shows a typical time division switch circuit. When both inputs (V and H) of AND gate Q1 or Q2 are grounded, a high impedance is present at the applicable gate output lead, which allows the clock drive pulse to be applied (unshunted) to the appropriate Q3 input lead. The positive clock pulse on either input turns Q3 on, causing the driver transistor Q4 to conduct. The Q4 collector current pulse via transformer coupling turns on the time division switch transistors Q5 and Q6.

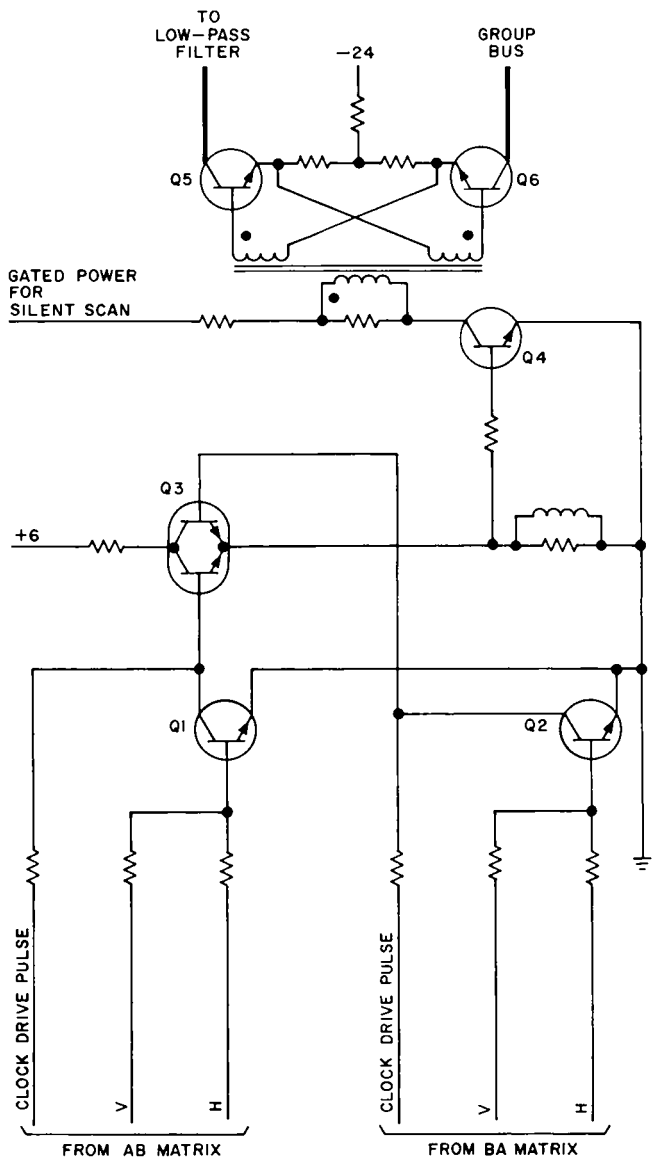


Fig. 6—Typical Time Division Switch Circuit

2.09 The time division switch in the line or trunk circuit connects the line or trunk via the low-pass filter to the time division bus when a time division connection is required. The low-pass filter and line transformer of the line or trunk circuit are shown in Fig. 7.

2.10 The harmonic transfer of energy is accomplished in the line or trunk circuit by employing a resonant transfer inductor (15 μh) and capacitor (3750 $\mu\mu$f) which are physically located in the low-pass filter. The values of the components are selected to completely transfer the energy stored on the capacitor in 800 nsec.

2.11 The low-pass filter (6 dB down at 6 kc) is required to band limit the input signals to the time division switch and to recover the time division signals from the switch. The filter also prevents any high-frequency sampling noise from reaching the line transformer. The line transformer converts the unbalanced audio signals from the filter to balanced signals suitable for transmission over the line or trunk via the tip (T) and ring (R) leads. The transformer also provides an impedance match between the filter and the line. The balanced winding is split to provide dc isolation for supervision of the line or trunk. The two segments are capacitively coupled to provide continuity for audio signals. A pair of zener diodes are provided in the return lead between T1 and the filter to limit voltage swings on the time division switch to $\pm$15 volts (input of +4 dbm).

2.12 In trunk circuits the lead designated A is not used, B is ac coupled to ground by a capacitor, C and D connect to the trunk supervisory portion of the trunk circuit, E connects to -24 volts, and F connects to +24 volts. In line circuits the lead designated A is connected through the make contacts (M6) of the ringing relay K1A to lead B. B is also ac coupled to ground via the break contacts (B6) of relay K1A. Furthermore, B connects to the base of a ringing control transistor which operates the K1A relay. C connects to the K1A cutoff transistor and the line supervisory circuit. D is not used in line circuits. E is connected to ground via the break contact (B1) of K1A and to the ringing voltage via the make contact (M1) of K1A. F connects to the +24 volt talk battery supply. The ringing and supervisory functions are described in their associated subparts of this section.

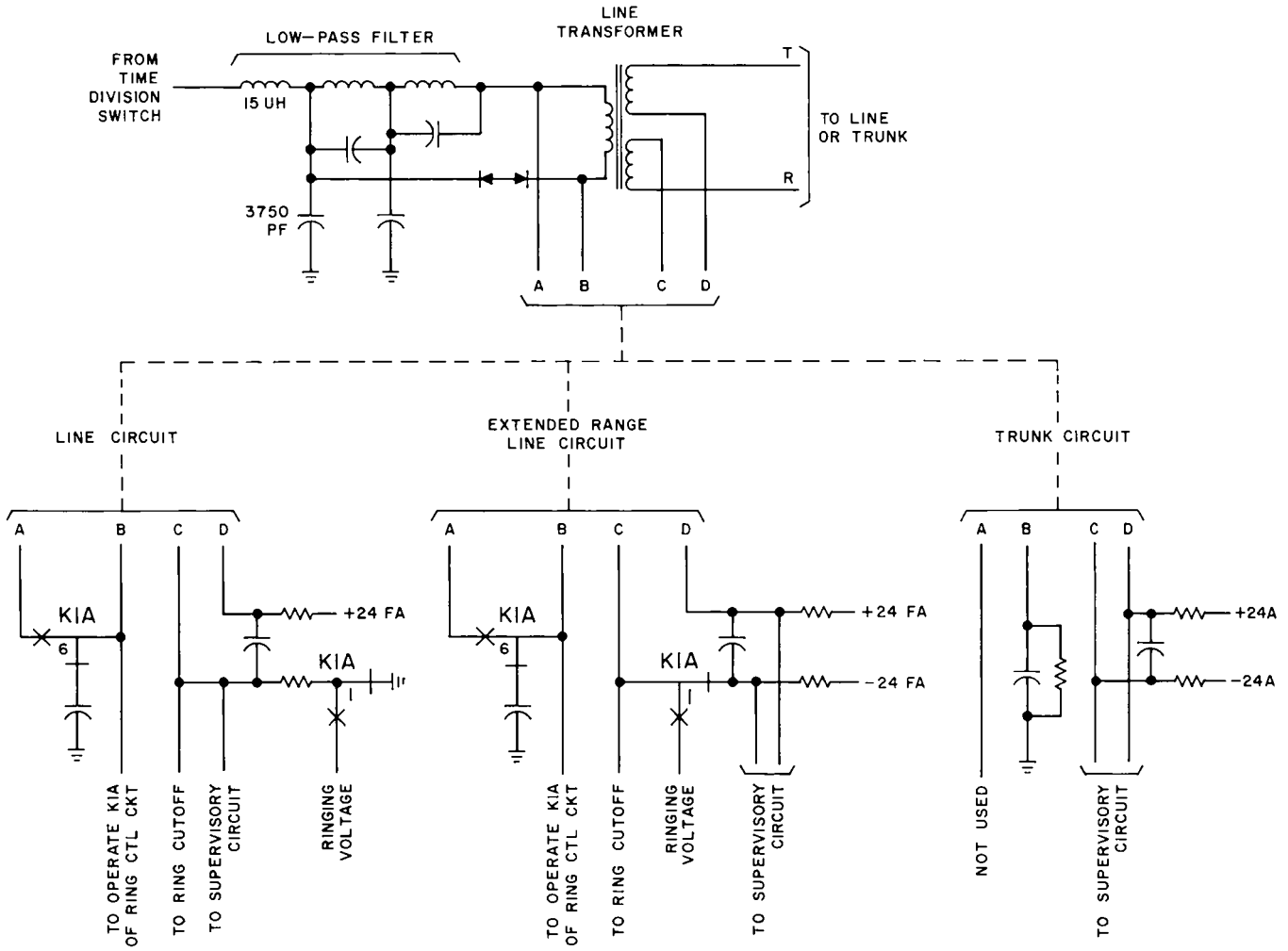


Fig. 7—Low-Pass Filter and Line Transformer

B. Group Circuits

2.13 Line and trunk circuits are arranged in groups of 64 equipment units. Fig. 8 shows the transmission path for a typical group circuit which may provide as many as 64 line or trunk circuits in subgroups (circuit cards) of four. Fifteen groups may be provided. The line and/or trunk circuits of each group, in accordance with a numbering plan, are assigned alternately by fours to the two group buses (group bus 0 and group bus 1). Table A outlines the translation format for the numbering plan in each group. The line and trunk circuits, for the purpose of selection, are arranged in a 3-dimensional matrix of four elements each (4 by 4 by 4). The 64 possible numbers per group are translated from the equivalent binary numbers 000000 through 111111. The 6-bit binary number provides 3-bit pairs which represent the four subgroup or clocking numbers (0 through 3), the four vertical numbers (0 through 3), and the four horizontal numbers (0 through 3). The six binary bits of the line or trunk number in a group are designated from 6 through 1 to represent the most significant bit through the least significant bit, respectively. The two least significant bits (2 and 1) produce the four horizontal select signals in the translation process. Bits 5 and 4 produce the four vertical select signals and bits 6 and 3 are combined to produce the four clocking group select signals. It should be noted that alternate subgroups of four lines are shown to the left and to the right of the table separated by a dotted vertical line. The first, third, etc, subgroups of four lines

are in the left blocks (clocking groups 0 and 2) and are assigned to group bus 0; the other subgroups of four lines are in the right blocks (clocking groups 1 and 3) and are assigned to group bus 1. Since the system logic uses binary coded numbers, it is only required that the IGS examine the third least significant bit of the numbers associated with the calling and called parties to determine the bus. These bits are taken from bit 27 of the calling line and bit 19 of the called line.

C. Intergroup Switch Circuits

2.14 The intergroup switch (IGS) circuit provides a time division switched intergroup transmission path between group buses. Two intergroup switch circuits (IGS 0 and IGS 1) are provided in the 3A basic switch unit (120 time slots) for system reliability. One intergroup switch circuit is employed in each time division control. Each is independent of the other and can accommodate 60 time-shared talking connections. A failure of either intergroup switch circuit in the basic switch unit will only reduce the maximum total traffic capacity to one-half the normal 120 transmission connections. Where the auxiliary time division controls (maximum of 120 additional time slots) are provided for additional time slot capacity, failure of an intergroup switch circuit will reduce the total traffic capacity by 60.

2.15 Other functions of the IGS, which will be described in subparts associated with their functions, are:

(a) To supply a positive dc ring control voltage to the intergroup bus (IB) which is transmitted to the line circuits via the time division connecting cables.

(b) To supply an audible ringback signal from an amplifier in the IGS which is switched via the IB to the calling parties as required.

(c) To supply six conference capacitor circuits per IGS. Each capacitor provides for a nongain bridging-type conference limited to three parties. The conference circuit is used for the call transfer feature which requires that a 3-party connection be established.

D. Special Group Circuits

2.16 The transmission connections previously discussed were between subscriber line and/or trunk circuits. Other types of connections are provided to ***common equipment*** via time division switches in the associated intergroup switch circuits and the special group circuits. The common equipment discussed in the following paragraphs consists of conference capacitors and the ringing circuits in the intergroup switch circuit. The tone, the attendant line, and the digit trunk connection and selection circuits are connected to the intergroup bus via the special bus and special switches.

TRANSMISSION PATH

2.17 Fig. 9 is the switching network overall transmission path which shows the 15 groups (0 through 3 and 5 through 15) of line and trunk circuits each with 2 group buses (0 and 1). Thirty group switches are provided in the intergroup switch circuit of each time division control to produce intergroup connections via the associated intergroup bus. Other circuits connected to the intergroup bus (IB) are the IB clamp, negative impedance converter (NIC), conference capacitors, attendant lines, and special group circuits via the special bus. The IB clamp circuit places a terminating resistor on the bus during the guard interval after each talking connection. The NIC is a shunt-type negative resistance amplifier permanently connected to the IB primarily to improve the return loss of trunk circuits by improving the impedance characteristics for these calls. A slight reduction in insertion loss is produced for all connections. Six conference capacitors and associated time division switches are provided with each intergroup bus. Each capacitor can be used to form a bridging-type add-on conference for up to three parties and to effectively bridge the parties by providing short term analog memory between the associated talking time slots.

2.18 A special bus associated with each intergroup bus provides for connection between the common equipment switch circuits and to intergroup bus connections. Any common equipment can be connected via the associated special bus. A special switch (ADT) provides connection between the special bus and the intergroup bus. Thus, in each TDC unit, the associated ADT switch connects the special bus and intergroup bus, eg, ADT/0 to IB0 and ADT/1 to IB1, etc. Each special bus is provided with a bus clamp circuit in the associated special group. The clamp switch is shown in the closed position to indicate that the bus is brought to ground level after each resonant transfer operation

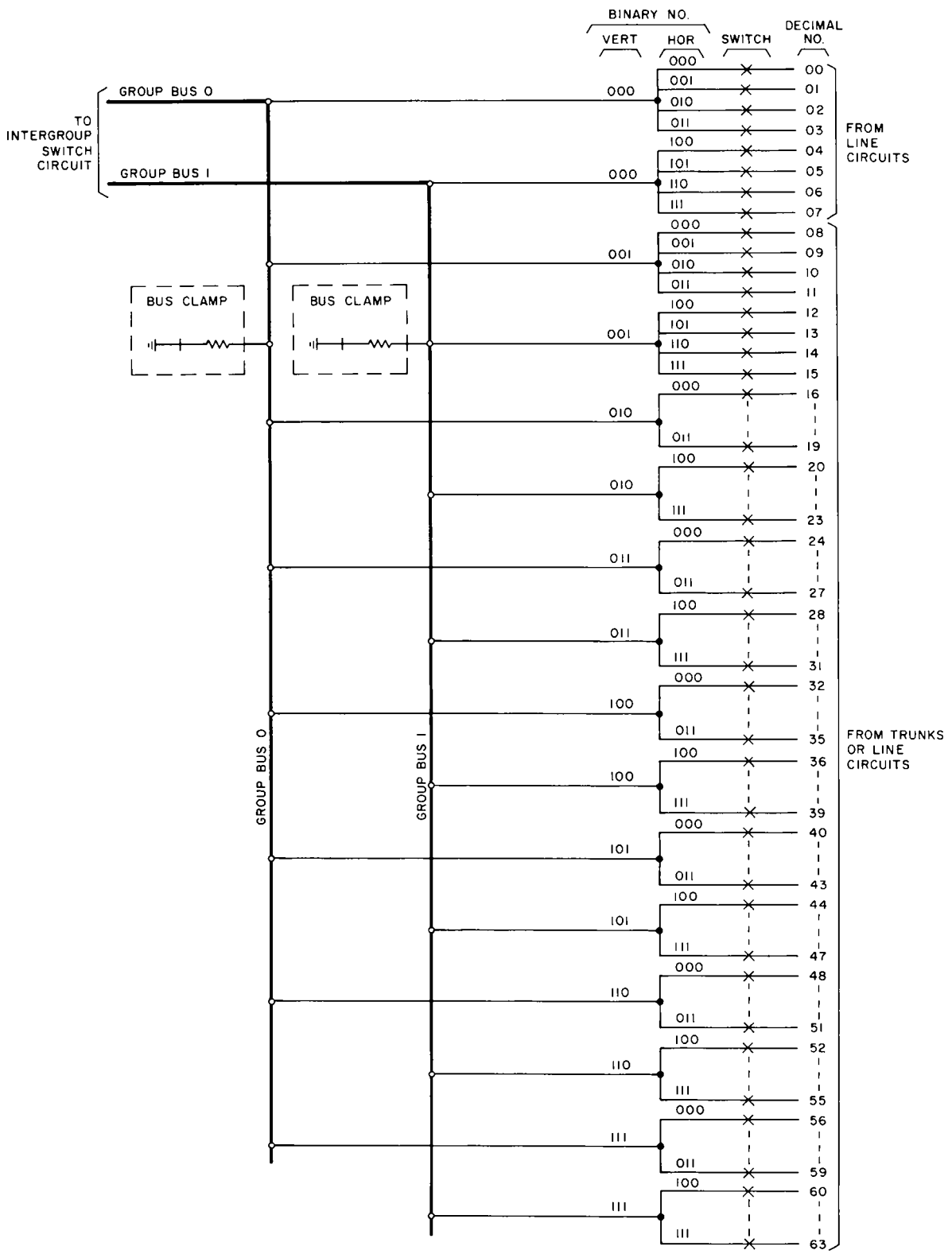
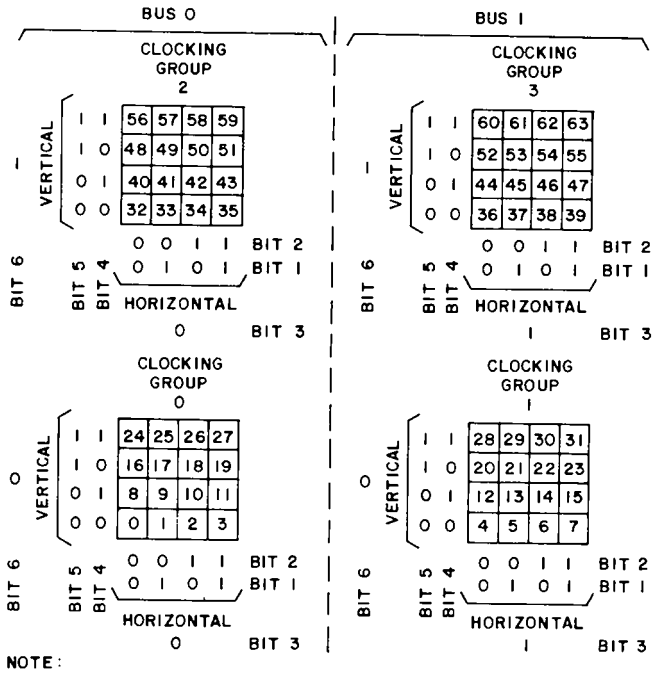


Fig. 8—Transmission Path of a Typical Group Circuit

Table A



NOTE:
IN THE 6-BIT BINARY NUMBER:
BITS 6 AND 3 DEFINE THE CLOCKING GROUP NUMBER (0-3).
BITS 5 AND 4 DEFINE THE VERTICAL NUMBER (0-3).
BITS 2 AND 1 DEFINE THE HORIZONTAL NUMBER (0-3).
THE STATE OF BIT 3 DETERMINES THE GROUP BUS ASSIGNMENT (0 OR 1).
BIT 3 IS DETERMINED FROM THE OUTPUT REGISTER BIT 27 OF THE CALLING LINE AND BIT 19 OF THE CALLED LINE.

to remove any energy left there during the transfer interval.

2.19 Tone circuits are provided on a per TDC basis to produce soft tone (ST), busy tone (BT), and fast busy tone (FB) for either special bus. The tones are combined in the tone generator to produce the audible ringback (ARB) signal for application to the associated intergroup bus. The ringback signal is produced in two levels via the ringback amplifier and two switches, ringback high (RBH) level and ringback low (RBL) level. A dc generator is connected to the associated intergroup bus by the dc ringing (RNG) switch to produce a signal suitable for operating the ringing relay control circuit in the subscriber line circuits.

2.20 The digit trunk circuit provides a bilateral voice frequency link between the control unit and a line or trunk circuit via the special bus associated with the digit trunk. The first six digit trunks (1 through 6) are assigned to special bus 0 and the second six digit trunks (7 through 12) are assigned to special bus 1. Accordingly, digit trunks 13 through 18 are assigned to special bus 2 of TDC2 and digit trunks 19 through 24 are assigned to special bus 3 of TDC3.

2.21 Attendant line circuits are duplicated in each TDC. The tip and ring of the attendant line circuit from each attendant console are multipled to the special bus of each TDC. Twelve attendant line circuits can be provided.

TIME DIVISION SWITCHING

2.22 Time division switching is employed in the No. 101 ESS. In general, time division switching requires less equipment in the local switching network than do other types of switching equipment. The 3A switch unit provides a voice frequency transmission path connection from periodic short duration ***samples***. Periodic short samples of a speech signal are sufficient to define the signal completely, provided these samples are taken frequently enough. The terminals of each line and trunk circuit are connected through high-speed solid-state switches to a common terminal or bus. A connection between two line or trunk circuits is established by closing the corresponding switches periodically for an extremely short interval, connecting both circuits to the common bus. The time interval allotted for the closing of each pair of switches is called a ***time slot***. The repetition rate of time slots is called the sampling frequency, which must be at least twice the highest frequency transmitted. Thus, a number of samples, each from a different signal, may be transmitted one at a time over a common path without interference, provided that each sample is confined to its own time slot within the sampling period.

2.23 The sampling technique can be used to transmit the frequency and relative amplitude characteristics of speech, but if unaided, a large loss in volume will result. In regular multiplex transmission systems, amplification is employed to compensate for the transmission channel loss. In the No. 101 ESS, which uses time division multiplexing, losses are adequately reduced through use of what is known as ***resonant transfer***.

2.24 The resonant transfer of voice energy for a single time division channel (time slot) is shown in Fig. 10. If switches A and B are closed simultaneously, any voltage on low-pass filter (LPF) capacitor C_A will be transferred by way of

the time division bus to capacitor C_B. Since the time constants of the two capacitors and the inductors between them give the bus path a low-loss resonant characteristic, all of the voltage initially on C_A will be on C_B after a time interval equal to half the natural period of the resonant circuit. If the two sampling switches are opened at this point, the transfer of energy will have been accomplished almost without loss.

2.25 In the 3A switch unit the sampling switches are closed for 800 nsec (0.8 μsec) during each recurrent period of approximately 85 μsec. After each sample is transmitted, switch C clamps the time division bus clamped to ground through the terminating resistor R to dissipate any remnant energy on the bus before the voice energies of the next talking time slot in the sequence are sampled. There are 60 time slots provided in the sequence for each bus. The basic switch unit provides up to 120 simultaneous conversation channels using two buses. Time division control (TDC) number 2 or the combination of TDC2 and TDC3 increases the traffic capacity to 180 or 240 simultaneous conversation channels, respectively. The channels are sampled at approximately a 12 – kHz rate. The time division connection appears to the user as a continuous transmission path due to the smoothing action of the filters forming a part of each line circuit.

BASIC TIME DIVISION CONNECTIONS

2.26 Fig. 11 illustrates a few typical examples of time division connections in the 3A switch unit. Two intergroup buses (IGB0 and IGB1) are shown; each may be independently connected to any group bus via the group switches in the respective intergroup circuits (IGS0 and IGS1). The group bus may be connected to half the line in a group via the line switch of the line circuit. For example, a call between station A and station B is shown assigned to time slot 2 via IGB0. The four switches close simultaneously for 800 nsec during the time slot number 2. Similarly, the call between station C and station D is connected via IGB1 for 800 nsec during time slot number 2. Shown symbolically is the bus clamp circuit associated with each intergroup bus. The bus clamp switch closes after the transmission path switches open. The bus clamp switch opens again before a transmission path switch closure in the next time slot.

2.27 Fig. 12 shows the speech waveform and the time division sampling current relationship for calls AB and EF which are connected to IGB0 during time slots 2 and 3, respectively. Call AB illustrates an intergroup connection via IGB0 in time slot 2, and call CD illustrates a call via IGB1 in time slot 2. The intergroup connection employs four switches, namely, two line switches and the two group switches associated with each of the two line circuit group buses. Call EF illustrates an intragroup connection via IGB0 during time slot 3 and call GH illustrates an intragroup connection via IGB1 during time slot 3. Since both stations in these calls are in the same line group circuit, one group switch operates to provide the connection of both lines to the intergroup bus.

2.28 Conference calls are shown assigned to the time slot pair, TS4 and TS5, for each bus. The voice energy of the IJ intergroup transmission path is connected to the associated conference capacitor via IGB0 during TS4; the same capacitor is connected via IGB0 to the K intergroup transmission path during TS5. Thus, the conference capacitor (IJK) via IGB0 samples the voice energy level of time slot (4) and transfers the energy level to time slot (5) to produce a transmission path between the two time slots which could connect as many as three parties (I, J, and K). Similarly, conference call MNOP is shown assigned via IGB1 to TS4 and TS5 and conference capacitor (MNOP). M and N represent an intragroup connection while O and P represent intergroup connection.

2.29 The separate, but seemingly simultaneous, transmission paths previously described are typical examples and illustrate connections between line circuits. The treatment of trunk circuit connections is the same as for line circuits. Therefore, trunks can be substituted for stations in Fig. 11. Shown symbolically is the bus clamp circuit associated with each intergroup bus. The bus clamp switch closes after the transmission path switches open. The bus clamp switch opens again before transmission path switch closure in the next time slot.

3. MEMORY AND LOCAL CONTROL

3.01 The memory and local control portion of the 3A switch unit consists of the switch store and switch control circuits which provide the control signals required to:

- Establish transmission connections

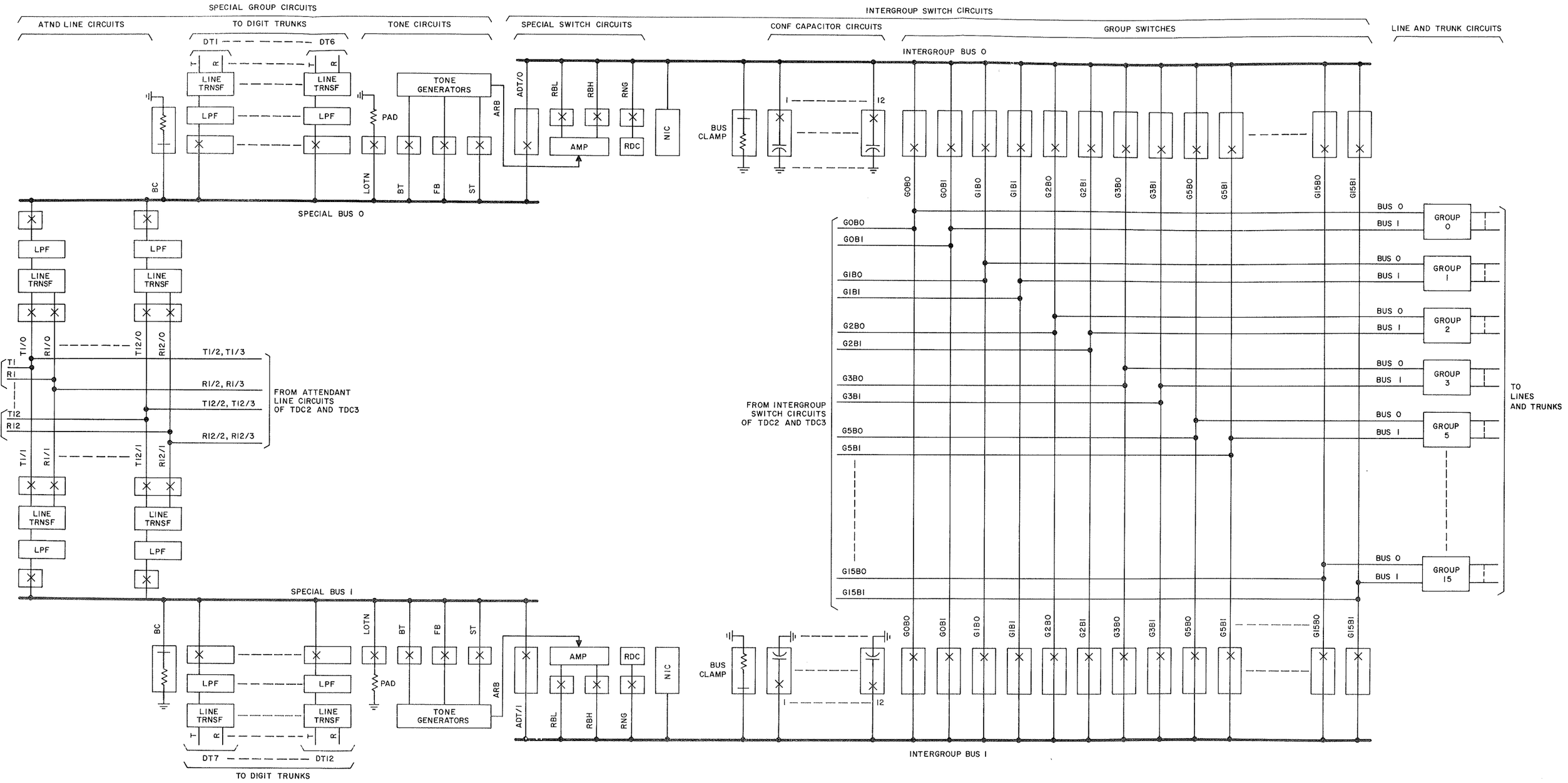
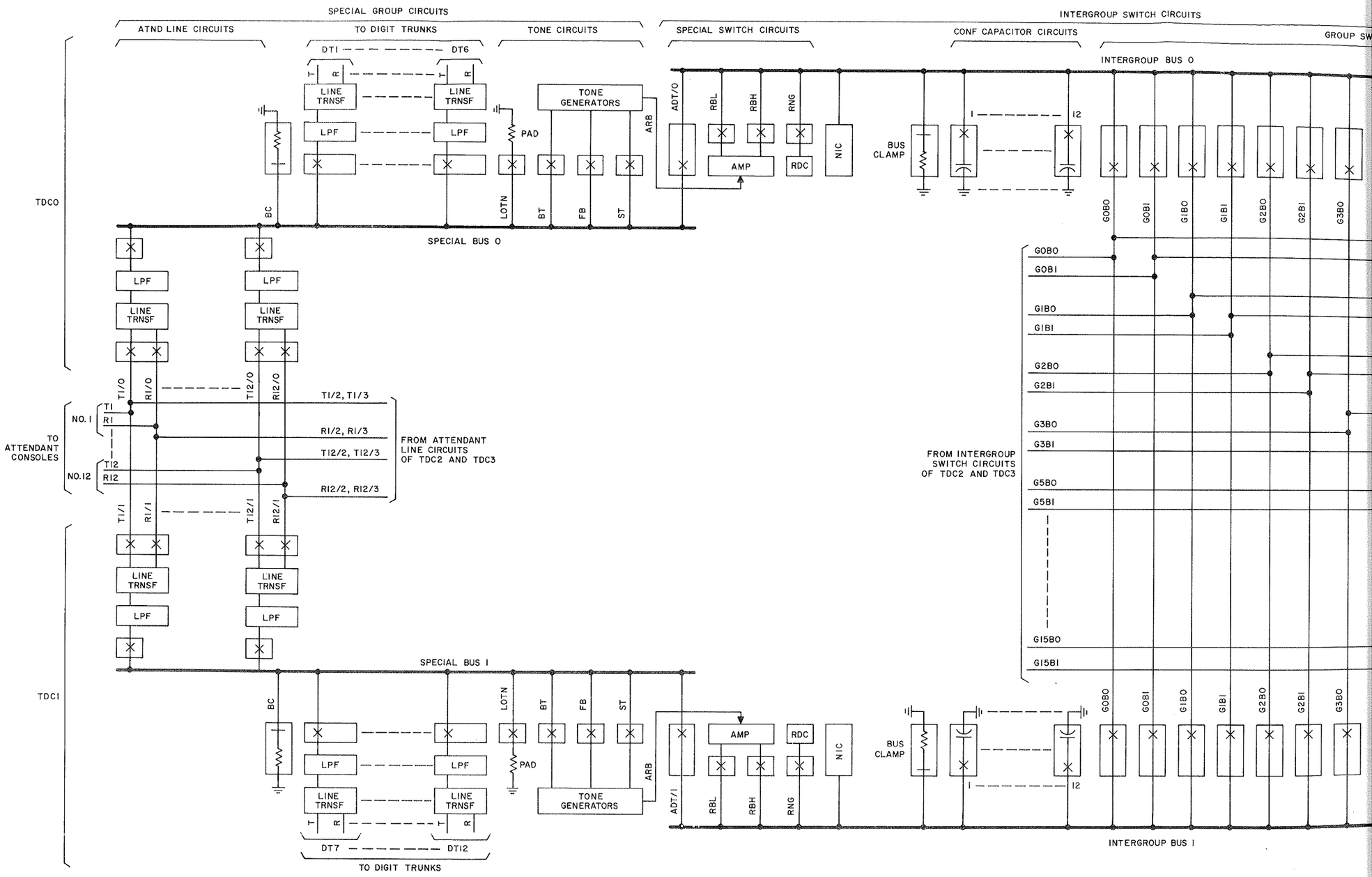


Fig. 9—Switching Network Overall Transmission Path


SPECIAL GROUP CIRCUITS
ATND LINE CIRCUITS
TO DIGIT TRUNKS
TONE CIRCUITS
SPECIAL SWITCH CIRCUITS
INTERGROUP SWITCH CIRCUITS
CONF CAPACITOR CIRCUITS
GROUP SW
INTERGROUP BUS 0
TDCO
DTI
DT6
T
R
LINE TRNSF
LPF
PAD
TONE GENERATORS
ARB
ADT/O
RBL
RBH
RNG
AMP
RDC
NIC
BUS CLAMP
I
I2
8C
LOTN
BT
FB
ST
SPECIAL BUS 0
GOBO
GOBI
GIBO
GIBI
G2BO
G2BI
G3BO
T1/O
R1/O
T12/O
R12/O
T1/2, T1/3
R1/2, R1/3
T12/2, T12/3
R12/2, R12/3
NO. 1
NO.12
T1
R1
T12
R12
TO ATTENDANT CONSOLES
FROM ATTENDANT LINE CIRCUITS OF TDC2 AND TDC3
FROM INTERGROUP SWITCH CIRCUITS OF TDC2 AND TDC3
G5BO
G5BI
G15BO
G15BI
T1/1
R1/1
T12/1
R12/1
TDCI
BC
ADT/I
DT7
DTI2
TO DIGIT TRUNKS
INTERGROUP BUS I

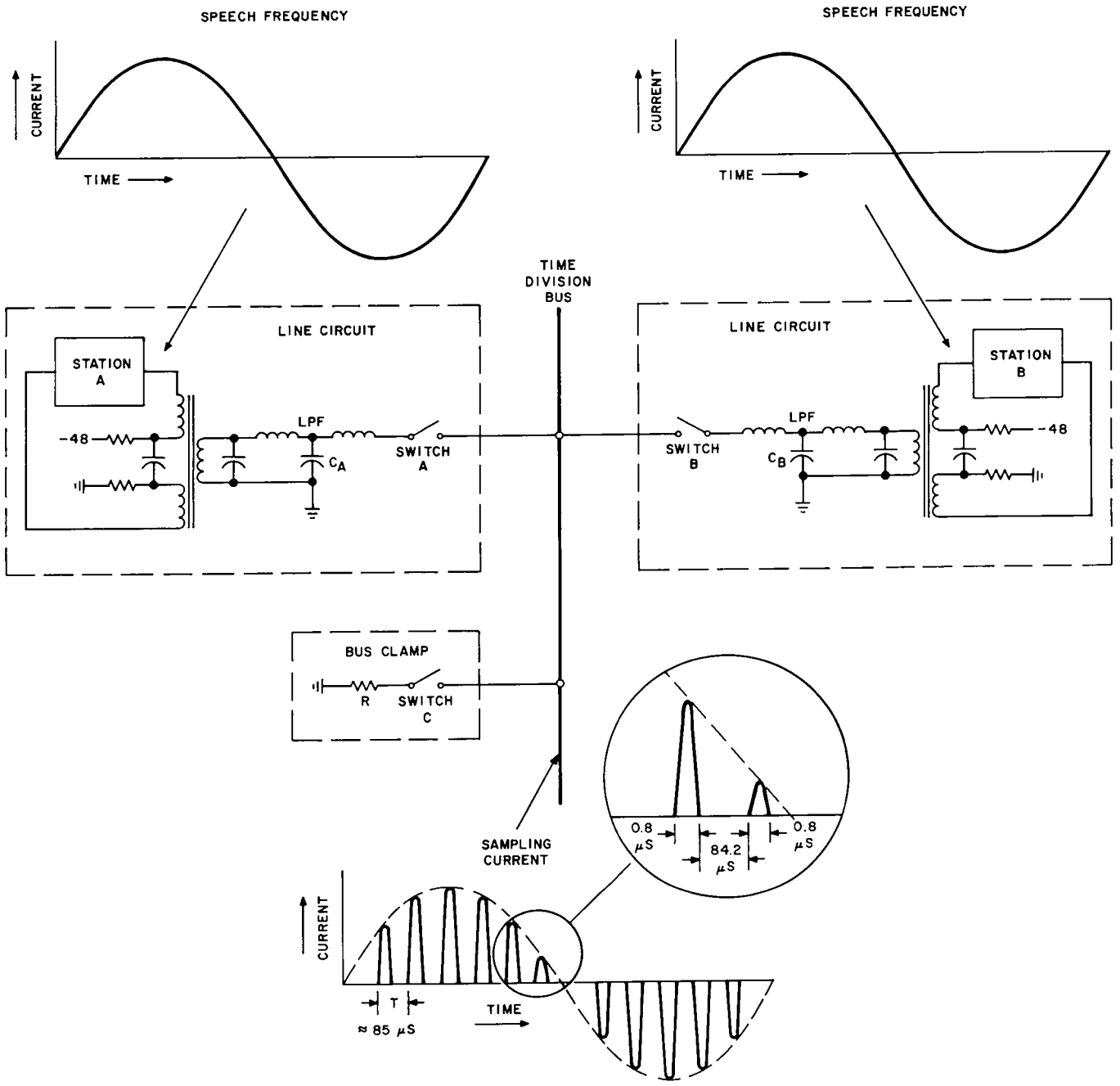


Fig. 10—Fundamental Time Division Transmission Circuit

- Scan all lines and trunks to detect changes of supervisory state
- Process outgoing and incoming messages
- Operate attendant lamps.

The control operations are performed during related time slot intervals.

TIME SLOTS

3.02 Each time division control (TDC) has a total of 60 time slots for establishing time division connections. The 128-word switch store memory of each TDC has two 30-word groups allocated for transmission connections. The 60 words are referred to as ***talking time slots*** and are numbered A2 through A31 and B2 through B31. There are also

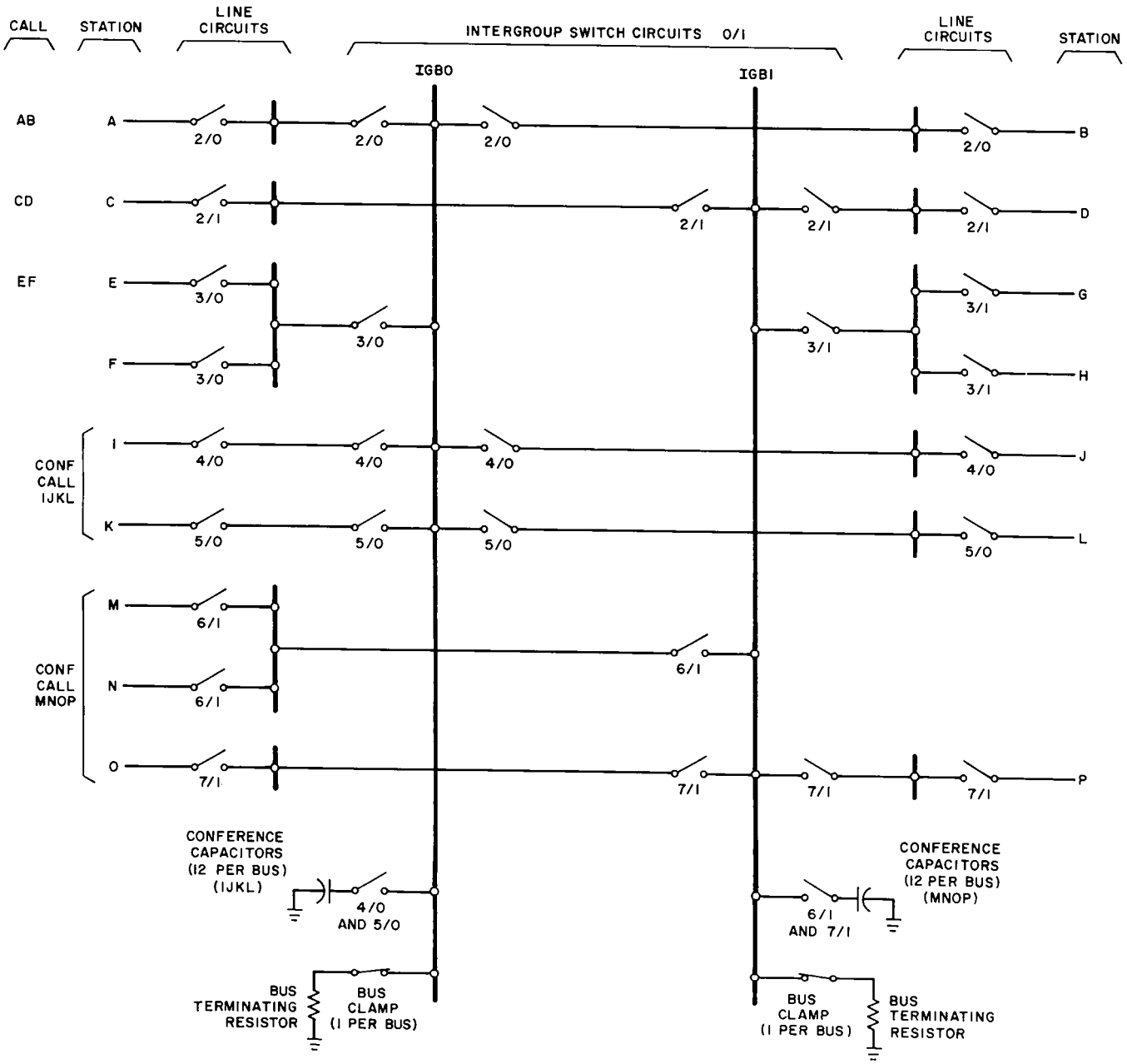


Fig. 11—Typical Examples of Simultaneous Conversations in the 3A Switch Unit

five time periods known as ***data time slots*** and numbered A0, A1, B0, B1, and B32. The data time slots are used for handling incoming and outgoing messages, lighting attendant lamps, and interrogating scan points. Thus, 65 time slots are provided for each TDC. Each time slot lasts 1.305 μsec. The 65 time slots are allocated in two blocks, A and B. Both blocks go through the cycles simultaneously while advancing alternately.

3.03 The store cycle sequence is shown in Fig. 13.

The switch control circuit associated with block A proceeds from time slot A0 through A31 and back to A0. The switch control circuit associated with block B proceeds from time slot B0 through time slot B32 and returns to B0. Thus, while block A employs 32 time slots of 1.305 μsec each, block B employs 33 time slots of 1.305 μsec each. Since the store cycle times, which are 83.52 μsec

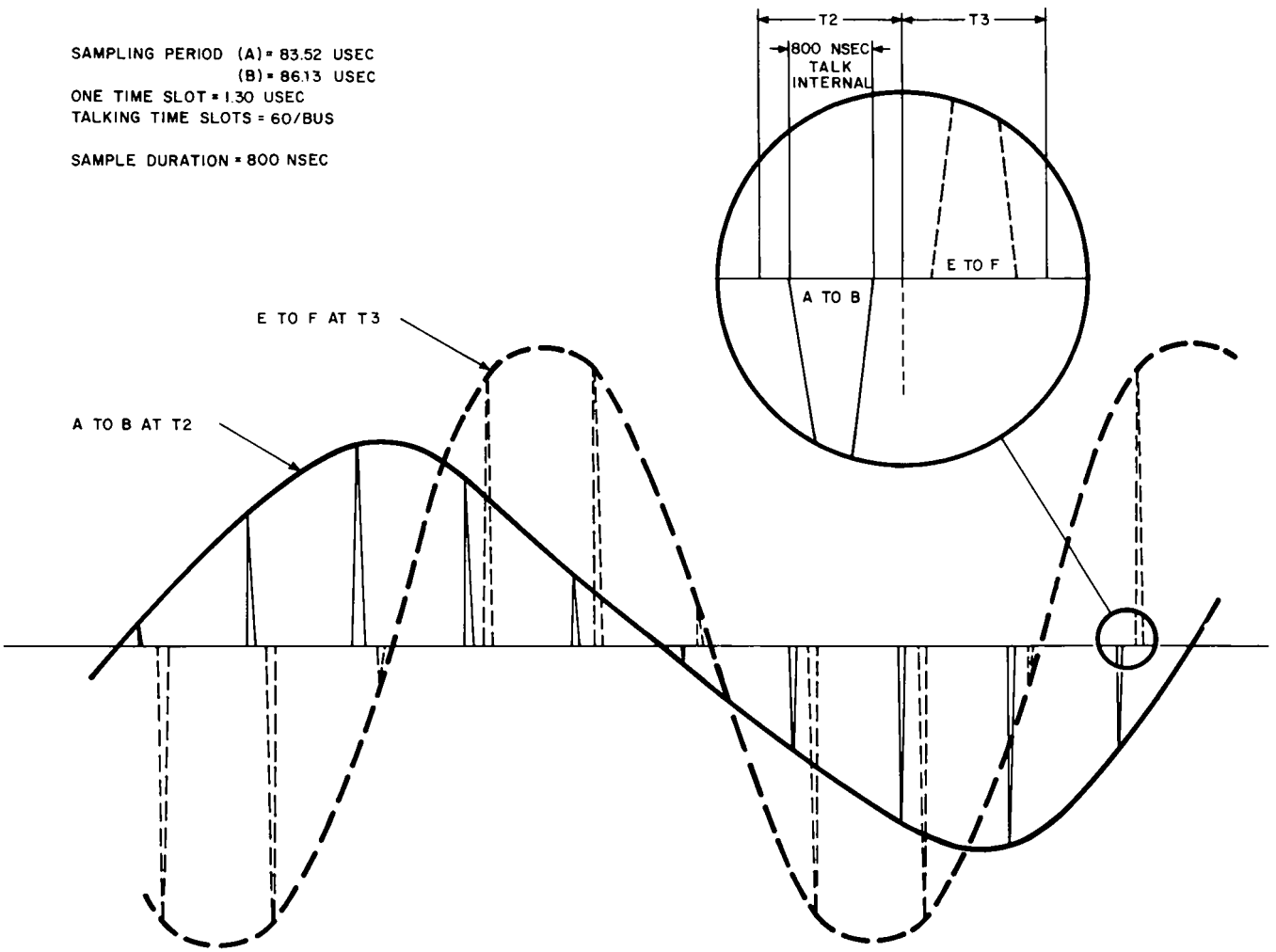
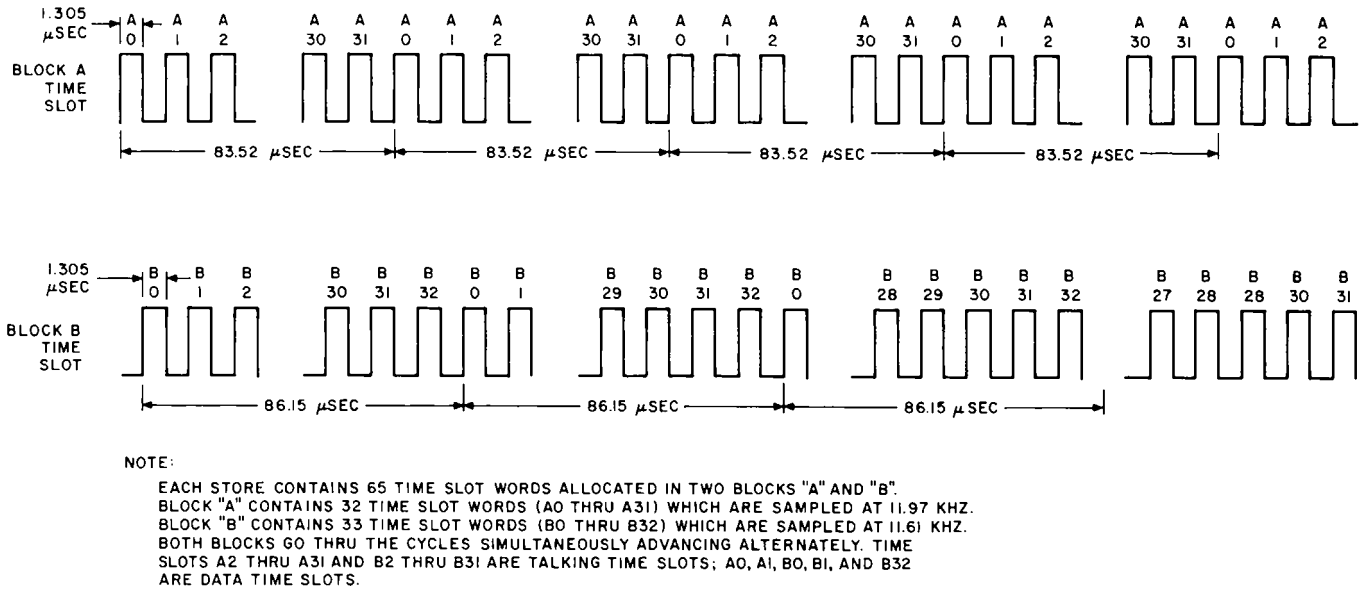


Fig. 12—Time Division in the 3A Switch Unit

and 86.13 μsec, respectively, differ by one time slot interval, the time slots of the two blocks move with respect to each other. For example, the first store cycle shown in Fig. 13 shows the same time slot numbers advancing alternately in both blocks for each 1.305 μsec time slot interval up through time slot B31 (A0, B0, A1, B1....A31, B31). Due to the omission of time slot A32 in block A, time slot A0 first follows B31 (then A0, B32, A1, B0, A2, B1....A31, B30). Since the A time slots and B time slots are interspersed and unequal in number, a rotation occurs between the time slots in the two blocks. After the fourth cycle of block A, time slot A0 follows B28 (then A0, B29, A1, B30, A2, B31, A3, B24, A4, B0, etc). Since 33 times 32 time slots are required to bring the time slots into line again, a rotation rate of approximately 360 Hz is produced between the time slot words of the two blocks. The precession provides a reduction in certain forms of crosstalk in the system.

TALK CONNECTION SWITCHING AND CONTROL

3.04 Fig. 14 is a simplified block diagram showing the time-shared switching section which provides talk connections between lines. Connections are also provided between lines and trunks for incoming or outgoing calls and between trunks for tandem trunk calls. The transmission path is shown by the heavy lines. The talk connection control function is shown by the thin lines. The associated functions, consisting of the digital data message information and the line supervisory scanning function, are shown by the dotted lines. The full 3A switch unit complement of four time



NOTE:
EACH STORE CONTAINS 65 TIME SLOT WORDS ALLOCATED IN TWO BLOCKS "A" AND "B".
BLOCK "A" CONTAINS 32 TIME SLOT WORDS (A0 THRU A31) WHICH ARE SAMPLED AT 11.97 KHZ.
BLOCK "B" CONTAINS 33 TIME SLOT WORDS (B0 THRU B32) WHICH ARE SAMPLED AT 11.61 KHZ.
BOTH BLOCKS GO THRU THE CYCLES SIMULTANEOUSLY ADVANCING ALTERNATELY. TIME SLOTS A2 THRU A31 AND B2 THRU B31 ARE TALKING TIME SLOTS; A0, A1, B0, B1, AND B32 ARE DATA TIME SLOTS.

Fig. 13—Store Cycle Time Slot Precession—Sequence Chart

division control (TDC) units and 15 line and trunk group circuits are shown. The basic switch unit consists of TDC0, TDC1, and the first nine line and trunk group circuits. The auxiliary units consist of TDC2, TDC3, and line and trunk group circuits numbered 10 through 15.

3.05 TDC0, TDC1, TDC2, and TDC3 are each equipped with time slot counter and store address translator circuits which control the access of the associated store memory words. The content of talking time slot memory words in a given switch store circuit provides information to the output register in the switch control circuit. The output register state is translated by the group pretranslator (GPX) during talking time slots into signals representing a 3-dimensional array which selects the required group, vertical, and horizontal time division crossing points for the calling (A) and called (B) parties. A line or trunk circuit within a group is selected by the two dimensions (vertical and horizontal) while the associated group bus is selected by the third dimension (group) in the TDC associated intergroup switch (IGS) circuit. Each intergroup switch circuit has 60 talking time slot intervals. All four IGS units are operated simultaneously, producing up to 240 talking time slot channels. Thus, four conversation channels may be established during the same time period. Each line and trunk group has access to all 240 talking time slot channels. To prevent double connections, each group bus is allowed connection to only one of the intergroup buses (IB0 through IB3) during any given time slot interval. In selecting a time slot for a call, the control unit program assures not only that the desired time slot is idle, but also that the corresponding time slot on all of the other intergroup buses is not being used by lines or trunks terminated in the same group bus as the line or trunk requesting service.

3.06 The GPX and scanner circuits of TDC0 and TDC1 each contain a scanner, and the switch control circuits each provide an associated outgoing message control circuit. The scanner and outgoing message control circuits are not provided with TDC2 and TDC3. Incoming message control circuits are provided in all TDC units. The incoming messages from the control unit supply information for controlling attendant lamp illumination and talking time slot connections.

3.07 The duplicate scanner circuits of TDC0 and TDC1 scan all 1216 scan points. One is assigned to on-line status while the other is off-line. The operation is essentially identical, except that only the on-line scanner can send an outgoing message to the control unit indicating a change in the supervisory state of a scan point.

3.08 The supervisory state changes in the line or trunk circuits are delivered to the on-line

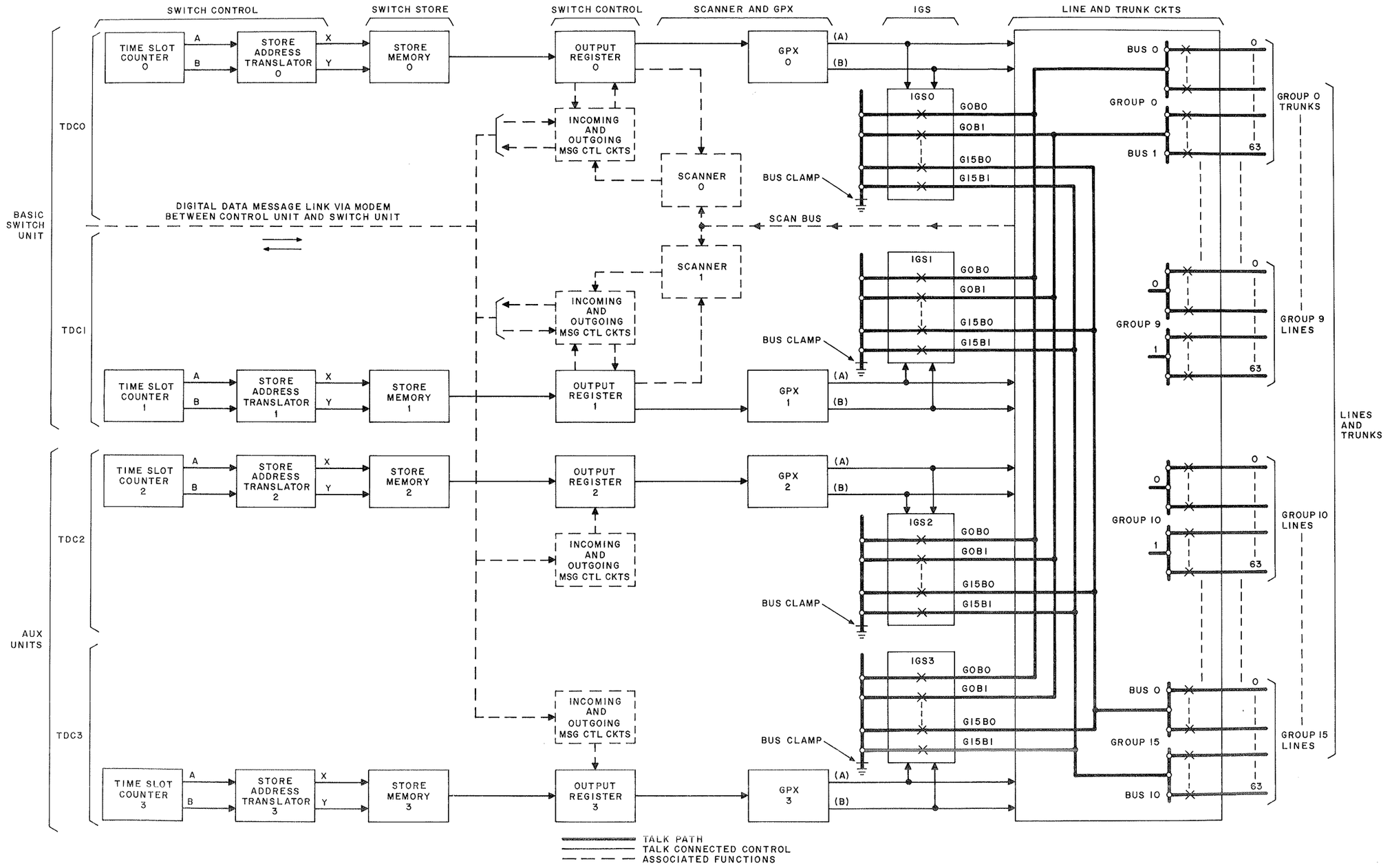


Fig. 14—Talk Connections Switching and Control (Simplified)—Block Diagram

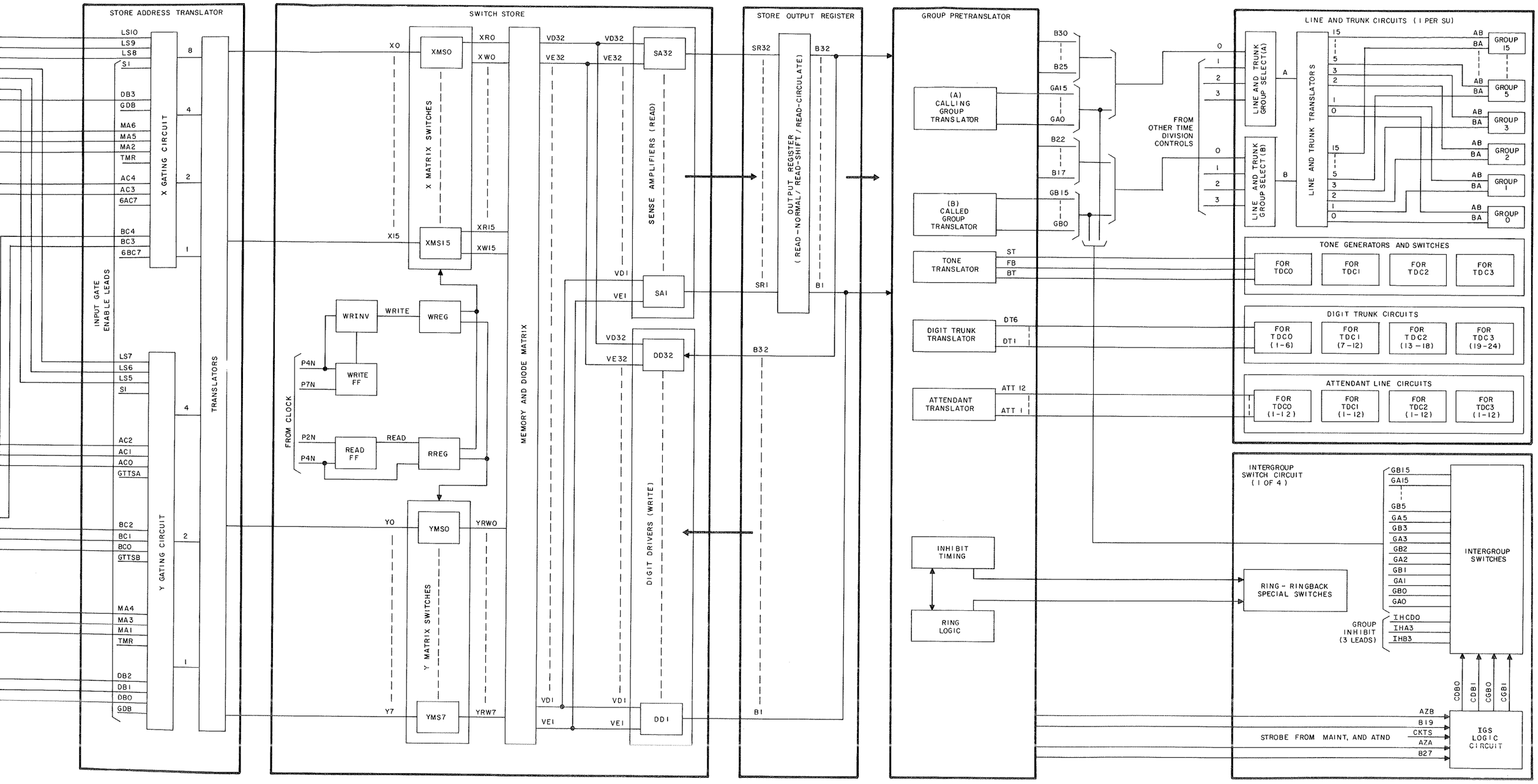
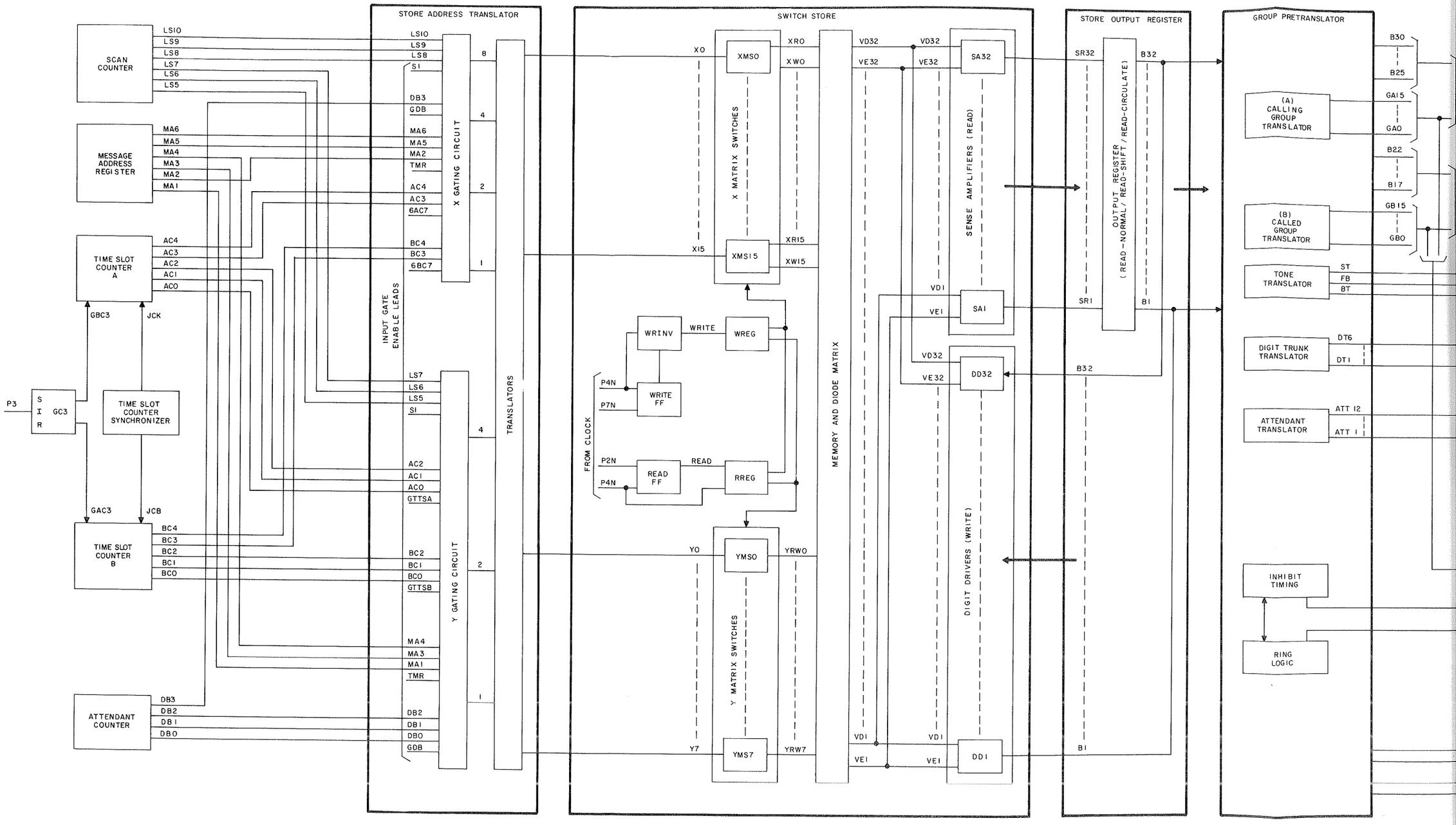


Fig. 15—Memory and Local Control for Talk Connections


STORE ADDRESS TRANSLATOR
SWITCH STORE
STORE OUTPUT REGISTER
GROUP PRETRANSLATOR
SCAN COUNTER
LS10
LS9
LS8
LS7
LS6
LS5
MESSAGE ADDRESS REGISTER
MA6
MA5
MA4
MA3
MA2
MA1
TIME SLOT COUNTER A
AC4
AC3
AC2
AC1
AC0
GBC3
JCK
P3
SIR GC3
TIME SLOT COUNTER SYNCHRONIZER
GAC3
JCB
TIME SLOT COUNTER B
BC4
BC3
BC2
BC1
BC0
ATTENDANT COUNTER
DB3
DB2
DB1
DB0
SI
DB3
GDB
6AC7
6BC7
GTTSA
GTTS8
GDB
INPUT GATE ENABLE LEADS
X GATING CIRCUIT
Y GATING CIRCUIT
TRANSLATORS
8
4
2
1
XO
X15
XMSO
XMS15
XRO
XWO
XR15
XW15
X MATRIX SWITCHES
YO
Y7
YMSO
YMS7
YRWO
YRW7
Y MATRIX SWITCHES
WRINV
WRITE
WREG
WRITE FF
P4N
P7N
READ
RREG
READ FF
P2N
FROM CLOCK
MEMORY AND DIODE MATRIX
VD32
VE32
VD1
VE1
SA32
SA1
DD32
DD1
SENSE AMPLIFIERS (READ)
DIGIT DRIVERS (WRITE)
SR32
SR1
B32
B1
OUTPUT REGISTER
(READ-NORMAL/READ-SHIFT/READ-CIRCULATE)
(A) CALLING GROUP TRANSLATOR
GA15
GA0
(B) CALLED GROUP TRANSLATOR
GB15
GB0
TONE TRANSLATOR
ST
FB
BT
DIGIT TRUNK TRANSLATOR
DT6
DT1
ATTENDANT TRANSLATOR
ATT 12
ATT 1
B30
B25
B22
B17
INHIBIT TIMING
RING LOGIC

scanner via the scan bus. The scanner orders the outgoing message circuit to send the new supervisory state information to the control unit via the digital data message link. The control unit returns a message to the applicable TDC unit. The message contains the idle ***time slot*** number and ***digit trunk*** number selected by the control unit and the number of the ***calling party***. The incoming message signal passes through the transfer and alarms circuit to the incoming message control circuit of each TDC. Every message is processed in both TDC0 and TDC1 of the basic switch unit or TDC2 and TDC3 where provided. The TDC in which the connection is to be made is designated in the message. The other TDC discards the message after reception is completed. The incoming message control loads the message one bit at a time into the least significant bit of the output register during the incoming data time slot. The least significant bit is transferred by a write-shift sequence to the data storage words in the switch store memory and read back into the output register to be further shifted with the next message bit loaded. The read-shift sequence is repeated with each new message bit until the incoming message loading (a bit at a time) is completed. The contents of the received message are then relocated by the addressed TDC from the storage word location to the addressed talking time slot word as assigned by the control unit.

3.09 As the time slot counters periodically advance, the A and B counter output states are alternately gated to and translated by the store address translator circuit into the appropriate X and Y drive currents to address and read the associated time slot word into the output register. The contents of the output register are applied to the group pretranslator (GPX) for translation. Translation of the calling party (A) number and the called party (B) number produces digits for use in the simultaneous selection of the specified line or trunk circuits. The line and trunk circuits may be provided in 15 groups up to 64 circuits each. The selected pair of line or trunk circuit switches and the associated group switches are operated simultaneously during the sampling period of the time slot to establish a transmission path between the calling party and the called party.

3.10 The transmission message described in 3.08 specified connecting the calling party to a digit trunk during each cycle of the time slot sampling. Dial tone is provided from the digit trunk to the calling party via the time-shared connection. Thus, the initial service request by the calling party has been fulfilled. After receiving dial tone, the calling party dials the called party number. The digits are received in a digit receiver in the control unit. The control unit sends another message to the switch unit. The stored talking time slot information now assigns the requested called party (B) number in place of the digit trunk plus ringing instruction for ring-ringback generation. The group pretranslator provides control for immediate, then interrupted ringing. When the called party answers, ringing current is removed at the line circuit, and the control unit, in response to scanner message containing the new supervisory state, deletes the ringing instruction from the time slot word by another message.

3.11 The two TDC units of the basic switch unit operate similarly with each half providing 60 independent talking time slots on the associated intergroup bus (IGB). Each bus, IGB0 or IGB1, has access to all the lines or trunks in the 15 groups. Similarly, IGB2 and IGB3 of TDC2 and TDC3, where provided, also have access to all the 15 line and trunk groups.

3.12 Fig. 15 is the memory and local control for time division connections which shows the switch store with access controlled by a store address translator circuit. The store address translator produces signals to the X and Y matrix switches in accordance with the state of the time slot counter, attendant counter, or scan counter. The attendant counter, enabled by the gate attendant counter (GDB) signal, is employed during time slot A1 to load or read attendant lamp word information. The scan counter, enabled by the S1 time slot signal, is employed for interrogation of lines or trunks and for retrieving last-look information from memory.

3.13 The A and B time slot counters are alternately driven by clock pulse P3. The store address translator produces two sets of output signals on leads X0 through X15 and Y0 through Y7. The signals are combined in the memory, one from each set at a time, to provide one for each word of the switch store.

3.14 The time slot counter circuit generates the total sequence of 65 time slot periods. The 5-stage counter A produces 32 time slots (A0 through A31). The 6-stage counter B produces 33

time slots (B0 through B32). The A and B counters are advanced alternately at clock pulse P3 by the binary counter stage GC3.

3.15 The A counter proceeds through the maximum 32 counts (0 through 31), and the output state of all five stages are ones. The thirty-third count causes the A counter to overflow and change the state of the five stages to all zeros. The B counter similarly proceeds with the counting, except the counter does not overflow after 32 counts. Since six stages are provided, the B counter advances on the thirty-third count, changing the state of the sixth stage to the one state and the other five stages to the zero state. At the thirty-fourth count, the first stage advances to the one state. Since the first and sixth stage outputs are ones, a logic signal is produced which immediately resets the B counter to the all zeros state.

3.16 The A counter circuit controlling the time division connections on one intergroup bus must be synchronized with the A counter in control of talking connections on all the other intergroup buses in the switch unit. Similarly, all B counter circuits must be synchronized.

3.17 The time slot counter synchronizer circuit is employed to synchronize all A counters and all B counters to prevent the spurious generation of crosstalk from one intergroup bus to another in the switch unit. Synchronization of the A and B counters is respectively accomplished by the JCA and JCB signals produced in TDC0 or TDC1. The TDC0 normally has control. The control may be switched from the JCA1 and JCB1 leads to the JCA2 and JCB2 leads by the GRAND SLAM circuit, which is described in the maintenance and attendant circuits of this section. The JCA signal is produced each time the A counter output produces the binary number 11111 (31 decimal). The JCB signal is produced each time the controlling B counter output produces the binary number 100001 (33 decimal), causing the B counter to be reset.

3.18 Fig. 16 is a sequence chart which illustrates the time slot counter circuit timing. The time slot counter circuit timing shown by solid lines provides control for the store cycle and time division connection control functions. These functions are shown by dotted lines and are described in the following subparts. A 1.305 μsec time slot consists of nine 145. nsec clock pulses. A particular A counter time slot is defined by a ground level signal on the GAC7 signal (clock pulse P7 through P6) together with the state of the A counter. Similarly, when the GBC7 signal is at ground level during the next P7 through P6 interval, the B counter state produces a B counter time slot. The GAC3 and GBC3 signals, together with the same A and B counter outputs respectively, define the same time slot A and B on a shifted basis during the P3 through P2 intervals. Thus, the operations associated with a given time slot basically serve three gating functions: store control during clock pulses 7 through 6, store cycle during P1 through P6, and talk connection control during P3 through P2.

3.19 The GC7 reset signal occurs at alternate clock pulse P9 intervals to ensure that the GC3 flip-flop (producing the GAC3 and GBC3 signals) operates in step on a shifted basis with the GC7 flip-flop (producing the GAB7 and GBC7 signals). Thus, if the GC3 flip-flop advances to the reset state at clock pulse P3, the GC7 flip-flop is advanced to the reset state at clock pulse P7. As long as the GC3 and GC7 flip-flops are in step, the reset signal has no effect upon the GC7 flip-flop which is already in the reset state. However, if the synchronizer circuit operation causes the GC3 flip-flop to be out of step with the GC7 flip-flop at clock pulse P9, a reset signal is produced which restores the GAC3 and GBC7 relationship, thereby ensuring that GC7 stays in step with GC3.

3.20 The store address translator (Fig. 15) produces two sets of output signals on leads X0 through X15 and Y0 through Y7. The signals, one from each set at a time, are combined in memory matrix diodes to provide for the selection of one of the 128 switch store words.

3.21 The store address translator provides memory word select signals from the binary output states of the time slot counter, the message address register, the attendant counter, or the scan counter. The time slot counter is employed during the normal sequence of reading talking time slot words. The message address register selects the time slot word to which an incoming transmission message is to be relocated. The attendant counter is employed to read the appropriate lamp information word. The scan counter is employed to retrieve the last-look word from the scan point storage area of memory.

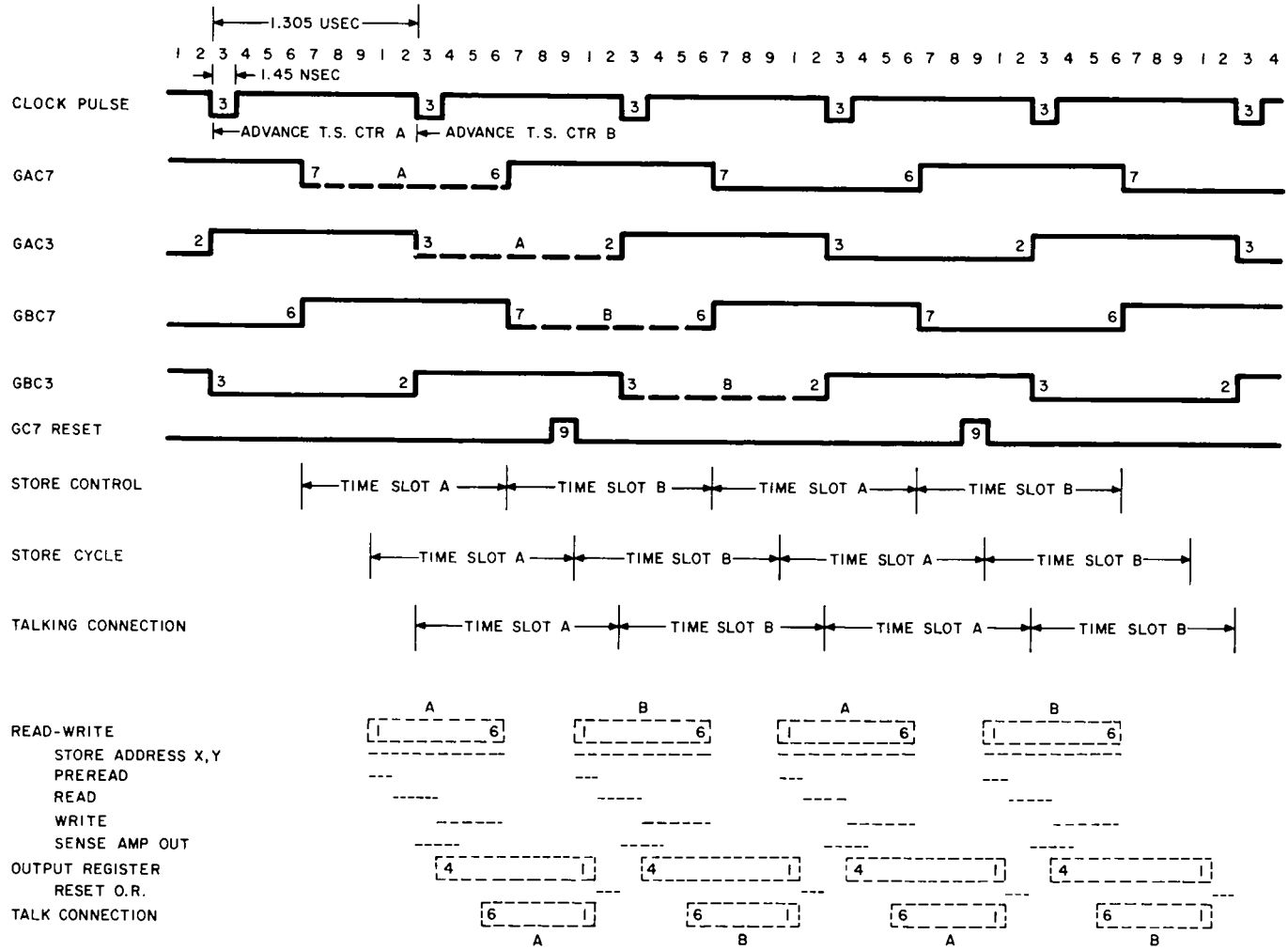


Fig. 16—Time Slot Counter Circuit—Sequence Chart

3.22 The store address translator circuits for X and Y translation consist of input gating and translation circuits for each. The gated input signals are translated into X plane and Y plane select signals which are supplied to the respective X and Y matrix switches of the switch store circuit. The input gating circuit combines the A counter output lead states with the enabling GAC7 signal. Similarly, the B counter output lead states are combined with the GBC7 signal. Thus, the A counter leads, AC0, AC1, and AC2, produce one-hot-out-of-eight signals Y0 through Y7, while leads AC3 and AC4 produce one-hot-out-of-four signals X0 through X3. The A counter produces translation for selection of the first 32 words from the store memory matrix. The B counter similarly produces translation for the second group of 32 store words from the same one-hot-out-of-eight signals Y0 through Y7 (via BC0, BC1, and BC2) and another group of one-hot-out-of-four signals X4 through X7 (via BC3 and BC4). Words 2 through 31, the 30 talking time slot words associated with the A counter, may also be accessed by the message address (MA) register of the incoming message control circuit. MA1, MA3, and MA4 produce the Y0 through Y7 signals, while MA5, MA6, and MA2N produce the X0 through X3 signals. The second half of the talking time slots associated with the B counter may similarly be accessed under control of MA1, MA3, and MA4 for Y0 through Y7, with MA5, MA6, and MA2 producing X4 through X7. Thus, the state of the MA2 output determines which half of the 60 time slot words are to be addressed during message relocation. Words 64 through 103 are used by the scanner for storing the present state supervisory information for lines,

trunks, and maintenance and attendant circuit scan points. The scan counter states LS5, LS6, and LS7 are combined with the S1 signal from the scanner to produce the one-hot-out-of-eight signals Y0 through Y7. Similarly, LS8, LS9, and LS10 produce one-hot-out-of-five signals X8 through X12 during the appropriate data time slot interval for the scanner.

3.23 Words 104 through 111 are allocated to the spare data time slot A1. A battery level output on the X13 lead is produced by a ground level lead T1 during each occurrence of the spare time slot if no incoming transmission messages are being relocated (TMRN and LMRN leads both at ground level). Under these conditions, the AC0 lead translates a Y0 signal and spare word 104 is selected.

3.24 Words 112 through 127 are read during data time slot A0 for attendant lamp lighting. The 32 attendant lamp information words are selected in accordance with the attendant counter state when the GDB lead is at ground level. The DB0, DB1, and DB2 states produce the Y0 through Y7 signals while the DB3 state produces the one-hot-out-of-two signals X14 and X15.

3.25 The attendant counter and scan counter circuits are described in the subsequent subparts of this section associated with the scanner and attendant circuits.

3.26 The switch store circuit provides the memory, matrix switches, sense amplifiers, and digit drivers. The memory provides 4096 ferrite cores arranged in three planes. There are 32 bit planes which provide 128 words in a 2-dimensional (X and Y) array of 8 by 16 words.

3.27 Fig. 17 is a simplified diagram for one word of the memory circuit in one bit plane. The matrix switches provide word selection by producing bipolar (read/write) drive currents in rows and columns which select a word core at the intersecting point in each bit plane. The diode arrangements at each end of the word line eliminate all sneak paths. The sense amplifier input line is coupled to every word core in the associated bit plane for reading the stored information from the core. Also connected to each sense line is the digit driver for writing information into the memory core for storage. Fig. 18 is a simplified diagram of the memory matrix diodes. The elements numbered 1 through 128 are word lines. Each word line passes through all 32 of the bit cores for that word.

3.28 The switch store (Fig. 15) in each half-system provides a 128-word random access ferrite core memory. The memory provides storage for incoming and outgoing messages between the switch unit and the control unit, talking connections, scanner last-look information, and attendant lamp lighting. The talking connection words are read sequentially with one word of the scanner information section and one word of the attendant lamp section. Thus, the talking connection section is cycled (at the 12-kc sampling rate) many times for one complete scan of the store because there are 1216 scan points and a group of attendant lamp loops for six attendants associated with the basic switch unit. The memory circuits of TDC2 and TDC3 may provide lamp information for up to six additional attendants.

3.29 Two 64-word, 32-bit core planes are connected to provide 32 folded bit lines, each 128 words long. Each core plane is a 2-dimensional array of 64 words at right angles to the 32 bit wires. The plan for translation and access in the 2-dimensional word oriented plane of the memory is illustrated in Fig. 19. The words of one 64-word core plane (4 by 16) are selected by X0 through X15, Y0 through Y3, and the words of the other one selected by X0 through X15, Y4 through Y7 to provide the total 128 words (8 by 16).

3.30 The first two words are allocated for the storage of incoming message bits during the data time slot B32. The next 30 words (2 through 31) are employed for the storage of talking time slot words associated with time slots A2 through A31. Words 32 and 33 are employed for interrogation of maintenance scan points and outgoing message bits in conjunction with time slot B0. Another group of 30 words (34 through 63) are employed for the storage of talking time slot words associated with time slots B2 through B31. Words 64 through 101 are allocated for storage of present-state information for a total of 1216 scan points out of scan point numbers 0 through 1343. The next 10 words (102 through 111) are unassigned spares. Words 112 through 127 are assigned for the storage of attendant lamp information which is read during time slot A0.

3.31 The matrix switches (Fig. 15) under control of the store address translator in the switch control circuit provide a bipolar path through the

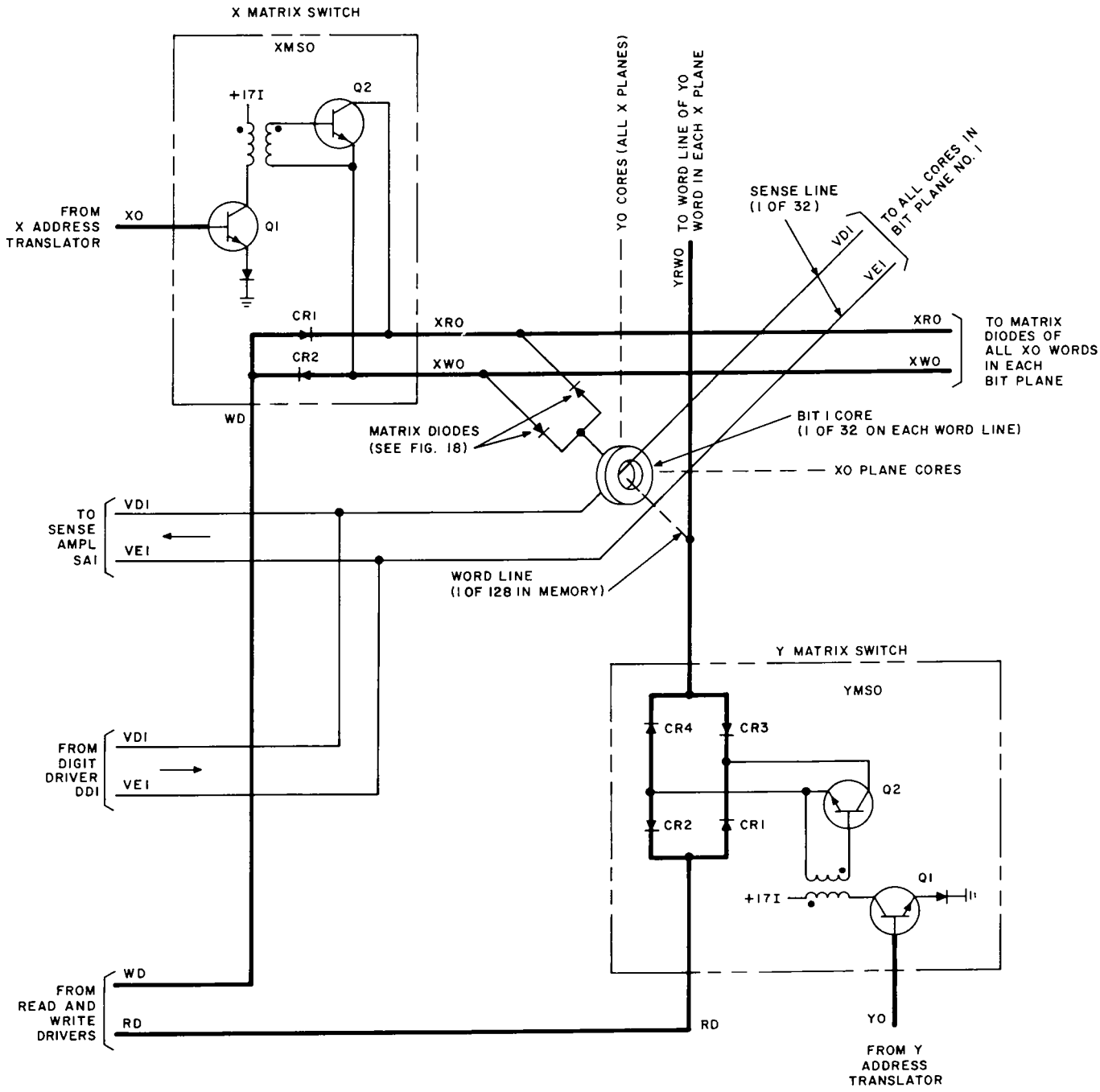


Fig. 17—Memory Circuit (One Bit)—Simplified Diagram

memory at the selected address. The bipolar current pulses are produced by the read and write drivers on the RD and WD leads, respectively.

3.32 The Y matrix switches select one of the eight vertical columns in the diode matrix (Fig. 18). Each Y matrix switch (Fig. 17) consists of a diode bridge (CR1, CR2, CR3, and CR4) which directs current of either polarity through transistor switch Q2. Q2 is driven by Q1 through transformer coupling. A positive pulse on the applicable input lead will turn on Q1 and then Q2 of the selected matrix switch.

3.33 Similarly, the X matrix switches select one of the 11 horizontal rows in the diode matrix.

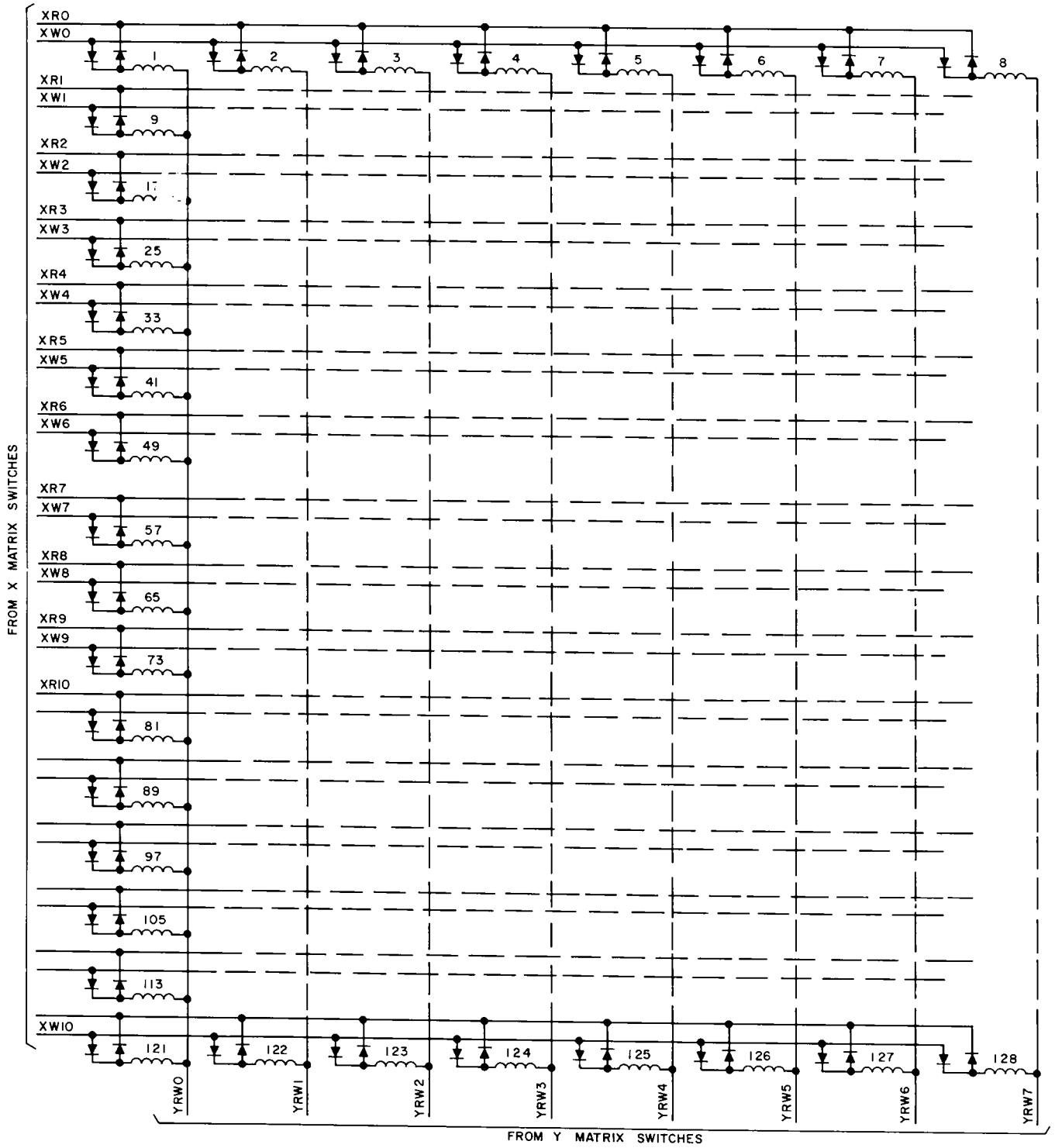


Fig. 18—Memory Matrix Diodes—Simplified Diagram

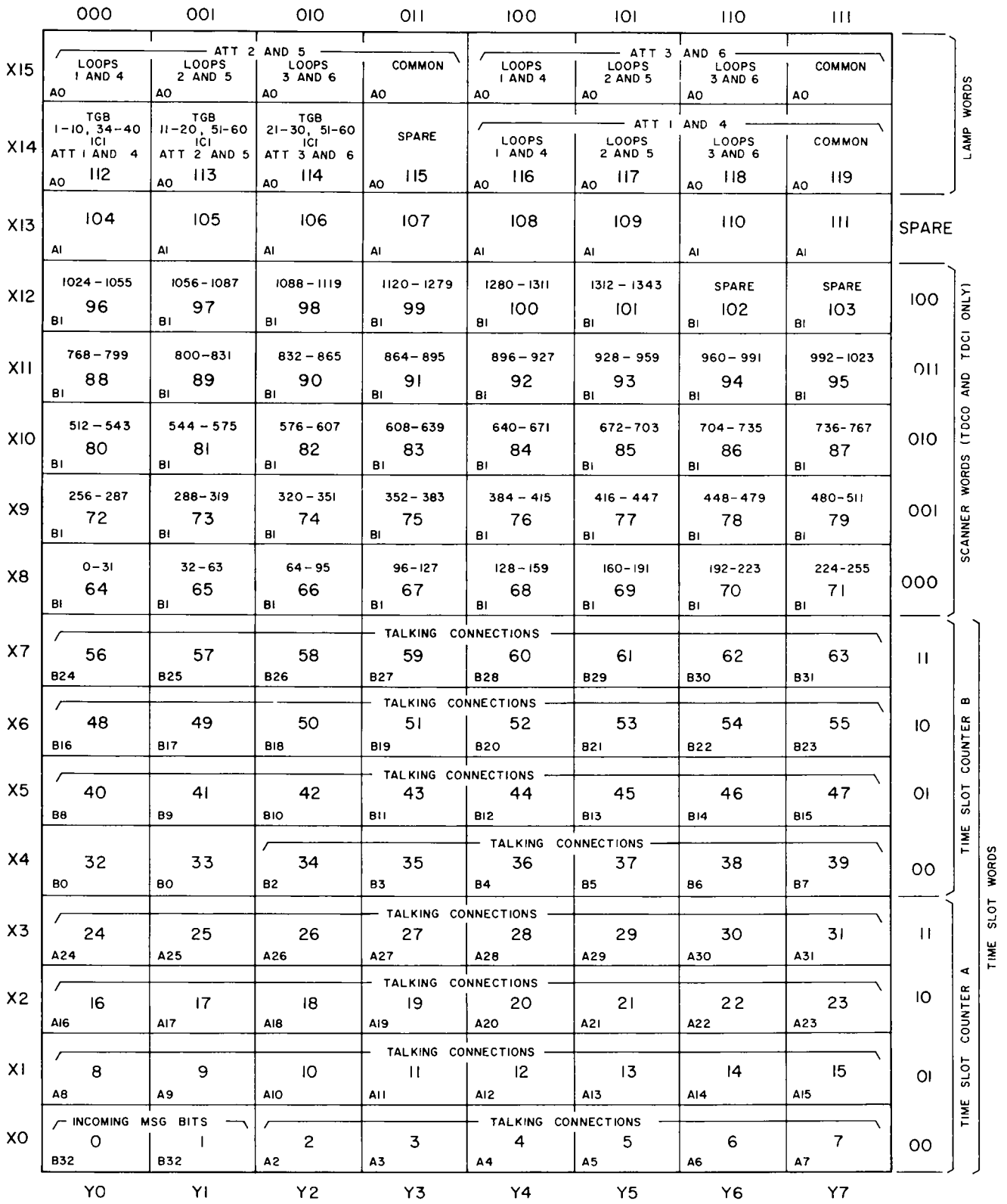


Fig. 19—Memory Word Plan—Store Address Translation and Access

The X matrix switch is identical to the Y matrix switch, except that the two matrix diodes associated with the selected horizontal row and vertical column complete the diode bridge.

3.34 The sense amplifier (Fig. 15) provides amplification, dc restoration, strobing, thresholding, and generates an output pulse. The sense amplifiers discriminate between a 1 signal on a memory output lead (bit line) and a 0 signal plus any noise coupled to the bit line in the memory. The bit line is transformer-coupled to the sense amplifier, which consists of a 2-stage linear amplifier whose gain can be switched. The gain of the sense amplifier is controlled by varying the feedback path. A maximum gain of approximately 50 is provided during read time. At other times, a minimum gain is provided by an ac feedback which produces a forward gain of approximately 1.5. During the strobe interval, the sense amplifier detects whether the input signal is a 1 or a 0.

3.35 The digit drivers are current drivers which are connected one to each bit line (V1 through V32) along the selected word line. The digit driver produces current pulses of the proper amplitude for half selecting all the cores on its associated bit line. The write driver produces the other half select current in the selected word line, and the combined field at the intersection will switch that core to the 1 state. The digit driver is turned on by a ground on the write lead if a ground is also present on the bit numbered V input lead. The V input is supplied by the associated vertical gating circuit from the output register in the switch control.

3.36 The timing circuit of the switch store generates the sequence of timing signals which govern the read and write operations. Read, strobe, and sense amplifier gate signals control the read operation of the sense amplifiers. The write signal controls the write operation of the digit drivers. Fig. 20 illustrates the timing sequence. The 145-nsec pulses (P1N, P2N, P4N, and P7N) from the system clock are applied to the gate, read, strobe, and write flip-flops to produce timing intervals by setting and resetting operations. The write signal from the write flip-flop is applied to the write driver (WREG). Similarly, the read signal is applied to the read driver (RREG). The read and write drivers produce the bipolar current pulses on the RD and WD leads which provide a current path through the selected matrix switches and the word line in the memory.

3.37 The memory drive current requirements change with temperature. A temperature compensated voltage supply provides a negative temperature coefficient to compensate for the temperature variations. The output voltage varies from +17 to +12.5 volts over the temperature range of 0°C to 60°C. The voltage is +15 at normal room temperature (25°C). The voltage is

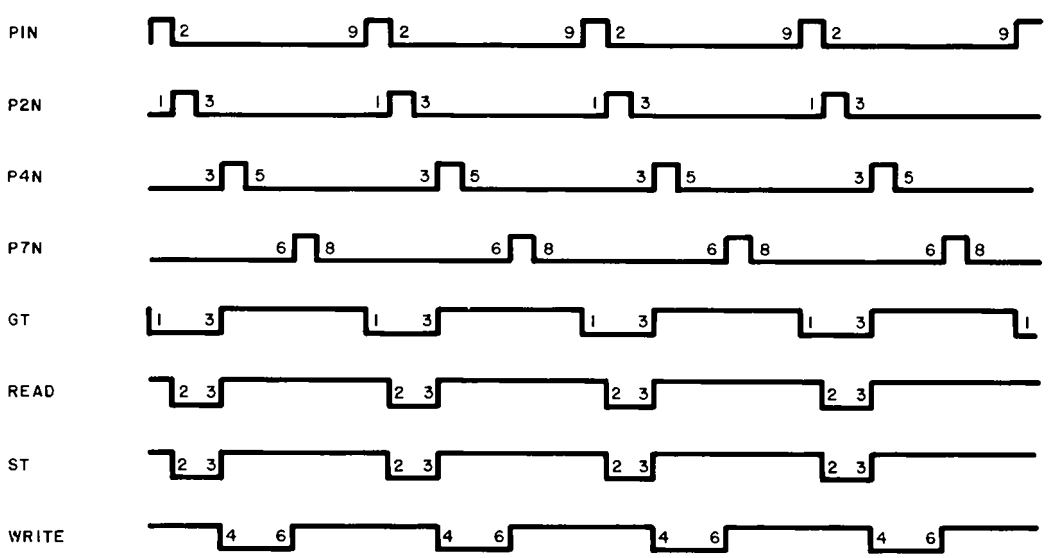


Fig. 20—Switch Store Timing—Sequence Chart

also used as a reference for the write current driver for temperature compensation and secondarily as a regulated voltage in the matrix switches.

3.38 The store output register (Fig. 15) of the switch control temporarily holds the information read from the memory via the sense amplifiers. The sense amplifier outputs SR1 through SR32 are applied to the output register. The output register provides memory information to the group pretranslator circuit. The bit outputs to the group pretranslator are employed to establish talking connections. The 32 output register bits are also employed to transfer information back into memory from the output register via the digit drivers in the switch store. The store output register circuit provides two types of transfer operations, write normal message (WNM) and write shift message (WSM). Both are employed during the data time slots and will be discussed in the subparts on the incoming and outgoing data message, scanner and attendant lamp functions. Also, for simplicity, the output register bit leads employed at the scanner and attendant circuits are not shown in Fig. 15 but are illustrated with the descriptions of their associated functions.

3.39 Fig. 21 shows the transmission time slot word format. The 32-bit information word is divided into two 10-bit address words plus individual bits which control associated operations such as conference calls, continuous or interrupted ring-ringback, and attendant and maintenance functions. The use of the associated bits is discussed separately in other subparts of this section.

3.40 The first 10-bit address word is composed of bits 8 and 10 plus bits 32 through 25 and contains the line circuit group crosspoint number for the calling party (A). The other 10 bits consisting of bits 7 and 9 plus bits 24 through 17 contain the crosspoint number for the called party (B). Each 10-bit word is subdivided into one binary number with four bits to define the group number and a binary number of six bits to define the line or trunk number within the group. The 4-bit number is translated into one-hot-out-of-16 codes (1/16). The 6-bit number is employed in the line and trunk circuits. Similarly, one-hot outputs are provided by the group pretranslator circuit for selecting each of the 6 digit trunks and 12 attendant circuits.

3.41 In Fig. 15, the group pretranslator provides two signals to the IGS logic circuits which signify that all bits are zero for the B party address (AZB) and that all bits are zero for the A party address (AZA). The AZB signal is generated during talking time slots if all nine of the called party bits (B7, B9, and B24 through B17) are 0. The AOCG signal is generated if all calling party bits (B8, B10, and B32 through B25) are 0.

3.42 Signals from the store output register (B19 and B27), the group pretranslator, and the maintenance and attendant circuit are combined in the IGS logic circuit to produce the four clock drive pulse signals (CDB0, CDB1, CGB0, and CGB1) which strobe the intergroup switches. If a binary number is associated with the called party and group bus 0, the B19N lead and the AZB lead will be at ground. Thus, the intergroup switch circuit is strobed by the CDB0 signal if the number is associated with the called party and a group bus 0. The group bus is defined by the state (0 or 1) of B19 or B27. B19 is associated with the called party number while B27 is associated with the calling party number.

3.43 Three special inhibit leads (IHCD0, IHG3, and IHD3) are applied to three of the intergroup switches. The IHCD0 signal inhibits closure of either group 0 intergroup switch (GOB0

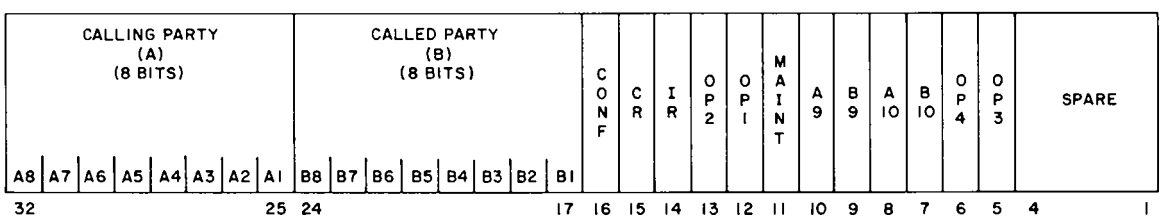


Fig. 21—Memory Word Format—Talking Time Slots

or GOB1), even though the proper group translator and clock drive pulse are present. The IHCD0 signal functions to inhibit when a digit trunk, which is always a called party, is selected. Similarly, the switch G3B1 is inhibited by the IHG3 and/or IHD3 leads when one of three system tones (which have group 3 bus 1 line numbers) in the special group circuits is selected.

3.44 The line and trunk circuit provides input gating, timing signals, and bus clamps for each group of up to 64 line and/or trunk circuits. There can be up to 15 such groups. The input gating and timing signals employed in line or trunk selection are discussed in the following paragraphs.

3.45 Fig. 22 is a block diagram of the line and trunk selection circuits. The line and trunk group select circuits provide independent methods of selecting each line and trunk circuit. Therefore, the group pretranslator and line and trunk group select circuits associated with each time division control may activate any of the line or trunk circuits. The group pretranslators for the A and B party numbers each produce 16 one-hot outputs. The group select circuit combines the calling and called party information with the associated group select pulse from all the time division control circuits into six leads for each party (TA1 through TA6 and TB1 through TB6). The TA1 through TA6 signals, in conjunction with the time division control associated group select pulse, produce an appropriate combination of CAB, VAB, and HAB signals for selection via the AB matrix, while the other set (TB1 through TB6) produces the CBA, VBA, and HBA signals for selection via the BA matrix.

3.46 The AB and BA matrix circuits make it possible for two different lines or trunks in the same group to be simultaneously selected. The matrices also provide reliability protection against certain equipment failures. If a line cannot be selected by one matrix, it can be selected by the other.

3.47 To select a line or trunk circuit within a group, one matrix must simultaneously have a battery level signal on the clocking select input, one of the vertical select inputs, and one of the horizontal select inputs. The applicable outputs from the three applicable line and trunk translators of one matrix enable and strobe the associated line or trunk circuit to produce a talking connection switch closure.

3.48 Two select circuits are employed per group for each time division control. Thus, a full system with 15 groups and 4 TDC units provides 15 groups of 8 select circuits each. Of the two TDC associated select circuits employed in a given group, one circuit gates the six binary bits from the output register associated with the calling party A, and the other circuit gates the B party bits. The six line and trunk group circuit output leads are designated TA1 through TA6 or TB1 through TB6 and gated by the applicable group enable to the line and trunk translators associated with the same group.

3.49 Each line and trunk translator circuit produces the four clock group select signals CAB0 through CAB3 or CBA0 through CBA3, the four vertical select signals VAB0 through VAB3 or VBA0 through VBA3, and the four horizontal select signals HAB0 through HAB3 or HBA0 through HBA3. The binary logic state of the applicable leads TA6 and TA3 or TB6 and TB3 thus determines which gate will produce an output signal when strobed by the resonant transfer timing signal via the maintenance and attendant circuit. The translator gate output leads (CA0 through CA3 or CB0 through CB3) are applied via their respective clock driver circuits to the applicable matrix input leads (CAB0 through CAB3 or CBA0 through CBA3) of the associated group of line or trunk circuits.

3.50 Since the resonant transfer interval is governed only by the clocking group translator circuits, the strobe signal and clock driver circuits are not supplied to the vertical and horizontal translators. The binary logic state of input leads TA5 and TA4 or TB5 and TB4 produces an output signal on the applicable vertical translator output lead VAB0 through VAB3 or VBA0 through VBA3, respectively. Similarly, the horizontal matrix input signals HAB0 through HAB3 or HBA0 through HBA3 are produced in accordance with the binary state of leads TA2 and TA1 or TB2 and TB1, respectively. The vertical and horizontal translator output signals are transmitted directly to the applicable line or trunk circuit input matrices.

SCANNER

3.51 The basic switch unit composed of TDC0 and TDC1 provides a complete scanner capable of interrogating and preparing messages for all switch unit scan points. TDC2 and TDC3 each contain a partial scanner which contains the circuits

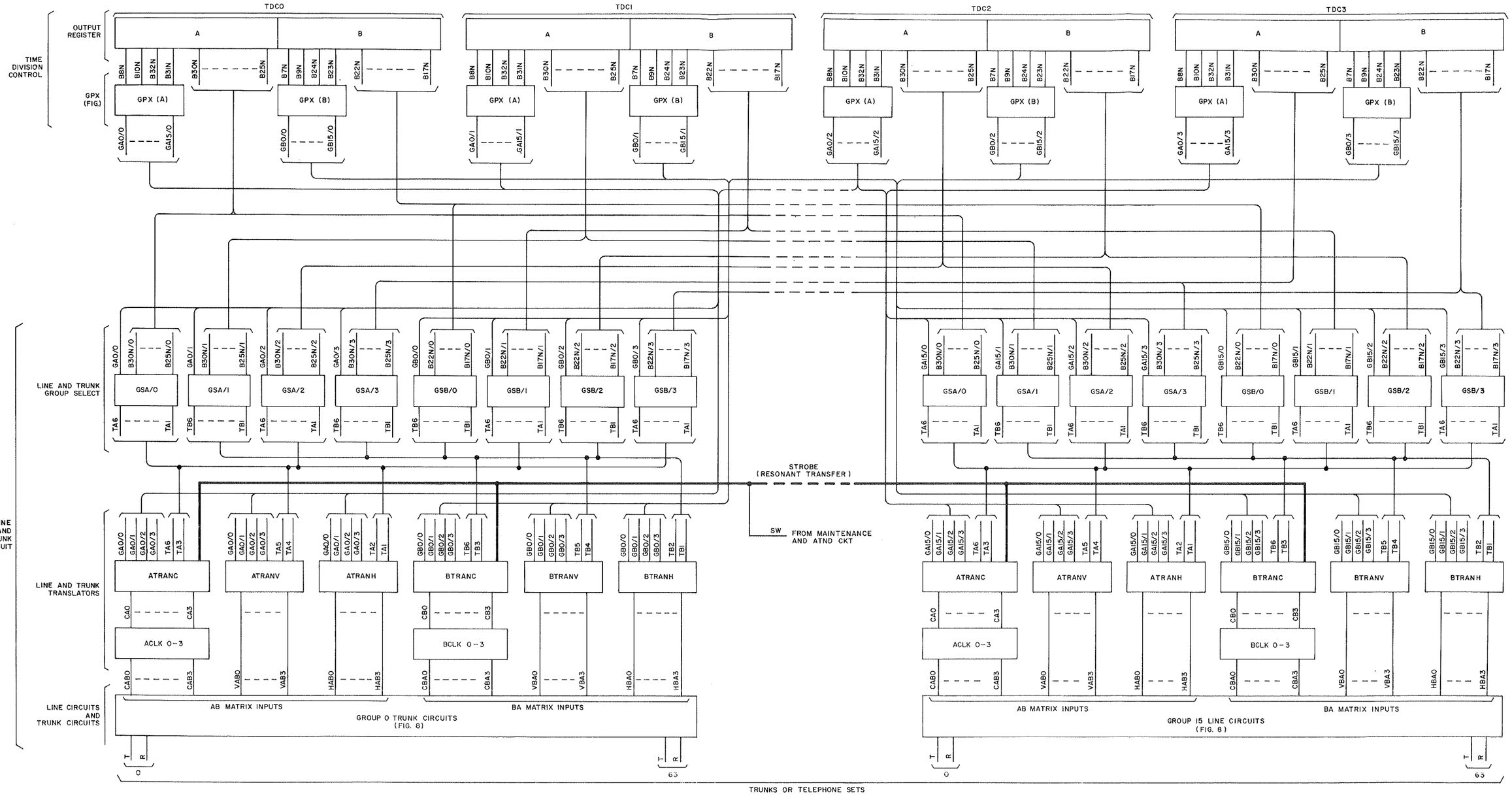


Fig. 22—Line and Trunk Selection Circuits

necessary to inhibit false scanning information caused by dial pulses. The complete scanners are called primary scanners, one of which is on-line while the other is off-line. The partial scanners are called auxiliary scanners. The off-line primary scanner performs only that function which the auxiliary scanners perform (dial pulse filtering). The dial pulse filtering function (see 3.156.1) of the scanners is included in the description of digit trunks. Trouble modes of operation which provide transfer and disable features for the scanner circuits are discussed in the description of maintenance and attendant circuits.

3.52 Fig. 23 is a block diagram of the primary scanner circuit which provides the scan counter, scan bus logic, and scan logic and timing circuits. The scan counter circuit consists of an 11-stage binary counter which is normally advanced once every store cycle if no change of scan state is detected. The scan counter circuit also provides a translator which produces signals that identify the two categories of scan points, the one-way scan point signal, and a 16s count signal for initializing a ring counter employed with maintenance and attendant scanning. The scan bus gating circuit provides an OR gate which combines the 15-line and trunk group associated present-state buses (PS0 through PS15) into a single scan bus (SB) which is applied to the scan logic circuit. The scan logic and timing circuit provides the control for the two types of scan points (LTMA) and for operating in two modes, scan and update. The scan logic and timing circuit also provides temporary storage registers for the present-state and last-look supervisory information, a comparator to detect changes in state, a rescan counter, a last-look storage word update circuit, a message (MSG) control, and a scan counter output control.

3.53 The sequence of scanner operations is controlled by a hardware program consisting of the scan logic and timing circuits. The timing of scanner operations is controlled by the B time slot counter. Time slots B32, B0, and B1 are employed in the scan time slot decoder to produce signals on the respectively associated leads S32, S0, and S1. Fig. 24 is a sequence chart which illustrates the scan time slot decoder timing. The B time slot counter output state and the GBC7 signal are employed to produce the three scanner time slot signals. Three additional time slots (AX, AY, and AZ) are produced immediately following each of the B counter data time slots. Although there is an A counter time slot between any two B counter time slots, the precession between counters causes a different A time slot to be produced between a given pair of B time slots during each cycle. Thus, the TX signal is produced from near the end of the S32 interval to the beginning of the S0 interval. Similarly, the TY signal is produced from near the end of the S0 interval to the beginning of S1. The TZ signal is also produced from near the end of the S1 interval through the following P5 pulse.

3.54 The SON3 and LTSC signals are produced during the B0 interval on a P3 through P2 basis. When the SON3 lead is at battery level, the silent scan interval is produced. The LTSC signal enables the group pretranslator to produce group number selection if the scanner is on-line and is interrogating lines or trunks. (SOL and MASN leads are at ground level).

3.55 Two basic types of scan points are interrogated by the scanner (Fig. 23). The state of the line and trunk or maintenance and attendant (LTMA) flip-flop defines which of the two types of scan points is to be interrogated. The reset state indicates that a line or trunk scan point is about to be interrogated.

3.56 A message (MSG) flip-flop is provided to inhibit scanner operation when the switch control is sending or receiving a message. When the message flip-flop is in the reset state, the scanner circuitry is enabled to operate normally.

3.57 An 11-stage binary scan counter provides the number of the scan point to be interrogated and translators which establish the category of the scan point number. The number is processed through the output register, called party (B) translator, and the line and trunk circuits in the same manner that the line and trunk circuits are selected for talking connections. During the scan point selection and interrogation, however, the time division switch closure is inhibited by the quiet scan circuit which removes power from the time division switch driver circuit.

3.58 The scan counter, a ripple counter, is advanced by the scanner advance (SAV) signal. With no change of scan point supervisory state, the scan counter is advanced every 86.13 μsec. The scan counter output is gated to the output register when line or trunk circuits are to

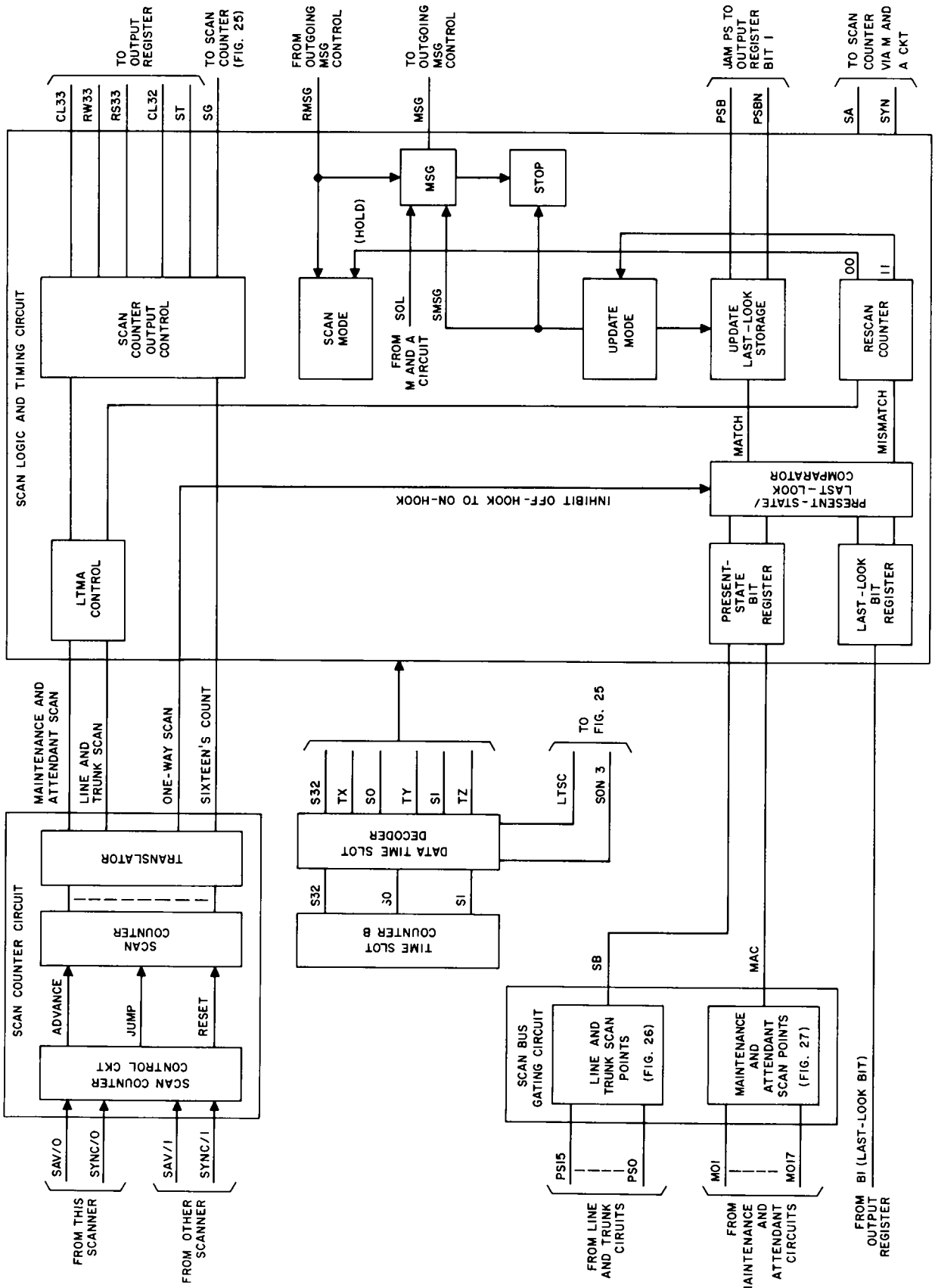


Fig. 23—Primary Scanner Circuit

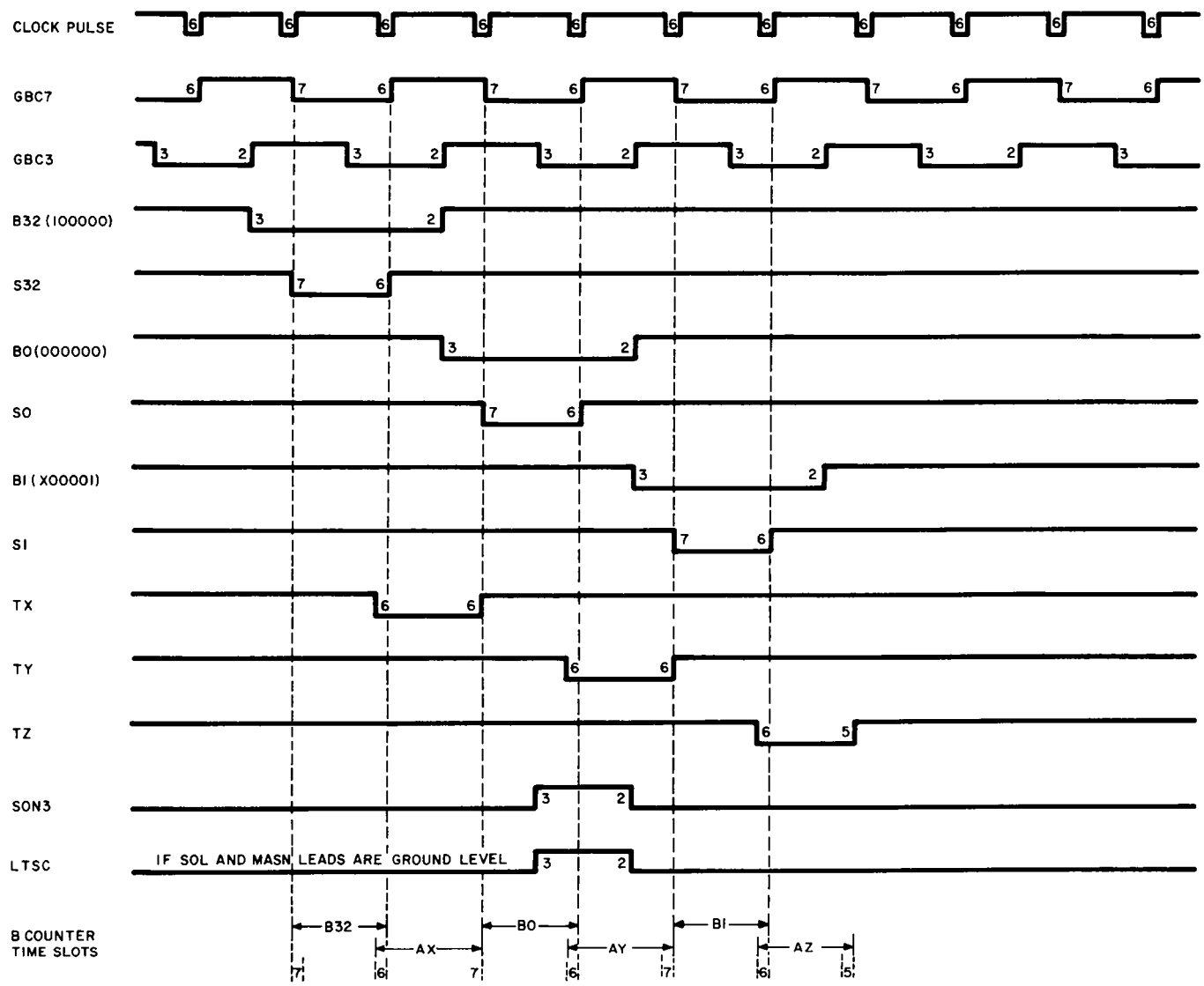


Fig. 24—Scanner Time Slots—Sequence Chart

be interrogated. The two most significant counter bits are also transmitted to output register bits 27 and 26 for use in the outgoing message memory word. The scan counter outputs are also supplied as double rail signals to translators in the scan counter circuit and to the memory access circuits.

3.59 The translator portion of the scan counter circuit (Fig. 23) produces signals which control the sequence of scanning operation. Table B outlines the sequence of operation. The translator establishes which of two categories of scan points is being interrogated. One category is for line and trunk scan points. The other category is for maintenance and attendant scan points (256 through 327 and 1024 through 1343). The LTMA flip-flop is set when the scan counter state reaches 256. The LTMA flip-flop is reset when the scan counter state reaches 328. The LTMA flip-flop is again set when the scan counter reaches state 1024 to produce a maintenance and attendant second scan operation. The LTMA flip-flop is held in the set state until the scan counter reaches state 1344.

3.60 The majority of the 1216 scan points are called 2-way scan points because a message is required when both off-hook and on-hook changes are detected. However, there are four blocks of one-way scan points in the two areas of maintenance and attendant scan points which require a message

TABLE B

SCAN COUNTER TRANSLATOR OPERATION

SCAN COUNTER STATE												
BINARY											DECIMAL	OPERATION
1024	512	256	128	64	32	16	8	4	2	1		
0	0	1	0	0	0	0	0	0	0	0	256	Set LTMA
0	0	1	0	0	0	0	1	0	0	0	264	Set OM
0	0	1	0	0	0	0	1	0	0	0	264	PF signal
0	0	1	0	1	0	0	0	0	0	0	320	Reset OM
0	0	1	0	1	0	0	1	0	0	0	328	Reset LTMA
1	0	0	0	0	0	0	0	0	0	0	1024	Set LTMA
1	0	0	0	0	0	0	1	0	0	0	1032	Set OM
1	0	0	0	1	0	0	0	0	0	0	1088	Reset OM
1	0	0	0	1	0	0	1	0	0	0	1096	Set OM
1	0	1	0	0	0	0	0	0	0	0	1280	Reset OM
1	0	1	0	0	0	0	1	0	0	0	1288	Set OM
1	0	1	0	0	0	0	1	0	0	0	1288	PF signal
1	0	1	0	1	0	0	0	0	0	0	1344	Reset OM
1	0	1	0	1	0	0	0	0	0	0	1344	Reset LTMA
X	X	X	X	X	X	X	0	0	0	0	16s	Initialize ring counter via C16

only for on-hook to off-hook changes. The one-way scan points are 264 through 319, 1032 through 1087, 1096 through 1151, and 1288 through 1343. To define the one-way subcategory, the one-way message flip-flop (OM) is provided to register whether the scan point is one-way (set) or 2-way (reset). The OM flip-flop (see Table B) is set at scan counter state 264, reset at scan counter state 320, set a second time at the 1032 count, and reset at 1088. The OM flip-flop is set a third time at 1096, reset at 1152, set for the fourth time at 1288, and reset at 1344. The OM flip-flop, when set, inhibits the sending of a message when the present-state change information changes to on-hook.

3.61 Another function of the translator is to generate a ground signal on the C16 lead each time the four lower order stages of the scan counter are all 0. The C16 signal is required for initializing the ring counter word (store word 33) which produces the maintenance scan interrogation signal. Word 33 is a ring counter word containing a single 1 which circulates successively through store output register stages B1 through B16. As the bit shifts from stage to stage, it interrogates successive groups of 16 scan points each. Seventeen groups of 16 or a total of 272 maintenance or attendant scan points are provided. The interrogation procedure is further discussed in 3.71.

3.62 The scan counter control circuit produces signals causing the scan counter to advance, jump, and reset. The primary scanner which is on-line provides the control (SAV/0 or SAV/1) which advances the scan counters associated with all four time division controls. The scan counters are advanced only during the update cycle at time slot TZ if no message is being sent and the scanner is on-line. If a message is being sent, the scan counter advance signal is inhibited. The MSG flip-flop is reset at the end of a message by the reset scan logic (RMSG) signal from the outgoing message control circuit in the switch control. It should be noted that the MSG flip-flop in the off-line scanner

is set by the SOL lead to inhibit the preparation of messages by the off-line scanner.

3.63 The scan counter advances from binary 00000000000 to 10001111111 (decimal 1151). The next count, 10010000000, produces a reset signal which jams the 128 counter stage to a zero. The count registered is 10100000000 because the reset to 0 state of the 128 bit produces a carry signal to advance the 256 bit to a 1. Thus, the counter state jumps from scan point 1152 to 1280.

3.64 The on-line primary scanner also controls the synchronization of scan counters. Synchronization is necessary to ensure proper operation of the dial pulse filter logic. The on-line primary scanner produces the SYN signal when the count is 10101000000 (decimal 1344).

A. Scan Operation

Line and Trunk Scan Points

3.65 The scan logic and timing circuit (Fig. 23) operates for interrogating line or trunk scan points and is in the scan mode. The switch control is not sending a message. Under the stated conditions, the output of the scan counter is transferred at time slot S0 to the output register for translation and selection of the scan point. The sense amplifier readout is inhibited by the CL32 signal, thereby preventing the contents of word 32 in the store from being read into the output register as would normally occur during time slot S0. The scanner also gates a start bit (ST) for the message into bit 28 of the output register where it is read back into word 32 of the memory.

3.66 Fig. 25 is a scan point selection and interrogation block diagram for lines and trunks which shows the scan counter output applied via LS10, LS9, and LS8 leads through LS1 to the output register to produce bits B7, B9, and B24 through B17, respectively. The four most significant output register bits are processed through the B portion of the group pretranslator (GPX) to produce the appropriate group one-hot-out-of-16 signals for application to the final translators in the line and trunk circuits. The final translators employ the six least significant bits to produce the clock, vertical, and horizontal one-hot-out-of-four signals which select the line or trunk circuit to be interrogated.

3.67 The interrogated line or trunk circuit produces a signal on the group associated present-state bus (PS0 through PS15) output from the applicable group circuit to the scan bus gating circuit (Fig. 26). The scan bus gating circuit combines the 15 group present-state leads in an OR gate to provide a single present-state scan bus (SB) lead to the scan logic and timing circuit. If the scan point is off-hook, the group scan bus signal produces a set signal to the present-state (PS) flip-flop. The PS flip-flop provides temporary memory for the present supervisory state. During talking time slots, the present-state signal is employed to generate rotary dial pulse information, which is converted to tones acceptable to the digit receivers at the control unit. The scan bus gating circuit transmits the present-state signal associated with the calling party (A) when the called party (B) is a digit trunk or special service trunk. The conversion of rotary dial pulse information is discussed in 3.155. The present-state signal employed for scanner action is always selected through the called party (B) group translation.

3.68 The present-state/last-look compare circuit (Fig. 23) detects changes in supervisory state between the scanned present-state and the stored last-look information. During time slot S1, the last-look bit from the store output register is gated via the B1 lead to set the last-look (LL) flip-flop if the scan point was previously off-hook. Thus, the PS and LL flip-flops at this point are registering the scan point states of the present and last-look, respectively. The double-rail outputs of the PS and LL flip-flops are compared; if a supervisory state change has occurred, a mismatch signal is generated. If the comparator output indicates that the scan states compared satisfactorily, no further scan cycle functions are required and the scan logic circuit is advanced to the update mode. The PS and LL flip-flops are reset during time slot S0 prior to each register and compare operation. If the present-state and last-look information are not identical, the scan logic circuit does not advance to the update mode.

3.69 When the result of the first interrogation and comparison with the last-look indicate that a change of state has occurred, the comparator output provides a mismatch signal to advance the rescan counter. The rescan counter circuit provides the control to interrogate the same scan point three times when a change is detected to ensure that the detected state is a legitimate change rather

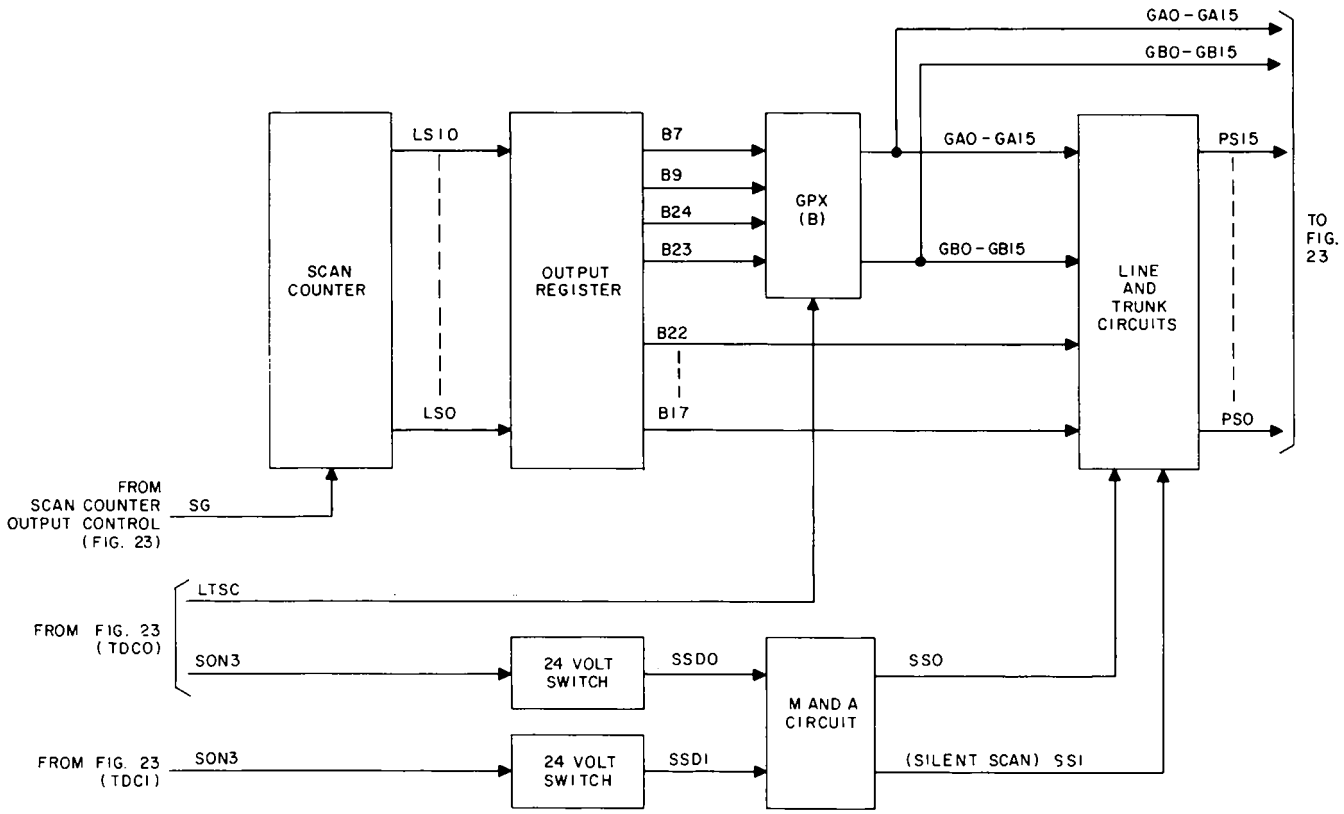


Fig. 25—Line and Trunk Scan Point Selection and Interrogation—Block Diagram

than a transient condition. The rescan is accomplished using the 2-stage binary counter. The rescan counter, initially in the 00 state, is advanced to the 01 state by the first mismatch detected. When the rescan counter provides a zero-not signal, a delay is provided between each of the next two rescan counter advance iterations. The rescan delay circuit employs attendant counter and lamp phase generator signals to produce several milliseconds of basic delay before the next rescan counter advance, even though the scan point is being rescanned once each store cycle.

3.70 The first advance of the rescan counter produces an output state 01. The same scan point will be interrogated again at the next time slot 32, and if the comparator circuit still indicates that the supervisory state is changed, the scan counter will advance to produce an output count of 10. If the result is still the same after the next pass (TS32), the rescan counter advances to the 11 state. After the third interrogation, the rescan counter advances to the 11 state, and the scan logic and timing circuit can then be advanced to the update mode at time slot S32; a send message (MSG) signal is generated. The MSG signal stops scan logic and timing circuit operation and starts the outgoing message control operation. The PS and LL flip-flops during the rescan mode are reset before each interrogation to ensure that the state of the PS flip-flop actually corresponded to the state of the scan point for each of the three successive interrogations. If at any point in the rescan procedure, however, a match occurred between the PS and LL flip-flop output states, the rescan counter would return to the 00 state. Otherwise, the RMSG signal lead is generated by the outgoing message control circuit after a message has been sent. The RMSG signal resets the outgoing message control circuit and enables the scan logic and timing circuit to operate in the update mode, thus allowing the scanner to resume normal operation.

Maintenance and Attendant Scan Points

3.71 The maintenance and attendant scan points are not associated with circuits accessed

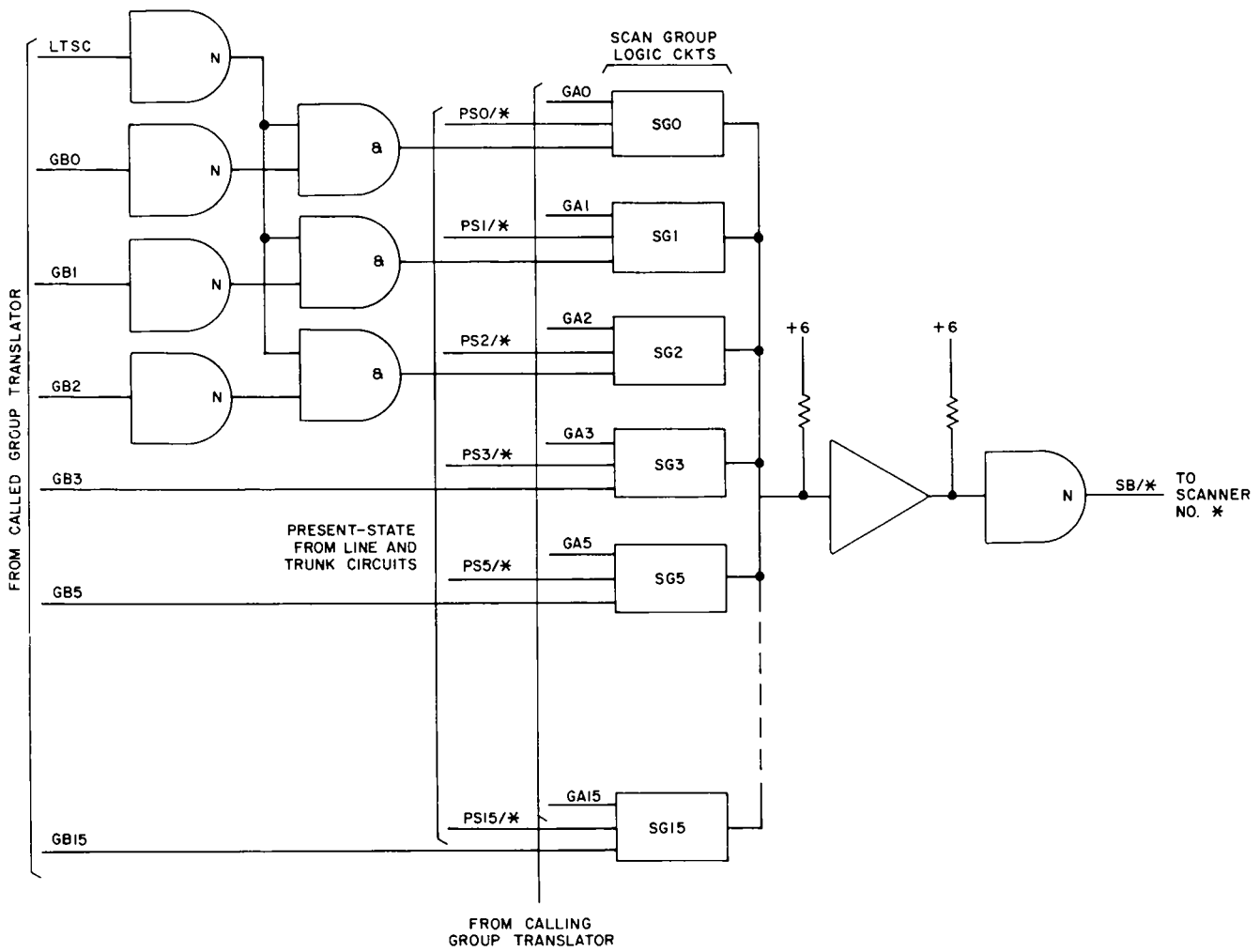


Fig. 26—Scan Bus Gating Circuit

during time division connections as was the case with line and trunk scan points. Therefore, a different method of translating a given scan counter state into an interrogation signal is employed for application to the appropriate maintenance or attendant scan point.

3.72 Since the scan logic and timing circuit (Fig. 23) is operated in the maintenance and attendant mode and the scanning mode during the scan cycle for maintenance and attendant scan points, a read word 33 (RW33) signal is produced during each time slot S0. The CL33 signal inhibits the sense amplifiers every sixteenth time slot S0 to clear the output register and jam bit 1 of the output register to initialize word 33. Word 33 is employed as a ring counter in the process of interrogating maintenance and attendant scan points. The ring counter word is cleared and initialized at each sixteenth occurrence of time slot S0 under the control of the C16 lead from the scan counter translator circuit. The maintenance and attendant common (MAC) bus signal sets the present-state flip-flop in accordance with the state of the scan point being interrogated.

3.73 The maintenance and attendant scan point selection and interrogation is shown in Fig. 27. The output register is employed during time slot S0 as a ring counter into which a single 1 has been jammed. The 1 is shifted a stage at a time from B1 to B16 by means of the read shift word 33 (RS33) feature of the output register. The contents (B1 to B16) of word 33 are gated to each

of the maintenance and attendant scan point circuits when the RW33 lead is activated.

3.74 Seventeen maintenance and attendant scan point circuits may be provided in the attendant circuit. Fig. 28 is a diagram of a typical scan point circuit which consists of scan point gates and common scan bus OR gates. The on-line switch control circuit (TDC0 or TDC1) produces, if the scan point state is off-hook, an output pulse on the applicable MO*/0 lead to scanner circuit No. 0 and MO*/1 lead to scanner circuit No. 1. The asterisk (*) denotes the number of the applicable scan point circuit. Scan point circuits 1 through 17 have outputs MO1 through MO17, respectively. The applicable output leads are applied to their respective scanners (0 or 1). The output pulse indicates to the on-line scanner circuit that the interrogated scan point was off-hook.

3.75 The maintenance scan circuit output leads MO1 through MO17 (Fig. 26) are combined in translator circuits to produce a signal for off-hook conditions on the MAC lead which sets the PS flip-flop. The LS9 and LS7 signals, which are not required in the translation of maintenance and attendant scan points, are not provided. The four least significant bit states (LS0 through LS3) which produce the ring counter operation are not provided at this stage of translation. The LS10 and LS8 leads thus produce the 01, 10, and 11 states which allow the respectively associated translation gates 000 through 100, 000 through 111, and 000 through X11 to operate in accordance with the states of the LS6, LS5, and LS4 leads.

3.76 Table C shows the maintenance and attendant scan point format. The ring counter in word 33 is initialized 17 times. The first initialization occurs at scan point number 256. The initialization is repeated at scan point numbers 272, 288, 304, 320, 1024, 1040, 1056, 1072, 1088, 1104, 1120, 1136, 1280, 1296, 1312, and 1328. Thus, a total of 17 times 16 or 272 scan points could be interrogated by the outlined method of operation. Although 80 scan points could be provided in the circuits MO1 through MO5, only 72 scan points are actually interrogated, after which line and trunk scanning resumes (328). The remaining 192 maintenance and attendant scan points are interrogated by MO6 through MO17, beginning with scan point number 1024.

3.77 The single 1 which appears in the output register bits B1 through B16 during time slot S0 produces the positive pulse which simultaneously interrogates the corresponding scan points in all 17 columns of Table C (except where the scan point gate circuits are not provided, ie, scan point numbers 328 through 335). However, the state of only one of the 17 scan points is gated to the common bus through the final translation stage under control of the LS leads of the scan counter which provide the 16s count. Thus, the scan point interrogations are transmitted one at a time, in sequence, by the column as shown in Table C. A column is provided which designates the scan point by function type, maintenance (M) or attendant (A). The OW column designates the category of the scan point. The 1 designates a one-way scan point and corresponds to the state of the OW flip-flop. Similarly, the 0 corresponds to the OW flip-flop state for 2-way scan points.

3.78 During the last-look time slot (time slot S1), scanner operations are the same for all scan points. The last-look bit (B1) from the last-look storage word via the output register is gated to the LL flip-flop when the scan logic and timing circuit is in the scan mode. The rescan procedure described for lines and trunks is not used for maintenance attendant scan points. If a mismatch exists between the states of the PS and LL flip-flops when scanning maintenance and attendant scan points, the rescan counter is jammed to the 3 state to immediately generate an SMSG signal at time slot S32.

B. Update Operation

3.79 Scanner operations are exactly the same during the update operation for all line and trunk scan points and the 2-way maintenance and attendant scan points. Where one-way maintenance and attendant scan points are involved, if the change of state is from on-hook to off-hook, an outgoing message is sent to the control unit; the updating operation is identical to that for other types of scan points. If the change of state is from off-hook to on-hook, no message is sent to the control unit since this information for one-way scan points is extraneous. However, the last-look area must be updated so that the next change of state from on-hook to off-hook may be detected for the same scan point.

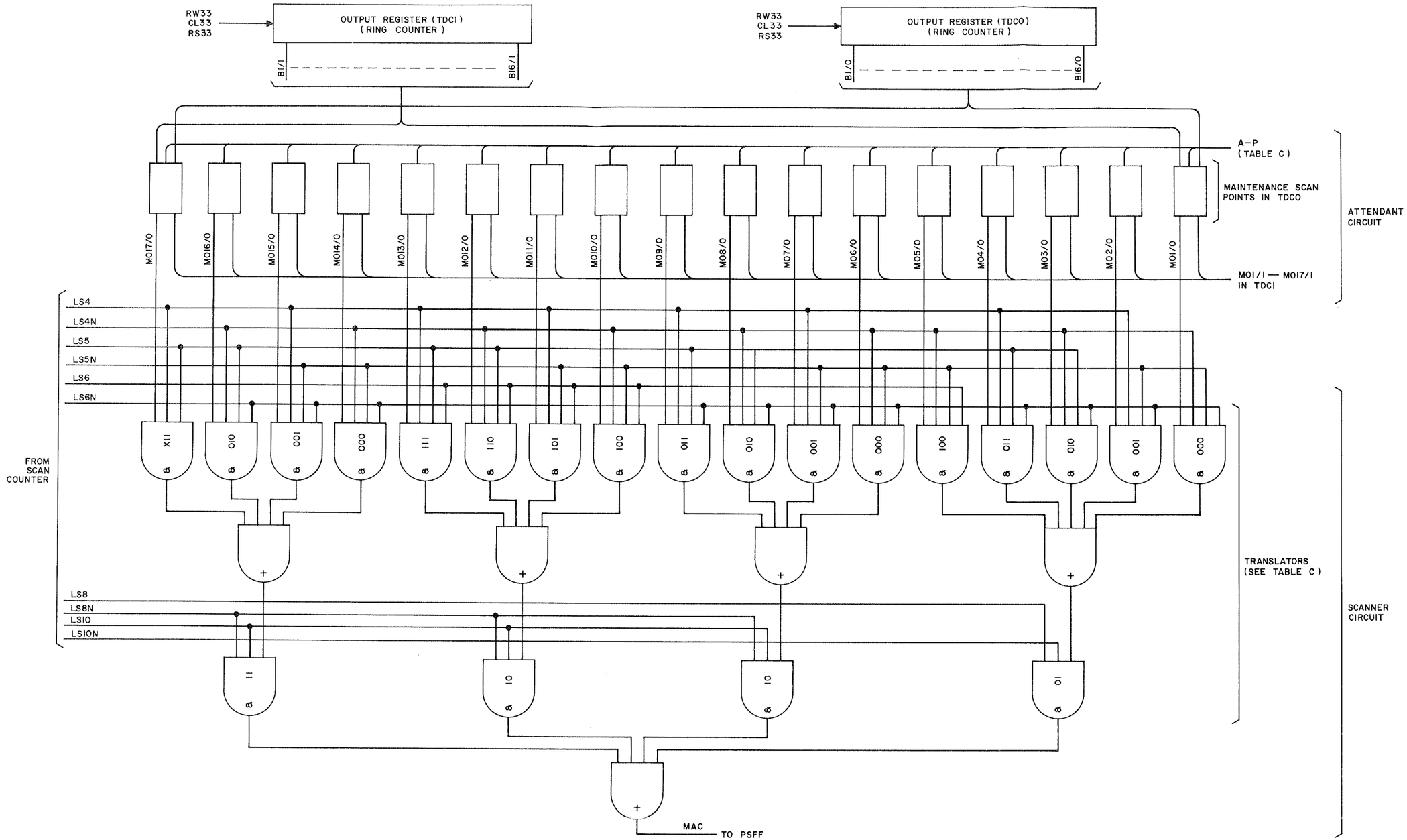


Fig. 27—Maintenance and Attendant Scan Point Selection and Interrogation

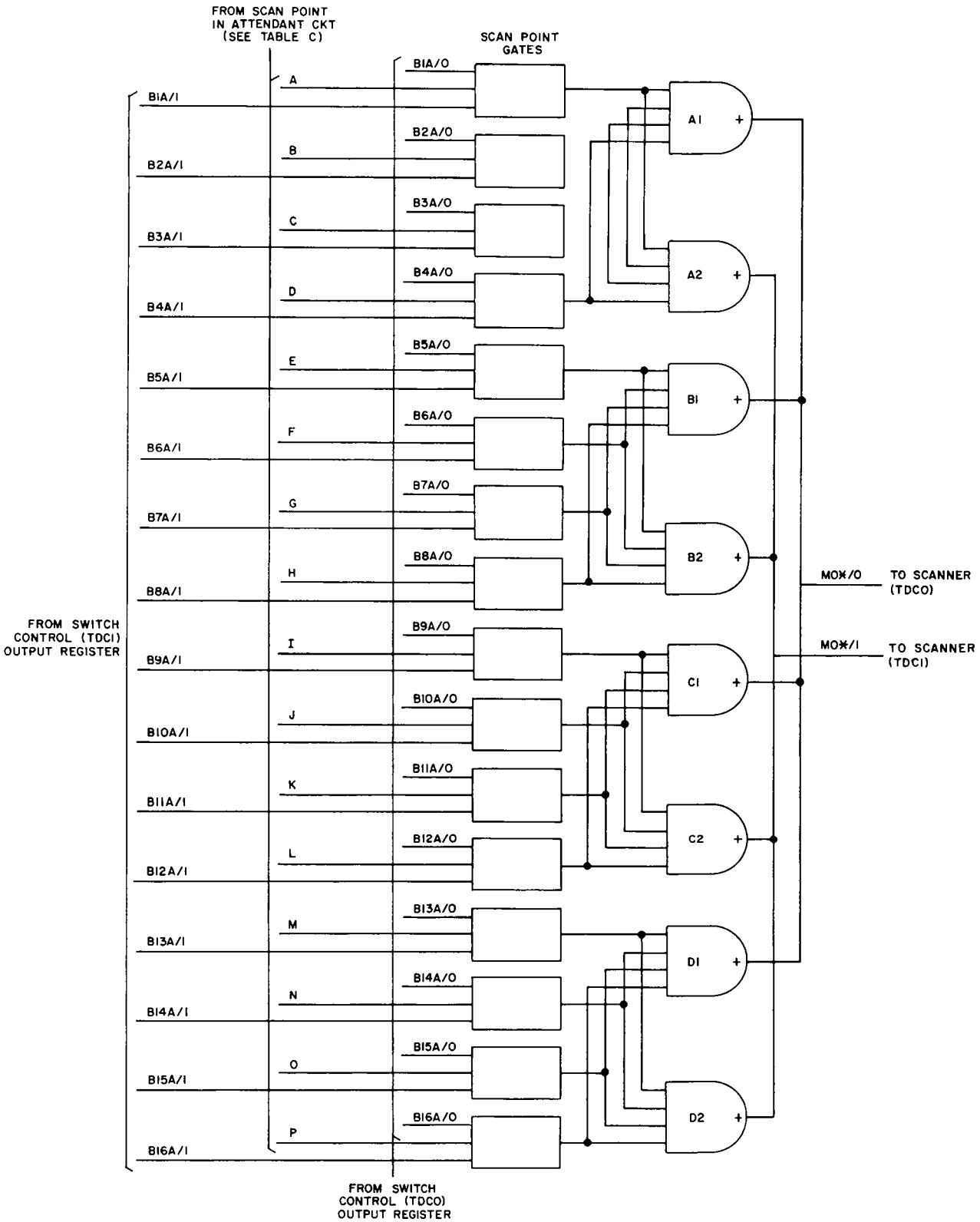


Fig. 28—Typical Scan Point Circuit Located in Attendant Circuit

3.80 An update operation is required if a mismatch occurs, causing the rescan counter to be advanced or jammed to the binary 11 state. The update operation begins at time slot S0 when the outgoing message information (start bit, scan point number, and present state) is loaded into word 32. During time slot S1, two functions are performed. First, the last-look storage word must be updated. Then, if a message is required, the outgoing message control circuit must be activated.

3.81 During time slot S0, a clear word 32 (CL32) signal is produced. The start bit (ST) is gated to output register bit 28, the scan counter output is gated by the SG signal to bits 27 through 17, and the present-state message (PSM) bit is sent to output register bit 16. The last-look bit, which circulates whithin the appropriate last-look word in accordance with the scan counter state, appears at bit 1 of the output register during time slot S1. As shown in Fig. 23, a double-rail present-state bus signal is gated to the output register via the PSB and PSBN leads to set bit 1 in accordance with the PS flip-flop state.

3.82 If a message is required (MSG flip-flop has been set), the STOP flip-flop is set during time slot S1. The STOP flip-flop, when set, inhibits the ST, SG, and CL32 signals while a message is being sent to the control unit. The MSG flip-flop, when set, inhibits all other scanner circuit functions. Thus, all scanner operation is inhibited, and the outgoing message control circuit of the associated switch control is activated. After the outgoing message process is completed, the RMSG signal is generated, which reactivates scanner operation and allows continuation of the update cycle to completion.

3.83 The UP and STOP flip-flops are reset, and the scan counter is advanced to the next scan point at time slot TY after the MSG flip-flop is reset. The scanner resumes the normal operation to interrogate the succeeding scan points.

MESSAGES

3.84 Two-way digital data communication links are provided between the 3A switch unit and the control unit and consist of digital data transmitter and receiver circuits at each end of a pair of data trunks and message control circuits. The digital data transmission equipment is described in Section 240-102-101. The message processing discussed in this section, 240-101-103, is limited to the outgoing message control circuit and the incoming message control circuit.

A. Outgoing Message Processing

3.85 When the outgoing message control circuit receives the signal from the scanner that a message is required, a sequence is started which transfers the contents of the scan message store word (word 32) a bit at a time to the data transmitter circuit. The rate at which the message bits are transmitted is governed by an oscillator in the data receiver circuit which supplies a timing signal via the maintenance and attendant transfer and alarm circuit to the outgoing message control circuit. The timing signal is processed through a 4-stage counter located in the outgoing message control circuit to provide a square wave with a period of 1.56 msec which governs the duration of each bit in the outgoing message. The counter output is employed to operate a read-circulate message routine during time slot B0. The read-circulate message routine transfers the stored data from bit 29 of the output register, one bit at a time, as a serial message output to the data transmitter for transmission to the control unit.

3.86 The read-circulate message routine consists of a 3-step sequence which ***reads*** from the switch store, ***shifts*** each bit to the next higher numbered bit, and ***writes*** the shifted information back into the switch store. Each time the process is repeated, the next lower numbered bit will successively appear at bit 29 of the output register during time slot B0 for transfer to the outgoing message control circuit.

3.87 In the outgoing message control circuit, the message content is serially shifted through bit 29 which is applied to the next bit register (NB) during each time slot B0 for subsequent transfer to the present bit register (PB). The present bit is applied to the data transmitter input.

3.88 When the start bit (ST), a one originally in bit 28, has been circulated (through bit 32, 1, 2, etc.) a sufficient number of times to appear in bit 9 of the output register, the parity generator output is gated to the next bit register for transmission with the outgoing message. When the one is further shifted from bit 9 to bit 12, a reset message (RMSG) signal is generated which clears the outgoing message control circuits and

TABLE C

MAINTENANCE AND ATTENDANT SCAN POINT INTERROGATION FORMAT

		MO1			MO2			MO3			MO4			MO5			MO6			MO7			MO8			MO9			MO10			MO11			MO12			MO13			MO14			MO15			MO16			MO17		
		SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW	SCAN PT	TYPE	OW
A	B1	256	M	0	272	A	1	288	A	1	304	A	1	320	A	0	1024	A	0	1040	A	1	1056	A	1	1072	A	1	1088	A	0	1104	A	1	1120	A	1	1136	A	1	1280	M	0	1296	A	1	1312	A	1	1328	A	1
B	B2	257	M	0	273	A	1	289	A	1	305	A	1	321	A	0	1025	A	0	1041	A	1	1057	A	1	1073	A	1	1089	A	0	1105	A	1	1121	A	1	1137	A	1	1281	M	0	1297	A	1	1313	A	1	1329	A	1
C	B3	258	M	0	274	A	1	290	A	1	306	A	1	322	A	0	1026	A	0	1042	A	1	1058	A	1	1074	A	1	1090	A	0	1106	A	1	1122	A	1	1138	A	1	1282	M	0	1298	A	1	1314	A	1	1330	A	1
D	B4	259	M	0	275	A	1	291	A	1	307	A	1	323	M	0	1027		0	1043	A	1	1059	A	1	1075	A	1	1091		0	1107	A	1	1123	A	1	1139	A	1	1283	M	0	1299	A	1	1315	A	1	1331	A	1
E	B5	260	M	0	276	A	1	292	A	1	308	A	1	324	M	0	1028		0	1044	A	1	1060	A	1	1076	A	1	1092		0	1108	A	1	1124	A	1	1140	A	1	1284	M	0	1300	A	1	1316	A	1	1332	A	1
F	B6	261	M	0	277	A	1	293	A	1	309	A	1	325	M	0	1029		0	1045	A	1	1061	A	1	1077	A	1	1093		0	1109	A	1	1125	A	1	1141	A	1	1285	M	0	1301	A	1	1317	A	1	1333	A	1
G	B7	262	M	0	278	A	1	294	A	1	310	A		326	M	0	1030		0	1046	A	1	1062	A	1	1078	A	1	1094		0	1110	A	1	1126	A	1	1142	A	1	1286	A	0	1302	A	1	1318	A	1	1334	A	1
H	B8	263	A	0	279	A	1	295	A	1	311	A	1	327	M	0	1031		0	1047	A	1	1063	A	1	1079	A	1	1095		0	1111	A	1	1127	A	1	1143	A	1	1287	A	0	1303	A	1	1319	A	1	1335	A	1
I	B9	264	M	1	280	A	1	296	A	1	312	A	1	(328)			1032		1	1048	A	1	1064	A	1	1080	A	1	1096		1	1112	A	1	1128	A	1	1144	A	1	1288	M	1	1304	A	1	1320	A	1	1336	A	1
J	B10	265	M	1	281	A	1	297	A	1	313	A	1	(329)			1033		1	1049	A	1	1065	A	1	1081	A	1	1097		1	1113	A	1	1129	A	1	1145	A	1	1289		1	1305	A	1	1321	A	1	1337	A	1
K	B11	266	M	1	282	A	1	298	A	1	314	A	1	(330)			1034		1	1050	A	1	1066	A	1	1082	A	1	1098		1	1114	A	1	1130	A	1	1146	A	1	1290		1	1306	A	1	1322	A	1	1338	A	1
L	B12	267	A	1	283	A	1	299	A	1	315	A	1	(331)			1035		1	1051	A	1	1067	A	1	1083	A	1	1099		1	1115	A	1	1131	A	1	1147	A	1	1291		1	1307	A	1	1323	A	1	1339	A	1
M	B13	268	M	1	284	A	1	300	A	1	316	A	1	(332)			1036		1	1052	A	1	1068	A	1	1084	A	1	1100		1	1116	A	1	1132	A	1	1148	A	1	1292		1	1308	A	1	1324	A	1	1340	A	1
N	B14	269	A	1	285	A	1	301	A	1	317	A	1	(333)			1037		1	1053	A	1	1069	A	1	1085	A	1	1101		1	1117	A	1	1133	A	1	1149	A	1	1293		1	1309	A	1	1325	A	1	1341	A	1
O	B15	270	M	1	286	A	1	302	A	1	318	A	1	(334)			1038		1	1054	A	1	1070	A	1	1086	A	1	1102		1	1118	A	1	1134	A	1	1150	A	1	1294		1	1310	A	1	1326	A	1	1342	A	1
P	B16	271	A	1	287	A	1	303	A	1	319	A	1	(335)			1039		1	1055	A	1	1071	A	1	1087	A	1	1103		1	1119	A	1	1135	A	1	1151	A	1	1295		1	1311	A	1	1327	A	1	1343	A	1

Note: Each scan point is given a "type" designation, maintenance (M) and attendant (A).
The column "OW" denotes the OM flip-flop state. 0 denotes 2-way; 1 denotes one-way.

resets the scanner circuit. When the scanner is reset, the regular scanning operation is resumed.

3.89 Fig. 29 shows the basic control applied to the outgoing message control circuit. When no message is being sent (MSGN), a clear word 32 (CL32) operation is performed at each time slot B0. When a message is sent (MSG), the data bit rate (CT4) is established by the data receiver timing signal (DM0 and DM1), counted down by 32, and the go-ahead (GO) signal is initiated (GH) by the incoming message control circuit. The read-circulate message (RCM) control and outgoing message data control circuits produce the serial data bits (DTA0 and DTA1) for transmission to the control unit via one of the data transmitters.

3.90 The data receiver timing circuit provides a 20.5880-kc crystal oscillator which produces a rectangular output waveform. Binary counter

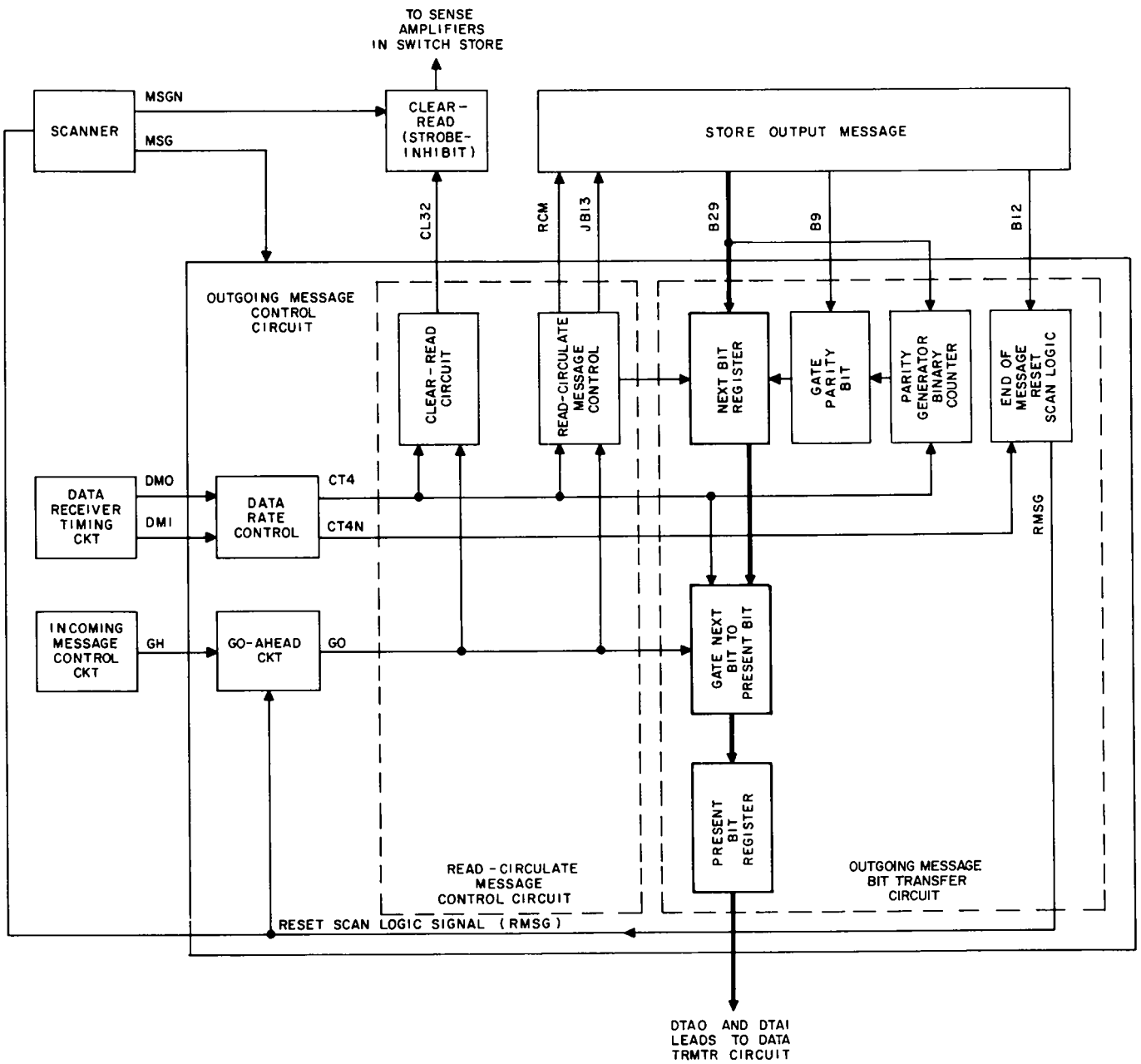


Fig. 29—Outgoing Message Timing and Control

stages produce the outgoing message rate at 643.4 bps by counting down the 20.5880 kc by a total of 32. The counter output CT4 is a square wave with a period of 1.56 msec. The CT4 output signals control the write-shift message, gate next-bit-to-present-bit register, gate parity-bit-to-next-bit register, read-circulate message signal generation, and reset scan logic circuits.

3.91 The outgoing message control circuit operation is enabled when the GO flip-flop is set and if CT4 is in the correct state. The GO flip-flop is set after the last outgoing message by a one in bit 3 of the incoming message. Bit 3 of the incoming message is read into B7 of store word zero. The pair of start bits 1 and 2 are similarly read into B9 and B8 of store word zero. Thus, the GH signal is generated during time slot S32 when B7, B8, and B9 of the output register are all ones.

3.92 The GH signal, when detected in the incoming message returned from the control unit, produces the GO signal enabling the next required outgoing message to be assembled and transmitted. However, if a GO bit is not received via the incoming message control circuit within three-fourths of a second after a message is sent from the switch unit to the control unit, the GO signal will be generated by a time-out circuit. The 3/4-second timing is provided by three wait flip-flops and the 120-ipm signal (G120) from the attendant circuit. In the following paragraphs, assume that by one or the other of these mechanisms, the GO flip-flop is set when the MSG lead goes to ground.

3.93 Since the MSG lead and the GO lead are operated all through the outgoing message processing, the rate of bit shift, transfer, and transmission is basically governed by the logic level on the CT4 lead. When the CT4 lead switches to battery level, the read-circulate message (RCM) signal will be produced at the next time slot B0, and the store word content of B28 will be transferred via output register bit 29 to the next bit (NB) register. The read-circulate operation is reset and inhibited from further operation until after the CT4 lead returns to ground (one-half message bit cycle later) when the next bit is transferred to the present bit (PB) register. Thus, the transmission message bits in word 32 are shifted a bit at a time under control of the 1.56-msec CT4 interval.

3.94 The content of bit 29 (Fig. 29) is transferred to the next bit register. One-half message bit cycle after the RCM flip-flop was set (B29 to NB), the CT4 lead switches from battery to ground level, enabling the contents of the NB register to be transferred to the present bit (PB) register. The state of the PB register is transmitted to the data transmitter circuits No. 0 and No. 1.

3.95 As each message bit is gated from the store via B29 of the output register, if it is a 1, the parity generator (PG) binary counter is advanced in addition to loading the NB register. The parity generator is provided to keep a record of the number of ones in a message for the purpose of generating a parity bit to add on to the message. After the 13 message bits shown in Fig. 30 have been read from B29 and transferred to PB, the start (ST) bit appears at B9. When the shift counter bit is detected at B9 during time slot B0, a gate parity bit (GPB) signal is produced which prevents the further reading of B29 into NB and transfers the parity bit state from the PG binary counter to the NB register.

3.96 When the ST bit is further shifted and is detected at B12 at time slot B0, the reset scan logic (RSL) circuit produces the SMSG signal. The SMSG signal resets the PG, NB, PB, GO, and scan logic circuits (MSG).

3.97 Fig. 30 is the bit arrangement of store word 32 at the beginning of message transmission. Fig. 31A is the bit arrangement of word 32 after the 13 message bits (16 through 28) are read-circulated a bit at a time when the ST bit appears at bit 9 to produce the GPB signal. Fig. 31B is the bit arrangement of word 32 when the ST bit appears at bit 12 to produce the RSL operation. All three bit arrangement figures show the single one(s) jammed a bit at a time into bit 13 (JB13) behind the message bits. The JB13 signal (Fig. 29), which is concurrent with the RCM operation, provides a second source of bits to ensure that a reset scan logic signal will be produced even if a transient condition destroys the message content from the output register. An empty output register with the MSG flip-flop set in the scanner circuit might otherwise cause a read-circulate runaway by the outgoing message control circuit.

B. Incoming Message Processing

3.98 Incoming digital data messages from the control unit are converted in the data receiver to dc logic signals suitable for processing by the

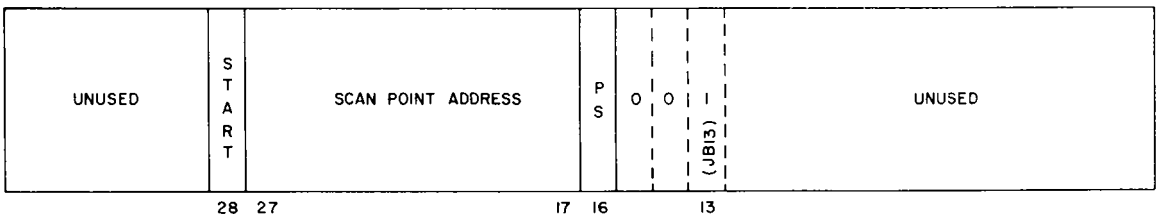
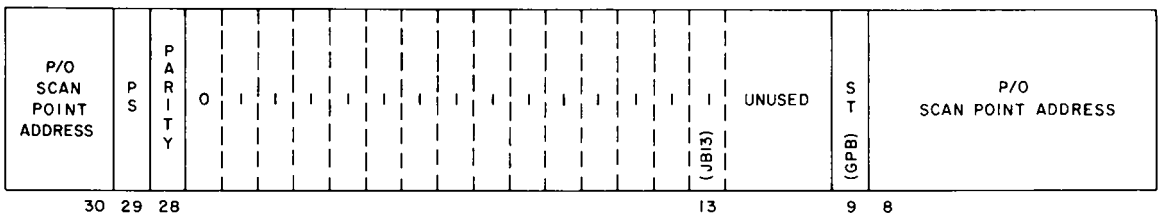
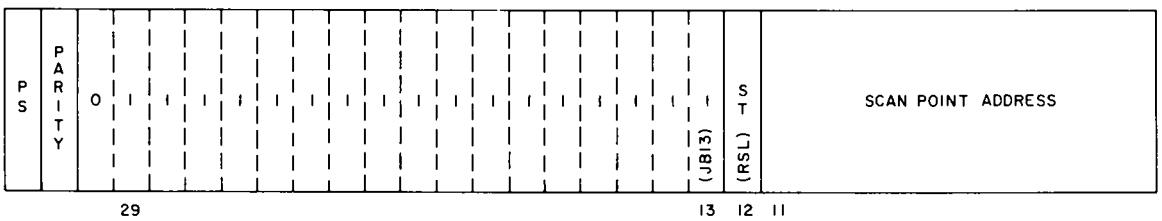


Fig. 30— Word 32—Beginning Message Transmission



A. After 13 Message Bits (Gate Parity Bit)



B. Reset Scan Logic

Fig. 31— Word 32

incoming message control circuit. The logic signals from the data receiver are sent to the switch controls at a 735.3-bps rate.

3.99 After a message start code is detected, time slot B32 is used for incoming message loading. Each message bit, as it is received, is jammed into the first stage (OR1) of the output register during the next time slot B32. When each new message bit is received, a read-shift process is employed to cause every bit contained in the store word to be shifted, each to the next higher bit in the output register, and written back into word zero. Word zero is normally read at each occurrence of time slot B32, but because the length of the message exceeds the number of bits in a single word of the store, two words are required. Therefore, word one is also employed to load certain parts of the message. The incoming message control circuit provides a read word circuit. The read word (RW) flip-flop governs which of the two words is to be read during each time slot B32. The X0 lead from the store address translator is always active during time slot B32. When it is necessary to read word zero during time slot B32, the Y0 lead is activated by the RW flip-flop in the reset state. When the RW flip-flop is set, the Y1 lead is active during time slot B32 to read word one. The switch control data time slot decoder circuit provides numbered time slot logic sequence control while the store address translator provides store word access.

3.100 Each message received from the control unit consists of a sequence of 47 binary digits, or bits. There are basically two types of

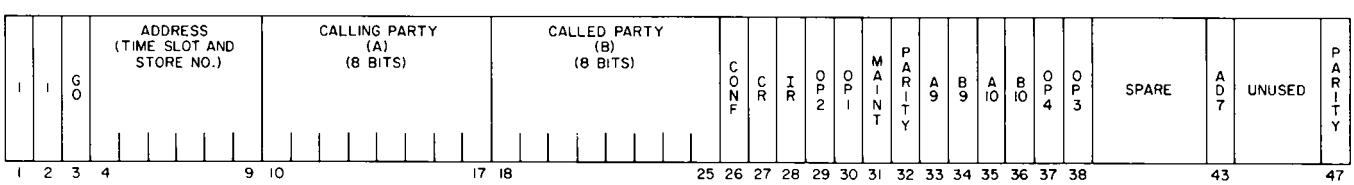
incoming messages. The incoming transmission message (TM) format is shown in Fig. 32A. Fig. 32B is the format for the incoming attendant lamp message (LM). The message decoding circuit determines from the address portion (bits 4 through 9) the type message being received and selects the appropriate routine required to process message bits 10 through 47. If bit 4 is a one and bits 5 through 9 are all zeros, the message contains information pertaining to the state of lamps on the attendant console. When bits 4 and 5 are both ones and bits 6 through 9 are zeros, a third type message of a special kind to initiate maintenance message controlled transfer in the maintenance circuits is indicated. The maintenance message information shown in Fig. 32C is not used for establishing talking connections but is used by the maintenance and attendant circuit; it is processed by the same method used for transmission messages.

3.101 Half of the transmission message addresses are allocated for TDC0 and half for TDC1. Since both time division controls receive each message simultaneously, when one control is transferring the contents of word zero to a talking time slot, the other control must be discarding the message. The state of message bit 5 determines which time division control accepts or discards the message.

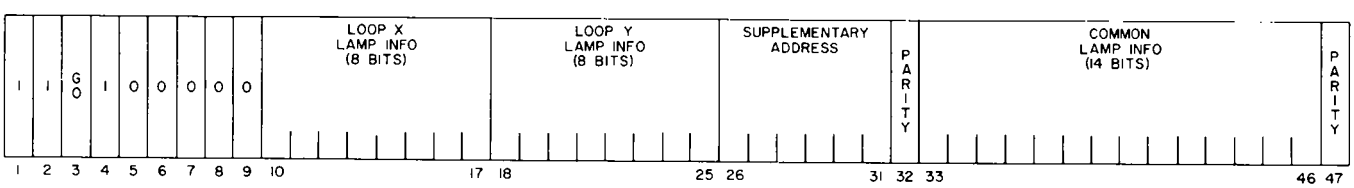
Read Word Sequence

3.102 Fig. 33 is the read word sequence for incoming messages. The read word sequence is shown for the transmission message, the attendant lamp message, and the maintenance message in Fig. 33A, 33B, and 33C, respectively. The maintenance message is a special kind of transmission message for maintenance purposes. All three messages are handled by the same operational pattern through the point where the ninth message bit is received.

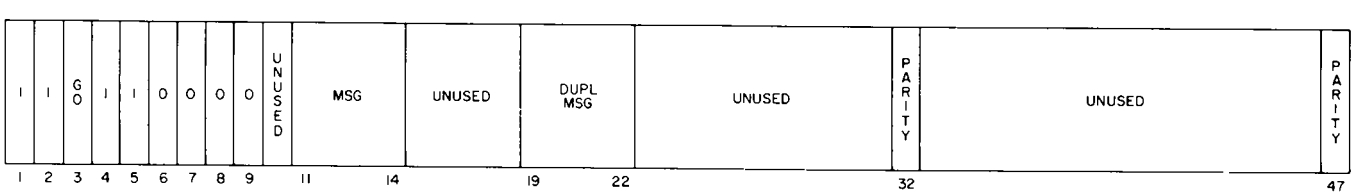
3.103 Word zero was cleared at the end of the preceding message. Subsequent received bits are loaded into a buffer circuit. If a zero is received after a single 1, a reset signal is produced which clears the single 1 out of the buffer. The process is repeated in the buffer until a consecutive pair of 1s (message bits 1 and 2) is received, indicating the start of a message. When the message start is detected, a 1 is jammed into bit 1 (ST) of ***word zero.*** Subsequent message bits (3



A. Incoming Transmission Message Format



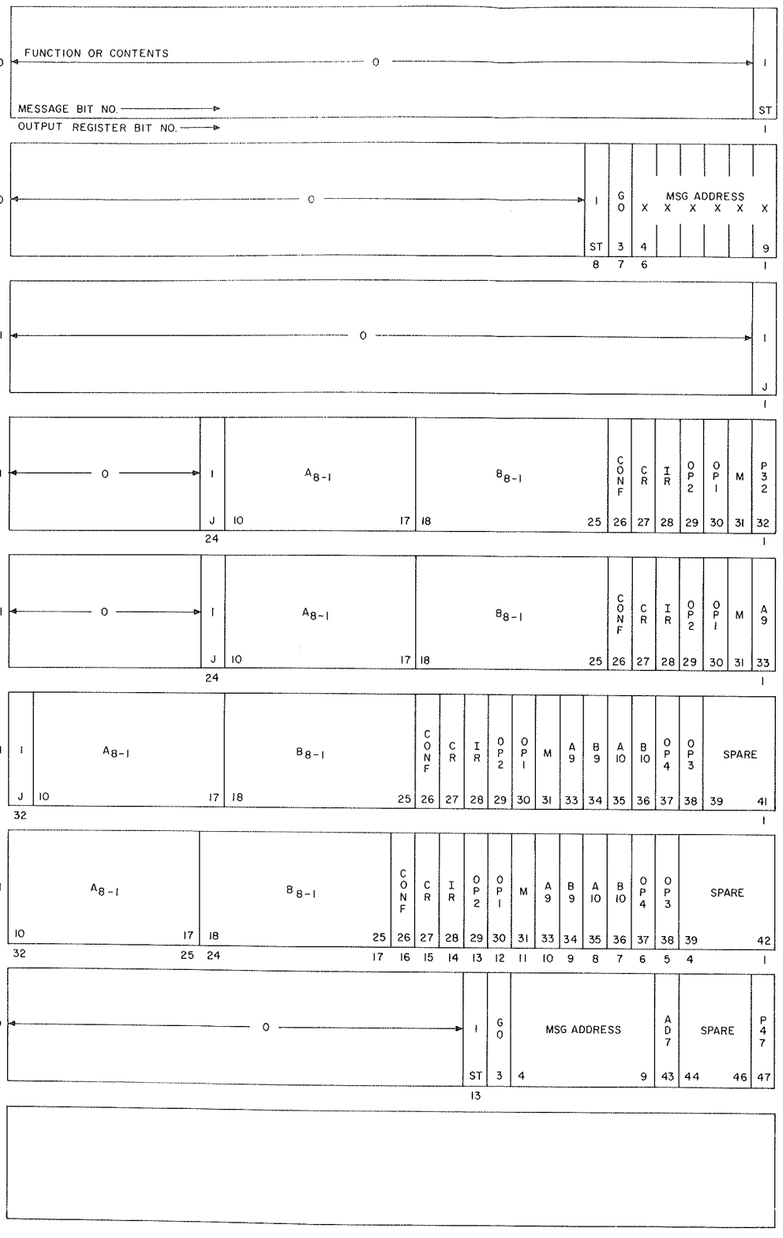
B. Incoming Attendant Lamp Message Format



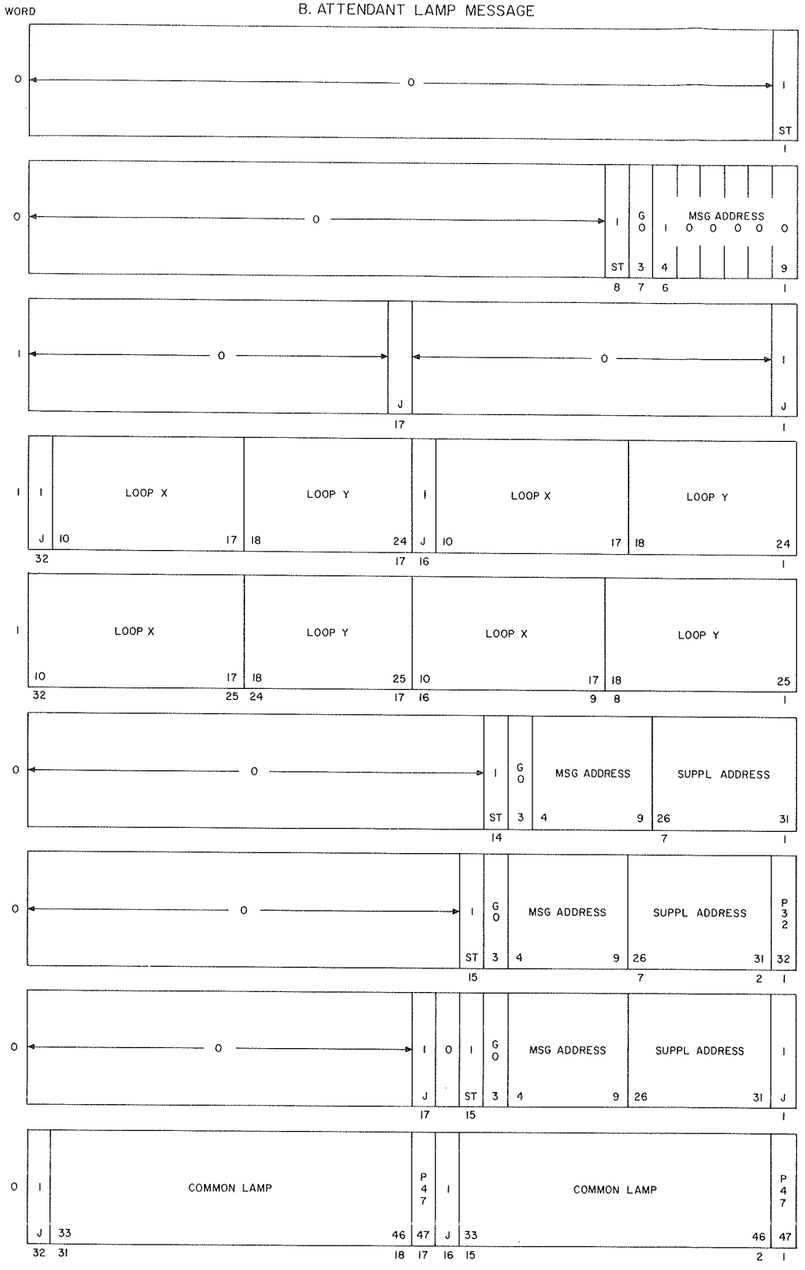
C. Incoming Maintenance Message Format

Fig. 32

A. TRANSMISSION MESSAGE



B. ATTENDANT LAMP MESSAGE



C. MAINTENANCE MESSAGE

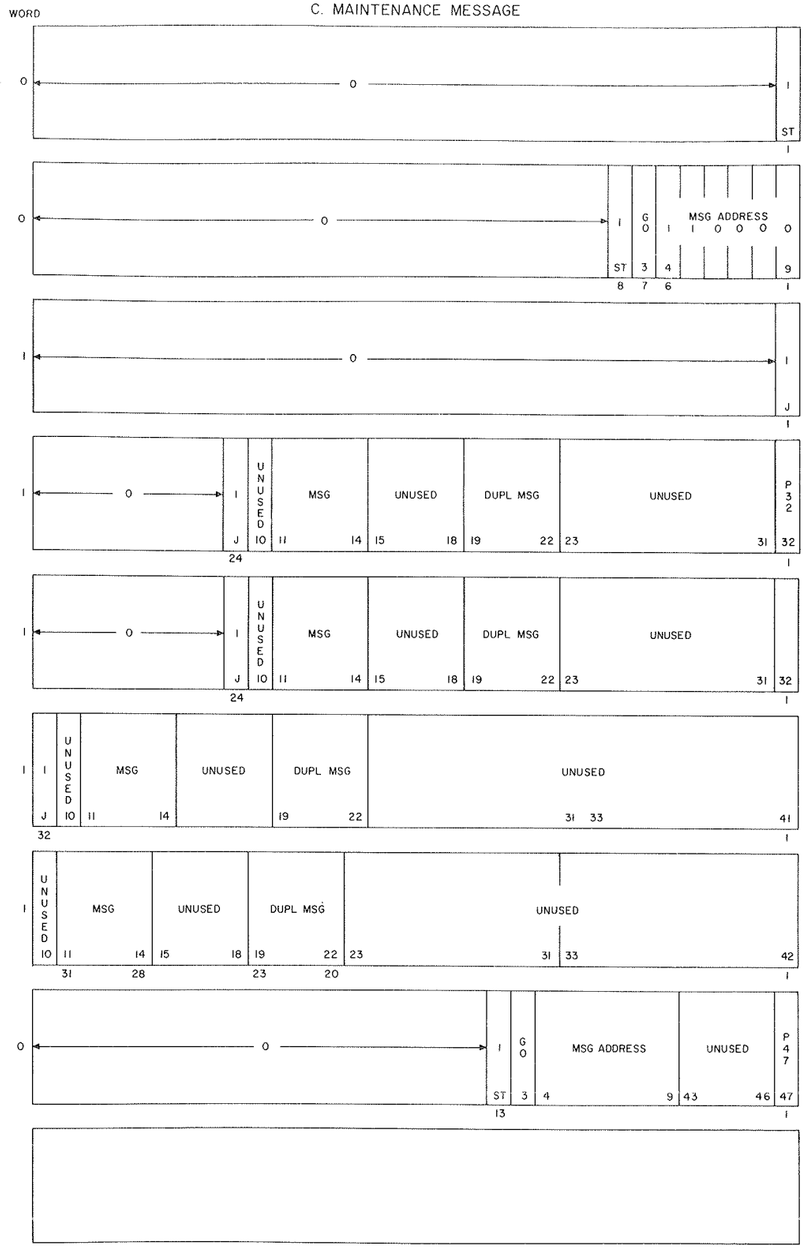
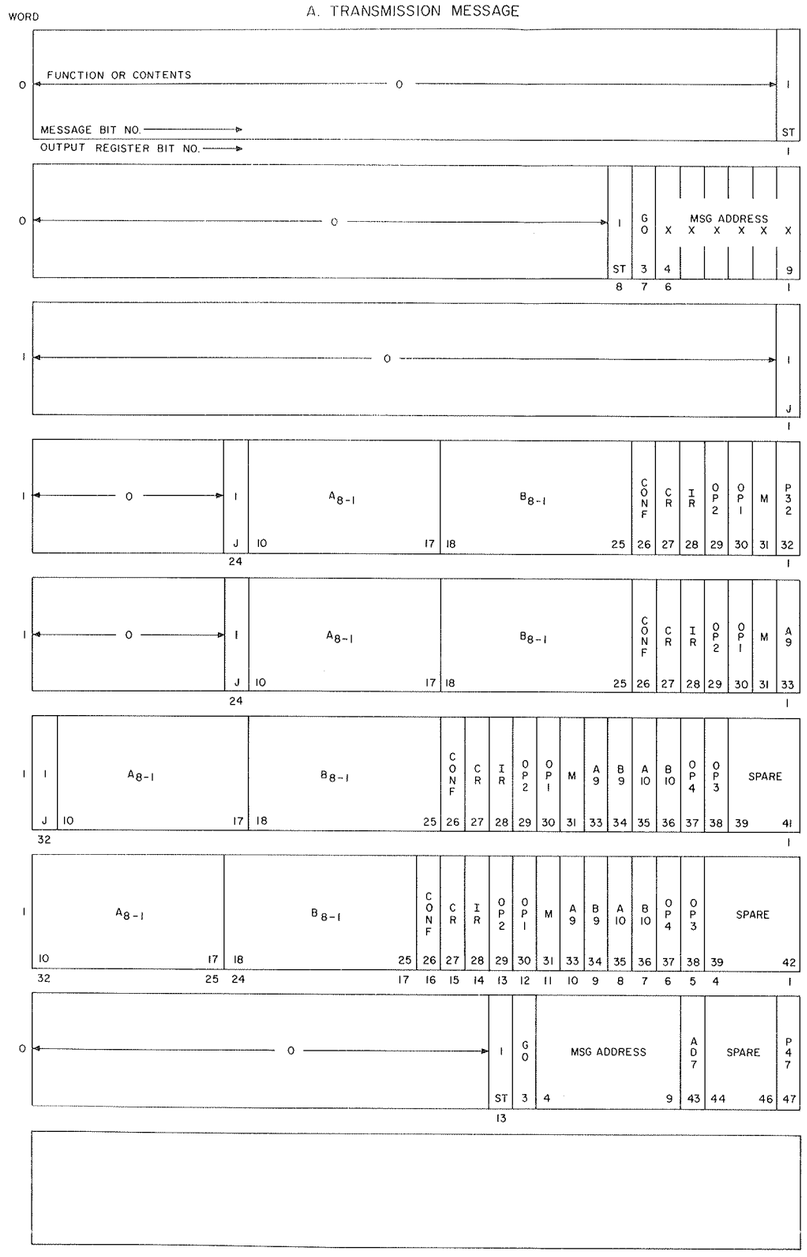
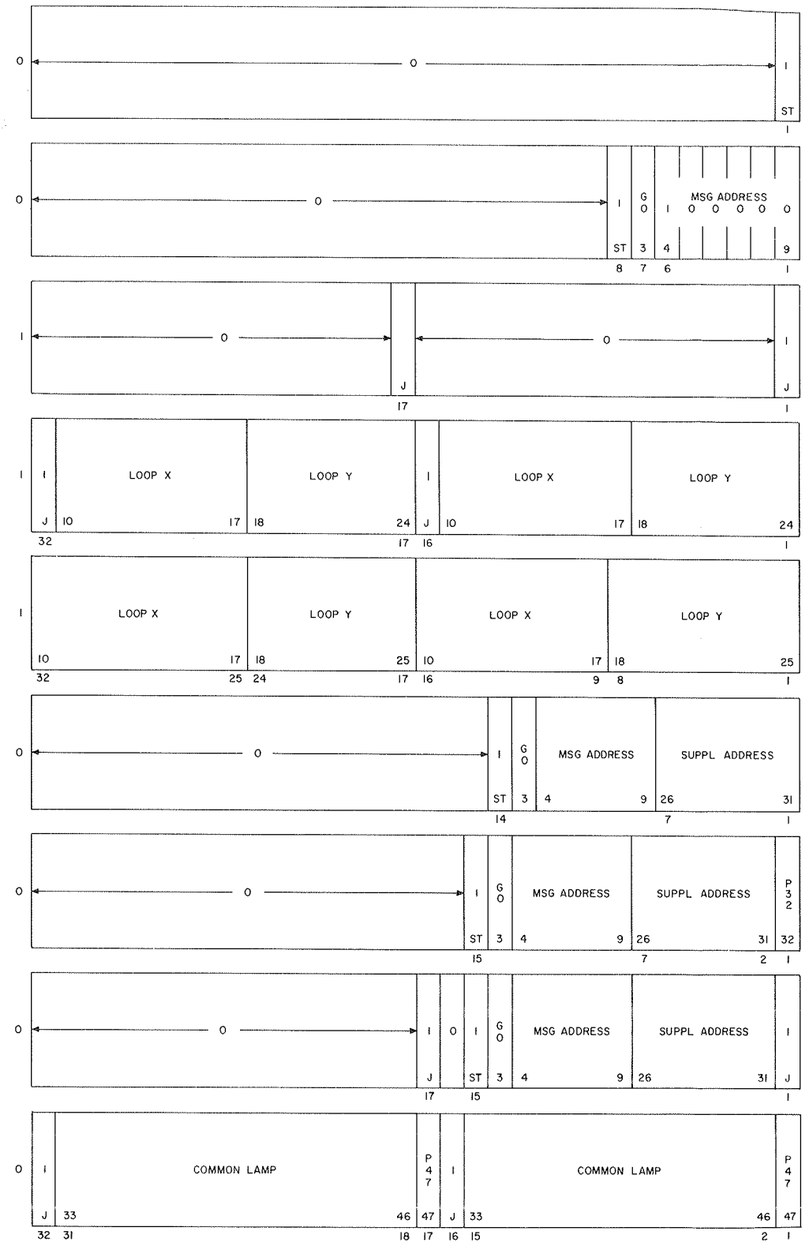


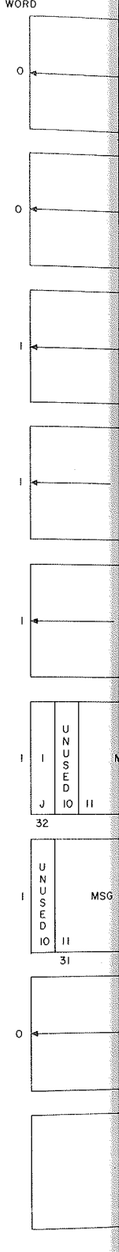
Fig. 33—Incoming Message—Read Word Sequence

A. TRANSMISSION MESSAGE



B. ATTENDANT LAMP MESSAGE





through 9) are loaded into store word zero via the first stage of the output register as each bit is received. When the start bit (ST) in bit 8 of word zero is read at time slot B32, the go-ahead bit (message bit 3) is sent to the outgoing message control, and the message address is stored in the message address register at time slot AX to provide control for relocation of the message after all bits have been received. The binary address number is decoded, and if the content is other than that indicated for a lamp or maintenance message, the transmission message (TM) type operation is selected.

Transmission Message

3.104 Fig. 33A is the read word sequence for the transmission-type message. When the message address is stored in the message address register, the read word circuit is switched to read ***word one.*** Word one is first read with sense amplifier inhibited to perform a clear-read on word one (CLR1). A single one is also jammed into bit 1 of word one. The next 23 message bits (10 through 32) are shifted into word one. The single one (J), now located in bit 24 of word one, causes a parity check and a read-shift inhibit (RSI) signal. A parity check is made and registered as a parity success or parity failure. If a parity failure is registered, the message will be discarded after the remaining message bits have been received. The RSI signal produces a read-normal operation, causing the next message bit (bit 33) to be loaded over parity bit 32 into bit 1 of word 1.

3.105 Whether the parity failure is registered or not, the remaining message bits must be received to complete the message. Assume that the parity check is successful.

3.106 Message bit 33, when loaded into OR1, replaces bit 32 which was not shifted. After the next eight message bits have been shifted into word 1, the single one (J) is located in bit 32 and one more read-shift word one operation is permitted for reception of the next message bit 42.

3.107 The read word circuit is switched back to read ***word zero*** to load the remaining 5 message bits into word zero of the store. The start bit now appears at store bit location 13, causing a second parity check to be performed. If the number of ones in the message is odd, another parity success is registered and a message relocate (MR) signal is generated.

3.108 The read word circuit is switched to read ***word one.*** Word one is read into the output register at the next time slot B32. At time slot AX, the X and Y gating circuits transfer the message address (containing the talking time slot number) from the message address register to the store address translator. The store readout is inhibited to retain the contents of word one in the output register. The contents of word one are written into the talking time slot storage word designated in the message address. Since time slot AX occurs during the A time slot counter interval immediately after time slot B32, the normal memory word select function of that A time slot is preempted by the message address register content. Due to precession of the A counter time slots with respect to the B counter time slots, the preemption may cause the exclusion of any one of the time slots A0 through A31. Thus, the normal function of the preempted A time slot, whether it be for a talking connection or attendant lamp memory readout, is obliterated for this one occurrence during message relocation.

3.109 After the message is relocated, the system is restored during time slot B1 to the correct state for the reception of a new message. The contents of ***word zero*** are destroyed by a clear-read word zero (CLR0) operation during time slot B32. With all zeros in word zero, the incoming message reset sequence is completed by the next time slot B0; the system is now ready to receive a new message.

Lamp Message

3.110 Fig. 33B is the lamp-type message. The first nine message bits are loaded in ***word zero*** in the same manner as the transmission message, the binary message address number is decoded, and since the contents indicate a lamp message, the lamp message (LM) type operation is selected.

3.111 The read word circuit is switched to read ***word one*** during each time slot B32. Word one is cleared, a single one (J) is jammed into bits 1 and 17 of word one, and the next 15 message bits 10 through 24 are shifted into word one via bits 1 and 17, simultaneously. The single one jammed into bit 17 now appears at bit 32 of word one. Message bit 25 is loaded into bits 1 and 17. Message bits 10 through 25 are employed to replace one half of a loop lamp memory word (bits 1

through 16 or 17 through 32) during the message relocation process.

3.112 The read word circuit is switched back to read ***word zero.*** Message bits 26 through 31 are shifted into bits 7 through 1, respectively, of word zero. The message start bit (ST) now appears in output register bit 14. The supplementary message address in output register bits 1 through 7 is transferred to message address register stages MA6 through MA1, respectively. Message bit 32, a parity bit, is then loaded into bit 1 of word zero, and the start bit is detected in output register bit 15 to produce a first parity check in the same manner as described for transmission messages. The parity success or parity failure condition is registered, and in conjunction with a read-shift inhibit signal, a single one is jammed into bits 1 and 17, simultaneously. The read-shift inhibit caused bit 1 to be jammed over the message parity bit 32. Word zero is thereby initialized to receive the common lamp information.

3.113 The last 15 bits of the incoming message contain common lamp information and the second parity bit. The bits are loaded simultaneously into bits 1 and 17 of word zero. The single one (J) jammed into bit 17 is now detected at bit 32 of the output register, causing a second parity check to be performed. If a parity failure occurred at either of the two checks, the message will be discarded. If both of the parity checks were satisfied, the message is to be relocated.

3.114 The message address relocation process is initiated during the same time slot B32 used for the parity check. Word zero is relocated (during time slot AX) to the common lamp word associated with the supplementary address; the read word circuit is then switched to read ***word one.*** Word one is similarly relocated (during the next time slot AX) to the addressed loop lamp word.

3.115 Table D shows the allocation of attendant lamp memory words 112 through 127. Bits 1 through 16 of these words are assigned to attendants 1 through 3. Bits 17 through 32 are used for attendants 4 through 6. Message bits 27 through 31 (the supplementary address), stored in the respective message address register stages MA2 through MA6, determine the method of relocation for the incoming lamp message. Message bit 27 stored in the MA2 stage indicates which of the duplicated 16 store bit half-words in word zero or one are to be relocated. If message bit 27 is 0, an RAL signal is produced which inhibits resetting output register bits 1 through 16 to preserve the desired half of word for relocation. Also, the strobe signal to sense amplifier bits 1 through 16 is inhibited to perform a clear-read operation on the same half of the stored word to be modified. Similarly, if message bit 27 is 1, an RAH signal inhibits resetting output register bits 17 through 32 and clear-reads the same half word from lamp word memory to be modified.

3.116 The remaining supplementary address message bits 28 through 31 indicate the words to which the lamp information is to be relocated. Bit 28 produces the X word select signals (X14 or X15) via the message address register, attendant counter, and store address translator circuits. Bits 29, 30, and 31 similarly produce the Y word select signals (Y0 through Y7). The two higher order bits of each common lamp word address are the same as for the associated loop lamp word address. Thus, a pair of ones are jammed into the two lowest order attendant counter stages with the states of higher order message bits 28 and 29 when the common lamp information stored in word zero is being relocated during the first iteration. All four message address bits are employed during the second data time slot iteration to relocate the loop lamp information stored in word one. The incoming message control circuit is reset during the third data time slot iteration of the message relocation process, restoring the system to the correct state for the reception of a new message in the same manner as that described for transmission messages in 3.109.

Maintenance Message

3.117 Fig. 33C is the maintenance message which is basically processed in the same manner as the transmisson message. When the binary message address is decoded, a transfer and alarm message (TAM) type operation is selected in conjunction with the transmission message-type operation selection described in 3.104. The process continues by shifting message bits 10 through 42 into word one in the same manner described for the transmission message. After the last message bit has been loaded and the parity successfully checked, word one is read at time slot B32 for transfer to the transfer and alarm circuit.

TABLE D

ATTENDANT LAMP MESSAGE RELOCATION

SUPPL. ADDRESS MSG BITS				ATND LAMP MEMORY WORD	LAMP MESSAGE RELOCATE BITS			
					17 THROUGH 32 (MSG BIT 27=1)		1 THROUGH 16 (MSG BIT 27=0)	
28	29	30	31					
0	0	0	0	112	TGB 31-40	Att. 4 ICI	TGB 1-10	Att. 1 ICI
0	0	0	1	113	TGB 41-50	Att. 5 ICI	TGB 11-20	Att. 2 ICI
0	0	1	0	114	TGB 51-60	Att. 6 ICI	TGB 21-30	Att. 3 ICI
0	0	1	1	115	Spare			
0	1	0	0	116	Loops 1 & 4	Att. 4	Loops 1 & 4	Att. 1
0	1	0	1	117	Loops 2 & 5		Loops 2 & 5	
0	1	1	0	118	Loops 3 & 6		Loops 3 & 6	
0	1	1	1	119	Common Lamp		Common Lamp	
1	0	0	0	120	Loops 1 & 4	Att. 5	Loops 1 & 4	Att. 2
1	0	0	1	121	Loops 2 & 5		Loops 2 & 5	
1	0	1	0	122	Loops 3 & 6		Loops 3 & 6	
1	0	1	1	123	Common Lamp		Common Lamp	
1	1	0	0	124	Loops 1 & 4	Att. 6	Loops 1 & 4	Att. 3
1	1	0	1	125	Loops 2 & 5		Loops 2 & 5	
1	1	1	0	126	Loops 3 & 6		Loops 3 & 6	
1	1	1	1	127	Common Lamp		Common Lamp	

3.118 The read word circuit is switched to read ***word one.*** Word one is read into the output register at the next time slot B32. A signal is produced which enables the transfer and alarm circuit to receive the word one message contents read into the output register bits 20 through 23 and 28 through 31. The system is restored to the correct state for the reception of a new message in the same manner as that described in 3.109.

COMMON EQUIPMENT

3.119 The primary purpose of the store output translator is to produce talk-connection-select signals for establishing connections between subscriber line and/or trunk circuits. Other types of connection are provided to ***common equipment*** via time division switches in the associated intergroup switch circuits and the tone and digit trunk group circuits. The common equipment discussed in the following paragraphs consists of the conference capacitor and ringing circuits of the intergroup switch circuit. The tone, attendant line, and digit trunk circuits are associated with the tone bus and digit trunk switches.

A. Conference Circuits (Call Transfer and Add-On)

3.120 Information is provided in one time slot word (32 bits) for the connection of only two subscribers to the intergroup bus during the one time slot interval. Conference calls may be established between three subscribers by the use of a pair of time slots effectively bridged together by conference capacitor circuitry. The presence of the conference bit (B16) in both of the time slot words (of a pair) will close the conference capacitor to intergroup bus in both time slots in which the three subscribers are located. Voice energies are mixed and transmitted from one subscriber to any other, either directly or indirectly. Direct transmission is accomplished between two subscribers in the same time slot. Indirect transmission is accomplished from one subscriber, via the conference

capacitor, to another subscriber in the other time slot.

3.121 Each intergroup bus circuit provides 12 conference capacitors in two circuits of six each. Six of the capacitors are associated with the A time slot counter and six with the B time slot counter. The system program control (in the control unit) assigns the conferees to one of the available sets of paired conference time slots. A conference capacitor is associated with each conference time slot pair. Conference calls are restricted to the first 12 talking time slots (2-13) for each time slot counter (A and B). The arrangement of time slot pairs is shown in Table E.

TABLE E

ARRANGEMENT OF TIME SLOT PAIRS FOR CONFERENCE CALLS

CONFERENCE PAIR	BINARY TIME SLOT COUNT				DECIMAL TIME SLOT NUMBER
	PAIRS			UNITS	
	*C3	*C2	*C1	*C0	
*1	0	0	1	0	2
	0	0	1	1	3
*2	0	1	0	0	4
	0	1	0	1	5
*3	0	1	1	0	6
	0	1	1	1	7
*4	1	0	0	0	8
	1	0	0	1	9
*5	1	0	1	0	10
	1	0	1	1	11
*6	1	1	0	0	12
	1	1	0	1	13

* Denotes A or B time slot conference.

3.122 The translation of time slot pairs, which causes the associated conference capacitor to be switched onto the intergroup bus, is shown in Fig. 34. Since both the A and B conference circuits are identical, only one is shown. The units count (AC0 or BC0) of the time slot counter is not employed in the translation of time slot pairs. Since *C1, *C2, and *C3 outputs are applied to gates in the group pretranslator, the twos digit *C1 is the least significant bit of the pair count number. The asterisk (*) denotes the associated talking time slot A or B. The conference bit (B16) must be present in the output register to enable gating the 3-bit pair count. The state of the three bits is temporarily stored in the time slot pair register. The three bits from the time slot pair register are connected to the conference capacitor circuits for translation and selection in a binary logic manner.

3.123 Translation of the 3-bit number occurs in the AND gate circuit of the applicable conference capacitor switch circuit. When the AND gate logic requirements are satisfied, the applicable capacitor circuit is enabled for operation when strobed by the positive CC* pulse (about 200 nsec later). A connection is established between the conference circuit storage capacitor and the intergroup bus (IB) for the 800 nsec resonant transfer interval of each time slot in the assigned pair.

B. Ringing Circuits

3.124 The ring-ringback logic produces signals which are applied to the talking bus when an appropriate combination of ring bits is contained in the control unit to switch unit message. The bits which control the ring-ringback operation are the conference (B16), continuous, immediate for 1-second ring (B15), interrupted ring (B14), and attendant present (B5, B6, B12, or B13).

3.125 The ringing signal rate is 1 second on (ring interval) and 3 seconds off (silent interval). The ring/silent intervals are staggered on a time slot basis to provide 4-phase ringing. The four phases of ringing interval are assigned to time slot intervals in accordance with the state of the least significant bit in each time slot counter.

3.126 The ringing circuit is designed for the following functions:

(1) Generates signals which activate the ring (DC RING) and ringback (RBH or RBL) switches in the intergroup switch circuit at the assigned ring and silent intervals

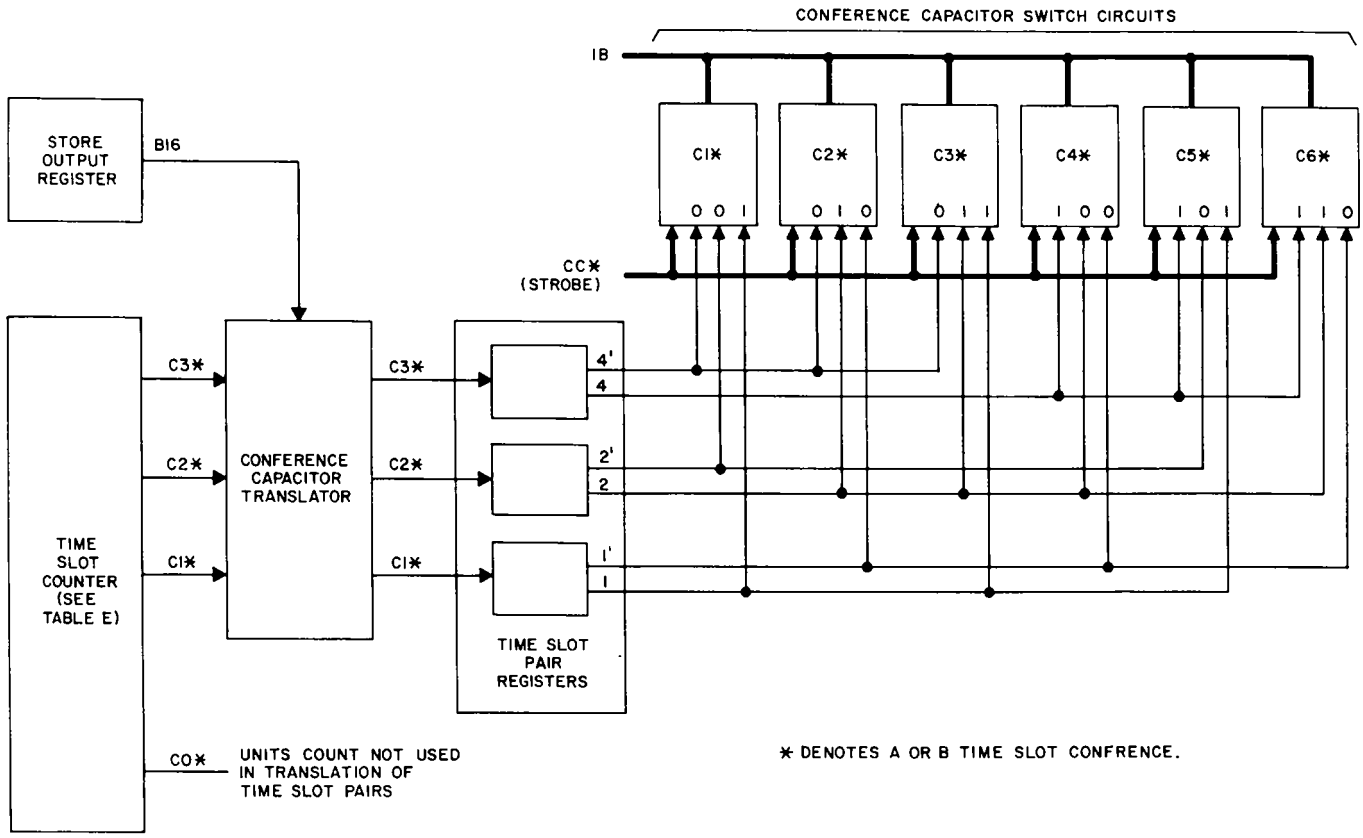


Fig. 34—Conference Call Circuit—Time Slot Pair Translation

(2) Inhibits translation of the calling party (A) number when the ring signal is on the bus

(3) Inhibits translation of the called party (B) number when the ringback signal is on the bus

(4) Inhibits translation of both parties (A and B) during the silent interval

(5) Activates a special ring-ringback switch when the calling party is a trunk

(6) Overrides inhibiting either party during the silent interval when an attendant is part of the call or when the call is a conference type.

3.127 The time slot counter, attendant circuit, output register, calling translator, and special function translator circuits produce the input signals to the ring-ringback logic circuit. The intergroup switch circuit provides and controls the dc ringing signals to the line circuits. The selected line circuit thus connects ringing current to the called subscriber line during the ringing interval while the ringing bit is in the store word until the called party answers.

3.128 The ring and ringback signals are generated on alternate store cycles for calls not involving trunks. Thus, the sampling rate provided in line circuits is approximately 6 kc for each signal, ring and ringback. Calls involving trunks use a superimposed ring-ringback signal on the bus and provide a sampling rate of approximately 12 kc.

3.129 Bits B14 and B15 control the ringing conditions. B14 provides interrupted ringing (IR) and B15 provides continuous ringing (CR). Both bits are used double rail in the ring logic circuit. The control unit governs which of the ring bits (continuous or interrupted) appears in the talking time slot store word. The simultaneous presence or absence of both ring bits is not recognized as ring commands and serves to disable the ring logic circuit. Initially, ringing is set up

by the control unit on a continuous basis (B15 and B14 are respectively one and zero). The continuous ring command overrides the silent interval conditions and allows ringing to occur immediately. After about 1 second of continuous ring, the control unit will change to the interrupted ring code (B15 and B14 are respectively zero and one).

3.130 When the third party of a conference, or a second party involved with an attendant and another party, is being rung, those already in the established connection must be able to communicate. Therefore, a signal is produced which prevents the normal inhibiting of translation during the silent interval. Bit B5, B6, B12, or B13 indicates an attendant is present, while B16 indicates that a conference is established.

3.131 ***When the calling party is a trunk circuit,*** a superimposed audible ringback and dc ring signal is applied to the talking bus. The ring and ringback signals are inhibited while the superimposed signal is being generated. When ***a trunk circuit is being called,*** the ring command is not present in the incoming message word from the control unit. The control unit outpulses the called number information to the central office, which rings the called station and supplies audible ringback tone to the calling PBX subscriber via the transmission path through the 3A switch unit.

3.132 The ring-ringback special switches provide connections for the DC RING, ringback low (RBL), and ringback high (RBH) signals to the intergroup bus. In normal ringing operation, ringback tone is received via the RBL switch. The RBH switch provides high level ringback tone plus dc during a ringing operation involving trunks. Thus, the ringback level is about 3 dB higher for trunks than for local lines.

3.133 Fig. 35 is the ringing circuit portion of the line circuit which is equipped to deliver standard 90-volt rms, 20-cps ringing via the RNG lead to the associated local subscriber telephone set. The ringing relay K1A in the ringing control circuit is operated when the DC RING signal is detected from the low-pass filter.

3.134 Normally, when the line is ***not*** being rung, the make contact 1 (early make-break type) of relay K1A is open and prevents the ringing current from being applied to the line. The capacitor C2A, which normally provides a low-impedance path to the talking signal, is connected via break contact 6 (early make-break type) of relay K1A between terminal 5 of line transformer T2A and ground. When the line is to be rung, the dc ringing control voltage arrives via the time division switch and low-pass filter to produce a charge on capacitor C2A of approximately 4 volts. This 4-volt

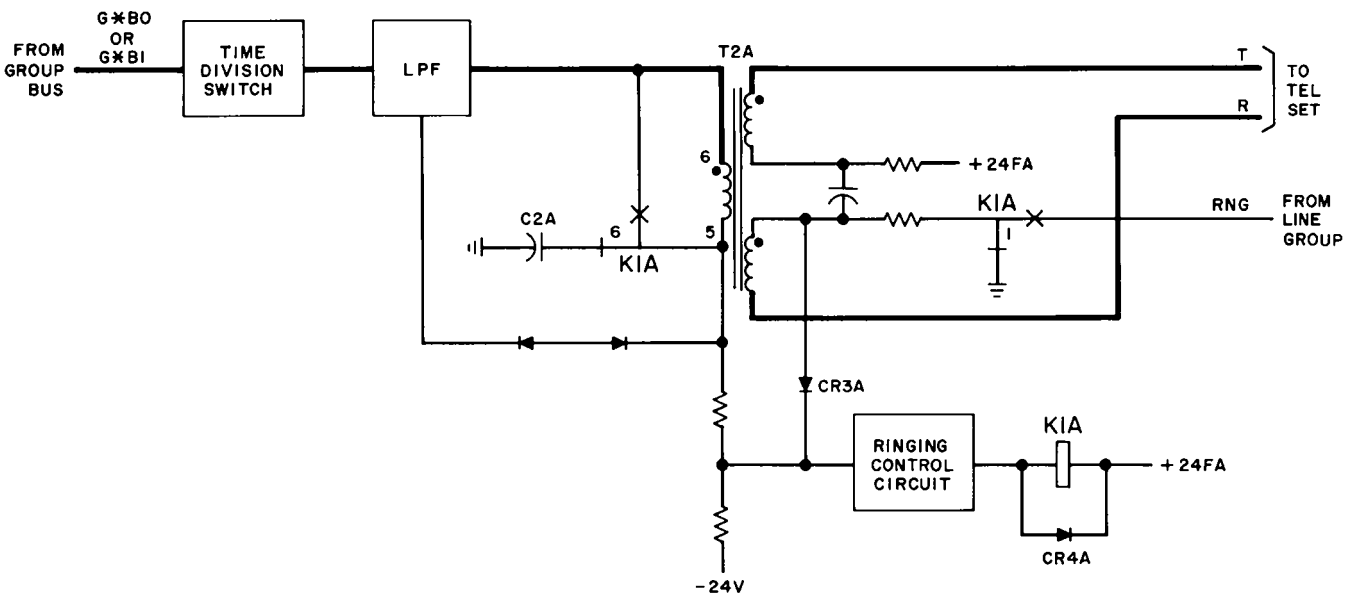


Fig. 35—Ringing Circuit in the Line Circuit Unit

signal causes relay K1A in the ringing control circuit to operate.

3.135 When relay K1A operates, the make contact 6 across winding 5, 6 of T2A closes to prevent 20-cps ringing from being coupled into the unbalanced transmission portion of the circuit. In the same operation, break contact 6 closes to remove capacitor C2A from the circuit. The break contact 1 opens to remove the ground from feed resistor and connect the 20-cycle ringing to the line. Relay K1A continues to operate as long as the dc ringing signal is received from the talking bus. Consequently, the ringing control circuit causes the ringing relay K1A to follow the dc ringing signal (continuous or interrupted) as long as the called party remains on-hook.

3.136 If the called party goes off-hook during the ringing interval, the positive voltage (talk battery through the local subset and line T and R leads) at the cathode of CR3A inhibits the ringing control circuit releasing relay K1A and illuminating the ringing operation. The line supervisory circuit, when scanned, will indicate a change from on-hook to off-hook to the scan comparison circuit which will originate an outgoing message. The control unit then sends a message with the same time slot address and word contents less the ring bits to the switch store via the incoming message control circuit of the switch unit.

C. Tone Circuits

3.137 The various tones needed for system operation are generated in the tone and digit trunk group circuit. The four tones produced in the tone generator circuit (Fig. 36) are audible ringback tone (ARB), soft tone (ST), fast busy tone (FB), and normal busy tone (BT). The tone generators are duplicated on a time division control basis for system reliability. Three tone oscillator circuits and frequency determining networks are provided.

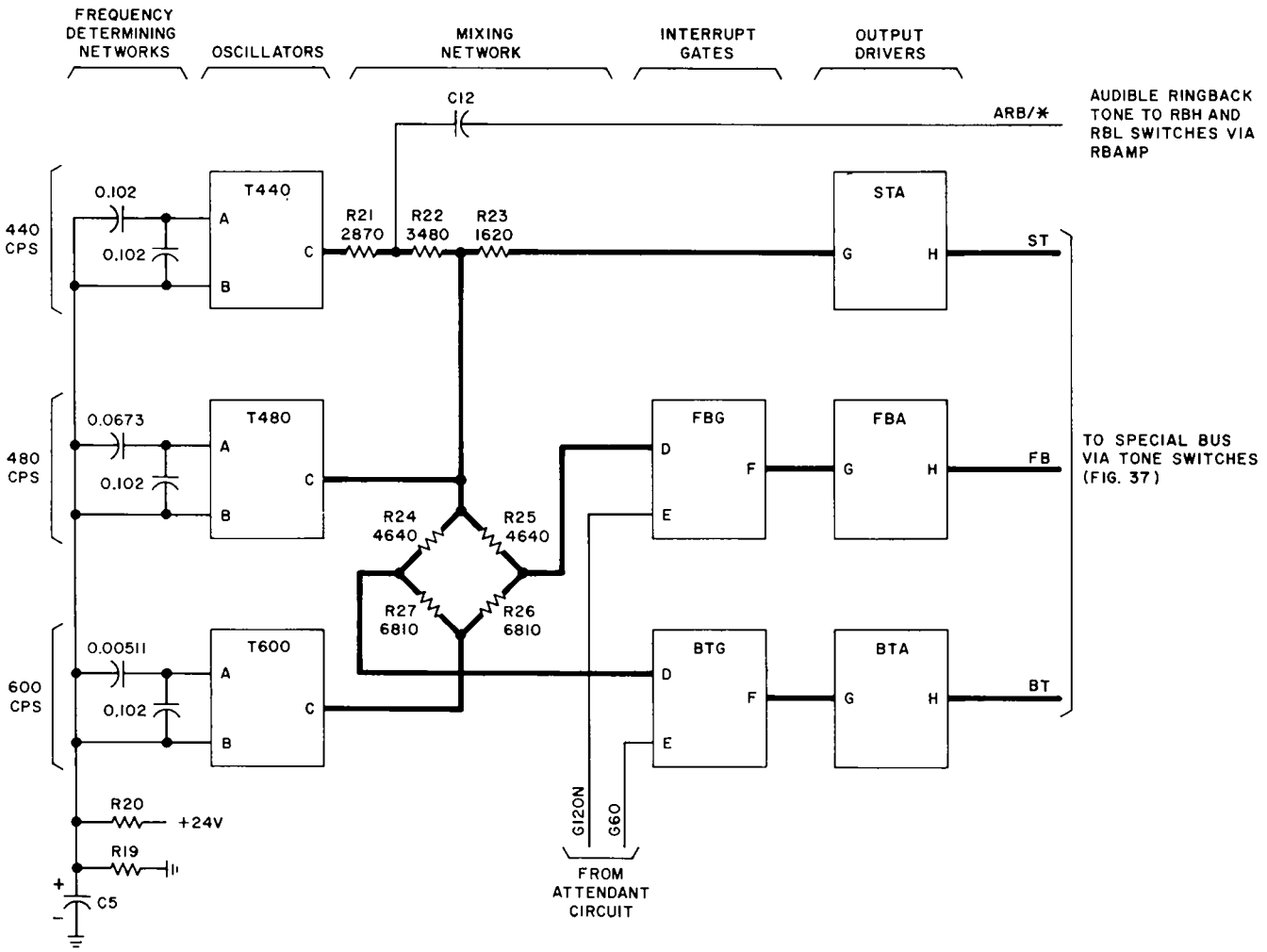
3.138 The tone oscillator circuits designated T440, T480, and T600 are identical circuits. The frequency determining networks differ with each oscillator circuit, and each network is chosen to produce the required tone. The 440-cps tone is applied uninterrupted to the assigned output driver (STA). The 480-cps output from oscillator T480 and the 600-cps output from oscillator T600 are combined in a resistive mixing network (R24 through R27) which provides the necessary mixing to produce the proper frequency combinations at a C-message weighted level. The weighted level allows each tone of a mixed pair to sound equally loud to the ear. The combined tone, when gated by the interrupt signal G60 in gate BTG, produces the busy tone which is applied to output driver BTA. When the combined tone is interrupted in gate FBG by the G120N signal, a fast busy tone is produced for application to output driver FBA.

3.139 Another part of the resistive mixing network consisting of resistors R21, R22, and R23 combine the 440-cps and 480-cps signals to produce the audible ringback tone which is capacitively coupled to the ringing circuit special switches.

3.140 The tone oscillator circuits are identical except for the external frequency determining networks. Resistors R19 and R20 and capacitor C5 comprise a low-impedance bias supply external to the tone oscillators. The bias connected via the lead designated B into each oscillator causes transistor operation in the linear region. The external capacitors C10 and C11 applied across leads A and B form a tuned circuit with the internal inductor to produce oscillations at a frequency in accordance with the value of capacitors furnished.

3.141 Fig. 37 is the tone selection circuit which activates the tone switches contained in the tone and digit trunk group circuit. A tone can be selected in place of either the calling (A) party or the called (B) party. The tones ST, FB, and BT are connected to the applicable bus ADT/0 through ADT/3 via the applicable time division tone switch. A lower tone (LOTN) switch connects a pad on the special bus to reduce the amplitude of any tone connected to the special bus in conjunction with a local line. However, when a tone is connected to a trunk circuit, the LOTN switch is not operated and the full tone amplitude appears on the special bus.

3.142 Since the closure period of time division switches must be accurately controlled to achieve proper resonant transfer of energy, a clock signal (SGCK) is provided to strobe the switch circuits. The switch, which has been enabled, operates for 800 nsec when strobed. The CLK signal is inverted to operate the special bus clamp for 430 nsec after each time division switch closure to remove any residue of energy remaining on the



NOTE:

ARB IS THE COMBINATION OF 440 CPS AND 480 CPS UNINTERRUPTED.
ST IS 440 CPS UNINTERRUPTED.
FB IS THE COMBINATION OF 480 CPS AND 600 CPS INTERRUPTED AT 120 IPM.
BT IS THE COMBINATION OF 480 CPS AND 600 CPS INTERRUPTED AT 60 IPM.

Fig. 36—Tone Generator Circuit (Transmission)

special bus after the resonant transfer interval to suppress crosstalk.

3.143 Signals for the selection of tone switch circuits are produced from the translation of certain output register codes from the tone translator portion of the group pretranslator. The binary number code which selects the soft tone is 0100111100 (group 4, vertical 7, and horizontal 4). The fast busy code is 0100111101 (group 4, vertical 7, and horizontal 5) and the normal busy tone code is 0100111110 (group 4, vertical 7, and horizontal 6). Thus, ST, FB, or BT switch operates with the selection of crosspoint.

3.144 The clock signal strobes all four switches. The soft tone switch (ST) is operated when strobed by the clock signal and enabled by the STA or STB lead. The fast busy switch (FB) operates when enabled by the FBA or FBB lead and strobed by the clock signal. The busy tone switch (BT) operates when enabled by the BTA or BTB lead and strobed by the clock signal.

3.145 The tone select (TNS) signal is produced when any tone is selected. The lower tone switch (LOTN) operates in conjunction with the TNS signal when enabled by the selection of A and B party line groups and strobed by the clock

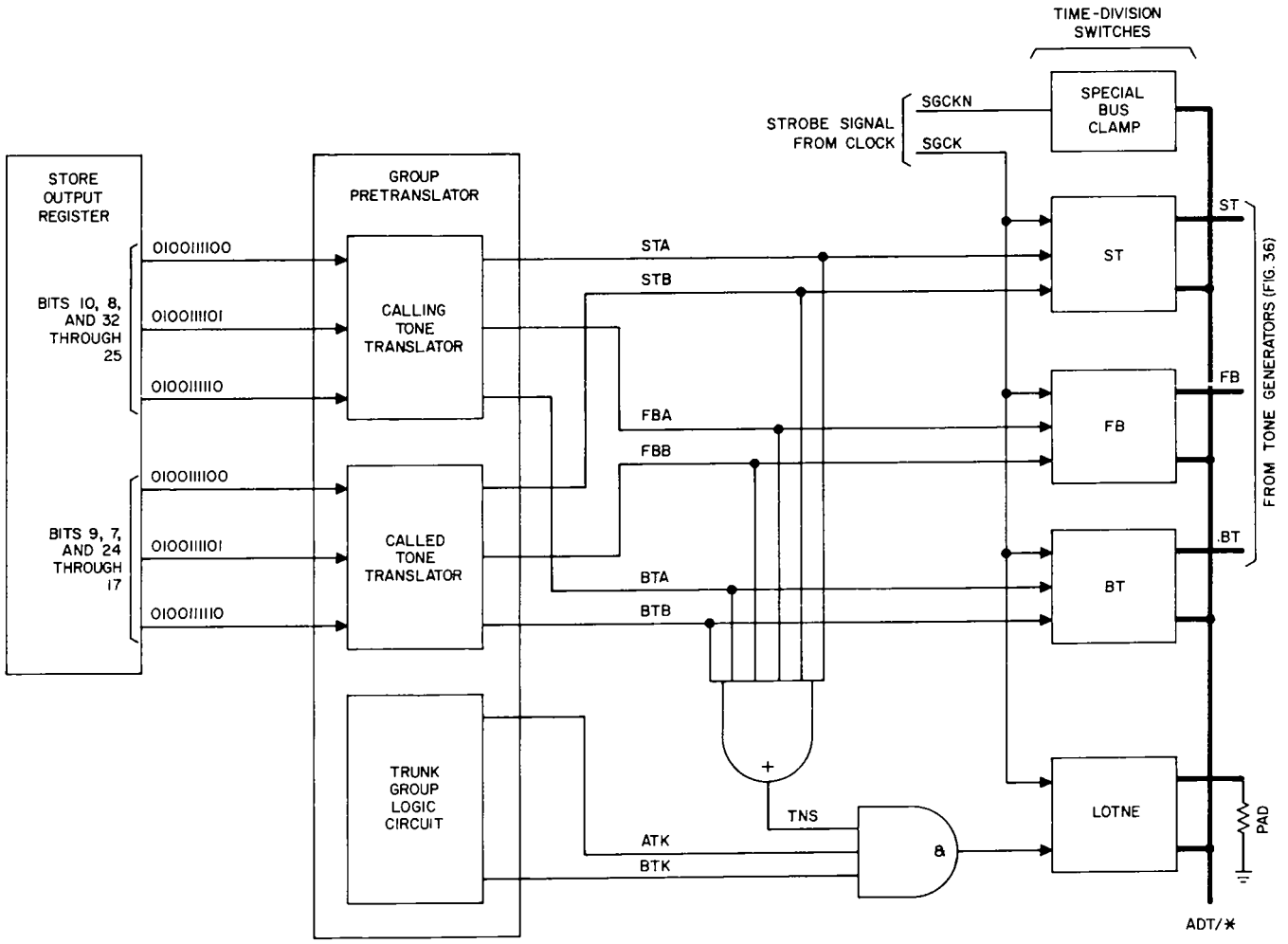


Fig. 37—Tone Selection Circuit

signal. The ATK and BTK leads are at ground level unless the calling or called party is a trunk. The tone select (TNS) signal is produced when any tone is selected. Thus, the LOTN switch is inhibited from providing a higher level tone to compensate for the additional transmission path loss when a trunk is connected to the tone circuits.

D. Attendant Line Circuit

3.146 The attendant line circuit provides a connection between the applicable attendant console and the assigned talking bus. A maximum of 12 attendant consoles may be provided. Each attendant console has access to a maximum of four attendant line circuits, each of which is assigned to the tone and digit trunk groups and buses in the switch unit.

3.147 Fig. 38 is the attendant selection and transmission circuit. The tone and digit trunk groups containing the attendant line circuits are a part of the line and trunk circuits. When 4 time division control units and 12 attendants are employed, 48 attendant line circuits are provided. Normally, the attendant tip and ring leads are not connected to any of the attendant line circuits. When an attendant is selected, the applicable numbered T and R leads are connected via relay contacts to the line transformer in the proper attendant line circuit. The line transformer couples the voice frequency energy through a low-pass filter (LPF) to the time division switch which provides connection to the associated special bus (ADT/0 through ADT/3).

3.148 The attendant line circuits are enabled by the appropriate attendant translator output

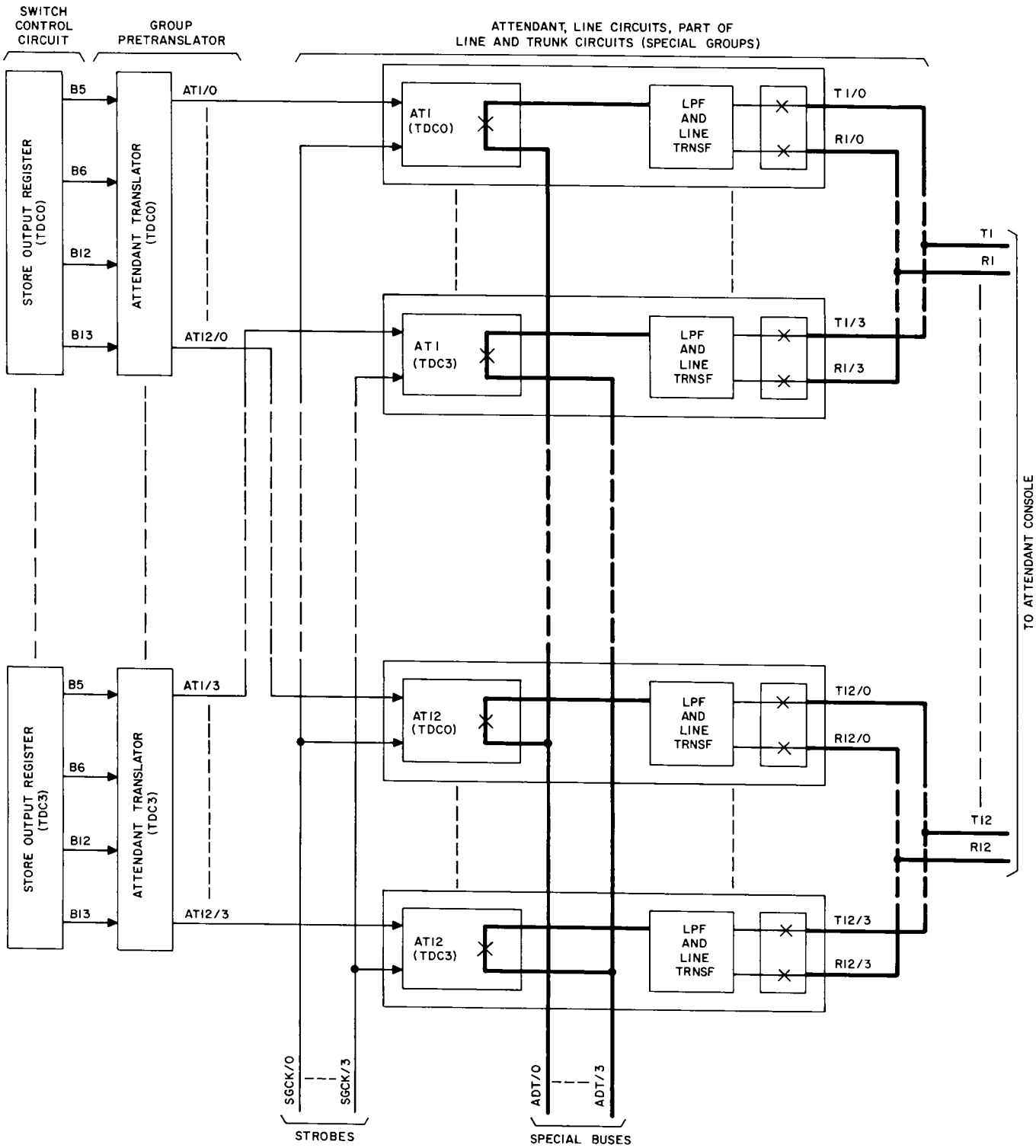


Fig. 38—Attendant Selection and Transmission Circuit

signal (AT1/* through AT12/*) and strobed by the appropriate clock signal (SGCK/*). The asterisk (*) indicates the time division control and associated tone and digit trunk group number. The attendant translator examines the state of a 4-bit combination (B6, B5, B13, and B12) of the talking time slot word contained in the store output register. Table F outlines the bit configuration for selecting each of the 12 attendants.

TABLE F

BIT CONFIGURATION FOR ATTENDANT SELECTION

B6	B5	B13	B12	ATTENDANT
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	1	4
0	1	1	0	5
0	1	1	1	6
1	0	0	1	7
1	0	1	0	8
1	0	1	1	9
1	1	0	1	10
1	1	1	0	11
1	1	1	1	12

3.149 The applicable select attendant signal (AT1 through AT12), in addition to enabling the attendant line time division switch, also operates the associated relay which connects the attendant tip and ring leads to the secondary windings. Relay control circuitry provides a time constant so that the relay will remain operated as long as the pulses on the applicable attendant select lead (AT1 through AT12) occur at the normal rate of one per store cycle.

E. Digit Trunk Circuit

3.150 The digit trunk circuit provides a bilateral voice-frequency link between the control unit and either a line circuit or a trunk circuit. The digit trunk is employed as a transmission path for dial tone and TOUCH-TONE signals. The digit trunk circuit accepts either rotary dial pulse or TOUCH-TONE signaling. The dial pulses are converted to tone bursts for transmission to the control unit. The TOUCH-TONE signals are transmitted directly (via a time division switch and low-pass filter) from the tone and digit trunk bus to the digit trunk without conversion. The digit trunk circuit also generates scan inhibiting pulses for the scanner circuit when the connected line or trunk is off-hook.

3.151 The digit trunk circuits, which are packaged two to a circuit card, connect between the assigned digit trunks and tone and digit trunk buses. Digit trunks 1 through 6, 7 through 12, 13 through 18, and 19 through 24 are assigned to tone and digit trunk buses 0, 1, 2, and 3, respectively.

3.152 Fig. 39 illustrates the transmission path and control for six digit trunk circuits. Six digit trunk circuits may be employed with each TDC. The time division switch in a given digit trunk circuit operates in accordance with the SB signal of the on-line scanner when enabled and strobed. DT1 through DT6 leads from the associated group pretranslator provide the enable signal. The special group clock signal (SGCK) strobes each digit trunk circuit.

3.153 When a time division connection is established between a calling party and a digit trunk, the signaling party is considered off-hook by the scanner because it was a change of supervisory state from on-hook to off-hook which signaled the control unit in the beginning to assign a digit trunk to the calling party. Also, dial pulse information in the form of a series of on-hook and off-hook states of the line circuit scan point may be generated and sent on the scan bus (SB) lead to the scanner and digit trunk circuit. Therefore, with the signaling party off-hook, the digit trunk supervisory circuit generates and sends scan inhibiting pulses DS*/0 (via leads designated A through F) which are combined in a multiple output detector (Fig. 40), producing the DTS signal applied to the scanner.

3.154 The DTS signal follows the digit trunk select signal occurring during the applicable talking time slot once each store cycle. When the signaling party goes on-hook, a capacitor charges through resistors. The voltage across the capacitor, divided by resistors, is applied to a circuit which provides a time-out feature to prevent the scanner circuit from recognizing hits of less than 75 msec.

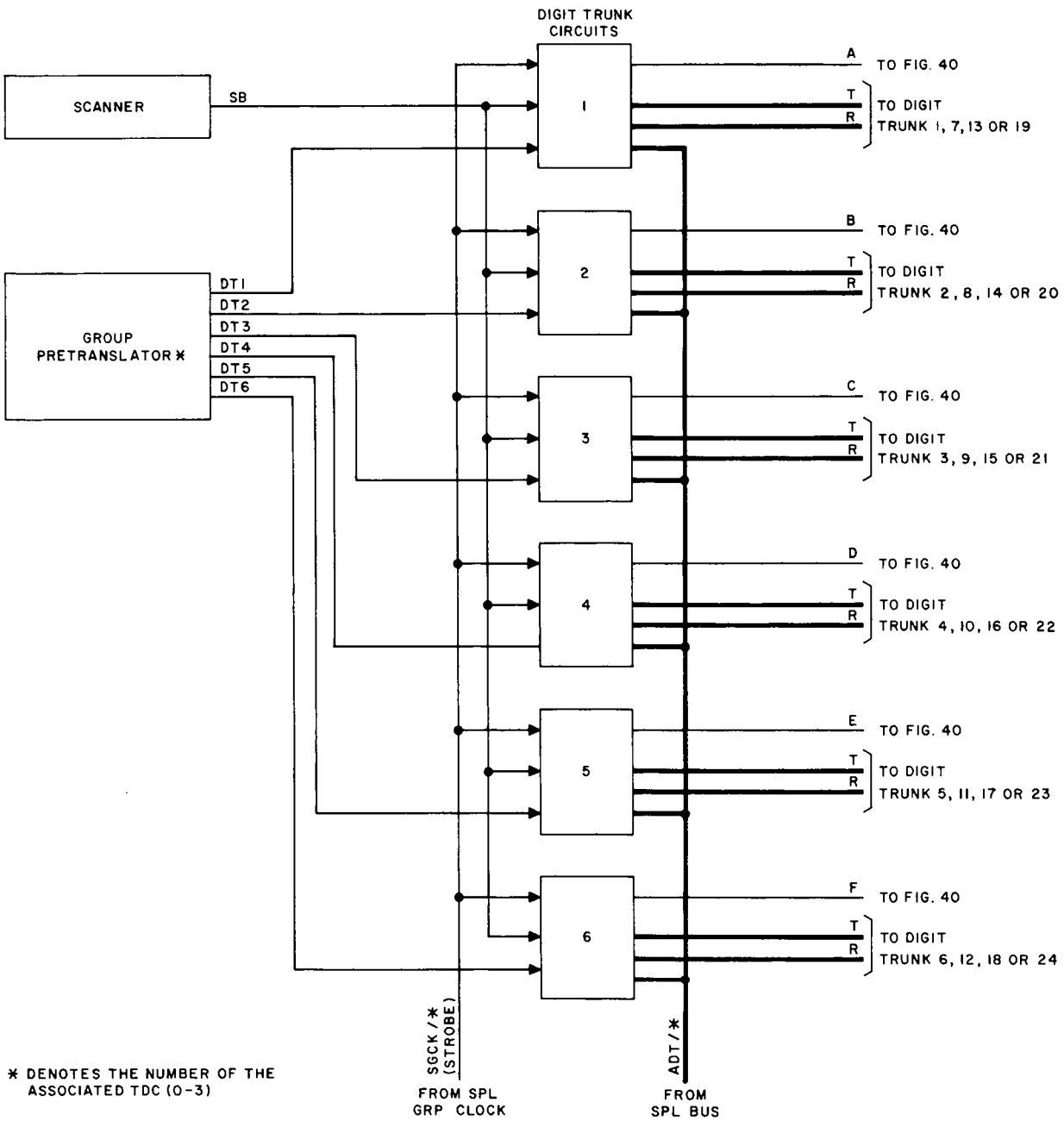
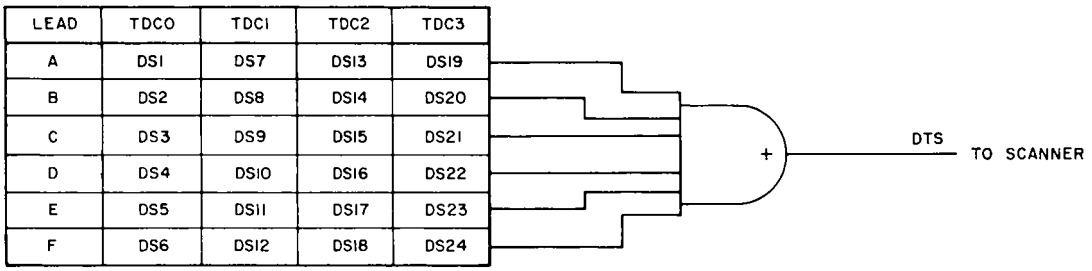


Fig. 39—Digit Trunk Circuit Transmission and Control

The time-out feature provides that during on-hook iterations of 75 msec or less, the capacitor ***does not*** charge to a voltage high enough to enable the circuit before the capacitor is again discharged by the next off-hook iteration of the signaling process. However, if the on-hook time is 300 msec or greater, the capacitor ***does*** charge to a voltage sufficient for the generation of scan inhibiting pulses, and the scanner circuit recognizes the on-hook condition of the signaling party.

3.155 The voice-frequency TOUCH-TONE signals are processed by the transmission path portion of the digit trunk circuit like any other talking connection. Since rotary dial pulses are not voice frequencies, but a series of on-hook and



LEAD	TDC0	TDC1	TDC2	TDC3
A	DS1	DS7	DS13	DS19
B	DS2	DS8	DS14	DS20
C	DS3	DS9	DS15	DS21
D	DS4	DS10	DS16	DS22
E	DS5	DS11	DS17	DS23
F	DS6	DS12	DS18	DS24

Fig. 40—Multiple Output Detector

off-hook states, the dial pulses from the signaling party are detected on the scan bus. The tone generator circuit produces a 50-msec tone burst each time the signaling party goes on-hook. The tone burst is coupled to the digit trunk via a third winding of the line transformer.

3.156 The tone generator in the digit trunk circuit oscillates at two frequencies simultaneously. If the signaling party is off-hook, the oscillator is prevented from operating due to a shunt path to ground. When the signaling produces an on-hook condition, a charged capacitor enables the oscillator to generate a 50-msec tone burst registering a change from off-hook to on-hook. Thus, the 50-msec multiple frequency tone burst, which is independent of the actual dial pulse length, is sent to the control unit for each on-hook state of the signaling party while the digit trunk is assigned.

Dial Pulse Filter

3.156.1 Rotary dialing requires the use of dial pulse filter circuits. When the calling party is scanned during the dialing interval, dial pulses appear as changes of state even though the long-term supervisory state of the calling party is off-hook. To eliminate this ambiguity, dial pulse filter circuits are provided in the scanner associated with each time division control.

3.156.2 Consider the interval of time just before a calling party in the dialing state is interrogated. After the scan counter advances to the calling party address, the contents of all talking time slots will appear in the output registers of the four TDCs prior to the calling party interrogation. A bit-by-bit comparison is made between the ten lower order stages of the scan counter and the calling address store contents in every time slot. Since the given line must be a calling address in one of the four TDCs, one of the comparitor gates will indicate when the scan counter is equal to the number of a calling party which is connected to a digit trunk.

3.156.3 The dial pulse filter circuit is the control element which prevents dial pulses from being interpreted as changes in the supervisory state of the calling party. When a change of supervisory state has been detected during a talking time slot, two possible courses of action occur during the subsequent data time slots:

(a) When the instantaneous supervisory state of the calling party is off-hook (between dialed digits), it is not necessary to force the scanner to advance to a new address. This does not cause a false message since the instantaneous and long-term state of the calling party is off-hook and there is no mismatch which will stop the scanner.

(b) When the instantaneous supervisory state of the calling party is on-hook (in this case, due to a dial pulse on the scan bus), the scanner is caused to advance to the next scan point (avoiding a false message).

3.156.4 When a calling party digit trunk connection exists in some talking time slot and that calling party flashes, scanner operation ensures that both an on-hook and off-hook message is transmitted:

(a) The beginning of the flash interval is treated as a dial pulse by the digit trunk with lead DTS staying at ground during the calling party digit trunk time slot, and no scanner detection of the on-hook change of state occurs.

(b) After 100 msec, the dial pulse filtering of the digit trunk times out so that lead DTS on longer pulses to ground during the calling party digit trunk time slot and the on-hook message is sent. No reinterrogation takes place for this on-hook change of state. This enhances the ability of the scanner to recognize short flashes.

(c) When the calling party goes back off-hook at the end of the flash interval, lead DTS immediately resumes pulsing to ground during the calling party digit trunk time slot. Now, however, the scanner detects a mismatch since the last-look bit of the calling party shows on-hook (because of the message sent at the beginning of the flash) and its present state is off-hook. After detecting the first mismatch, the scanner goes through reinterrogation as with any other line or trunk scan point.

3.156.5 It should also be noted that if a calling subscriber abandons in the process of dialing, the on-hook message transmission is the same as for the initial on-hook message for a flash. This ensures that the control unit will clear the calling party digit trunk connection from the time slot.

F. Special Switches

3.157 Special switches (ADT/0 through ADT/3) of the respective intergroup switch circuits (IGS0 through IGS3) provide connections between the intergroup buses and the special buses of each associated special group circuit. Fig. 41 is a block diagram of the special bus switch and control circuit associated with one time division control.

3.158 When a digit trunk is required, the DTN signal is produced and the special bus switch in the associated TDC is enabled. The conference circuit clock signal (CCA) strobes the enabled switch (ADT) to produce the voice frequency connection.

3.159 When one of the attendant circuits or tone circuits is required in a given time division control, the applicable special switch (ADT) is operated to connect the intergroup and special buses of the same number designation together. The attendant or tone (ATNE) select signal enables the applicable ADT switch, which operates when strobed by the CLK signal. The CLK signal is the same signal employed with the special group

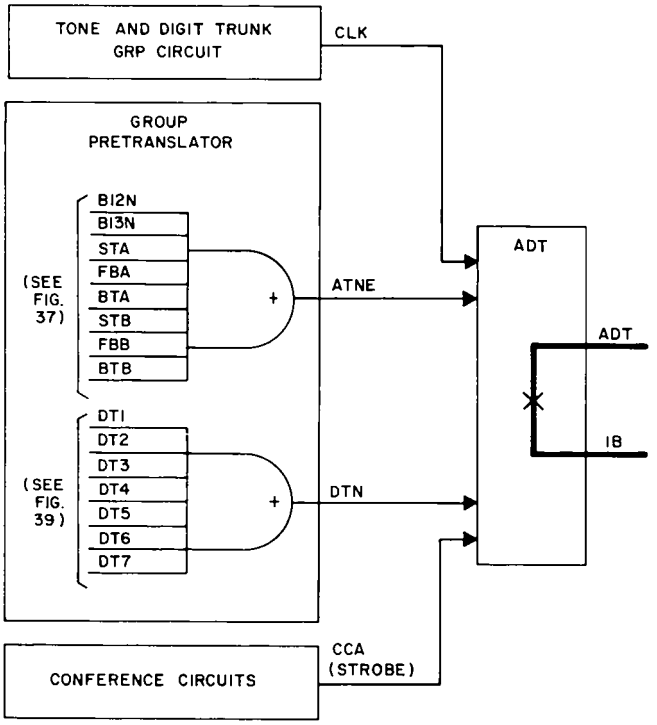


Fig. 41—Special Bus Switch and Control

tones circuit. The ATNE signal is produced when any of the ST, FB, or BT (A or B) tone leads are activated or when either of the two least significant attendant select bits (B12 or B13) is a logic one.

ATTENDANT CIRCUITS

3.160 The maintenance and attendant circuit provides the lamp control and key supervision at the attendant console. Lamp drive currents are produced by information translated from the contents of the associated lamp word. Sixteen attendant lamp words are provided in each switch store circuit. The contents of the attendant lamp words are sequentially accessed during the attendant time slot. The 16 attendant lamp words in TDC0 and TDC1 provide lamp information for attendants 1 through 6. Six additional attendant consoles (7 through 12) may be controlled by TDC2 and TDC3. The attendant key circuits are supervised by the attendant and common scan point circuits which provide off-hook signals to the scanner when interrogated. The method of interrogation for attendant scan points was described in 3.71 through 3.78.

3.161 Fig. 42 is the arrangement of lamp word memory which employs store words 112 through 127. A given attendant lamp word is accessed once every 16 store cycles or once every 1.38 msec. The first four words are trunk group busy, incoming call identification, and calls waiting information. The remaining three groups of four words are assigned to the six associated attendant circuits for the control of loop lamps and common lamps at each console. The attendant lamp words are numbered 0 through 15 and are selected by the store address translator (Fig. 15) under control of the attendant counter during each time slot A0 except during the incoming lamp message relocation iteration (see 3.114).

3.162 Fig. 43 is the lamp address assignment plan which shows the supplementary message address bits and the related attendant counter bits which are associated with lamp words. The two least significant bits define the lamp information word associated with a given pair of six attendants in TDC0 and TDC1 or six attendants in TDC2 and TDC3. The attendant pair number corresponds to the binary state of the two most significant bits. Pair number 00 information governs operation of the trunk group busy, incoming call identification, and calls waiting lamps. In pairs 1, 2, and 3, information governing loops 1 and 4 is stored in the first word, loops 2 and 5 in the second word, loops 3 and 6 in the third word, and the common lamp information in the fourth word.

3.163 Fig. 44 is the bit arrangement for each of the first three words (store words 112, 113, and 114) containing the trunk group busy (TGB) and incoming call identification (ICI) lamp information. Each 32-bit word (of the 3) provides 20 bits employed to control TGB lamps. The three store words thus provide 60 bits which control as many as 60 TGB lamps for all of the 12 attendant consoles in parallel. A maximum of 30 TGB lamps for attendants 1 through 3 can be provided by using circuits within the switch unit. The remaining TGB lamps require added circuitry contained in the auxiliary cabinet. Each word (of the 3) provides an attendant associated 5-bit code for controlling as many as 30 ICI lamps for each attendant independently. A maximum of 12 ICI lamps per attendant for the first 3 attendants and 6 ICI lamps per attendant for the other attendants can be provided by using circuitry within the switch unit. The remaining ICI lamps require added circuitry contained in the auxiliary cabinet.

3.164 Fig. 45 is the bit arrangement for the fourth attendant word (store word 115) which contains a 2-bit code for the operation of calls waiting (CW) lamps on all attendant consoles. The dark state denotes no calls waiting, the steady state denotes one or two calls waiting, and the flashing state is selected when there are three or more calls waiting. When a traffic supervisor control cabinet is provided, three calls waiting lamps may be operated steady, one at a time, on the traffic supervisor position. The white, green, and red traffic supervisor calls waiting lamps are respectively designated CW1, CW2, and CW3.

3.165 The first three words assigned (Fig. 42) to a given attendant (words 4 through 6, 8 through 10, or 12 through 14) contain loop lamp

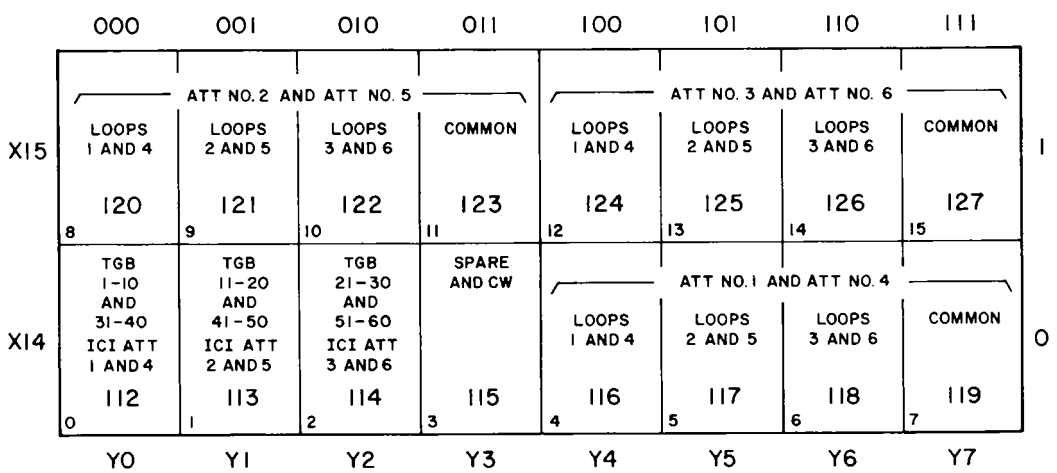
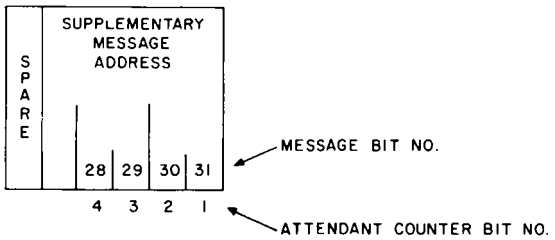


Fig. 42—Memory Arrangement for Attendant Lamp Words



NOTE:

ATTENDANT COUNTER BITS 1 AND 2 PROVIDE FOUR COUNTS (0 THROUGH 3). THE FIRST THREE COUNTS SELECT LOOP LAMP WORDS. THE FOURTH COUNT SELECTS THE COMMON LAMP WORD ASSOCIATED WITH THE APPLICABLE ATTENDANT PAIR (1-3). ATTENDANT COUNTER BITS 3 AND 4 ARE THE FOURS COUNT WHICH CORRESPONDS TO THE ATTENDANT PAIR NUMBER (0 THROUGH 3). PAIR 0 IS ASSIGNED TO TRUNK GROUP BUSY, INCOMING CALL IDENTIFICATION, AND CALLS WAITING LAMPS. 1, 2, AND 3 (FOURS COUNT) ARE ASSIGNED TO THE ATTENDANT ASSOCIATED LOOP AND COMMON LAMPS.

ATND COUNTER BIT NO.				ATND PAIR NO.	ATND NO.		LAMP PHASE	
4	3	2	1		TDC0 TDC1	TDC2 TDC3	A	B
0	0	0	0	00	1 AND 4	7 AND 10	TRUNK GP BUSY INC CALL IDENT	TRUNK GP BUSY INC CALL IDENT
0	0	0	1		2 AND 5	8 AND 11	TRUNK GP BUSY INC CALL IDENT	TRUNK GP BUSY INC CALL IDENT
0	0	1	0		3 AND 6	9 AND 12	TRUNK GP BUSY INC CALL IDENT	TRUNK GP BUSY INC CALL IDENT
0	0	1	1		ALL	ALL	CALLS WAITING	CALLS WAITING
0	1	0	0	01	1 AND 4	7 AND 10	LOOP 1	LOOP 4
0	1	0	1		1 AND 4	7 AND 10	LOOP 2	LOOP 5
0	1	1	0		1 AND 4	7 AND 10	LOOP 3	LOOP 6
0	1	1	1		1 AND 4	7 AND 10	COMMON	COMMON
1	0	0	0	02	2 AND 5	8 AND 11	LOOP 1	LOOP 4
1	0	0	1		2 AND 5	8 AND 11	LOOP 2	LOOP 5
1	0	1	0		2 AND 5	8 AND 11	LOOP 3	LOOP 6
1	0	1	1		2 AND 5	8 AND 11	COMMON	COMMON
1	1	0	0	03	3 AND 6	9 AND 12	LOOP 1	LOOP 4
1	1	0	1		3 AND 6	9 AND 12	LOOP 2	LOOP 5
1	1	1	0		3 AND 6	9 AND 12	LOOP 3	LOOP 6
1	1	1	1		3 AND 6	9 AND 12	COMMON	COMMON

Fig. 43—Lamp Address Assignment Plan

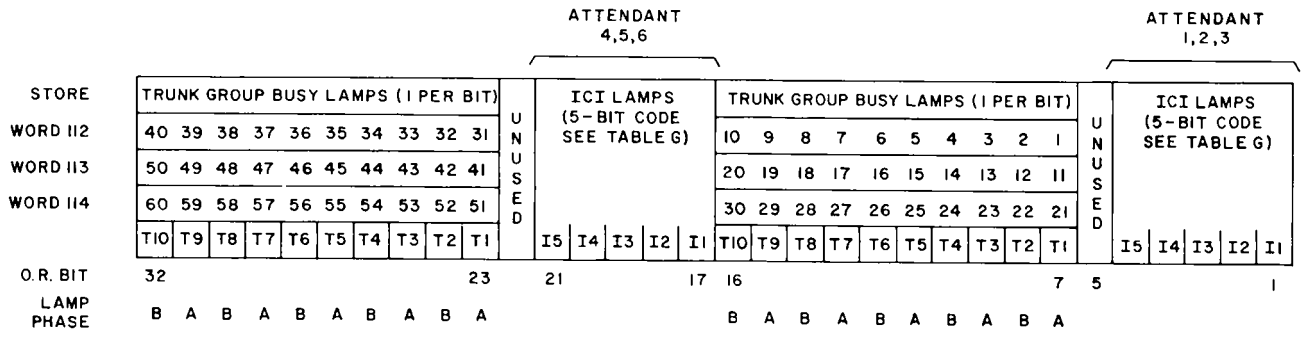
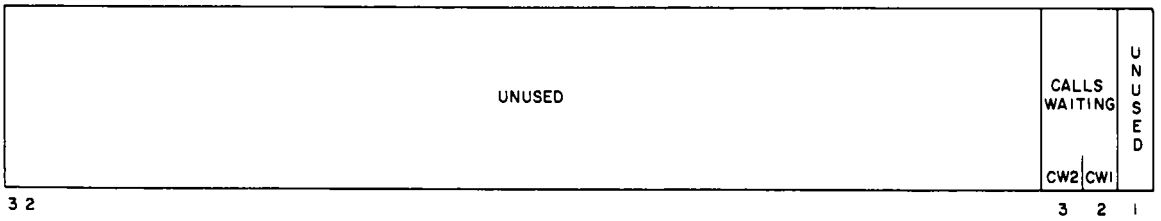


Fig. 44—TGB and ICI Lamp Word Bits



* TSC NOT EQUIPPED

SELECT BITS		CW LAMP ALL CONSOLES
CW2	CW1	
0	0	DARK
0	1	STEADY
1	0	30 IPM
1	1	30 IPM

* TSC EQUIPPED

SELECT BITS		CALLS WAITING INDICATION				
		ALL CONSOLES	TRAFFIC SUPERVISOR CABINET			
CW2	CW1		WHITE LAMP	GREEN LAMP	RED LAMP	AUDIBLE ALERT
0	0	DARK	DARK	DARK	DARK	OFF
0	1	STEADY	STEADY	DARK	DARK	OFF
1	0	STEADY	DARK	STEADY	DARK	ON
1	1	STEADY	DARK	DARK	STEADY	ON

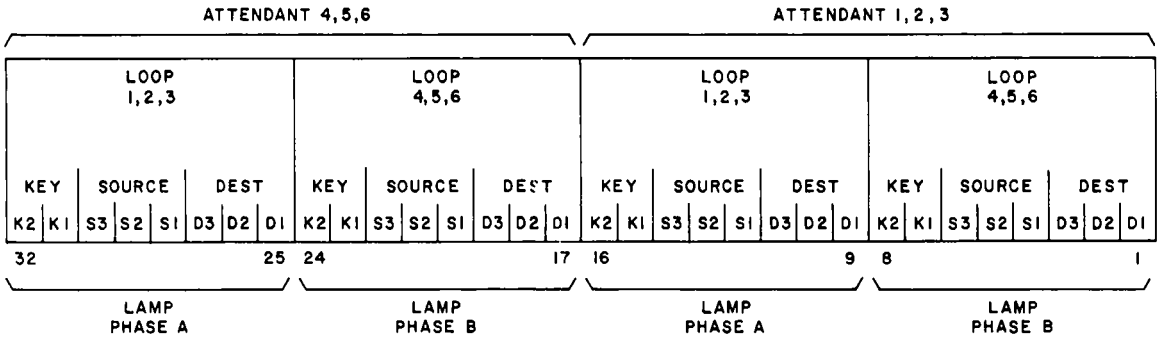
* TRAFFIC SUPERVISOR CONTROL

Fig. 45—Calls Waiting Lamp Word Bits

information; the fourth word (word 7, 11, or 15) contains common lamp information. Fig. 46 is the arrangement of bits in the loop lamp store word. Each 32-bit loop lamp store word provides two 16-bit loop lamp information words. Bits 1 through 16 are assigned to attendants 1, 2, or 3 in the three words. Bits 17 through 32 are similarly assigned to attendants 4, 5, or 6. TDC2 and TDC3 provide attendants 7 through 12 in a like manner. Lamp state information for the key, source, and destination lamps is provided for two loops in each loop lamp word. Loops 1, 2, and 3 are associated with phase A of loop lamp words 1, 2 and 3, respectively, while loops 4, 5, and 6 are associated with phase B of loop lamp words 1, 2, and 3. The key lamp word consists of two bits (K2 and K1) which, when translated, can produce three lamp states (dark, wink, and steady). The three bits (S3, S2, and S1) in the source lamp word are used to produce four lamp states (dark, 60 ipm, 120 ipm, and steady). The three bits (D3, D2, and D1) in the destination lamp word are used to produce five lamp states (dark, wink, 60 ipm, 120 ipm, and steady).

3.166 Fig. 47 is the arrangement of bits in the common lamp word. Four lamp states are provided for the two conference lamps, CONF 1 and CONF 2. The four states are dark, wink, 120 ipm, and steady. Other common lamp words are the night service (NS), position busy (PB), exclude destination (ED), ready (RD), exclude source (ES), audible signal (AS), and position available (PA).

3.167 Fig. 48 is the block diagram for attendant lamp circuits which provide the control for illumination of loop and common lamps, trunk group busy lamps, and incoming call identification lamps. The attendant lamp words are selected by the attendant counter and read into the output register which applies the lamp word bits to the loop lamp translator, common lamp translator, trunk group busy lamp control, and incoming call identification lamp control circuits. The attendant counter state is also translated by the attendant word selector circuit to produce one-hot-out-of-sixteen signals which are employed in the control of the word-associated portions of the various lamp translator and driver circuits. The interrrupt generator provides signals which produce certain gated outputs from the loop lamp and common lamp translators, enabling certain lamps to be operated in five different states: dark (off), steady (on), slow flash (60 ipm), fast flash (120 ipm), and wink (1/4 second "off" during each 2-second "on" interval). The lamp phase generator provides two low-frequency control signals, phase A and phase B, which are 1/12 of the attendant counter cycling frequency. All the circuits are duplicated and TDC associated except the lamp driver circuits



KEY LAMP WORD

SEL BITS		LAMP STATE
K2	K1	
0	0	DARK
0	1	WINK
1	0	STEADY
1	1	———

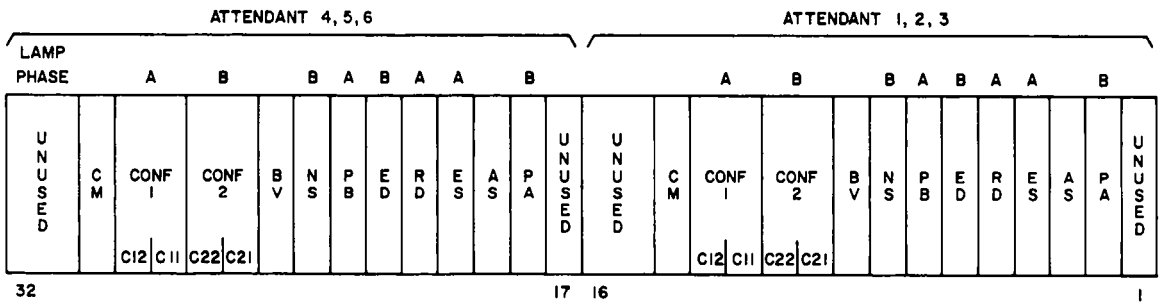
SOURCE LAMP WORD

SELECTION BITS			LAMP STATE
S3	S2	S1	
0	0	0	———
0	0	1	DARK
0	1	0	———
0	1	1	60 IPM
1	0	0	STEADY
1	0	1	120 IPM
1	1	0	———
1	1	1	———

DESTINATION LAMP WORD

SELECTION BITS			LAMP STATE
D3	D2	D1	
0	0	0	———
0	0	1	DARK
0	1	0	WINK
0	1	1	60 IPM
1	0	0	STEADY
1	0	1	120 IPM
1	1	0	———
1	1	1	———

Fig. 46—Loop Lamp Word Bits



CONFERENCE LAMP WORD

SEL BITS		LAMP STATE	FUNCTION
C12	C11		
C22	C21		
0	0	DARK	
0	1	WINK	
1	0	120 IPM	
1	1	STEADY	

Fig. 47—Common Lamp Word Bits

and the attendant transfer circuit which selects the switch control from which the lamp information is read. The switch store circuits of TDC0 and TDC1 both contain the same attendant lamp information for reliability purposes and are associated with the first six attendants. Similarly, the information contained in switch store circuits of TDC2 and TDC3 is identical and is associated with the second six attendants.

A. Attendant Counter

3.168 The attendant counter circuit consists of four stages AC0 through AC3. The counter is normally advanced once each store cycle at time slot B0. Although the attendant counter state is not employed by the store address translator and attendant word selector circuits until time slot A1, the counter is advanced during time slot B0 to ensure that the counter stages have time to settle before the attendant lamp time slot.

3.169 The double-rail attendant counter output leads DB0 through DB3 are applied to the store address translator for store word memory access control and to the scanner circuit for generating a noise mask. The eight counter output leads are also applied to the attendant word selector, which translates each attendant counter state into a corresponding one-hot-out-of-sixteen signal. The negate output (DB3N) from the fourth counter stage is applied to the lamp phase generator.

B. Lamp Phase Generator

3.170 The lamp phase generator circuit provides low-frequency lamp phasing signals for the purpose of interrupting the latched dc lamp drive currents operating during the given phase. The latching action occurs in the operation of a single PNPN transistor of the lamp driver circuits which also provide two phasing gates to control the state of two independent console lamps. The lamp driver is described later in 3.191.

3.171 The basic timing source to the lamp phase generator is the DB3N lead which provides a symmetrical square wave with a period of 1.38 msec. The first four stages of the ripple counter are arranged to produce 12 states out of a possible 16 counts. The counter advances in a routine manner from the binary state 0001 through 0110. At the next count, when the first three stages are all ones, a reset signal is applied to the second stage. Since the first and third stages are ones, the second stage, when reset, advances to the zero state, producing a carry signal which ripples through the higher order stages to produce a 9 count; this causes the counter to jump from the binary state 0110 to 1001. During the following six counts, the binary state advances from 1001 to 1110. Again, at next count when the first three stages are all ones, the second stage is reset and the change of state ripples through to produce a 1 count, eg, the binary state jumps from 1110 to 0001. Thus, the count sequence is 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13, 14, 1, 2, etc.

3.172 The state of the fourth counter stage changes after counts 6 and 14, producing a frequency division of 12 based upon the 1.38-msec attendant lamp word input signal, which results in a symmetrical square wave with a period of 16.56 msec. The double-rail outputs from the fourth stage are applied to regulating monopulsers which modify the symmetry of the applied square waves to establish a guard interval between applied 8.28-msec lamp phases and to regulate the rms voltage of the console lamps that are lighted during the produced phase. The rms lamp voltage is adjusted by varying the pulse width. Therefore, to hold the lamp voltage from the +24 volt supply constant over a range from +20.4 to +26.4 volts, the pulse width is varied from 7 msec to 4.6 msec, respectively. The minimum guard interval between phases (when both monopulser outputs are at ground level) is 1.56 msec. The outputs of the two monopulsers thus provide two lamp phase signals, A and B.

C. Interrupt Generator

3.173 The interrupt generator is provided to establish the interruption rate for the busy tones, ringing interval, attendant busy verification, and attendant lamp illumination. The application for busy tones (G120N and G60), ringing (G30, G30N, G15, and G15N), and busy verification (G120N and G60) are described in the special group circuits, ringing circuits, and line and trunk circuit parts of this section, respectively. The interruption rate for attendant lamps employs the G120, G60N, and GW (wink) signals in the loop lamp translator and common lamp translator circuits to produce five lamp states. The states of illumination are dark (off), steady (on), fast flash (120 ipm), slow flash (60 ipm), and wink (1/4 second "off" during each 2-second "on" interval).

D. Attendant Word Selection

3.174 The attendant word selector circuit produces one of 16 output signals in accordance with the attendant counter state. Each attendant word selection signal partially enables the lamp driver circuits associated with the attendant lamp word. Other inputs required for operation of a given lamp driver circuit are supplied by the loop lamp word and common lamp word translator circuits and the phase signal A or B from the lamp phase generator. Thus, the attendant word selector circuit operates during time slot A0 from the attendant counter output signals as a one-hot-out-of-sixteen translator. Duplicated attendant word selector circuits are provided within the attendant circuit for reliability. The output leads of one of the TDC associated circuits are selected by the attendant transfer control relay contacts to provide the output signals A01M01 through A34M01 in the basic switch unit (TDC0 and TDC1) and A01M23 through A34M23 in the auxiliary switch unit (TDC2 and TDC3) circuits.

E. Loop Lamp Translator

3.175 The loop lamp translator circuit determines the state of each attendant console loop lamp from coded information contained in the associated loop lamp word. Three of the four lamp words are each allocated to a given pair of attendants, eg, attendants 1 and 4, 2 and 5, and 3 and 6. Information governing attendant 1, 2, or 3 is contained in bits B1 through B16 of TDC0 and TDC1. Similarly, information governing attendants 4, 5, and 6 is contained in bits B17 through B32 of TDC0 and TDC1. The loop lamp translator circuit is duplicated for reliability, and either of the duplicated set of attendant lamp word translations may be selected by the attendant transfer circuit for application to the lamp gate and driver circuits. TDC2 and TDC3 similarly provide translation for the second group of six attendants (7 through 12).

3.176 Six loops with three lamps each are provided for each attendant. The three lamps associated with each loop are: key, source, and destination. Loop lamp bits for loops 1, 2, and 3 are translated during the lamp phase A cycle while loops 4, 5, and 6 are translated during the lamp phase B cycle.

3.177 Bits 16 and 15 during phase A produce one of three states for loop 1 key lamp (Fig. 46) on the KAB01 lead: dark, wink, or steady. Bits 8 and 7 produce the same three states on the KAB01 lead for loop 4 key lamp during phase B. Similarly, bits 14, 13, and 12 during phase A produce one of four source lamp states (Fig. 46) on the SAB01 lead: dark, steady, 60 ipm, or 120 ipm. Bits 6, 5, and 4 produce source lamp states during phase B on the SAB01 lead for loop 4 lamps. Five states of illumination may be translated for the destination lamps of loop 1 (from bits 11, 10, and 9) during phase A and loop 4 (from bits 3, 2, and 1) during phase B. The five states are dark, steady, 60 ipm, 120 ipm, and wink.

F. Common Lamp Translator

3.178 The common lamp translator circuit determines the state of all attendant common lamps. The common lamp translator operation is generally the same as that described for the loop lamp translator. The common lamp word bits 1 through 16 and 17 through 32, which were shown in Fig. 47, are translated to produce corresponding lamp driver enable signals for operating the common lamps of attendants 1 through 3 and 4 through 6, respectively. The four lamp states which are provided on the conference lamp CFA01 output lead are dark, wink, 120 ipm, and steady. The lamp state is translated by a pair of bits. Two conference lamps are provided. The first, CONF 1, is translated from bits 29 and 28 or 13 and 12 during phase A, and the other, CONF 2, is translated from bits 27 and 26 or 11 and 10 during phase B.

3.179 With the exception of calls waiting lamp translation, all other common lamps have only the two states, steady and dark. The RDPA01 lead is at ground level at each attendant time slot during phase A when lead B21 or B5 is at ground level to operate the attendant associated ready (RD) lamp during phase A. Lead B2, at ground level, produces the RDPA01 signal during phase B to operate the position available (PA) lamp. The ESED01 signal is similarly produced by a ground level on the B4 or B6 lead to operate the exclude source (ES) lamp or exclude destination (ED) lamp during phase A or B, respectively. The PBNS01 signal is similarly produced by the B7 or B8 leads during phase A or B for the respective operation of the position busy (PB) or night service (NS) lamp.

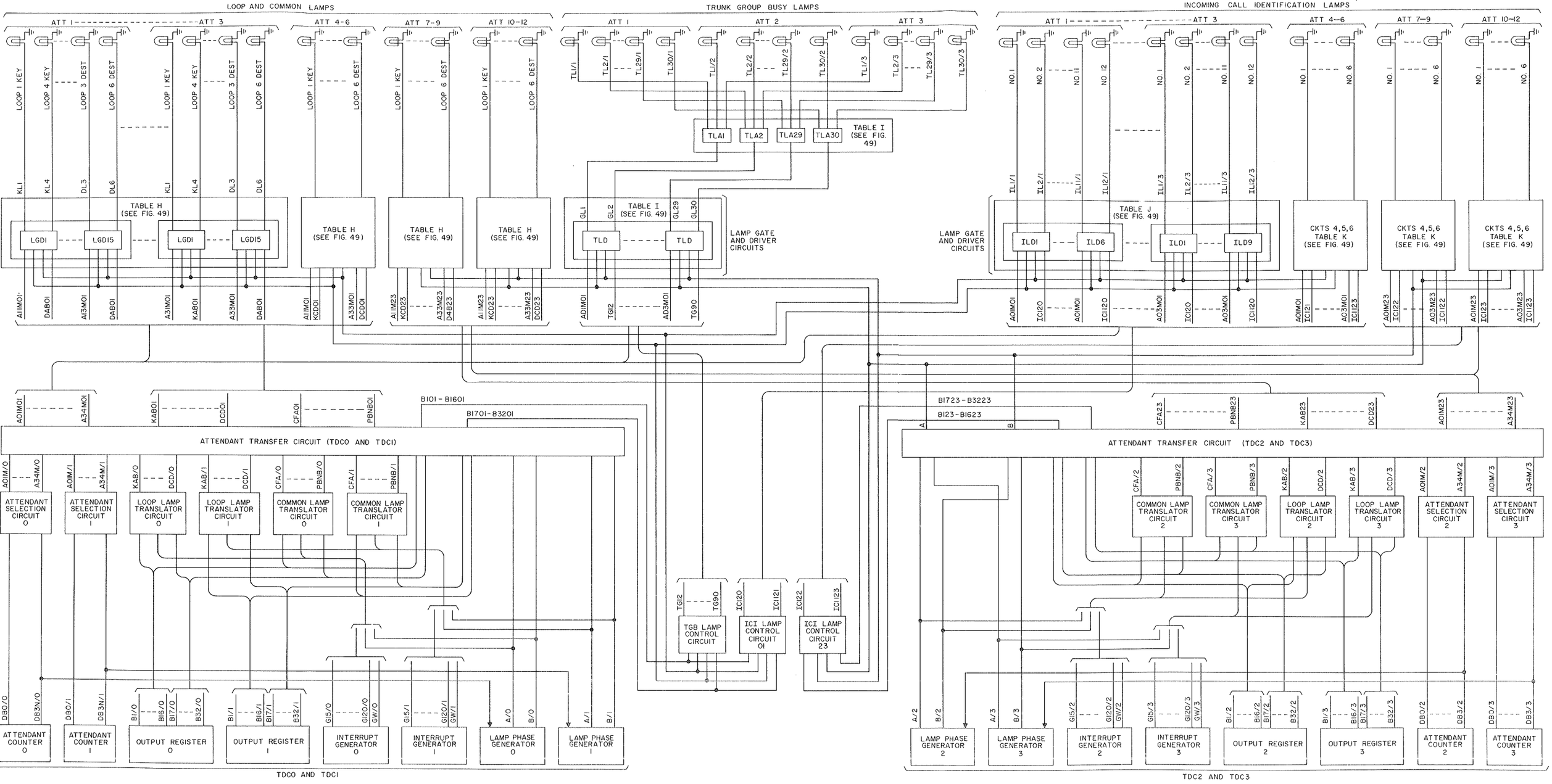
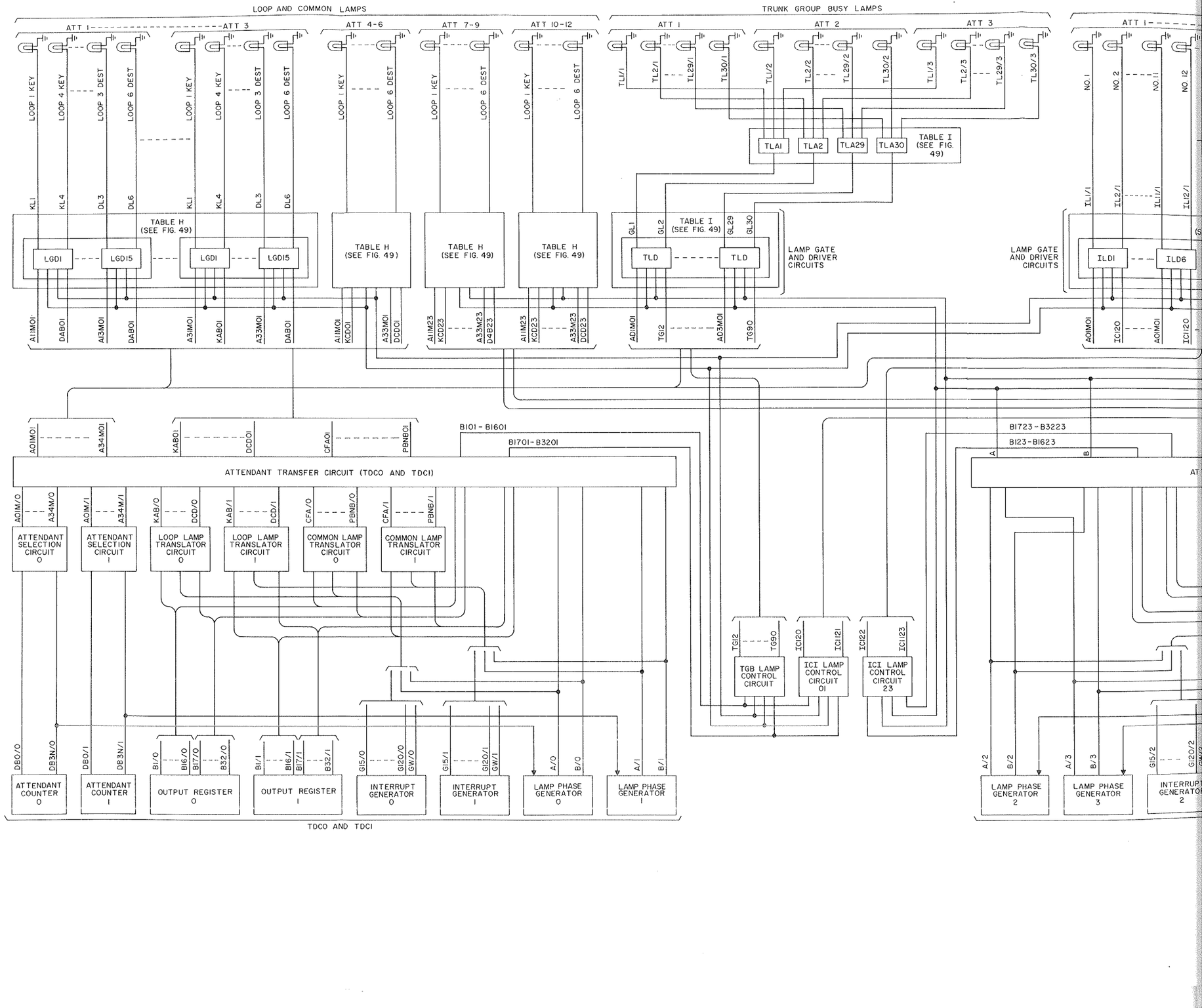


Fig. 48—Attendant Lamp Control Circuit—Block Diagram


LOOP AND COMMON LAMPS
ATT 1
ATT 3
ATT 4-6
ATT 7-9
ATT 10-12
LOOP 1 KEY
LOOP 4 KEY
LOOP 3 DEST
LOOP 6 DEST
KL1
KL4
DL3
DL6
TABLE H (SEE FIG. 49)
LGD1
LGD15
A11M01
DAB01
A13M01
A33M01
KAB01
KCD01
DCD01
A11M23
KCD23
A33M23
D4B23
DCD23
TRUNK GROUP BUSY LAMPS
ATT 2
TLI/1
TL2/1
TL29/1
TL30/1
TLI/2
TL2/2
TL29/2
TL30/2
TLI/3
TL2/3
TL29/3
TL30/3
TLA1
TLA2
TLA29
TLA30
TABLE I (SEE FIG. 49)
GL1
GL2
GL29
GL30
TLD
LAMP GATE AND DRIVER CIRCUITS
AD1M01
TG12
AD3M01
TG90
NO. 1
NO. 2
NO. 11
NO. 12
IL1/1
IL2/1
IL11/1
IL12/1
ILD1
ILD6
AO1M01
IC120
IC1120
AO1M01
A34M01
DCD01
CFA01
PBNB01
B101 - B1601
B1701 - B3201
B1723 - B3223
B123 - B1623
A
B
ATTENDANT TRANSFER CIRCUIT (TDCO AND TDCI)
AO1M/0
A34M/0
AO1M/1
A34M/1
KAB/0
DCD/0
KAB/1
DCD/1
CFA/0
PBNB/0
CFA/1
PBNB/1
ATTENDANT SELECTION CIRCUIT 0
ATTENDANT SELECTION CIRCUIT 1
LOOP LAMP TRANSLATOR CIRCUIT 0
LOOP LAMP TRANSLATOR CIRCUIT 1
COMMON LAMP TRANSLATOR CIRCUIT 0
COMMON LAMP TRANSLATOR CIRCUIT 1
TG12
TG90
IC120
IC1121
IC122
IC1123
TGB LAMP CONTROL CIRCUIT
ICI LAMP CONTROL CIRCUIT 01
ICI LAMP CONTROL CIRCUIT 23
DE0/0
DB3N/0
DE0/1
DB3N/1
BI/0
BI6/0
BI7/0
B32/0
BI/1
BI6/1
BI7/1
B32/1
GI5/0
GI20/0
GW/0
GI5/1
GI20/1
GW/1
A/0
B/0
A/1
B/1
ATTENDANT COUNTER 0
ATTENDANT COUNTER 1
OUTPUT REGISTER 0
OUTPUT REGISTER 1
INTERRUPT GENERATOR 0
INTERRUPT GENERATOR 1
LAMP PHASE GENERATOR 0
LAMP PHASE GENERATOR 1
A/2
B/2
A/3
B/3
GI5/2
GI20/2
LAMP PHASE GENERATOR 2
LAMP PHASE GENERATOR 3
INTERRUPT GENERATOR 2
TDCO AND TDCI

3.180 The calls waiting portion of the common lamp control circuit provides a translation of bits 2 and 3 shown in Fig. 45. The translation produces the CW01 signal during phase A in three states: dark, steady, and 30 ipm. Where the traffic supervisor position and control circuit is provided, white, green, or red CW lamp signals and an audible alert signal may be produced. The traffic supervisory control circuit will be described in 3.197.

3.181 In switch units which provide "attendant line circuits with tone", the busy verification tone (BVTN) is produced as an indication to the talking parties that an attendant has come onto the line for the purpose of busy verification. The steady tone (440 cps) is gated by the G15 interrupt signal in the "attendant line circuit with tone" when the control unit supplies a 1 in the applicable bit 25 or 9 (BV) of the associated attendant common word (Fig. 47). The busy verification feature only provides a warning tone to the talking parties and does not control lamp driver operation.

G. Trunk Group Busy Lamp Control

3.182 The trunk group busy (TGB) lamp control circuit determines the state of all TGB lamps located on the individual attendant consoles. The TGB lamps can have two states (steady or dark). The TGB lamp control circuit produces signals for selecting up to 60 lamps. The 3A switch unit provides circuits to drive 30 lamps on each of the first 3 attendant consoles. Where more than 30 lamps must be provided or more than 3 attendants must be served, additional lamp driver circuits may be provided in the auxiliary cabinet. The TGB lamps at each attendant position, respectively, operate in parallel.

3.183 The first three attendant words (0 through 2) read from store words 112 through 114 (Fig. 42) provide the TGB lamp state information (Fig. 44) on a single lamp per bit basis. The first 30 TGB lamps are controlled by the 10 bits (7 through 16) of the 3 store words (112 through 114). Similarly, the same three store words provide TGB lamp state information for TGB lamps 31 through 60 via bits 23 through 32.

3.184 The lamp phase and lamp state information are combined in the TGB lamp control circuit. The five even numbered bits (8, 10, 12, 14, 16) of the on-line TDC (0 or 1) produce the five output signals TG12, TG34, TG56, TG78, and TG90, respectively, during the phase B interval. The five odd numbered bits (7, 9, 11, 13, 15) similarly produce the same five output signals during the phase A interval. Thus, a single output lead provides a path for the information of two bits on a time shared basis, eg, during their assigned phase intervals.

3.185 The five TGB lamp control output leads, TG12 through TG90 (Fig. 48), are applied to the trunk group busy lamp drivers for providing lamp currents under control of the attendant word selector and lamp phase signal. The applicable lamp is illuminated by a 1 in the corresponding lamp word bit and is dark when the bit is a 0.

H. Incoming Call Identification Lamp Control

3.186 The incoming call identification (ICI) lamp control circuit optionally provides the translation signals necessary to illuminate up to a maximum of 30 ICI lamps on each of the 12 attendant consoles. Translation circuits are provided by circuits in the switch unit to generate signals which select 12 ICI lamps at each of the 12 attendant positions. However, lamp driver circuits in the switch unit can only accommodate 12 ICI lamps for attendant consoles, 1, 2, and 3. The auxiliary cabinet may be equipped with circuits to produce the translation and drive for the additional ICI lamps.

3.187 The ICI lamps operate independently on each console. Only one of the ICI lamps on a particular attendant console can be illuminated at any one time. The information which controls the ICI lamps is contained in the first three attendant lamp information words (Fig. 44), which also contain the trunk group busy lamp bits.

3.188 Table G shows the 5-bit ICI lamp code. Each code corresponds to one lighted ICI lamp. The 5-bit code contained in B1 through B5 of the first three attendant words is associated with the first three attendants. Similarly, the code contained in B17 through B21 of the same three words is associated with attendants 4, 5, and 6. The same lamp information is stored for attendants 1 through 6 in TDC0 and TDC1, and one or the other channel of information is applied to the ICI lamp control circuit via the attendant transfer relays. The redundant signals are utilized to ensure circuit reliability. Redundant storage is similarly

employed in TDC2 and TDC3 to provide ICI lamp information for attendants 7 through 12.

3.189 Lamp phasing signals A and B are combined with the least significant bit of the lamp code to enable all odd numbers during phase A and all even numbers during phase B. The three next higher order bits define six pair count numbers associated with the translator output signals used to drive 12 lamps, 6 during phase A and 6 during phase B. The ICI lamp control circuit output signals are combined with the attendant word selector signals (A01M01, A02M01, and A03M01) and lamp phase signals in one of the six ICI lamp drivers in Fig. 48 to provide current to the selected ICI lamp.

I. Lamp Driver Circuits

3.190 Fig. 49 is a diagram of a block of lamp driver circuits. Forty-four blocks (circuit cards) may be provided in the switch unit. Each block of six lamp drivers is provided with two lamp phase drivers, one for phase A and the other for phase B. Thus, the 44 circuit cards of 6 circuits provide 264 lamp driver circuits including spare driver circuits.

3.191 Each lamp driver circuit may control the illumination of two attendant console lamps. The one lamp is illuminated via output lead G during the phase A interval. Similarly, the other lamp is illuminated via output lead H during phase B. The PNPN driver transistor is caused to latch in a saturated state of conduction when both input leads E and F are at ground level. As shown in Fig. 48, one input lead is controlled by one of the attendant word selector output leads, while the other input lead is controlled by one of the lamp translator output leads. The AND gate input lead (E and F) designations for each loop and common lamp driver circuit are listed in Table H. Also listed are the phase-associated output lead designations and lamp illumination functions for each attendant. Table I lists similar information for trunk group busy lamp illumination functions, and Tables J and K list the incoming call identification lamp illumination functions for each attendant.

3.192 As shown in Fig. 48, all the lamp driver circuits for loop lamps, common lamps, and incoming call identification lamps and trunk group busy lamps (for the first attendant) are identical. The second and third attendant trunk group busy lamp driver circuits are controlled by the first position lamp driver to provide the required parallel operation.

J. Audible Signal Control Circuit

3.193 Fig. 50 is the audible signal circuit which provides an audible signal for each attendant in the switch unit. Also shown is an optional audible signal circuit for calls waiting lamp lighted conditions. The optional circuit may be provided at the first attendant position only. The audible signal flip-flop (ASFF) follows the state of bit 3 or bit 19 of the attendant associated common lamp words (word 7, 11, or 15) duplicated in TDC0 and TDC1 for the first six attendants. Bit 3 of words 7, 11, and 15 is associated with attendants 1, 2, and 3, respectively. Bit 19 of words 7, 11, and 15 is associated with attendants 4, 5, and 6, respectively. The same two bits of words 7, 11, and 15 duplicated in TDC2 and TDC3 are similarly associated with the second six attendants (7 through 12). When the AS bit is equal to 1, the ASFF is set to turn on the audible signal driver (ASD), which provides a ground return path for the audible signal generator. When the AS bit is equal to 0, the ASFF is reset, turning off the audible signal.

3.194 The optional control circuit for the audible signal generator to also indicate calls waiting is used only with the first attendant. The option consists of adding another control circuit, the calls waiting signal flip-flop (CWSFF), which is set when the CWS01 and A04M01 leads are at ground level. The CWS01 lead is at ground level whenever bit 2 or bit 3 of the calls waiting bit pair is equal to 1. The A04M01 lead is at ground level when the fourth attendant word (word 3) is read into the output register. The reset side output of CWSFF, when set, is at battery level and turns the ASD on via double inversion to produce an audible signal. When both CW bits are equal to 0, the CWSFF is reset, turning off the audible signal, provided it is not also turned on by the associated AS bit being equal to 1, as previously described in 3.180.

K. Attendant Console Maintenance Circuit

3.195 Fig. 51 is the attendant console maintenance circuit which sets the assigned console maintenance scan point to the off-hook state whenever bit 14 or bit 30 of the applicable attendant associated common lamp word (word 7, 11, or 15) is a 1. A ground level (B14 or B30 is a 1) on

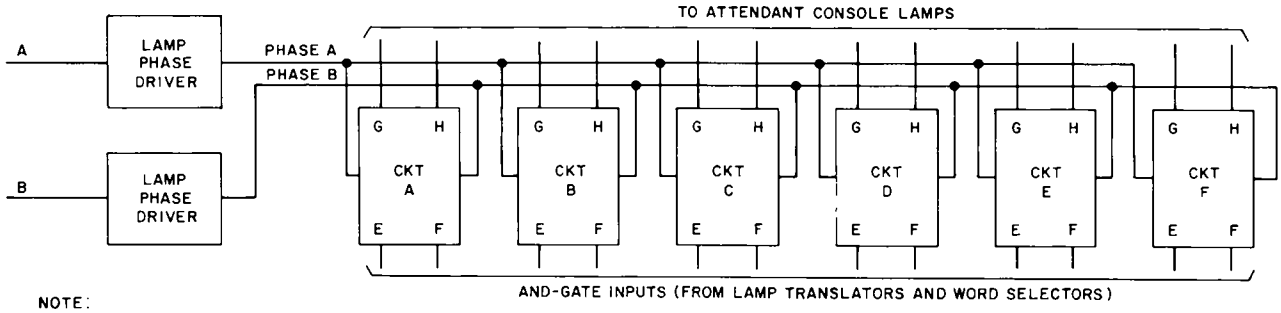
TABLE G

5-BIT CODE FOR SELECTION OF ICI LAMPS

ICI CONTROL CIRCUIT INPUT BIT NO.					LAMP PHASE	ICI LAMP NO.	LAMP DRIVER INPUT	ATTENDANT		
PAIR COUNT NO.				ODD/ EVEN				1	2	3
B5 B21	B4 B20	B3 B19	B2 B18	B1 B17						
0	0	0	0	0	—	—	——	——	——	——
0	0	0	0	1	—	—				
0	0	0	1	0	A	1	IC12*	ILD1	ILD1	ILD1
0	0	0	1	1	B	2				
0	0	1	0	0	A	3	IC34*	ILD2	ILD2	ILD2
0	0	1	0	1	B	4				
0	0	1	1	0	A	5	IC56*	ILD3	ILD3	ILD3
0	0	1	1	1	B	6				
0	1	0	0	0	A	7	IC78*	TLD4	ILD4	ILD7
0	1	0	0	1	B	8				
0	1	0	1	0	A	9	IC910*	TLD5	ILD5	ILD8
0	1	0	1	1	B	10				
0	1	1	0	0	A	11	IC112*	TLD6	ILD6	ILD9
0	1	1	0	1	B	12				
0	1	1	1	0	A	13				
0	1	1	1	1	B	14				
1	0	0	0	0	A	15				
1	0	0	0	1	B	16				
1	0	0	1	0	A	17				
1	0	0	1	1	B	18				
1	0	1	0	0	A	19				
1	0	1	0	1	B	20				
1	0	1	1	0	A	21				
1	0	1	1	1	B	22				
1	1	0	0	0	A	23				
1	1	0	0	1	B	24				

Translation for these ICI lamp numbers may be provided in the auxiliary cabinet.

* Equals 0 for attendants 1 through 3,
1 for attendants 4 through 6,
2 for attendants 7 through 9,
3 for attendants 10 through 12.



NOTE:

THE FOLLOWING TABLE LISTS THE 6 DRIVER CIRCUIT DESIGNATIONS ON EACH OF THE 44 BLOCKS (CIRCUIT CARDS) OF LAMP DRIVER CIRCUITS.

* INDICATES CIRCUITS EMPLOYED WITH IC17/1 THOUGH IC112/1 LAMP CIRCUITS.

CKT NO.	DRIVER CIRCUIT CARD										
	1	2	3	4	5	6	7	8	9	10	11
A	LGD1	LGD7	LGD13	LGD1	LGD7	LGD13	LGD1	LGD7	LGD13	LGD1	LGD7
B	LGD2	LGD8	LGD14	LGD2	LGD8	LGD14	LGD2	LGD8	LGD14	LGD2	LGD8
C	LGD3	LGD9	LGD15	LGD3	LGD9	LGD15	LGD3	LGD9	LGD15	LGD3	LGD9
D	LGD4	LGD10	ILD1	LGD4	LGD10	ILD1	LGD4	LGD10	ILD1	LGD4	LGD10
E	LGD5	LGD11	ILD2	LGD5	LGD11	ILD2	LGD5	LGD11	ILD2	LGD5	LGD11
F	LGD6	LGD12	ILD3	LGD6	LGD12	ILD3	LGD6	LGD12	ILD3	LGD6	LGD12

CKT NO.	DRIVER CIRCUIT CARD										
	12	13	14	15	16	17	18	19	20	21	22
A	LGD13	LGD1	LGD7	LGD13	LGD1	LGD7	LGD13	LGD1	LGD7	LGD13	LGD1
B	LGD14	LGD2	LGD8	LGD14	LGD2	LGD8	LGD14	LGD2	LGD8	LGD14	LGD2
C	LGD15	LGD3	LGD9	LGD15	LGD3	LGD9	LGD15	LGD3	LGD9	LGD15	LGD3
D	ILD1	LGD4	LGD10	ILD1	LGD4	LGD10	ILD1	LGD4	LGD10	ILD1	LGD4
E	ILD2	LGD5	LGD11	ILD2	LGD5	LGD11	ILD2	LGD5	LGD11	ILD2	LGD5
F	ILD3	LGD6	LGD12	ILD3	LGD6	LGD12	ILD3	LGD6	LGD12	ILD3	LGD6

CKT NO.	DRIVER CIRCUIT CARD										
	23	24	25	26	27	28	29	30	31	32	33
A	LGD7	LGD13	LGD1	LGD7	LGD13	LGD1	LGD7	LGD13	LGD1	LGD7	LGD13
B	LGD8	LGD14	LGD2	LGD8	LGD14	LGD2	LGD8	LGD14	LGD2	LGD8	LGD14
C	LGD9	LGD15	LGD3	LGD9	LGD15	LGD3	LGD9	LGD15	LGD3	LGD9	LGD15
D	LGD10	ILD1	LGD4	LGD10	ILD1	LGD4	LGD10	ILD1	LGD4	LGD10	ILD1
E	LGD11	ILD2	LGD5	LGD11	ILD2	LGD5	LGD11	ILD2	LGD5	LGD11	ILD2
F	LGD12	ILD3	LGD6	LGD12	ILD3	LGD6	LGD12	ILD3	LGD6	LGD12	ILD3

CKT NO.	DRIVER CIRCUIT CARD										
	34	35	36	37	38	39	40	41	42	43	44
A	LGD1	LGD7	LGD13	TLD1	TLD1	TLD1	ILD4	LGDP1	LGDW	LGDP7	SPARE
B	LGD2	LGD8	LGD14	TLD2	TLD2	TLD2	ILD5	LGDP4	LGDGR	LGDP10	SPARE
C	LGD3	LGD9	LGD15	TLD3	TLD3	TLD3	ILD6	SPARE	LGDAS	SPARE	SPARE
D	LGD4	LGD10	ILD1	TLD4	TLD4	TLD4*	ILD7	LGDP2	LGDP6	LGDP8	LGDP12
E	LGD5	LGD11	ILD2	TLD5	TLD5	TLD5*	ILD8	LGDP5	SPARE	LGDP11	SPARE
F	LGD6	LGD12	ILD3	TLD6	TLD6	TLD6*	ILD9	LGDP3	SPARE	LGDP9	SPARE

Fig. 49—Lamp Driver Circuits—Block Diagram

TABLE H

LOOP AND COMMON LAMP ILLUMINATION

LAMP FUNCTION		DRIVER CIRCUIT	LAMP DRIVER AND-GATE INPUT SIGNALS						LAMP DRIVER OUTPUT SIGNALS	
PHASE A	PHASE B		ATT. 1 ATT. 7	ATT. 2 ATT. 8	ATT. 3 ATT. 9	ATT. 4 ATT. 10	ATT. 5 ATT. 11	ATT. 6 ATT. 12	PHASE A	PHASE B
Loop 1 Key	Loop 4 Key	LGD1	KAB# A11M#	KAB# A21M#	KAB# A31M#	KCD# A11M#	KCD# A21M#	KCD# A31M#	KL1	KL4
Loop 1 Source	Loop 4 Source	LGD2	SAB# A11M#	SAB# A21M#	SAB# A31M#	SCD# A11M#	SCD# A21M#	SCD# A31M#	SL1	SL4
Loop 1 Dest.	Loop 4 Dest.	LGD3	DAB# A11M#	DAB# A21M#	DAB# A31M#	DCD# A11M#	DCD# A21M#	DCD# A31M#	DL1	DL4
Conf. 1	Conf. 2	LGD4	CFA# A14M#	CFA# A24M#	CFA# A34M#	CFB# A14M#	CFB# A24M#	CFB# A34M#	CL1	CL2
Ready	PA	LGD5	RDPA# A14M#	RDPA# A24M#	RDPA# A34M#	RDPB# A14M#	RDPB# A24M#	RDPB# A34M#	RYL	PAL
ES	ED	LGD6	ESDA# A14M#	ESDA# A24M#	ESDA# A34M#	ESDB# A14M#	ESDB# A24M#	ESDB# A34M#	ESL	EDL
Loop 2 Key	Loop 5 Key	LGD7	KAB# A12M#	KAB# A22M#	KAB# A32M#	KCD# A12M#	KCD# A22M#	KCD# A32M#	KL2	KL5
Loop 2 Source	Loop 5 Source	LGD8	SAB# A12M#	SAB# A22M#	SAB# A32M#	SCD# A12M#	SCD# A22M#	SCD# A32M#	SL2	SL5
Loop 2 Dest.	Loop 5 Dest.	LGD9	DAB# A12M#	DAB# A22M#	DAB# A32M#	DCD# A12M#	DCD# A22M#	DCD# A32M#	DL2	DL5
PB	NS	LGD10	PBNA# A14M#	PBNA# A24M#	PBNA# A34M#	PBNB# A14M#	PBNB# A24M#	PBNB# A34M#	PBL	NSL
Calls Waiting	———	LGD11	CW# A04M01	CW# A04M01	CW# A04M01	CW# A04M01	CW# A04M01	CW# A04M01	CWL	——
———	———	(Spare) LGD12	———	———	———	———	———	———	——	——
Loop 3 Key	Loop 6 Key	LGD13	KAB# A13M#	KAB# A23M#	KAB# A33M#	KCD# A13M#	KCD# A23M#	KCD# A33M#	KL3	KL6
Loop 3 Source	Loop 6 Source	LGD14	SAB# A13M#	SAB# A23M#	SAB# A33M#	SCD# A13M#	SCD# A23M#	SCD# A33M#	SL3	SL6
Loop 3 Dest.	Loop 6 Dest.	LGD15	DAB# A13M#	DAB# A23M#	DAB# A33M#	DCD# A13M#	DCD# A23M#	DCD# A33M#	DL3	DL6

equals 01 for attendants 1 through 6 (TDC0 & TDC1).
equals 23 for attendants 7 through 12 (TDC2 & TDC3).

the TMA01 or TMB01 lead and the coincidence of a ground level on the applicable attendant word selection lead (A*4M01) sets the assigned attendant console maintenance scan point to the off-hook state. The asterisk (*) denotes which of the three numbered attendants the lead is assigned to control.

3.196 The state, B14 equal to 1, is defined as off-hook for the console maintenance (CM) scan point for attendant 1, 2, or 3. The state of B30 similarly is associated with the CM scan point of attendant 4, 5, or 6. To clear the scan point (eg, switch it to the on-hook state), a 0 is employed

TABLE I

TRUNK GROUP BUSY LAMP ILLUMINATION

LAMP FUNCTION		TGB LAMP DRIVER CIRCUIT	INPUT SELECT LEADS	OUTPUT LEADS	TGB LAMP AMPLIFIER CIRCUIT	OUTPUT LEADS					
						ATTENDANT 1		ATTENDANT 2		ATTENDANT 3	
PHASE A	PHASE B					PHASE A	PHASE B	PHASE A	PHASE B	PHASE A	PHASE B
No. 1	No. 2	TLD1	TG12 A01M01	GL2	TLA1	TL1/1	———	TL1/2	———	TL1/3	———
					TLA2		TL2/1	———	TL2/2	———	TL2/3
No. 3	No. 4	TLD2	TG34 A01M01	GL4	TLA3	TL3/1		TL3/2	———	TL3/3	———
					TLA4		TL4/1	———	TL4/2	———	TL4/3
No. 5	No. 6	TLD3	TG56 A01M01	GL6	TLA5	TL5/1		TL5/2	———	TL5/3	———
					TLA6		TL6/1	———	TL6/2	———	TL6/3
No. 7	No. 8	TLD4	TG78 A01M01	GL8	TLA1	TL7/1		TL7/2	———	TL7/3	———
					TLA2		TL8/1	———	TL8/2	———	TL8/3
No. 9	No. 10	TLD5	TG90 A01M01	GL10	TLA3	TL9/1		TL9/2	———	TL9/3	———
					TLA4		TL10/1	———	TL10/2	———	TL10/3
No. 11	No. 12	TLD6	TG12 A02M01	GL12	TLA5	TL11/1		TL11/2	———	TL11/3	———
					TLA6		TL12/1	———	TL12/2	———	TL12/3
No. 13	No. 14	TLD1	TG34 A02M01	GL14	TLA1	TL13/1		TL13/2	———	TL13/3	———
					TLA2		TL14/1	———	TL14/2	———	TL14/3
No. 15	No. 16	TLD2	TG56 A02M01	GL16	TLA3	TL15/1		TL15/2	———	TL15/3	———
					TLA4		TL16/1	———	TL16/2	———	TL16/3
No. 17	No. 18	TLD3	TG78 A02M01	GL18	TLA5	TL17/1		TL17/2	———	TL17/3	———
					TLA6		TL18/1	———	TL18/2	———	TL18/3
No. 19	No. 20	TLD4	TG90 A02M01	GL20	TLA1	TL19/1		TL19/2	———	TL19/3	———
					TLA2		TL20/1	———	TL20/2	———	TL20/3
No. 21	No. 22	TLD5	TG12 A03M01	GL22	TLA3	TL21/1		TL21/2	———	TL21/3	———
					TLA4		TL22/1	———	TL22/2	———	TL22/3
No. 23	No. 24	TLD6	TG34 A03M01	GL24	TLA5	TL23/1		TL23/2	———	TL23/3	———
					TLA6		TL24/1	———	TL24/2	———	TL24/3
No. 25	No. 26	TLD1	TG56 A03M01	GL26	TLA1	TL25/1		TL25/2	———	TL25/3	———
					TLA2		TL26/1	———	TL26/2	———	TL26/3
No. 27	No. 28	TLD2	TG78 A03M01	GL28	TLA3	TL27/1		TL27/2	———	TL27/3	———
					TLA4		TL28/1	———	TL28/2	———	TL28/3
No. 29	No. 30	TLD3	TG90 A03M01	GL30	TLA5	TL29/1		TL29/2	———	TL29/3	———
					TLA6		TL30/1	———	TL30/2	———	TL30/3

in the common lamp word. The common scan points 278, 294, 310, 1302, 1318, 1334, 1046, 1062, 1078, 1110, 1126, and 1142 are assigned to attendants 1 through 12, respectively. The 12 scan points, a part of the maintenance and attendant scan points, were described in 3.71 through 3.78.

Traffic Supervisor Lamps

3.197 The switch unit may be optionally equipped with lamp control and driver circuits for a traffic supervisor position. Fig. 52 is the traffic

TABLE J

INCOMING CALL IDENTIFICATION LAMP ILLUMINATION (ATTENDANTS 1 THROUGH 3)

LAMP FUNCTION		ATTENDANT 1				ATTENDANT 2				ATTENDANT 3			
PHASE A	PHASE B	DRIVER CIRCUIT DESIG-NATION	AND-GATE INPUTS	OUTPUT LEADS		DRIVER CIRCUIT DESIG-NATION	AND-GATE INPUTS	OUTPUT LEADS		DRIVER CIRCUIT DESIG-NATION	AND-GATE INPUTS	OUTPUT LEADS	
				PHASE A	PHASE B			PHASE A	PHASE B			PHASE A	PHASE B
No. 1	No. 2	ILD1	IC120 A01M01	IL1/1	IL2/1	ILD1	IC120 A02M01	IL1/2	IL2/2	ILD1	IC120 A03M01	IL1/3	IL2/3
No. 3	No. 4	ILD2	IC340 A01M01	IL3/1	IL4/1	ILD2	IC340 A02M01	IL3/2	IL4/2	ILD2	IC340 A03M01	IL3/3	IL4/3
No. 5	No. 6	ILD3	IC560 A01M01	IL5/1	IL6/1	ILD3	IC560 A02M01	IL5/2	IL6/2	ILD3	IC560 A03M01	IL5/3	IL6/3
No. 7	No. 8	TLD4	IC780 A01M01	IL7/1	IL8/1	ILD4	IC780 A02M01	IL7/2	IL8/2	ILD7	IC780 A03M01	IL7/3	IL8/3
No. 9	No. 10	TLD5	IC9100 A01M01	IL9/1	IL10/1	ILD5	IC9100 A02M01	IL9/2	IL10/2	ILD8	IC9100 A03M01	IL9/3	IL10/3
No. 11	No. 12	TLD6	IC1120 A01M01	IL11/1	IL12/1	ILD6	IC1120 A02M01	IL11/2	IL12/2	ILD9	IC1120 A03M01	IL11/3	IL12/3

TABLE K

INCOMING CALL IDENTIFICATION LAMP ILLUMINATION (ATTENDANTS 4 THROUGH 12)

LAMP FUNCTION		DRIVER CIRCUIT DESIG-NATION	AND-GATE INPUT LEAD DESIGNATIONS									OUTPUT LEAD DESIGNATIONS	
PHASE A	PHASE B		ATND 4	ATND 5	ATND 6	ATND 7	ATND 8	ATND 9	ATND 10	ATND 11	ATND 12	PHASE A	PHASE B
No. 1	No. 2	ILD1	IC121 A01M01	IC121 A02M01	IC121 A03M01	IC122 A01M23	IC122 A02M23	IC122 A03M23	IC123 A01M23	IC123 A02M23	IC123 A03M23	IL1/*	IL2/*
No. 3	No. 4	ILD2	IC341 A01M01	IC341 A02M01	IC341 A03M01	IC342 A01M23	IC342 A02M23	IC342 A03M23	IC343 A01M23	IC343 A02M23	IC343 A03M23	IL3/*	IL4/*
No. 5	No. 6	ILD3	IC561 A01M01	IC561 A02M01	IC561 A03M01	IC562 A01M23	IC562 A02M23	IC562 A02M23	IC563 A01M23	IC563 A02M23	IC563 A03M23	IL5/*	IL6/*

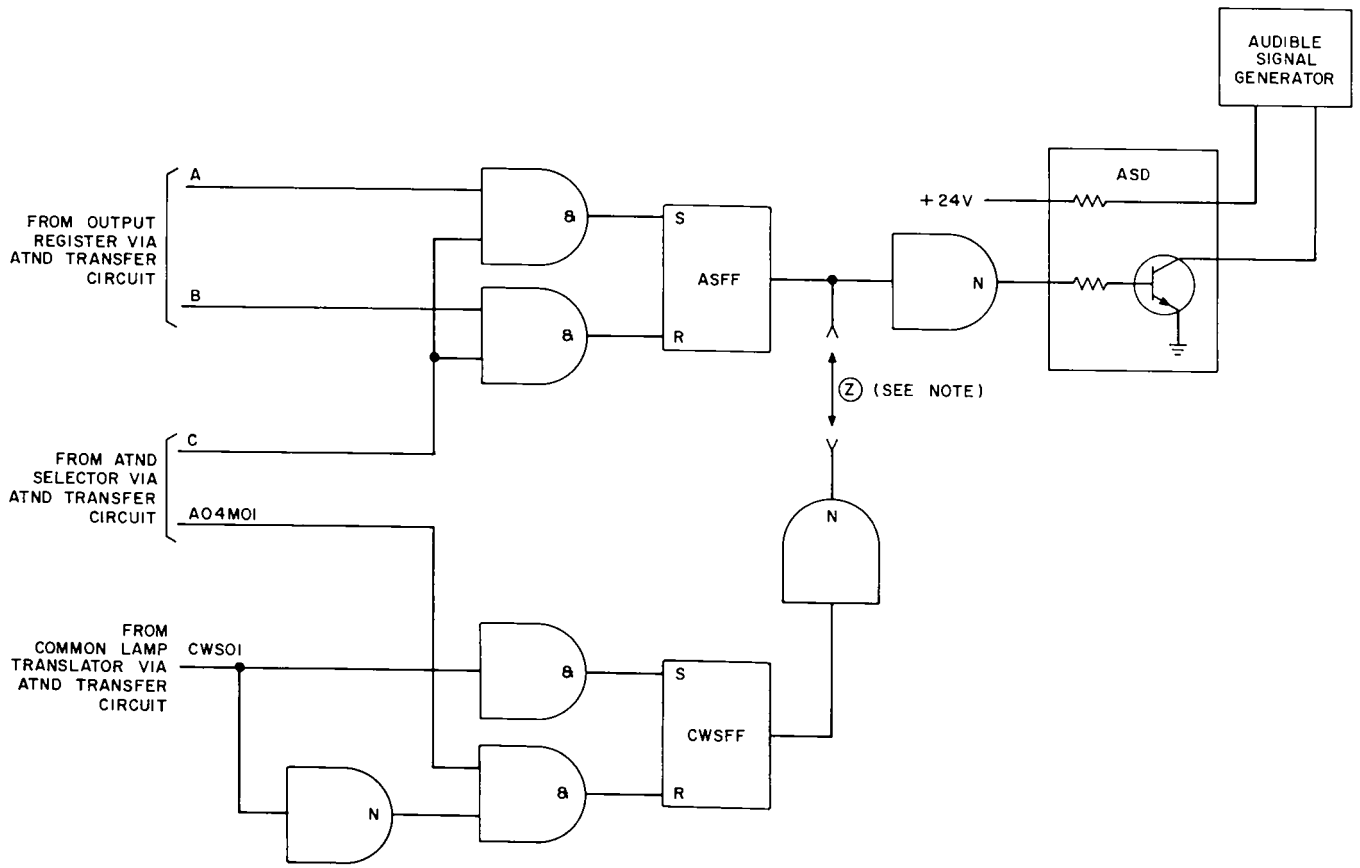
* denotes attendant number.

supervisor position lamp and control circuit. The option provides the following features:

- Position available and position busy lamps for each attendant
- Three calls waiting lamps
- An audible alert
- A nonlocking alarm cutoff for interrupting the audible alert.

3.198 Four lamp driver circuit cards are provided by the traffic supervisor position option. The lamp driver circuits were discussed in 3.190. Table L shows each lamp function and phase interval, the driver circuit designation, the AND gate input enable signals, and the lamp driver output signals associated with phase A and phase B.

3.199 The states of the position available (PA) and position busy (PB) lamps on the traffic supervisor cabinet simply reproduce the states of the PA and PB lamps on all the individual consoles

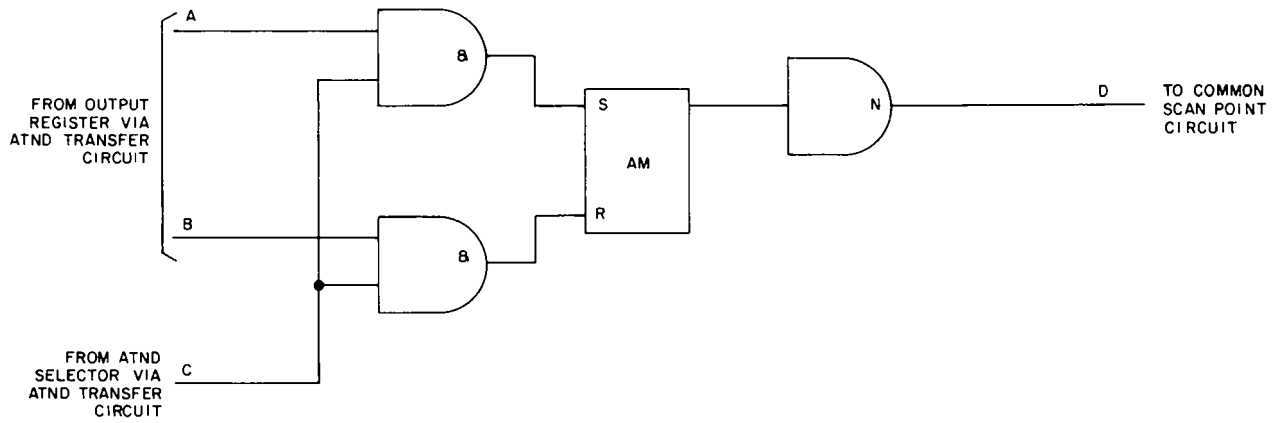


NOTE:
THE AUDIBLE SIGNAL CIRCUIT IS PROVIDED ON A 1 PER ATTENDANT BASIS. OPTION Z PROVIDES AN AUDIBLE SIGNAL FOR CALLS WAITING LAMP LIGHTED ON THE FIRST ATTENDANT POSITION ONLY.

LEAD DESIGNATION	ATTENDANT NUMBER											
	1	2	3	4	5	6	7	8	9	10	11	12
A	TSAOI	TSAOI	TSAOI	TSBOI	TSBOI	TSBOI	TSA23	TSA23	TSA23	TSB23	TSB23	TSB23
B	TSNAOI	TSNAOI	TSNAOI	TSNBOI	TSNBOI	TSNBOI	TSNA23	TSNA23	TSNA23	TSNB23	TSNB23	TSNB23
C	AI4MOI	A24MOI	A34MOI	AI4MOI	A24MOI	A34MOI	AI4M23	A24M23	A34M23	AI4M23	A24M23	A34M23

Fig. 50—Audible Signal Circuit

at a single location and are derived from the states of the corresponding PA and PB lamps on the individual attendant consoles. The lamp driver output leads designated SPA1 through SPA12 or SPB1 through SPB12 may be activated by the assigned attendant word selector and traffic supervisor control signals to the AND gate inputs in conjunction with the assigned lamp phase signals. The PA lamps for attendants 1 through 3 are activated during phase B by the PAB13 signal, which is translated from the state of bit 2 (B201 signal) in common lamp words 1 through 3, respectively, in TDC0 and TDC1. Bit 7 (B701 signal) of the same three common lamp words similarly activates the PAB13 lead during phase A to operate the three respective lamps PB1 through PB3. The PAB46 lead similarly operates PA and PB lamps 4 through 6 during their assigned lamp phases in accordance with the respective bits 18 and 23 of the same three common lamp words



LEAD DESIGNATION	ATTENDANT NUMBER											
	1	2	3	4	5	6	7	8	9	10	11	12
A	TMA01	TMA01	TMA01	TMB01	TMB01	TMB01	TMA23	TMA23	TMA23	TMB23	TMB23	TMB23
B	TMNA01	TMNA01	TMNA01	TMNB01	TMNB01	TMNB01	TMNA23	TMNA23	TMNA23	TMNB23	TMNB23	TMNB23
C	A14M01	A24M01	A34M01	A14M01	A24M01	A34M01	A14M23	A24M23	A34M23	A14M23	A24M23	A34M23
D	278	294	310	1302	1318	1334	1046	1062	1076	1110	1126	1124

Fig. 51—Console Maintenance Scan Point

in TDC0 and TDC1. All PA lamps are assigned to phase B and all PB lamp operation occurs during the phase A interval. The three common lamp words in TDC2 and TDC3 similarly provide the PAB79 signal from bits 2 and 7 to operate the PA and PB lamps of attendants 7 through 9. The common lamp words in TDC2 and TDC3 also provide the PAB102 signal from bits 18 and 23 to operate the PA and PB lamps of attendants 10 through 12.

3.200 The PB lamps have an additional source of control provided by attendant associated signal supervisory flip-flops in the supervisory control circuits. The supervisory signal flip-flop associated with a given attendant is set via the SK* lead by operation of the nonlocking SUPV key on the attendant console. The asterisk (*) indicates the applicable attendant number. When the supervisory signal flip-flop is set, the associated PB lamp flashes at a 60-ipm rate, and an audible alert sounds until the nonlocking ACO key is operated at the supervisor position or until the alarm is reset via the SJ# lead by jacking into the supervisor jacks on the individual console. The audible alert is described in 3.193.

3.201 Three calls waiting (CW) lamps, colored white, green, and red, are provided at the traffic supervisor position and are designated CW1, CW2, and CW3, respectively. Store word 115 (Fig. 42) of TDC0 and TDC1 provides the CW lamp information (Fig. 45) to the first traffic supervisor control circuit for translation of the state of bits 2 and 3. If both bits contain zeros, all three lamps are dark, indicating that there are no calls waiting. If bit 2 only is a 1, the WCW lead (Fig. 52) is activated during phase B to operate the white lamp CW1. If bit 3 only is a 1, the GRCW lead is activated during phase B to operate the green lamp CW2. If both bits are ones, the GRCW lead is active during phase B to produce drive current for the red lamp CW3. Only one CW lamp operates at a time on the traffic supervisor position, indicating by color the relative number of calls waiting.

3.202 The audible alert (buzzer) at the traffic supervisor position sounds whenever the red or green CW lamps are lighted. When both the red and green lamps become dark, the alarm flip-flop is automatically reset and the alarm is

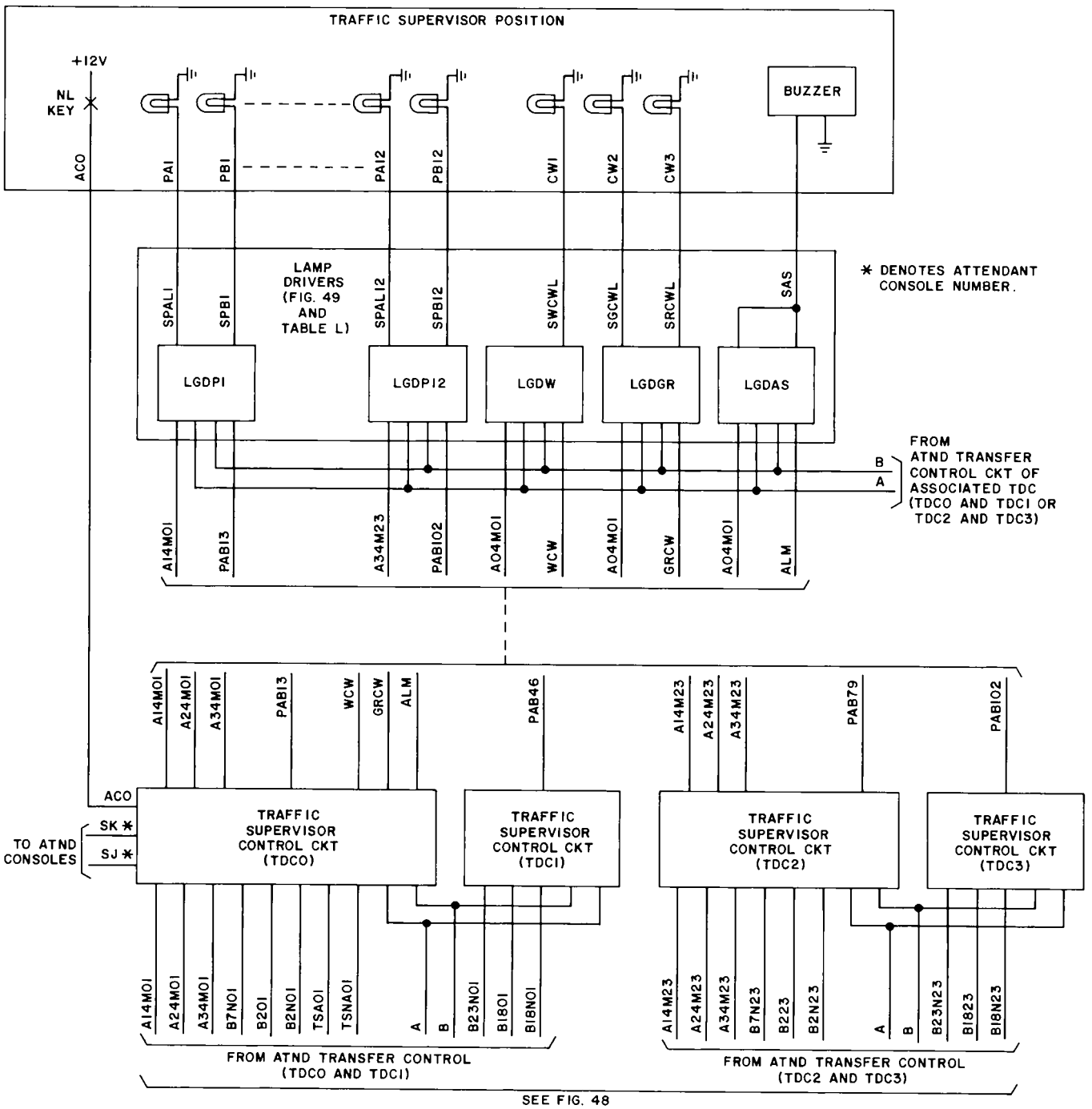


Fig. 52—Traffic Supervisor Position Lamp and Control Circuit—Block Diagram

silent unless operated by the supervisory signal flip-flops described in 3.200. Both output leads of the audible alert driver are strapped so that current to the buzzer can flow during both lamp phase intervals to establish an average current large enough to operate the buzzer.

3.203 A nonlocking alarm cutoff (ACO) key is provided at the traffic supervisor position to turn off the buzzer. Operation of the ACO key silences the buzzer when it is operating because of red or green CW lamp operation or because of the state of one of the signal supervisory flip-flops.

TABLE L

TRAFFIC SUPERVISOR POSITION LAMP ILLUMINATION

LAMP FUNCTION		DRIVER CIRCUIT	AND-GATE INPUT SIGNALS	LAMP DRIVER OUTPUT SIGNALS		LAMP FUNCTION		DRIVER CIRCUIT	AND-GATE INPUT SIGNALS	LAMP DRIVFR OUTPUT SIGNALS	
PHASE A	PHASE B			PHASE A	PHASE B	PHASE A	PHASE B			PHASE A	PHASE B
PB1	PA1	LGDP1	PAB13 A14M01	SPBL1	SPAL1	PB7	PA7	LGDP7	PAB79 A14M23	SPBL7	SPAL7
PB2	PA2	LGDP2	PAB13 A24M01	SPBL2	SPAL2	PB8	PA8	LGDP8	PAB79 A24M23	SPBL8	SPAL8
PB3	PA3	LGDP3	PAB13 A34M01	SPBL3	SPAL3	PB9	PA9	LGDP9	PAB79 A34M23	SPBL9	SPAL9
PB4	PA4	LGDP4	PAB46 A14M01	SPBL4	SPAL4	PB10	PA10	LGDP10	PAB102 A14M23	SPBL10	SPAL10
PB5	PA5	LGDP5	PAB46 A24M01	SPBL5	SPAL5	PB11	PA11	LGDP11	PAB102 A24M23	SPBL11	SPAL11
PB6	PA6	LGDP6	PAB46 A34M01	SPBL6	SPAL6	PB12	PA12	LGDP12	PAB102 A34M23	SPBL12	SPAL12
——	CW1	LGDW	WCW A04M01	——	SWCWL	——	——	——	——	——	——
CW2	CW3	LGDGR	GRCW A04M01	SGCWL	SRCWL	——	——	——	——	——	——
BUZZER		LGDAS	ALM A04M01	SAS	SAS	——	——	——	——	——	——
——	——	——	——	——	——	——	——	——	——	——	——
——	——	——	——	——	——	——	——	——	——	——	——
——	——	——	——	——	——	——	——	——	——	——	——

4. MAINTENANCE CIRCUITS

4.01 When switch unit trouble conditions arise, the maintenance circuits provide a means of switching the redundant portions of switch unit circuitry in and out of service to maintain a satisfactory working mode. The maintenance circuits consist of the following four circuits:

- Message controlled
- Hardware controlled
- Checking and alarm
- Power failure
- Ringing generator failure.

4.02 The control unit program contains automatic test routines for checking whether a switch unit is operating satisfactorily. The control unit may send a maintenance message to the switch unit. The switch unit accumulates the message content in the output register and transfers the message content to the maintenance circuit for control purposes. The incoming message processing for maintenance messages is described in 3.95 and 3.96. Eleven types of transfer messages may be sent; if a satisfactory working mode is not reached by message control, hardware controlled circuits may be employed to perform a ***grand slam*** operation. The grand slam operation is controlled by dc supervision of the input data link pairs from the control unit. The grand slam operation switches those portions of the switch unit whose failure is most likely to result in a total lack of response to the automatic testing routines performed by the control unit. The checking and alarms circuit provides information to the control unit concerning the maintenance status of several circuits via maintenance scan points. The power failure circuit

monitors the commercially supplied input power and, in case of failure, provides special emergency communication path connection of six prespecified lines to central office pairs.

MESSAGE CONTROLLED CIRCUITS

4.03 The message control circuits transfer redundant portions of the switch unit in and out of service to arrange a satisfactory working system. The maintenance message, which contains a 4-bit binary code located in bits 11 through 14 and duplicated in bits 19 through 22, is loaded into message translator circuits via output register bits 31 through 28 and 23 through 20. The 4-bit binary codes and their respective transfer functions are listed in Table M. Although more translations are possible from the 4-bit binary code, translation is presently provided for only 11 codes.

4.04 Fig. 53 is a block diagram of the two identical message translator circuits of TDC0 and TDC1. Each translator produces a group of one-hot-out-of-11 outputs (0001 through 1011), which may be selected one at a time for connection to the output leads M1 through M11 via the message control transfer relay S1 contacts 1 through 11, respectively. Each one-hot code is translated by a message translation gate when enabled by the inverted GTA signal from the incoming message control circuit of the associated switch control unit. Fig. 54 is the circuit of one of the 11 message translator gates G1 through G11. A given gate operates when all the input leads A through J are at ground level. The leads A through H of each gate are assigned to output register bits 20 through 23 and 28 through 31 in accordance with the arrangement outlined in Table N.

4.05 The ground level at lead J is produced by the gate message control portion of the maintenance message translator circuit when the GTA signal (on the lead P) is generated. The GTA signal produces an enable on the J lead which transfers the one-hot from the translator (L) to the register (M) where it is stored for 10 μsec when the K lead resets the register. Thus, the applicable message code signal (M1 through M11) is produced for 10 μsec by the addressed half-system.

A. Scanner Control Circuit

4.06 Fig. 55 is the scanner and switch control transfer circuit which provides the signals necessary to determine which scanner circuit and outgoing message control circuit are to be employed in the on-line mode. The transfer is initiated by the first one-hot output (code 0001) on the M1 lead which indicates a scanner transfer message and advances the binary counter C1. Changes of the C1 flip-flop output state produce changes in state for the scanner on-line (SOL) signal, the updating disable (UDS) signal, and the maintenance scan point 260 lead.

4.07 The binary counter C1 controls the state of flip-flops FF12 and FF13. C1 sets FF7 while resetting FF8 and vice versa. Thus, the

TABLE M

MAINTENANCE MESSAGE FUNCTIONS

BINARY CODE	FUNCTION
0001	Transfer scanning and outgoing message control from one switch control circuit to the other.
0010	Disable TDC0 ; enable TDC1.
0011	Disable TDC1; enable TDC0.
0100	Enable all time division control circuits.
0101	Transfer attendant lamp drive control from one time division control group to the other.
0110	Simulate a dial pulse to the test line circuit, causing a 100-msec on-hook signal on the test line scan points (71 or 255).
0111	Enable the DTA1/* output lead(s) to data transmitter 0.
1000	Enable the DTA2/* output lead(s) to data transmitter 2.
1001	Restore data transmission to normal (alternate use of data transmitters 0 and 2).
1010	Disable TDC2; enable TDC3.
1011	Disable TDC3; enable TDC2.

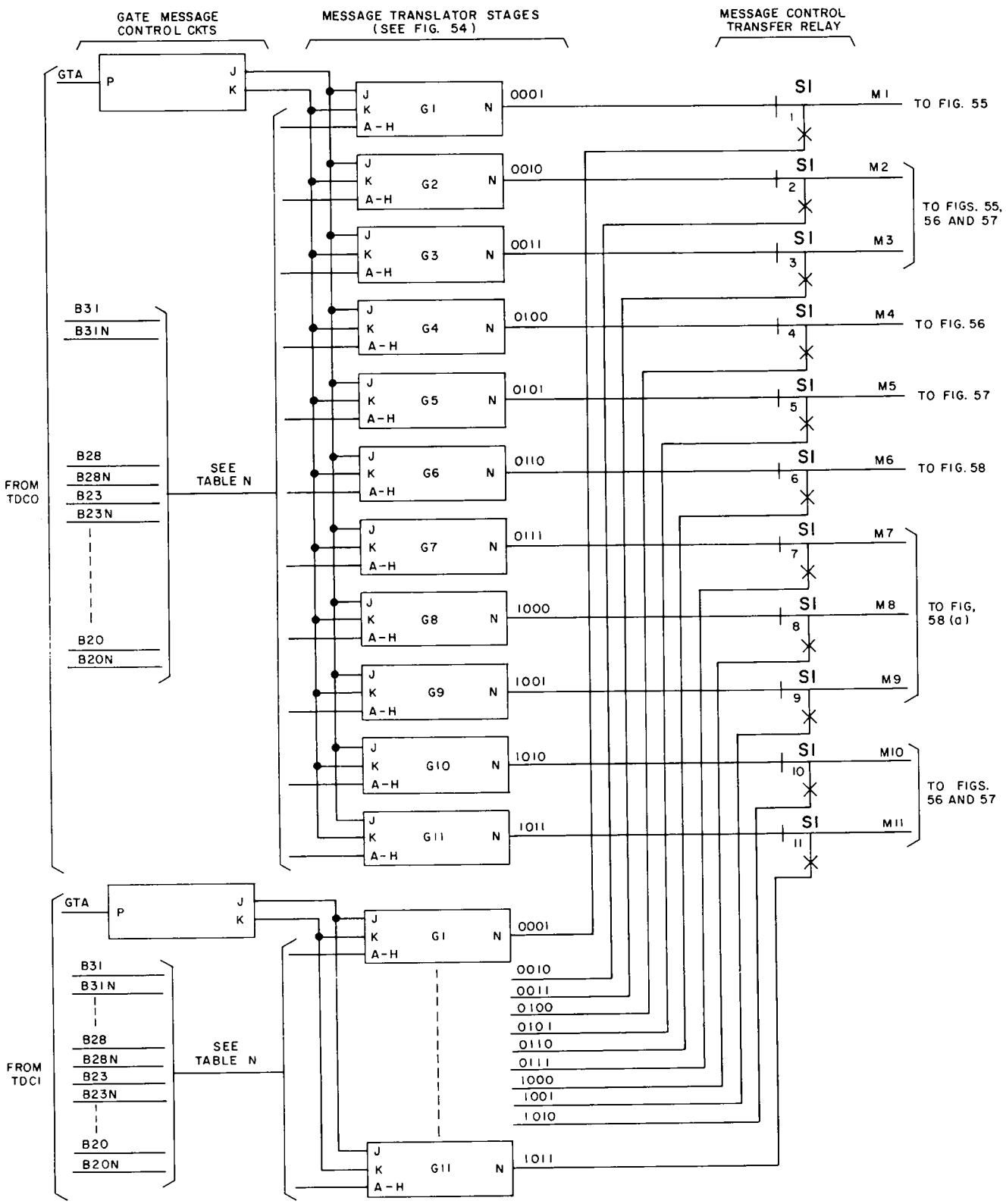


Fig. 53—Maintenance Message Translator Circuit

set-side outputs of FF13 and FF12, which are always opposite in state, produce the respective SOL/0 and SOL/1 signals to the switch control and scanner circuits. When SOL/0 is at ground level, scanner 0 and switch control 0 are on-line and able to send messages to the control unit.

4.08 When the binary counter C1 switches to a battery level output on the BC1 lead, monopulser MP2 produces a 200-msec battery level pulse on the UDS/1 lead which prevents scanner 1 from initiating a message while the last-look memory is being updated in switch control 1. Similarly, a positive transition on the other output (BC0 lead) of C1 causes MP3 to generate a 200-msec inhibit signal on the UDS/0 lead when scanner 0 goes on-line.

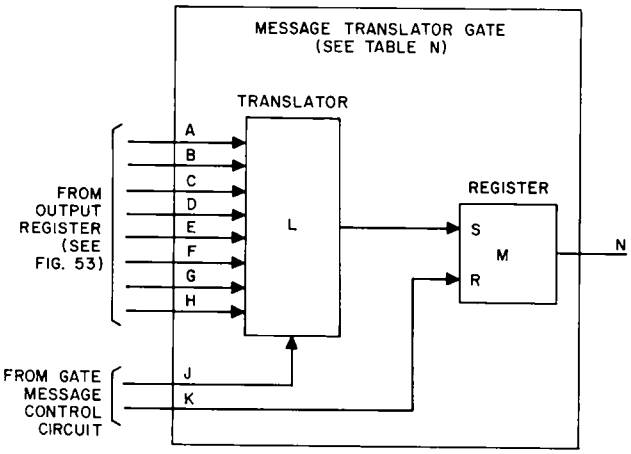


Fig. 54—Single Message Translator Gate

TABLE N

MESSAGE TRANSLATOR INPUT LEAD ARRANGEMENT

OUTPUT CODE	REGISTER	TRANSLATOR	TRANSLATOR INPUT LEADS							
N	M	L	A	B	C	D	E	F	G	H
0001	FF1	G1	B31N	B30N	B29N	B28	B23N	B22N	B21N	B20
0010	FF2	G2	B31N	B30N	B29	B28N	B23N	B22N	B21	B20N
0011	FF3	G3	B31N	B30N	B29	B28	B23N	B22N	B21	B20
0100	FF4	G4	B31N	B30	B29N	B28N	B23N	B22	B21N	B20N
0101	FF5	G5	B31N	B30	B29N	B28	B23N	B22	B21N	B20
0110	FF6	G6	B31N	B30	B29	B28N	B23N	B22	B21	B20N
0111	FF7	G7	B31N	B30	B29	B28	B23N	B22	B21	B20
1000	FF8	G8	B31	B30N	B29N	B28N	B23	B22N	B21N	B20N
1001	FF9	G9	B31	B30N	B29N	B28	B23	B22N	B21N	B20
1010	FF10	G10	B31	B30N	B29	B28N	B23	B22N	B21	B20N
1011	FF11	G11	B31	B30N	B29	B28	B23	B22N	B21	B20

4.09 The state of flip-flop FF14 controls the state of maintenance scan point number 260. An on-hook signal is indicated when FF14 is in the reset state, producing a ground level signal on scan point 260. FF14 is switched to the reset state by a battery level output signal from AND gate G13 which operates 200 msec after scanner 1 and switch control 1 go on-line, eg, FF12 is set, FF13 is reset, and the UDS/1 lead has returned to ground level. Similarly, 200 msec after FF12 is reset and FF13 is set, gate G12 operates to set FF14 which produces a battery level (off-hook) signal and indicates that scanner 0 and switch control 0 are on-line.

4.10 The state of C1 flip-flop may be changed by three additional means. The M2 and M3 leads are associated with the switch control disable circuit part of the message controlled circuits and will be described in 4.11 through 4.14. The

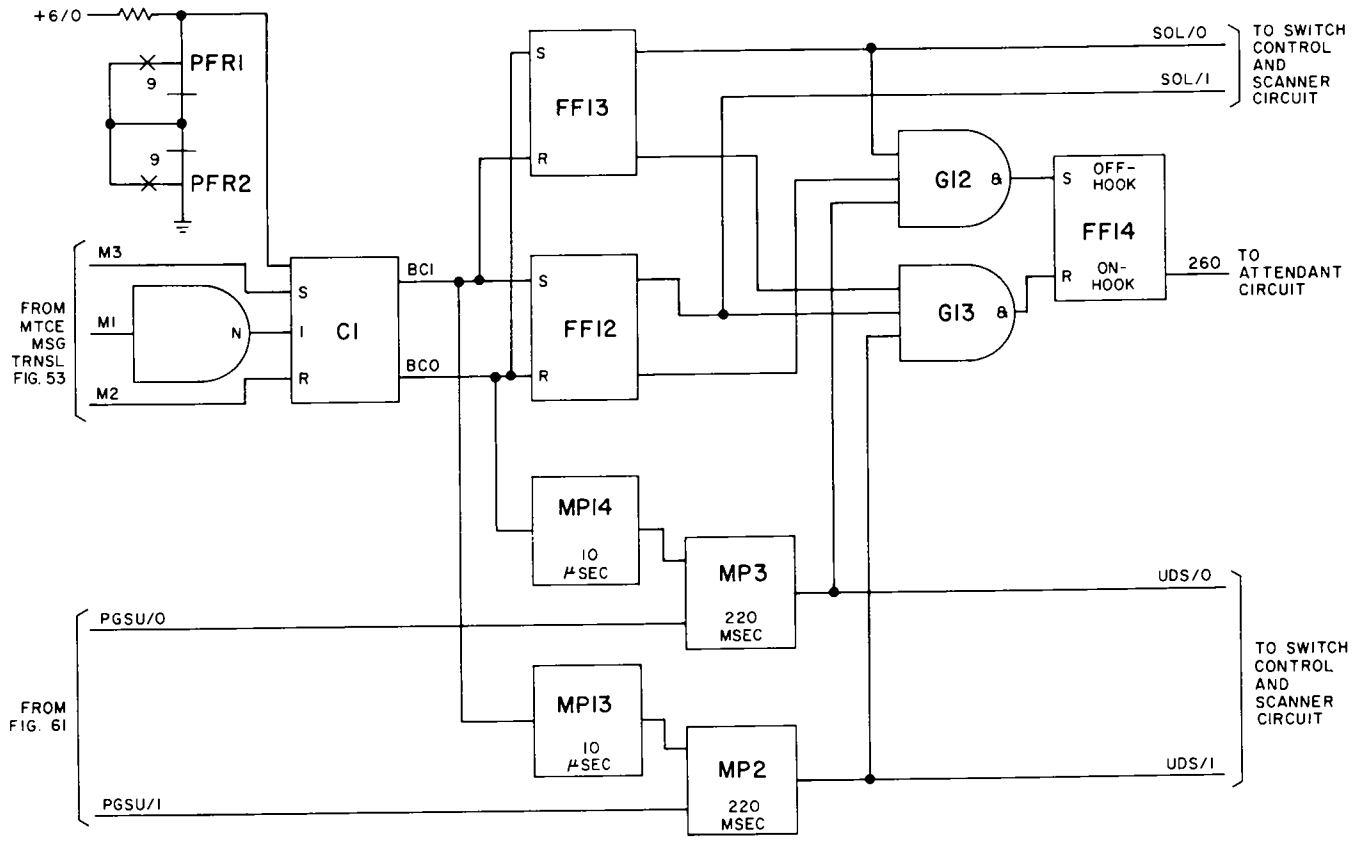


Fig. 55—Scanner and Switch Control Transfer Circuit

PFRR lead is associated with power failure circuits and will be described in 4.46 through 4.48. The lead is associated with the grand slam operation of hardware controlled circuits and will be described in 4.22 through 4.34.

B. Time Division Control Disable Circuit

4.11 Fig. 56 is the time division control disable circuit which consists of relays S6, S7, S15, and S16 operated by message codes 2, 3, 10 and 11, respectively. The relays are respectively controlled via relay drivers RD2, RD1, RD4, and RD5 by message control flip-flops FF20, FF19, FF21, and FF22. The flip-flops operate in pairs, and their input leads are arranged in a manner which allows one of a pair to be set while the other remains reset and vice versa, or allows both of a pair to be reset, but never allows both flip-flops of a pair to be set simultaneously.

4.12 A 10-μsec battery level input pulse on the M2 lead sets flip-flop FF20 to operate relays S6 and S6A which disable TDC0. Similarly, the M3 code sets FF19 to operate relays S7 and S7A which disable TDC1. The M10 code sets FF21 to operate relay S15, disabling TDC2, while the M11 code sets FF22 to operate relay S16, disabling TDC3. In addition to the flip-flop input connection scheme, continuity between the coil of relay S6 and relay driver RD2 is broken by S7 break contact 12 when relay S7 is operated. Similarly, when relay S6 is operated, break contact 12 of S6 breaks the circuit to relay S7. Thus, double protection is provided to prevent simultaneous operation of relays S6 and S7, which would result in both switch control circuits (TDC0 and TDC1) being disabled. A similar interlocking contact arrangement is provided between relays S15 and S16 to prevent disabling TDC2 and TDC3 simultaneously.

4.13 The M4 code pulse provides a reset signal for flip-flops FF19, FF20, FF21, and FF22

which causes the relays S6, S7, S15, and S16 to be in the released state. The M4 message code enables all switch control circuits. In a similar manner, all switch control circuits are also enabled by a PFRR pulse. The PFRR pulse is associated with the power failure circuits and will be described in 4.60.

4.14 Tables O and P list the action and function associated with the switch control disable operations. When neither relay is operated, both switch control circuits are enabled.

C. Attendant Transfer Circuit

4.15 The lamp control circuits are provided in duplicate for controlling the lamps on each attendant console. The message information for lamp lighting is duplicated in both switch store circuits of TDC0 and TDC1 for attendants 1 through 6 and of TDC2 and TDC3 for attendants 7 through 12. Either lamp control circuit of a pair is available for lamp lighting, but only one of the two circuits of a pair may be selected at a time.

4.16 The control unit maintenance program routinely performs tests in the operating lamp control circuit. If the applicable maintenance scan point does not respond in accordance with the maintenance program requirements, faulty operation is indicated and the control unit sends a maintenance message containing code 5 to the switch unit. The purpose of message code 5 is to transfer the attendant lamp drive control from one switch control circuit to the other.

4.17 Fig. 57 is the attendant transfer circuit. The message code 5, translated to produce a 10-μsec battery level pulse on lead M5, advances the binary counter C2. When C2 advances, the state of relay S8 is changed via relay driver RD3. Relays S9, S10, S11, S12, S13, S14, S22, S23, S24, S25, S26, S27, and S28 follow the operation of relay S8 via make contacts 4, 6, 8, and 10. Message code M2 or M10 sets C2 to transfer the lamp control to TDC1 and TDC3 while code M3 or M11 resets C2, transferring lamp control to TDC0 and TDC2. Since each relay provides 12 contacts and the contacts are schematically identical, only one set of contacts is shown. The break contact lead is designated A, the make contact lead is designated B, and the common lead is designated C. The corresponding circuit designations for the 168 contacts are listed in Table Q.

4.18 Scan point number 259 (relay S11 contact 8) is employed to indicate to the control unit which of the two switch control circuits of each pair is supplying lamp-lighting signals to the attendant consoles. A ground level (off-hook) signal on scan point 259 indicates that the attendant console lamps are controlled by TDC0 and TDC2 with all attendant transfer relays released. A battery level (on-hook) signal indicates that TDC1 and TDC3 are in control with all attendant transfer relays operated.

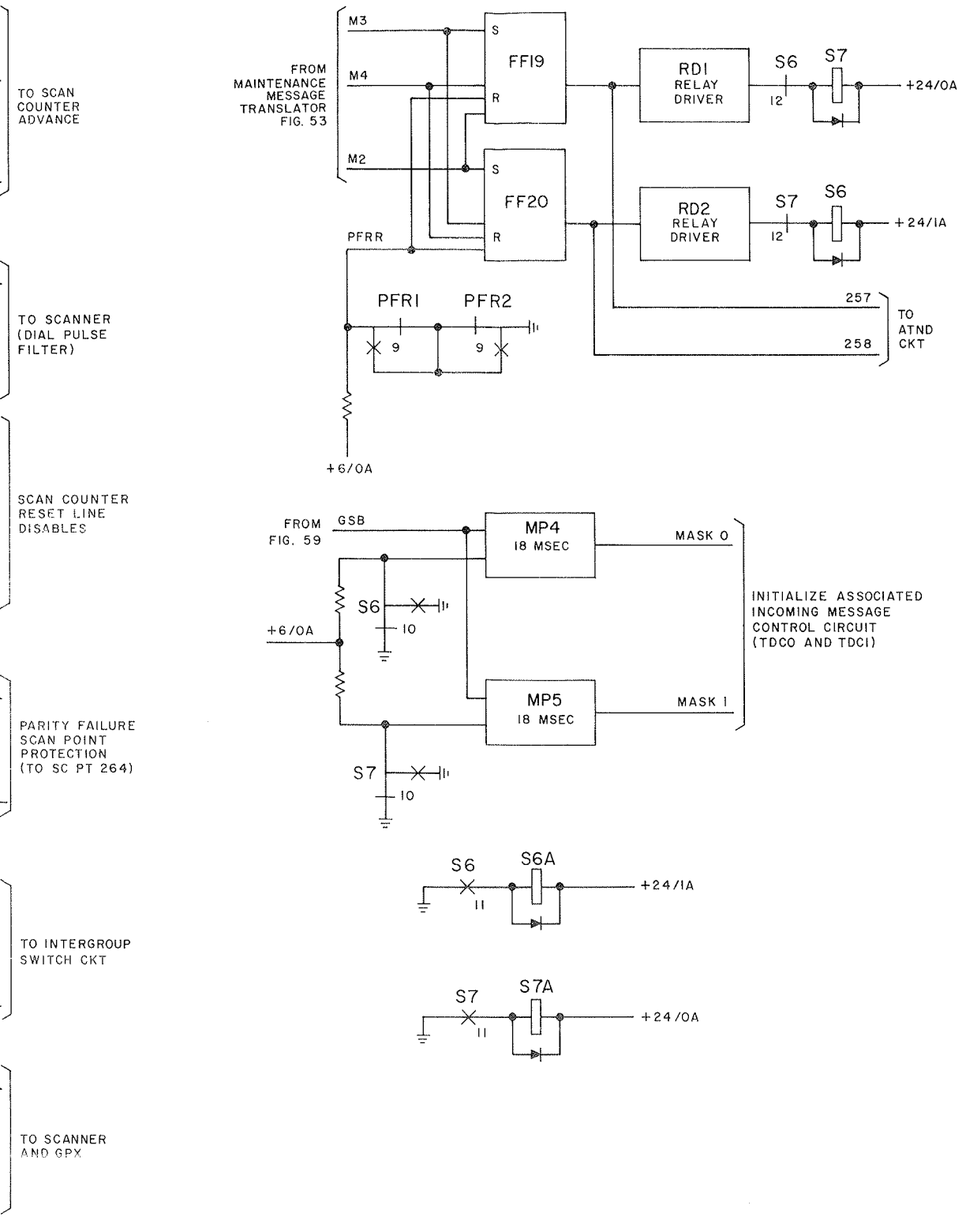
D. Dial Pulse Simulator Circuit

4.19 The dial pulse simulator circuit sends a 100-msec dial pulse to a digit trunk under test to verify the dial pulse path from the test line via the scanner circuit. The test lines are used for processing test calls set up in the switch unit by the maintenance program in the control unit. The test calls indicate whether or not the equipment being tested is operating in a satisfactory manner. If a test call is completed satisfactorily, no action will be taken. However, if a test call fails, the maintenance program will switch in various combinations of redundant equipment until the test call can be completed in a satisfactory manner. The selected combination of redundant equipment will be used until repairs can be made on defective equipment.

4.20 A typical test call consists of a talking connection between a test signal and a detector circuit with various transmission modes tested, eg, voice frequency tones and dc signals. If the detector receives the transmitted signal satisfactorily, the detector output scan point gives an off-hook indication.

4.21 In another portion of the test call involving a digit trunk circuit, the control unit may request a dial pulse simulator test via message code 6. When the switch control receives and translates message code 6, a 10-μsec battery level pulse is applied via the M6 lead to monopulser MP10 in Fig. 58. The monopulser output (MVC), which is normally at ground level, switches to battery level, producing a simulated dial pulse (on-hook state) for 100 msec. The on-hook (dial pulse) signal switches the PSB1 lead from ground (off-hook) to battery level. The PSB1 and other group numbered present state buses are combined via an OR gate in the scanner to produce corresponding ground pulse on the PSB lead to

(A) TDCO AND TDCI



(B) TDC2 AND TDC3

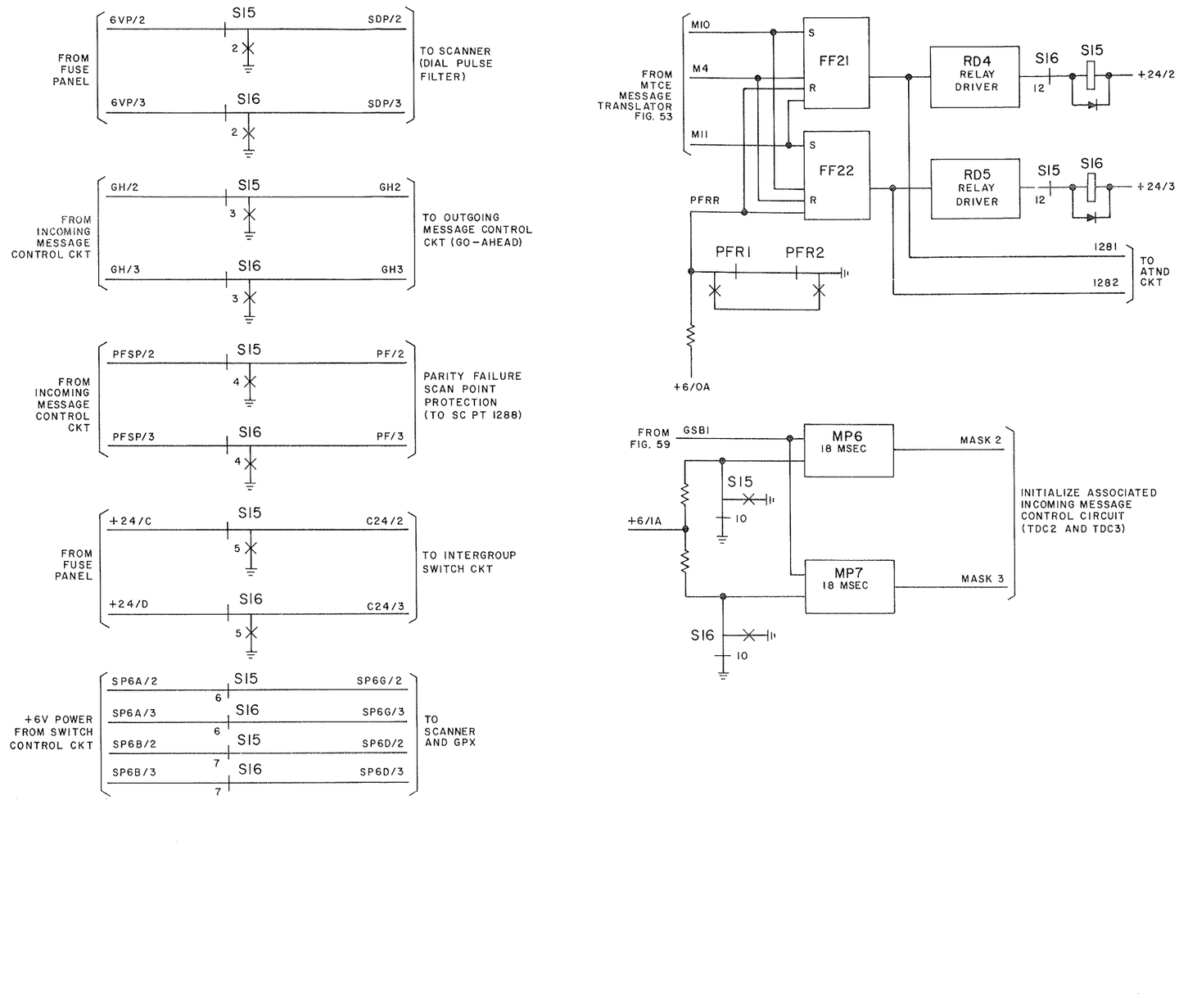
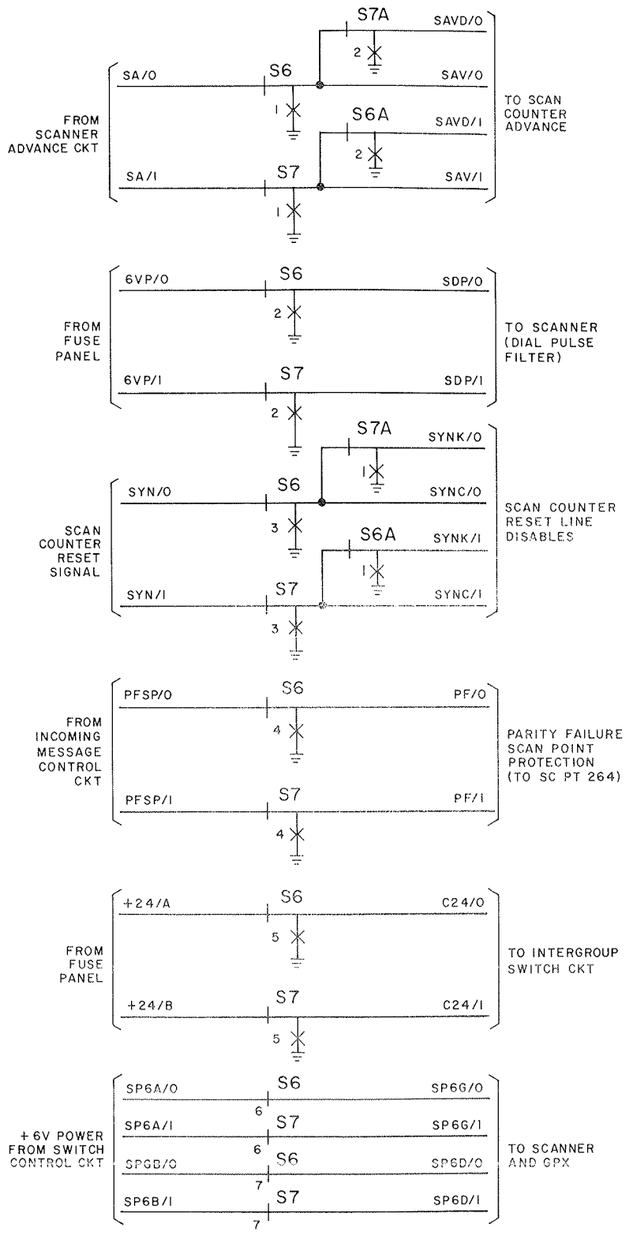
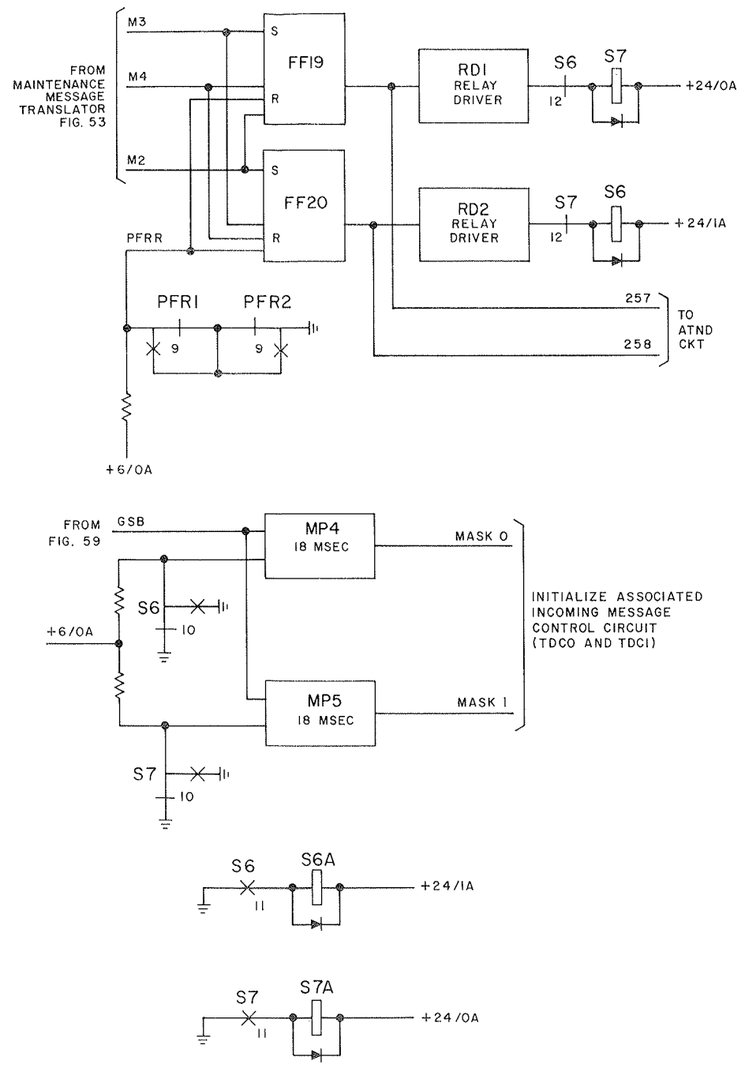


Fig. 56—Time Division Control Disable Circuit

(A) TDCO AND TDCI





(B) TDC2

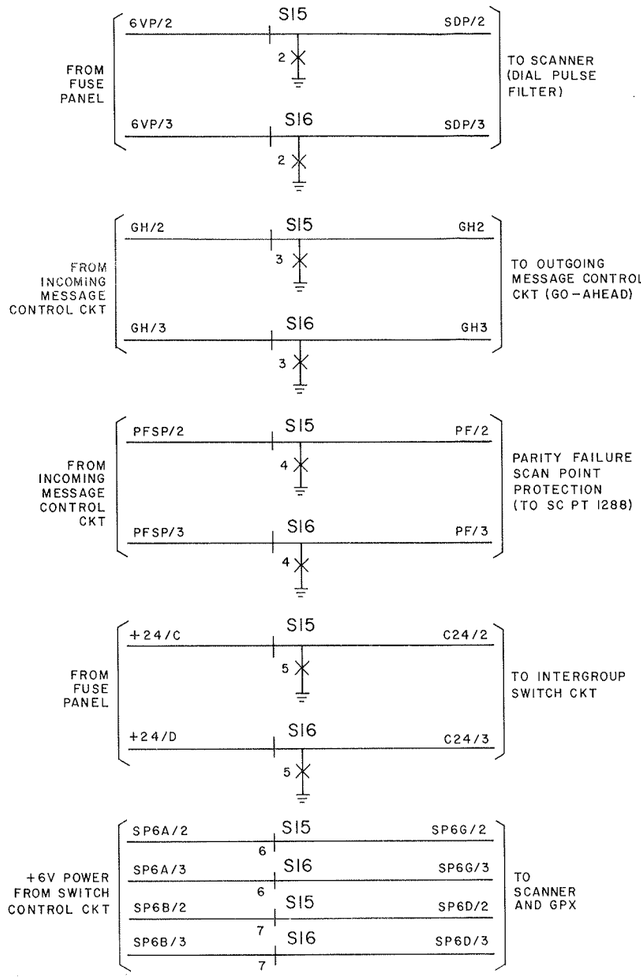


TABLE O

ACTION CAUSED BY SWITCH CONTROL DISABLE FOR TDC0 AND TDC1 (See Fig. 56)

RELAY CONTACTS S6	RELAY CONTACTS S6A	DISABLE TDC0 (RELAYS S6 AND S6A OPERATED)	RELAY CONTACTS S7	RELAY CONTACTS S7A	DISABLE TDC1 (RELAYS S7 AND S7A OPERATED)	FUNCTION
B1		Break path between lead SA/0 and leads SAV/0 and SAVD/0.	B1		Break path between lead SA/1 and leads SAV/1 and SAVD/1.	Prevents the primary scan counter of the enabled switch control and the auxiliary scan counters 2 and 3 from being advanced by the scanner circuit of the disabled switch control.
M1		Place ground on leads SAV/0 and SAVD/0.	M1		Place ground on leads SAV/1 and SAVD/1.	
	B2	Break path between leads SAV/1 and SAVD/1.		B2	Break path between leads SAV/0 and SAVD/0.	
	M2	Place ground on lead SAVD/1.		M2	Place ground on lead SAVD/0.	
B2		Break path between leads 6VP/0 and SDP/0.	B2		Break path between leads 6VP/1 and SDP/1.	Disable the dial pulse filter in scanner of the disabled switch control circuit by removing the special switched power (SDP).
M2		Place ground on lead SDP/0.	M2		Place ground on lead SDP/1.	
B3		Break path between lead SYN/0 and leads SYNC/0 and SYNK/0.	B3		Break path between lead SYN/1 and leads SYNC/1 and SYNK/1.	Prevents the primary scan counter of the enabled switch control and the auxiliary scan counters 2 and 3 from being reset by the scanner circuit of the disabled switch control.
M3		Place ground on leads SYNC/0 and SYNK/0.	M3		Place ground on leads SYNC/1 and SYNK/1.	
	B1	Break path between leads SYNC/1 and SYNK/1.		B1	Break path between leads SYNC/0 and SYNK/0.	
	M1	Place ground on lead SYNK/1.		M1	Place ground on lead SYNK/0.	
B4		Break path between leads PFSP/0 and PF/0.	B4		Break path between leads PFSP/1 and PF/1.	Prevent erroneous parity failure information in the disabled switch control circuit from producing an off-hook state at the parity failure scan point (264).
M4		Place ground on lead PF/0.	M4		Place ground on lead PF/1.	
B5		Break path between leads +24V/A and C24/0.	B5		Break path between leads +24V/B and C24/1.	Disable the intergroup switch of the disabled switch control.
M5		Place ground on lead C24/0.	M5		Place ground on lead C24/1.	
B6		Break path between leads SP6A/0 and SP6G/0.	B6		Break path between leads SP6A/1 and SP6G/1.	Disable the A portion of the common timing circuits in the disabled switch control.
B7		Break path between leads SP6B/0 and SP6D/0.	B7		Break path between leads SP6B/1 and SP6D/1.	Disable the B portion of the common timing circuits in the disabled switch control.
B10		Remove shunt to ground on input lead to MP4.	B10		Remove shunt to ground on input lead to MP5.	Generate an 18-msec battery level pulse on the MASK lead from the transient between break and make to initialize the incoming message control circuit of the disabled switch control.
M10		Place shunt to ground on input lead to MP4.	M10		Place shunt to ground on input lead to MP5.	
M11		Place ground on the ground return lead of relay coil S6A.	M11		Place ground on the ground return lead of relay coil S7A.	Operate relays S6A and S7A when relays S6 and S7 operate, respectively.
B12		Break path between RD2 and relay coil S7.	B12		Break path between RD1 and relay coil S6.	Prevent relays S6 and S7 from both being energized at the same time due to component failure in logic control circuits.

TABLE P

ACTION CAUSED BY SWITCH CONTROL DISABLE FOR TDC2 AND TDC3 (See Fig. 56)

RELAY CONTACT S15	DISABLE TDC2 (RELAY S15 OPERATED)	RELAY CONTACT S16	DISABLE TDC3 (RELAY S16 OPERATED)	FUNCTION
B2 M2	Break path between leads 6VP/2 and SDP/2. Place ground on lead SDP/2.	B2 M2	Break path between leads 6VP/3 and SDP/3. Place ground on lead SDP/3.	Disable the dial pulse filter in scanner of the disabled switch control circuit by removing the special switched power (SDP).
B3 M3	Break path between leads GH/2 and GH2. Place ground on lead GH2.	B3 M3	Break path between leads GH/3 and GH3. Place ground on lead GH3.	Prevent the incoming message control circuit of the disabled switch control from gating go-ahead bits to the outgoing message control circuit associated with the on-line scanner.
B4 M4	Break path between leads PFSP/2 and PF/2. Place ground on lead PF/2.	B4 M4	Break path between leads PFSP/3 and PF/3. Place ground on lead PF/3.	Prevent erroneous parity failure information in the disabled switch control circuit from producing an off-hook state at the parity failure scan point (1288).
B5 M5	Break path between leads +24/C and C24/2. Place ground on lead C24/2.	B5 M5	Break path between leads +24/D and C24/3. Place on lead C24/3.	Disable the intergroup switch of the disabled switch control.
B6	Break path between leads SP6A/2 and SP6G/2.	B6	Break path between leads SP6A/3 and SP6G/3.	Disable the A portion of the common timing circuits in the disabled switch control.
B7	Break path between leads SP6B/2 and SP6D/2.	B7	Break path between leads SP6B/3 and SP6D/3.	Disable the B portion of the common timing circuits in the disabled switch control.
B10 M10	Remove shunt to ground on input lead to MP6. Place shunt to ground on input lead to MP6.	B10 M10	Remove shunt to ground on input lead to MP7. Place shunt to ground on input lead to MP7.	Generate an 18-msec battery level pulse on the MASK lead from the transient between break and make to initialize the incoming message control circuit of the disabled switch control.
B12	Break path between RD4 and relay coil S15.	B12	Break path between RD5 and relay coil S16.	Prevent relays S15 and S16 from both being energized at the same time due to component failure in the logic control circuits.

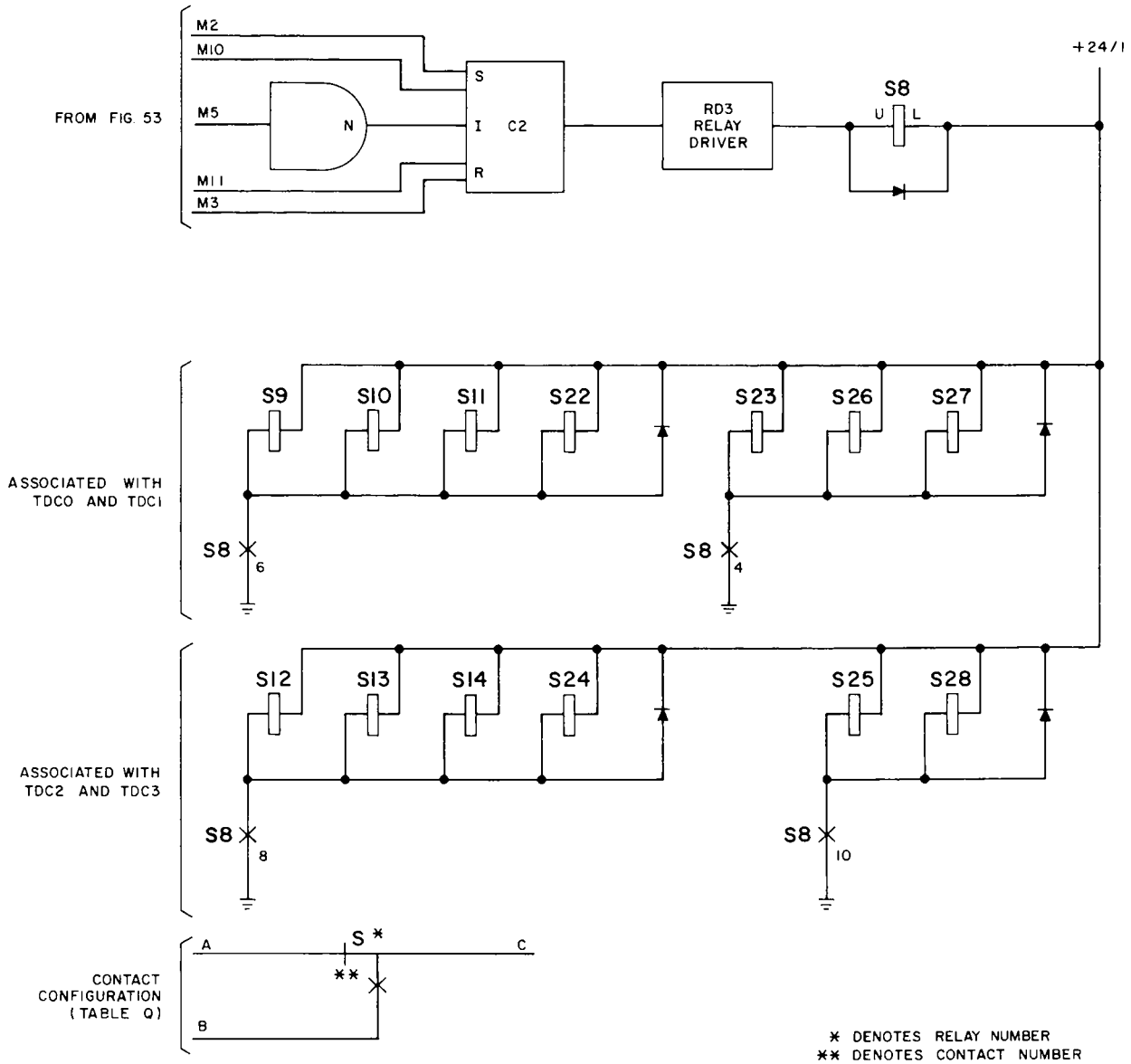


Fig. 57—Attendant Transfer Circuit

the digit trunk circuit. The digit trunk circuit sends scan inhibit pulses to the scanner and converts the on-hook pulse to a tone burst which is sent to the control unit if the path is satisfactory.

E. Data Transmitter Control Circuit

4.22 Fig. 58A is the data transmitter control circuit which employs two flip-flops, FF17 and FF18, to provide transfer circuits for isolating a trouble between the control unit and switch unit. The trouble isolation is accomplished by use of a maintenance message which restricts the outgoing message control circuit to use only one pair for data transmission. Thus, a trouble condition may be isolated to a particular data transmitter or data link pair.

4.23 Normal operation of a 3- or 4-TDC switch unit entails the alternate use of data transmitters 0 and 2. Data transmitter 1 (Fig. 58A) is a spare and, under control of the grand slam relays GSR1 and GSR2, will replace either data transmitter 0 or data transmitter 2. When data

TABLE Q

ATTENDANT TRANSFER RELAY CONTACT ARRANGEMENT (See Fig. 57)

RELAY	LEAD DESIG-NATION	CONTACT NUMBER											
		1	2	3	4	5	6	7	8	9	10	11	12
S8	A	A04M/0	LPHG/0	LPHH/0	—	G/0	—	H/0	—	—	—	—	—
	B	A04M/1	LPHG/1	LPHH/1	Ground	G/1	Ground	H/1	Ground	—	Ground	—	—
	C	A04M01	LPHG01	LPHH01	S23, S26, S27	G01	S9, S10, S11, S22	H01	S12, S13, S14, S24	—	S25, S28	—	—
S9	A	KAB/0	SAB/0	DAB/0	CFA/0	RDPA/0	ESDA/0	PBNA/0	CWA/0	LPHA/0	LPHB/0	KCD/0	SCD/0
	B	KAB/1	SAB/1	DAB/1	CFA/1	RDPA/1	ESDA/1	PBNA/1	CWA/1	LPHA/1	LPHB/1	KCD/1	SCD/1
	C	KAB01	SAB01	DAB01	CFA01	RDPA01	ESDA01	PBNA01	CWA01	LPHA01	LPHB01	KCD01	SCD01
S10	A	DCD/0	CFB/0	RDPB/0	B3A0	B3NA0	B14A0	B14NA0	A11M/0	A12M/0	A13M/0	A14M/0	A21M/0
	B	DCD/1	CFB/1	RDPB/1	B3A1	B3NA1	B14A1	B14NA1	A11M/1	A12M/1	A13M/1	A14M/1	A21M/1
	C	DCD01	CFB01	RDPB01	TSA01	TSNA01	TMA01	TMNA01	A11M01	A12M01	A13M01	A14M01	A21M01
S11	A	A22M/0	A23M/0	A24M/0	A31M/0	A32M/0	A33M/0	A34M/0	Ground	ESDB/0	PBNB/0	CWS/0	B19A0
	B	A22M/1	A23M/1	A24M/1	A31M/1	A32M/1	A33M/1	A34M/1	+6/0A	ESDB/1	PBNB/1	CWS/1	B19A1
	C	A22M01	A23M01	A24M01	A31M01	A32M01	A33M01	A34M01	259	ESDB01	PBNB01	CWS01	TSB01
S22	A	B19NA0	B30A0	B30NA0	LPHC/0	LPHD/0	LPHE/0	LPHF/0	B2/0	B2N/0	B7N/0	B18/0	B18N/0
	B	B19NA1	B30A1	B30NA1	LPHC/1	LPHD/1	LPHE/1	LPHF/1	B2/1	B2N/1	B7N/1	B18/1	B18N/1
	C	TSNB01	TMB01	TMNB01	LPHC01	LPHD01	LPHE01	LPHF01	B201	B2N01	B7N01	B1801	B18N01
S23	A	B23N/0	E/0	F/0	B9A0	G15/0	BVTN/0	B1/0	B1N/0	B4N/0	B5/0	B5N/0	B7/0
	B	B23N/1	E/1	F/1	B9A1	G15/1	BVTN/1	B1/1	B1N/1	B4N/1	B5/1	B5N/1	B7/1
	C	B23N01	E01	F01	B901	G1501	BVTN01	B101	B1N01	B4N01	B501	B5N01	B701
S26	A	B8/0	B10/0	B11/0	B12/0	B13/0	B15/0	B16/0	B17/0	B17N/0	B20N/0	B21/0	B21N/0
	B	B8/1	B10/1	B11/1	B12/1	B13/1	B15/1	B16/1	B17/1	B17N/1	B20N/1	B21/1	B21N/1
	C	B801	B1001	B1101	B1201	B1301	B1501	B1601	B1701	B17N01	B20N01	B2101	B21N01
S27	A	B23/0	B24/0	B25/0	B26/0	B27/0	B28/0	B29/0	B31/0	B32/0	A01M/0	A02M/0	A03M/0
	B	B23/1	B24/1	B25/1	B26/1	B27/1	B28/1	B29/1	B31/1	B32/1	A01M/1	A02M/1	A03M/1
	C	B2301	B2401	B2501	B2601	B2701	B2801	B2901	B3101	B3201	A01M01	A02M01	A03M01
S12	A	KAB/2	SAB/2	DAB/2	CFA/2	RDPA/2	ESDA/2	PBNA/2	CWB/2	LPHA/2	LPHB/2	KCD/2	SCD/2
	B	KAB/3	SAB/3	DAB/3	CFA/3	RDPA/3	ESDA/3	PBNA/3	CWB/3	LPHA/3	LPHB/3	KCD/3	SCD/3
	C	KAB23	SAB23	DAB23	CFA23	RDPA23	ESDA23	PBNA23	CW23	LPHA23	LPHB23	KCD23	SCD23
S13	A	DCD/2	CFB/2	RDPB/2	B3E2	B3NE2	B14E2	B14NE2	A11M/2	A12M/2	A13M/2	A14M/2	A21M/2
	B	DCD/3	CFB/3	RDPB/3	B3E3	B3NE3	B14E3	B14NE3	A11M/3	A12M/3	A13M/3	A14M/3	A21M/3
	C	DCD23	CFB23	RDPB23	TSA23	TSNA23	TMA23	TMNA23	A11M23	A12M23	A13M23	A14M23	A21M23

TABLE Q

ATTENDANT TRANSFER RELAY CONTACT ARRANGEMENT (See Fig. 57) (Cont)

RELAY	LEAD DESIG-NATION	CONTACT NUMBER											
		1	2	3	4	5	6	7	8	9	10	11	12
S14	A	A22M/2	A23M/2	A24M/2	A31M/2	A32M/2	A33M/2	A34M/2	ESDB/2	PBNB/2	—·—	B19E2	B19NE2
	B	A22M/3	A23M/3	A24M/3	A31M/3	A32M/3	A33M/3	A34M/3	ESDB/3	PBNB/3	--- -	B19E3	B19NE3
	C	A22M23	A23M23	A24M23	A31M23	A32M23	A33M23	A34M23	ESDB23	PBNB23	··—	TSB23	TSNB23
S24	A	B30E2	B30NE2	LPHC/2	LPHD/2	——	LPHE/2	LPHF/2	B2/2	B2N/2	B7N/2	B18/2	B18N/2
	B	B30E3	B30NE3	LPHC3 /	LPHD/3	· —	LPHE/3	LPHF/3	B2/3	B2N/3	B7N/3	B18/3	B18N/3
	C	TMB23	TMBN23	LPHC23	LPHD23	·——	LPHE23	LPHF23	B223	B2N23	B7N23	B1823	B18N23
S25	A	B23N/2	E/2	F/2	G/2	——	B1/2	B1N/2	- —	B1/2	B5/2	B5N/2	B17/2
	B	B23N/3	E/3	F/3	G/3	-- ·	B1/3	B1N/3	——	B4/3	B5/3	B5N/3	B17/3
	C	B23N23	E23	F23	G23	—·-	B123	B1N23	— ·	B423	B523	B5N23	B1723

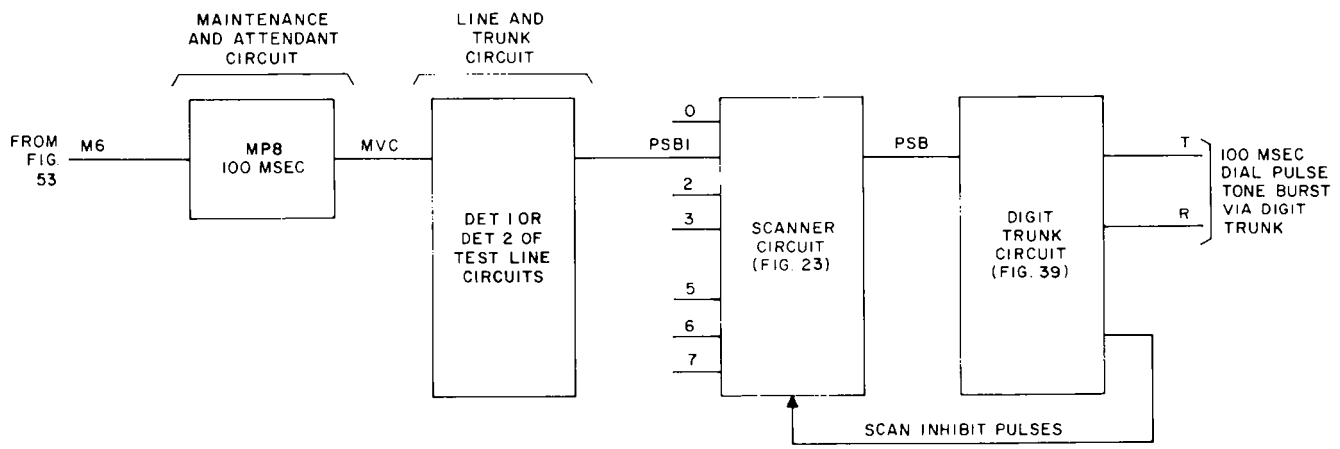
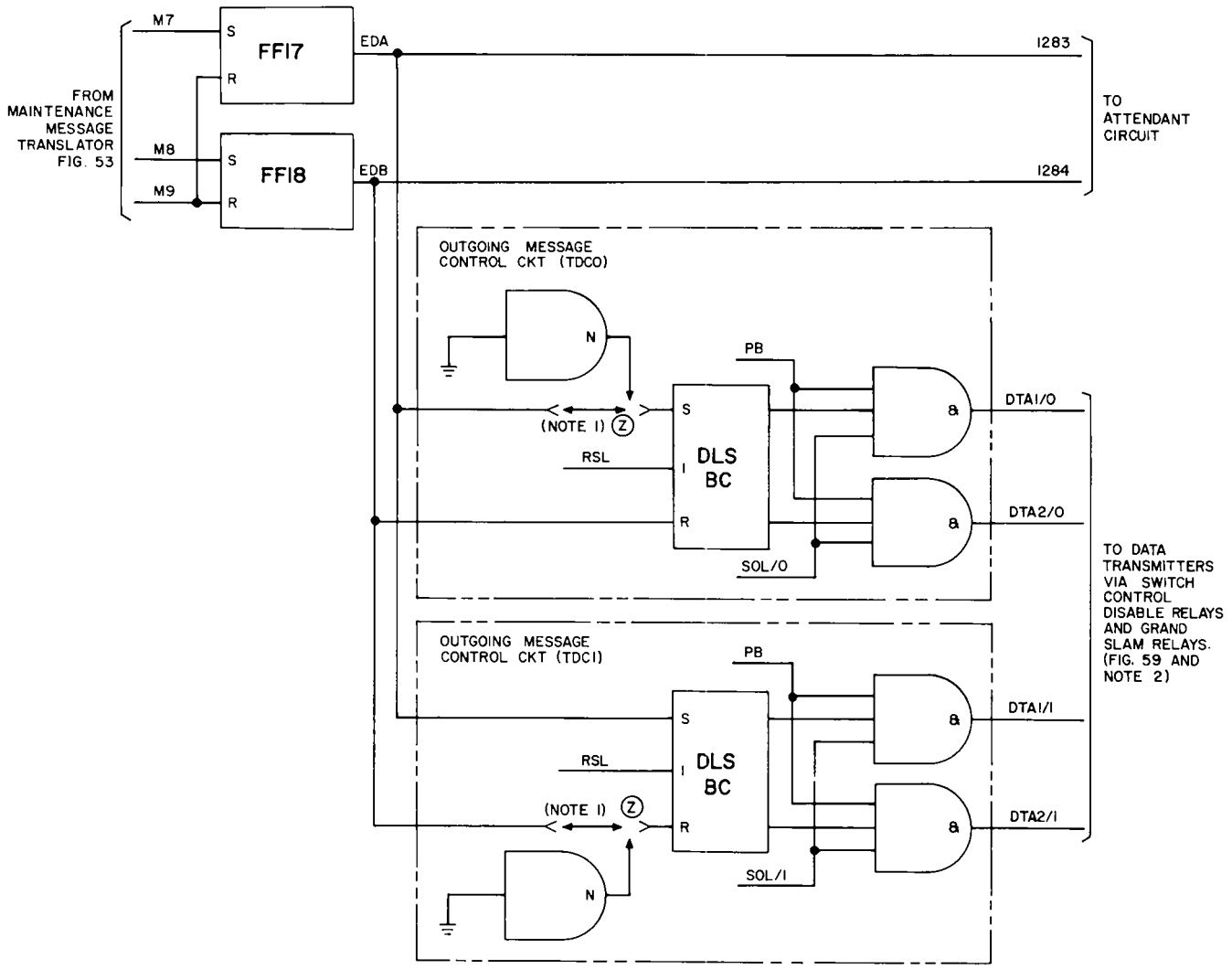


Fig. 58—Dial Pulse Simulator Circuit

transmitter 1 replaces data transmitter 0, the pair normally used to connect digit trunk 2 to the control unit is used to transmit data from data transmitter 1 to the control unit. When data transmitter 1 replaces data transmitter 2, the pair which normally connects digit trunk 14 to the control unit is used to transmit data from data transmitter 1 to the control unit.

4.24 The FF17 and FF18 flip-flops (Fig. 58A) are normally in the reset state providing ground level signals (on-hook) to the maintenance scan points 1283 and 1284 via the EDA and EDB leads, respectively. When both EDA and EDB are at ground level, the on-line switch control (TDC0 or TDC1) will send messages alternately via data transmitter 0 over outgoing data link pair 1 and



NOTES:

1. OPTION (Z) IS USED WHEN ONLY TDCO AND TDCI ARE PROVIDED.
   OPTION (Z) SUBSTITUTES A PERMANENT BATTERY LEVEL SIGNAL TO THE SET SIDE INPUT OF THE DLS BINARY COUNTER OF TDCO AND TO THE RESET SIDE INPUT OF THE DLS BINARY COUNTER OF TDCI.
2. OUTPUT LEAD DESTINATIONS FOR OUTGOING MESSAGE CONTROL CIRCUIT.

OUTPUT		INPUT LEAD TO DATA TRANSMITTER		
UNIT	LEAD	MSG. CONTROL	GSRI *	GSRZ *
TDCO	DTA1/O	DATO/O	DATO/1	DATO/O
	DTA2/O	DATO/2	DATO/2	DATO/1
TDCI	DTA1/1	DATI/O	DATI/1	DATI/O
	DTA2/1	DATI/2	DATI/2	DATI/1

* GRAND SLAM RELAYS GSRI AND GSR2 ARE HARDWARE CONTROLLED AND ARE ILLUSTRATED IN FIG. 59.

Fig. 58A—Data Transmitter Control Circuit

via data transmitter 2 over outgoing data link pair 3.

4.25 Message code M7 produces a battery level EDA signal which sets the DLS binary counters in both outgoing message control circuits. When the DLS binary counters are set, the on-line switch control is restricted to sending messages via data transmitter 0. An off-hook signal on the associated scan point 1283 causes a message to be sent to the control unit via the selected data link pair. Message code M8 similarly produces the EDB signal which resets both DLS flip-flops. When the DLS binary counters are reset, message transmission is restricted to data transmitter 2, and a scan point 1284 off-hook message is sent to the control unit. Successful receipt of the off-hook data transmitter control message at the control unit verifies that the selected data link is operating satisfactorily. Message code M9 produces ground level signals on the EDA and EDB leads, restoring the outgoing message control circuits to the normal alternate transmission of messages. The reset scan logic (RSL) signal which resets the outgoing message control circuit at the end of each message transmission also advances the DLS binary counter. Thus, the DLS binary counter enables the present state bit (PB) to be sent alternately via the DTA1 and DTA2 leads of the on-line message control circuit (where SOL lead is at ground level).

HARDWARE CONTROLLED CIRCUITS

4.26 The hardware controlled circuits provide a dc controlled transfer when the normal method, message control, cannot be employed to produce a satisfactory working system. A dc control current is normally sent with the audio frequency signal via each of the two data link pairs from the control unit to the switch unit. A relay is employed to supervise the presence of dc current on each of the data link pairs. If one of the supervisory relays releases, a ***grand slam*** operation is initiated.

4.27 The grand slam operation results in the following:

(a) An exchange of physical data link pairs used between the switch unit and the control unit.

(b) The data transmitter and receiver are replaced by spare units.

(c) The basic clock oscillator circuit switches to another oscillator.

(d) A transfer of control by the common timing circuits from one switch control to the other.

(e) A transfer of maintenance message control from one switch control to the other.

4.28 Fig. 59 is the grand slam circuit. Relays GSR1 and GSR2, respectively, supervise incoming data link pairs numbered 1 and 3. If either of the dc circuits is opened by control unit command or within the data link, the applicable grand slam relay releases to initiate a grand slam operation. When ***either*** grand slam relay (not both) releases, a ground return path is completed to associated grand slam control relays. Control relays S1, S2, S3, S4, S5, S17, S18, and S20 operate when the GSR1 relay releases. Control relays S1, S2, S3, S4, S5, S17, S19, and S21 operate when the GSR2 relay releases. It should be noted that none of these 10 control relays will operate if both grand slam relays (GSR1 and GSR2) are simultaneously in the released state.

A. Grand Slam No. 1

4.29 A grand slam No. 1 occurs when relay GSR1 releases if GSR2 remains operated. When relay S18 operates due to the release of the GSR1 relay, the normal path via break contacts 1 and 2 is broken between the incoming data link pair No. 1 TIDL1 and RIDL1 and data receiver 0 input leads RT/0 and RR/0, respectively. Also, the normal path via break contacts 5 and 6 is broken between digit trunk pair No. 1 and digit trunk circuit No. 1. The incoming data link pair becomes connected to digit trunk circuit No. 1 via make contacts 1 and 2. The spare data receiver No. 1 input leads RT/1 and RR/1 become connected via make contacts 5 and 6 to digit trunk pair No. 1 leads TTK1 and RTK1, respectively.

4.30 Relay S18 similarly removes data transmitter No. 0 from service and transfers the outgoing data link pair No. 1 to digit trunk circuit No. 2 via contacts 7 and 8. Contacts 11 and 12 isolate digit trunk circuit No. 2 from the associated digit trunk pair No. 2 and connect the spare data transmitter No. 1 to digit trunk pair No. 2.

4.31 Relays S18 and S20 provide eight contacts which transfer the incoming and outgoing

message control circuits of TDC0 and TDC1 from data receiver and transmitter No. 0 to the spare data receiver and transmitter No. 1. The message control input leads BP0, D0, and DM0 are transferred from the normal data receiver No. 0 outputs to ground level. The normally grounded message control input leads BP1, D1, and DM1 are transferred to the output connections of the spare data receiver 1. The message control output leads DTA1/0 and DTA1/1 are transferred from data transmitter No. 0 to the spare data transmitter No. 1.

B. Grand Slam No. 2

4.32 A grand slam No. 2 occurs when relay GSR2 releases if GSR1 remains operated. When relay S19 operates due to the release of the GSR2 relay, the incoming data link pair No. 3, normally connected to data receiver No. 2, is transferred by contacts 3 and 4 to digit trunk circuit No. 13. Digit trunk pair No. 13 is isolated from digit trunk circuit No. 13 by contacts 1 and 2 and is transferred to the spare data receiver No. 1.

4.33 Relay S19 similarly removes data transmitter No. 2 from service and transfers the outgoing data link pair No. 3 to digit trunk circuit No. 14 via contacts 11 and 12. Contacts 7 and 8 isolate digit trunk circuit No. 14 from the associated digit trunk pair No. 14 and connect the spare data transmitter No. 2 to digit trunk pair No. 14.

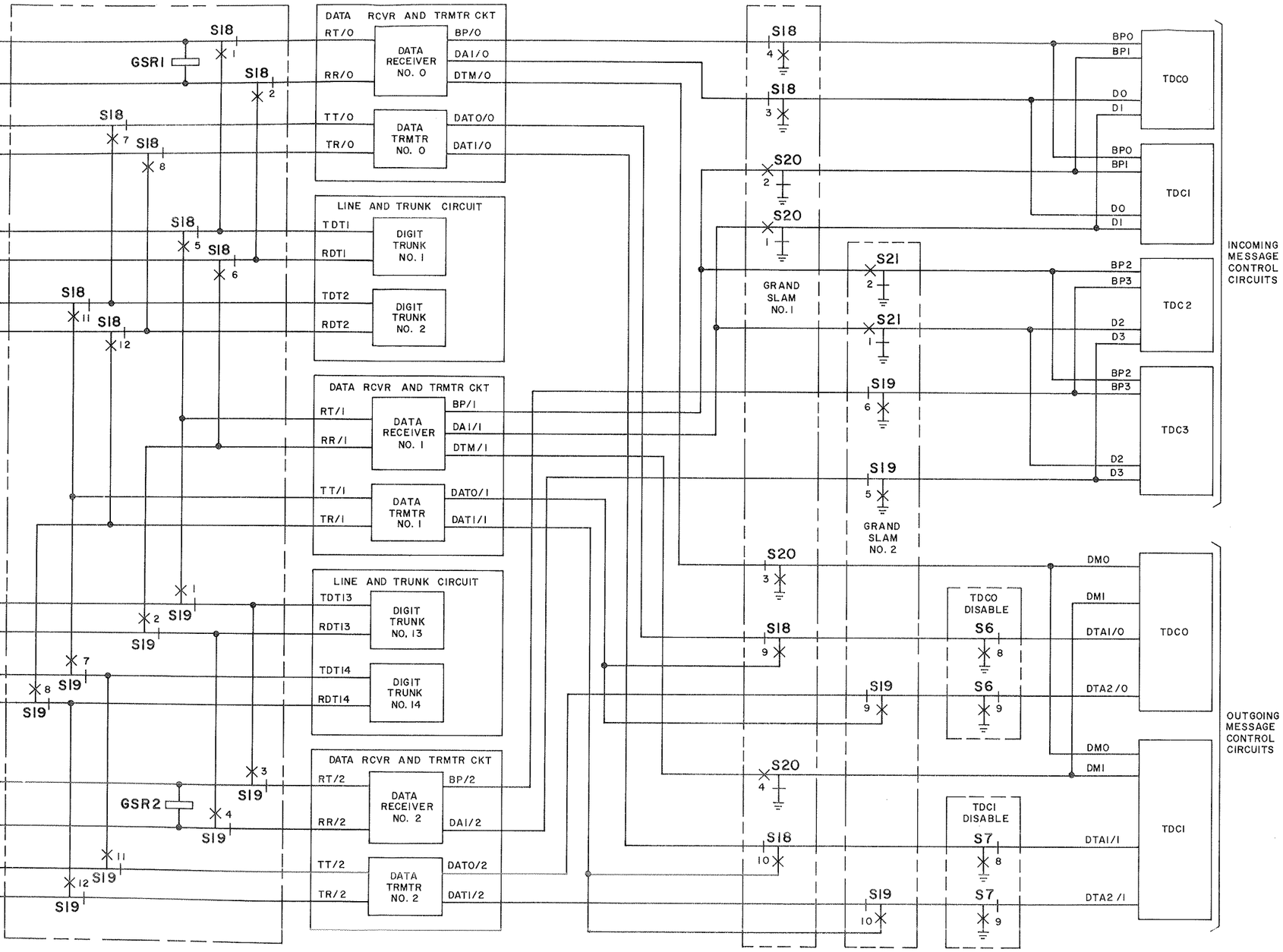
4.34 Relays S19 and S21 provide six contacts which transfer the incoming message control circuits of TDC2 and TDC3, and outgoing message control circuits of TDC0 and TDC1 from data receiver and transmitter No. 2 to the spare data receiver and transmitter No. 1. The message control input leads BP3 and D3 are transferred from the normal data receiver No. 2 to ground level. The normally grounded message control input leads, BP2 and D2, are transferred to the output connections of the spare data receiver No. 1. The message control output leads DTA2/0 and DTA2/1 are transferred from data transmitter No. 2 to the spare data transmitter No. 1.

C. Grand Slam Common Control

4.35 Grand slam common control relays S1 through S5 plus S17, as described in 4.28, are operated when either of the grand slam relays (GSR1 or GSR2) releases. Relay GSR1 contact 4 is an early break-make contact which normally provides a ground on the GSB lead. The GSR2 relay contact 4 similarly provides a normal ground on the GSB1 lead. The GSB or GSB1 lead may rise to battery level via it associated resistor during the transition between the break and make conditions. The GSB and GSB1 signals prevent false signals of operation during the operating time of relays S1 through S5 and S17 through S21. The series configuration of relay contacts (S1 through S5 plus S17) ensures that all the relays are operated to produce an off-hook grand slam verification signal to maintenance scan point 261. The battery level verification signal is inhibited via a ground on the GSPC lead for 320 msec after either one of the grand slam relays is released.

4.36 Fig. 60 is the grand slam verification delay circuit which produces the inhibit signal for scan point 261. The inhibit signal is generated in part of the scanner and switch control circuit when the GSB or GSB1 signal sets flip-flop FF23. When FF23 is set, scan point 261 is clamped to ground level (on-hook) via the GSPC lead. The GSPC lead remains at ground level until FF23 is reset 320 msec later at the end of the 220 msec UDSN pulse generated by monopulser MP2 or MP3 from the UDS/0 or UDS/1 pulse. The PGSU/0 or PGSU/1 pulse from the clock inhibit and transfer circuit starts the UDS/0 or UDS/1 pulse, respectively, 100 msec after the GSB or GSB1 signal. Thus, scan point 261 is enabled to send an (off-hook) grand slam verification message 320 msec after the GSB or GSB1 signal is generated (when either grand slam relay releases).

4.37 Switch control 0 normally controls the synchronizing of the time slot counters and clock circuits in all the switch control circuits. All of the A counters in a switch unit must be synchronized, all the B counters must also be synchronized, and the ring counters of all clock circuits must be synchronized. During a grand slam operation, the control for synchronizing these counters is transferred to switch control 1. Relay S2 contacts 3 and 4 (Fig. 59) supply the jam counter A (JCA/0 or JCA/1) signals to OR gates in all A time slot counters. The relay contacts are arranged so that when one OR gate input lead is active, the other lead is always grounded. Relay S2 contacts 5 and 6 similarly transfer the synchronization for B time slot counters from switch control 0 to switch control 1. The CSYN0 and CSYN1 leads connecting to OR gates in TDC0 and TDC1 supply the P6N synchronizing signal source from clock 0



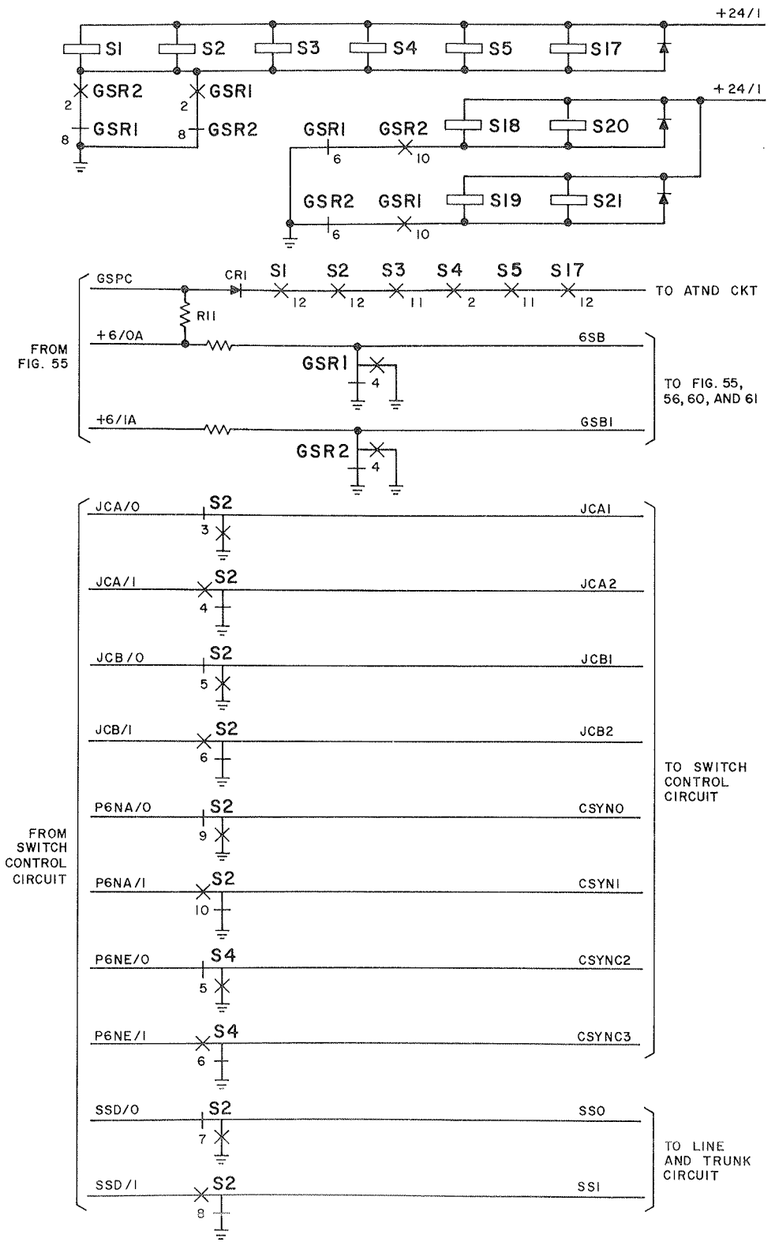
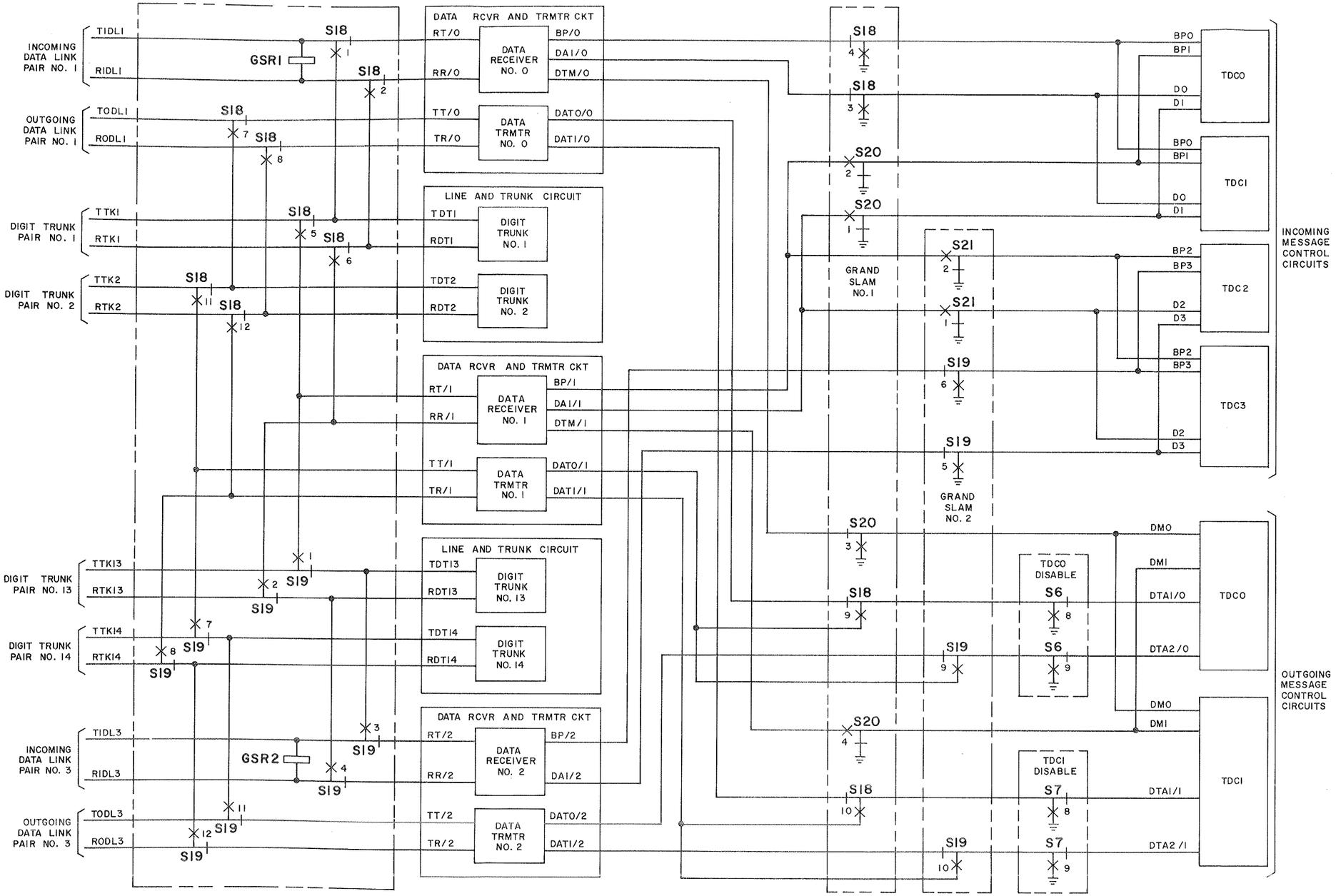


Fig. 59—Grand Slam Circuit


INCOMING DATA LINK PAIR NO. 1
TIDL1
RIDL1
GSR1
S18
1
2
OUTGOING DATA LINK PAIR NO. 1
TODL1
RODL1
7
8
DIGIT TRUNK PAIR NO. 1
TTK1
RTK1
5
6
DIGIT TRUNK PAIR NO. 2
TTK2
RTK2
11
12
DATA RCVR AND TRMTR CKT
RT/0
RR/0
DATA RECEIVER NO. 0
BP/0
DAI/0
DTM/0
TT/0
TR/0
DATA TRMTR NO. 0
DATO/0
DATI/0
LINE AND TRUNK CIRCUIT
TDT1
RDT1
DIGIT TRUNK NO. 1
TDT2
RDT2
DIGIT TRUNK NO. 2
DATA RCVR AND TRMTR CKT
RT/1
RR/1
DATA RECEIVER NO. 1
BP/1
DAI/1
DTM/1
TT/1
TR/1
DATA TRMTR NO. 1
DATO/1
DATI/1
LINE AND TRUNK CIRCUIT
TDT13
RDT13
DIGIT TRUNK NO. 13
TDT14
RDT14
DIGIT TRUNK NO. 14
DATA RCVR AND TRMTR CKT
RT/2
RR/2
DATA RECEIVER NO. 2
BP/2
DAI/2
TT/2
TR/2
DATA TRMTR NO. 2
DATO/2
DATI/2
S19
S20
S21
GRAND SLAM NO. 1
GRAND SLAM NO. 2
TDCO DISABLE
TDCI DISABLE
S6
S7
TDC0
TDC1
TDC2
TDC3
BPO
BPI
DO
DI
BP2
BP3
D2
D3
DMO
DMI
DTAI/0
DTA2/0
DTAI/1
DTA2/1
INCOMING MESSAGE CONTROL CIRCUITS
OUTGOING MESSAGE CONTROL CIRCUITS
FROM FIG. 55
FROM SWITCH CONTROL CIRCUIT

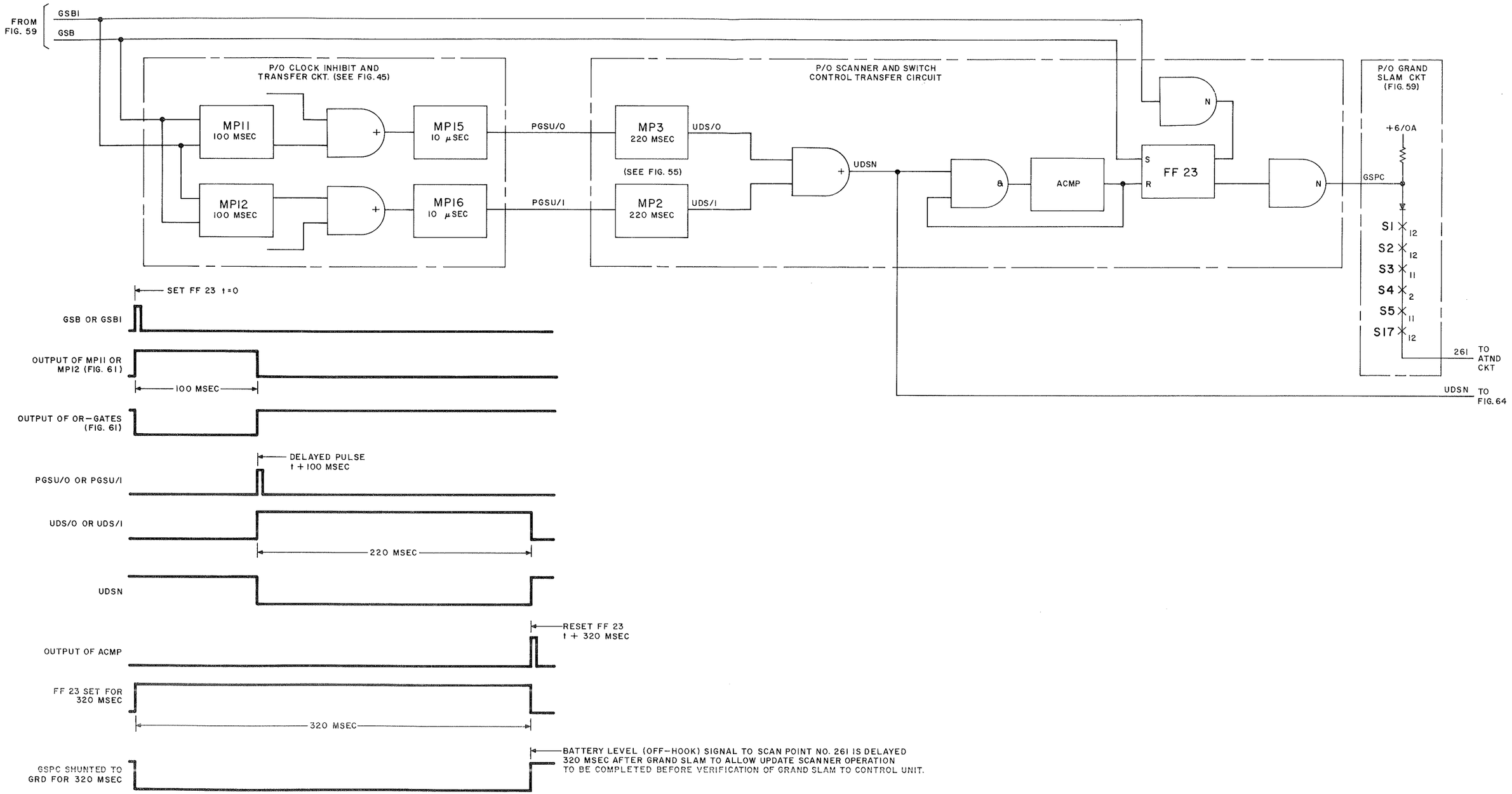


Fig. 60—Grand Slam Verification Delay Circuit

or clock 1 via relay S2 contacts 9 and 10. The CSYN2 and CSYN3 leads similarly supply the P6N signal from clock 0 or clock 1 via relay S4 contacts 5 and 6 to OR gates in TDC2 and TDC3.

4.38 The SSD/0 lead from switch control 0 normally supplies ***silent scan pulses*** via relay S2 break contact 7 and the SS0 lead to the line and trunk circuit while the SS1 lead is grounded by relay S2 break contact 8. The grand slam operation produces silent scan pulses from switch control 1 on the SS1 lead while the SS0 lead is grounded.

4.39 Relay S1 operates as shown in Fig. 53 in the grand slam operation to transfer the source of the 11 message controlled maintenance leads M1 through M11 from TDC0 to TDC1. Thus, the different maintenance control message route through the duplicate path may afford successful maintenance control when the primary maintenance control circuit has failed.

4.40 The GSB and GSB1 leads are applied to the clock inhibit and transfer circuit (Fig. 61), which produces via monopulsers MP11 and MP12 battery level pulse outputs on the CKI/0, CKI/1, CKI/2, and CKI/3 leads. The outputs of the same monopulsers, MP12 and MP13, are applied via the OR gates and the monopulsers, MP15 and MP16, to produce 10-μsec pulses delayed by 100 msec (PGSU/0 and PGSU/1).

4.41 Switch control 0 clock circuit normally controls the time division transmission timing for switch unit operation. During a grand slam operation, the clock control is transferred from switch control 0 to switch control 1. Contacts of relays S2, S3, and S5 perform the transfer operation. The 024V/0 and 06V/0 power leads are respectively disconnected from the +24/0 and +6/0A clock leads which are then grounded. The normal ground connections to clock 1 +24/1 and +6/1A are disconnected and power leads 024V/1 and 06V/1 are connected to clock 1. Only the controlling clock provides resonant transfer timing (strobe) signals for entire switch unit. Thus the clock output leads CSA/0 through CSK/0 normally supply the talking time slot strobe signals to the line and trunk circuit leads SWA/0 through SWK/0, respectively. The SWA/0 through SWK/0 leads are disconnected from the assigned switch control circuit and transferred by relay S3 to ground. The SWA/1 through SWK/1 leads are disconnected from ground and respectively transferred by relay S5 to clock output leads CSA/1 through CSK/1. The PF1, PF2, SC0, SC1, and PFRR leads shown in Fig. 61 are associated with the power failure circuit functions and will be described in 4.44 through 4.52.

4.42 The GSB and GSB1 leads are applied to monopulsers MP2 and MP3 in Fig. 55. A battery level pulse on either lead produces the 220 msec UDS/0 and UDS/1 signals. The UDS signals inhibit message sending while the last-look memory is updated after the occurrence of a scanner transfer. The state of maintenance scan point 260 is changed if the scanner status changes. The GSB signal is applied to monopulsers MP4 and MP5 in Fig. 56 to produce the 18-msec MASK/0 and MASK/1 signals which initialize the associated incoming message control circuits (TDC0 and TDC1) during a transfer. Similarly, the GSB1 signal is applied to monopulsers MP6 and MP7 to produce the 18-msec MASK/2 and MASK/3 signals associated with the incoming message control circuits of TDC2 and TDC3.

CHECKING AND ALARM CIRCUITS

4.43 The checking and alarm circuits provide a means of detecting fuse failures among the various power buses and equipment failures which cause multiple time division connections in a given group. The fuse failure and multiple connection detector units indicate circuit faults to the control unit via the supervisory status of their respectively assigned maintenance scan points.

4.44 Fig. 62 is the multiple output detector circuit which interrogates the power monitor output leads of the line and trunk circuit and intergroup switch circuit. A battery level pulse on any of the power monitor output leads signifies a multiple switch closure in the associated circuit group. Each lead monitors the current drawn from a 24-volt power supply by the assigned time division switches. The power monitor outputs, when interrogated during maintenance routines, are applied to the scan point driver TD1. The interrogation is performed for special test connections by a particular code written into a talking time slot word by the switch unit maintenance program of the control unit.

4.45 The code for interrogation is transmitted to the switch unit via incoming message bits 27, 28, and 31. The bits are transferred to the

addressed time division control time slot word to be subsequently read into output register bits 15, 14, and 11, respectively. Bits 15 and 14 are the ring bits and bit 11 is the maintenance bit. The group pretranslator (GPX) produces one of two signals (MOD1 or MOD2) in accordance with the state of the 3-bit interrogation code. The two ring bits alone produce the MOD1 signal which enables the scan point driver. TD1 via the AND gate designated A to monitor the line and trunk circuit for multiple switch closures in any one group. The maintenance bit alone produces the MOD2 signal which enables TD1 via the AND gate designated B to monitor the intergroup switch circuit.

4.46 The DC0 through DC15 leads monitor the time division switch closures for multiple connections of the group circuits 0 through 15, respectively. The DCSG/0 through DCSG/3 leads monitor the tone and digit trunk group switch circuits (digit trunk and attendant circuits) of the respective time division controls TDC0 through TDC3. The special group is part of the line and trunk circuit. The DCIG/0 through DCIG/3 leads monitor the respective intergroup switch circuits IGS/0 through IGS/3. The intergroup switch circuit includes the group switches, conference capacitors, and special bus switch.

4.47 The scan point driver consists of parallel transistors connected in an emitter-follower configuration. The driver operates as an OR gate, producing a battery level output to maintenance scan point 265 when any of the inputs receives battery level input pulses. Although multiple connections may occur during some time slots such as those involving intragroup talking connections, the scan point output does not change to off-hook state unless a special test connection has been set up to provide an enable or interrogate signal to the scan point driver. The interrogate signal is applied to one of the AND gates designated A or B by the appropriate MOD1 or MOD2 signal from one of the time division control circuits during a special test connection.

4.48 The interrogation pulse, which enables the scan point driver when a special test connection is to be established, is produced by translators of the ring logic portion of the associated group pretranslator (GPX). Two multiple output detector address codes are provided. When the switch store bits B11, B14, and B15 are 0, 1, and 1, respectively, the MOD1 signal enables the scan point driver via gate A to interrogate line, trunk, special group, digit trunk, or attendant circuits. Similarly, if B11, B14, and B15 are 1, 0, and 0, the MOD2 signal enables the scan point driver via gate B to interrogate the intergroup switch, conference capacitor, and special bus switch circuits. Bit 11 is the maintenance bit; although bits 14 and 15 are the ringing bits, the ring logic circuit does not produce ring-ringback output signals when both ring bits are logic 1 state.

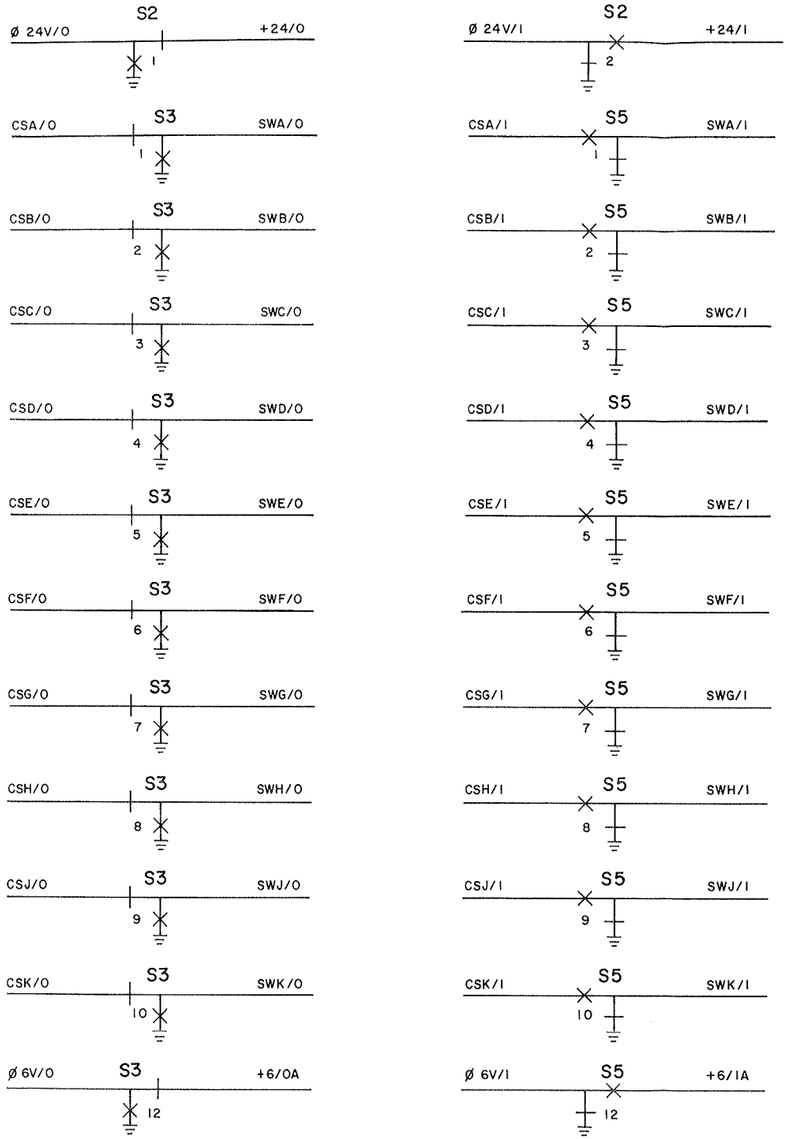
4.49 Fig. 63 is the fuse alarm circuit. Power to the various fused circuits is distributed from the applicable power bus via the assigned circuit fuse. The several power buses provide +24, +24F (filtered 24 volts), -24, and 6-volt dc power sources. Each fuse is the 70-type which provides alarm contacts to make a connection between the applied power bus and the associated fuse alarm bus when the fuse fails.

4.50 When a 6-volt fuse fails, the fuse alarm contact operates to connect the +6 volt power bus through a current limiting resistor (R14, R17, or R21) to lead 266. When the scanner detects the resulting on-hook to off-hook change of state, a message is sent to the control unit to indicate the fuse failure. Failure of any of the assigned +24 or +24F power bus fuses operates the associated alarm contact to provide a differential current between the +24 volt and +6 volt buses via the applicable current limiting resistor (R15, R18, R19, or R22) via fuse 49. The rating of fuse 49 is such that it will immediately operate; the off-hook signal will be the same as previously described for the +6 volt power bus. Similarly, a failure of a fuse assigned to the -24 volt power buses produces a differential current through the applicable resistor R16, R20, or R23 to operate fuse 50. If a fuse fails in the power cabinet, ground is connected to the FA lead operate fuse 51. Similarly, a failure in the optional features (or auxiliary) cabinet produces a ground on the AEFA lead to operate fuse No. 52.

POWER FAILURE CIRCUITS

4.51 Power failure detection and logic circuits are provided in the maintenance circuit to inhibit switch unit operation when a power failure is detected. The power failure circuits include the following circuits:

- ac power failure detection



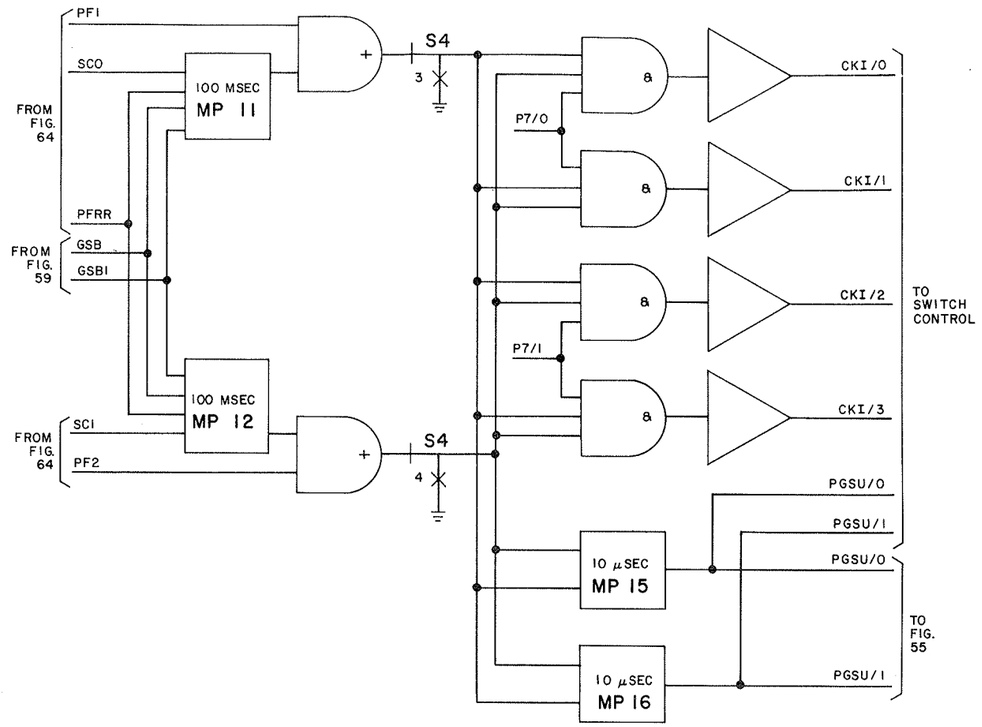
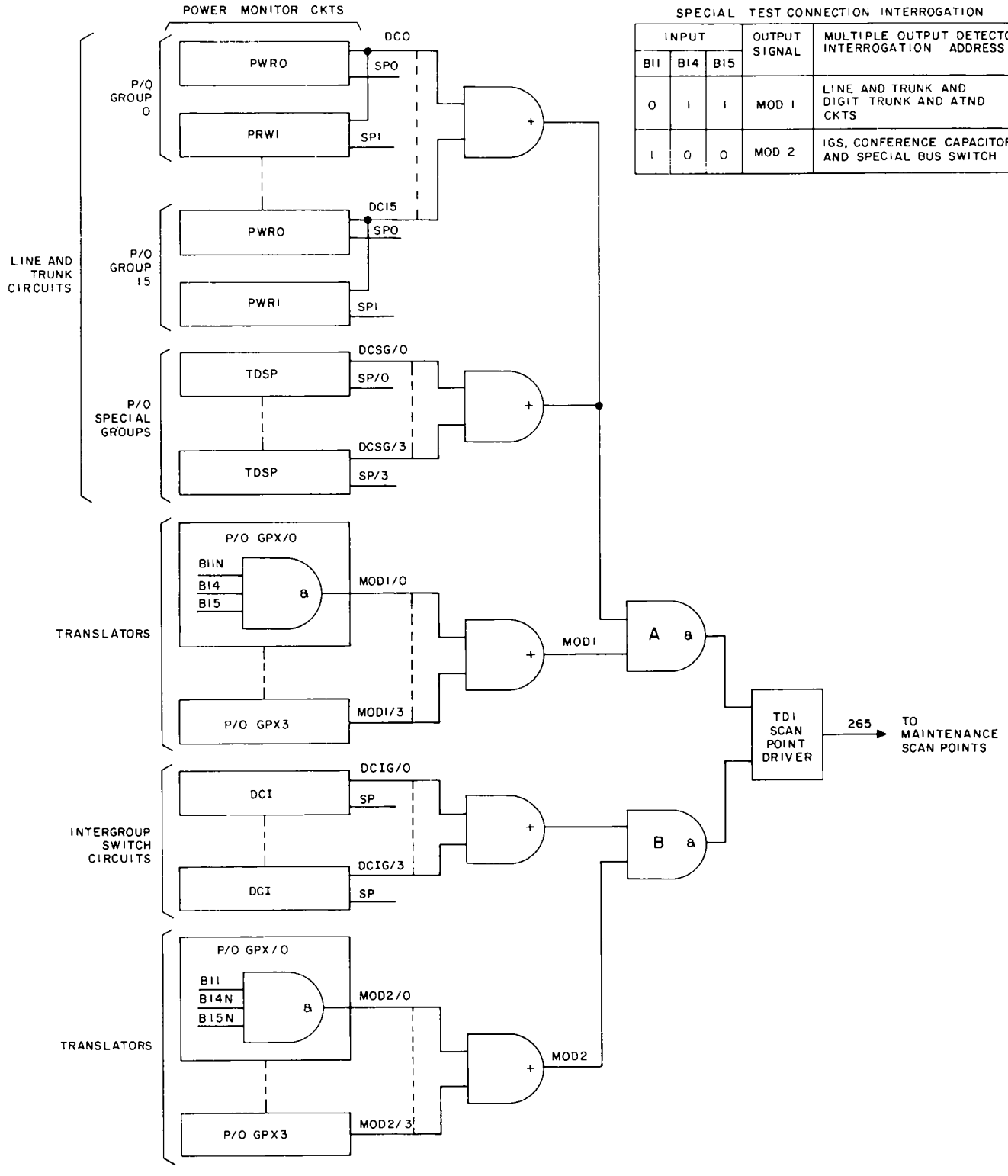


Fig. 61—Clock Inhibit and Transfer Circuit



SPECIAL TEST CONNECTION INTERROGATION

INPUT			OUTPUT SIGNAL	MULTIPLE OUTPUT DETECTOR INTERROGATION ADDRESS
BII	BI4	BI5		
0	1	1	MOD 1	LINE AND TRUNK AND DIGIT TRUNK AND ATND CKTS
1	0	0	MOD 2	IGS, CONFERENCE CAPACITOR AND SPECIAL BUS SWITCH

Fig. 62—Multiple Output Detector Circuit

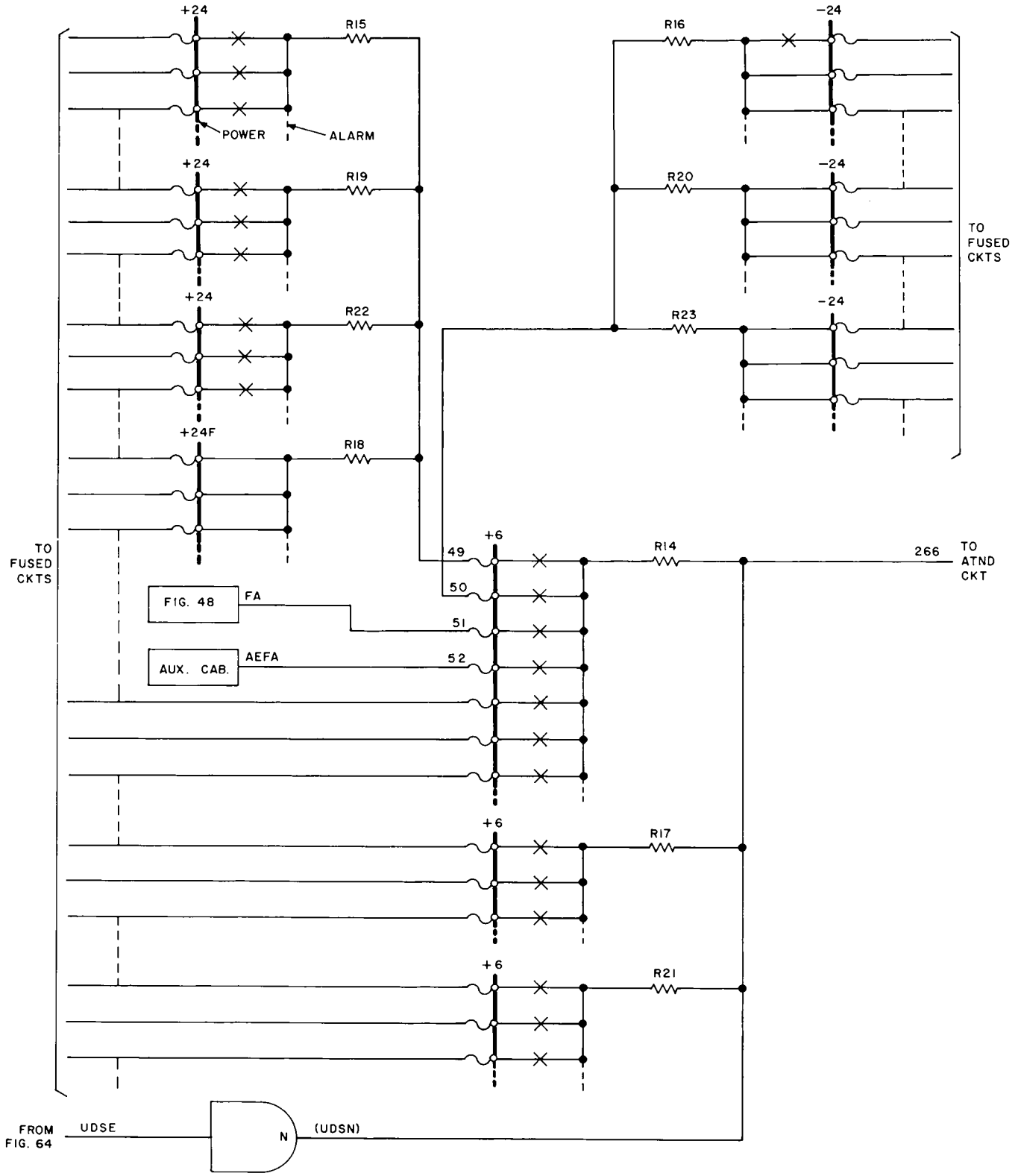


Fig. 63—Fuse Alarm Circuit

- Power failure relays and station transfer relays
- dc power failure
- Power restoration
- Ringing voltage generation
- Ringing generator failure detection.

4.52 Fig. 64 is the ringing generator and power failure detector circuit which provides ringing current for the line and trunk circuits and failure detection circuits for the ringing and power circuits.

A. AC Power Failure

4.53 The ac failure detector circuit is provided in duplicate and the outputs of both detectors must compare before the subsequent stages can react. Thus, an individual detector circuit failure is prevented from causing a false power failure indication. In the case of an ac power failure, both detectors will produce battery level signals (VD0 and VD1). When the VD0 lead switches from ground to battery level, the monopulser MP9 follows with an output transition from ground to battery level. Although MP9 times out in 150 msec for input signals of shorter duration, the output level of MP9 remains at battery level for the entire input signal duration. Consequently, the output level of MP9 follows the input level with a guaranteed minimum 150-msec output interval. The output MP10 similarly follows the VD1 signal. The MP9 and MP10 monopulser output signals are respectively applied to the set input leads of flip-flops FF15 and FF16. The signals normally at ground level are inverted to provide constant reset signals on the respective flip-flops FF15 and FF16 during the long periods of no failure. When an ac failure occurs, the battery level signals set flip-flops FF15 and FF16 for 150 msec or more. The flip-flop output signals are compared in AND gates G25 and G26 which respectively produce battery level signals PF1 and PF2. The PF1 and PF2 leads are applied to the common timing control circuit which produces clock inhibit signals CKI/0 through CKI/3 (described in 4.40) that freeze the existing state of clock ring counters in both switch control circuits to preserve the information in each store circuit. The battery level PF1 and PF2 signals operate gates G27 and G28, respectively, to cut off the associated relay drivers RD7 and RD6 to release power failure relays PFR1 and PFR2 which otherwise are operated. When PFR1 and PFR2 release, the power is removed from the clock ring counters. When the ac power is restored to a satisfactory level, the constant reset signals are again supplied to power failure flip-flops FF15 and FF16, causing the PF1 and PF2 leads to return to ground. Although the clock inhibit signal is removed and contact numbers 2, 3, 4, and 7 of the relays PFR1 and PFR2 operate to restore dc power to the ring counters, contacts number 9 generate a power failure reset (PFRR) signal which produces the 100-msec clock inhibit pulses CKI/0 and CKI/1 described in 4.40. The 100-msec clock stoppage during the restore operation provides the time necessary for the switch control logic circuits to reach a stable condition.

4.54 If the power failure is sufficiently short to prevent the decay of the dc supplies below the level at which the monopulsers fail to operate, the released PFR1 and PFR2 relays which were released for the minimum 150 msec, operate to restore the ring counter power. However, since the PFRR signal generated the 100-msec clock inhibit for the restore operation, it is evident that the minimum time a switch unit can be inoperative due to an ac power failure is 250 msec.

4.55 The connections from the PF1 lead to gate G27 and from the PF2 lead to gate G28 are provided in nonreserve powered switch units to produce the release of relays PFR1 and PFR2 during temporary ac power failures as described in 4.47. When the switch unit is equipped with a reserve power supply, the connections are not provided and the PFR1 and PFR2 relays do not release during temporary power failures, but the PF1 and PF2 signals do stop the clock for 150 msec (CKI signal) and the UDS signals are generated as described in 4.40 and 4.06, respectively.

4.56 Additional contacts on the power failure relays PFR1 and PFR2 cause the following operations:

(a) When make contact number 5 of both relays opens upon release, the station line transfer relays SLR1 and SLR2 transfer six predesignated station lines to central office trunk pairs for emergency operation during the power failure as described in 4.68.

(b) When make contact number 1 of both relays opens upon release, the 24-volt power via resistor R13 and the PFRB lead is removed from the auxiliary 229B key telephone units that may be provided to transfer additional station lines needed for emergency power failure operation as described in 4.68.

(c) When break contact number 6 of both relays closes upon release, the tip and ring leads on digit trunk number 3 are shorted together, indicating to the control unit that a power failure has occurred at the switch unit.

B. DC Power Failure

4.57 A dc failure detector circuit consisting of four resistors (R6A, R7A, R6B, and R7B) and four diodes (CR3A, CR4A, CR3B, and CR4B is provided). The value of resistors is chosen to provide a bias slightly more negative than the ground level required to produce the normal battery level output from gates G27 and G28. The diodes provide protection to the power supply circuits as well as a logic circuit arrangement which requires a failure of both -24 volt or both +24 volt supplies to cause the release of power failure relays PFR1 and PFR2. If both -24 volt supplies fail, the detector output leads (designated -24 volt fail) are biased positively to produce battery level signals which operate gates G27 and G28, causing relay drivers RD7 and RD6 to cut off and releasing the normally operated relays PFR1 and PFR2, respectively. If both +24 volt supplies fail, the relay driver collector current through the associated power failure relays is cut off to release the relays by direct means. Failure of both +6 volt supplies produces a loss of battery level on the output leads of gates G27 and G28. The resulting ground level input to the relay drivers causes the power failure relays to release. Since the nature of a dc power failure is generally permanent, it is not necessary to provide an orderly transition from the normal to the power failure state (via the PF1 and PF2 leads) as is provided for ac power loss which may be very temporary in nature.

C. Ringing Voltage Failure

4.58 The ringing voltage generator provides 20-cycle power at the proper dc level to the line and trunk circuits for the purpose of ringing subscriber telephone sets. The approximate 95-volt sinusoidal output of the ring generator is dc restored by the network consisting of capacitor C5 and four diodes with output to the RNG lead via make contact 8 of the normally energized relay SR1. The diodes clamp the upper excursion of the generator output to ground. When the generator output is positive, the diodes are forward biased, causing C3 to be negatively charged to the peak output voltage (approximately 125 volts). Thus, the ringing voltage applied to the line and trunk circuits via relay SR1 and lead RNG is never more positive than ground potential.

4.59 The ringing generator output is also applied to a ring generator threshold detector (RGTD) via the dc restorer circuit (DCR), producing a positive level on the RGTD input lead. When the ringing generator is operating satisfactorily (output greater than 70 volts rms), the ripple-free voltage from the filter network of RGTD is sufficient to overcome a threshold and cause maintenance scan point 268 to be held at ground level (on-hook). The scan point is maintained in the on-hook state until the ring voltage amplitude falls below a usable level, causing a battery level signal (off-hook) on the scan point. The off-hook message is sent to the control unit, indicating a ringing circuit generator failure.

D. Power Failure in the Switch Unit Equipped with Reserve Power

4.60 When the ac power falls to a level that causes the loss of dc power, the power failure relays PFR1 and PFR2 release as described in 4.55 to accomplish the transfer to the reserve supply. The transfer to reserve power is accomplished when the break contact 8 of relays PFR1 and PFR2 connects a ground to the PFR lead of the reserve supplies. The transfer to reserve power causes the PFR1 and PFR2 to operate and initiate a restore power operation via the PFRR lead which generates a battery level pulse during the relay operation transition of PFR1 and PFR2 contacts.

4.61 The power control circuit holds the reserve supply in operation until the correct ac level and ferroresonant supply levels are detected to initiate a transfer to the normal supply. When the transfer to normal supply occurs, battery level pulses on the SC0 and SC1 leads generate 100-msec clock inhibit pulses and subsequent 220-msec update scanner (UDS) operation described in 4.40 and 4.06, respectively.

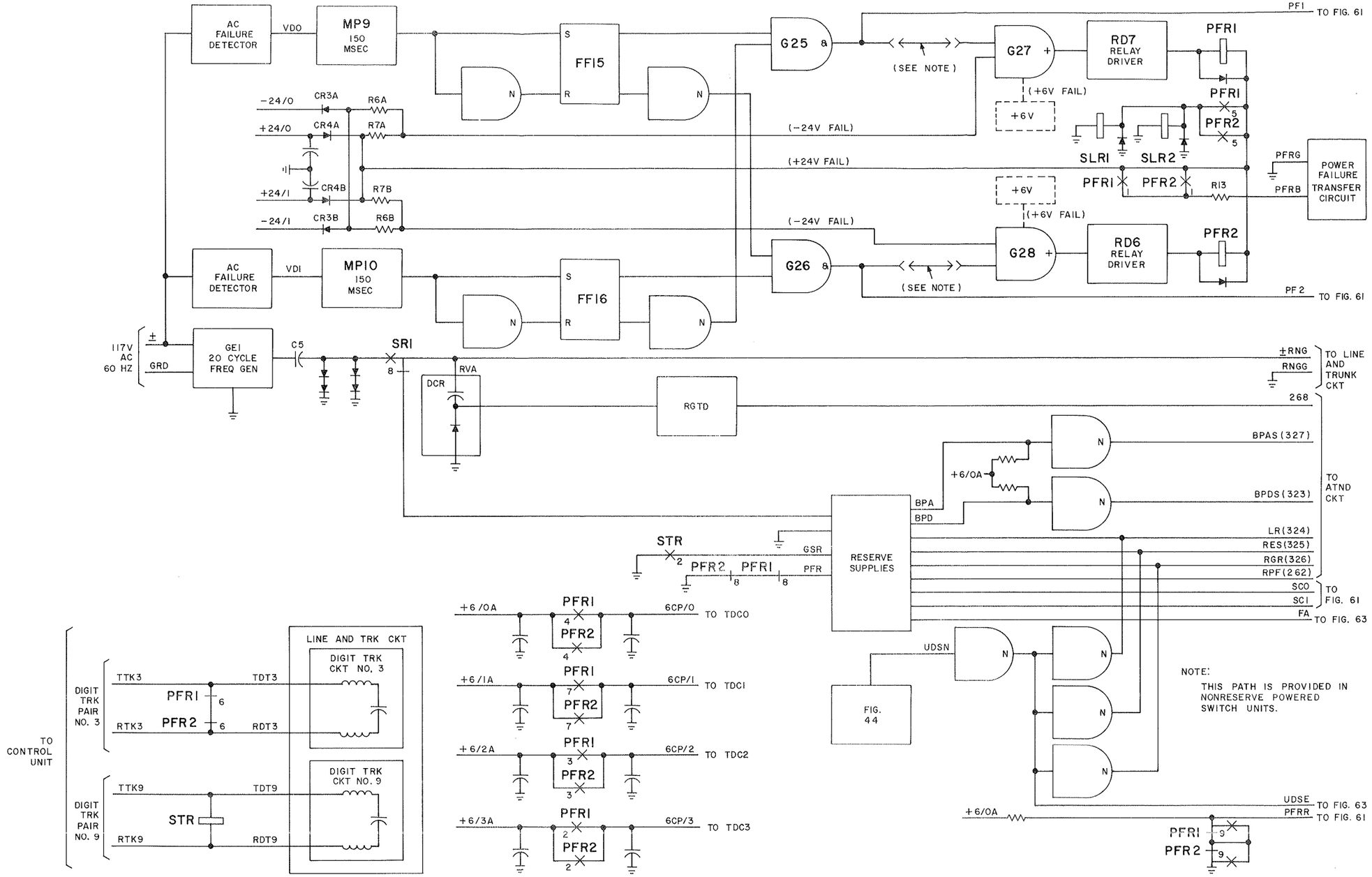


Fig. 64— Ringing Generator and Power Failure Detector Circuit

E. Control Unit Controlled Transfer to Reserve Power

4.62 In a switch unit equipped with reserve supplies, the control unit may produce a transfer to the reserve supply by means of automated test routines. The automated test routines in the control unit may accomplish the transfer by utilizing a dc transfer similar to the grand slam, provided normal power is operating. The control unit sends battery to the switch unit via digit trunk pair number 9 to operate the STR relay. When the STR relay is operated, make contact 2 places ground on the GSR lead, causing the power supply control circuit to transfer from normal to reserve. The SC0 and SC1 signals stop the clock for 100 msec during the transfer to prevent loss of switch store information followed by the 220-msec UDS signal. Removing ground from the GSR lead via control unit action releasing the STR relay transfers the power from reserve to normal and initiates the power restoration sequence described in 4.53.

F. Reserve Power Scan Points

4.63 Reserve power transfer and alarm status provided by the reserve supply is relayed to the control unit by the maintenance and attendant scan points. The scan points indicate battery alarms, fuse alarm, reserve transfer status, and reserve power failure.

4.64 The BPA and BPD signals produce off-hook signals on scan points 327 and 323 to indicate minor and major battery alarms, respectively. Battery level applied to the BPA and BPD leads converts the relay signals from the reserve supply via inverters to on-hook signals (ground level) on the BPAS and BPDS leads to ensure the scan points will be in the on-hook state during UDS.

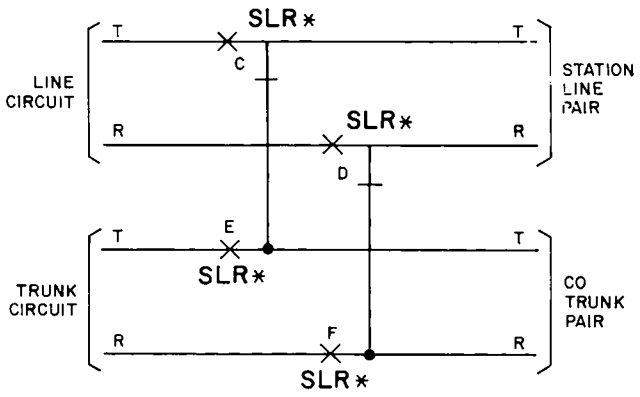
4.65 The LR, RES, and RGR signals produce off-hook signals on scan points 324, 325, and 326 to indicate locked on reserve (LR), reserve power in use (RES), and reserve ringing supply in use (RGR), respectively. The LR lead off-hook condition is caused by disagreement between the power failure signals from the maintenance and attendant circuit and the indications monitored by the power supply control circuit. The LR condition can be released manually at the switch unit or remotely at the control unit via digit trunk pair number 9 and the STR relay. The RES lead off-hook signal is due to a transfer from normal power to reserve power. The RGR lead off-hook signal is caused when the SR1 relay releases to transfer from the normal 20-cps frequency generator to the reserve ringing supply. The UDSN signal from the scanner and switch control transfer circuit (Fig. 55) is employed via an inverter stage to produce a battery level UDSE signal. The UDSE lead fans out through inverters to produce a clamp grounding scan points 324, 325, and 326 to ensure they will be in the on-hook state during the UDS operation immediately following a transfer.

4.66 The FA signal produces an off-hook signal on scan point 266 (Fig. 63) via fuse 51 as described in 4.50. The UDSE signal is employed via an inverter to clamp scan point 266 in an on-hook condition during the UDS operation.

4.67 The RPF signal (Fig. 64) produces an off-hook signal on scan point 262 to indicate a failure in the reserve power plant.

G. Station Line Transfer

4.68 The SLR1 and SLR2 relays of the switch unit provide contacts for the transfer of six predesignated station lines to central office trunk pairs for emergency operation during a power failure. Fig. 65 is the transfer circuit for one station line using the SLR1 or SLR2 relay. Since all six line transfer circuits are identical, the relay contacts are designated with letters. The contact numbers are listed in Table R under the corresponding letters for each transfer circuit. Additional line transfer circuits may be provided by auxiliary units to transfer 12 additional station lines to central office trunk pairs for emergency operation. The coil operating current is supplied from the power failure detector circuit via leads PFRB and PFRG.



* DENOTES THE RELAY DESIGNATION NUMBER (TABLE R). COILS FOR RELAYS SLR1 AND SLR2 ARE SHOWN IN FIG. 64.

Fig. 65—Station Line Transfer Circuit Using Relays SLR1 and SLR2

TABLE R

STATION LINE TRANSFER RELAY ASSIGNMENT

RELAY	TRANSFER CIRCUIT NO.	RELAY CONTACT NO.			
		C	D	E	F
SLR1 (Fig. 65)	1	1	2	3	4
	2	5	6	7	8
	3	9	10	11	12
SLR2 (Fig. 65)	4	1	2	3	4
	5	5	6	7	8
	6	9	10	11	12