

DATA TRANSMISSION
DESCRIPTION OF SYSTEM OPERATION
NO. 101 ELECTRONIC SWITCHING SYSTEM

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1. BASIC DATA LINK ARRANGEMENT

A. General

1.01 This section is reissued to include the 2A and 3A switch units. Because this reissue covers a general revision, arrows ordinarily used to indicate changes have been omitted.

1.02 The data links are comprised of voice frequency facilities and those circuits that enable supervisory and control data signals to be transmitted between the control unit and switch units. These circuits provide a means for data intercommunication to supply the information required to set up dialing, ringing, and talking connections. Fig. 1, Fig. 2, and Fig. 3 depict the basic data link arrangement used for the data connection between one switch unit and the control unit. Fig. 1 is for a 1A switch unit, Fig. 2 is for a 2A switch unit, and Fig. 3 is for a 3A switch unit.

B. Incoming Message

1.03 The incoming message is defined as the data message transmitted by the switch unit to the control unit. At the switch unit there are two data receivers and two data transmitters. Only one transmitter is *on-line* at a time, as determined by relay contacts in the transfer and alarms circuit. The scanner circuits feed the 14-bit incoming message (12 bits for 1A switch unit) serially to the data transmitter in dc form. Each bit is 1554 μ sec in duration, corresponding to a bit rate of 643.4 bits per second. This bit interval is significant for two reasons:

(1) It can be detected easily by scanning at the control unit where the scanning rate is fixed at 735.3 bps (8/7 of 643.4 cps).

(2) It is easily produced in the switch unit scanner by the use of a reference frequency from the associated data receiver oscillator.

1.04 When a single mark (1) is to be transmitted, an input lead to a data transmitter is grounded for 1554 μ sec; and when the bit is a space (0), the lead is plus TRL potential for a 1554- μ sec period. The data transmitter converts the dc input to a frequency-shift ac signal suitable for transmission over the data trunk pair. The

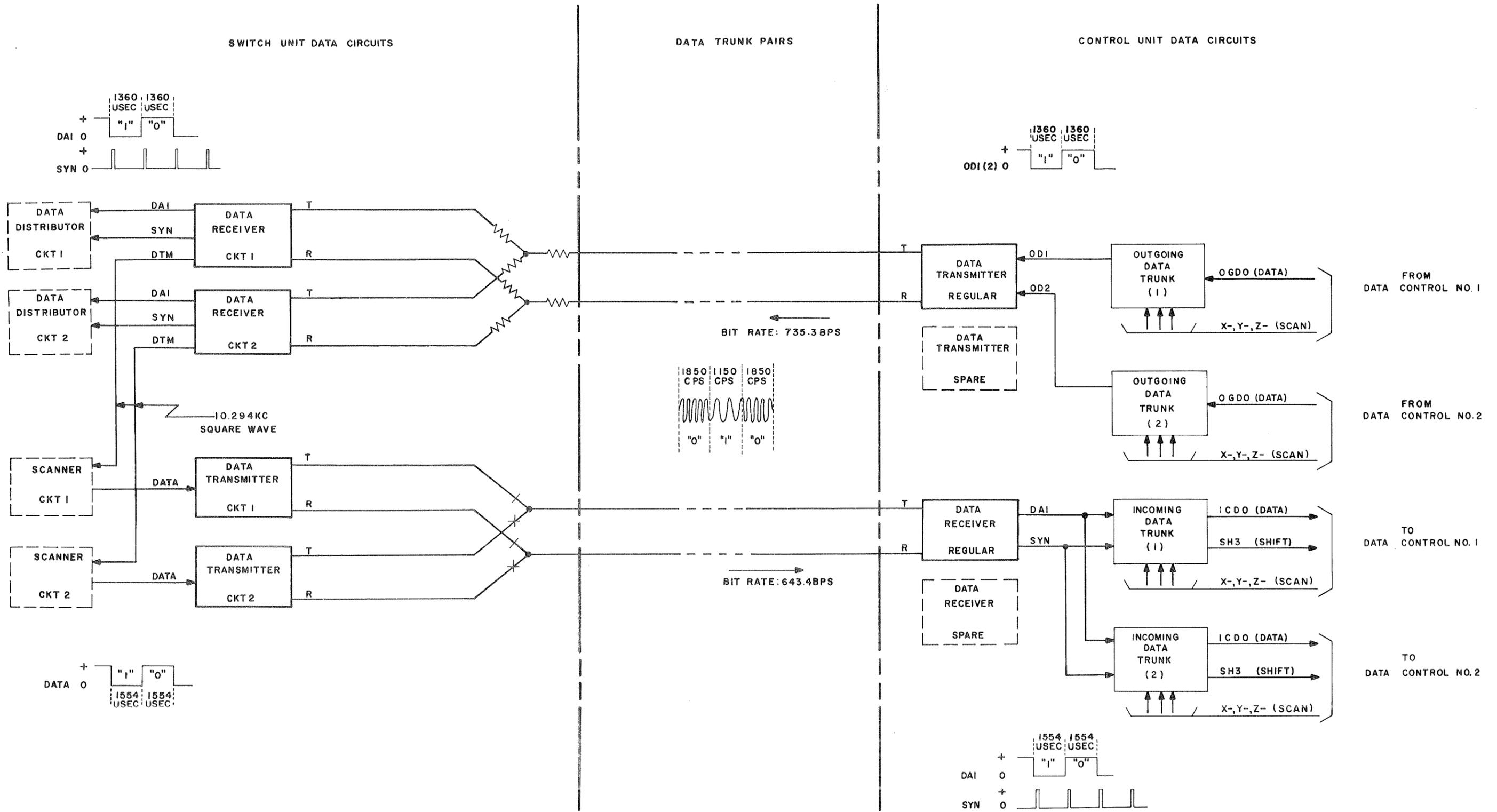


Fig. 1 — Basic Data Link Arrangement for 1A Switch Unit

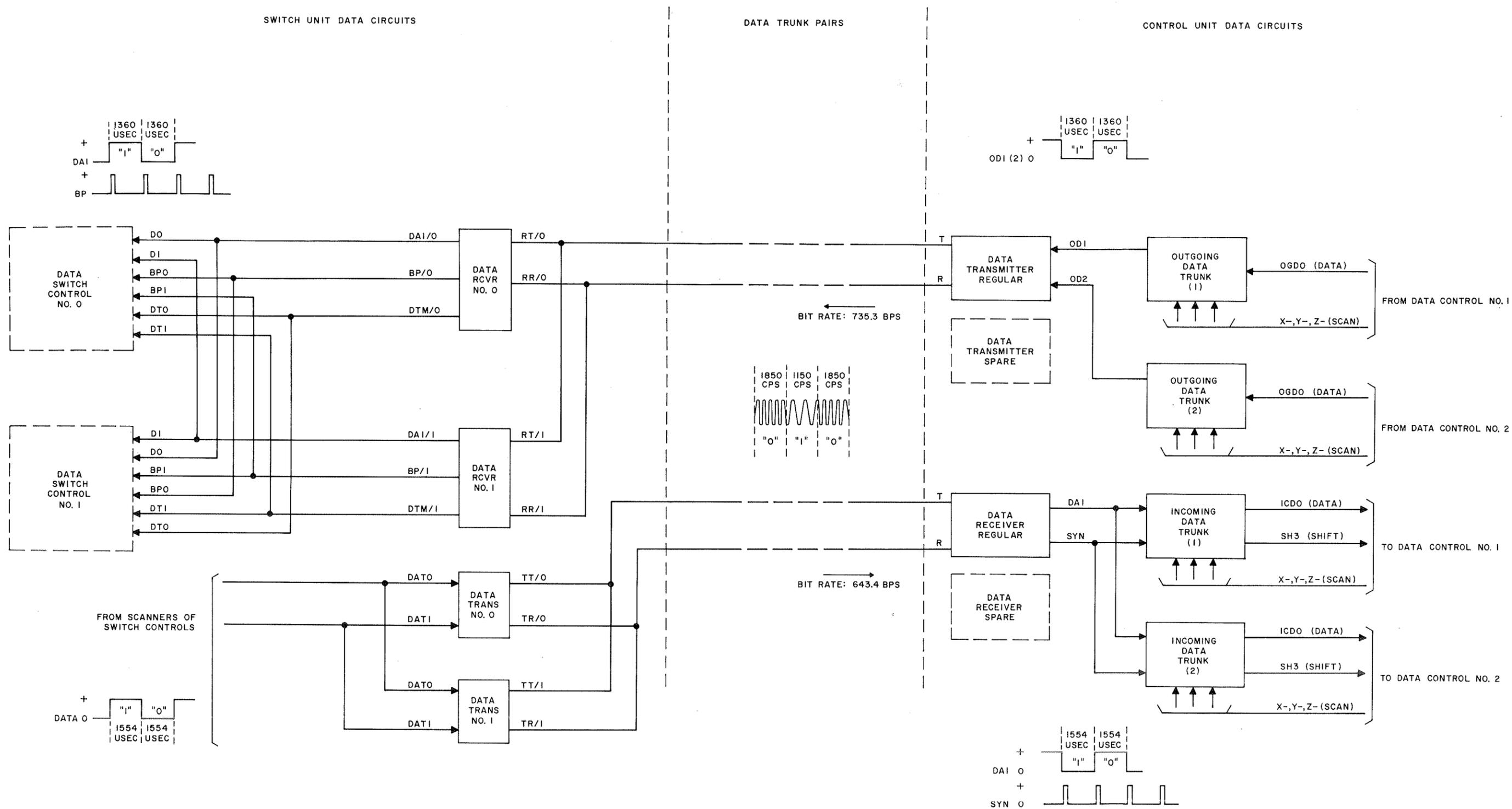


Fig. 2 — Basic Data Link Arrangement for 2A Switch Unit

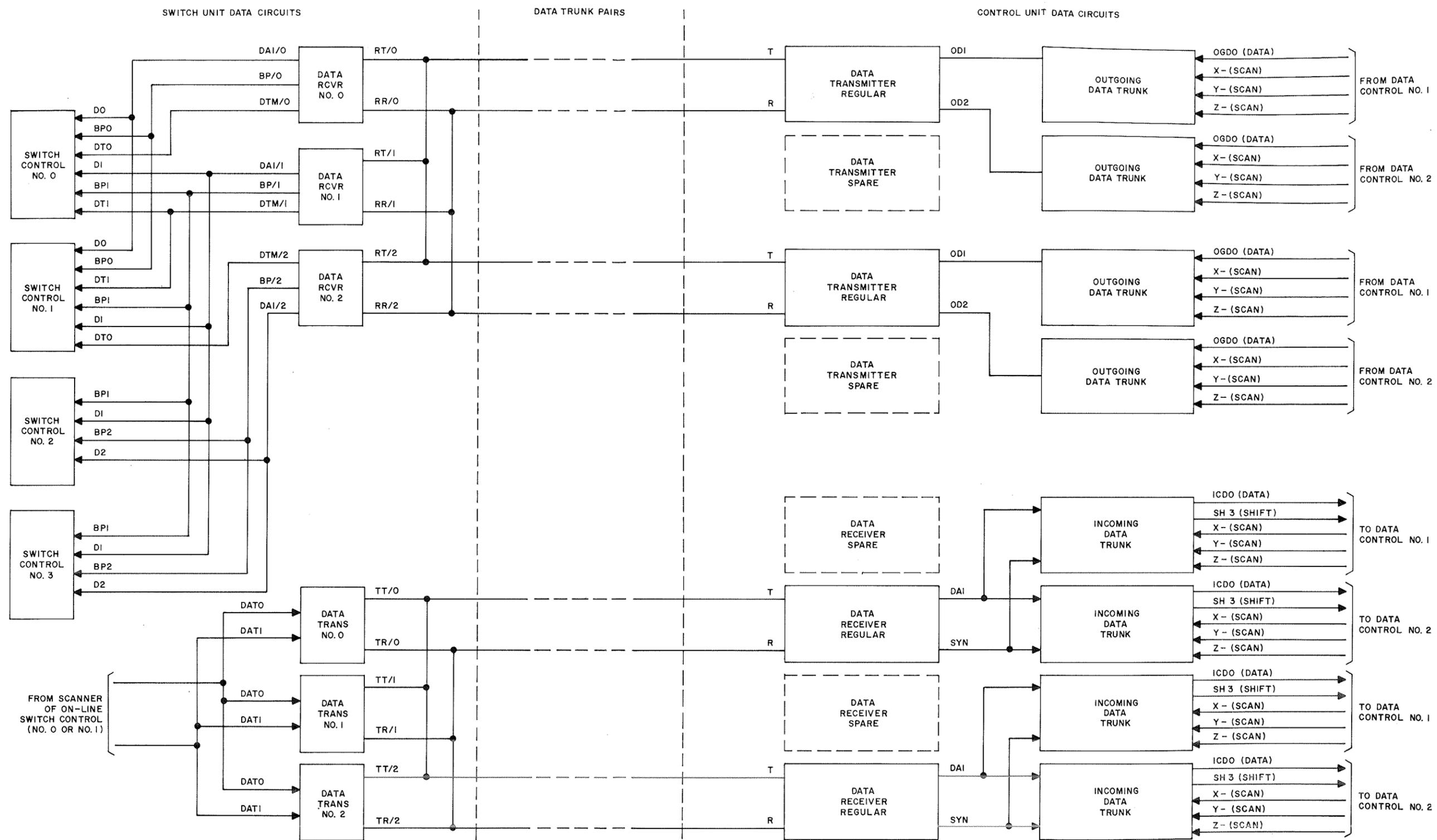


Fig. 3 — Basic Data Link Arrangement for 3A Switch Unit

mark and space frequencies are 1150 and 1850 cps, respectively.

1.05 At the control unit, the data signals are detected by a data receiver. Here the frequency-shift signals are converted to dc pulses (DA1) of the same polarity as originally fed to the data transmitter in the switch unit.

1.06 Accompanying the dc data bits are timing pulses on lead SYN. These pulses are developed within the receiver, and during the data message are phased to occur immediately following the start of the data bits, one SYN pulse per DA1 bit, i.e., every 1554 μ sec. In the 2A and 3A switch units the SYN lead is called the BP lead.

1.07 The incoming message is presented to the incoming data trunk circuit where the bits are scanned by the data control circuit through the medium of the assigned X-, Y-, Z- leads. The sampled data bits on lead ICDO and a shift pulse on lead SH3, each 4 μ sec in duration, are fed to the data control circuit.

1.08 The output of a single data receiver is multiplied to two incoming data trunks, one trunk for each associated data control circuit.

C. Outgoing Message

1.09 The data message to be transmitted to the switch unit (termed an outgoing message) is first directed from the data control circuit to an outgoing data trunk on lead OGDO. Within the trunk circuit, and under control of leads from the data control, the outgoing data bits are timed for a bit length of 1360 μ sec. As in the case of the incoming data, the outgoing data polarity is ground for mark and positive voltage for space.

1.10 Leads OD1 and OD2, from two outgoing data trunks (one per associated data control circuit), carry the outgoing message (47 bits long) to the data transmitter. (The maintenance center enables only one of the two OD- leads.) The data transmitter functions as described for the switch unit except that the data bits are fed to it at a 735.3-bps rate.

1.11 In the 1A switch unit the frequency-shift signals are multiplied through a splitting pad to both data receiver circuits. (This dual data

reception is required by the operating principles of the switch unit.) These receivers operate in the same manner as their counterparts in the control unit. The data receiver timing circuitry contains a crystal-controlled precision oscillator. This oscillator is also used to supply a reference frequency to the scanner circuit (1A) or switch control circuit (2A and 3A). The reference frequency, 10.294 kc, on lead DTM, is used to derive the data bit rate for the data transmitter in the switch unit.

1.12 The 2A and 3A switch units do not have the splitting pad.

1.13 Leads DA1 and SYN for 1A switch units connect to associated data distributor circuits where the data message is acted on. Leads DA1 and BP for 2A and 3A switch units are connected through maintenance and attendant circuits to the switch control circuits.

2. DATA TRANSMITTER, RECEIVER

A. General

2.01 Fig. 4 shows the basic circuitry of both the data transmitter and receiver as used in both the 1A switch unit and the control unit.

2.02 Fundamentally, the data transmitter serves to convert data bits from dc form to a frequency-shift ac signal suitable for transmission over a voice channel. The data receiver, located at the other end of this channel, detects the presence of both ac signal frequencies and restores them to data bits in dc form.

B. Circuit Operation of 1A Switch Unit and Control Unit

2.03 Fig. 4 also shows the waveforms related to the operation of the data transmitter and data receiver circuits. Lettered designations are used to correlate the waveforms with the action of specific circuit details. For this illustration, it is assumed that the data message originates in the switch unit and therefore has a bit period of 1554 μ sec. The following paragraphs are alphabetically designated to correlate with the circuits and waveforms in Fig. 4.

(a) Assume that following a period of space input, a data mark (1) arrives at the transmitter input. In the switch unit installation this

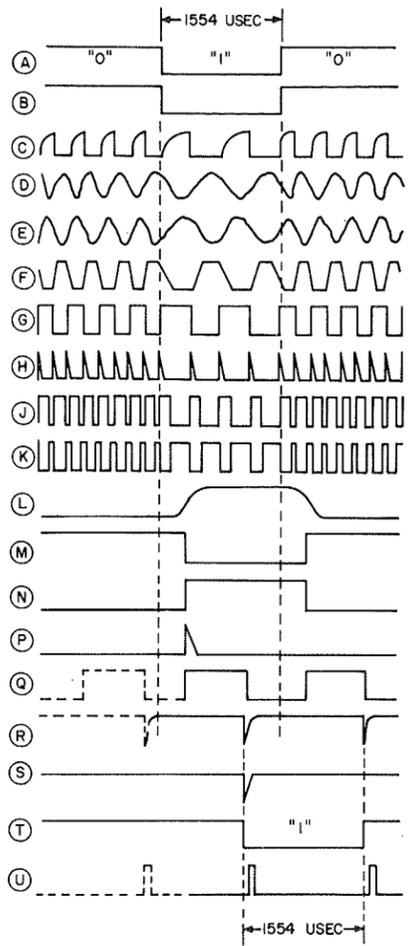
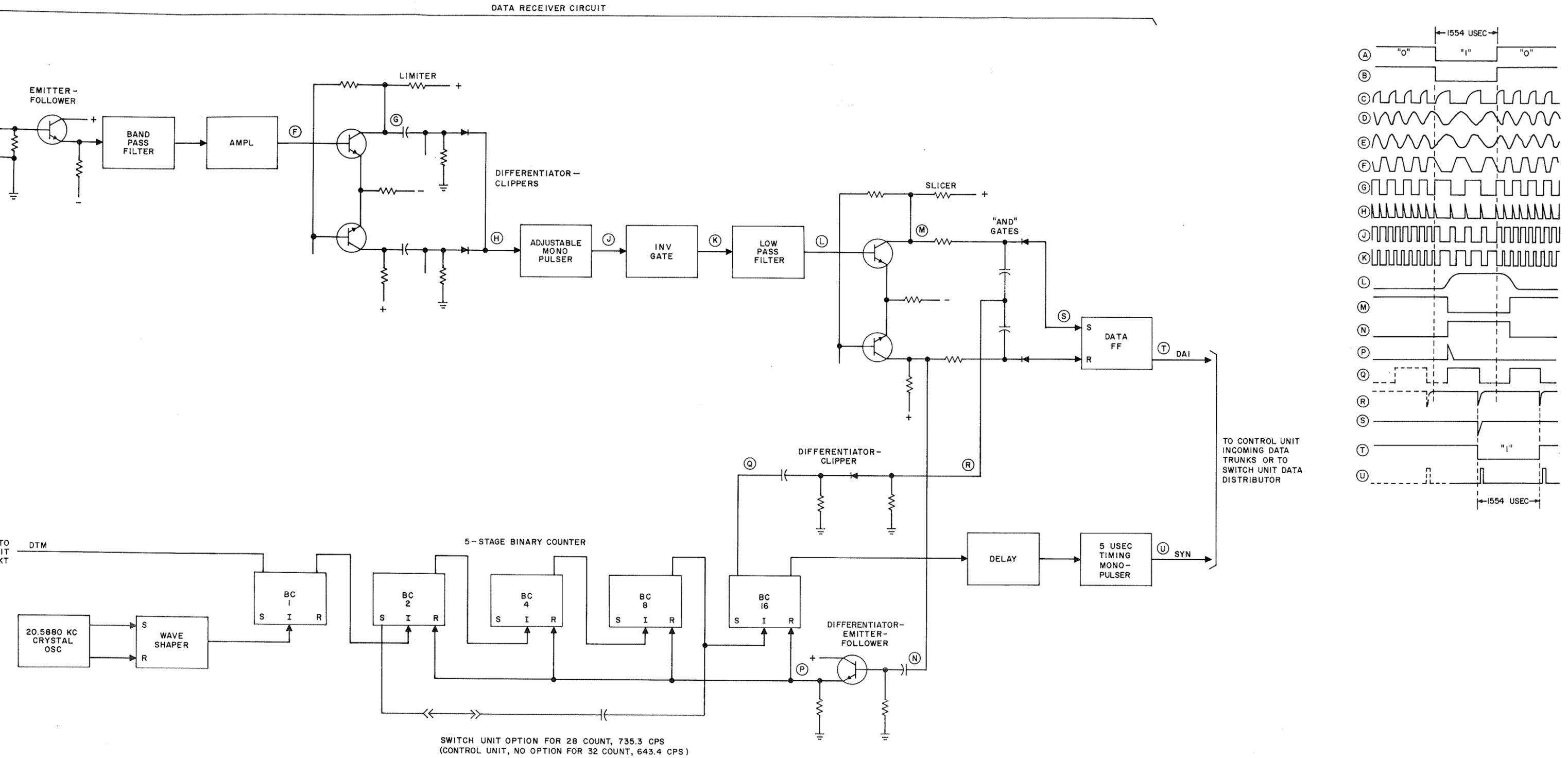
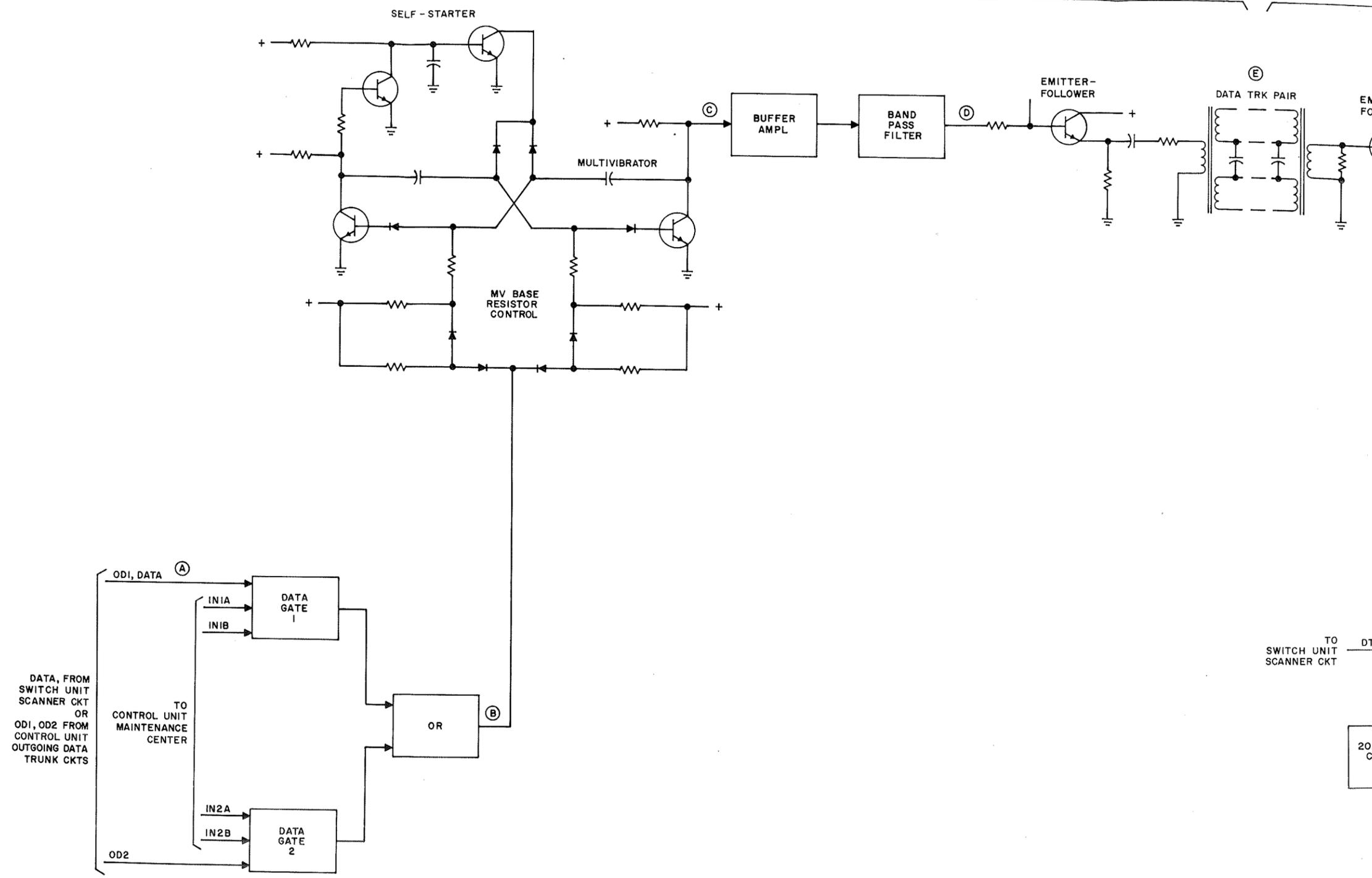


Fig. 4 — Data Transmitter and Receiver Circuits and Waveforms for 1A Switch Unit and Control Unit

DATA TRANSMITTER CIRCUIT



will be derived from the scanner circuit on lead DATA to data gate 1. Via optional wiring, data gate 2 is disabled. (In the control unit installation the 1360- μ sec data bits are received from the outgoing data trunks on leads OD1 and OD2. The active data gate, 1 or 2, is determined by an enable or inhibit signal from the maintenance center.)

(b) Here a gating function followed by an OR function has caused a double inversion of waveform A.

(c) At point C the output waveform of the multivibrator is shown, whose frequency is dependent on the input signal polarity. Normally, when there is a space input, the astable multivibrator changes state at an approximate 1850-cps rate. When the input signal changes to mark, the resulting ground at point B, through the action of the base resistor control, causes the multivibrator time constant to be increased. In effect, the base resistor control has increased the resistance portion of the RC network. Under these conditions the multivibrator changes its output from 1850 cps to 1150 cps. In this way the frequency-shift signals are generated. The self-starter is an auxiliary circuit used to automatically restore multivibrator action should the collectors of both multivibrator transistors remain at ground for a period longer than a normal cycle period.

(d) The waveform at point D assumes an approximate sinusoidal form after passing through a buffer amplifier and bandpass filter.

(e) The frequency-shift signal has a nominal level of -4 dbm. The emitter follower stage ensures a good impedance termination to the trunk.

(f) From the data trunk pair, the frequency-shift signal enters the data receiver through input circuitry similar to that at the transmitter output, i.e., an input transformer, 900-ohm termination, emitter follower, and bandpass filter. At the output of the amplifier the waveform is clipped or partially squared, which is typical of medium transmission level.

(g) The waveform is further squared by the limiter circuit, a high gain balanced output amplifier with positive feedback. The limiting

action eliminates the otherwise detrimental effects of possible amplitude modulation and provides an output waveform with fast leading edges to operate the differentiator-clippers.

(h) The two differentiator-clippers form a positive spike at each zero crossing of the original signal. In effect, the frequency of the line signal is doubled by this action.

(j) Each of the spike inputs to the adjustable monospacer causes a positive pulse of fixed duration to occur. The interval between the pulses is inversely proportional to the input frequency. Note that the average positive potential is noticeably greater for the space intervals.

(k) Here an inverting gate decouples the monospacer from the effects of the low-pass filter.

(l) The low-pass filter removes the line frequency components and substantially recovers the original dc data signals. The filter is required to pass a frequency no higher than approximately 350 cps (one-half the bit rate), occurring when an alternate mark and space are present. A 550-cycle low-pass filter cutoff provides adequate removal of undesired frequencies and retains a good signal level for reliable slicer action.

(m) The waveform at this point is the result of the slicer action where the leading and trailing edges of the LPF waveform are squared. Here circuit actions start which make the final output pulse (mark or space) dependent on the voltage level at the approximate midpoint of the bit interval at circuit point M. The reason for this principle of operation is to guard against the distorting effects of line noise and other variables.

(n) This waveform is similar to waveform M but of opposite polarity.

(p) Here the positive going leading edge of waveform N is differentiated and, without inversion, used to reset the last four stages of the 5-stage binary counter. The binary counter is free running until the last four stages are reset by the differentiator.

(q) This is the final stage of the 5-stage binary counter. The frequency is equal to 643.4 cps (1554 μ sec period). The 643.4 cps is one thirty-second (because of the 5-stage binary counter) of the 20.588 kc input to the binary counter. Of particular interest is the shortened period caused by the random arrival time of the mark at the beginning of a data message which is used to reset the last four stages of the binary counter. The reset causes the counter to shift into phase with the line signal.

(r) At this point there are negative-going differentiated pulses derived from the trailing edge of waveform Q. This series of pulses is used to sample the slicer output.

(s) A negative pulse occurs at point "S" at the end of a timing pulse which is in the middle of a data mark at "M".

(t) This is the regenerated data output waveform. The data flip-flop (FF), which is normally in a set condition becomes reset by the application of waveform S, thus producing a ground potential (i.e., a mark or 1) on lead DA1. (Note that in this case the manner in which the flip-flop is reset involves cutting off the transistor with a negative potential on the set side as the initial action, rather than the more usual method of applying a positive voltage to the reset side.) One bit later (1554 μ sec) another timing pulse and the slicer output N, now at ground, are *anded* to generate a negative spike to set the data flip-flop. Note that the regenerated data output occurs in the approximate middle of the slicer output which permits sampling (by the timing pulse) during a stable portion of the slicer waveform.

(u) This shows the approximate phasing of the timing pulse SYN in relation to DA1 (waveform T). It appears approximately 1 μ sec after the data mark for a duration of 5 μ sec and recurs at intervals of 1554 μ sec, once per data bit interval.

C. Circuit Operation of 2A and 3A Switch Units

2.04 The basic operation of the data transmitter and receiver of the 2A and 3A switch units is similar to the data transmitter and receiver of the 1A switch unit. Therefore, only the block dia-

gram in Fig. 5 is discussed. The following paragraphs are lettered to correspond to the circled letters in Fig. 5.

(a) For a 2A switch unit, the input to the data transmitter is from the outgoing message control circuit of switch control. For a 3A switch unit, the input is from the maintenance and attendant circuit. The on-line input follows the dc level of the transmission message. The positive level or ground corresponds to a logical 1 or 0.

(b) The modulator circuit converts the dc level of the received signal to a square wave output at one of two frequencies. If the input is a logical 1, the free-running multivibrator has a frequency of 1150 cps. A logical 0 input produces a frequency of 1850 cps.

(c) The amplifier circuit converts the square wave modulator output into sinusoidal waveforms, sets the output power level, and provides the proper source impedance for the data link. The period for a single mark or space transmitted to the control unit is 1554 μ sec.

(d) The period for a single mark or space received from the control unit is 1360 μ sec.

(e) The data receiver amplifier-limiter provides the proper termination for the data link. The amplifier-limiter amplifies, limits, and shapes the incoming sinusoidal waveforms.

(f) The trigger circuit provides amplification and a two-phase output (one shown) on two leads to the detector.

(g) The monopulser circuit of the detector produces a 175- μ sec pulse on the positive going portion of both input waveforms. An output pulse then occurs every 435 μ sec for a logical 1 and every 270 μ sec for a logical 0.

(h) The output of the monopulser is inverted and passed through a low-pass filter which produces a dc waveform resembling the original data waveform but slightly delayed in time.

(j) Other portions of the detector circuit amplify, invert, and clip the output of the low-pass filter to supply inputs to the mark AND gate and the timing reset circuit.

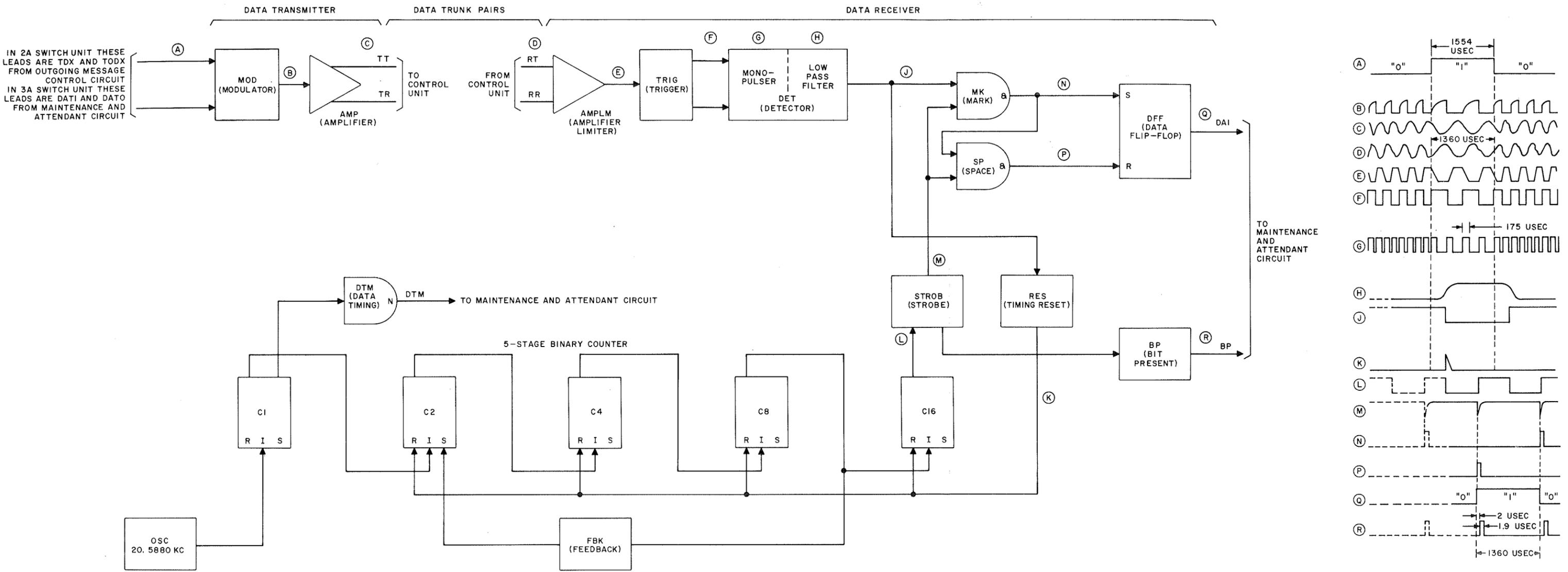
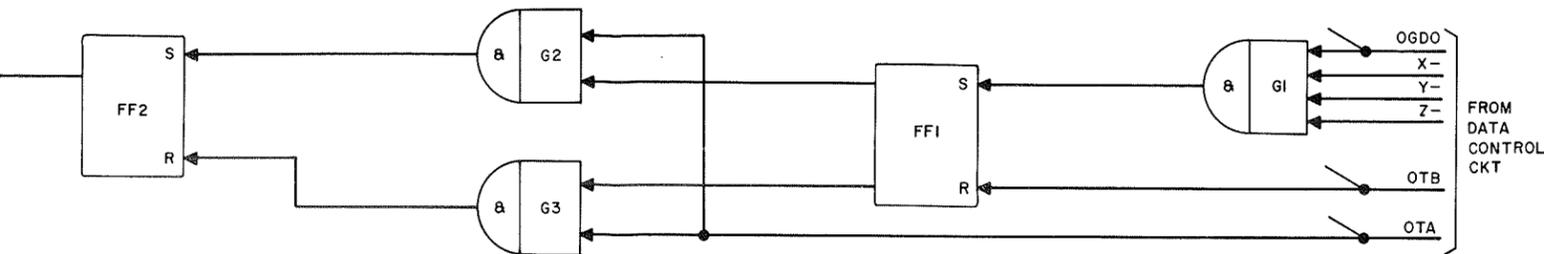


Fig. 5 — Data Transmitter and Receiver for 2A and 3A Switch Units

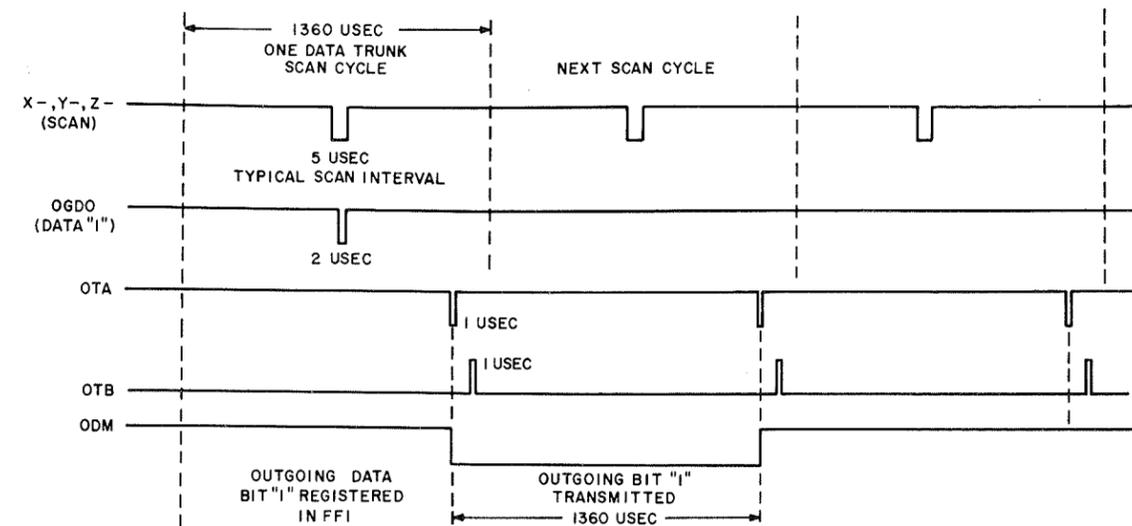
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OUTGOING DATA TRUNK

CIRCUIT

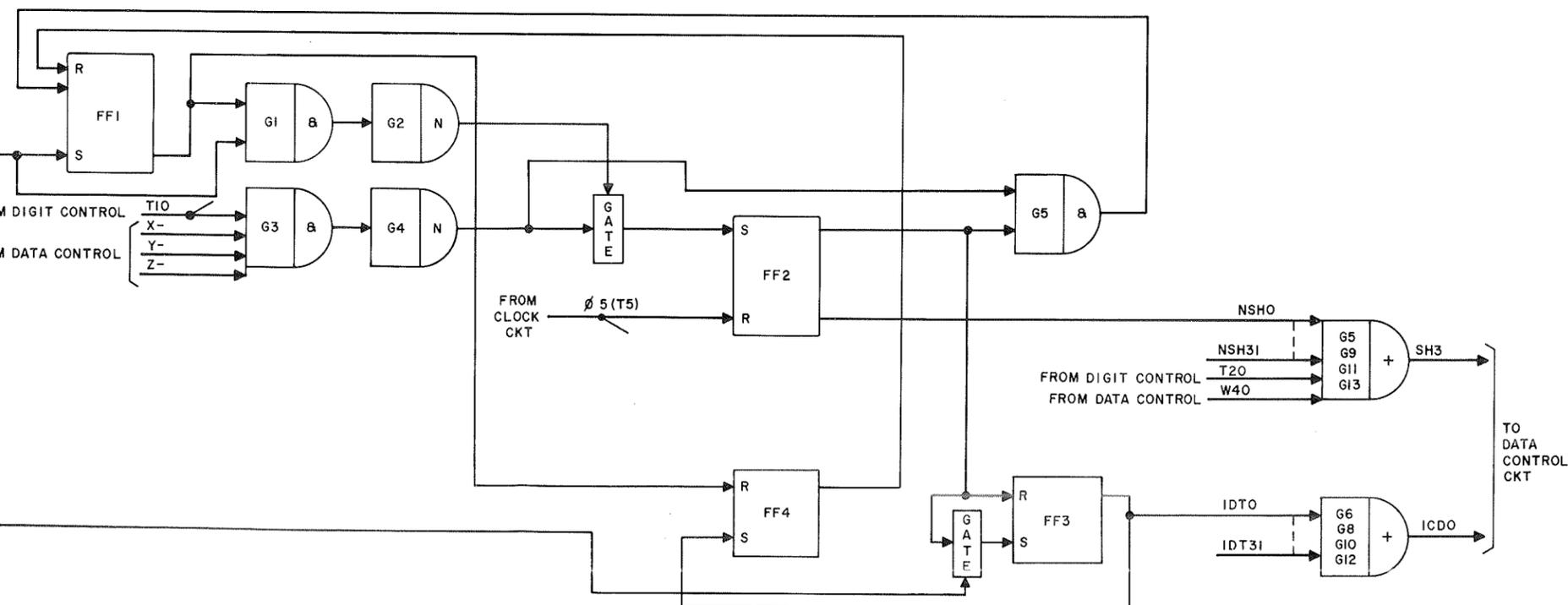


SEQUENCE DIAGRAM

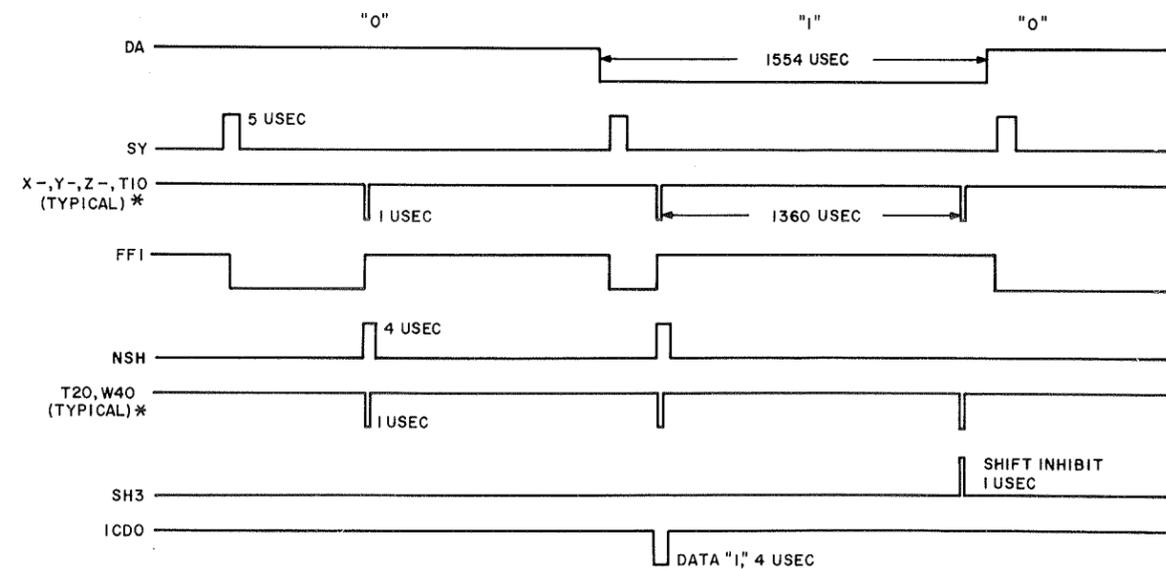


INCOMING DATA TRUNK

CIRCUIT



SEQUENCE DIAGRAM

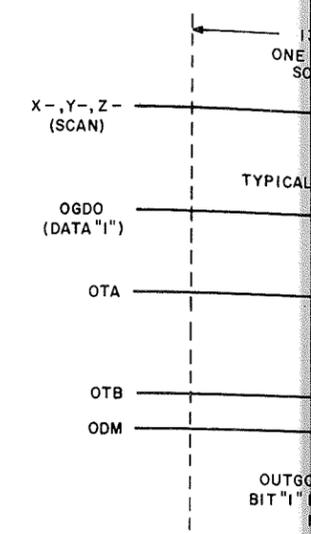
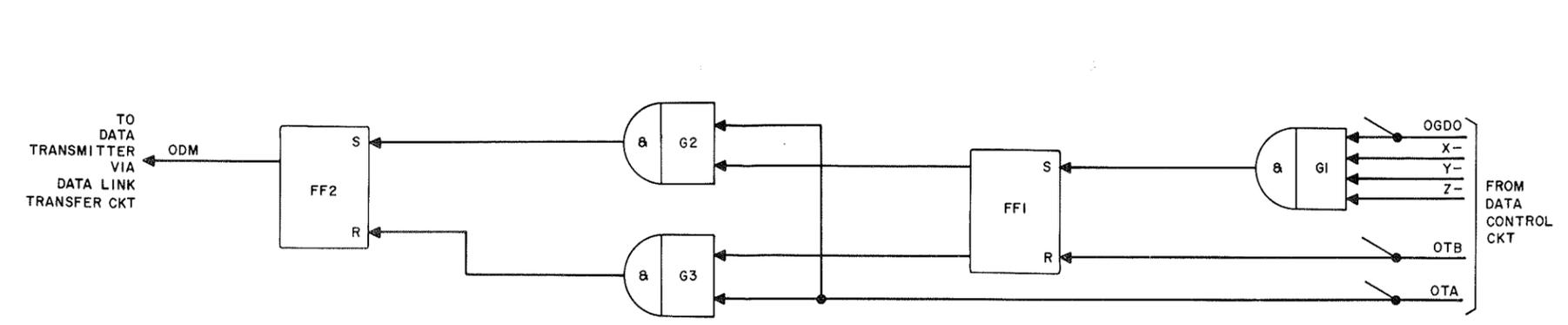


* ILLUSTRATED WAVEFORM IS FOR 1 OF 32 TRUNKS.

Fig. 6 — Data Trunks

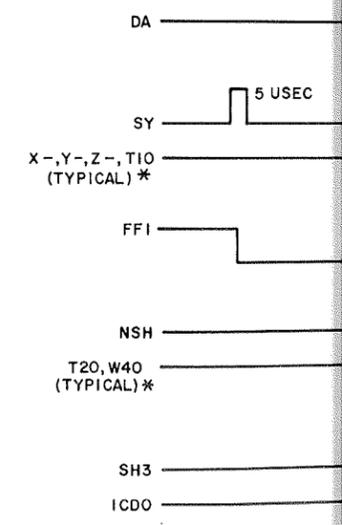
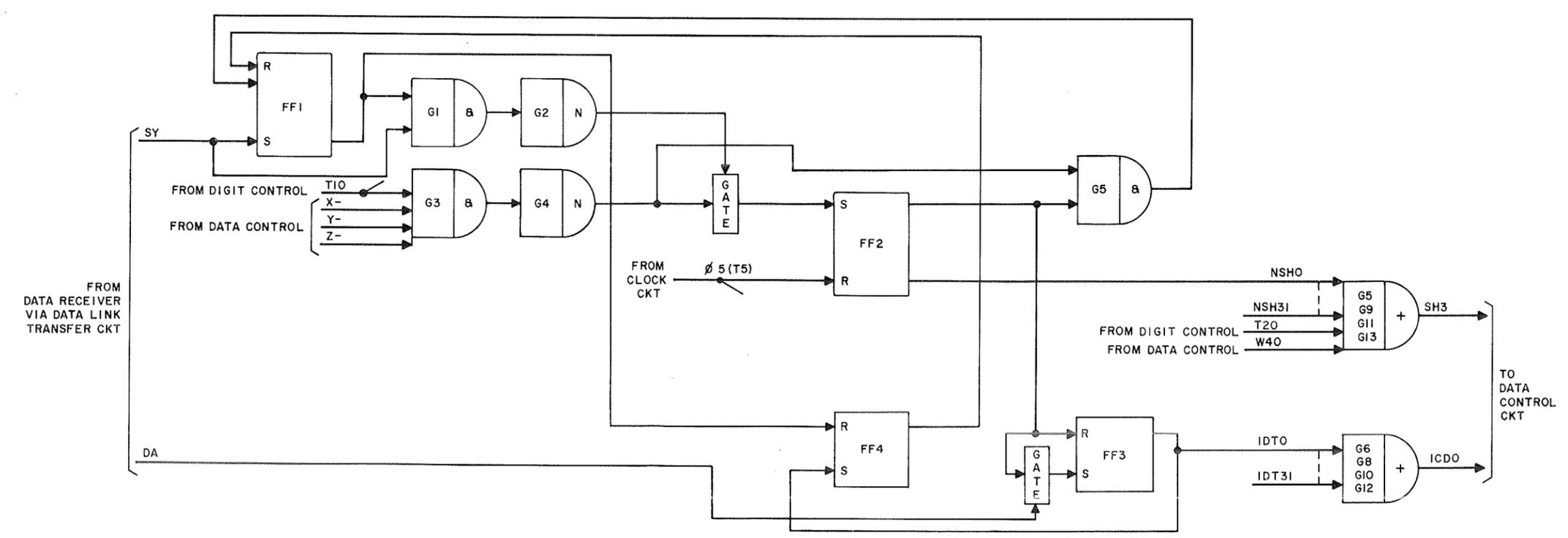
OUTGOING DATA TRUNK

CIRCUIT



INCOMING DATA TRUNK

CIRCUIT



* ILLUSTRATION

This results in ground on lead ODM to the associated data transmitter. Two microseconds later, at T6, a 1- μ sec battery pulse appears on lead OTB to reset FF1 which puts ground on one of the two inputs to G3. At the end of the next complete scan cycle, the second input to G3 is enabled when lead OTA drops to ground for 1 μ sec (assuming the original mark is followed by a space). With the output of gate G3 at battery, FF2 becomes reset which returns lead ODM to battery. In this way, the data mark on lead ODM is at ground for a duration of 1360 μ sec.

3.03 If the original mark bit had been followed by another mark, FF1 would have been set again and lead ODM would have remained at ground potential for another 1360 μ sec.

3.04 Although temporary bit registrations, for the various outgoing data trunks, occur during different times in the sequential trunk scan, all data bits are transmitted simultaneously at time OTA of the end of trunk-scan cycle. The outgoing data message intended for one switch unit is transmitted serially one bit per data and digit store scan for each of the 47 bits of a data message.

C. Redundancy

3.05 Circuit redundancy is accomplished by supplying two outgoing data trunks per switch unit. There is one trunk associated with each of the two data control circuits. One data control circuit is used by the system while the other remains off line. Messages from the off-line data control circuit are inhibited in the data transmitter by the maintenance center.

4. INCOMING DATA TRUNK

A. General

4.01 Since the operation of the switch unit and control units are not synchronized, it is necessary to provide an incoming data trunk circuit which will recognize the presence of a received data bit and deliver it to the data control circuit at a time and in a form that is compatible with control unit operational techniques. Here the serial message, arriving at a bit rate of 643.4 bps on lead DA, is sampled by the assigned X-, Y-, Z-scanning leads (from the data control) at time T1

of the scan and fed to the data control circuit on lead ICDO.

4.02 The scan interval, occurring at a 735.3-bps rate, guarantees that each incoming bit (643.4 bps) will be sampled. Provision is made for preventing the sampling of the same bit twice through the use of an inhibit shift pulse to the memory register in the data control circuit (lead SH3).

B. Circuit Operation

4.03 The following references are made to the lower part of Fig. 6. A data mark ground, arriving on lead DA from the data receiver, enables a transmission gate for setting FF3. A 5- μ sec positive pulse every 1554 μ sec appears on lead SY to set FF1, which puts the set output at ground. Upon the return of SY to ground, the AND condition (inputs at ground) for gate G1 is satisfied and the ground output of G2 enables the transmission gate to allow FF2 to be set. Sometime within the next data control scan cycle (735.3 bps), the X-, Y-, Z- inputs assigned to this incoming data trunk will go to ground for 5 μ sec (T0-T4 inclusive). At time T1 of this scan interval, the last input (lead T10) to gate G3 goes to ground for 1 μ sec. For this 1- μ sec interval the G3 output will go to plus TRL battery. The inverted output of gate G4 then sets FF2. The ground output of the set side of FF2 sets FF3 if a data mark ground is present on the DA lead. The reset output of FF3 will go to plus battery. This battery appears as an input to the G6 (G8, G10, G12) OR distribution gate which results in a ground on lead ICDO. The duration of this ground (which starts at time T1 of the sampling interval) lasts until the appearance of the ϕ 5 battery pulse (1 μ sec at T5) from the clock circuit. This pulse resets FF2 which resets FF3 and terminates the ground on lead ICDO. Therefore, lead ICDO is a ground for 4- μ sec duration for each mark bit.

4.04 When FF2 is set, the resultant battery on the reset side (lead NSH-) appears as an input to the distribution OR gate G5 (G9, G11, G13) for a 4- μ sec duration. The output of G5, i.e., lead SH3, is held at ground for this 4- μ sec interval which permits the shift of the data bit in the data control circuit memory register.

4.05 If another scan interval occurs before the appearance of the next SY pulse, lead NSH will remain at ground. Then, when leads W40 and T20 go to ground during time 2 of word 4, lead SH3 will go to plus battery. (For this condition, gate G5 is used for the AND function.) The resultant 1- μ sec positive pulse inhibits the shift of the data bit in the data control memory register. Therefore, the second scan of the same data bit is inhibited.

4.06 FF1 must be reset (following recognition of the SY pulse by the data control scan) in order to set up the conditions for inhibiting the next scan should it occur before the next SY pulse. The reset of FF1 is accomplished in either of two ways:

(1) The first FF1 reset path occurs following the coincidence of the return of SY to ground and the appropriate scan which results in a 1- μ sec battery pulse from AND gate G5. This pulse resets FF1 and occurs whether the data bit is a mark or space.

(2) The second reset path occurs only when a data mark is present. When FF2 is set (as previously described), the set output of FF2 is gated to set FF3. The reset output of FF3 sets FF4. The output from the reset side of FF4 resets FF1. This reset path is used to cover the situation where the phasing of the input signals is such that the FF1 setting function by the SY pulse may still be present when the reset pulse from gate G5 occurs.

4.07 The incoming data word is received and scanned one bit at a time until all 12 or 14 bits have been received and placed in the data and digit store.

C. Redundancy

4.08 In the control unit data circuits (Fig. 1, 2, and 3) there are two incoming data trunk circuits for each regular data receiver. The inputs to each of these incoming data trunk circuits are from a single data receiver, and each set of outputs and scanning leads connects to its associated data control circuits. Likewise there are two outgoing data trunk circuits for each regular data transmitter. The data and scanning inputs are from the associated data control circuits and the

outputs from both outgoing data trunk circuits drive a single data transmitter

5. DATA LINKS AND TRANSFER CIRCUITS

A. General

5.01 To provide reliability for the interchange of data messages, both the control unit and switch units are equipped with data link transfer circuits. A view of the fundamental circuitry involved is given in Fig. 7, 8, and 9. It can be seen that reliability is accomplished in three ways:

(1) At the control unit, a spare data transmitter and receiver can be substituted for the regular circuits under control of the maintenance center. The arrangement is such that one spare serves a group of eight transmitters and receivers.

(2) Data transmitters and receivers are furnished at the switch unit as follows:

(a) In the 1A switch unit (Fig. 7) there are two data transmitters and two data receivers. The transmitter that is active is controlled by the transfer and alarms circuit. Both data receiver circuits receive the same data by the use of a splitting pad at their inputs. If difficulty is experienced with one receiver or associated circuits, service is continued but with traffic volume limitations.

(b) In the 2A switch unit (Fig. 8) there are two data transmitters and two data receivers. The transmitter and receiver that are active are connected to the data trunk pairs by contacts of relay S2 and to the switch controls by contacts of relay S5. Both switch controls receive the same data but it will be retained only by the switch control to which it is addressed. The loss of one circuit will cause the other circuit to become active and switch unit operation will continue normally.

(c) In the 3A switch unit (Fig. 9) there can be two or three data transmitters and two or three data receivers, depending upon the number of switch control circuits in the switch unit. Switch controls No. 0 and No. 1 normally operate with data receiver and transmitter No. 0. Switch controls No. 2 and

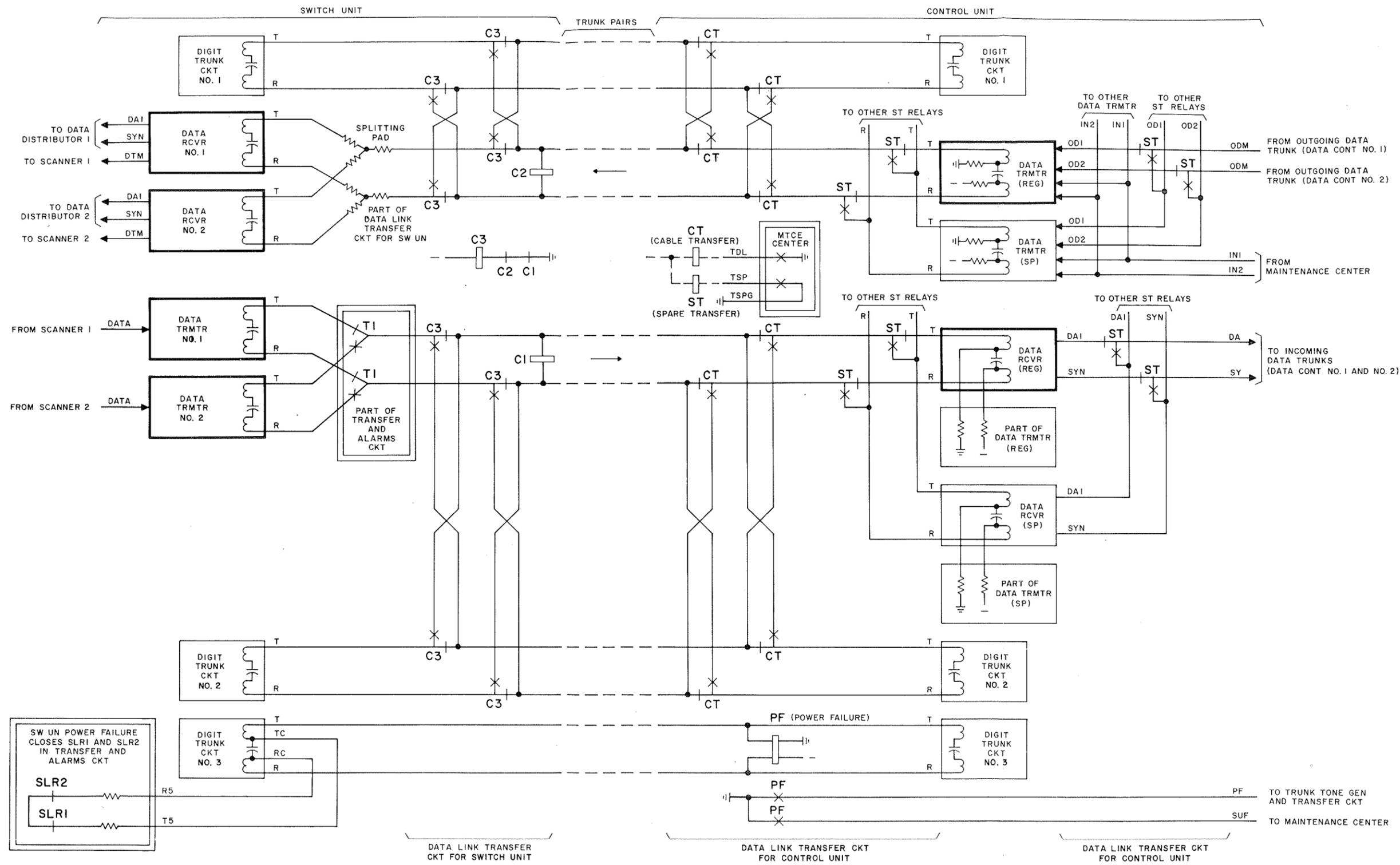


Fig. 7 — Data Links and Transfer Circuits for 1A Switch Unit

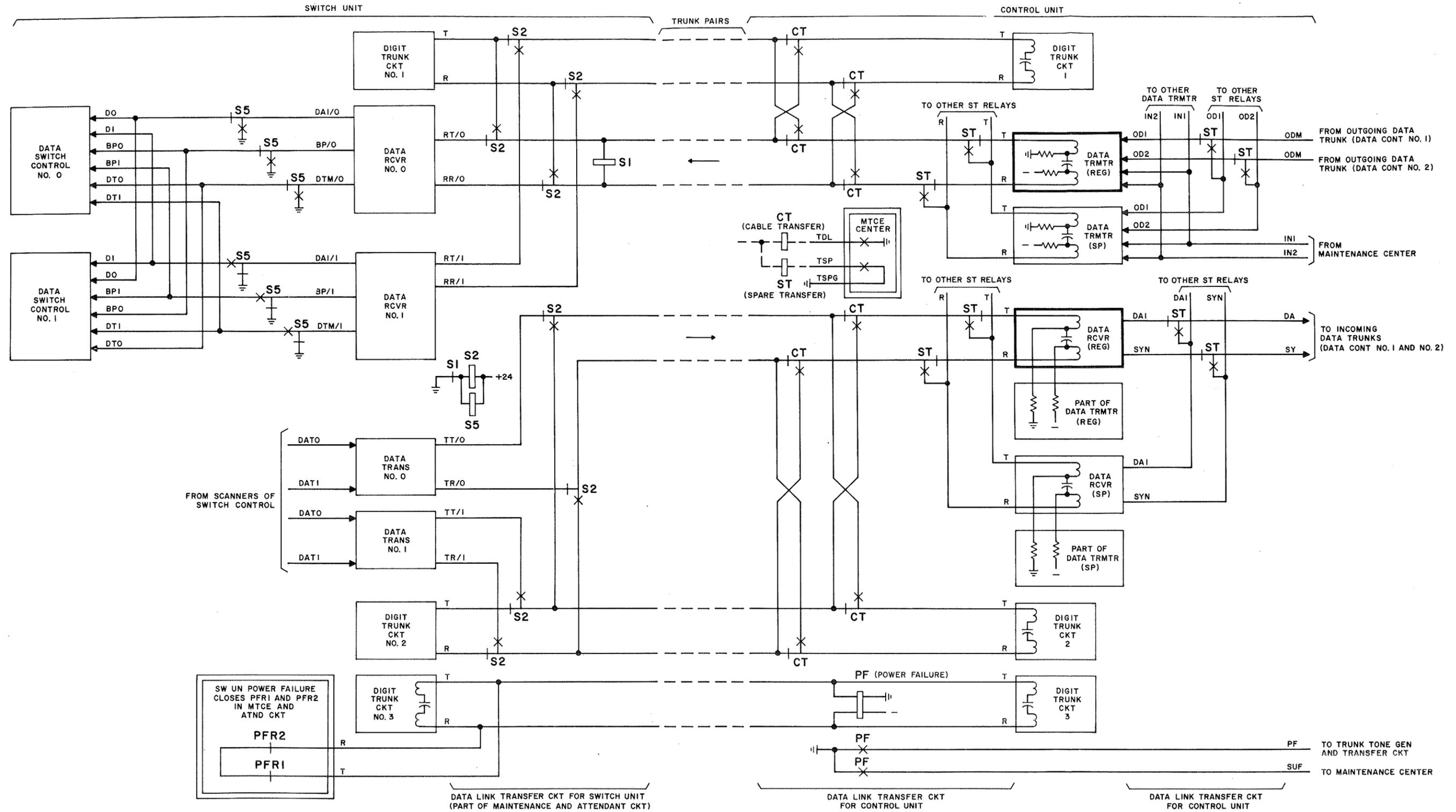


Fig. 8 — Data Links and Transfer Circuits for 2A Switch Unit

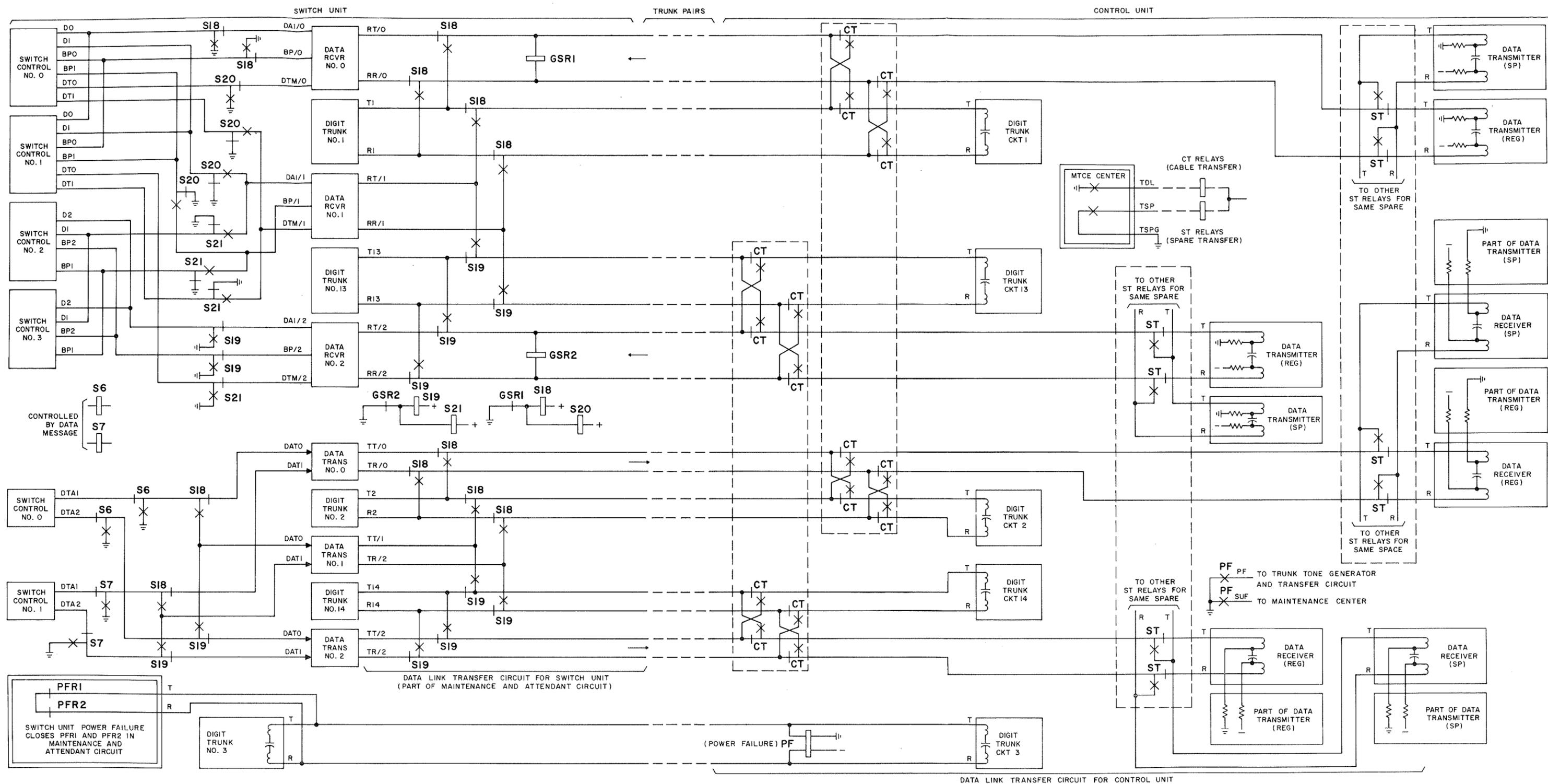


Fig. 9 — Data Links and Transfer Circuits for 3A Switch Unit

No. 3 normally operate with data receiver and transmitter No. 2. Data receiver and transmitter No. 1 act as spares for both the No. 0 and No. 2 circuits and are transferred under control of grand slam relay GSR1 or GSR2. All data messages to the control unit are generated by switch control No. 0 or No. 1. The loss of one data circuit will cause the spare circuit to be switched into service without affecting switch unit operation.

(3) Under control of the maintenance center, two cable pairs normally used for incoming and outgoing data (Fig. 7, 8, and 9) can be interchanged with two cable pairs associated with digit trunk circuits. In the event of a defective data cable pair, the incoming and outgoing data trunk pairs containing the defective cable pair are interchanged with associated digit trunk pairs, thus transferring the trouble, pending correction, to a digit trunk where the system reaction is less serious.

B. Cable Transfer

5.02 When system maintenance determines that an interchange of data and digit trunk pairs should be made, ground is put on the TDL lead by the control unit maintenance center. This completes the operate path for the cable transfer (CT) relay. Transfer contacts, associated with this relay, cause an interchange of the outgoing and incoming data trunk pairs with digit trunk pairs 1 and 2, respectively.

5.03 With a 1A switch unit (Fig. 7), when the CT relay in the control unit is not operated (normal condition) a loop current supplied by the associated data transmitter holds relays C1 and C2 in the switch unit operated. However, when a cable transfer is originated by the maintenance center in the control unit, the loop current is broken and relays C1 and C2 release. Relay C3 then operates and performs an interchange of data and digit trunks complementary to the one that occurred in the control unit.

5.04 For a 2A switch unit (Fig. 8), when the CT relay is not operated (normal condition), a loop current supplied by the associated data transmitter holds relay S1 in the switch unit operated. However, when a cable transfer is originated in

the control unit, the loop current is broken and relay S1 releases. Relays S2 and S5 then operate and perform an interchange of data and digit trunks complementary to the one that occurred in the control unit. A transfer of facilities is thus made at both ends of the trunk pairs.

5.05 For a 3A switch unit (Fig. 9), one set of the two sets of cables can be transferred. When neither of the CT relays is operated (normal condition), loop currents supplied by the associated data transmitters hold grand slam relays GSR1 and GSR2 in the switch unit operated. When a cable transfer is originated in the control unit, one of the CT relays will release and the loop current to the related relay (GSR1 or GSR2) in the switch unit is broken, releasing the switch unit relay. If GSR1 is released, relays S18 and S20 are operated, performing an interchange of data and digit trunk circuits complementary to the one that occurred in the control unit. This places data receiver No. 1 and data transmitter No. 1 in service in place of data receiver No. 0 and No. 1. If GSR2 is released, relays S19 and S21 are operated and a similar action occurs except data receiver and data transmitter No. 1 replaces data receiver and data transmitter No. 2. Relays S6 and S7 are controlled by data messages from the control unit. When relay S6 is operated, switch control No. 0 is disconnected from the data transmitters. When relay S7 is operated, switch control No. 1 is disconnected from the data transmitters.

5.06 The data and digit trunk pairs that are interchanged must have loop resistance and transmission characteristics that meet the requirements of both the data and digit circuits.

C. Control Unit Spare Data Circuit Transfer

5.07 If, for maintenance purposes, it is desired to remove a control unit regular data transmitter and receiver from service and substitute a spare, the maintenance center furnishes a ground on lead TSP of the data link transfer circuit. This causes the operation of the spare transfer (ST) relay which results in a complete transfer of all the leads to and from a regular to a spare transmitter and receiver. Transmitters and receivers are always transferred together, never singly. Transfer may be caused by either teletype request or system maintenance.

5.08 The equipment arrangement is such that one spare transmitter and receiver are available for substitution in place of the transmitter and receiver associated with any one of a group of eight switch units. Once a transfer has been made for one switch unit, a lockout condition is set up that prevents further transfers from taking place for any of the other seven switch units in the group.

D. Switch Unit Power Failure Alarm

5.09 Another function performed by the data link transfer circuit is to signal the control unit, via a supervisory relay PF (Fig. 7, 8, and 9) on digit trunk pair 3, when a switch unit power failure occurs. When switch unit power is normal, contacts of relays in the switch unit power failure circuit hold the power failure (PF) relay in an unoperated state. A switch unit power failure causes the relays of the power failure circuit to release. Contacts of these relays close, completing the circuit for loop current to operate the PF relay. PF relay contact closures give a ground to the trunk tone generator and transfer circuit and to the maintenance center, indicating that a power failure has occurred in this particular switch unit.

6. REFERENCES

6.01 The following SD drawings and associated circuit descriptions (CDs) give additional information. These are not attached.

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| Data Link Transfer Circuit for Switch Unit | SD-1H021-01 |
| Data Receiver Circuit for Switch or Control Unit | SD-1H031-01 |
| Data Transmitter Circuit for Switch or Control Unit | SD-1H032-01 |
| Incoming Data Trunk Circuit for Control Unit | SD-1H033-01 |
| Outgoing Data Trunk Circuit for Control Unit | SD-1H034-01 |
| Data Link Transfer Circuit for Control Unit | SD-1H054-01 |
| Switch Control Circuit for 2A Switch Unit | SD-1H120-01 |
| Maintenance and Attendant Circuit for 2A Switch Unit | SD-1H121-01 |
| Maintenance and Attendant Circuit for 3A Switch Unit | SD-1H206-01 |
| Data Modem for 3A Switch Units | SD-1H207-01 |