DIGIT RECEPTION AT CONTROL UNIT
DESCRIPTION OF SYSTEM OPERATION
NO. 101 ELECTRONIC SWITCHING SYSTEM

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1. INTRODUCTION TO DIGIT AREA

A. Function of Digit Circuits

1.01 Part of the outgoing message to the switch unit, originating in program control, contains information that instructs the switch unit to connect the subscriber to a particular idle digit trunk circuit on a time division basis. Program control also commands the digit receiver connector circuit (DRC) to make a time division connection between a like numbered control unit digit trunk circuit and one of the digit receiver circuits. Upon transmission of dial tone to the switch unit subscriber, the control unit is prepared to accept digit signals over the same trunk facility.

B. Circuit Arrangement

1.02 The digit trunk, receiver, and connector subsystem are shown in Fig. 1. There are two DRC circuits provided, one to process commands for connections to the odd numbered digit receivers and one for the even receivers (42 maximum).

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1.03 Each of the DRC circuits has access to all of the digit trunk circuits (128 maximum). Both program controls have access to both DRC circuits.

1.04 Each group of three digit receivers connects to a single digit distributor where the sampled receiver outputs are combined in an *or* gate. The distributor outputs (14 circuits for a fully equipped system) are multipled and deliver the digit information, now in dc form, to 2-out-of-8 translators in each of two digit control circuits.

1.05 Scanning of the digit information every 1360 μsec (leads X-, Y-, Z-) is provided by data controls 1 and 2.

1.06 Digit controls 1 and 2, on leads TOW, command the digit receiver to gate off the dial tone in the case of a time-out. Also, via the remove data store reset (RDSR) lead, the digit control circuits remove the reset data store pulse. The maintenance center, with appropriate ground or battery on inhibit leads IN1 and IN2, determines which of the two digit control circuits has control over the reset dial tone (TOW) and RDSR functions.

C. Circuit Operation

1.07 A 2-frequency tone representing a specific dialed digit from a TOUCH-TONE set, arrives from the switch unit and is entered into a digit trunk circuit. When the digits originate from a rotary dial, the dc dialing pulses are converted in the switch unit digit trunk circuit to a two-tone signal. Horizontal (H-) and vertical (V-) leads, from the digit receiver connector translator, enable a time division switch which closes a path for the received signal through the digit trunk circuit to a common bus. Similar leads activate the time division switch in a digit receiver and connect the receiver to the same bus for the same interval of time. The original ac signal appears at the input to the digit receiver in 2-μsec increments every 80 μsec. After filtering, which removes the high frequency components and restores the 2-frequency tone, the signal is entered into a TOUCH-TONE calling receiver for detection and conversion to dc form. Scanning pulses on leads X-, Y-, Z- from the data control circuit, appearing once every 1360 μsec for 5 μsec, sample the two dc outputs and present them to the digit control circuits via the digit distributor *or* gates. The original tone, consisting of two frequencies, one low and one high, is now represented by two 5-μsec ground pulses appearing on leads L- and H-. A 2-out-of-8 translation takes place in the digit control circuit.

1.08 In addition to the above, the digit circuits also serve another purpose, that is, to send dial tone to the switch unit over the assigned digit trunk pair. This is accomplished by using part of the initial command to the DRC (from program control) to enable the dial tone function of the DRC receiver number translator. This results in enabling the dial tone gate via receiver translator dial tone horizontal output leads (DTH0 to DTH3) and the transmission of dial tone to the switch unit subscriber. At the same time, a sampled output is sent to the digit control circuit on dial tone lead DTO1 to ready the digit control for accepting digits.

2. DIGIT RECEPTION

A. General

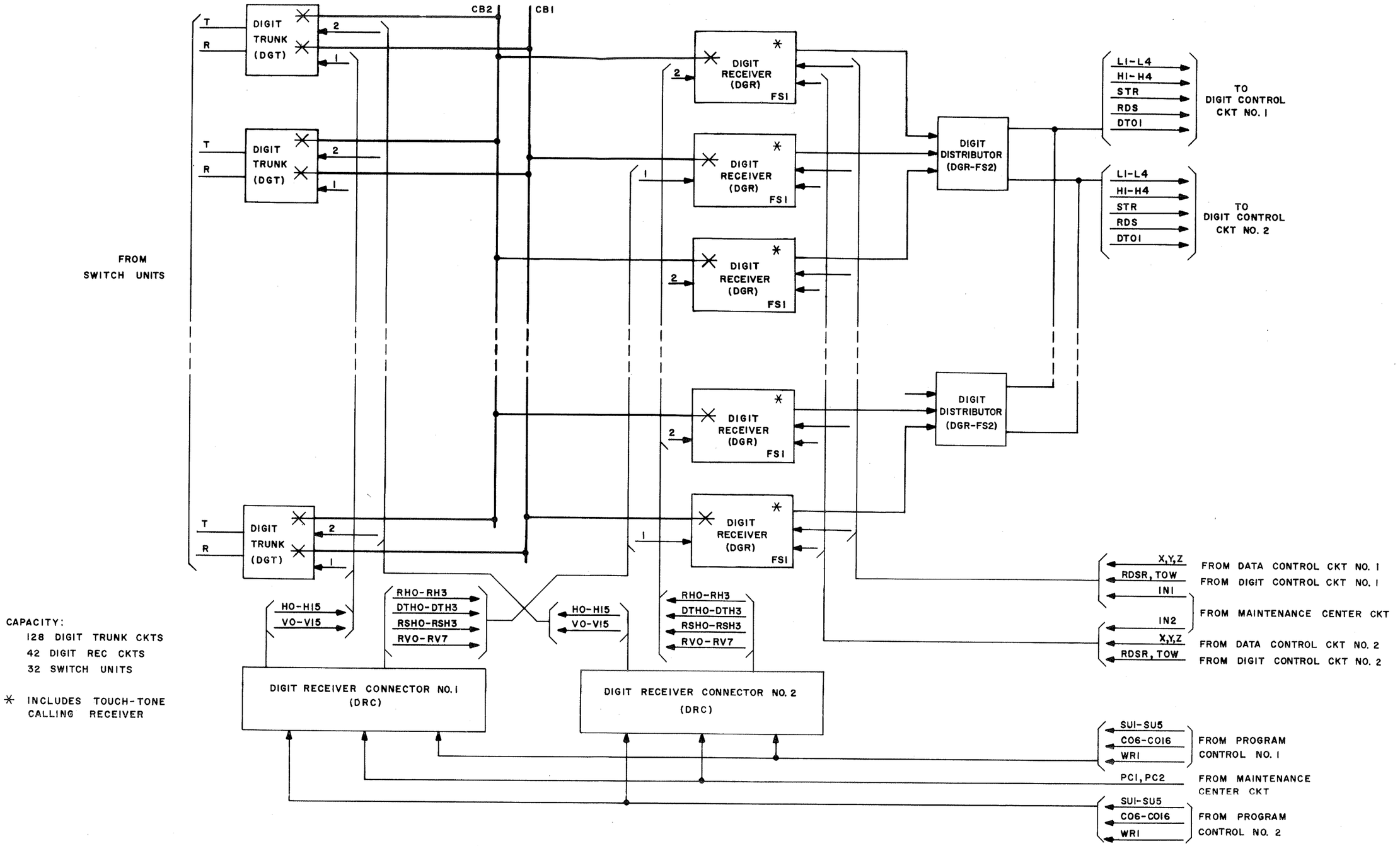
2.01 The main function of the digit receiver is to accept TOUCH-TONE signals from the switch unit, decode them in an associated TOUCH-TONE calling receiver, and present them to a digit control circuit. An intermediate circuit, the digit trunk, faces the digit trunk pair. The sections that follow make reference to Fig. 2.

B. Transmission Path

2.02 The operation of the digit trunk and receiver circuits depends on the simultaneous closing of time division switches in both circuits by translator output pulses from the digit receiver connector circuit (DRC). Two specific pairs of leads H- and V- to the trunk and horizontal transmission (HT) and vertical transmission (VT) to the receiver cause the switches to close to a common bus for a 2-μsec interval every 80 μsec. A TOUCH-TONE signal, arriving from a switch unit, will pass through the time division network during this timed interval and be restored to its basic 2-frequency tone at the output of the low pass filter in the TOUCH-TONE time division switch (TTTDS) of the digit receiver.

C. TOUCH-TONE Calling Receiver

2.03 The output of the transmission switch enters the TOUCH-TONE calling receiver where the signals are decoded and converted to



CAPACITY:
- 128 DIGIT TRUNK CKTS
- 42 DIGIT REC CKTS
- 32 SWITCH UNITS

✳ INCLUDES TOUCH-TONE CALLING RECEIVER

Fig. 1 – Control Unit Digit Trunk, Receiver and Connector Subsystem

battery. pulses. The TOUCH-TONE calling receiver, SD-98148-01, in production for other applications, is considered to be a part of the digit receiver for descriptive purposes. The original 2-frequency tone, after detection, appears as one low group output (LG1-LG4) and one high group output (HG1-HG4). Each pulse is timed to have a duration of approximately 45 msec. Accompanying these pulses is lead STR which is present as long as a legitimate TOUCH-TONE signal appears on the receiver input. These outputs are not compatible with the system logic input requirements and, therefore, a voltage translation is required. Besides adjusting the voltage to standard logic levels, the voltage translator circuit inverts its input signal polarity.

D. Digit Receiver Scanning

2.04 Digit signals may be present in many receivers at any one time and are available to the digit control circuit. However, in order to differentiate between signals from the various digit receivers, the data control circuit originates scanning leads (X-, Y-, Z-) which are assigned to each receiver according to receiver number. (The scanning leads from data control originate in the store address counter and are gated through the trunk and digit receiver scanner to the digit receiver circuits.) The combination of the assigned X-, Y-, and Z- leads causes an effective 5 μsec ground for sampling purposes. When the appropriate scan interval occurs, an interrogation of the contents of one particular receiver takes place. Two digit sampling circuits (Fig. 2) are provided, one for each of two digit-data control circuits.

E. Digit Distribution

2.05 The sampled digits are fed through the digit distributor gates which provide an *or* function for groups of three digit receiver outputs. This furnishes the correct signal polarity (ground) to the digit control circuit and satisfies equipment considerations.

F. Dial Tone

2.06 The digit receiver circuit also contains circuitry to transmit dial tone from the control unit to the switch unit subscriber. Part of the initial command from program control causes the DRC receiver translator to enable time division switch TDS1 (Fig. 2) for a single 2-μsec interval during the appropriate time slot for this receiver. This causes a positive battery pulse to set dial tone (SDT) flip-flop. The positive output of SDT is used to enable the dial tone gate resulting in the transmission of dial tone through the same time division network as used for TOUCH-TONE signal reception but in the reverse direction. The ground output from SDT is scanned during the appropriate interval and sent to the digit control circuit via lead DTO1 in order to put the digit control in a condition for accepting digits and starting the time-out count.

2.07 Removal of dial tone is accomplished by resetting the flip-flop SDT with the first signal tones ready (STR) pulse occurring coincident with the LG- and HG- TOUCH-TONE receiver outputs. This action also removes the ground pulse on lead DTO1 to the digit control circuit.

2.08 A second reset path for SDT is derived from lead TOW from one of the two digit control circuits. The condition of inhibit leads IN1 and IN2 from the maintenance center determines which of the two digit control circuits will have access. Lead TOW will drop to ground when a predetermined time-out interval has elapsed and, after being scanned, the resulting battery pulse resets flip-flop SDT.

G. Digit-Data Store Reset

2.09 Upon completion of dialing, the digit trunk to digit receiver time division connection is no longer required. Therefore, program control initiates a command to the DRC to remove the connection and to reset the digit-data store area associated with this particular digit receiver. This command causes the receiver translator of the DRC to produce a single 2-μsec pulse between leads VT and horizontal reset data store (HRD) to energize time division switch TDS2. The resulting battery pulse sets reset data store (RD1) flip-flop and during the appropriate scan time causes a ground to appear on reset data store (RDS) lead to the digit control circuits for clearing the digit-data store.

H. Reset of Flip-Flop RD1

2.10 Flip-flop RD1 remains in the set condition until the next time the receiver is selected by program control. When the dial tone indica-

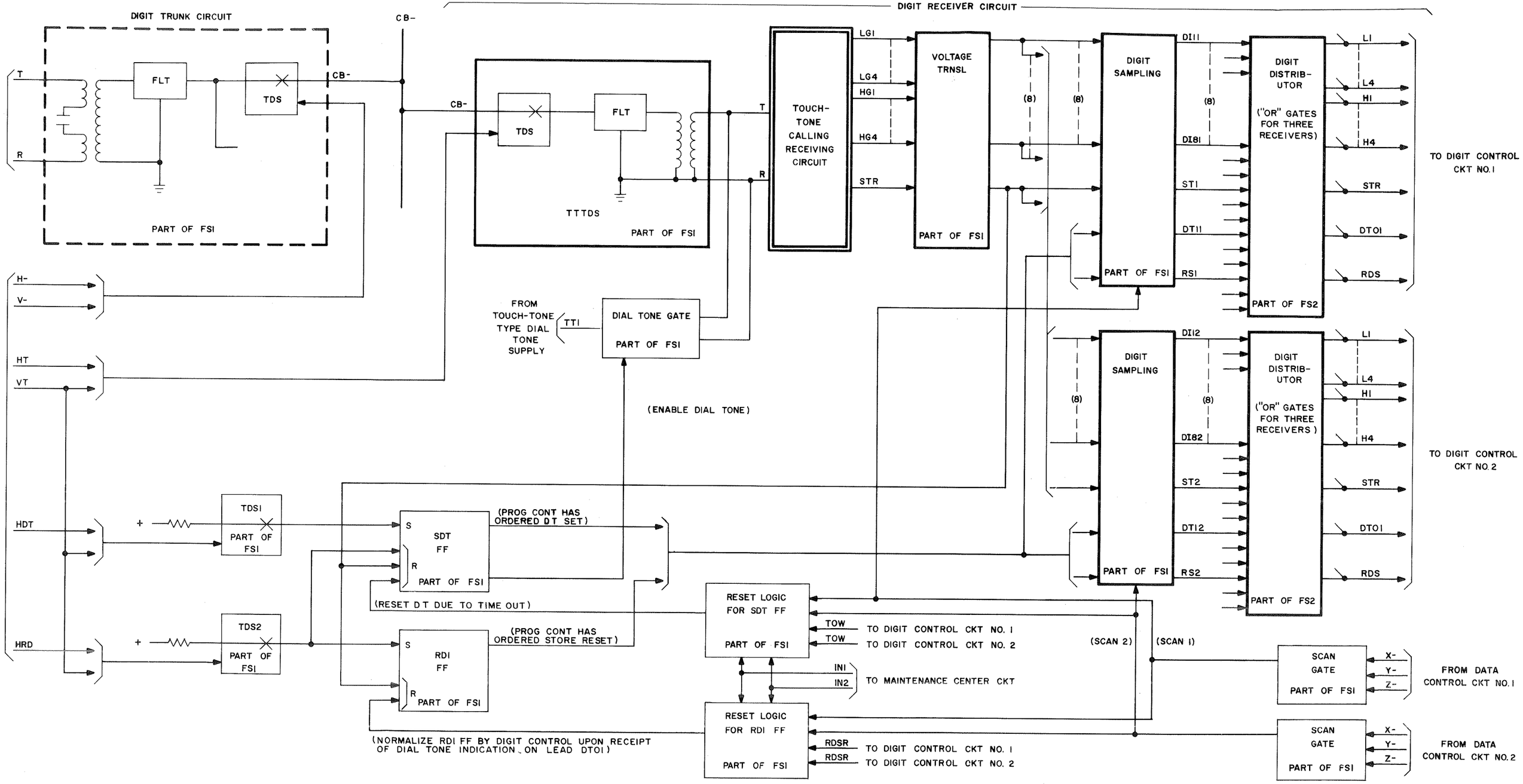


Fig. 2 – Digit Receiver Block Diagram

DIGIT RECEIVER CIRCUIT

DIGIT TRUNK CIRCUIT

FROM SWITCH UNIT

T

R

FLT

TDS

CB-

PART OF FSI

CB-

TDS

FLT

TTTDS

PART OF FSI

T

R

TOUCH-TONE CALLING RECEIVING CIRCUIT

LGI

LG4

HGI

HG4

STR

VOLTAGE TRNSL

PART OF FSI

(8)

(8)

DIGIT SAMPLING

PART OF FSI

DIGIT SAMPLING

(8)

PART OF FSI

H-

V-

HT

VT

FROM TOUCH-TONE TYPE DIAL TONE SUPPLY

TTI

DIAL TONE GATE

PART OF FSI

(ENABLE DIAL TONE)

FROM DIGIT RECEIVER CONNECTOR CKT

HDT

HRD

\+

TDSI

PART OF FSI

TDS2

PART OF FSI

S

SDT FF

R

PART OF FSI

(PROG CONT HAS ORDERED DT SET)

(RESET DT DUE TO TIME OUT)

S

RDI FF

R

PART OF FSI

(PROG CONT HAS ORDERED STORE RESET)

(NORMALIZE RDI FF BY DIGIT CONTROL UPON RECEIPT OF DIAL TONE INDICATION ON LEAD DTOI)

RESET LOGIC FOR SDT FF

PART OF FSI

TOW TO DIGIT CONTROL CKT NO. 1

TOW TO DIGIT CONTROL CKT NO. 2

(SCAN 2)

(SCA

INI

IN2

TO MAINTENANCE CENTER CKT

RESET LOGIC FOR RDI FF

PART OF FSI

RDSR TO DIGIT CONTROL CKT NO. 1

RDSR TO DIGIT CONTROL CKT NO. 2

tion is sent to digit control via lead DTO1, digit control generates a ground on lead RDSR. When this ground is scanned by the online data control, the resulting battery pulse resets flip-flop RD1. This action removes the store clearing pulse on lead RDS and enables a path for storing digit information in the store area assigned to this particular receiver.

2.11 A second reset path for RD1 occurs upon receipt of the first dialed digit. This is the same reset pulse that resets the dial tone flip-flop SDT (to disable dial tone), but when it is used to reset RD1 it merely guarantees that the store is in a condition to accept digit information.

3. DIGIT RECEIVER CONNECTOR — GENERAL

A. Basic Features

3.01 The digit receiver connector constitutes the heart of the digit subsystem. Its primary function is to translate binary coded information from program control into output pulses suitable for completing time division connections between specific digit receiver and trunk circuits. Secondary functions include those that enable dial tone and cause a reset of the digit-data store on command.

3.02 The complexity of the DRC circuit is due to its nonsynchronous operation with respect to the program control (driven by the system clock) and the large storage capacity required to maintain a multitude of simultaneous time division connections.

3.03 A large part of the digit receiver connector (DRC) operates continually in a cyclic manner regardless of the state of the input signals from program control. These circuits are the clock, receiver address binary counter, register enable and translator drive, horizontal access to the memory array, and the greater part of the horizontal and vertical receiver translator circuitry. Fig. 3 shows the relative position of these circuits within the DRC.

3.04 Many sections of the DRC depend on the clock and receiver address binary counter outputs for their operation. For this reason, the clock and binary counter will be discussed before treating other circuitry.

B. Clock Operation

3.05 The DRC clock circuit consists of a crystal controlled 312.5-kc oscillator providing 0.5-μsec output pulse every 3.2 μsec. These pulses drive a 3-μsec delay line having 30 equally spaced taps with 0.1 μsec between each tap. The delay line outputs are used to control the state of various flip-flop whose outputs are combined in gates to satisfy timing and load requirements.

3.06 There are 13 clock outputs used throughout the DRC. The phasing and duration of each output are shown in Fig. 4. They provide the means for sequencing all the DRC functions. For instance, one of these outputs is the advance (ADV) lead, used to advance the receiver address binary counter. This lead carries a positive 0.5 μsec pulse beginning at time 0 (T0) and ending at time 5 (T5) and recurring every 3.2 μsec. The delay line tap number is used to designate the timed interval. The ADV pulse, determined by taps 0 and 5, is said to be active during the interval T0 to T5.

3.07 The clock circuits in each of the two DRC circuits operate independently of each other and of the remainder of the system.

C. Receiver Address Binary Counter

3.08 Fig. 5 depicts the receiver address binary counter and output waveforms. This is a 5-stage, parallel advance counter and is unique in that it counts from state 1 through 25 and recycles.

3.09 The advance gates (G1 to G6) are diode logic with no inversion. They are ***and*** gates for positive voltages, ie, when all the inputs are positive the output is positive. However, the active state of the gate as far as the binary stage is concerned occurs with the appearance of the negative advance pulse. The resulting negative transition is coupled via a 510-$\mu\mu$f capacitor to the negative side of a diode which drives the positive collector of the binary counter (BC) stage transistor to ground and reverses the output states. (Positive transitions are blocked by the diode.) Amplifiers on each side of the BC stage invert the output voltages.

3.10 The BC advance takes place by setting up the appropriate positive BC states on the gates and then grounding the gate output via the advance pulse.

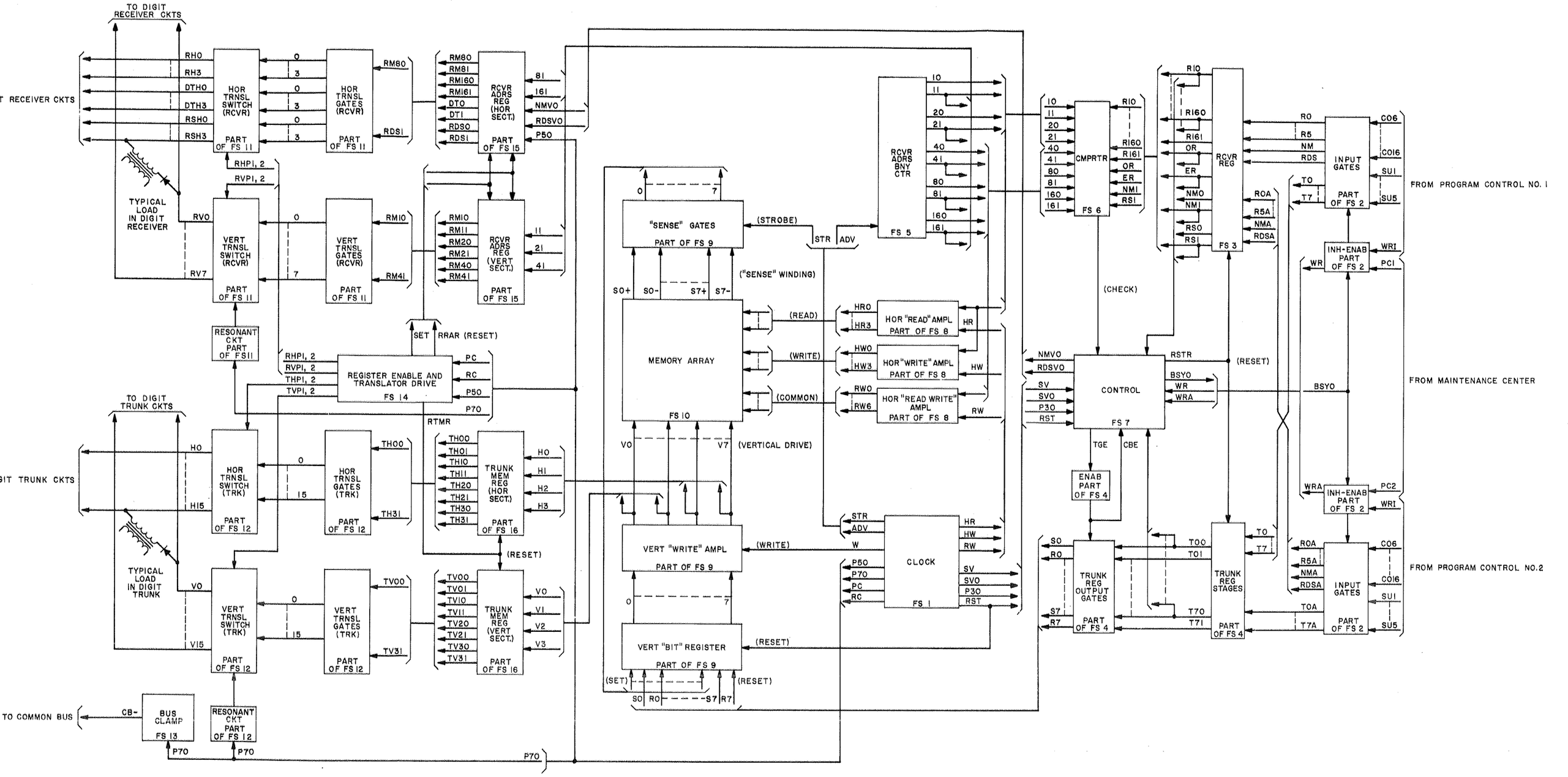
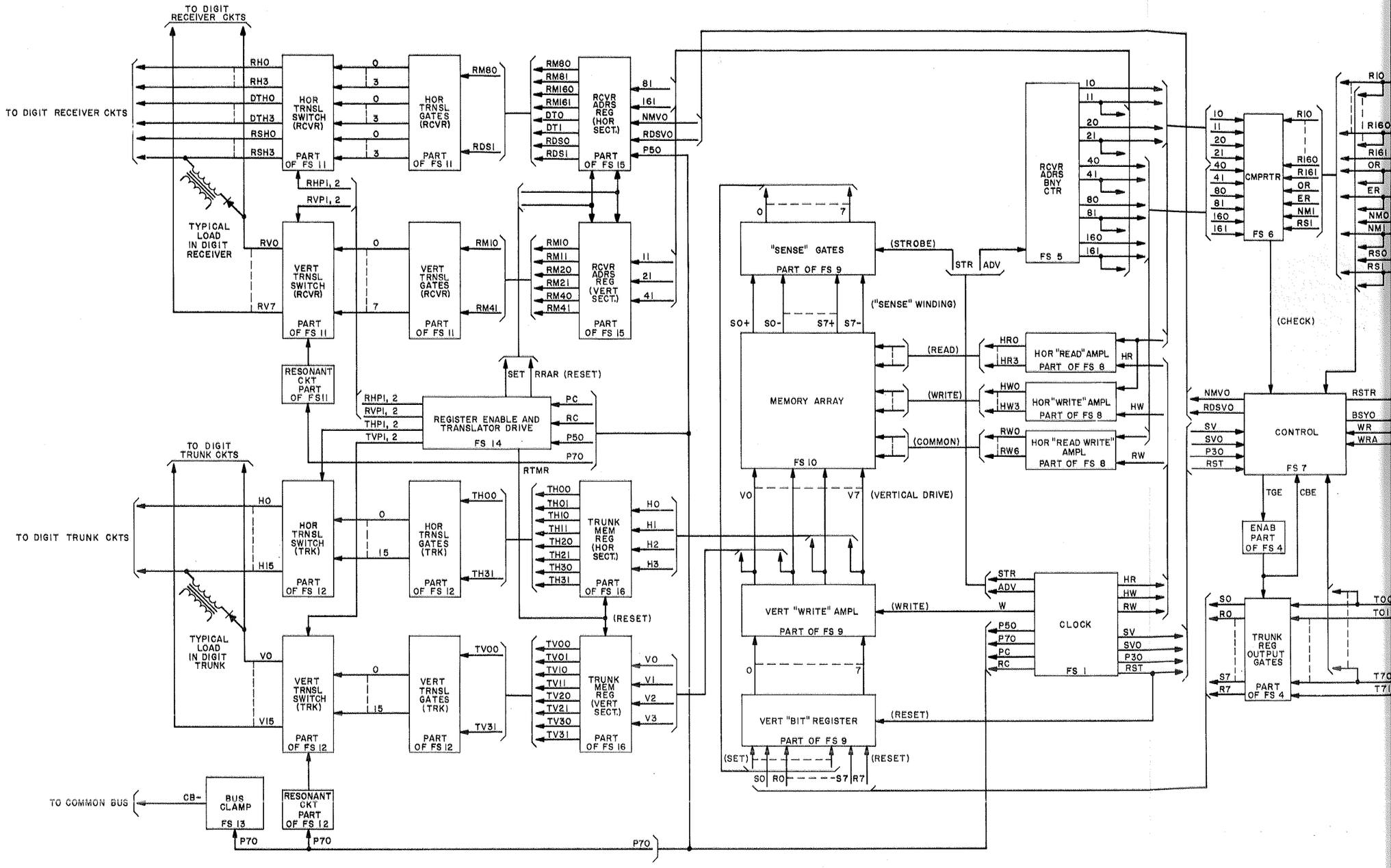
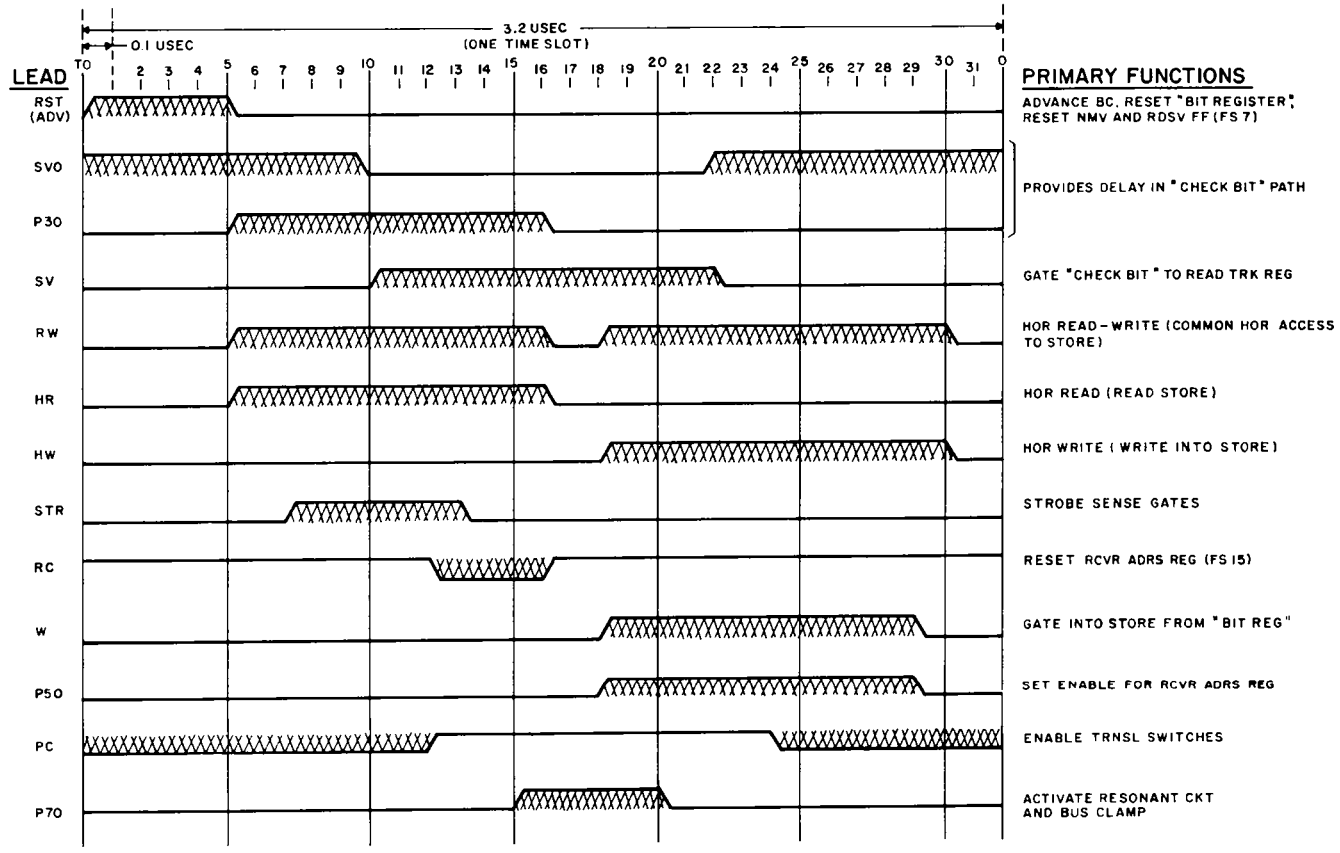


Fig. 3 – Digit Receiver Connector Block Diagram


TO DIGIT RECEIVER CKTS
RH0
RH3
DTH0
DTH3
RSH0
RSH3
HOR TRNSL SWITCH (RCVR)
PART OF FS 11
HOR TRNSL GATES (RCVR)
RM80
RDS1
RCVR ADRS REG (HOR SECT.)
PART OF FS 15
RM80
RM81
RM160
RM161
DT0
DT1
RDS0
RDS1
81
161
NMV0
RDSV0
P50
TYPICAL LOAD IN DIGIT RECEIVER
RHP1, 2
RVP1, 2
RV0
RV7
VERT TRNSL SWITCH (RCVR)
VERT TRNSL GATES (RCVR)
RM10
RM41
RCVR ADRS REG (VERT SECT.)
RM10
RM11
RM20
RM21
RM40
RM41
11
21
41
RESONANT CKT PART OF FS11
SET
RRAR (RESET)
REGISTER ENABLE AND TRANSLATOR DRIVE
FS 14
RHP1, 2
RVP1, 2
THP1, 2
TVP1, 2
PC
RC
P50
P70
RTMR
TO DIGIT TRUNK CKTS
H0
H15
HOR TRNSL SWITCH (TRK)
PART OF FS 12
HOR TRNSL GATES (TRK)
TH00
TH31
TRUNK MEM REG (HOR SECT.)
PART OF FS 16
TH00
TH01
TH10
TH11
TH20
TH21
TH30
TH31
H0
H1
H2
H3
(RESET)
TYPICAL LOAD IN DIGIT TRUNK
V0
V15
VERT TRNSL SWITCH (TRK)
VERT TRNSL GATES (TRK)
TV00
TV31
TRUNK MEM REG (VERT SECT.)
TV00
TV01
TV10
TV11
TV20
TV21
TV30
TV31
V0
V1
V2
V3
TO COMMON BUS
CB-
BUS CLAMP
FS 13
RESONANT CKT PART OF FS 12
P70
"SENSE" GATES
PART OF FS 9
(STROBE)
STR
ADV
RCVR ADRS BNY CTR
FS 5
("SENSE" WINDING)
SO+
SO-
S7+
S7-
MEMORY ARRAY
FS 10
(READ)
(WRITE)
(COMMON)
HR0
HR3
HOR "READ" AMPL PART OF FS 8
HR
HW0
HW3
HOR "WRITE" AMPL PART OF FS 8
HW
RW0
RW6
HOR "READ WRITE" AMPL PART OF FS 8
RW
V0
V7
(VERTICAL DRIVE)
VERT "WRITE" AMPL
PART OF FS 9
(WRITE)
VERT "BIT" REGISTER
PART OF FS 9
(RESET)
(SET)
S0
R0
S7
R7
CMPRTR
FS 6
RI0
RI60
RI61
OR
ER
NMI
RSI
(CHECK)
CONTROL
FS 7
NMV0
RDSV0
SV
SV0
P30
RST
RSTR
BSY0
WR
WRA
TGE
CBE
ENAB PART OF FS 4
CLOCK
FS 1
W
P50
P70
PC
RC
TRUNK REG OUTPUT GATES
PART OF FS 4
TO0
TO1
T7
T7I



NOTE - SHADED AREAS DENOTE ACTIVE PERIOD FOR LISTED FUNCTIONS

Fig. 4 – Clock Output Pulses and Their Primary Functions

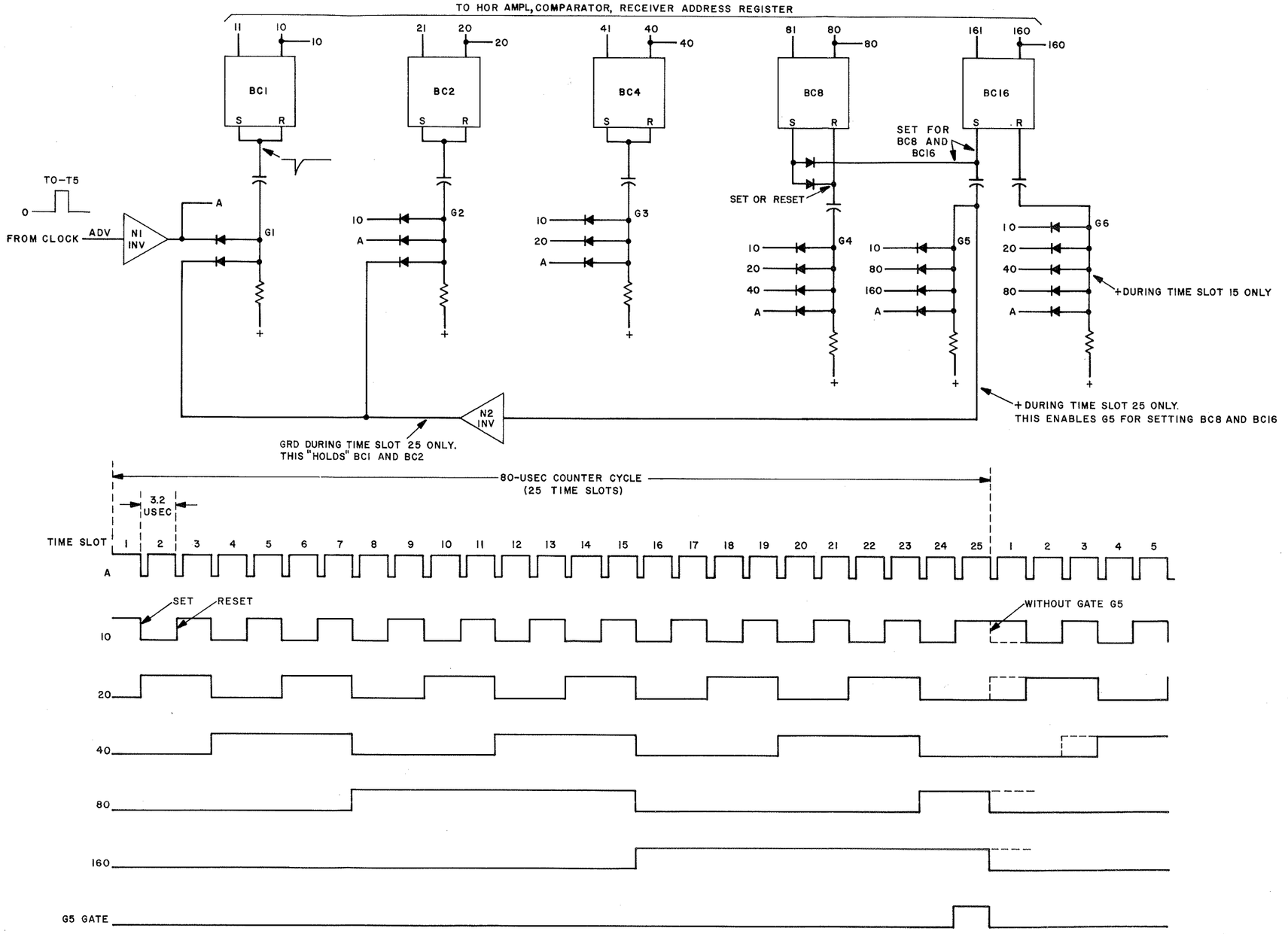


Fig. 5 – Receiver Address Binary Counter and Waveforms

3.11 The BC operation is more easily understood by assuming that it runs in the conventional manner, for a parallel advance counter, from count 1 (00001) to count 25 (11001). At this time, counter state 11001 (25) must be changed to 00001 (1). At time 25, the BC count is such that stages 1, 8, and 16 have a positive voltage on their reset side. This is true only at count 25 and therefore these states can be used to return the counter to the 1 count. To change from count 11001 to 00001, BC1, BC2, and BC4 must be held and BC8 and BC16 must be set. This is accomplished by ***anding*** the reset side of BC1, BC8, BC16, and the advance pulse A in gate G5 and then inverting the output voltage in gate N2 to give a ground during the interval of count 25. This effectively holds BC1 and BC2 by inhibiting the next advance pulse. BC4 is held by the ground on lead 20 of gate G3.

3.12 The remaining action necessary to return count 25 to count 1 is to set stages BC8 and BC16. The same gate (G5) that holds BC1 and BC2 is used to set stages BC8 and BC16 to ground at the leading edge of the next advance pulse. The resulting state for all stages (BC16, BC8, BC4, BC2, and BC1) becomes 00001 or count 1. Recurrence of the advance pulse (every 3.2 μsec) advances the counter through to count 25 and then recycles as described.

3.13 To guarantee against lockup when the counter is first powered or following voltage surges, special consideration is given to advancing stages BC8 and BC16. The advance gate G4 will set or reset BC8 depending on its previous state. (The set gate, G5, for BC16 also sets BC8 following count 25 as previously described.) The reset gate for BC16 is enabled at count 15 only. The result of this treatment is to allow the counter to advance even though it may start up in an unwanted state, ie, state 0 or states 26 to 31.

3.14 The sequence diagram in Fig. 5 shows the state of the reset side of each BC stage for each time slot. One time slot refers to one of the twenty-five 3.2-μsec intervals. Various circuits within the DRC use combinations of BC outputs.

3.15 Reference to these waveforms, remembering that the reset or "0" side of the binary counter stage is shown, will simplify the understanding of the connecting circuits.

4. PROGRAM CONTROL COMMAND REGISTRATION

A. Lead Identification

4.01 As shown in Fig. 3, two identical sets of input gates are provided to accept commands from either of two program controls. Both sets of gates are controlled by a lead (BSY0), generated within the DRC, which inhibits the message write-in when this connector is processing a previous command. Program control leads, PC1 and PC2, from the maintenance center, enable the proper gates according to which program control is active. The WRI lead carries a 3-μsec positive pulse, coincident with the command to direct the command to the DRC circuits only.

4.02 The switch unit (SU) number is contained on leads SU1 to SU5, in binary form with SU1 containing the least significant bit. Trunk number leads CO8, CO9, and CO10 give the digit trunk number with the least significant bit in CO8.

4.03 Receiver number leads CO11 through CO16 carry the digit receiver number assigned to a specific connection. When lead CO11 is ground, it indicates that this command is intended for the ***odd*** DRC (DRC No. 1). A positive voltage directs the message to the ***even*** DRC (No. 2). (The technique for accomplishing this will be discussed later in the text.) CO11 is the least significant bit of the digit receiver number. The remaining portion of the digit receiver number occurs on leads CO12 through CO16. This serves to determine the memory array time slot number to be used for trunk and switch unit number storage.

4.04 A ground on the new message bit lead (CO7) indicates that this is a new message and that dial tone should be sent, via the assigned digit receiver and trunk circuits, to the switch unit subscriber.

4.05 The reset data store bit lead (CO6) carries the command to reset the digit-data store area assigned to this digit receiver. In normal operation, this bit when accompanied by the appropriate receiver number and zeros for the

switch unit and trunk numbers, also removes the transmission time division connection after dialing has been completed.

B. Temporary Storage of Command

4.06 Any time the DRC is idle, a program control command will pass through the input gates and be temporarily stored in the receiver and trunk register stages. The trunk and switch unit number will remain in the trunk register awaiting the trunk gate enable (TGE) pulse (Fig. 3). However, the receiver number passes on to the comparator and control circuits immediately. The receiver and trunk numbers remain in their respective registers until the command has been processed, the trunk and switch unit numbers have been stored in the memory array, and the control timer cycle completed.

C. Receiver Number Comparison

4.07 Following registration of the command, one of the first actions within the DRC is the comparison of the registered receiver number and the state of the receiver address binary counter. This will eventually determine the position in the memory array to be used for storage. A comparator check is accomplished in the following manner. At some time within the 80-μsec cycle period following registration, the receiver number and the binary counter state will agree. Also, a check is made to ensure that a dial tone or reset data store bit is registered and that the receiver number is directed to this particular ***odd*** or ***even*** DRC. When all these conditions have been satisfied, a positive pulse will occur on lead CHK, which, after gating and inversion, appears on lead TGE as a ground. (See Fig. 6.) This is a signal to gate the trunk and switch unit number from the trunk register into the appropriate memory array time slot during this 3.2-μsec time interval. Meanwhile, the proper time slot has been selected by horizontal write leads HW- and RW-, derived from the clock and receiver address binary counter through the horizontal access circuits.

D. Control Logic

4.08 Fig. 6 breaks down the control logic into four basic parts as described in the following paragraphs.

Dial Tone and Reset Data Store Circuits

4.09 This circuit gates the bit appearing on lead NM1 or RS1, when there has been a comparator check (CBE), into a flip-flop for temporary storage until the next appearance of RST (T0 to T5). This insures that the dial tone and reset data store functions of the receiver translator will be enabled only during the assigned time slot.

Trunk Gate Enable (TGE) Circuit

4.10 During clock time T10 to T22 (lead SV), provided there has been a comparator check (lead CHK), lead TGE will go to ground to permit gating from the trunk register to the memory array. At the termination of SV, T22, a positive pulse starts the 10-μsec timing monopulser.

Timing Circuits

4.11 Upon registration of a dial tone or reset data store bit, the 120-μsec timer (monopulser) is started. If, for any reason an illegitimate receiver number is registered, there will be no check, and the timer will time out after 120 μsec and the receiver and trunk registers will be reset by a positive pulse on reset register lead (RSTR). Also, via lead BYS0, the DRC is made available for subsequent commands.

4.12 If the registered receiver number and the DRC number do not match with respect to the ***odd*** or ***even*** aspect, the 10-μsec monopulser will be started immediately. At the end of 10 μsec, the 120-μsec timer will be reset. This also results in the receiver and trunk register being reset.

4.13 When the normal situation exists, that is there has been a comparator check, the 10-μsec monopulser is started by a pulse from the trunk gate enable circuit. Again, at the end of the 10-μsec period the 120-μsec timer is reset, resulting in the receiver and trunk registers being reset and made available for a subsequent registration. In this way, the receiver and trunk registers are cleared regardless of the legitimacy of the command from program control.

Digit Receiver Connector (DRC) Busy

4.14 One of the immediate effects of any registered command is the activation of a downcheck circuit. This is nothing more than a large ***or*** gate which combines the outputs of

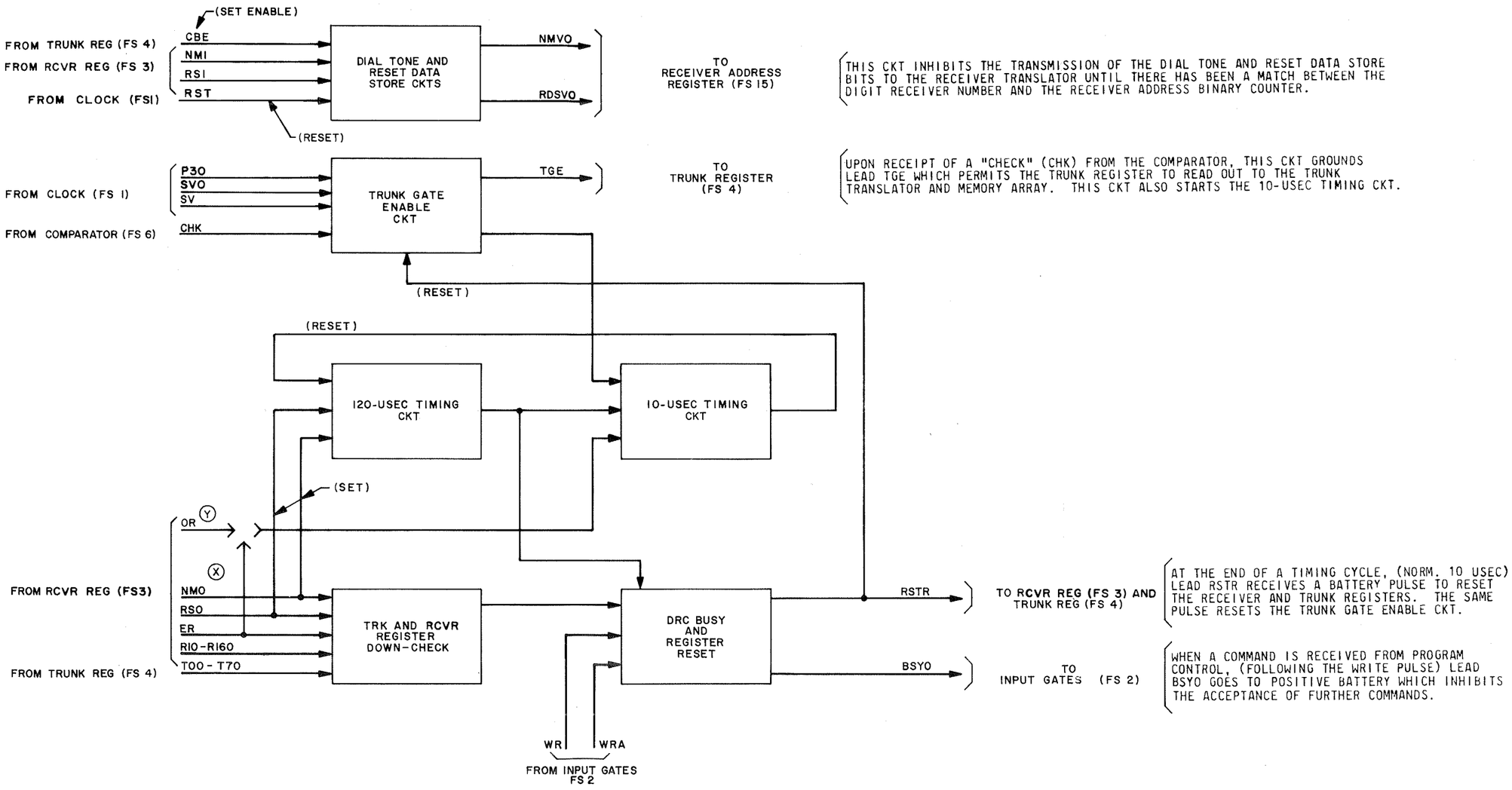


Fig. 6 – The Four Functions of the Control Circuit (FS7)

each receiver and trunk register stage. The resulting gate output, ground, ***anded*** with the termination of the program control write pulse, is used to set a busy flip-flop. The flip-flop positive output, on lead BSY0, disables the input gates (Fig. 3) which prevents acceptance of further commands until the receiver and trunk registers have been reset (approximately 10 μsec later).

E. Dial Tone

4.15 The receiver number translation is relatively straightforward as seen in Fig. 3. Once the comparator match has been made and the trunk and switch unit number stored in the proper time slot of the memory array, there is no further need for the receiver number bits with the exception of the dial tone or reset data store bit. Special consideration is given to these two functions before they are translated in order to guarantee that either of them will appear only once at the assigned digit receiver and that a comparator match has occurred. It should be noted that for a particular digit receiver the transmission gate is enabled every 80 μsec with the exception of the initial time slot when the dial tone or reset data store bit appears. This occurs as a result of receiver translator action.

4.16 In Fig. 7 the logic and sequence diagram for a dial tone command is detailed. The dial tone bit is included as a part of the receiver number portion of the initial message to the DRC from program control. The dial tone bit is called a new message bit and therefore the designation NM is used when referring to it.

4.17 Again, referring to Fig. 7, the dial tone bit appears as a ground on lead CO7. When the supplementary inputs are in an appropriate state, gate NM will go positive for approximately 3 μsec which will set flip-flop NM. At T10 to T22, lead CBE, derived from the comparator output when a check occurs, will go to ground and when this is ***anded*** with the ground side of flip-flop NM, a positive output occurs to set special flip-flop NMV. [The following RST (T0 to T5) will reset NMV causing this to be the only pulse from NMV. The message will be completely processed and cleared from the registers before the next comparator check is attempted 80 μsec later.] The positive output from flip-flop NMV (T10 to T0), ***anded*** with clock pulse P50 in gate SDT, drives to ground the set output of special flip-flop RMDT which is part of the receiver address register. The actual setting takes place at T18 to T29 (P50, clock) when an output from gate SDT occurs. The reset of RMDT is a pulse derived from clock output RC via gate RRG. Note that in the sequence diagram the DT1 lead is at ground from T18 of the first time slot to T12 of the next. However, this does not mean that the dial tone will be enabled in the digit receiver associated with the second time slot. It is the translator switch that supplies the dial tone enabling pulse and its duration is determined by circuit constants within a blocking oscillator type circuit. The translators and related circuitry are discussed later in the text.

4.18 The positive output of RMDT, DT0, is used to disable the horizontal translator switches for transmission and reset data store functions. Lead DT1 enables those switches associated with the horizontal portion of the dial tone function. After translation, a single negative going horizontal switch output (DTH0 to DTH3) and a positive going vertical switch output (RV0 to RV7) are combined to activate the time division switch in the digit receiver in order to enable dial tone.

4.19 The treatment of the reset data store bit (lead CO6 from program control) is similar to that described for dial tone.

5. TRUNK AND SWITCH UNIT NUMBER STORAGE

A. Processing a Trunk Number Command

5.01 The leads carrying the trunk and switch unit numbers, described in subsection 4, are unique in that they are destined for storage in the memory array. In Fig. 8 a ground on lead CO8 is traced through the affected circuitry to its destinations, the memory array and the trunk memory register. This is one of eight similar input paths to the memory.

5.02 As in the case for the receiver number, the trunk number is processed through a set of input gates (Fig. 3). A ground on the particular lead being discussed, CO8, generates a positive pulse from input gate T0 to set flip-flop T0 (part of the trunk register). The ground output enables one of the 2 inputs to ***and*** gate SOV. The ground remains on gate SOV until some time during the next 80-μsec receiver address binary counter cycle when a comparator

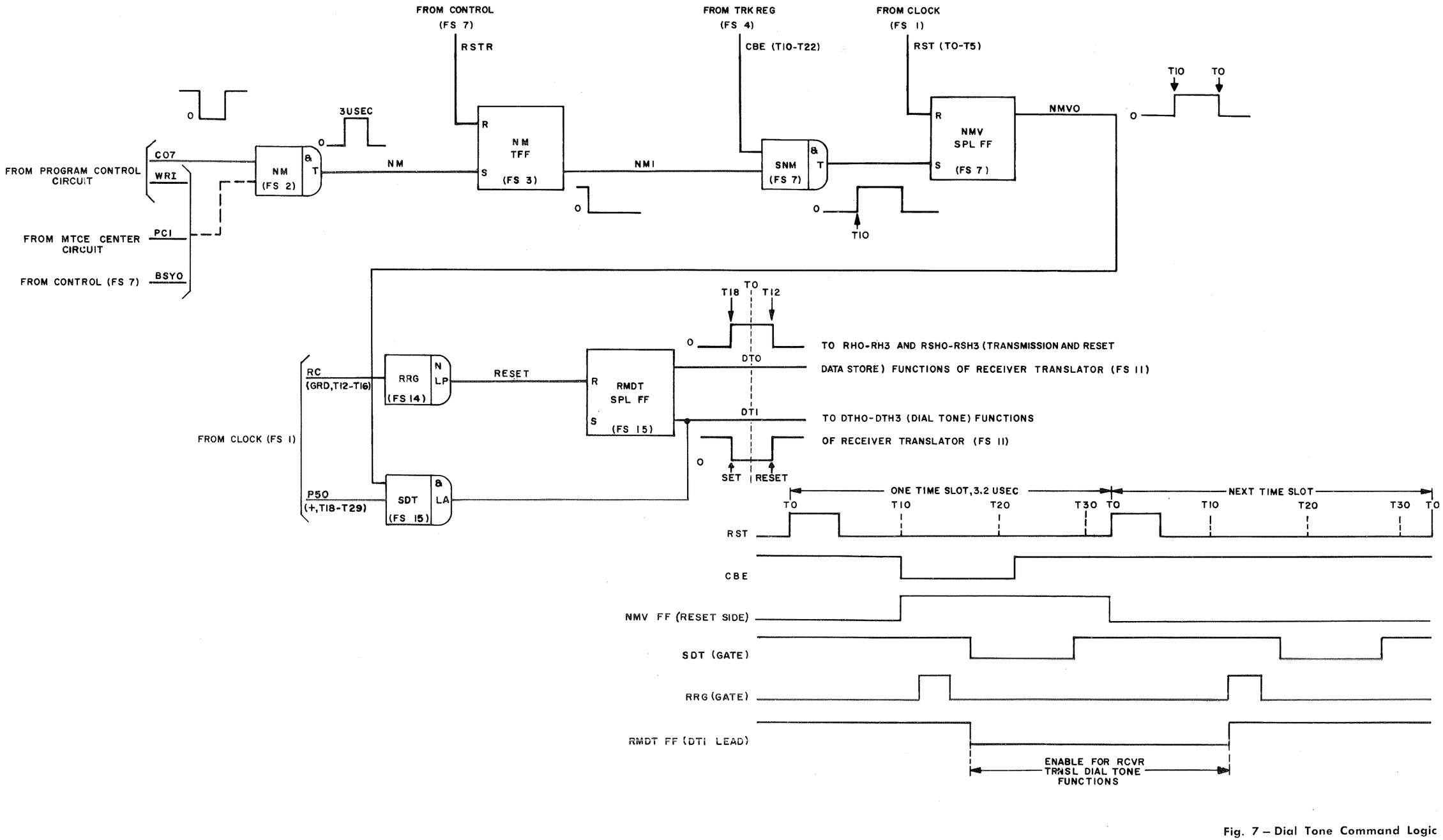
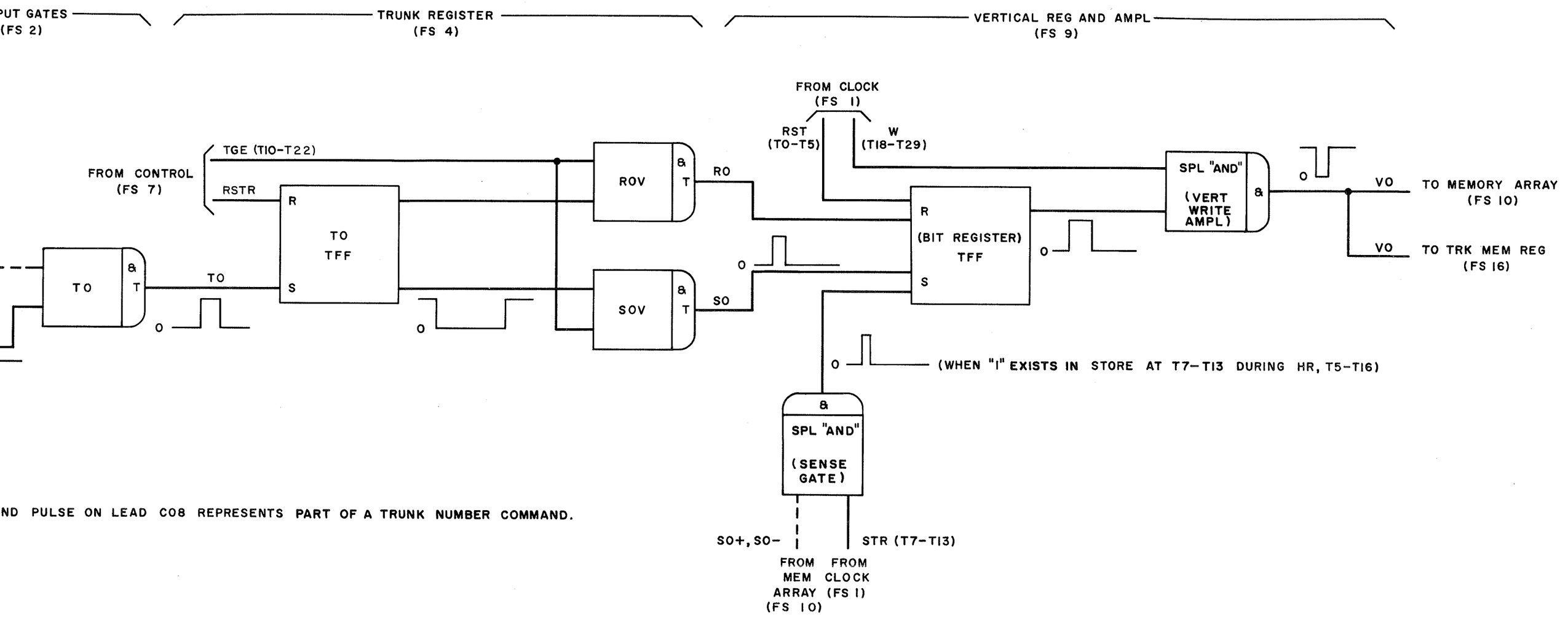
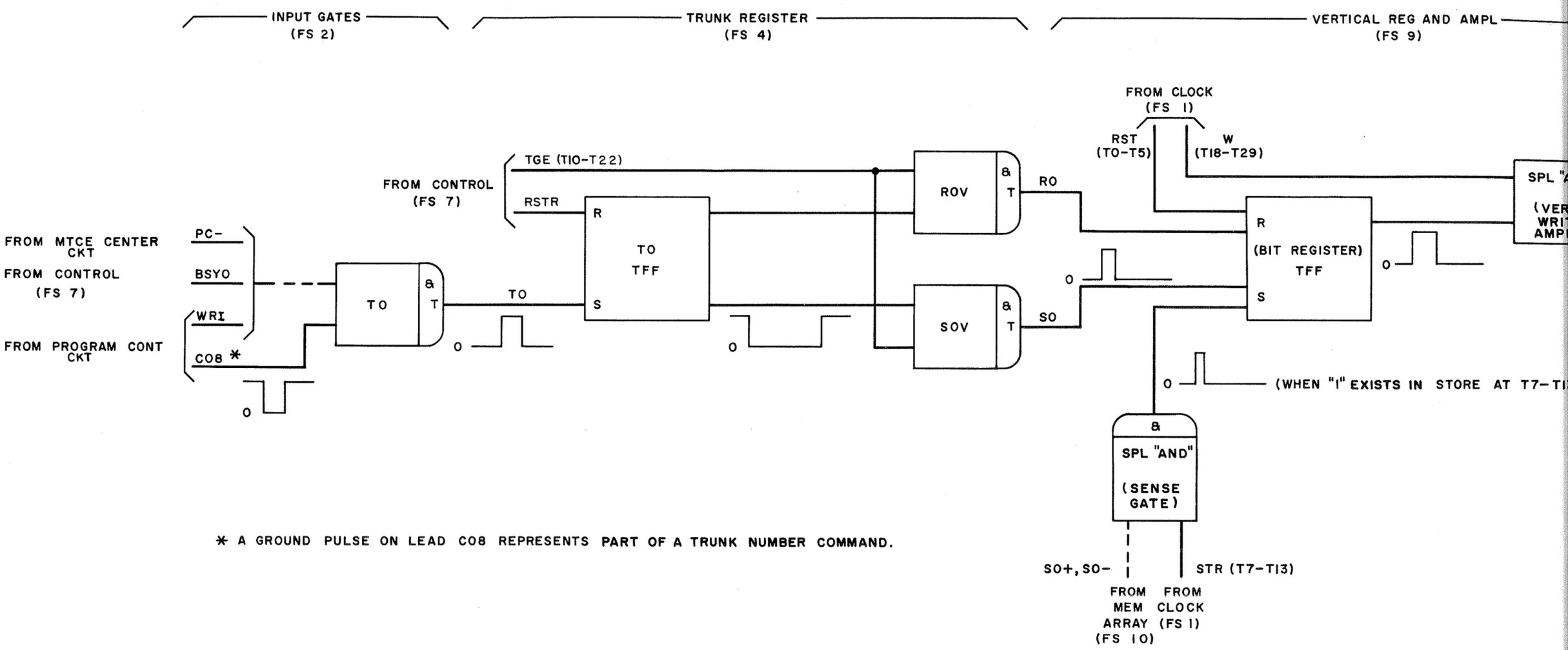


Fig. 7 – Dial Tone Command Logic



ND PULSE ON LEAD C08 REPRESENTS PART OF A TRUNK NUMBER COMMAND.

Fig. 8 – Processing a Trunk Number Command



* A GROUND PULSE ON LEAD CO8 REPRESENTS PART OF A TRUNK NUMBER COMMAND.

check will occur and lead TGE drops to ground. This satisfies the ***and*** condition for gate SOV. The resulting positive output will set the bit register which is part of the vertical register and amplifier circuit. The positive output, ***anded*** with the write pulse on clock lead W (T18 to T29) in a special ***and*** gate, drives both the vertical write winding of the memory array and the trunk memory register. The bit will be stored in the horizontal row (time slot) that is being addressed by the receiver address binary counter at this time.

5.03 The reset for the bit register occurs at the beginning of the next time slot by the RST clock lead at T0 to T5. The bit stored in the memory array is read 80 μsec later when the time slot is again addressed by the horizontal read pulse during T5 to T16. Reading destroys the stored information in this time slot. However, the sense winding (SO+, SO−) has detected that a stored bit was read and has produced a voltage pulse to one input of a special ***and*** gate called the sense gate. A strobe pulse (STR), during T7 to T13, serves to sample the sense winding output which results in a positive output from the sense gate. This output pulse is used to again set the bit register flip-flop. During the following write pulse (W, T18 to T29) the bit is rewritten into the store and the trunk memory register is again enabled. Thus, it can be seen that the bit is retained in the memory array by a process of reading out during T5 to T16 and immediately rewriting during T18 to T29 of the same time slot period.

B. Clearing the Time Slot

5.04 It would appear that once a bit was stored in the memory, the cycling of the read and write pulses would retain the bit permanently. This is partially true because the bit will be retained until the appearance of a reset data store message from program control. Normally, this message will not appear until dialing has been completed and processed. This message will contain the number of the time slot which identifies the digit receiver, trunk number zero, switch unit zero, and a reset data store bit.

5.05 The reset data store bit merely causes a single receiver translator output (lead RSH0 to RSH3) which is used by the digit receiver to clear the digit-data store area assigned to this receiver. However, the receiver number has a significant function in clearing the DRC store module because it will generate another comparator check bit. Again referring to Fig. 8, it is seen that flip-flop T0 is in a reset condition and remains reset because of the absence of bits in the trunk and switch unit numbers. Then, when the comparator derived ground pulse arrives on lead TGE, gate ROV will rise to a positive potential for a duration of the TGE pulse, approximately T10 to T22. This pulse, appearing on lead R0, is of sufficient duration to overlap the sense gate output (T7 to T13) and hold the bit register in a reset state for the remainder of the 3.2-μsec time slot interval. Then, when the next clock write pulse occurs (lead W, T18 to T29) it will find the vertical write path inhibited. Rewrite has been prevented and the bit removed from the memory array.

C. Store Operation

5.06 The preceding subsection has treated the trunk and switch unit number portion of the program control command that uses the memory array for temporary storage. The memory array and its access circuitry is detailed in Fig. 9. The following paragraph describes the operating techniques used in the storage process.

5.07 The store module, as used in the DRC circuit, consists of a 3-hole core matrix comprised of 8 vertical columns and 25 horizontal rows. Each of the 25 horizontal rows, called time slots, are addressed sequentially by pulses derived from the receiver address binary counter and the clock circuit. A time slot is assigned to each digit receiver. Odd numbered receivers are assigned time slots in DRC No. 1, and even numbered receivers in DRC No. 2. Each time slot encompasses a time interval of 3.2 μsec in which the 8 cores in a specific horizontal row are pulsed (addressed) in parallel with first read pulses and then write pulses. The occurrence of a read pulse (HR-) or write pulse (HW-) is always accompanied by a common read/write pulse (RW-) to complete the current path for the horizontal addressing function. There must be a coincidence of a vertical write (V-) pulse and horizontal write (HW-) pulse to set the magnetic core. The cores are destructively read by a single horizontal (HR-) pulse and if the stored bit is to be retained it must be sensed and rewritten upon application of the clock-derived write pulse (W)

occurring within this same time slot interval. The circuitry and method for accomplishing this has been discussed in the previous subsection.

D. Timing Logic

5.08 When sufficient time has elapsed for the complete processing of the program control command, the state of all trunk and receiver register stages must be reset to a "0" condition. Until this is done, the DRC remains inhibited to further commands by a positive inhibiting voltage to the input gates on lead BSY0. See Fig. 3 for the broad perspective.

5.09 Fig. 10 details the circuitry involved in the timing operation. There are four ways in which the timing circuit may act to produce the register reset pulse on lead RSTR. Each of these methods depends on a different variation in the receiver number portion of the program control command. Regardless of which timing path is utilized, the end result is a positive pulse on lead RSTR to clear the receiver and trunk registers and make them available for subsequent commands. Each of the four timing paths will be described separately.

Normal Operation

5.10 Any legitimate program control command will contain either a reset data store bit or a dial tone bit and appear at the output of the receiver register as a positive potential on lead RS0 or NM0, respectively. Again referring to Fig. 10, it is seen that either lead RS0 or NM0 will cause a ground output from OR gate STM. The ground-going transition is differentiated and inverted in differentiator TS to produce a positive setting (starting) function for the 120-μsec timer TM0. The TM0 timer output rises to plus TRL potential which inhibits ***and*** gate BS1. The other input to gate BS1 (from the BSY flip-flop) went to ground following the registration of the command and the return of the program control write in (WRI, 3 μsec) pulse to ground. (It remains in this state until the registers are cleared.)

5.11 The greater part of the timing circuitry is used to produce a reset for the 120-μsec timer TM0. If no reset circuitry existed, the TM0 timer would time-out after 120 μsec and its output would return to ground. This would enable gate BS1 and result in a positive pulse on lead RSTR. This pulse would last as long as it took the receiver and trunk registers to become reset, at which time the lower BS1 input would go positive and disable BS1. This would hold the DRC busy for a greater time than is necessary to process a command. Therefore, a reset for TM0 is initiated to shorten the timed busy interval.

5.12 It must be realized that the command must remain registered until there has been a comparator check which may occur as late as 80 μsec after the registration. The presence of this check is used to start an additional 10-μsec count which resets timer TM0 at the end of the 10-μsec period.

5.13 When a comparator match does occur, it appears as a ground from the ST flip-flop to ***and*** gate RS (Fig. 10). Then, at the end of the positive SV clock pulse, T10 to T22, gate RS rises positive which starts the 10-μsec TRS monopulser. At the end of the 10-μsec pulse the trailing edge (negative-going) of the waveform is differentiated and inverted in differentiator TR. The resulting positive transition resets the TM0 timer immediately and returns its positive output to ground. Both inputs to ***and*** gate BS1 are now at ground which produces a positive RSTR pulse which lasts as long as it takes the receiver and trunk register stages to become reset by RSTR. When all the registers have been reset, the BSY flip-flop returns to an idle state which terminates the RSTR pulse by inhibiting gate BS1.

5.14 The second setting (starting) path to the TRS 10-μsec monopulser via gates FTO and FTA, has been ignored for this reason. The command that was discussed above was a normal command, ie, it was intended for this particular DRC. By optional wiring X or Y, the least significant bit in the receiver register caused a positive battery to appear on lead OR or ER. This inhibited ***and*** gate FTO and prohibited it from setting the TRS 10-μsec monopulser.

Other Digit Receiver Connector (DRC)

5.15 Let us consider what would occur if this was the other DRC, ie, the receiver number was not intended for this DRC. Immediately upon registration of the receiver number, lead RS0 or NM0 would start the 120-μsec timer TM0 as previously described. Also, this DRC would temporarily be marked busy. However, because

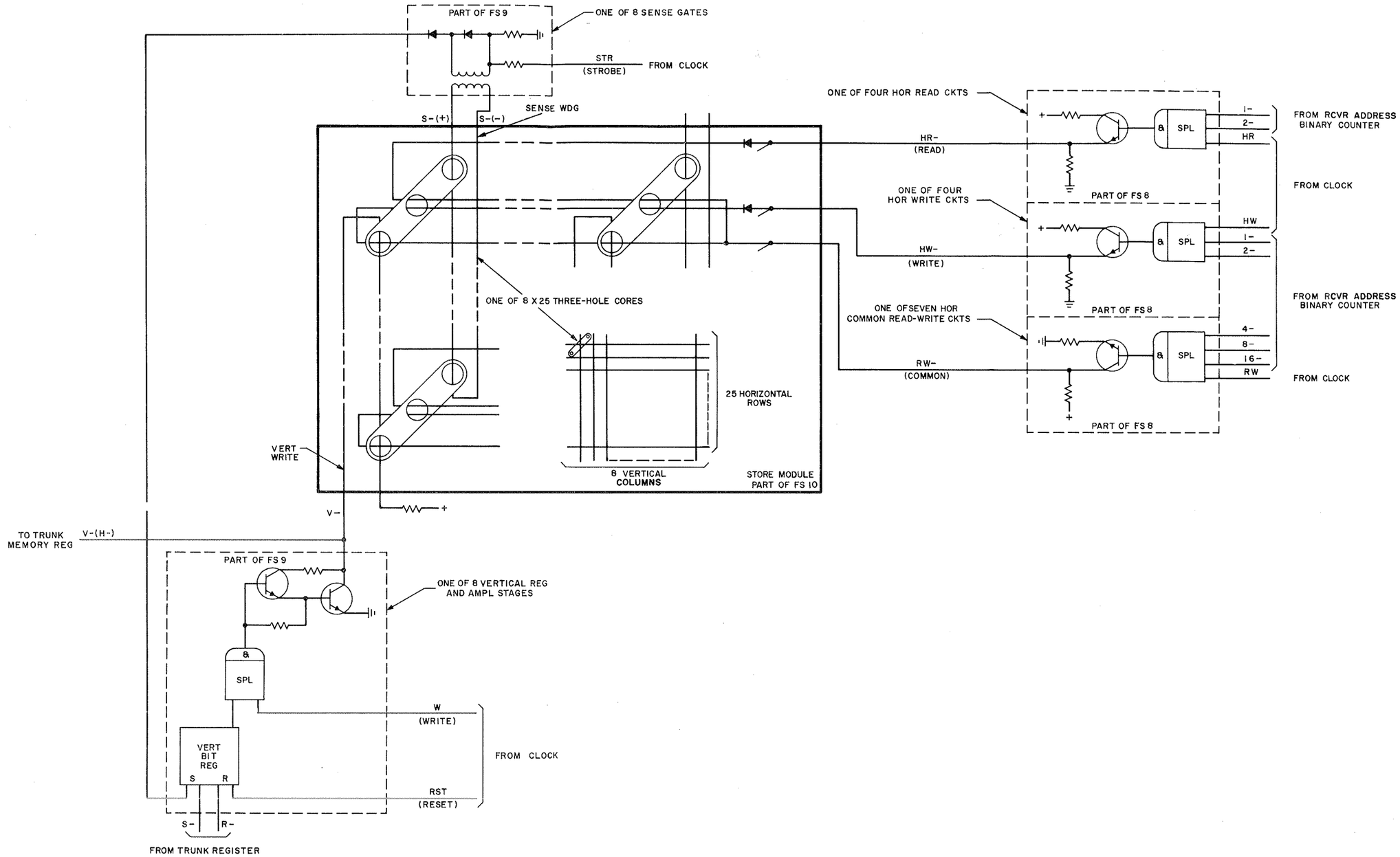


Fig. 9 – Memory Module and Access Circuitry

this is the other DRC a comparator match can never occur to start the 10-μsec TRS monopulser and reset the timer TM0. The timer TM0 would eventually time out after 120 μsec, however, it is important that this DRC be made available for a subsequent command as soon as possible. Therefore, another setting (starting) path is required for the 10-μsec TRS monopulser. This is accomplished by ***anding*** the OR or ER lead, which is now at ground because this is the other DRC, with the inverted TM0 timer output. This produces a positive output from ***and*** gate FTO to start the 10-μsec monopulser which will reset the 120-μsec timer TM0 after 10 μsec and cause an immediate reset of the receiver and trunk registers by a positive pulse on lead RSTR as previously described. In this way, the DRC is made available for further commands in approximately 10 μsec.

Illegal Receiver Number

5.16 There is the possibility that an illegal receiver number could be registered, ie, a number other than 1 through 25. Therefore, the comparator would never produce a check bit to cause a normal reset of timer TM0. Actually, this condition is handled in two ways. If the least significant bit of the illegal receiver number agrees with this DRC option, ie, the number is intended for this DRC, no setting path for the 10-μsec TRS monopulser exists and, therefore, timer TM0 cannot become reset. However, after 120 μsec the timer TM0 will time out to clear the registers and idle the DRC.

5.17 Secondly, if this is the other DRC, the X or Y optional wiring (leads ER or OR) will cause an enable for gate FT0 which will result in the resetting of TM0 after approximately 10 μsec and the clearing of the registers as described earlier.

No Reset Data Store (RS0) or New Message (NM0) Bit

5.18 The fourth receiver number variation can also be considered an illegal number. This is the situation where neither RS0 or NM0 is present to start timer TM0 but a receiver number has been registered. This will result in a ground on the BS1 gate lead from the BSY flip-flop and a ground on the input from timer TM0. The result is an immediate positive voltage on lead RSTR to reset the registers.

5.19 It should be pointed out that in every situation except the normal case, no comparator check occurred. As a result, the trunk and switch unit number portion of the command proceeded no further in the DRC than the trunk register, because a ground on lead TGE, normally derived from the check bit, never occurred to enable the trunk register output gates. (See Fig. 3.)

5.20 From the foregoing, it can be realized that there is no combination of program control command bits that can cause the DRC to be locked up, and that the maximum time that an illegal receiver number will cause the DRC to be marked busy is 120 μsec. Also, this improper command will never cause a trunk translator output to make an unwanted digit trunk and receiver time division connection.

6. TRANSLATION AND TIME DIVISION SWITCH DRIVES

A. Receiver Translator (Fig. 3)

6.01 The receiver translator output pulses are used to enable the time division switches in the digit receivers. The pulses to the transmission switch in the digit receiver occur coincident with those supplied to the digit trunk circuit in order to connect both the trunk and receiver circuits to a common bus on a time division basis.

6.02 To close a time division switch, both horizontal and vertical pulses are required. The receiver translator vertical section is enabled by outputs from the three least significant stages of the receiver address binary counter. The translator outputs, RV0 to RV7, are the result of a 1-out-of-8 translation. A single vertical translator output pulse is common to all three time division switches in a given receiver and are applied continually regardless of other action within the DRC.

6.03 The horizontal translator is divided into three sections to supply horizontal pulses to each of three digit receiver time division switches. Output leads RII-, DTH-, and RSH- supply the negative-going pulses to activate the switches for transmission, dial tone, and reset data store functions, respectively. The 12 translator outputs (of a possible 16) are derived from the 2 most significant receiver address binary

counter stages, dial tone bit, and reset data store bit. When a dial tone or reset data store bit enables the translator, a single pulse results to activate the associated time division switch in the digit receiver. This causes a single pulse to be missed for the transmission switch. At all other times the translator supplies pulses to enable the transmission switch and connect the receiver to the common bus.

B. Trunk Translator (Fig. 3)

6.04 The trunk translator is made up of a vertical and horizontal section which supply enabling pulses to the digit trunk circuit time division switches. They occur coincident with the digit receiver transmission enabling pulses in order to complete a time division connection over a common bus between the digit trunk and receiver circuits.

6.05 The trunk translation gates and switches are similar to those used in the receiver translator; however, a 1-out-of-16 translation is used for each of the horizontal and vertical sections.

6.06 The inputs to the trunk translator are derived from the same leads that write into the memory array, that is, the outputs from the vertical write amplifiers. These outputs are made up of trunk and switch unit number bits that are part of the program control command to the DRC. The three trunk number bits and the least significant switch unit number bit are used in the vertical translation. The horizontal translator is gated by the four most significant switch unit number bits.

C. Temporary Registration (Fig. 3)

6.07 For both the receiver and trunk translators, a set of temporary registers feed the input bits to the gates that do the actual translation. These registers serve to temporarily store the bit information while the binary-to-decimal translation takes place. The register stages are unique in that an operating threshold is provided to make them immune to voltage transients. A reset pulse derived from the clock during T12 to T16 every 3.2 μsec terminates the register output signal resulting in an adequate pulse length to enable the translator. Furthermore, a high fanout capability provides adequate input levels to eight translator gates.

D. Translator Switch Enable (Fig. 3)

6.08 Leads THP1, THP2, TVP1, and TVP2, derived from clock pulse PC, serve to enable the trunk horizontal and vertical translator switches only during T24 through T12. This gives the trunk memory register sufficient time to stabilize, and thus make up the differences in switching speeds of the various parallel paths to the translators. The object of this treatment is to prevent spurious translator outputs during the period that the registers are in transition.

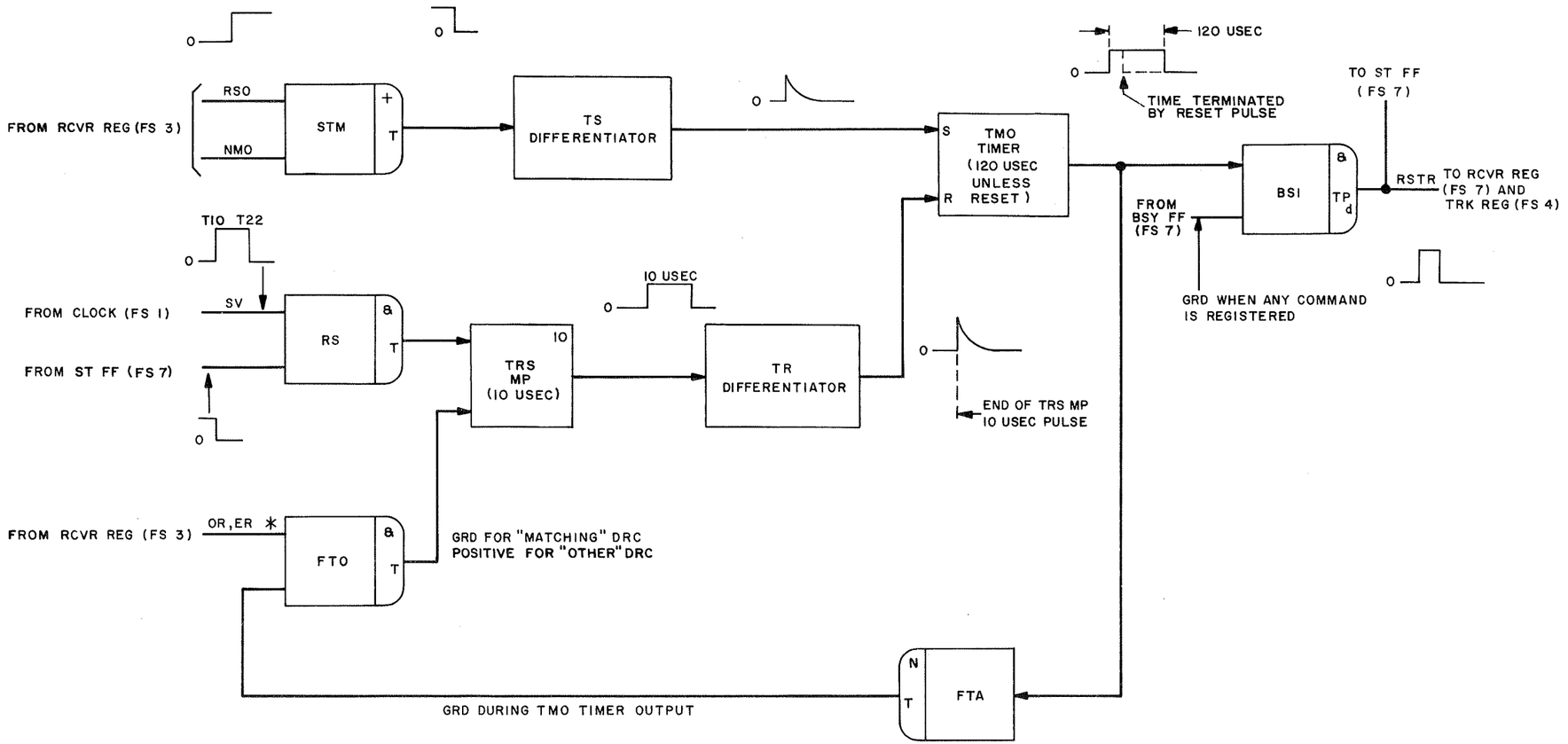
6.09 Leads RHP1, RHP2, RVP1, and RVP2 provide a similar service to the receiver translator during the same clock time.

E. Resonant Circuit

6.10 Resonant circuits are used in conjunction with the vertical switches of both the trunk and receiver translators. In effect, the resonant circuit is in series with both the vertical and horizontal translator switches because the current through the time division switch load is common to both of them. The basic configuration of the resonant circuit consists of an inductor-capacitor network which determines the amplitude and duration of the half sine wave current through the selected time division switch. The ideal waveform is a half sine wave with a current peak of 450 ma and a duration of 2 μsec.

F. Capacitor Discharge Switch

6.11 The proper operation of the resonant circuit requires the use of an associated capacitor discharge switch. The purpose of this circuit is to resonantly discharge the voltage on the timing capacitor in the resonant circiut after the 2-μsec switching pulse. This discharge action must be completed within the next 1.2 μsec in order to make the resonant circuit available for subsequent pulses every 3.2 μsec. Note that one resonant circuit and capacitor discharge switch is common to all switches in each trunk and receiver translator. This arrangement is possible because only one set of switches is actuated in each translator during one 3.2-μsec interval.



* POSITIVE FOR "MATCHING" DRC, GRD FOR "OTHER" DRC

Fig. 10 – Timing Logic for Reset of Receiver and Trunk Registers

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