DATA, DIGIT, AND SENDER CONTROLS

DESCRIPTION OF SYSTEM OPERATION

NO. 101 ELECTRONIC SWITCHING SYSTEM

CONTENTS PAGE

1. GENERAL

1.01 This section is reissued to include changes required by the 2A and 3A switch units. Because this reissue covers a general revision, arrows ordinarily used to indicate changes have been omitted.

1.02 The heavy work load imposed on the call processor allows it to spend only a small period of time (measured in μsec) on each communication involving the acquisition or distribution of supervisory, digital, or control information.

1.03 On the other hand, the intervals of time required to generate and transmit such information, whether incoming to the control unit or outgoing from it, are relatively long.

1.04 In order to accommodate these disparities in time factors, appropriate ***input-output*** equipment is provided whose central feature is a temporary (ferrite sheet) type memory known as the data and digit store. Signals from the switch units in the form of data messages and dialed digits are placed in this store a bit or pulse at a time as they arrive. When such information is completely registered, provision is made for transferring it to the call processor on a parallel transmission basis requiring only a short interruption of the call processor cycle. (Exception: The digits of an outside call remain in the store until outpulsed to the central office.) Outgoing information is similarly transferred from the call processor to the data and digit store at high speed and then pulsed out at the rate required by the switch units (data messages) or the central office (dial digits), as the case may be.

1.05 The three circuits that control the various phases of the data and digit store operation are the data control, digit control, and sender control circuits. In this description these are treated largely as a unit.

2. MAJOR FUNCTIONS

2.01 The major functions of the data, digit, and sender control area are to handle incoming and outgoing data messages, to receive digits, and to outpulse digits. (See Fig. 1.) The data and digit store is used in conjunction with all four functions. The scanner circuit is used to provide sample access between the various data trunks, digit receiver circuits, and the data and digit store. The four functions can be performed for as many as 32 switch units on a time-sharing basis.

2.02 The switch unit sends an incoming message to the call processor when a line goes off-hook. This incoming message is received serially by the incoming data trunk circuit and is shifted into the store through the memory register. When the complete message has been accumulated by the store, it is sent to the call processor, in parallel form, through the memory register.

2.03 The call processor then sends an outgoing message to the switch unit to connect the digit trunk to the line which had gone off-hook. The message is loaded into the data and digit store in parallel form. It is shifted out of the store serially. In this way, the store and the data control circuit are used for serial-to-parallel and parallel-to-serial conversion.

2.04 When the calling line is connected to a digit trunk at the switch unit, the digit trunk is connected to a digit receiver at the control unit. The digit receiver accepts TOUCH-TONE (T-T) signals or dial pulse signals and translates them to a 2-out-of-8 parallel code. The digit control circuit receives this code when the digit receiver is enabled by the scanner. It uses the store to count the dial pulses, time the interdigital intervals, and store the digits received. When the digit message is complete, it is forwarded to the call processor.

2.05 The sender control circuit is used only on those calls which require outpulsing. The sender control uses the data and digit store to count outpulses and to time interpulse intervals and interdigital intervals. It uses the trunk number, which is stored with the digit information, to activate the trunk connector circuit. The trunk connector circuit has a function similar to the scanner. It directs the outpulsed message to the proper trunk.

2.06 The data control, digit control, and sender control circuits are described together. All three circuits make use of the data and digit store and they are interrelated in many of their functions. Much of the data control circuitry (the address register, the memory register, and the scanner) is used by the digit control and the sender control. Fig. 2, for general reference, shows the entire data, digit, and sender control area.

3. ORGANIZATION OF DATA AND DIGIT STORE

A. General

3.01 The data and digit store contains 512 words. Three-quarters of the store is used for digit receivers. The bottom quarter of the store consists of data information. (See Fig. 3.)

B. Digit Receiver Area

3.02 Forty-two digit receivers are numbered 2 through 43. (See Fig. 3.) Each digit receiver is allotted eight words. A digit receiver area is described by bits 4 through 9 of the address register. Bits 1 through 3 identify one of the eight words in a digit receiver area.

3.03 The first four words of the eight words assigned to each digit receiver are used for control functions. The last four words are used to store digits. A total of 16 digits can be stored, 4 digits per word. The fifth word contains digits 1 through 4, the sixth word contains digits 5 through 8, the seventh word contains digits 9 through 12, and the eighth word contains digits 13 through 16. Words one, two, and four are used primarily by the digit control. They are concerned with receiving incoming digits from the digit receiver. Words three and four are used primarily by the sender control. The fourth word contains the trunk and switch unit numbers which are used in outpulsing.

C. Data Area

3.04 There are 32 four word switch unit areas. The address for a switch unit word consists of: bits 8 and 9 (which are always 1 and 1), indicating the bottom quarter of the store; bits 3 through 7, representing the switch unit number; and bits 1 and 2, representing one of the four words.

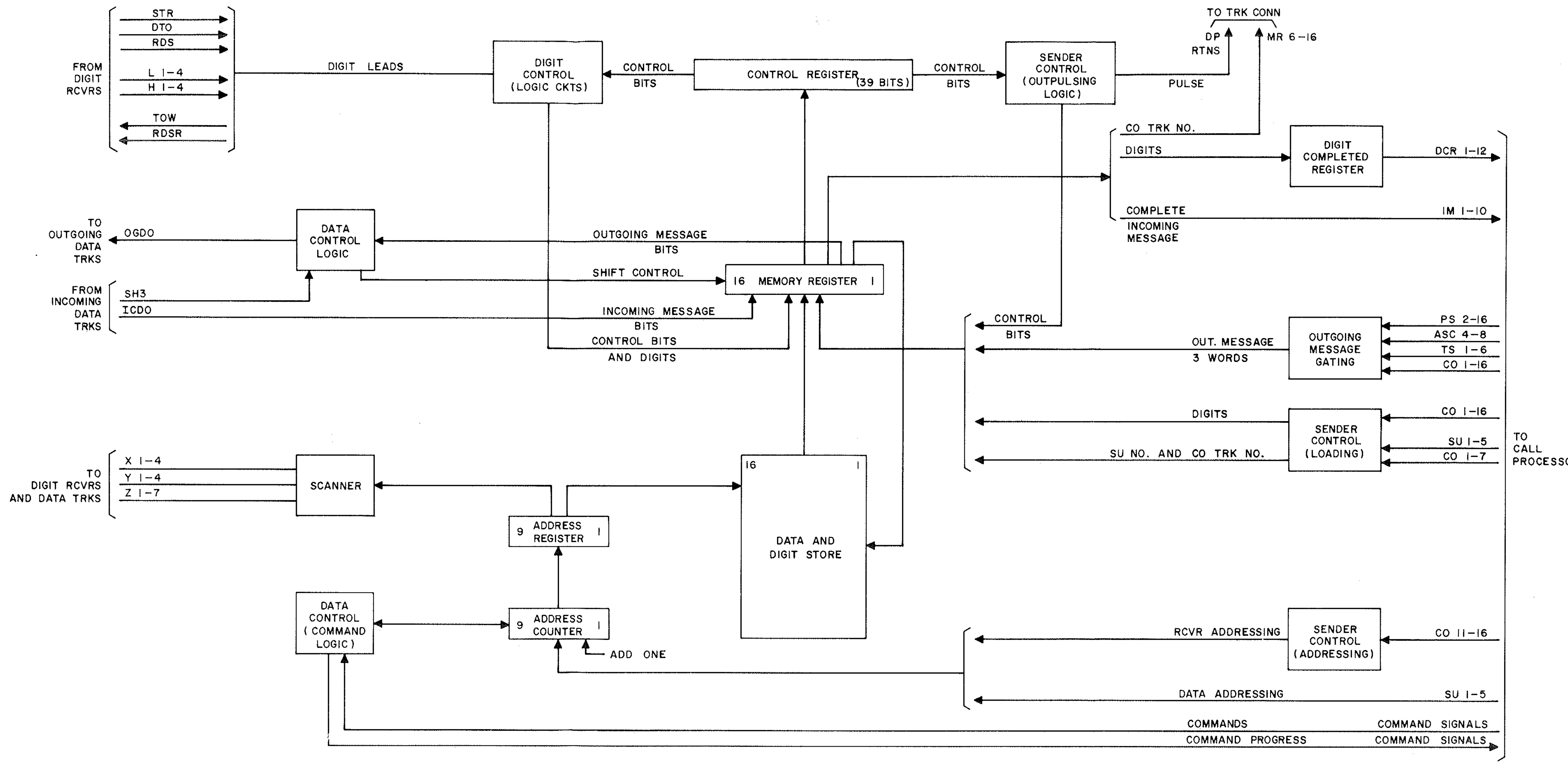


Fig. 1 — Block Diagram of Data, Digit, and Sender Control Areas

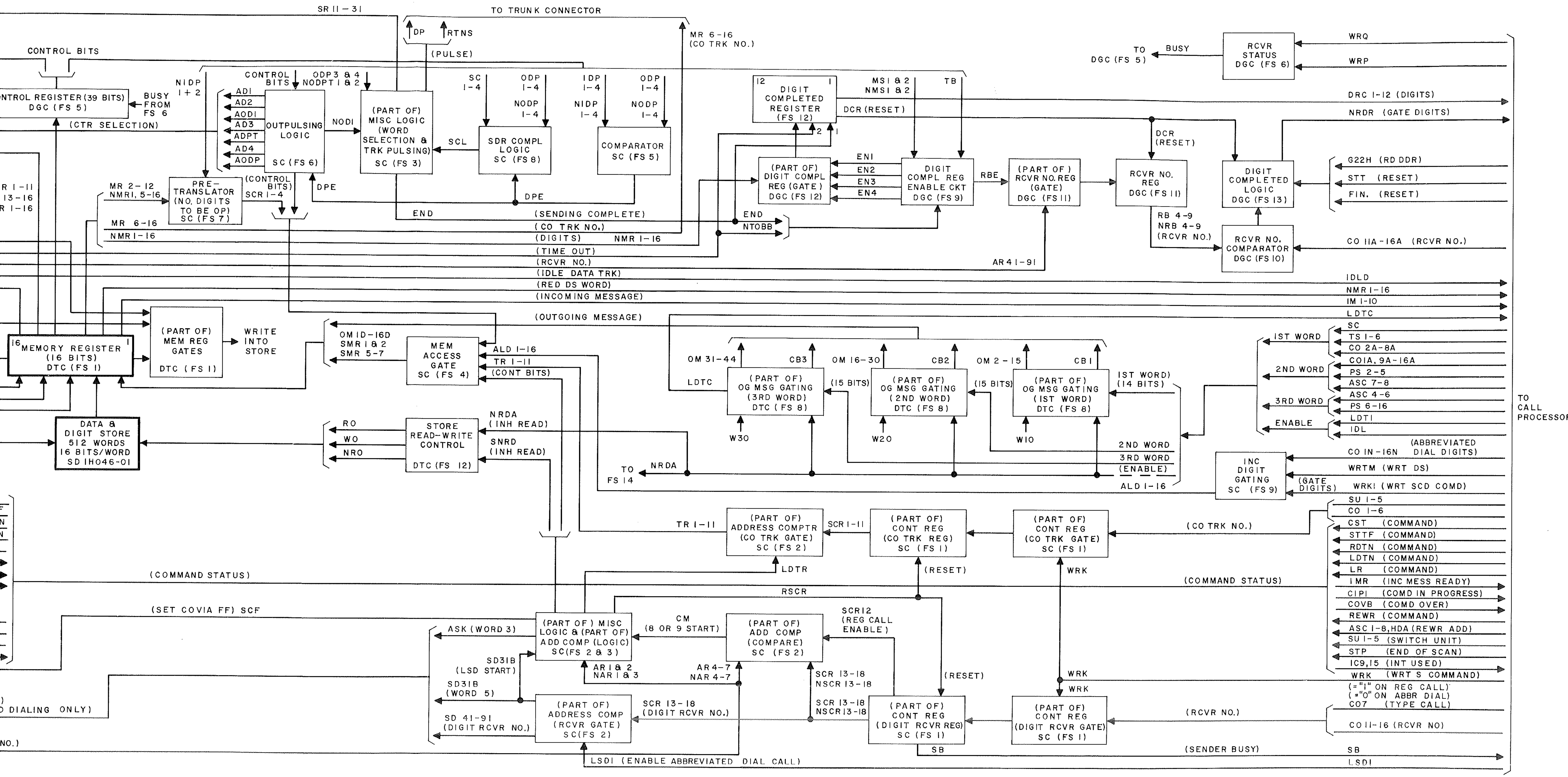
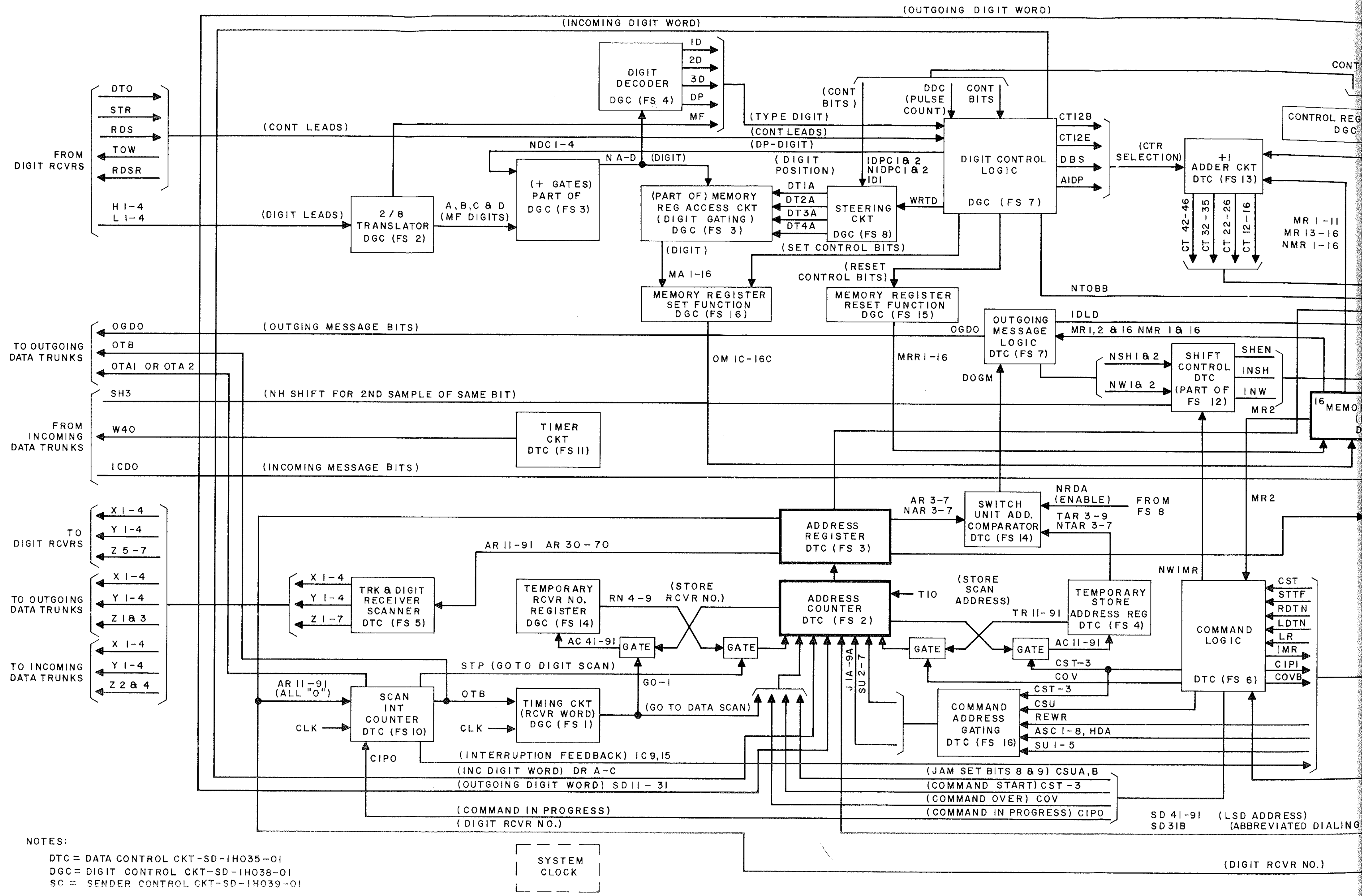


Fig. 2 — Detailed Block Diagram of Data, Digit, and Sender Control Areas



NOTES:

DTC = DATA CONTROL CKT-SD-1H035-01
DGC = DIGIT CONTROL CKT-SD-1H038-01
SC = SENDER CONTROL CKT-SD-1H039-01

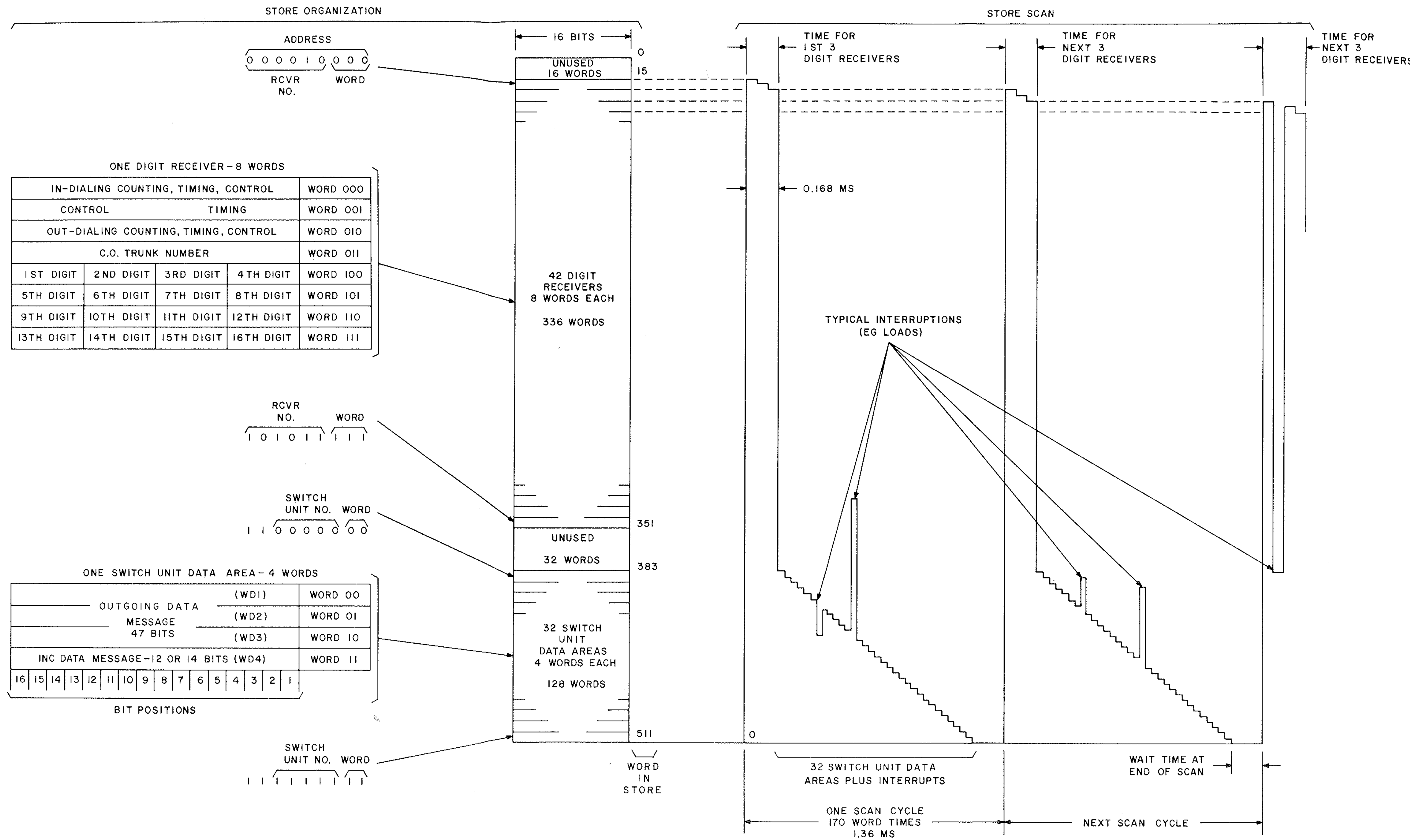


Fig. 3 — Data and Digit Store — Organization and Scan

3.05 The first three words of the switch unit area are concerned with the outgoing data message. The contents of these words are fed into the outgoing data trunks. The fourth word contains the incoming data message. The incoming data trunk loads its message into this word.

D. Store Scan

3.06 The words in the data and digit store are read out in a definite pattern. The beginning of the scan cycle is used to process three digit receivers. Each receiver uses seven word times (seven read/write cycles). However, when 15 of the 21 word times have been used, the call processor is prohibited from interrupting the scan. It must wait until the scan is complete and deliver its interruption command during the new scan. Each read/write cycle contains eight 1-μsec phases known as T00 through T70. Therefore, the three digit receivers require 21 word times (168 μsec) to be processed. This is referred to as the digit scan. The store is then directed to the data area. The words in the data area are read sequentially. The three words concerning the outgoing message are scanned and the fourth word concerning the incoming data message for each switch unit data area is then scanned. Each succeeding switch unit data area is processed sequentially until the data scan is complete. One hundred and twenty-eight word times (1024 μsec) are required to completely scan the switch unit areas.

3.07 Twenty-one word times (168 μsec) are reserved for the call processor to interrupt the normal scan cycle. However, when 15 of the 21 word times have been used, the call processor is prohibited from interrupting the scan. It must wait until the scan is complete and deliver its interruption command during the new scan. Fig. 3 shows some representative scan interruptions. The call processor can address any word in the data and digit store during a command interruption which can occur during a data or digit time. If the call processor does not use all 21 word times by the end of data scan, the system waits until the allotted scan time is completed, then a new scan cycle is started, the next three digit receivers are scanned, etc.

3.08 Fifteen scan cycles of the store are used to scan all the digit receivers. Actually, time is used for three receivers which are not equipped. In this way, the scan of the store is used to handle data trunks and digit receivers at the appropriate rate.

E. Scan Control Circuits

3.09 The data control command logic is shown in Fig. 1 and in more detail in Fig. 2. The circuits which control the scan are shown in the lower left-hand corner of Fig. 2.

3.10 The end of the data scan is determined by the scan interruption counter which activates the STP lead. The first digit receiver number is then gated from the temporary receiver number register to the address counter and in turn to the address register and the first read/write cycle of this scan then begins.

3.11 Each digit receiver scan has seven word times. However, Fig. 3 shows that there are eight words associated with each digit receiver. Certain of the eight words are scanned every cycle while others are scanned as needed. Table A shows the scan sequence for one digit receiver scan. The seven word times used are shown under the column "Word Addressed."

TABLE A

SCAN SEQUENCE FOR ONE DIGIT RECEIVER

WORD TIME	WORD ADDRESSED
1	000
2	001
3	010
4	011
5	100 or 101 or 110 or 111 or 000
6	100 or 101 or 110 or 111 or 000
7	010

3.12 The digit control timing circuit supplies timing phase leads to the digit control during the digit scan. This timing is generated by combining the eight clocking phases T00 through T70 with the seven outputs of the word time counter (see FS1 of SD-1H038-01), giving a total of 56 timing pulses numbered T000, T010, ... , T540, and T550 (see Table B). The receiver areas are also counted. When three receivers have been scanned, the timing circuit activates the GO-1 lead. This lead gates the number of the next receiver (first receiver of next scan) from the address counter to the temporary receiver number register. The address counter is then cleared (reset) and the first data address (110000000) is jam set into the address counter. Jam set here means changing the address to one that is not the next in sequence. The address counter is incremented by one during each following read-write cycle to advance through the data scan.

3.13 Commands from the call processor may interrupt the normal digit and data scans at any time. All the interruption commands activate the command start (CST) lead. This lead activates the command logic, which in turn gates the normal scan address from the address counter to the temporary store address register. It also allows the scan interruption counter to be incremented once every read-write cycle throughout the duration of the command. At the completion of the command it gates the normal scan address back to the address counter.

4. ADDRESSING AND SCANNING

A. Address Counter

4.01 The address counter advances the address for a continuous scan cycle of the data and digit store. (See Fig. 4.) The address counter actually consists of two parallel carry binary counters. The first counter consists of bits 1 through 3. The second counter consists of bits 4 through 9. The two counter sections are tied together by means of the SAD gate.

4.02 The counting operation is as follows. Gate IADG is activated by lead T10. This pulse increments the first parallel carry binary counter. When bits 1 through 3 are all ones, the SAD gate is activated. The SAD gate increments the second counter. Inhibit address counter advance leads IAD, IAD2, and IAD3 are used to inhibit the pulsing gates. At T1 the address counter is incremented. At T7 the new address is gated from the address counter to the address register.

4.03 The address in the address counter is, therefore, effectively one word time ahead of the address register. The address used to access the data and digit store is derived from the address register. This is done because the address counter is in a transition state, but the address register is stable during the reading of the store. This holds true whether the counter is merely adding one to facilitate scanning the data area or if interruption commands are used to change the address to an entirely new location in the store. The address register and the address counter contain the same information from T70 through T00.

TABLE B

DIGIT CONTROL TIME PHASES

DIGIT CONTROL TIME PHASE	DIGIT CONTROL TIMING LEADS						
	WORD TIME 1	WORD TIME 2	WORD TIME 3	WORD TIME 4	WORD TIME 5	WORD TIME 6	WORD TIME 7
T00	T000	T080	T160	T240	T320	T400	T480
T10	T010	T090	T170	T250	T330	T410	T490
T20	T020	T100	T180	T260	T340	T420	T500
T30	T030	T110	T190	T270	T350	T430	T510
T40	T040	T120	T200	T280	T360	T440	T520
T50	T050	T130	T210	T290	T370	T450	T530
T60	T060	T140	T220	T300	T380	T460	T540
T70	T070	T150	T230	T310	T390	T470	T550

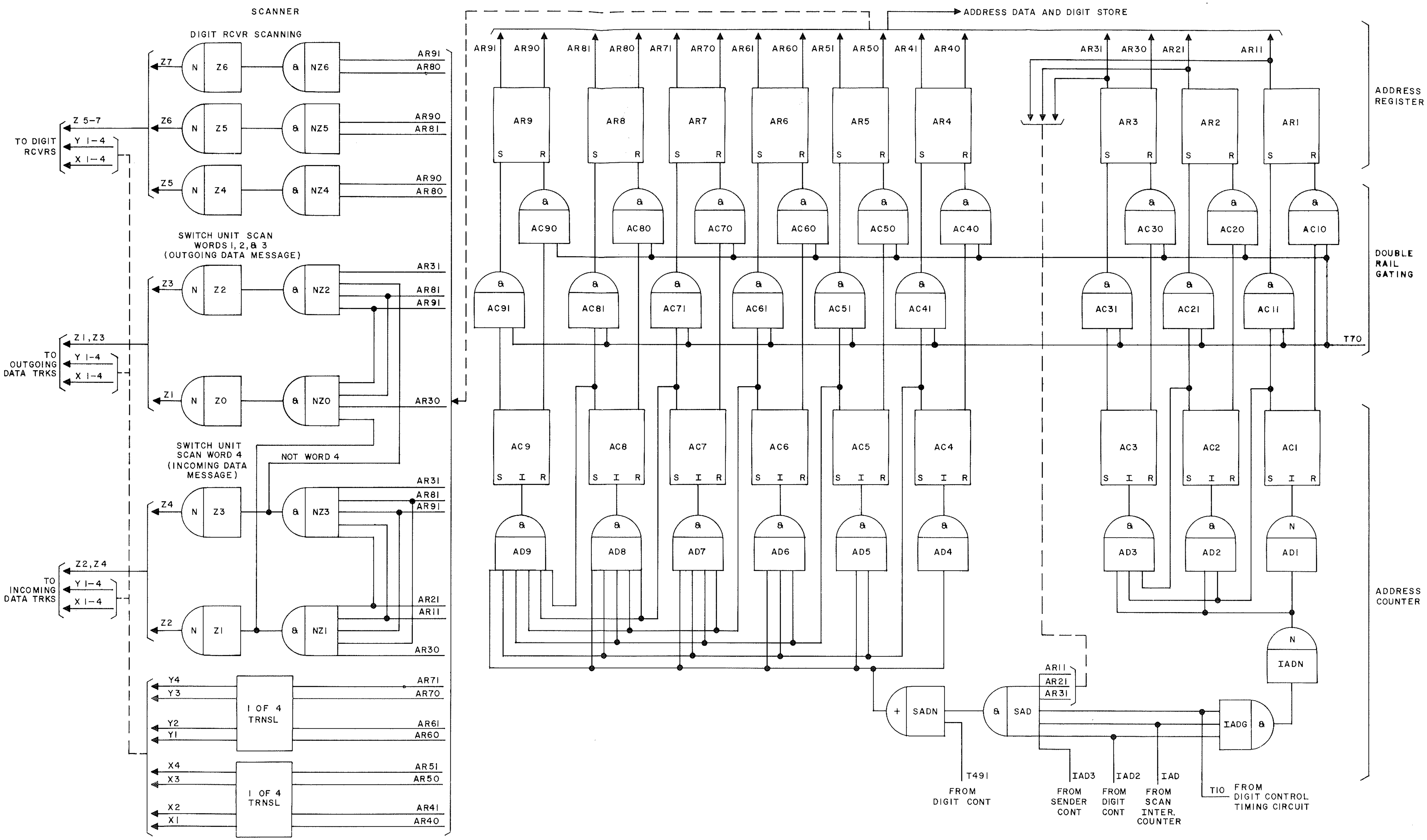


Fig. 4 — Data and Digit Store Addressing and Trunk and Receiver Scanning

B. Scanner

4.04 In addition to being used for addressing the data and digit store the output of the address register is also used by the scanner circuit. The function of the scanner circuit is to enable the incoming data trunks, outgoing data trunks, and digit receivers when the appropriate area in the store is being scanned.

4.05 In scanning the digit area of the data and digit store each digit receiver is scanned for seven of the eight words associated with it (refer to 3.11). The address of the digit receiver word is generated by flip-flops AR 1-3. It is necessary that the receiver be addressed throughout the entire seven word times of the scan. Since bits AR 1-3 determine which of the seven words of the scan is being addressed, AR 1-3 need not be used by the scanner in determining which digit receiver is being scanned.

4.06 The incoming and outgoing data trunks also make use of the scanner. Whenever AR8 and AR9 are both set to "ones," this indicates that the switch unit portion of the scan is in progress. As previously stated, each switch unit assignment (0 through 31) has a group of four words associated with it in the data and digit store. In order to acquire or deposit information from or to the appropriate store location, the scanner outputs are used by the incoming data trunks to deposit information in word 4, and by the outgoing data trunk to acquire information (from either words 1, 2, or 3) to be sent to the switch unit.

4.07 Summing up, the scanner can be used to enable both digit receivers and incoming or outgoing data trunks by the appropriate selection of the X, Y, and Z leads formed in the scanner circuit. Fig. 4 is a general schematic of the translation, and Table C gives a condensed formation of the X 1-4, Y 1-4, and Z 1-7 leads. For a complete application of these leads, see the Data Control Circuit (SD-1H035-01) Cross Connection.

TABLE C

SCANNER OUTPUT TO SELECT STORE ADDRESS

SCANNER OUTPUT	ADDRESS REGISTER BITS								
	9	8	7	6	5	4	3	2	1
X1	–	–	–	–	0	0	–	–	–
2	–	–	–	–	0	1	–	–	–
3	–	–	–	–	1	0	–	–	–
4	–	–	–	–	1	1	–	–	–
Y1	–	–	0	0	–	–	–	–	–
2	–	–	0	1	–	–	–	–	–
3	–	–	1	0	–	–	–	–	–
4	–	–	1	1	–	–	–	–	–
Z1	1	1	–	–	–	–	0	*	*
2	1	1	–	–	–	–	0	1	1
3	1	1	–	–	–	–	1	*	*
4	1	1	–	–	–	–	1	1	1
5	0	0	–	–	–	–	–	–	–
6	0	1	–	–	–	–	–	–	–
7	1	0	–	–	–	–	–	–	–

– = lead not used to obtain scanner output

1 = set state of AR-

0 = reset state of AR-

* = bits 2 and 1 can be 00, 01, or 10 but not 11

5. MEMORY REGISTER FUNCTIONS

A. General

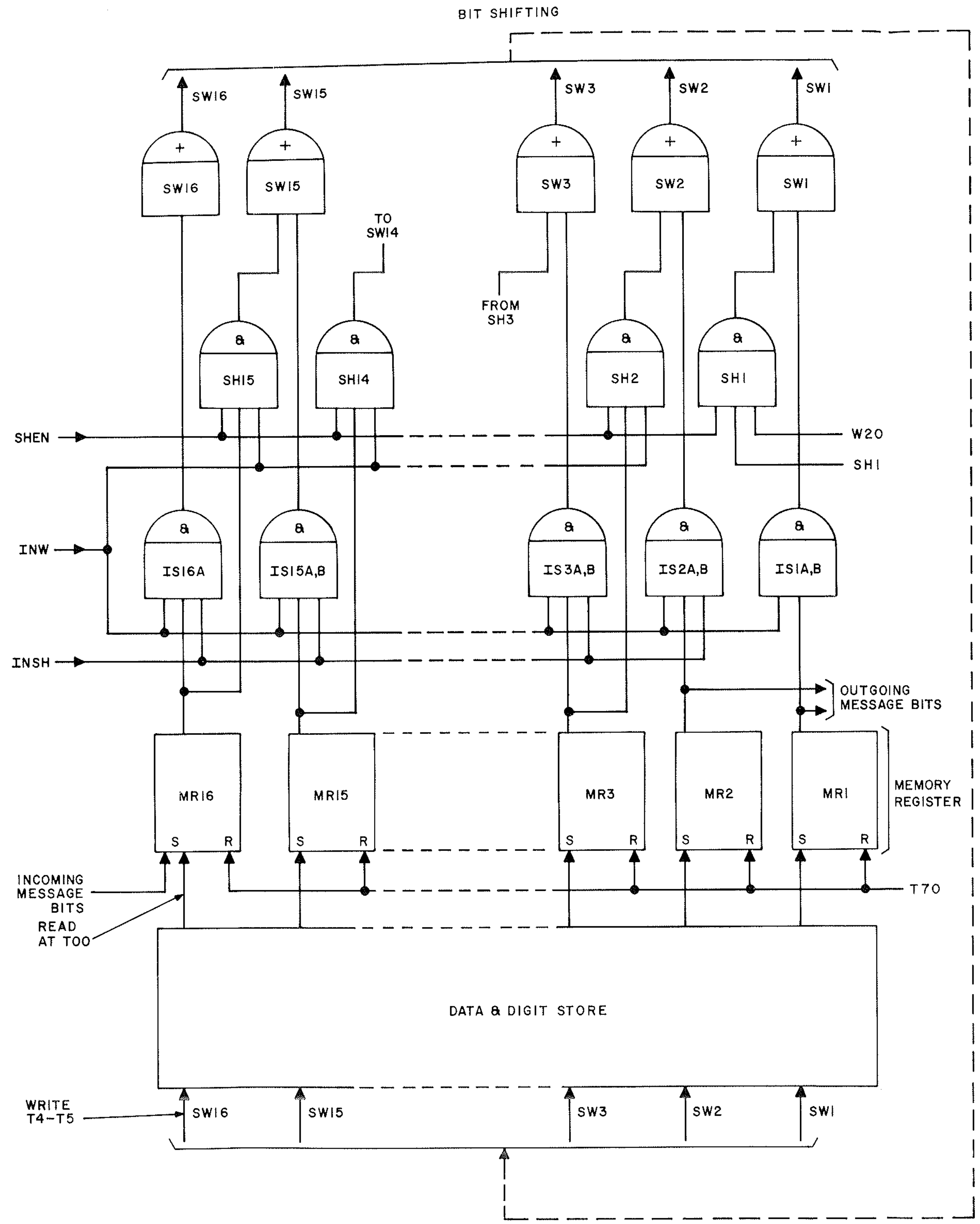
5.01 The functions of the memory register are to:

(1) Accept bits from peripheral circuits to be written in to the data and digit store for later processing.

(2) Accept bits which are read out of the store and to write them back into the store (see Fig. 5).

(3) Act as a shift register for processing incoming and outgoing data messages.

(4) Act as a counter when necessary in processing digit information. Fig. 5 shows two views of the memory register. The view called bit shifting contains the necessary logic circuitry to explain the shifting function. The view called



COUNTER OPERATION

M.R. STATE	OPER CT— GATE	INHIB IS— GATE	WRITE INTO STORE
0000	CT12	NONE	0001
0001	CT13	IS1A	0010
0010	CT12	NONE	0011
0011	CT14	IS1A IS2A	0100
0100	CT12	NONE	0101
0101	CT13	IS1A	0110
0110	CT12	NONE	0111
0111	CT15	IS1A IS2A IS3A	1000
1000	CT12	NONE	1001
1001	CT13	IS1A	1010
1110	CT12	NONE	1111
1111	CT16	IS1A THRU IS4A	0000
0000	CT12	NONE	0001

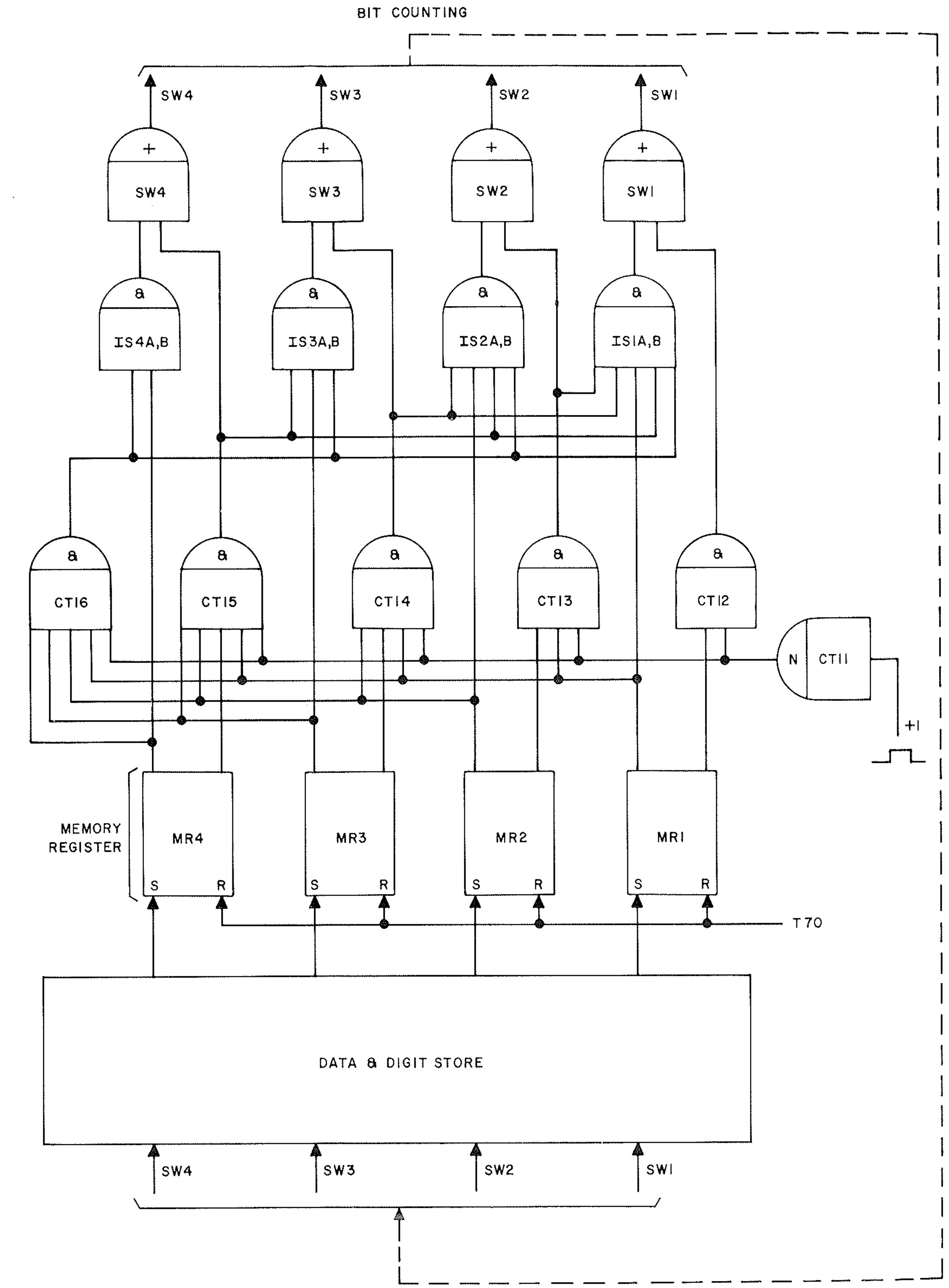


Fig. 5 — Memory Register Functions

bit counting shows only those gates necessary to accomplish the counting function.

B. Shift Register

5.02 The data and digit store is read at time T00. The output of the store is used to set the bits in the memory register (MR). If a bit in the store is a 1, it sets the corresponding flip-flop in the memory register when it is read. If it is a zero, no action takes place. All the bits of the memory register are reset to zero at the beginning of the read-write cycle. The word in the store is then read into the memory register. If the memory register is not being used as a shift register, the inhibit shift (INSH) lead is grounded and the shift enable (SHEN) lead is positive. Therefore, IS gates 1A through 16A are enabled and SH gates 2 through 15 are inhibited. When a bit position is set to 1, the set output of the flip-flop for this bit is in the ground state.

5.03 When it is desirable to use the memory register as a shift register, the SHEN lead is ground and the INSH lead is positive. Now IS gates 1A through 16A are inhibited and SH gates 2 through 15 are enabled. As an example when MR16 is a 1 (set side at ground state), the SH15 gate is enabled which in turn enables the SW15 gate. Lead SW15 writes the 1 into bit 15 of the store. The bit has therefore been shifted one position to the right. By controlling the INSH and SHEN leads, it is possible to make the memory register write its contents directly into the store in the same relative position or to shift its message down one position to the right.

5.04 This shifting function is used either to receive incoming messages or to send outgoing messages from and to the switch unit. The incoming message bits are fed to the set side of MR16 during time T20. At T40 this bit is written into bit 15 of the store. On the next scan at T00, bit MR15 is read out of the store, at time T20 the next bit of the incoming message is used to set bit 16 of the MR, and the first bit is now read into MR15. Both bits are shifted to the right by one position when written back into the store at T40. The entire 12 or 14 bits of the incoming message are processed in this way.

5.05 Since the first bit of an incoming message is always a 1, it will continue to shift down the memory register until it reaches MR2, at which time circuitry is used to recognize a 1 in this position signifying that a complete message has been received and that further shifting should be inhibited. The contents of the memory register are written into the data and digit store without shifting and are cycled between the store and memory register until the program is ready to accept the message.

5.06 Outgoing messages also use the shifting function of the store to shift the bits out. It is noted that MR2 cannot shift into MR1 because the SH1 gate does not have MR2 as an input and the first outgoing data bits are sent to the outgoing data logic from MR2 as each bit of the word is successively shifted into MR2. When bits 3 through 16 are detected as being all zeros and MR2 is a "one" (outgoing messages always have a one in bit 16 originally), MR1 will then be sampled (the one in bit 16 originally is not sent out).

5.07 The INW lead inhibits both the IS gates and the SH gate, thereby causing zero output on all SW leads, which clears the store.

C. Counter

5.08 Fig. 5 also shows the bit counting function of the memory register. Only 4 bits are shown, but the memory register has the capability to count in four separate sections. The first counter consists of bits 1 through 4, the second counter consists of bits 5 through 8, a third consists of bits 9 through 12, and a fourth consists of bits 13 through 16. It is possible to tie the first three counters together and use bits 1 through 12 as a single large counter.

5.09 The counting (CT) gates shown in Fig. 5 are not actually part of the memory register functional schematic. They belong to the circuit called plus 1 adder. However, it is convenient to show their operation directly with the memory register. The SH gates are disabled during the counting function and are not shown.

5.10 Counting is accomplished by using the +1 adder, memory register, and the read-write cycle of the store. Consider that MR1 through 4 are all zeros. The output of each flip-flop goes directly to its IS gate. In the case of all zeros, all the IS gates are inhibited because bits MR1 through 4 are reset. However, when the CT11 gate is pulsed by a positive pulse with MR1 reset, the "and" condition of gate CT12 is satisfied, causing the output of the SW1 gate to go to ground. Therefore, a 1 is written into bit 1 of the store, while bits 2 through 4 are written as zeros.

5.11 On the next scan MR1 is set to a one by the store while MR2 through 4 remains reset. The set side of the MR2, MR3, and MR4 being positive inhibits their respective IS gates. However, gate IS 1A,B is inhibited from writing a "one" back into MR1 because gate CT13 is now enabled. Gate CT13 conditions are satisfied because the reset side of MR2 and the set side of MR1 are ground, when the CT11 gate is pulsed to ground. The result is that bit 1 in the store is reset and bit 2 is set to a one. Bits 3 and 4 are still zeros. On succeeding scans, similar techniques cause the count of bits MR1 through 4 to be incremented once every cycle.

5.12 The preceding description is shown on line 2 of the counter operation chart (center of Fig. 5). The first column of the chart shows the state of the memory register which has been read from the data and digit store. The next column indicates the particular CT gate which is operated. The third column shows the IS gate or gates that are inhibited by the CT output, if any; and the fourth column shows the information that is written into the store.

5.13 When the lower order bits are all ones (e.g. MR1 through 4), gate CT16 inhibits ones from being written back into bits 1 through 4 and causes gate CT21 (not shown on Fig. 5) to be pulsed to ground and the second group of 4 bits (MR5 through 8) are incremented by one. The second group of 4 bits will be incremented once every time the lower order bits are all "ones."

5.14 In this manner the memory register, the plus 1 adder, and the store all operate together to perform a counting function. The function is limited in that only one count can be added per scan, and in that the counter is only enabled during the digit portion of the scan. Both the digit and the sender control use it for timing, counting dial pulses, and counting incoming and outgoing digit positions.

6. DATA CONTROL

A. Incoming Message

6.01 The incoming message bits are sent serially from the switch unit to the incoming data trunk. (See Fig. 6.) When the word in the data and digit store associated with the incoming data trunk is addressed, the scanner enables the trunk to sample the incoming data. If the bit in the incoming data trunk was a 1, the ICDO lead sets MR16 of the memory register. The memory register is used as a shift register in this operation. The bit is shifted one position to the right when it is written into the data and digit store (see Fig. 5). On succeeding scans the other bits of the message are sampled and shifted into the store through the memory register.

6.02 The bit rate of the incoming message is such that each bit is sampled at least once (scan cycle time/message bit duration = 7/8). When a bit is sampled for the second time, the incoming data trunk puts a positive potential on the SH3 lead (Fig. 6), which sets flip-flop NSH3A. This in turn causes the INSH lead to go to ground and conversely the SHEN lead is positive. The shifting function of the memory register is inhibited at this time, the word is written into the store, and the pulse is therefore not double sampled.

6.03 When the incoming message has been completely shifted into the store, bit MR2 contains the start bit (see Fig. 7). The start bit is always a 1. MR2, being a 1, enables gate NSH5 in the shift control circuit which sets the NSH3A flip-flop. This inhibits the shift. Bit MR2, being a 1, causes the WMR2 lead to be positive which inhibits gate NICD so that no further bits can be received by the memory register for this switch unit. The incoming message is cycled between the store and the memory register without shifting until the program is ready to accept the message.

6.04 The call processor is organized to handle the problems of each switch unit in what is called a sector. At the beginning of each sector a start (STT) command interrupts the data control to perform three functions:

(1) It checks to see if the outgoing data trunk for the switch unit is available.

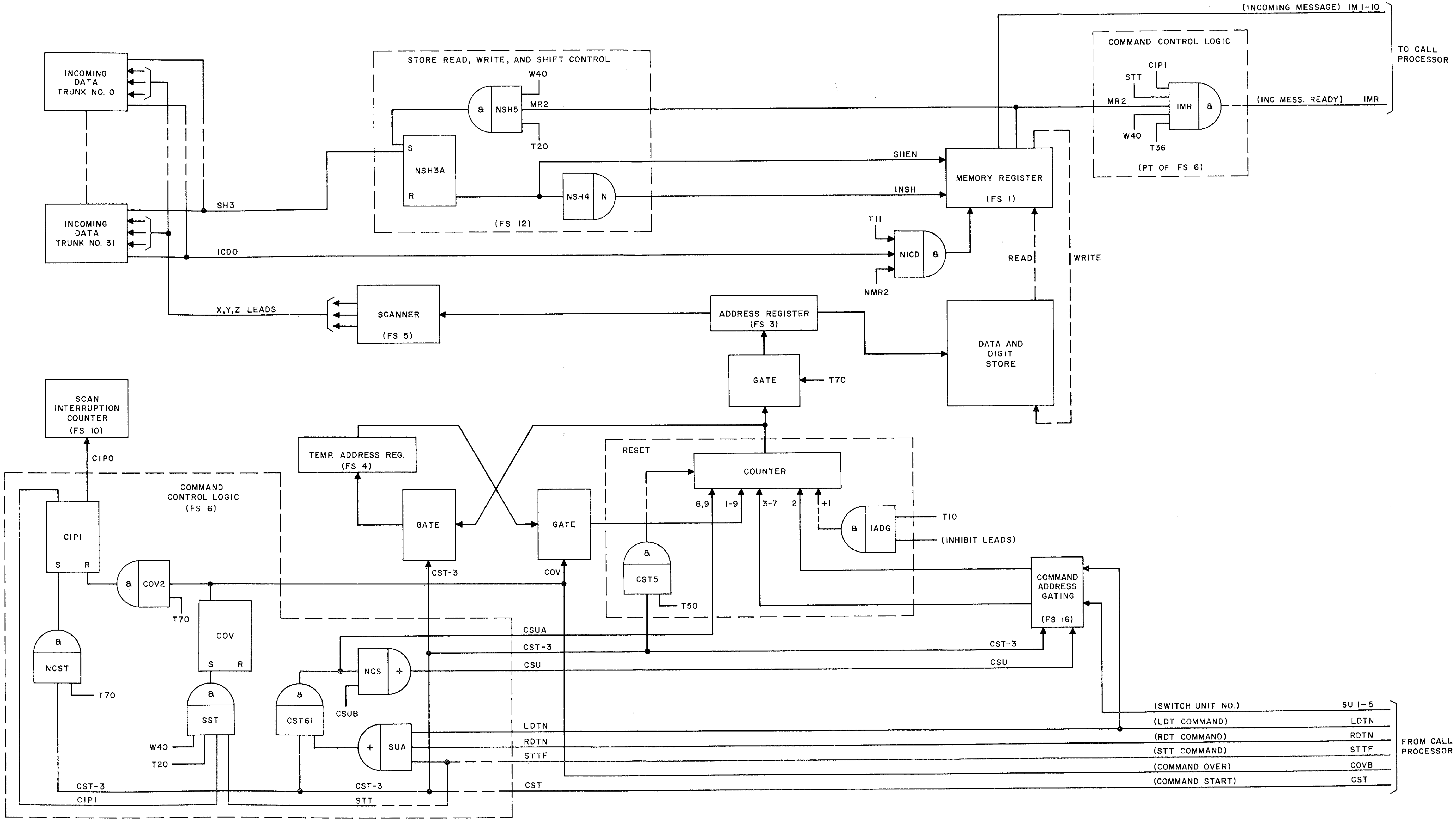


Fig. 6 — Incoming Message Function of Data Control

BIT POSITION IN STORE AND MEMORY REGISTER

TYPE OF MESSAGE	WORD DECIMAL	WORD BINARY		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
OG	1	00	ORDER OF BIT TRANSMISSION	–	15	14	13	12	11	10	9	8	7	6	5	4	3	2,1	16
			DATA CONTROL DESIGNATION	CB1	A3	A4	A5	A6	A7	A8	TS1	TS2	TS3	TS4	TS5	TS6	SC	–	A2
			CALL PROCESSOR DESIGNATION	–	CO3	CO4	CO5	CO6	CO7	CO8	TS1	TS2	TS3	TS4	TS5	TS6	SC	–	CO2
OG	2	01	ORDER OF BIT TRANSMISSION	–	30	29	28	27	26	25	24	23	22	21	20	19	18	17	31
			DATA CONTROL DESIGNATION	CB2	CN1	CN2	R2	R1	CF	B1	D2	B3	D4	B5	B6	B7	B8	A1	SPLIT
			CALL PROCESSOR DESIGNATION	–	ASC7	ASC8	P54	P53	P52	CO9	CO10	CO11	CO12	CO13	CO14	CO15	CO16	CO1	P55
OG	3	10	ORDER OF BIT TRANSMISSION	–	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32,47
			DATA CONTROL DESIGNATION	CB3	C1	C2	C3	D1	D2	D3	S1	S2	S3	K1	K2	L1	L2	L3	
			CALL PROCESSOR DESIGNATION	–	PS6	PS7	PS8	PS9	PS10	PS11	PS12	PS13	PS14	PS15	PS16	ASC4	ASC5	ASC6	–
1A SWITCH UNIT INC	4	11	ORDER OF BIT RECEPTION	–	–	–	12	11	10	9	8	7	6	5	4	3	2	1	–
			SWITCH UNIT DESIGNATION	–	–	–	PARITY	STATUS	1	2	4	8	16	32	64	128	256	START "1"	PARITY CHECK 1=GOOD
			CALL PROCESSOR DESIGNATION	–	–	IM1	IM2	IM3	IM4	IM5	IM6	IM7	IM8	IM9	IM10			–	–
2A AND 3A SWITCH UNIT INC	4	11	ORDER OF BIT RECEPTION		14	13	12	11	10	9	8	7	6	5	4	3	2	1	
			SWITCH UNIT DESIGNATION		PARITY	STATUS	1	2	4	8	16	32	64	128	256	512	1024	START "1"	PARITY CHECK 1=GOOD
			CALL PROCESSOR DESIGNATION			IM1	IM2	IM3	IM4	IM5	IM6	IM7	IM8	IM9	IM10				

NOTE:

CB1, 2 AND 3 ARE CONTROL BITS AND ARE NOT TRANSMITTED. (THEY ALSO EQUAL ONE)

Fig. 7 — Store Layout of Switch Unit Data Words

(2) It checks to see if an incoming message has been received by the data control and if so the message is gated to the call processor.

(3) It causes the digit receiver of the digit control to be cleared if it was in the appropriate state.

6.05 All interruption commands activate the CST lead. The CST lead activates the command control logic. The command control logic directs a number of events. The next normal scan address is gated from the address counter to the temporary address register. Then word 3 of the desired switch unit area is loaded into the address counter. This is accomplished by jam setting bits 8 and 9 of the address counter to one, gating the switch unit number into bits 3 through 7, and jam setting a one into bit 2. The command in progress (CIP1) flip-flop is set and it activates the scan interruption counter. The address for word 3 of the switch unit area is gated into the address register, and word 3 is read out of the store. Word 3 is associated with the outgoing message and its treatment is discussed later. During the read/write cycle of word 3, the address counter is incremented by adding one. Then the address for word 4 is gated to the address register, and word 4 is read into the memory register. Bit MR2 contains the control bit if the message is complete (see Fig. 7). Therefore, the incoming message ready (IMR) lead transfers the indication of a completed message to the call processor. The incoming message is then gated to the call processor through a gate which is located in the call processor. In the meantime, the COV flip-flop in the command logic circuit is set. This generates a command-over signal which resets the CIP1 flip-flop, stopping the scan interruption counter. The COV flip-flop also sends a command-over signal to the call processor, and it gates the address which marks the normal scan location back to the address counter. The normal scan is then resumed.

B. Outgoing Message

6.06 At the beginning of a sector (switch unit area) in the call processor, the STT command is used to check for an available data trunk. (See Fig. 8.) The STT command directs the data and digit store to read word 3 of the scanned switch unit area. If word 3 contains all zeros, the gate IDL1 will be enabled, causing lead IDLD to go to ground. If the IDLD lead is ground for this switch unit, the outgoing data trunk is idle. The call processor remembers this condition and at a later time sends another command to load an outgoing message into the data and digit store. The incoming message is interrogated during word 4. The COV flip-flop is set during word 4 to end the command. The call processor stores the incoming message if it is complete and records the busy-idle status at the outgoing trunk. Then it proceeds to process the sector (switch unit area at call store). If it becomes necessary to send an outgoing message, it checks its memory to see if the outgoing trunk was idle at the time of the STT command. If the outgoing trunk is busy, the call processor keeps sending request data trunk (RDT) commands to the data control circuit. The RDT command checks word 3 for an idle outgoing trunk. When the outgoing trunk becomes idle, the next RDT command relays this information to the call processor. Now everything is ready to load the new outgoing message into the data and digit store.

6.07 The load data trunk (LDT) command activates the CST lead which enables the command control logic and sets the CIP1 flip-flop, causing the scan interrupt counter to start timing. The contents of the address counter are then gated to the temporary address register. The address counter is reset, bits 8 and 9 are set to one, the switch unit number is gated into bits 3 through 7, and bits 1 and 2 are left zero.

6.08 Word 1 is cleared from the store by using the destructive read-out mode during the LDT command. This inhibits the sense amplifiers and all zeros are read into the memory register. The outgoing data (Fig. 7) is gated into the store through the outgoing message gate. The first word of a new outgoing message is gated into the memory register and written into the store. The address is advanced by ***adding*** one to the address counter. Word 2 is destructively read out of the store and the second word of the new outgoing message is gated into the store. Then word 3 is destructively read from the store and a third word of the new outgoing message is gated in. At the beginning of each LDT command lead NSHN goes positive. This inhibits sending of the message to the switch unit until the program gives a go-ahead signal by setting NSHN to ground. This is necessary, for the program may wish to change the

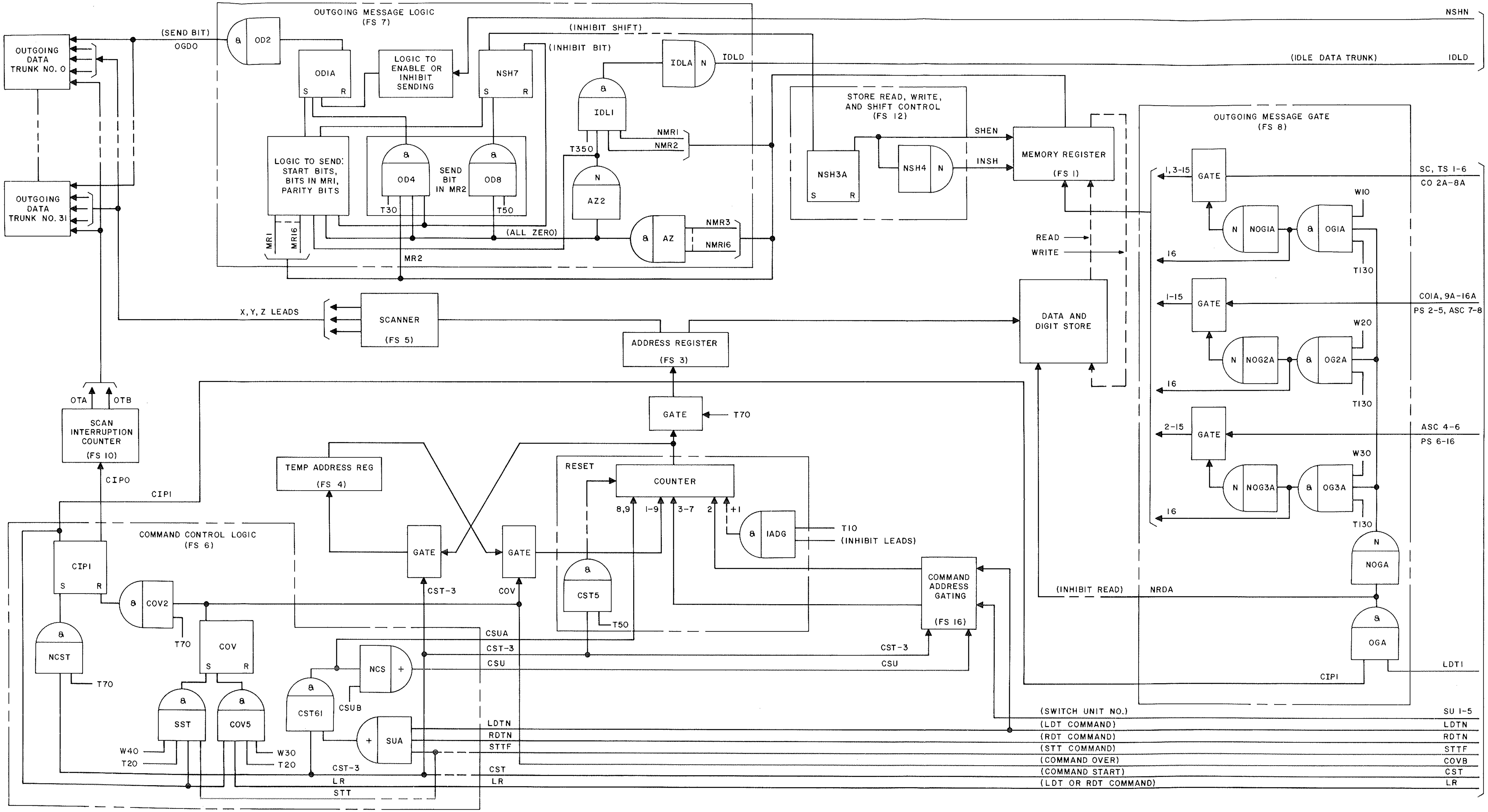


Fig. 8 — Outgoing Message Function of Data Control

contents of the outgoing message by giving RED and WRDS commands.

6.09 Message bits are sent to the outgoing data trunk on the OGDO lead by way of the outgoing message logic, assuming lead NSHN is ground. When the outgoing message words are addressed in the store, the scanner enables the corresponding data trunk and a one is written into the trunk if the OD1A flip-flop is set. This flip-flop is set during T3 of words 1, 2, or 3. At T50 the NSH7 flip-flop is set to inhibit the shift of the other message words. For instance, if the message bits are being shifted out of word 1, the NSH7 flip-flop prevents shifting words 2 and 3. At T50 when the NSH7 flip-flop is set, the first word has already been shifted into the store, but the shift is inhibited for words 2 and 3.

6.10 On the first scan after the message has been loaded, it appears exactly as in Fig. 7. The message bit position does not necessarily correspond to the memory register bit position. In the first word, bit 16 (control bit) is a one and bit 2 is a zero. This word, when read into the outgoing message logic, activates a section of logic (not shown in Fig. 8) which generates the start bits of the message. The OD1A flip-flop is set, and a one is sent to the data trunk. The NSH3A flip-flop in the shift control circuit (Fig. 6) is set immediately, and the shift is inhibited during words 1, 2, and 3. A one is written into bit position 2 of the first word.

6.11 On the next scan the second start code bit which had been written into bit 2 of the first word is sent using a portion of the outgoing message logic called in Fig. 8 ***send bit in MR2.*** The OD1A flip-flop is set because bits 3 through 16 are not all zeros and MR2 is a one. The NSH7 flip-flop is set at T50 (after word 1 has shifted) inhibiting the shift of words 2 and 3. On the following scan the ***send bit in MR2*** logic is used again and a one is sent to the outgoing data trunk if MR2 is a one. The message is shifted out, one bit per scan, until the control bit which was originally in MR16 has been shifted into MR2. Now, MR3 through MR16 are all zeros and MR2 is a one. A portion of the outgoing message logic to ***send bit in MR1*** (not shown in Fig. 8) is activated and sets the OD1A flip-flop if MR1 is a one. It is necessary to do this because bit 1 of the store never shifts. It is simply rewritten into its respective position of each scan. The ***send bit in MR1*** logic circuitry sets the NSH7 flip-flop at T50, inhibiting the shift of words 2 and 3 and also inhibiting the write of the memory register during word 1. Therefore, on the next scan word 1 is all zeros and no action takes place.

6.12 When word 2 is read, the ***send bit in MR2*** circuitry is used to shift out the bits through MR2 of word 2. Now the shift is inhibited during the third word of the data message by NSH7. Bits are sent on subsequent scans using ***send bit in MR2*** logic circuitry until the control bit of the second word is shifted into MR2. Now the ***send bit in MR1*** circuitry is used to send the bit in MR1 of word 2 to the outgoing data trunk. On word 2, however, the inhibit write function is not used. Instead a one is written into bit MR1. The control bit in MR2 is shifted out of the store so that on the next scan word 2 is all zeros except for MR1 being a one.

6.13 This activates the send parity logic portion of the outgoing message logic. When word 2 is read, the NSH7 flip-flop is set to inhibit the shift of the third word. Word 2 is written back into the store in an inhibit write function. When word 3 is read, the bit in MR1 (parity bit) is sent to the outgoing data trunk.

6.14 On the next scan words 1 and 2 are all zeros. When word 3 is read, the message is sent using the ***send bits in MR2*** logic. This is used until the control bit of word 3 is read into MR2. Now the ***send bit in MR1*** logic circuitry sends the bit in MR1 (parity bit), inhibits the write function, and the message is complete.

7. DIGIT CONTROL

A. Receiver Scan

7.01 Three digit receivers are scanned during each scan cycle of the store. Seven word times (read/write cycles) are used for each receiver. Word times 1 through 4 correspond to words 1 through 4 of the digit receiver store area (see Fig. 9). The first 4 words are addressed by resetting the word address to 000 and adding 1 to each read-write cycle to increment the counter. Words 1, 2, and 4 contain control bits used by the digit control. Words 3 and 4 contain control bits used by the sender control. Words 5 through 8

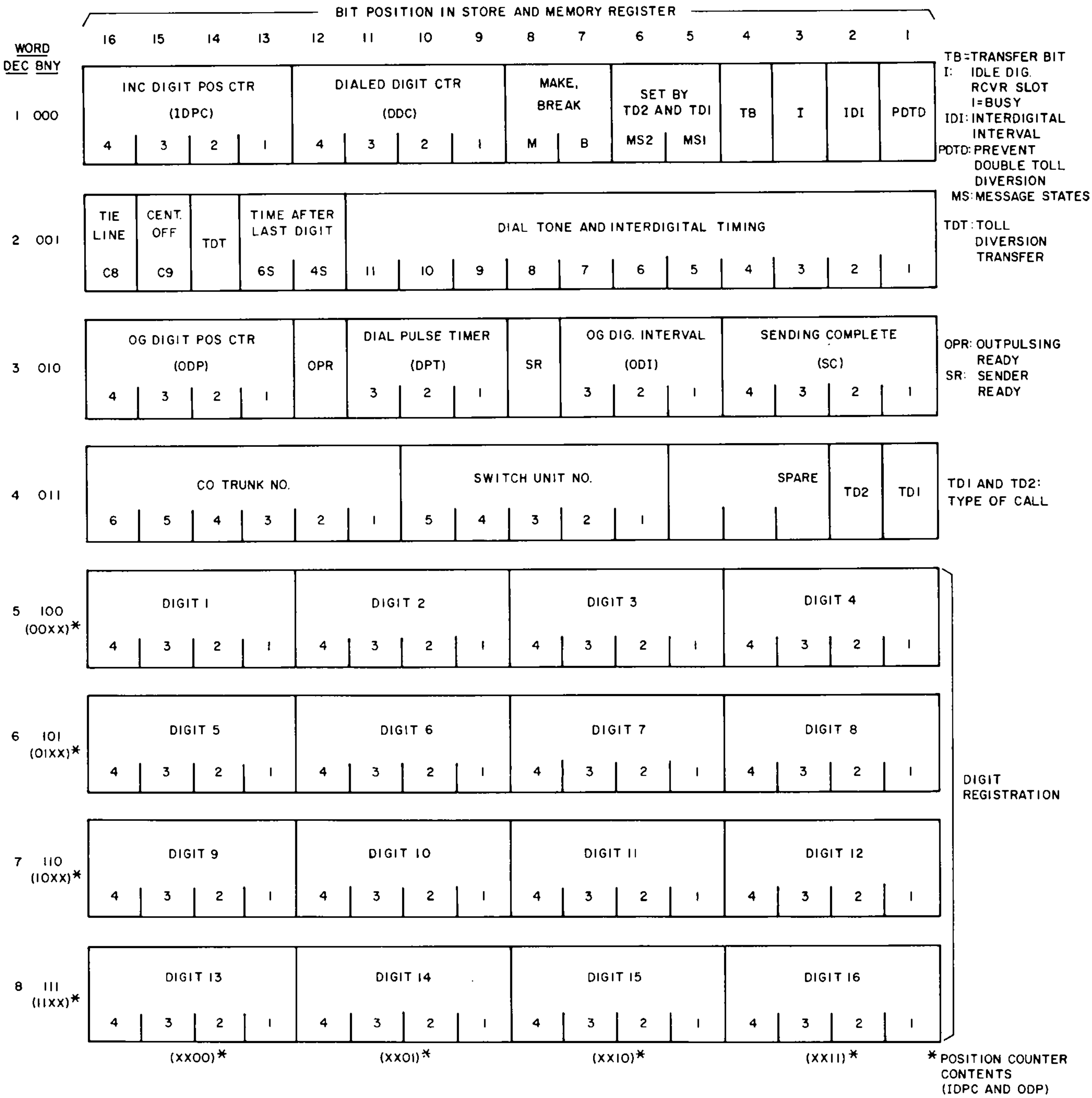


Fig. 9 — Store Layout of Digit Receiver and Sender Information

contain the stored digits. There is room for 16 digits, 4 digits per word. The fifth word time is used by the digit control circuit to store digits. The word addressed depends upon the digit being received. If it is not necessary to read a digit word on a scan, word 1 or word 5 is addressed during the fifth word time. The sixth word time is used by the sender control to address the digit being outpulsed. Word 1 is addressed during the sixth word time if the sender control does not direct the store to a digit. The seventh word time is always used to address word 3.

7.02 The control bits and control counters in words 1 through 4 will be explained later. The incoming digit position counter (IDPC) section (MR13 through MR16) in word 1 contains the position of the digit. The two high order bits of the IDPC describe the word which is used to store the digits (see Fig. 9). The two low order bits are used to describe the quadrant of the word which contains the digits. The IDPC bits are used to remember which digit is being received.

B. Receiving Digits

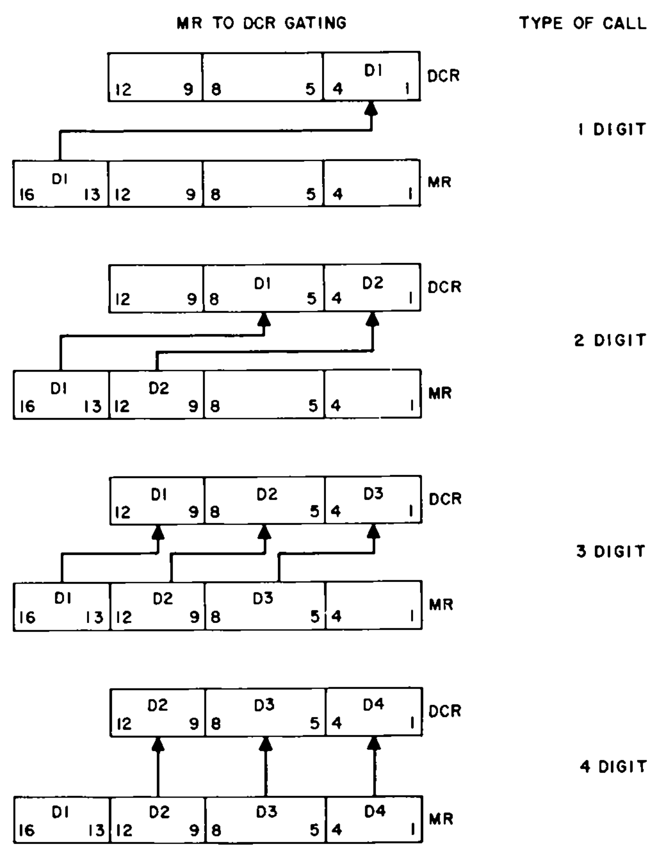
7.03 The digit receiver is enabled (can pass received digits to the digit control) by the scanner throughout all seven word times. The digit leads (L1 through L4, H1 through H4) are fed into the 2-out-of-8 translator (Fig. 10) which translates the 2-out-of-8 code signal to a binary number. Leads A, B, C, and D carrying binary digit information are fed from the 2-out-of-8 translator into the memory register access circuit. The leads are fed through OR gates into the digit decoder circuit. The only things the digit decoder does is to recognize the dial pulse code (1111), to send signals over the dial pulse (DP) lead to the digit control logic circuit if dial pulses are present, and to determine whether an 8, 9, or 0 has been dialed. The digit control logic, in conjunction with the +1 adder, counts dial pulses and also assembles digits. When a digit has been assembled, the digit control logic circuit presents this digit to the OR gates in the memory register access circuit. During word 4 the digit word address for word time 5 is gated into the address counter from the digit control logic on leads DRA, DRB, and DRC. These leads are derived from the two high order bits of the IDPC. During word time 5, the store is addressed to the word which contains the digit being received. The two low order bits of the IDPC are fed into the steering circuit which are then coded to enable one of four gates: DT1A, DT2A, DT3A, or DT4A. This steers the digit into the proper position in the store. The memory register set function circuit and the memory register reset function circuit provide inputs to the memory register. The digit words are first cleared by reading the store destructively before steering the first, fifth, ninth, and thirteenth digits into the store.

C. Types of Digit Messages

7.04 In the processing of all types of calls, intra-PBX as well as trunk, the first digit is always handled in the same manner. (See Tables D and E.) On the first digit receiver scan after the digit has been received, if the digit completed register is idle, the digit will be transferred to the digit completed register. The digit receiver number associated with the dialed digit will be gated from the data control address register to the digit control receiver number register. When the call store output register (CO) of the program control contains the same digit receiver number as the receiver number register and a RED DDR command is given, the contents of the digit completed register are transferred to the CO. The digit completed register is cleared by the next STT command. The program will then decide what type of call is being processed on the basis of the first dialed digit.

TABLE E

MEMORY REGISTER TO DIGIT COMPLETED REGISTER GATING FOR DIFFERENT CALLS



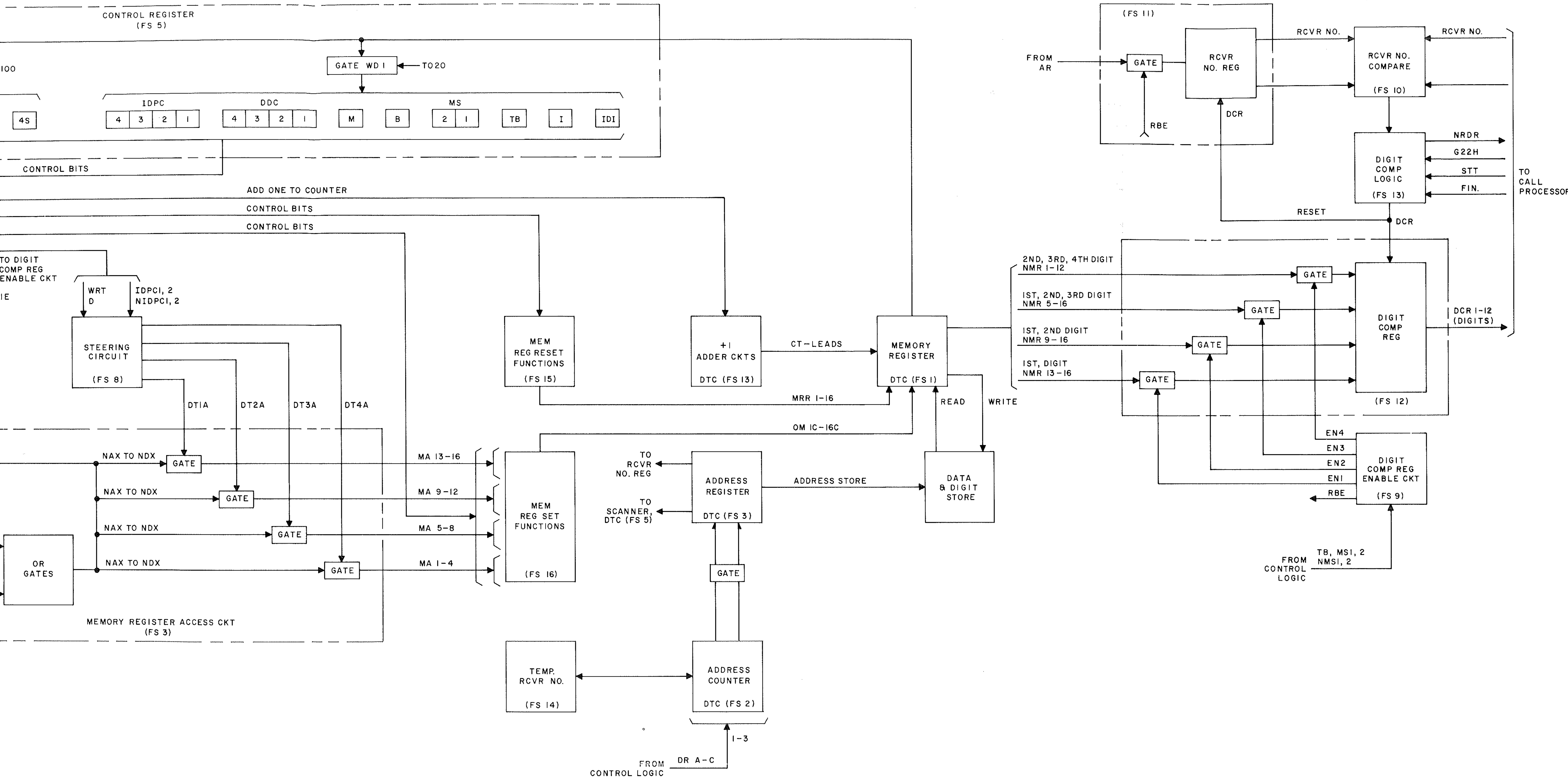


Fig. 10 — Digit Control Function

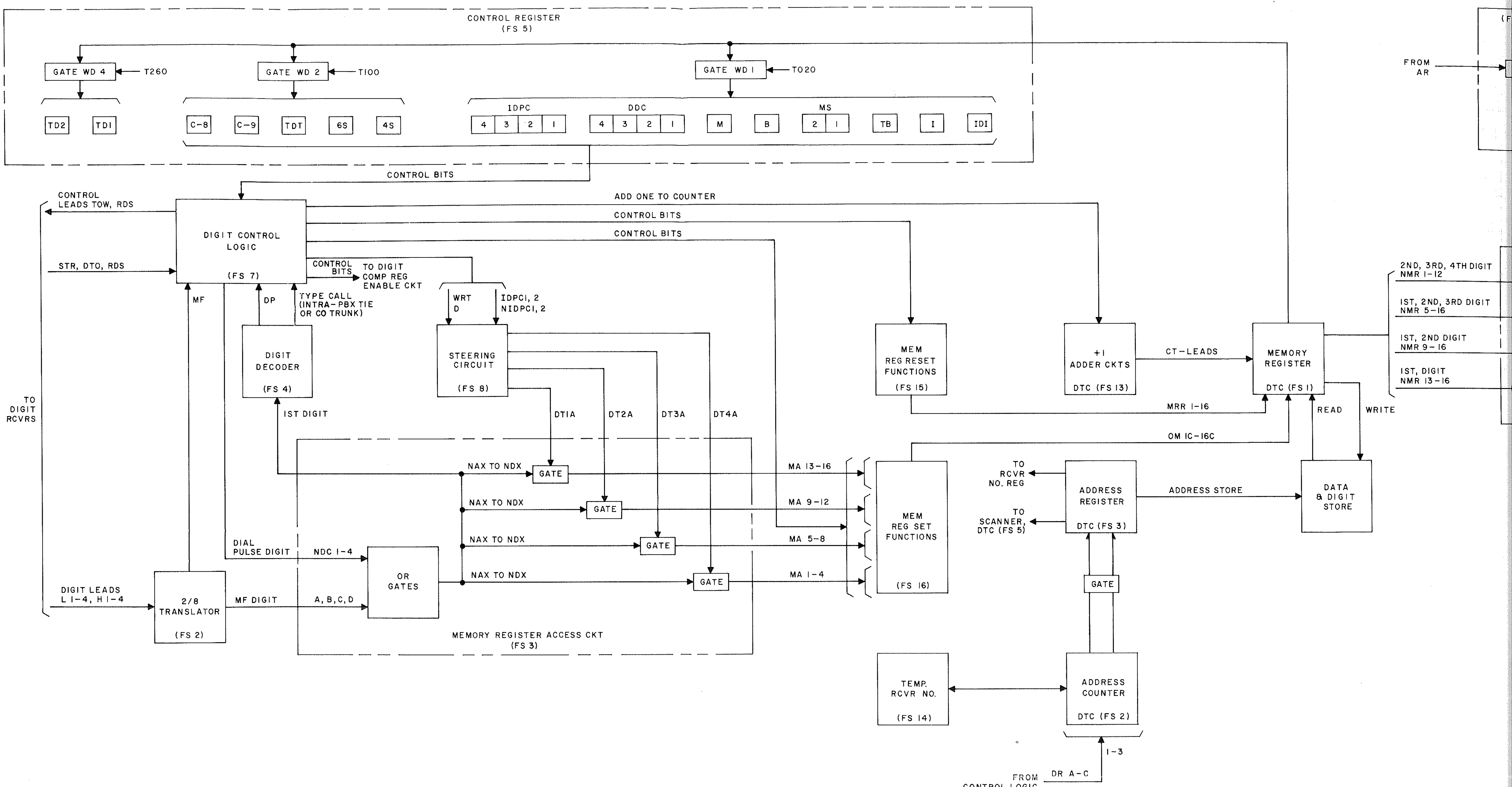

CONTROL REGISTER
(FS 5)
GATE WD 4
T260
GATE WD 2
T100
GATE WD 1
T020
TD2
TD1
C-8
C-9
TDT
6S
4S
IDPC
4 3 2 1
DDC
4 3 2 1
M
B
MS
2 1
TB
I
IDI
FROM
AR
CONTROL BITS
CONTROL
LEADS TOW, RDS
DIGIT CONTROL
LOGIC
(FS 7)
STR, DTO, RDS
ADD ONE TO COUNTER
CONTROL BITS
CONTROL BITS
CONTROL
BITS
TO DIGIT
COMP REG
ENABLE CKT
MF
DP
TYPE CALL
(INTRA-PBX TIE
OR CO TRUNK)
WRT
D
IDPC1, 2
NIDPC1, 2
DIGIT
DECODER
(FS 4)
STEERING
CIRCUIT
(FS 8)
MEM
REG RESET
FUNCTIONS
(FS 15)
+1
ADDER CKTS
DTC (FS 13)
CT-LEADS
MEMORY
REGISTER
DTC (FS 1)
2ND, 3RD, 4TH DIGIT
NMR 1-12
1ST, 2ND, 3RD DIGIT
NMR 5-16
1ST, 2ND DIGIT
NMR 9-16
1ST, DIGIT
NMR 13-16
TO
DIGIT
RCVRS
1ST DIGIT
DT1A
DT2A
DT3A
DT4A
MRR 1-16
READ
WRITE
OM 1C-16C
NAX TO NDX
GATE
MA 13-16
NAX TO NDX
GATE
MA 9-12
NAX TO NDX
GATE
MA 5-8
NAX TO NDX
GATE
MA 1-4
MEM
REG SET
FUNCTIONS
(FS 16)
TO
RCVR
NO. REG
TO
SCANNER,
DTC (FS 5)
ADDRESS
REGISTER
DTC (FS 3)
ADDRESS STORE
DATA
& DIGIT
STORE
DIAL
PULSE DIGIT
NDC 1-4
OR
GATES
DIGIT LEADS
L 1-4, H 1-4
2/8
TRANSLATOR
(FS 2)
MF DIGIT
A, B, C, D
MEMORY REGISTER ACCESS CKT
(FS 3)
GATE
TEMP.
RCVR NO.
(FS 14)
ADDRESS
COUNTER
DTC (FS 2)
1-3
FROM
CONTROL LOGIC
DR A-C

TABLE D

DIGIT CONTROL AND PROGRAM RESPONSES FOR DIFFERENT TYPES OF CALLS

TYPE OF CALL	ONE DIGIT	TWO DIGIT		THREE DIGIT		FOUR DIGIT		CO TRUNK AND COMMON CONTROL SWITCHING ARRANGEMENT		TIE TRUNK					
										8X		TX		TXX	
DIALED NUMBER	(NOTE 3) 0,11,12,13,15	FIRST DIG 1-7,14	(NOTE 1) (1-7)+X 14+X	FIRST DIG 1-7	(1-7)+XX	FIRST DIG 2-7	(2-7)+ XXX	FIRST DIG 8,9		8	8X	T=(2-7)	TX	T=(2-7)	TXX
DIGIT CONTROL RESPONSE	A TRANSFER TO DCR.	A TRANSFER TO DCR.	C TRANSFER (1-7)+X OR 14+X TO DCR.	A TRANSFER TO DCR.	C TRANSFER (1-7)+XX TO DCR.	A TRANSFER TO DCR.	C TRANSFER XXX TO DCR.	A 1. TRANSFER TO DCR. 2. SET C9.	C TREATED AS A TDT (CODE RESTRICTION) CALL.	A 1. TRANSFER TO DCR. 2. SET C9.	C TRANSFER 8X TO DCR.	A TRANSFER TO DCR.	C TRANSFER TX TO DCR.	A TRANSFER TO DCR.	C TRANSFER TXX TO DCR.
PROGRAM RESPONSE	B 1. RED DDR. 2. RELEASE THE DDR.	B 1. RED DDR. 2. WRT DS WD 011 SET BIT 1 (TD1).	D 1. RED DDR. 2. RELEASE THE DDR.	B 1. RED DDR. 2. WRT DS WD 011 SET BIT 2 (TD2).	D 1. RED DDR. 2. RELEASE THE DDR.	B 1. RED DDR. 2. STORE THIS DIGIT. 3. WRT DS WD 011 SET BITS 1 & 2 (TD1 & TD2)	D 1. RED DDR. 2. RELEASE THE DDR.	B 1. RED DDR. 2. IF CCSA OR COT GIVE SECOND DIAL TONE	D 1. RED DDR. 2. WRT S TO LOAD TRK & SU NUMBER.	B 1. RED DDR. 2. WRT DS WD 011 SET BIT 1 (TD1).	D 1. RED DDR. 2. WRT DS WD 001 SET BIT 16 (CB) & RESET BIT 15 (C1).	B 1. RED DDR. 2. WRT DS WD 011 SET BIT 1 (TD1).	D 1. RED DDR. 2. WRT DS WD 001 SET BIT 16 (C8).	B 1. RED DDR. 2. WRT DS WD 011 SET BIT 2 (TD2)	D 1. RED DDR. 2. WRT DS WD 001 SET BIT 16 (C8) 3. WRT DS WD 010 SET BITS 13 & 14 (ODP 1 & 2).

NOTES:

1. X CAN BE ANY DIGIT.
2. SEQUENCE A-B-C-D IS FOLLOWED FOR EACH TYPE OF CALL.
3. DIGITS 11, 12, 13, 14, 15 ARE TTC DIGITS.

Intra-PBX Calls

7.05 *1-Digit Call:* The reception of the first digit has been previously described. If no further digit information is expected, the program will release the digit receiver.

7.06 *2-Digit* Call: After transfer of the first digit which can be 1 through 7 or TOUCH-TONE 14, the program will execute a WRT DS command to word 4 of the digit receiver to set TD1 (Fig. 9). This informs the digit control that a 2-digit transfer is required. After accumulating the two digits, the digit control will transfer them to the digit completed register and the associated digit receiver number to the receiver number register. A RED DDR, directed to the appropriate digit receiver, will then result in the transfer of the two digits from the digit completed register to the CO. If the program does not expect any further digits, it then must release the digit receiver in order to clear the corresponding time slot in the digit receiver connector. This action will in turn clear the associated digit receiver memory location in the data and digit store.

7.07 *3-Digit Call:* The first digit of a 3-digit call may be any number 1 through 7. After the first digit has been received and transferred to the program control, a WRT DS command will be executed by the program to set TD2 of word 4. This informs the digit control that a 3-digit transfer is required. When the three digits have been recorded, they will be transferred to the digit completed register. After executing the RED DDR, the program will release the digit receiver and the data and digit store will be cleared in the same manner as previously described.

7.08 *4-Digit Call:* The first digit of a 4-digit call may be any number 2 through 7. This number will be processed through the digit control in the same manner as the first digit of the 2- and 3-digit calls, but unlike the first digit of the other calls, the first digit of a 4-digit call must be stored by the program. Since the digit completed register can handle only three digits, the second transfer will gate the second, third, and fourth digits to the digit completed register.

7.09 After reception of the first digit, the program will execute a WRT DS setting TD1 and TD2 of word 4. This informs the digit control that a 4-digit transfer is required. No further action is taken by the digit control until four digits have been recorded. Once all digits have been recorded, the second, third, and fourth digits will be gated to the digit completed register. A RED DDR will transfer the information to the CO. Again the digit receiver must be released by the program to clear the data and digit store.

Trunk Calls

7.10 *First digit 9 or 8:* If the first digit of the call is a 9, the call is treated as a regular CO trunk call with no change in the toll diversion transfer routine. However, if the first digit is an 8, the program must decide if this is a Common Control Switching Arrangement (CCSA) call or an 8X-type call. If it is a CCSA-type call, the action taken is similar to the 9-type call. If the call is an 8X type, the program must receive the second digit before taking further action. Transfer of the 8X is made in the same manner as the 2-digit call. However, since the first digit is an 8 or 9, bit C9 is automatically set. This would normally cause outpulsing to start from the second digit. Hence, C9 must be reset and C8 set. The program must give a WRT DS command to set C8 (bit 16) and reset C9 (bit 15) of word 2. Once C8 = 1, the outgoing digit position counter (ODP) will be updated to a count of two, and outpulsing will start with the third digit. After outpulsing is complete, a signal known as sender complete will (1) notify the program that outpulsing has terminated, and (2) cause the data and digit store to be cleared.

7.11 *TX or TXX:* The initial reception of the T, which can be any digit 2 through 7, by the program must be decoded to determine whether TX or TXX is to be expected.

(a) The transfer of TX to the program control is performed in the same manner as a 2-digit intra-PBX call. However, before second dial tone can be given, the C8 bit must be set by a WRT DS. This again updates the ODP to a count of 2 so that outpulsing will start from the third digit.

(b) The transfer of TXX to the program control is handled in the same manner as a 3-digit intra-PBX call, but after TXX has been decoded as a tie trunk code, outpulsing must start with the next digit. To accomplish this, the program must execute two WRT DS commands before proceeding any further. The first sets C8 and the other updates the ODP to a count of 3.

Special Case

7.12 In certain situations, the program may not be able to determine how many digits to expect, after reception of the first digit. An example of this is the 1X or 11X codes. The program has no way of determining, after receiving a 1 as the first digit, whether or not the second digit will be a 1. For this reason, after receiving the first 1, conditions should be set for a transfer of 1X. It is possible, however, that the 11X code is being dialed and that it might be received before the 2-digit transfer is made. If this were to happen, the first two digits would never be transferred to the digit completed register, since the incoming digit position counter (IDPC) would be equal to a count of 3. Circuitry within the digit control will recognize this condition and execute a 2-digit transfer, even though three digits have been received. After the program receives the 11, it should then execute a WRT DS command to set TD2 and the 3-digit transfer of the 11X will ensue.

D. Digit Control Logic

7.13 The digit control logic in conjunction with the +1 adder counts dial pulses, temporarily stores the pulses, steers dial pulse or TOUCH-TONE (T-T) digits into the proper digit position of the store, and recognizes when the total number of digits have been received.

7.14 Some of these functions are shown in Fig. 11. Control leads are from the digit receiver. During the break intervals of a rotary dialed digit and also while a T-T key is depressed, the STR lead is ground which sets the STRF flip-flop (see STR lead buffer section of Fig. 11). Leads STRA and NSTRA are used to enable various gates in the digit control logic circuit.

7.15 Word 2 of the digit receiver store area contains the timer used for interdigital and dial tone time (see Fig. 9). This timer is only active when the digit receiver is in a busy state (I bit of word 1 is a one). When this is the case, gate CT12B will increment the count once every 20.4 milliseconds. If this timing occurs during a dial tone period, counting will continue for 12 or 24 seconds, at which time a time-out message will clear the store. The program will then be informed via the digit completed register that the digit receiver has timed out. After a digit has been dialed, time-out can occur in 6 or 24 seconds. In either case, the counter will be reset if a new digit is dialed.

7.16 The dial pulse call section of Fig. 11 shows the STR lead condition for the last pulse of a digit. On the first scan of the break, the M bit of the control register is a 1 and the B bit is 0. These bit states are gated from the store at time T020. When inputs STRA, DP, and NB are all ground at time T030, gate DBS is enabled. The output of this gate resets the M bit, sets the B bit, and adds 1 to the dialed digit counter (DDC) in the store. This is accomplished by setting or resetting the bits in the memory register and then writing the result back into the store. The +1 adder circuit is used to add 1 to the DDC. The DDC is used to count the Make-Break cycles of a rotary dialed digit. The digit control logic can detect when a rotary digit is complete by timing for 160 msec after a Make-Break cycle. When the digit is completely received it will be transferred from the DDC to the digit storage location in the store. Gate WRTD enables the steering circuit to perform this function. During the second word at time T110, the dial tone time-out count in the timer will be reset by gate DTOR.

7.17 During the next scan the timer is incremented, but no other action takes place. On the first scan of the Make interval, however, gate DMS is activated at time T030 during the first word. This gate updates the M and B bits in the store to indicate a Make condition. Several more scans are used in which the only action taking place is to increment the timer. On the ninth scan, counting from the first scan of the Break, the memory register contains a 1 in MR4 of word 2. During this scan the IDTA,B gate sets the IDT0 flip-flop during the second word time. During the fifth word time the IDTOG gate is enabled and sets the IDI (interdigital interval) bit in the memory register. The fifth word time is normally used for addressing word 5 if no digits are being outpulsed. The first word is read during the fifth word time, as a special case, so that the IDI bit can be set.

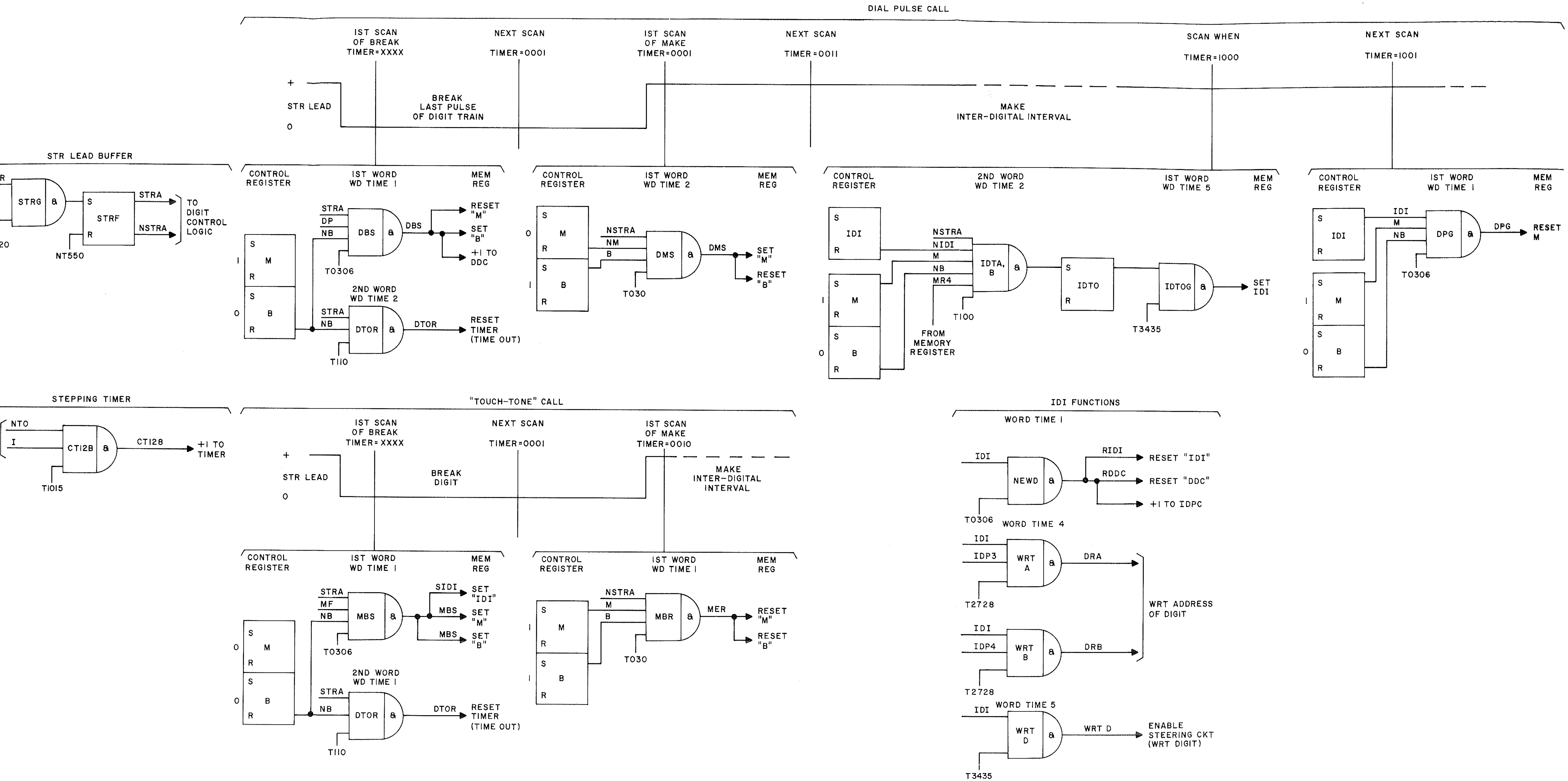
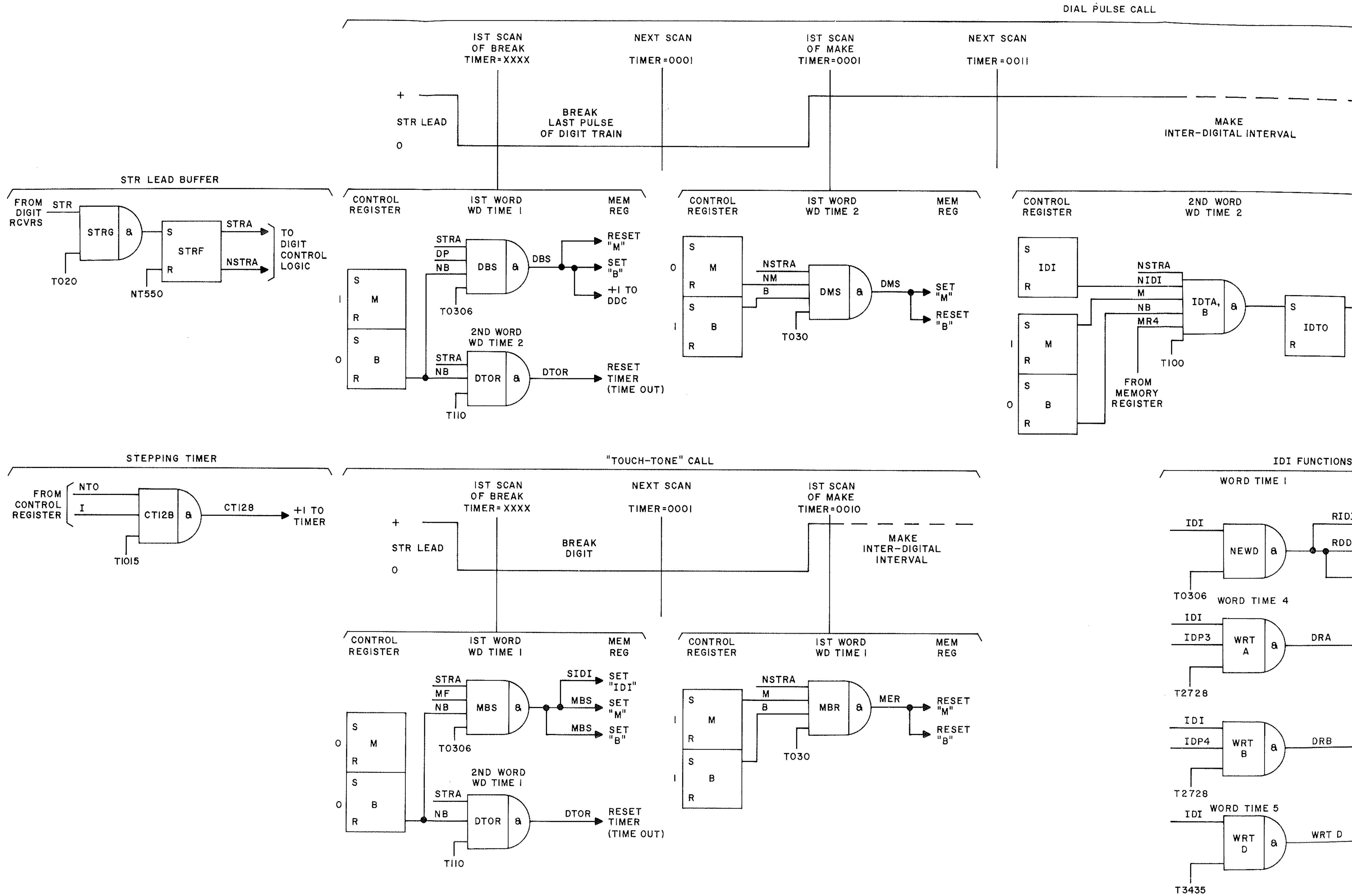


Fig. 11 — Receiving Pulses and Digits in Digit Control



DIAL PULSE CALL
IST SCAN OF BREAK TIMER=XXXX
NEXT SCAN TIMER=0001
IST SCAN OF MAKE TIMER=0001
NEXT SCAN TIMER=0011
STR LEAD
BREAK LAST PULSE OF DIGIT TRAIN
MAKE INTER-DIGITAL INTERVAL
STR LEAD BUFFER
FROM DIGIT RCVRS
STR
STRG
STRF
STRA
NSTRA
TO DIGIT CONTROL LOGIC
T020
NT550
CONTROL REGISTER
IST WORD WD TIME I
MEM REG
DP
NB
DBS
RESET "M"
SET "B"
+I TO DDC
T0306
2ND WORD WD TIME 2
DTOR
RESET TIMER (TIME OUT)
T110
IST WORD WD TIME 2
NM
DMS
SET "M"
RESET "B"
T030
2ND WORD WD TIME 2
IDI
NIDI
MR4
IDTA, B
IDTO
T100
FROM MEMORY REGISTER
STEPPING TIMER
FROM CONTROL REGISTER
NTO
CT12B
CT128
+I TO TIMER
T1015
"TOUCH-TONE" CALL
IST SCAN OF BREAK TIMER=XXXX
NEXT SCAN TIMER=0001
IST SCAN OF MAKE TIMER=0010
BREAK DIGIT
MAKE INTER-DIGITAL INTERVAL
IST WORD WD TIME I
MF
MBS
SIDI
SET "IDI"
SET "M"
SET "B"
2ND WORD WD TIME I
MBR
MER
RESET "M"
RESET "B"
IDI FUNCTIONS
WORD TIME I
NEWD
RIDI
RDDC
WORD TIME 4
IDP3
WRT A
DRA
T2728
IDP4
WRT B
DRB
WORD TIME 5
WRT D
T3435

7.18 On the next scan the IDI flip-flop in the control register is set, enabling a number of gates. The DPG gate is activated during the first word time to reset the M bit. The NEWD gate (see IDI functions in Fig. 11) is also activated during the first word time to reset the IDI, reset the DDC, and add 1 to the IDPC. These actions prepare the control bits in word 1 to receive the next string of dial pulses.

7.19 The state of the STR lead condition for a T-T call is shown in the lower portion of Fig. 11. During the first scan of the Break the M and B bits are both zero. The STRA lead is grounded, indicating the presence of a digit. The MBS gate is enabled to set the IDI bit, the M bit, and the B bit. The DTOR gate resets the timer in word 2. On the next scan the timer is incremented but no other action takes place. On the first scan of the Make interval, the MBR gate is activated. This gate resets the M and B bits. In this way T-T digits are stored.

8. SENDER CONTROL

A. Regular Outgoing Call

8.01 The call processor assigns a trunk number to all outgoing calls. (See Fig. 12.) It must load this trunk number into the digit receiver area of the store. The WRT S command (WRK lead) gates the trunk number, the switch unit number, and the digit receiver number into the sender register. It also gates a 0 or 1 into bit SCR12 of the sender register to indicate an abbreviated dialed call or regular outgoing call.

8.02 The SCR12 bit is a 1 for regular outgoing calls. This bit enables the compare receiver number circuit in the address comparator. The receiver number portion of the data control address register is compared with the receiver number in the sender register. When a comparison is made, the COMP flip-flop is set. This gates the trunk and switch unit number into the store during word 4.

> *Note:* This is not an interrupt type of command for a regular call.

B. Abbreviated Dialing of Central Office Call

8.03 After the WRT S command has loaded the sender register with the CO trunk number, switch unit number, and receiver number, the call processor gives an LSD (load sender) command to the sender control. This is an interruption command. The CST lead (Fig. 2) performs essentially the same functions as for any other interrupt command. The address of the normal scan is saved in the temporary address register and the scan interruption counter is enabled. The LSD command (Fig. 12) gates the receiver number from the sender register to bits 4 through 9 of the address counter and sets bits 1 through 3 to 100 (word 5) with the SD31B lead.

8.04 Word 5 is read destructively into the memory register and the call processor gates the first four digits into word 5. In the meantime the address counter is incremented by adding 1. Words 6, 7, and 8 are loaded in the same way. During word 8 the counter adds 1 and the word address becomes 000 (word 1). Word 1 is read destructively into the memory register. The address comparator circuit sets the I bit to 1, indicating a busy receiver, and sets the incoming digit position counter (IDPC) to all ones. While word 1 is being processed, ASK lead jam sets the address counter to word 3. Word 3 is read destructively into the memory register and the outgoing OPR (outpulsing ready) bit is set. The address counter is incremented by one and word 4 is read destructively into the memory register. The CO trunk and switch unit numbers are written into word 4.

C. Outpulsing

8.05 When the trunk and switch unit numbers are written into the store and the OPR bit is set, the sender control can access the selected trunk through the trunk connector and outpulse into it. On initial digit 9-type calls the SR (sender ready) bit must also be set to permit outpulsing. This bit is set when the second group of digits is transferred from the digit control to the program control when bit TDT is set.

8.06 The digits are written into the store in an inverted binary form. This is true of all digit information written into the store. This is

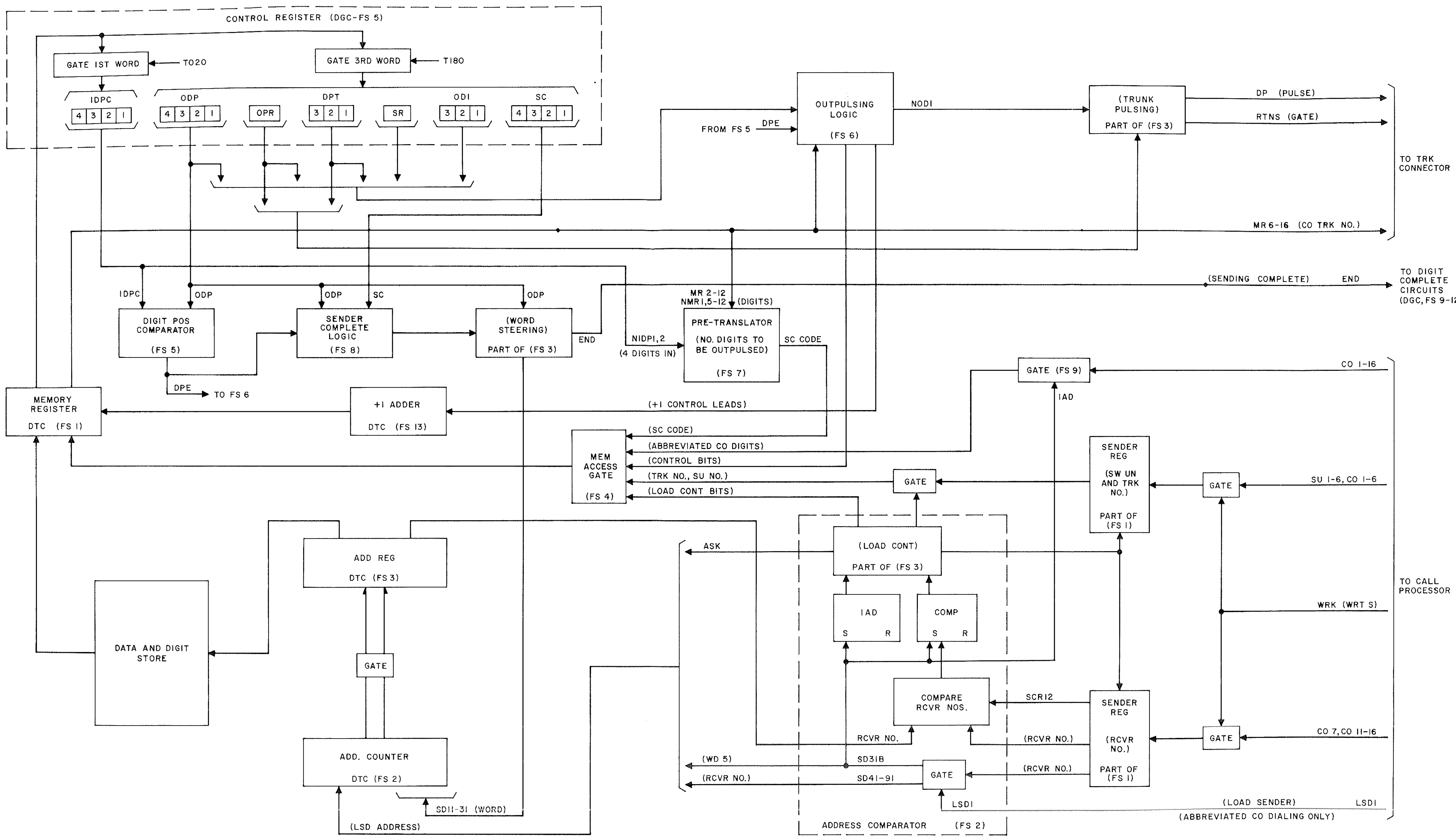


Fig. 12 — Sender Control Function

Pp. 43-44 missing