MAINTENANCE CIRCUITS
DESCRIPTION OF SYSTEM OPERATION
NO. 101 ELECTRONIC SWITCHING SYSTEM

CONTENTS

1. GENERAL

1.01 The maintenance activities of the No. 101 electronic switching system (ESS) are performed in three areas. Two of these areas, maintenance center and teletypewriter, operate in conjunction with each other and are dependent on the call processor to pass information between them. The third area, test point comparator, is manually operated and is used to locate troubles in the data, digit, and sender controls.

1.02 Under normal conditions programmed testing is conducted after the program has completed its call processing duties. These tests are designed so that each test must be successful if the program is to reach its termination point in the scan. A failure of any one of the tests causes a message, to that effect, to be printed out by the teletypewriter. Thus, the teletypewriter furnishes a record of troubles in the No. 101 ESS. This printed record is supplemented by the STATE OF REPAIR REGISTER lamps.

1.03 The teletypewriter can also be used to print in requests for the program to conduct tests. After the requested test has been performed, the teletypewriter prints out the result of that test.

1.04 In addition to testing activities, the maintenance center and the teletypewriter administer the redundant circuits. If a trouble develops, the call processor sends a command to the maintenance center to remove the faulty circuits from service and to place the standby circuits in service. Requests to place redundant circuits in service can be initiated by the teletypewriter in order to facilitate maintenance. A third method of administering the redundant circuits is the use of the keys which appear on the maintenance panel. The last two methods of administering the redundant circuits are impor-

tant because they offer a way to isolate faulty circuits for testing.

2. MAINTENANCE CENTER

A. General Description

2.01 The maintenance center contains circuits which perform three functions. The first function is the placing of the redundant circuits in an on-line or off-line status. To do this, the maintenance program commands the maintenance center telling it which circuits are to be on line and which are to be off line.

2.02 The second function performed by the maintenance center is the detection of failures within the system and the replacement of the faulty circuit with standby circuits. Once a failure has been detected and the faulty circuit has been removed from service, the maintenance program localizes the trouble, and the teletypewriter prints out the information.

2.03 The third function is to permit maintenance activities to be performed without interfering with normal call processing activities. This is accomplished by the teletypewriter and the various keys and lamps on the maintenance panel.

2.04 The maintenance center block diagram (Fig. 1) shows the different circuits which are included in the maintenance center. These circuits are described in detail according to the specific function which they perform. Any effect which these circuits have on each other is determined by the maintenance program.

2.05 Considering the functions of the maintenance center, the administration of the redundant circuits is performed by the timers and transfer control (comprising the on-line timers, 20-minute timer, and the timer transfer control) and the on-line off-line transfer controls (comprising the timer transfer control, trunk connector transfer, data control transfer, and data link switching). The first of these controls which program control is on line, and the second controls the data, digit trunk, and data link circuits.

2.06 A complementary function is performed by the test point reader. This circuit gates signals to the call store output register (CO) which are indicative of the operability of the circuits being monitored. This keeps a current record of the state of repair of these circuits and enables the program to determine what circuits to place in service.

2.07 The test call circuit continually makes test calls which require the proper operation of the digit receivers, digit receiver connectors, and digit controls. Failure to set up a test call results in the replacement of these circuits with their standby counterparts.

2.08 All of the above circuits receive their instructions from the maintenance control translator. In the case of the 20-minute timer, which is the only one capable of independent operation, the command advances the time of the switchover of program controls.

2.09 The program store comparator permits the contents of every word in the program store to be compared and detects any discrepancies which exist.

2.10 The program control controls contain the lamps and keys necessary for manually testing the system. The register lamps permit the display of the contents of the program store address register (PA), program store output register (PSOR), call store output register (CO), line information store address register (LISAR), and line information store output register (LISOR). It is possible to jam set the PA to any address and to execute the command appearing in the PSOR. The STATE OF REPAIR REGISTER lamps indicate the operability of the circuits they monitor.

B. Maintenance Control Translator

General

2.11 There are two maintenance control translators, one associated with each program control. Fig. 2 is a diagram of a maintenance control translator. Instructions are sent from the program shift register circuit over leads CO1A through CO9A to the maintenance control translator. The nine input leads from the program shift register are divided into three groups of three. Each of these input leads goes through an ***and*** gate to a flip-flop. Since a group of three flip-flops has eight different possible combinations of states of conduction and there are three

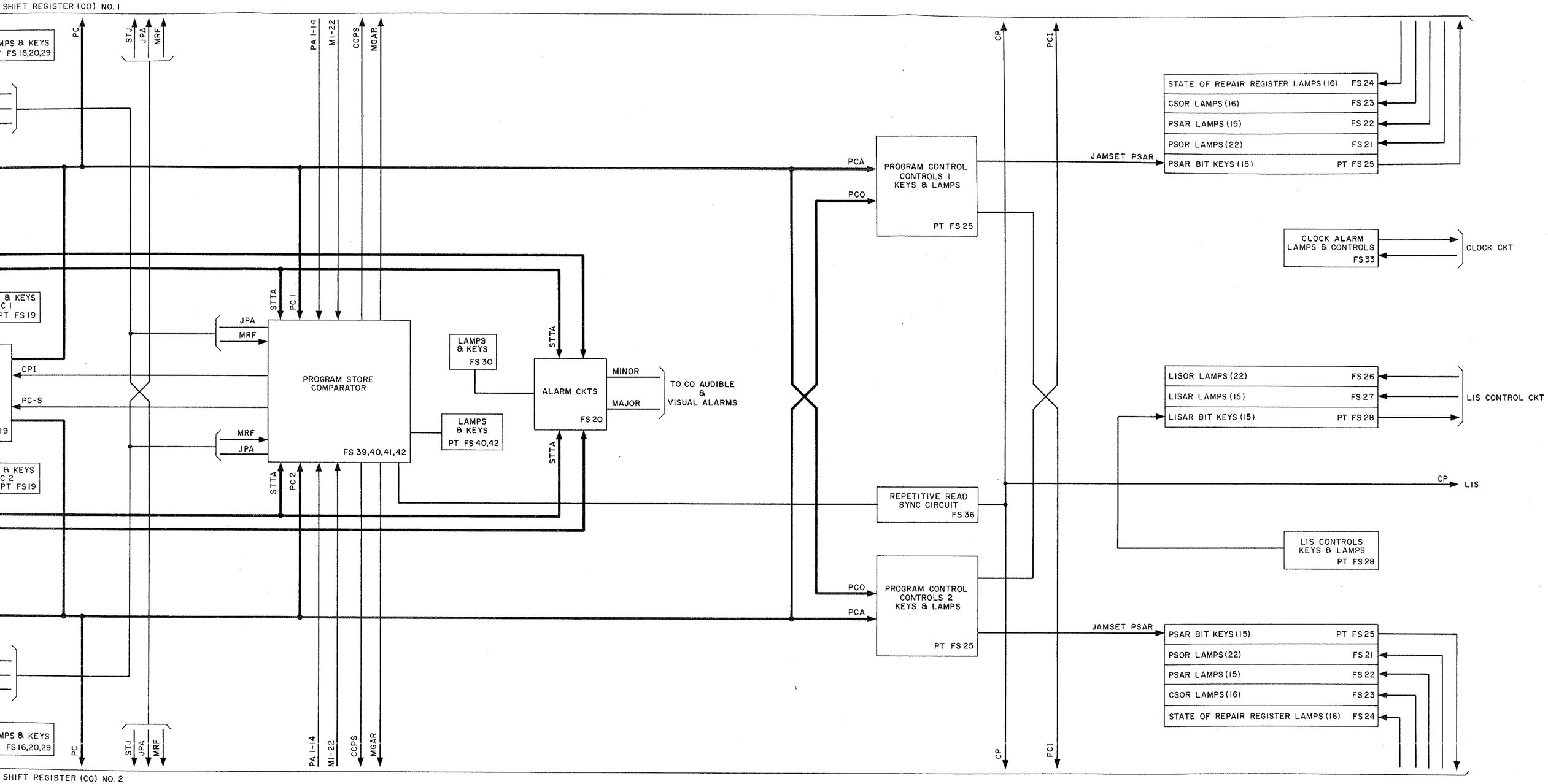


Fig. 1 – Maintenance Center Block Diagram

PROGRAM CONTROL AND PROGRAM SHIFT REGISTER (CO) NO. 1

TPR 1-16

COIA-9A

MAINTENANCE CONTROL TRANSLATOR 1
FS 1,2,3,4

HL- VL- XP-

MTJ1

COIA-3A

ON LINE TIMER 1
FS 15,16

ETJ
MTJ2
CMTJ2

STJ
JPA
MRF

PCO PCA STTA

LAMPS & KEYS PT FS 16,20,29

PC

STJ JPA MRF

PA 1-14 MI-22 CCPS MGAR

DIGIT RCVR CONN 1

TEST POINT READER GATES
FS 37

BUS 1 BUS 2

DIGIT TRUNK APPEARANCE
FS 12

TEST CALL CIRCUIT
FS 8,9,10,11

CONTROL PANEL DIGIT TRUNK APPEARANCE
FS 35

CONTROL PANEL DIAL & T.T. CALLER
FS 34

LAMPS & KEYS PT FS 17,29

PC1 STTA ETJ

20 MINUTE TIMER
FS 17

MTJ1
CMTJ2
CMTJ1
MTJ2

PC2 STTA ETJ

LAMPS & KEYS PC 1 PT FS 19

TIMER TRANSFER CONTROL
FS 18,19

CPI
PC-S

LAMPS & KEYS PC 2 PT FS 19

STTA PC1

JPA
MRF

PROGRAM STORE COMPARATOR
FS 39,40,41,42

MRF
JPA

LAMPS & KEYS FS 30

LAMPS & KEYS PT FS 40,42

STTA PC 2

DIGIT RCVR CONN 2

ALARM DER
FS 45

TEST POINT READER GATES
FS 37

TPR 1-16

HL- VL- XP-

MAINTENANCE CONTROL TRANSLATOR 2
FS 1,2,3,4

COIA-9A

PCO PCA STTA

CMTJ1
MTJ1
ETJ

ON LINE TIMER 2
FS 15,16

STJ
JPA
MRF

LAMPS & KEYS PT FS 16,20,29

MTJ2

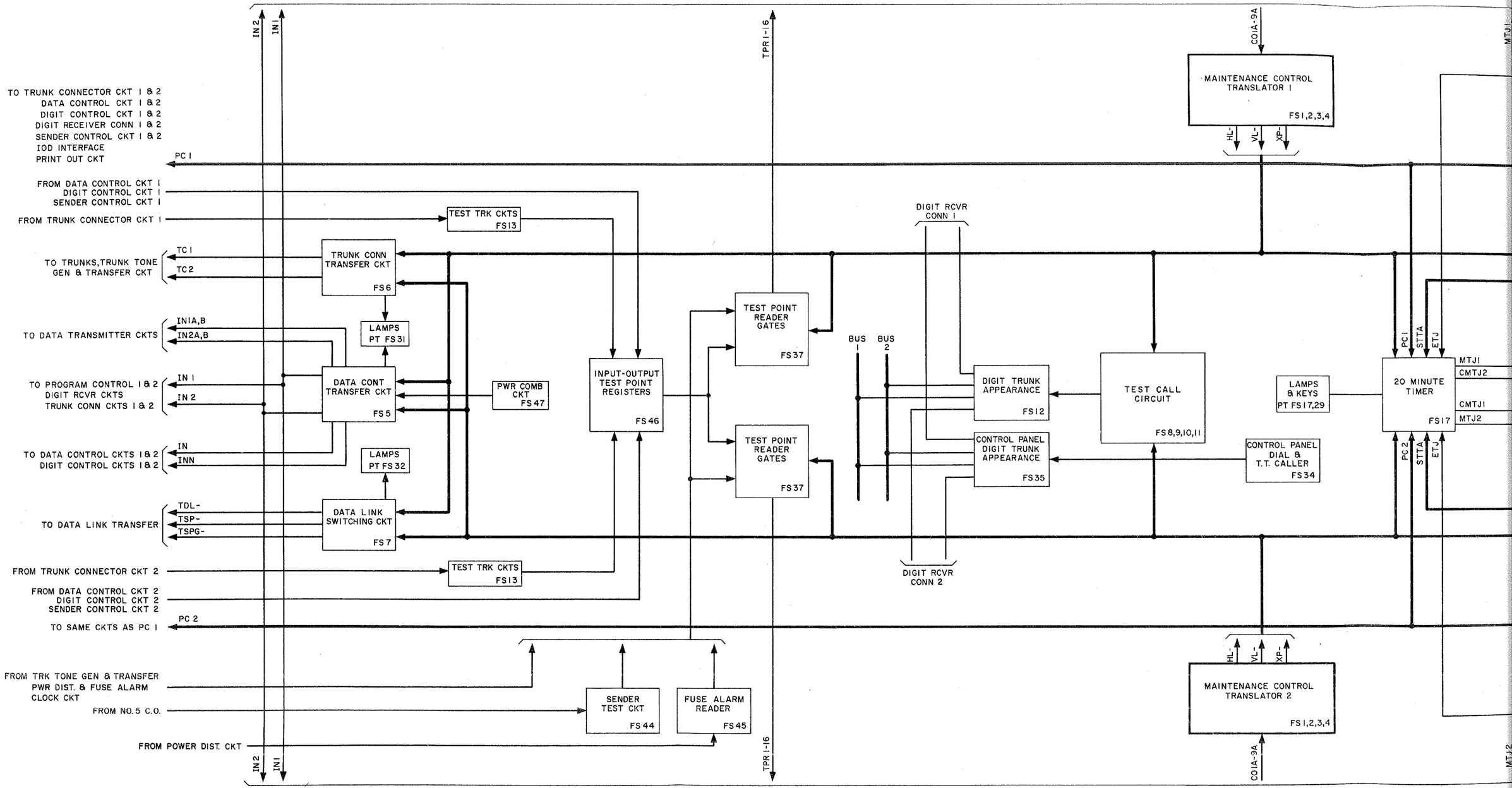
COIA-3A

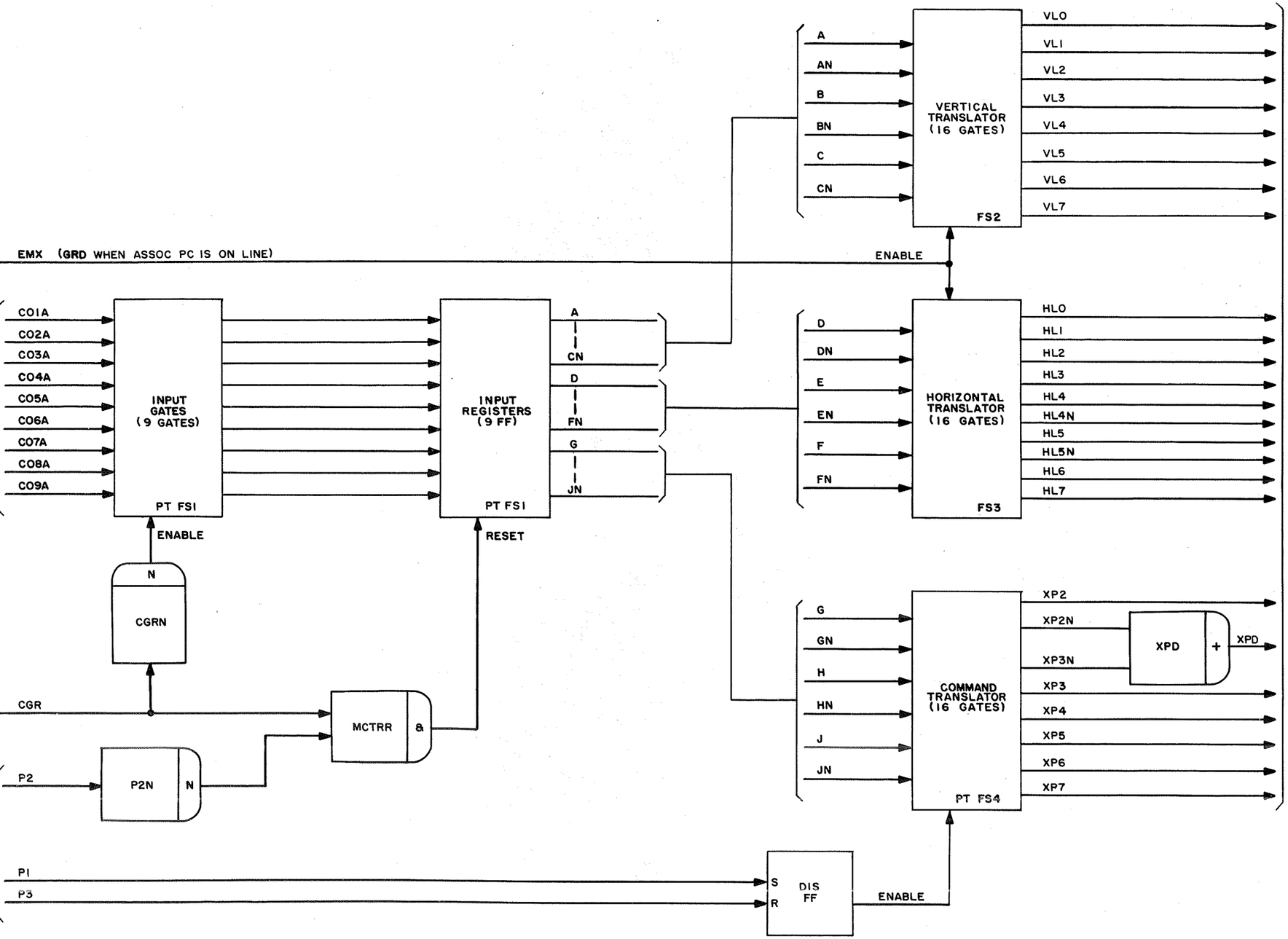
PC

STJ JPA MRF

PA 1-14 MI-22 CCPS MGAR

PROGRAM CONTROL AND PROGRAM SHIFT REGISTER (CO) NO. 2


TO TRUNK CONNECTOR CKT 1 & 2
DATA CONTROL CKT 1 & 2
DIGIT CONTROL CKT 1 & 2
DIGIT RECEIVER CONN 1 & 2
SENDER CONTROL CKT 1 & 2
IOD INTERFACE
PRINT OUT CKT
PC 1
FROM DATA CONTROL CKT 1
DIGIT CONTROL CKT 1
SENDER CONTROL CKT 1
FROM TRUNK CONNECTOR CKT 1
TO TRUNKS, TRUNK TONE GEN & TRANSFER CKT
TC 1
TC 2
TO DATA TRANSMITTER CKTS
IN1A,B
IN2A,B
TO PROGRAM CONTROL 1 & 2
DIGIT RCVR CKTS
TRUNK CONN CKTS 1 & 2
IN 1
IN 2
TO DATA CONTROL CKTS 1 & 2
DIGIT CONTROL CKTS 1 & 2
IN
INN
TO DATA LINK TRANSFER
TDL-
TSP-
TSPG-
FROM TRUNK CONNECTOR CKT 2
FROM DATA CONTROL CKT 2
DIGIT CONTROL CKT 2
SENDER CONTROL CKT 2
PC 2
TO SAME CKTS AS PC 1
FROM TRK TONE GEN & TRANSFER
PWR DIST. & FUSE ALARM
CLOCK CKT
FROM NO. 5 C.O.
FROM POWER DIST. CKT
IN2
IN1
TPR 1-16
TEST TRK CKTS FS13
TRUNK CONN TRANSFER CKT FS6
LAMPS PT FS31
DATA CONT TRANSFER CKT FS5
LAMPS PT FS32
DATA LINK SWITCHING CKT FS7
PWR COMB CKT FS47
INPUT-OUTPUT TEST POINT REGISTERS FS46
TEST POINT READER GATES FS37
TEST POINT READER GATES FS37
SENDER TEST CKT FS44
FUSE ALARM READER FS45
DIGIT RCVR CONN 1
BUS 1
BUS 2
DIGIT TRUNK APPEARANCE FS12
CONTROL PANEL DIGIT TRUNK APPEARANCE FS35
DIGIT RCVR CONN 2
TEST CALL CIRCUIT FS8,9,10,11
CO1A-9A
MAINTENANCE CONTROL TRANSLATOR 1 FS1,2,3,4
HL-
VL-
XP-
LAMPS & KEYS PT FS17,29
CONTROL PANEL DIAL & T.T. CALLER FS34
20 MINUTE TIMER FS17
MTJ1
CMTJ2
CMTJ1
MTJ2
PC1
STTA
ETJ
PC2
STTA
ETJ
HL-
VL-
XP-
MAINTENANCE CONTROL TRANSLATOR 2 FS1,2,3,4
CO1A-9A
MTJ2



TO DATA CONTROL TRANSFER CKT
TRUNK CONNECTOR TRANSFER CKT
DATA LINK TRANSMITTER AND RECEIVER SWITCHING CONTROL
DIAL PULSE GENERATOR
TWENTY MINUTE TIMER
ALARM CKTS
TEST POINT READER

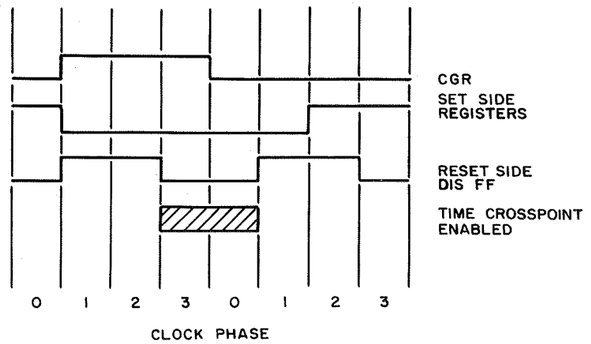
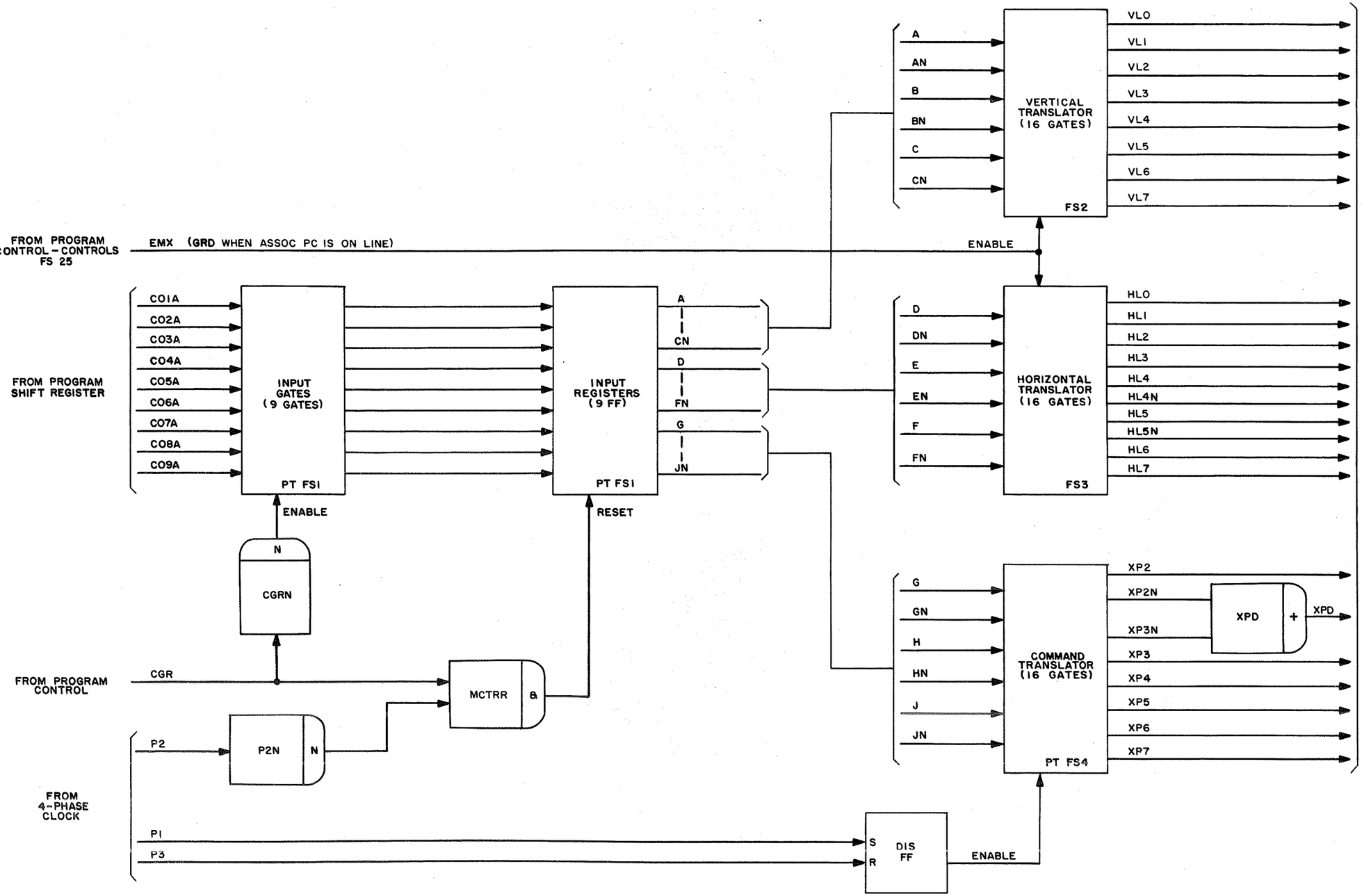


Fig. 2 – Maintenance Control Translator



TO DATA CONTROL TRANSFER CKT
TRUNK CONNECTOR TRANSFER CKT
DATA LINK TRANSMITTER AND RECEIVER SV
DIAL PULSE GENERATOR
TWENTY MINUTE TIMER
ALARM CKTS
TEST POINT READER

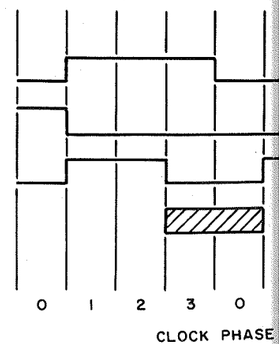


Fig. 2 -

groups, the inputs from the program shift register can identify a cross point in a 512-point (8 by 8 by 8) matrix. However, only 264 cross points are utilized in this system.

Setting the Input Register

2.12 A positive pulse on the CGR lead (CGT COXMCT command) enables the input gates of the translator and sets the contents of the program shift register in the flip-flops of the input registers. When these flip-flops are set, the gates in the horizontal and vertical translators are enabled and the command translator is partially enabled. When the enabling pulse (P3 to P1) is generated, the command is passed to the rest of the maintenance center. The positive CGR pulse also disables the MCTRR gate, preventing the P2 clock pulse from resetting the input registers during the translation.

Enabling the Translator Gates

2.13 A gate in the vertical and horizontal translator is enabled by the setting of the flip-flops in the input registers (clock phase 1); however, the enabling of the command translator is delayed until clock phase 3 to assure that no transient voltages exist in the input registers which would cause erroneous commands to the maintenance center. The outputs of the horizontal and vertical translators are not effective until the command translator is enabled.

2.14 In the command translator, clock pulse P1 sets the disable (DIS) flip-flop which disables the translator gates until the flip-flop is reset at P3. The resetting of the flip-flop at P3 generates the enabling pulse to the command translator supplying the third signal necessary to identify the correct cross point in the matrix. The 2-μsec time interval, P1 to P3, permits any transients to pass before the gates are enabled. The translator registers are then reset at the next P2. Ground potential on the enable maintenance translator (EMX) lead comes from the program control controls and permits only the translator associated with the active program control to pass commands.

Special Signal for the Test Call Circuit

2.15 In checking circuits the equipment makes test calls (see C. Test Call Circuit below) in which TOUCH-TONE (a multifrequency code using 2 of 8 frequencies) or dial pulse digits are generated. When test calls are being made, a positive voltage on the XP2 lead identifies a multifrequency digit, while a positive voltage on the XP3 lead identifies a dial pulse digit. Certain portions of the test call circuit are used when either type digit is to be dialed and are enabled by the XPD voltage. The XPD voltage is present when a voltage exists on either XP2 or XP3.

C. Test Call Circuit

General

2.16 The test call circuit (Fig. 3) simulates the different signals to which the digit receiver must respond. It receives its input signals from the maintenance control translator. The circuit is used to test the digit receivers, digit receiver connectors, and digit controls.

Specifying the Digit Dialed

2.17 The information for setting up the digit to be dialed comes to the test call circuit from the maintenance control translator. Digits 1 through 10 may be either dial pulse or multifrequency (TOUCH-TONE) digits, while digits 11 through 16 are multifrequency digits. These numbers are set up by the dial digit gates.

2.18 The information coming from the maintenance control translator is divided into three groups. The leads VL0 through VL7 and HL4 or HL5 serve to identify the digit to be dialed. HL4 specifies that the digit is 1 through 8 and HL5, 9 through 16. The VL lead specifies the particular digit within the group of digits identified by the HL lead. Lead XP2 identifies a TOUCH-TONE digit and XP3 a dial pulse digit. A signal appears on XPD whenever a signal is present on XP2 or XP3. A signal appearing on leads VL0, HL4, and XP3 identifies the digit as being the dial pulse digit 1. A signal on leads VL0, HL5, and XP2 identifies the digit as being the TOUCH-TONE digit 9.

2.19 The VL, HL, and XPD leads enable the dial digit gates whenever a digit is to be dialed. These gates set the digit in both the pulse counter and the frequency selector.

Setting the Pulse Counter

2.20 The pulse counter consists of four binary stages which have a natural count of 16. When a number is set into the counter, the counter is set to 16 minus that number. This means that when the number of pulses corresponding to the desired digit have been generated, the counters will be in their zero state.

Specifying Multifrequency Digits

2.21 The decision must now be made as to whether the digit is a dial pulse or a multifrequency pulse. ***And*** gates, MFPG-, and DPSG- will be partially enabled by the output of ***or*** gate DPIG. (The particular gates operated will depend on whether program control 1 or 2 is on line.) The enabling of the particular gate, MFPG or DPSG, will be completed by a ground appearing on lead XP2 or XP3.

2.22 If a multifrequency digit is to be dialed, a ground potential appears on lead XP2, enabling the gate MFPG- which triggers monopulser MFPS. The output of MFPS goes through two inverters, to the pulse counter and the MVI gate.

2.23 The period of monopulser MFPS is longer than the period during which the output of the dial digit gates is positive. The longer time interval permits the monopulser to set the pulse counter for one pulse. (While the dial digit gates were enabled, the pulse counter was set for the number of pulses corresponding to the digit.)

2.24 A positive voltage applied to any input of MVI prevents oscillation of the astable multivibrator. One of the leads from the CHL- gates will be positive during gating of the dial digit inputs, and the MFPSG or DPS lead will be positive until the digit conditions are completely set. The positive voltage from one of the CHL- gates keeps the FSFFR ***and*** gate disabled, preventing the possibility of disturbing the pair of frequencies which have been selected.

Specifying Dial Pulse Digits

2.25 If a dial pulse digit is to be dialed, ground potential appears on lead XP3 enabling gate DPSG- which triggers monopulser DPS. The output of DPS goes through two inverters and then to the frequency selector and the MVI gate.

2.26 The period of monopulser DPS is longer than the period during which the output of the dial digit gates is positive. The longer time interval permits the monopulser to set the pair of flip-flops in the frequency selector which are used for a dial pulse digit, and to reset the pair of flip-flops which corresponded to the digit which was indicated by the dial digit gates. (While the dial digit gates were enabled, voltages were present to set both pairs of flip-flops.)

2.27 The positive voltages appearing at MVI and FSFFR perform the same function as for a multifrequency digit.

Pulsing the Digit

2.28 When the digit has been translated (all CHL- gate outputs at ground) and the DPS monopulser period is over (DPS inverter output at ground), MVI enables the astable multivibrator. The multivibrator breaks into oscillation enabling the relay drivers which were partially enabled by the flip-flops in the frequency selector. The relays activated by these drivers tune the multifrequency oscillator.

2.29 The complementary output of the astable multivibrator goes through two inverters, which put it in the same phase as the output which enabled the relay drivers. This pulse activates a relay which turns on the multifrequency oscillator and sends a burst of multifrequency tone to the digit trunk appearance.

2.30 Each time the relays are activated, a positive pulse goes to the pulse counter stepping the binary counters once. When the binary counters reach their zero state, the zero detector gate produces a positive output which goes to the MVI gate, halting further oscillation of the astable multivibrator. The positive output of the zero detector gate is also inverted to enable ***and*** gate FSFFR which resets the flip-flops in the frequency selector.

D. On-Line Off-Line Transfer Controls

General

2.31 The on-line off-line transfer controls (Fig. 4) administer the redundancy which is designed into the control unit. The placing of circuits in on-line and off-line status is done in response to instructions from the maintenance programs.

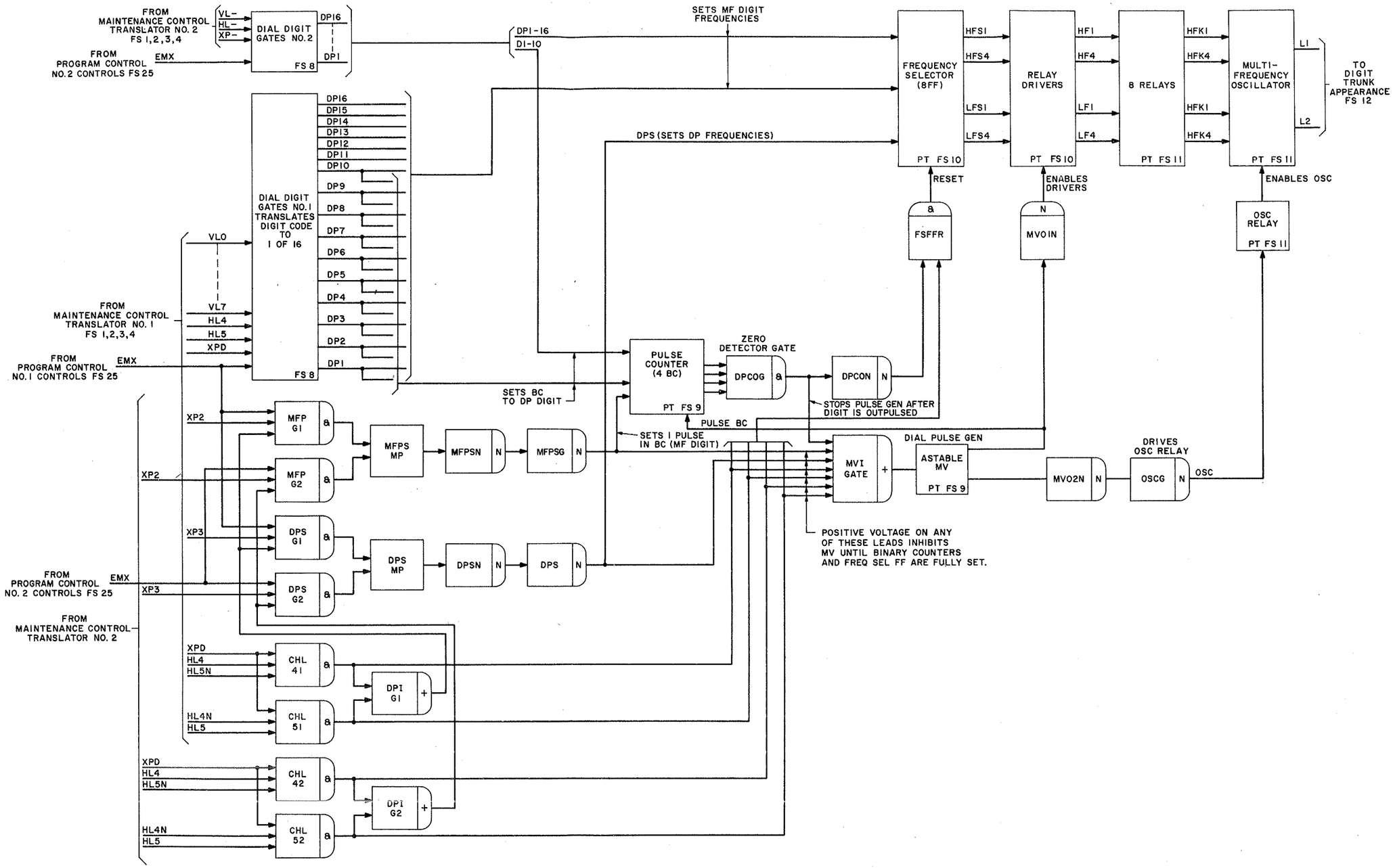


Fig. 3 – Test Call Circuit

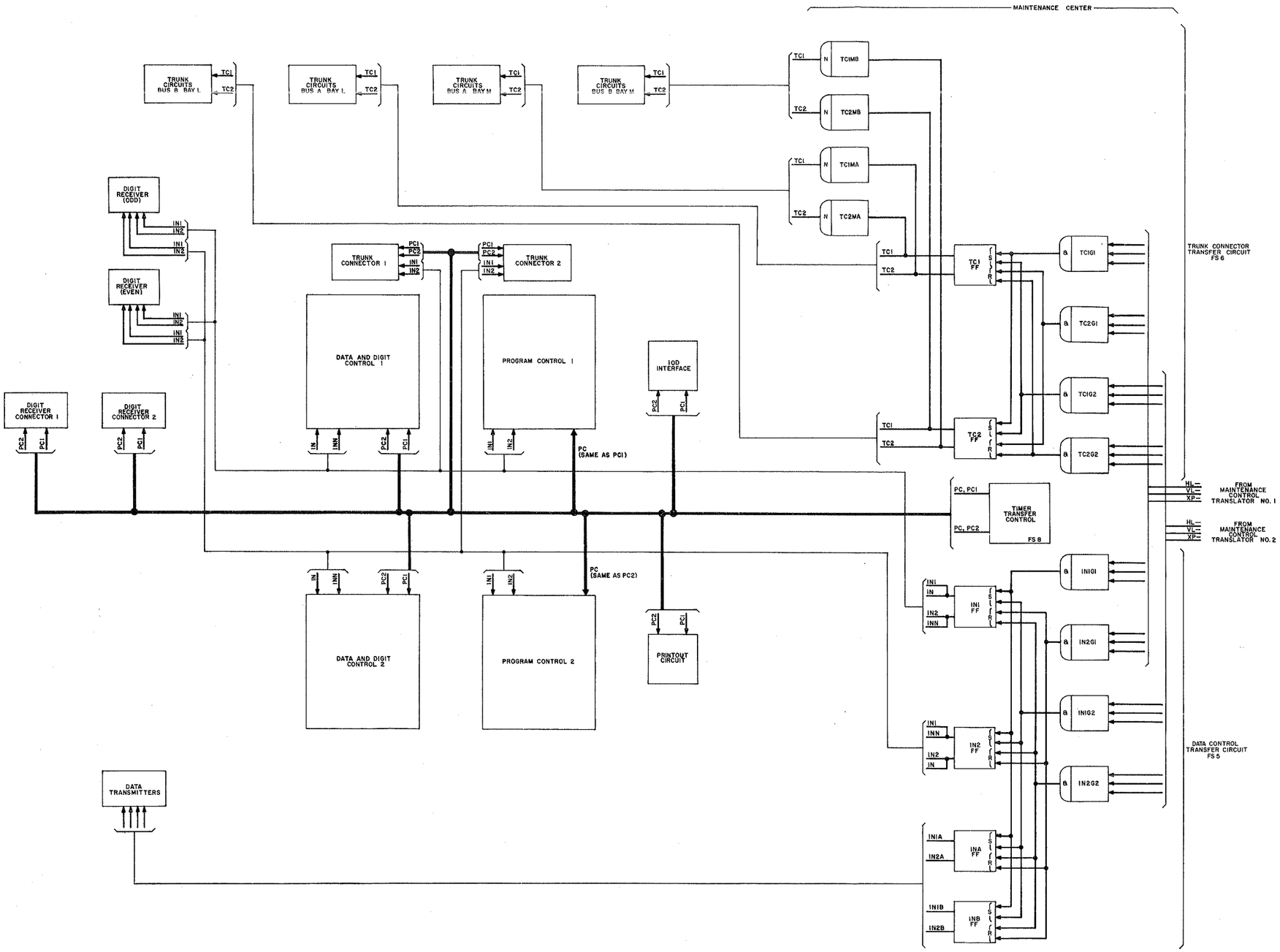


Fig. 4 – On-Line Off-Line Control Transfer Controls

2.32 The instructions of the maintenance program are translated in the maintenance control translator which sends the signals to the on-line off-line transfer control. The signals result in the setting or resetting of flip-flops which place the circuits in their desired status. In all cases ground potential on the IN- and TC- leads enables the circuits which they control.

Data Control Transfer Circuit

2.33 Four flip-flops are used to administer the data control transfer circuits. Two flip-flops, IN1 and IN2, are used to control the status of the program controls, data and digit controls, trunk connectors, and digit receiver connectors. The remaining flip-flops, INA and INB, control the data transmitters.

2.34 The circuits which are controlled by the flip-flops IN1 and INA are those receiving their power from bus A, and flip-flops IN2 and INB control those which receive their power from bus B. This arrangement assures that there will always be a full complement of circuits able to supply call processing functions and receive correlated IN signals.

Trunk Connector Transfer Circuit

2.35 Two flip-flops control the activity of the trunk circuits. The trunk connector control No. 1 (TC1) flip-flop controls the trunk circuits which are powered from the bus A, and TC2 controls those which are powered from bus B. These flip-flops receive their power from the buses which supply power to the trunk circuits they control. This assures that properly correlated TC signals will be available in the case of failure within the control unit. The four inverters, TC1MA, TC2MA, TC1MB, and TC2MB, provide the necessary fan out to power the trunk circuits.

Conjunctive Functions of the Timer Transfer Control

2.36 The timer transfer control, which will be described subsequently, controls the status of the digit receiver connectors, trunk connectors, sender controls, data controls, and digit controls in the data and digit controls and program controls. In addition, it enables the identified outward dialing (IOD) interface and print-out circuit to operate with the on-line program control. In the case of the trunk connectors, data controls, digit controls, and program controls, it permits operation of all possible combinations of these circuits.

2.37 For example, program control 1 can operate with data control 2, digit control 2, and trunk connector 2. The particular combination on line is selected by the maintenance program.

E. Data Link and Transmitter and Receiver Switching Control

General

2.38 There is one of these controls for each switch unit in the switching system. Its function is to switch the spare data link and the spare transmitter and receiver in and out of on-line status. These controls operate in response to instructions from the maintenance program.

Circuit Operation

2.39 The circuit is similar to the trunk connector transfer circuit (Fig. 4). However, there are two minor differences. A relay driver appears on the reset side of each of the two flip-flops rather than having the inverters on both sides. Each flip-flop is set and reset independently of the other, and four input ***and*** gates are needed for each flip-flop to accomplish this, two from each maintenance control translator.

2.40 The relays when operated by setting the flip-flop, place an enabling ground on the spare circuits.

F. Test Point Reader

General

2.41 The test point reader (Fig. 5) is equipped to read four 16-bit words, each of which is represented by a cross point in the maintenance control translator matrix. These words, when read on command of the program control, are gated to the call store output register. The contents of the CO are then entered in the maintenance record areas of the call store keeping the system's status current.

Grouping of Test Points

2.42 Three groups of 16 test points are significant regardless of which program control is on line. Two of these groups are used to

detect power failures within the switch units, and the third group monitors the sender test circuit, power distribution and fuse alarm, clock circuit, and tone generator alarm.

2.43 The fourth group is identified with the on-line program control. This group monitors test points in the data control, digit control, sender control, and trunk connector circuits. ***And*** gate PCOL provides an output in bit 1 of this word when program control 2 is on line. Program control 1 is identified by the absence of a bit, and PCOL does not appear in its associated circuit.

Reading the Test Points

2.44 Clock phase P3 provides the positive pulse to reset the input flip-flops, RTP1 through 4. Almost coincidentally the command translators enable one of the input ***and*** gates. (Assume in this discussion that RTPG1 is enabled.)

2.45 ***And*** gate RTPG1 is enabled during clock phases P3 and P0 applying a setting pulse to flip-flops RTP1 and TPR1. Setting TPR1 disables the output gates. Clock phase P3 applies a resetting pulse to the flip-flops RTP1 through 4. Whether or not flip-flop RTP1 is set during P3 is not important since the function of P3 is to reset one of the other flip-flops which was previously set. During clock phase PO flip-flop RTP1 is set. Clock phase P0 is inverted and, together with the ground from the set side of TPR1, enables ***and*** gate RCSSM. RCSSM, when enabled, generates a positive pulse which resets the CO in the on-line program control.

2.46 The ground potential appearing on the set side of flip-flop RTP1 enables the test point group gates, gating the contents of the test points through the combining ***or*** gates to the output gate. Clock phase P1 then resets flip-flop TPR1, placing a ground potential on lead TPR and enabling the output gates. This action gates the contents of the test points to the CO. The enabled test point group gates are disabled at P3 when RTP1 is reset.

Additional Timing Sequence in Reading Input-Output Test Points

2.47 The input-output test point gates are enabled by the setting of flip-flop RTP2. The sequence of events in the reading of these test points is the same as described above. However, there is an additional timing sequence connected with the presenting of the test point information to the input of the gates.

2.48 During clock phase PO when RTP2 is set, the ground appearing on the set side is inverted by gate RTPN-. The output of RTPN- sets flip-flop IOR and disables ***and*** gate IORG. At P3 the output of RTPN falls to ground, enabling the IORG and resetting the input registers. During the next P0, IOR is reset to disable IORG. The test point information is then stored in the input registers until it is read again.

G. Program Store Comparator

General

2.49 The program store comparator (Fig. 6) is used to compare every word in the program stores. When the comparison cycle is completed, a lamp on the input-output panel of the maintenance center is lighted to indicate whether or not the contents of the stores match.

2.50 There are two modes of operation. One mode is to interrupt call processing and to cycle completely through the two stores, comparing every word. When the cycle is completed, the program control which was taken off line to execute the cycle is returned to on-line status. This cycle is repeated every 2 seconds as long as the program comparator is turned on.

2.51 The second mode of operation is to repeat the comparison cycle every 2 seconds until a mismatch is detected. If this occurs, the off-line program control is stopped at the point of the mismatch and the other program control is returned to on-line status.

Initiation of Comparison Cycle

2.52 The program store comparator is turned on manually by the ON-OFF switch on the input-output panel. Operation of the switch to ON applies a positive voltage to ***or*** gates IPSCD, IPSC2, ONA, and ONB, turning them on and enabling a 2-second timing circuit and the circuit which generates the JPA pulses.

2.53 Two seconds after the comparator is turned on, the 2-second timer (2ST) produces a positive pulse which results in the setting of flip-flop CPE. The ground potential appearing

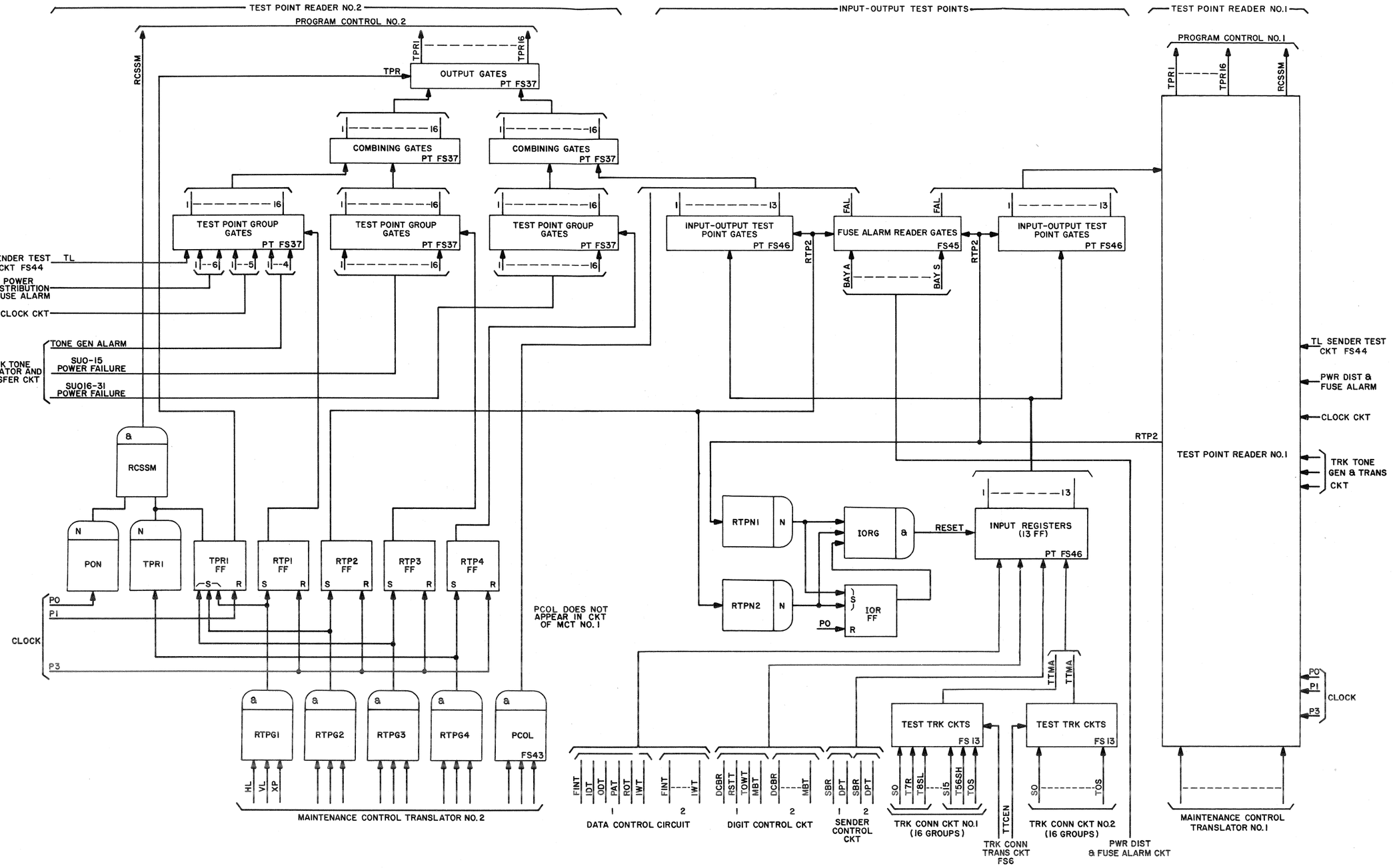


Fig. 5 – Test Point Reader

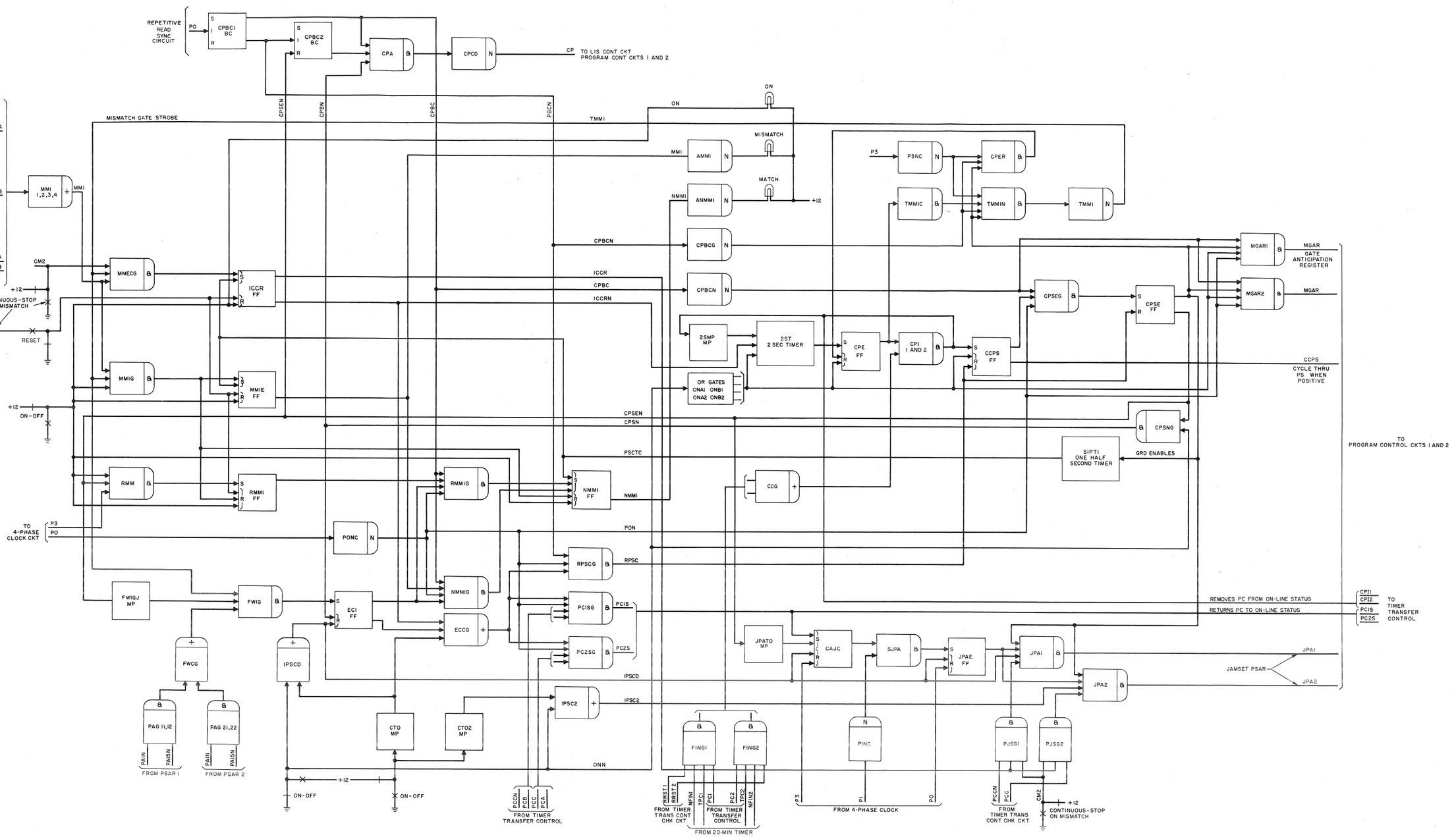
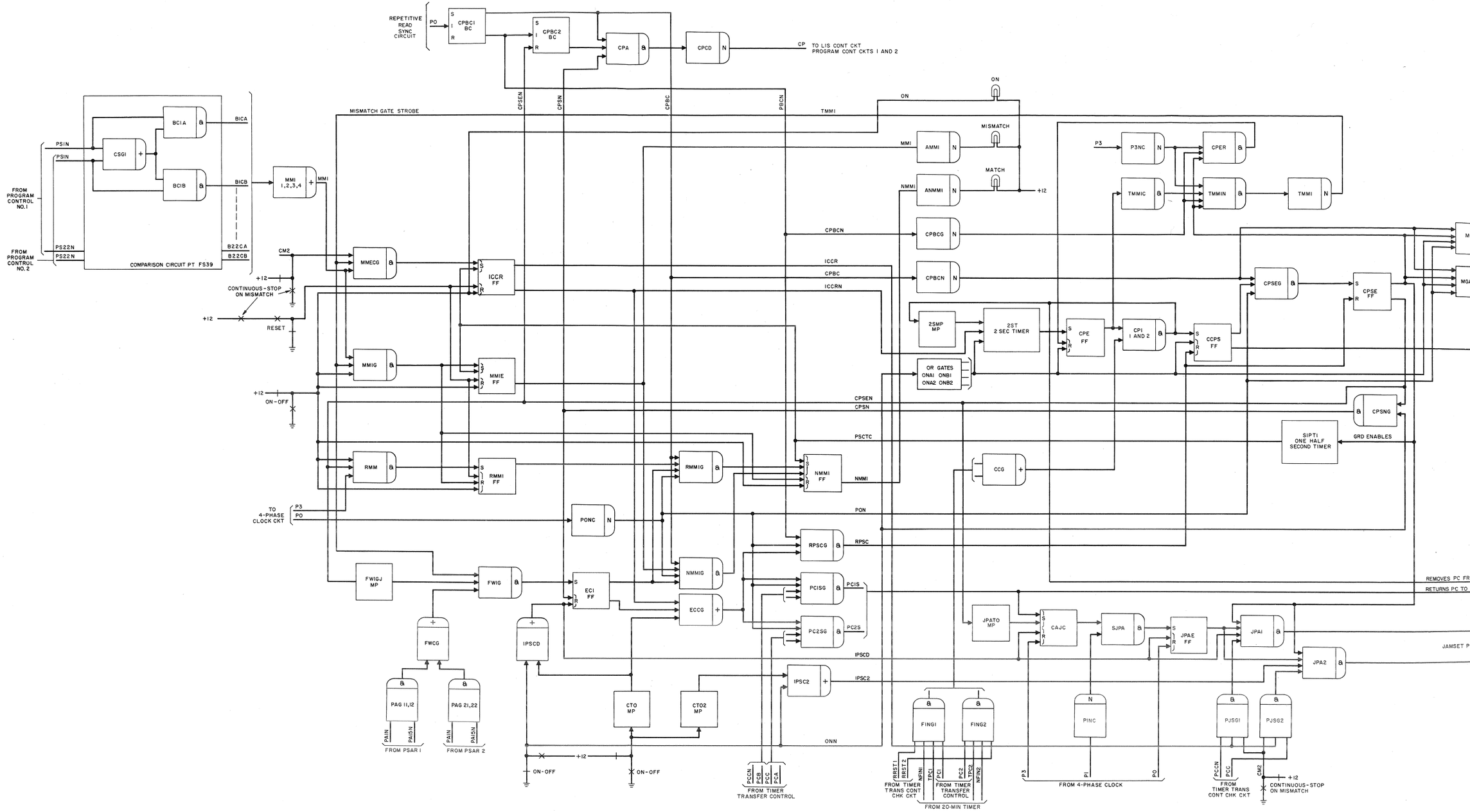


Fig. 6 – Program Store Comparator


REPETITIVE READ SYNC CIRCUIT
PO
CPBC1 BC
CPBC2 BC
CPA
CPCD
CP
TO LIS CONT CKT
PROGRAM CONT CKTS 1 AND 2
MISMATCH GATE STROBE
CPSEN
CPSN
CPBC
PBCN
TMMI
ON
MISMATCH
MATCH
MMI
NMMI
AMMI
ANMMI
+12
P3
P3NC
CPER
TMMIC
TMMIN
TMMI
BC1A
BC1B
CSGI
PSIN
BICA
BICB
MMI 1,2,3,4
FROM PROGRAM CONTROL NO.1
FROM PROGRAM CONTROL NO. 2
PS22N
B22CA
B22CB
COMPARISON CIRCUIT PT FS39
CM2
MMECG
ICCR FF
CONTINUOUS-STOP ON MISMATCH
RESET
CPBCN
CPBCG
CPBCN
ICCR
CPBC
ICCRN
CPSEG
CPSE FF
2SMP MP
2ST 2 SEC TIMER
CPE FF
CPI 1 AND 2
CCPS FF
OR GATES ONA1 ONB1 ONA2 ONB2
MMIG
MMIE FF
CPSEN
CPSN
CPSNG
PSCTC
SIPTI ONE HALF SECOND TIMER
GRD ENABLES
RMM
RMMI FF
RMMIG
NMMI FF
NMMI
CCG
TO 4-PHASE CLOCK CKT
P3
PO
PONC
PON
RPSCG
RPSC
FWIGJ MP
FWIG
NMMIG
ECI FF
PCISG
PCIS
REMOVES PC FROM
RETURNS PC TO ON
ECCG
PC2SG
PC2S
JPATO MP
CAJC
SJPA
JPAE FF
JPAI
JPA2
JAMSET PSAR
FWCG
IPSCD
IPSCD
IPSC2
IPSC2
PAG 11,12
PAG 21,22
PAIN
PAIDN
FROM PSAR 1
FROM PSAR 2
CTO MP
CTO2 MP
ONN
FING1
FING2
PINC
PJSG1
PJSG2
ON-OFF
+12
ON-OFF
PCCN
PCCB
PCCC
PCCA
FROM TIMER TRANSFER CONTROL
RRST1
RRST2
NFIN
TPC1
PC1
PC2
TPC2
NFIN2
FROM TIMER TRANS CONT CHK CKT
FROM TIMER TRANSFER CONTROL
FROM 20-MIN TIMER
P3
P1
P0
FROM 4-PHASE CLOCK
PCCN
PCCC
FROM TIMER TRANS CONT CHK CKT
CM2
+12
CONTINUOUS-STOP ON MISMATCH

on the set side of CPE partially enables two ***and*** gates CPI1 and 2. Gates CPI1 and 2 remain partially enabled until the active program generates the end program scan (FIN) command signifying the end of the sector scan. The CPI1 and 2 pulses are then generated which go to the timer transfer control where they force both program controls into off-line status for the duration of the comparison cycle.

Setting the Program Store Reading Rate

2.54 In addition the CPI pulses set the flip-flop CCPS which partially enables ***and*** gate CPSEG. CPSEG is then enabled by clock pulse P0. The reset side of CCPS remains at positive potential during the comparison cycle and permits the cycling through of the program store. The output of CPSEG sets the flip-flop CPSE. The ground potential appearing on the set side of CPSE partially enables the two output gates JPA1 and 2. The positive voltage on the reset side triggers monopulser JPAT0. JPAT0 generates a positive pulse which is inverted and delayed until the next clock phase P1 at which time the JPAE flip-flop is set, enabling gates JPA1 and 2. These gates produce positive output pulses which go to program controls 1 and 2 where they jam set both PSARs to the address of octal 200.

2.55 The reset side of flip-flop CPSE, the setting of which is described above, also goes to the repetitive read sync circuit where it holds the binary counter CPBC2 in its reset state. It also goes to ***and*** gate CPSNG to hold its output at ground potential, partially enabling ***and*** gate CPA.

2.56 The input element of the repetitive read sync circuit is binary counter CPBC1 which is driven by clock pulse P0. The set side of CPBC1 is connected to ***and*** gate CPA and enables CPA on alternate P0 pulses, generating the pulses, CP, which read the program store once every 8 μsec.

Comparing the Program Store Contents

2.57 In the comparison circuit each bit of one PSOR is compared with the corresponding bit in the other PSOR. If corresponding bits are alike, the output of each of the 22 stages will be at ground potential. If each bit does not compare, the output of at least one of the stages will be positive. One positive output is sufficient to turn on ***or*** gate MMI, partially enabling ***and*** gate MMECG.

2.58 MMECG will be enabled by pulse TMMI if a mismatch has been detected. The TMMI pulse occurs 3 μsec after the next CP pulse is generated. This delay is to insure that the contents of the anticipation register have settled in the PSOR and that there are no transient voltages which might cause an erroneous comparison.

Reading the Program Store

2.59 When binary counter CPBC1 is in its set state, a negative CP pulse of 4-μsec duration is produced by the repetitive read sync circuit which adds one to the contents of the PSARs. The contents of the program store are in the anticipation register until CPBC1 is put in its reset state by the next P0 pulse.

2.60 The output of the set side of CPBC1 becomes positive and is inverted by gate CPBCN to enable the MGAR- ***and*** gates. The MGAR pulse gates the contents of the anticipation register to the PSORs.

2.61 The next P0 pulse returns the binary counter to its set state generating another CP pulse. The reset side becomes positive and is inverted by gate CPBCG to partially enable ***and*** gate CPER. Clock pulse P3 then enables TMMIN producing pulse TMMI which enables ***and*** gates MMECG and MMIG if a mismatch in the program stores has been detected. This process continues until the cycling through the program store is completed.

Normal Termination of Comparison Cycle

2.62 If the comparison mode is continuous or if no mismatch has been detected, the comparison cycle will continue until the PSARs of the program stores have returned to the starting address of octal 200. Actually it is only necessary for one PSAR to return to the starting address.

2.63 At this point PAG- ***and*** gates cause the FWIG ***and*** gate to produce an output setting flip-flop ECI. The reset side of ECI goes through inverter ECCG to ***and*** gates RPSCG,

PC1SG, and PC2SG. Gate RPSCG is enabled by the clock pulse P0 which is generated when binary counter CPBC1 is reset. The output of RPSCG resets flip-flops CCPS and CPSE which were set to initiate the comparison cycle.

2.64 One of the gates, PC1SG or PC2SG, is partially enabled by a PC- lead from the timer transfer control. The partially enabled gate will be enabled by the same clock phase P0 which enabled gate RPSCG, producing a positive pulse. The positive pulse returns the program control which was on line before the test to on-line status.

Termination of Comparison Cycle on Mismatch

2.65 When the comparator is in the stop or mismatch mode and ***or*** gate MMI is turned on, indicating a mismatch in the word being compared, pulse TMMI enables ***and*** gate MMECG which sets flip-flop ICCR. The set side of ICCR goes to gates PJSG1 and PJSG2 to partially enable one of these gates. The PCC lead indicates the program control which was on line prior to the comparison cycle. The PJSG gate which is enabled generates a JPA pulse to the program control which is to be returned to on-line status. The reset side of ICCR goes to the 2-second timer disabling this timer. The TMMI pulse also turns on ***and*** gate FWIG which sets flip-flop ECI and turns on the proper program control as previously described.

Indication of Match or Mismatch

2.66 When the comparison cycle is initiated, ***and*** gate RMM is enabled by the ON-OFF key, the resetting of flip-flop CPSE, and any clock phase other than P3. RMM sets flip-flop RMMI which partially enables ***and*** gate RMMIG. RMMIG is enabled by the set sides of CPBC1 and ECI and the clock phase P0 to set flip-flop NMMI. The reset side of NMMI goes through an inverter to turn on the MATCH lamp. The MATCH lamp remains turned on until a mismatch condition turns it off.

2.67 ***And*** gate MMIG is partially enabled by the ON-OFF key and the output of ***or*** gate MMI if a mismatch has been detected. Pulse TMMI then enables this gate, setting flip-flop MMIE. The positive voltage on the reset side of MMIE controls inverter to turn on the MISMATCH lamp.

2.68 The reset side of MMIE also goes to ***and*** gate NMMIG which removes the positive output to the set side of flip-flop NMMI. At the same time, the positive output of MMIG resets flip-flop NMMI placing ground potential on inverter ANMMI to turn off the MATCH lamp.

Special Features

2.69 When the comparison cycle is initiated, the positive voltage appearing on the reset side of flip-flop CPSE triggers monopulser FWIGJ. The positive output of FWIGJ disables ***and*** gate FWIG whose function is to end the comparison cycle when the address in the PSARs returns to the starting address. If FWIG were not disabled, the comparison cycle could not be started.

2.70 The CT0 monopulsers produce a positive pulse when the comparator is turned off. This pulse generates JPA pulses which return the program stores to the starting address. This is a precaution to guard against the interruption of a comparison cycle at a point when the stores were not at the proper address. A PC1S or PC2S pulse is also generated which returns the proper program control to on-line status.

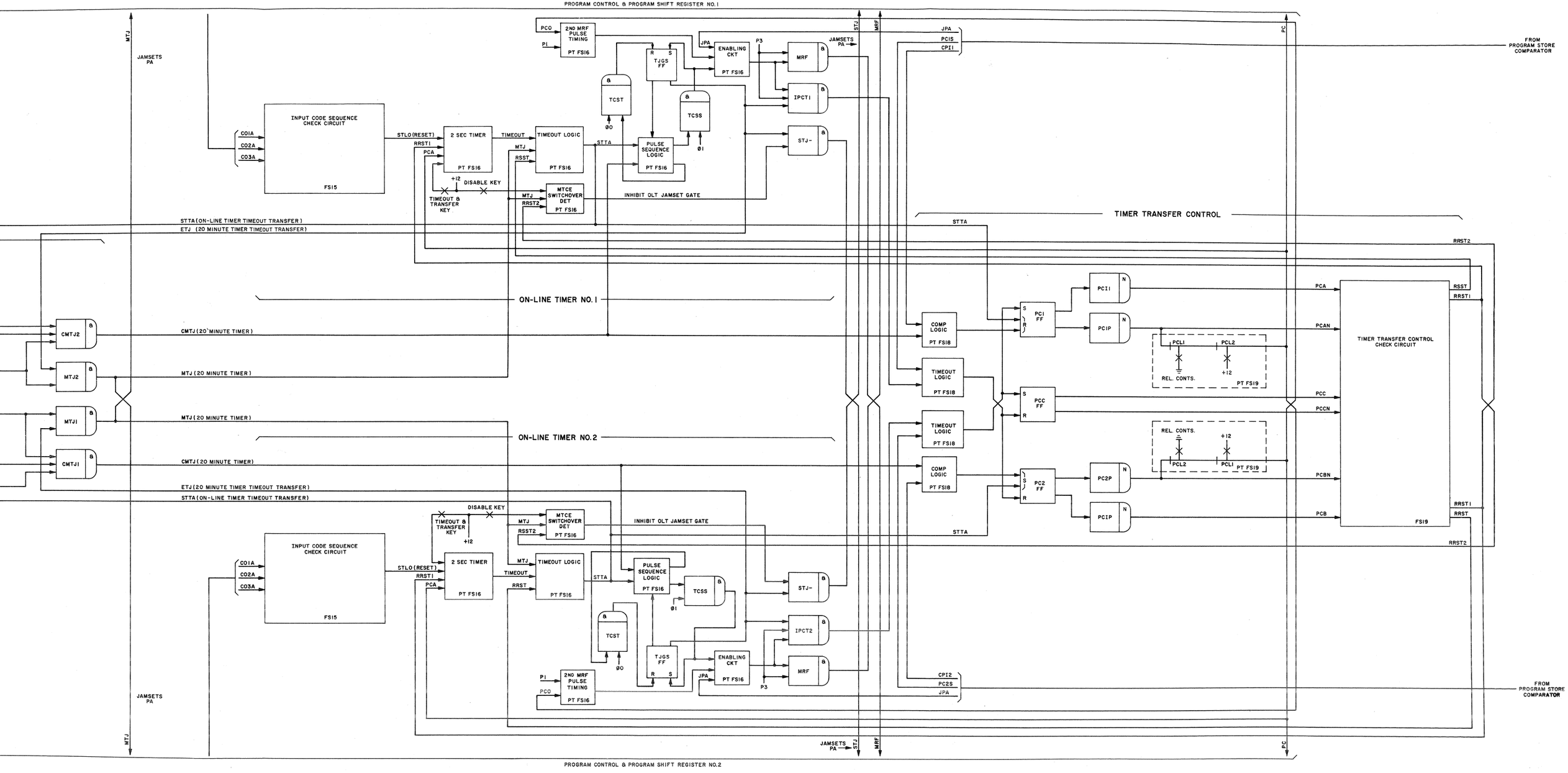
2.71 SIPT1 is a 1/2-second timer which guards against the possibility of both program controls not returning to the starting address. The output of this timer turns on the MATCH and the MISMATCH lamps and returns the proper program to on-line status.

H. Timers and Transfer Control

General

2.72 This portion of the maintenance center is comprised of three distinct types of circuits. There are two on-line timers, one 20-minute timer, and one timer transfer control (Fig. 7).

2.73 The function of the on-line timers is to indicate that the on-line program control has successfully completed a sector scan. When a sector scan has been completed, the 2-second timer within the on-line timer is reset by the STL0 pulse. As long as call processing is pro-



PROGRAM CONTROL & PROGRAM SHIFT REGISTER NO.2

Fig. 7 – Timers and Transfer Control

PROGRAM CONTROL & PROGRAM SHIFT REGISTER NO.1

FINN

END OF SECTOR SCAN

MTJ

JAMSETS PA

INPUT CODE SEQUENCE CHECK CIRCUIT

FSI5

CO1A

CO2A

CO3A

STLO(RESET)

RRST1

PCA

2 SEC TIMER

PT FSI6

TIMEOUT

TIMEOUT LOGIC

PT FSI6

MTJ

RSST

STTA

PULSE SEQUENCE LOGIC

PT FSI6

+12

DISABLE KEY

TIMEOUT & TRANSFER KEY

MTCE SWITCHOVER DET

PT FSI6

RRST2

INHIBIT OLT JAMSET GATE

PCO

2ND MRF PULSE TIMING

PT FSI6

PI

JPA

ENABLING CKT

PT FSI6

P3

R S

TJGS FF

TCST

ØO

TCSS

ØI

MRF

IPCT1

STJ-

JAMSETS PA

STJ

MRF

JPA

PCIS

CPI1

STTA(ON-LINE TIMER TIMEOUT TRANSFER)

ETJ (20 MINUTE TIMER TIMEOUT TRANSFER)

STTA

20 MINUTE TIMER

TIMEOUT KEY

+12

20 MIN DISABLE KEY

20 MIN TIMER

PT FSI7

1 ---- 6

20 MIN DETECTOR

PT FSI7

NFIN2

CMTJ2

CMTJ(20 MINUTE TIMER)

ETG2 FF

MTJ2

MTJ(20 MINUTE TIMER)

FROM MAINTENANCE CONTROL TRANSLATOR

HL–

VL–

XP–

INPUT LOGIC

PT FSI7

ETG1 FF

MTJ1

MTJ(20 MINUTE TIMER)

ON-LINE TIMER NO.1

ON-LINE TIMER TIMEOUT LOGIC

PT FSI7

NFIN1

CMTJ1

CMTJ(20 MINUTE TIMER)

ETJ(20 MINUTE TIMER TIMEOUT TRANSFER)

STTA(ON-LINE TIMER TIMEOUT TRANSFER)

ON-LINE TIMER NO.2

COMP LOGIC

PT FSI8

PC1 FF

S J R

TIMEOUT LOGIC

PT FSI8

PCC FF

S R

COMP LOGIC

PT FSI8

PC2 FF

S J R

CPI2

PC2S

JPA

STTA

DISABLE KEY

TIMEOUT & TRANSFER KEY

+12

MTCE SWITCHOVER DET

PT FSI6

INHIBIT OLT JAMSET GATE

MTJ

RSST2

INPUT CODE SEQUENCE CHECK CIRCUIT

FSI5

CO1A

CO2A

CO3A

STLO(RESET)

RRST1

PCA

2 SEC TIMER

PT FSI6

TIMEOUT

TIMEOUT LOGIC

PT FSI6

RRST

STTA

PULSE SEQUENCE LOGIC

PT FSI6

TCSS

ØI

STJ-

TCST

ØO

IPCT2

TJGS FF

R S

ENABLING CKT

PT FSI6

JPA

P3

MRF

PI

2ND MRF PULSE TIMING

PT FSI6

PCO

END OF SECTOR SCAN

FINN

JAMSETS PA

MTJ

JAMSETS PA

STJ

MRF

PROGRAM CONTROL & PROGRAM SHIFT REGISTER NO.2

ceeding normally, the timer should never time out. A time-out in the on-line timer is indicative of troubles within the program control, and causes the standby program control to be switched into on-line status.

2.74 Every 20 minutes call processing is transferred from the on-line program control to the standby program control. The 20-minute timer measures these time intervals, and upon expiration of the time interval, initiates routine transfers of the program controls. The circuit to measure the 20-minute time intervals is an integral part of the 20-minute timer and requires no external signals. However, it can be disabled or timed out prematurely by the program control.

2.75 The timer transfer control contains the circuits that govern which program control is on line. The inputs to this circuit come from the two on-line timers and the 20-minute timer. It also contains circuits which prevent both program controls from being on line or off line at the same time.

Time Measurement in the On-Line Timer

2.76 The two on-line timers, one associated with each program control, measure a 2-second time interval. These timers receive their inputs directly from the program shift register circuit of the call processor. If call processing is proceeding normally, a sector scan is completed in a fraction of the 2-second time interval, and the timer should never time out.

2.77 Three commands are gated to the input code sequence check circuit of the timer during the end of sector portion of the sector scan. If these commands are formed in the correct sequence, it is an indication that the maintenance tests were successful and the 2-second timer will be reset. If the 2-second timer is not reset, an STTA pulse is generated by the time-out logic and results in the change of program controls.

On-Line Timer Time-Out

2.78 Assuming that program control 1 is on line, the time-out logic sends an STTA pulse to pulse sequence logic partially enabling ***and*** gate TCSS which is enabled at clock phase 1. The output of TCSS sets flip-flop TJGS and also goes to the enabling circuit which produces a ground output to ***and*** gates MRF and IPCT. The ground on the set side of TJGS produces an output from ***and*** gate STJ-, and together with the ground output from the enabling circuit permits ***and*** gates MRF and IPCT1 to be enabled during the next clock phase P3. (The output of TJGS is not required to enable gate MRF.) Pulse STTA also goes to the timer transfer control where it resets flip-flop PC1 turning off program control 1.

2.79 When TJGS is set, the positive voltage which appears on the reset side of the flip-flop is sent to the pulse sequence logic. There it results in the disabling of ***and*** gate TCSS and the enabling of ***and*** gate TCST. At clock phase 0, gate TCST is triggered resetting flip-flop TJGS and returning the circuit to its original condition.

2.80 The output pulse of STJ goes to the program control which is to assume call processing where it jam sets the PSAR to octal 100. The MRF pulse goes to program control 2 where it sets the circuit conditions needed to start call processing.

2.81 The IPCT1 pulse goes to the timer transfer control where it causes the PCC and PC2 flip-flops to be reset. The ground output on the reset side of PC2 is inverted PC2P and turns on program control 2. The output of PC2 also goes to on-line timer 1, where it appears as PC0, and results in the generating of a second MRF pulse at the next P1. The second MRF pulse is used to assure that all of the circuits in program control 2 are in the proper state to start call processing.

2.82 The STTA pulse also goes to the on-line timer time-out logic portion of the 20-minute timer where it causes the circuits which initiate a routine switch of program controls to be disabled.

Twenty-Minute Timer

2.83 The 20-minute time interval in the 20-minute timer is measured by a monopulser with a period of 19 seconds which drives a 6-stage binary counter. When all of the binary stages are in their reset condition, a 20-minute detector

comprised of *and* gates produces a positive output. This output sets the ETG1 and 2 flip-flops.

2.84 The set sides of the ETG1 and 2 flip-flops go to the input of CMTJ1 and 2 and MTJ1 and 2 *and* gates. These gates remain inactive until a FIN command is received from the on-line program control. The FIN command indicates the end of a sector scan or a time when program controls can be changed without interrupting call processing. (In the case of a 2-second time-out, the sector scan was not completed, and the FIN command was never generated.)

2.85 Assuming that program control 1 is on line, the FIN command enables *and* gate CMTJ2 producing a positive pulse. This pulse goes to the pulse sequence logic portion of on-line timer 1 where the sequence of events described in conjunction with the 2-second time-out occurs. The pulse for CMTJ2 also goes to the timer transfer control where it causes flip-flop PC1 to be reset in an action similar to that of pulse STTA in the case of a 2-second time-out.

2.86 However, in the case of the 20-minute time-out, the TJGS input to *and* gates IPCT1 and STJ- also goes to the 20-minute timer on lead ETJ where it enables *and* gate MTJ2. Gate MTJ2 had been enabled when flip-flop ETG2 was set.

2.87 The output of MTJ2 goes to the maintenance switchover detector portion of on-line timer 1 where it produces a positive voltage to disable *and* gate STJ-.

2.88 The output of MTJ2 also goes to program control 2 where it jam sets the PSAR to octal 120, the address from which call processing starts when the changeover is routine.

I. Alarm Circuits

General

2.89 The alarm circuit (Fig. 8) provides audible and visual signals to indicate the presence of trouble in the No. 101 ESS. A major alarm is used to indicate that a failure affecting basic telephone service has occurred. A minor alarm indicates that the trouble affects at least one of the switch units.

2.90 A minor alarm is also generated in the event of a time-out of the on-line timer. If the other on-line timer should fail before the original trouble is cleared, a major alarm is sounded.

2.91 Once an alarm is sounded, it must be turned off by a repairman. If the trouble results in the removal of equipment from service, the EQUIP TROUBLE lamp is lighted. The EQUIP TROUBLE lamp can be extinguished only by restoring the equipment to service.

Alarm Resulting from Removing Equipment from Service

2.92 These alarms may be either major or minor. If major, a positive output is produced by *and* gate MAAX1 or MAAX2 depending on whether program control 1 or 2 was on line. If minor, *and* gate MIAX1 or MIAX2 produces the output. The output of each of these gates is multipled to set flip-flop EOSM which, when set, turns on the EQUIP TROUBLE lamp.

2.93 The output of the gates also causes one of the flip-flops, MAAL1, MAAL2, MIAL1, or MIAL2, to be set. The ground potential appearing on the set side of the flip-flop disables the relay driver, releasing one of the relays, MAA1, MAA2, MIA1, or MIA2. The relay, when released, closes a normally closed contact and applies voltage to the audible and visual alarms circuit in the central office.

2.94 The positive voltage, appearing on the reset side of the flip-flop, causes an inverter to turn on the appropriate lamp on the maintenance panel.

Alarm Not Resulting from Removing Equipment from Service

2.95 This is always a minor alarm. The alarm indication is initiated by a positive output from *and* gate MIAN1 or MIAN2. The output of these gates is not multipled to the EOSM flip-flop, but otherwise the operation is the same as that of the MIAX1 or MIAX2 gates described above.

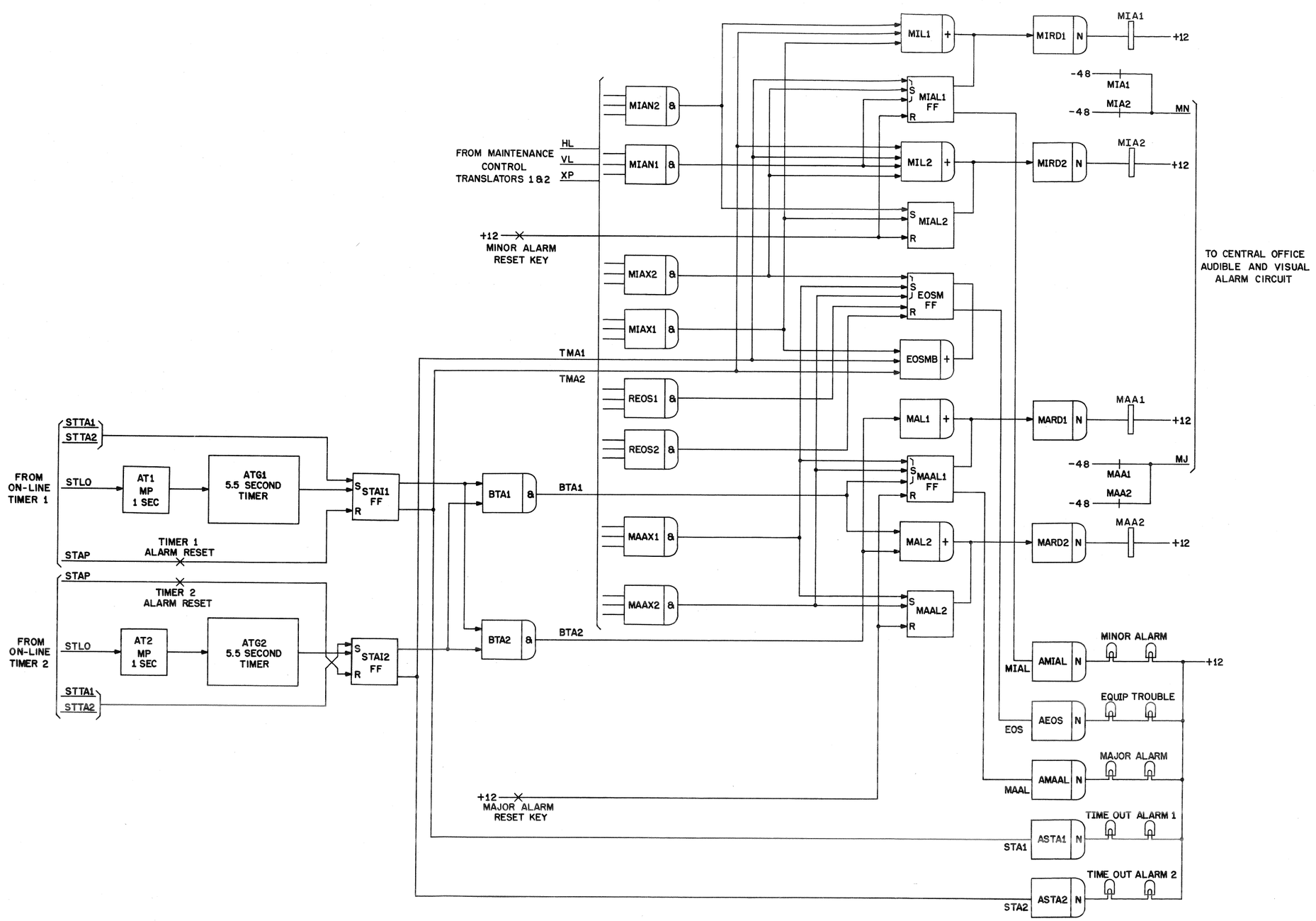


Fig. 8 – Alarm Circuits

Time-Out of the On-Line Timer

2.96 In this discussion assume that on-line timer 1 has timed out. The pulses STAA 1 and 2, generated as a result of this time-out, set flip-flop STAI1. STAI1, when set, partially enables ***and*** gates BTA1 and BTA2. The positive voltage, appearing on the reset side of STAI1, sets flip-flop EOSM by driving its set side output to ground through inverter EOSMB to turn on the EQUIP TROUBLE lamp. The positive voltage also operates gate ASTA1 to turn on TIME OUT ALARM CALL PROC NO. 1 lamp and sets flip-flop MIAL1 to turn on the central office alarms.

2.97 If on-line timer 2 now times out, the STTA1 and 2 pulses set flip-flop STAI2 enabling ***and*** gates BTA1 and BTA2. The outputs from BTA1 and 2 set flip-flops MAAL1 and 2 indicating a major alarm. The positive voltage on the reset side is applied to gate ASTA2 to turn on the TIME OUT ALARM CALL PROC NO. 2 lamp. The MINOR ALARM and EQUIP TROUBLE lamps were turned on previously by the first time-out.

Turning Off Both On-Line Timers

2.98 It is possible to turn off both on-line timers with the keys appearing on the maintenance panel. If this should happen, the on-line timers could not produce the STTA time-out pulse to indicate the fact. Also the STL0 pulses would not be produced. The STL0 pulses prevent the time-out of two 5.5 second timers. The time-out of these timers generates a major alarm as described above.

Terminating the Alarm

2.99 The audible and visual alarms may be turned off by operating RESET keys on the timers and alarm panel in the maintenance center. The EQUIP TROUBLE lamp can be turned off only by action of the maintenance program after the failure has been corrected.

J. Maintenance Center Control Panels

General

2.100 The maintenance center control panels (Fig. 9) contain the keys and lamps with which manual testing of the No. 101 ESS is accomplished. In addition to their use in testing, the lamps also give an indication of which circuits are on line and whether or not any of the circuits are in trouble.

Testing the Off-Line Program Control

2.101 Manual testing must be done in the off-line circuits, and the circuits being tested must be isolated so they can have no effect on call processing. The REMOVE SYSTEM ACCESS TO CALL PROCESSOR key provides this function. Once this key is operated, the operation of the standby program control can be tested by jam setting the PA to the desired address and operating either the ONCE EXECUTE key or the REPETITIVELY EXECUTE key.

2.102 If the ENABLE MAINTENANCE TRANSLATOR key is operated in addition to the REMOVE SYSTEM ACCESS TO CALL PROCESSOR key, the maintenance personnel may switch the redundant circuits on line or off line. This feature provides control in the event of failure in the teletypewriter circuits.

Testing the Off-Line Program Store and Call Stores

2.103 The MARGINAL TEST CALL STORE and MARGINAL TEST PROGRAM STORE keys place the threshold voltage on these stores under control of the potentiometers on the panels. The threshold voltage may then be tested to see if any degradation of the stores has occurred. This test may be conducted only in the off-line stores.

Testing the Line Information Store

2.104 The line information store test procedure is similar to the procedure described above, and the controls used are labeled in an analogous fashion.

State of Repair Registers

2.105 The state of repair registers give a visual indication as to the status of the circuits. The first six lamps are used to indicate the status of the other call processor. The lamps form two groups indicating if the program store (PS), line information store (LIS), and call store (CS) are out of service and out of order. If a trouble exists, the lamps indicating both states will be lighted. However, it is possible by use of the tele-

typewriter or manual switches to place the program control out of service when it is not out of order. For this reason both lamps are used. The seventh lamp is used to indicate when a requested test has failed, and the sixteenth lamp is used to indicate that a retry of tests is in process. The eighth lamp indicates a digit receiver connector has been removed from service. Lamps 9 and 10 indicate the relative status of data control 1, and lamps 11 and 12 indicate the relative status of data control 2. If both lamps associated with a data control are out, there is no failure. If the right lamp is on, there is a trivial failure, the left lamp a major failure, and both lamps a catastrophic failure. Lamps 13 and 14 indicate the condition of the trunk connectors. If lamp 14 is on, trunk connector 2 is in use. If lamp 14 is not on, trunk connector 1 is in use. If lamp 13 is on, the other trunk connector is bad. If lamp 15 is on, data control 2 is on line. If lamp 15 is out, data control 1 is on line. Indications by lamps 14 and 15 should agree with lamp indications on the input-output panel.

3. TELETYPEWRITER CIRCUITS

A. General

3.01 A teletypewriter is used as a link between the No. 101 ESS machine and the maintenance personnel. The teletypewriter handles characters in 5-bit serial form. The call processor gates characters in parallel form. The print-out circuit is used as an interface between the call processor and the teletypewriter (TTY). The TTY is a 28-type machine which has been modified to accept characters in parallel form.

B. Teletypewriter Description (See Fig. 10)

3.02 Characters in serial form are pulsed to the TTY on what is called the loop. The loop is indicated by the heavy lines running between the 120-volt dc rectifier and the select magnet. The select magnet is in series with the loop, and it responds to the character pulses. The select magnet receives the serial character pulses electrically and converts them to a parallel form mechanically. This mechanical linkage is extended through a stunt box to the typing unit. The typing unit receives the character in parallel form mechanically and types the character onto the page.

3.03 The keyboard of the TTY is used to send messages to the call processor. This keyboard consists of a number of keys which are mechanically linked with five code bars. Each code bar is assigned to a bit position of all TTY characters. The code bars are slotted so that when a key is depressed some of the code bars are moved to the left and some are not moved, depending on the code of the TTY character. The movement of the bars corresponds to the TTY code. The signal generator is mechanically linked to the code bars. The signal generator uses the displacement of each code bar to formulate a TTY character which it sends serially on the TTY loop. The character is received by the select magnet and sent through various linkages to the typing unit.

3.04 The character is then printed out on the page. In the No. 101 ESS the typing unit has been modified to include a set of contacts (code reading contacts). The code reading contacts are operated or released by the mechanical linkage in the typing unit according to the TTY code. The bits are transmitted to the print-out circuit as battery and ground signals in parallel form.

3.05 The loop is normally associated with the transmission path which links two or more teletypewriters together. The serial message which is received is normally generated from another teletypewriter on the loop. In our case the call processor message is sent out in parallel form to a parallel to serial distributor. This distributor converts the parallel message to a serial pulsing of the loop.

C. Print-Out Characters

3.06 In order to print out a character from the call processor to the TTY, it is necessary to lock the keyboard. To lock the keyboard, the call processor sends the set keyboard lock (WRT KL1) command. This command resets the KL flip-flop which operates the MCR-G relay. The MCR-G relay operated, opens the operating path of the LSR relay. This releases the normally operated LSR relay. Normally closed contacts of relay LSR shunt the signal generator from the loop so that the keyboard is ineffective (locked) and light the red keyboard locked lamp. The output of the KL flip-flop also inhibits the gate which gates the character from the code

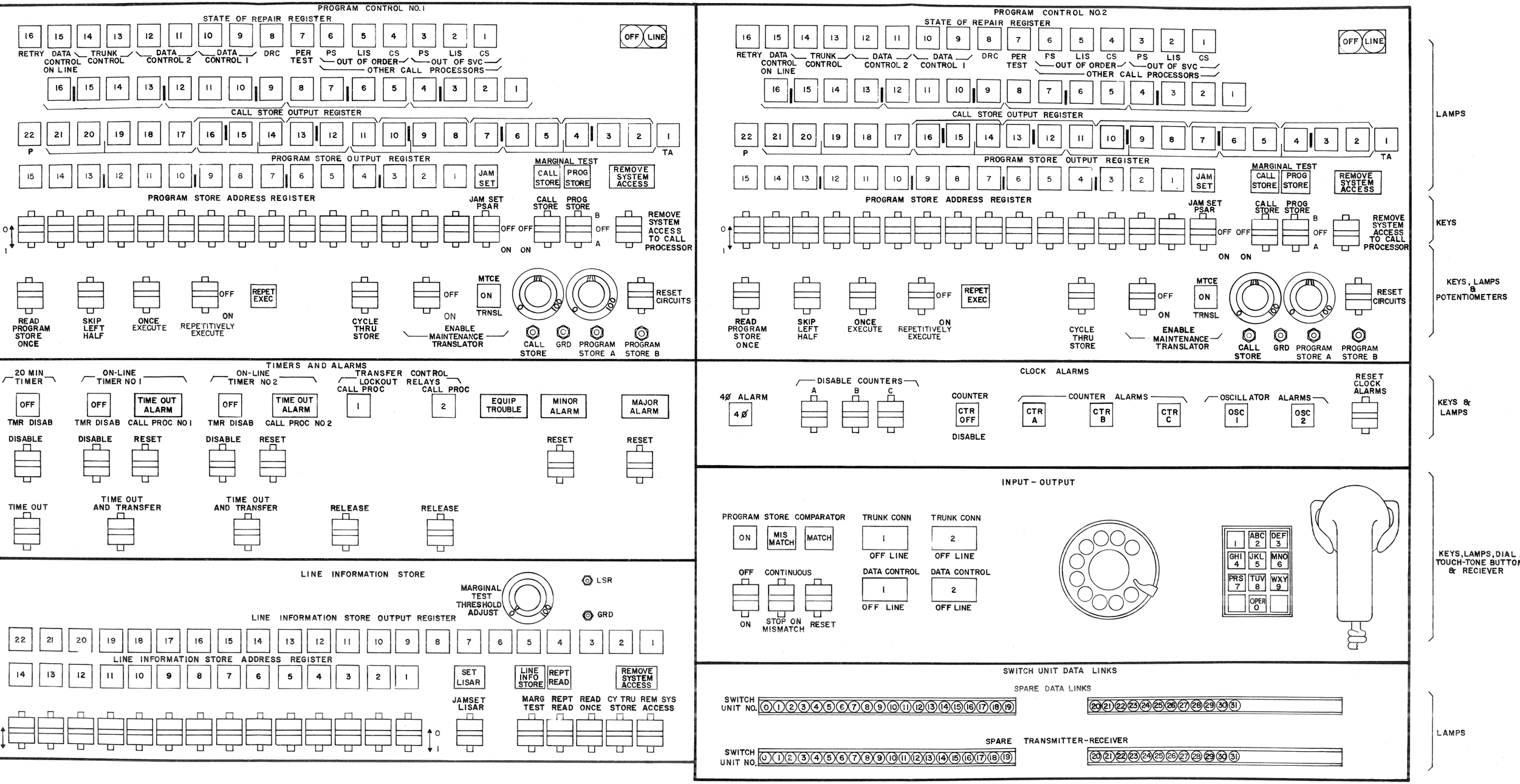


Fig. 9 – Maintenance Center Control Panels

LAMPS

KEYS

KEYS, LAMPS & POTENTIOMETERS

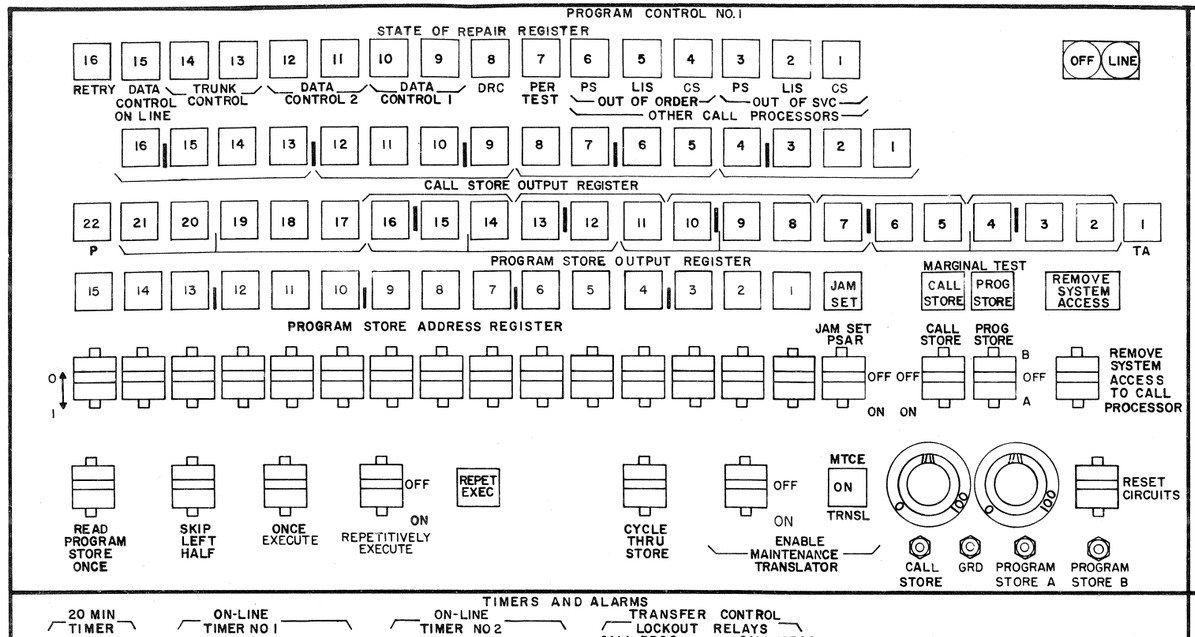
LAMPS

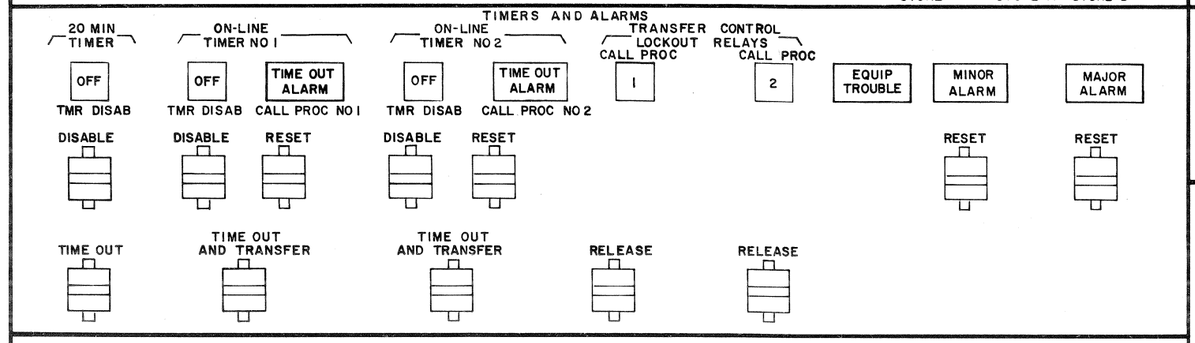
KEYS

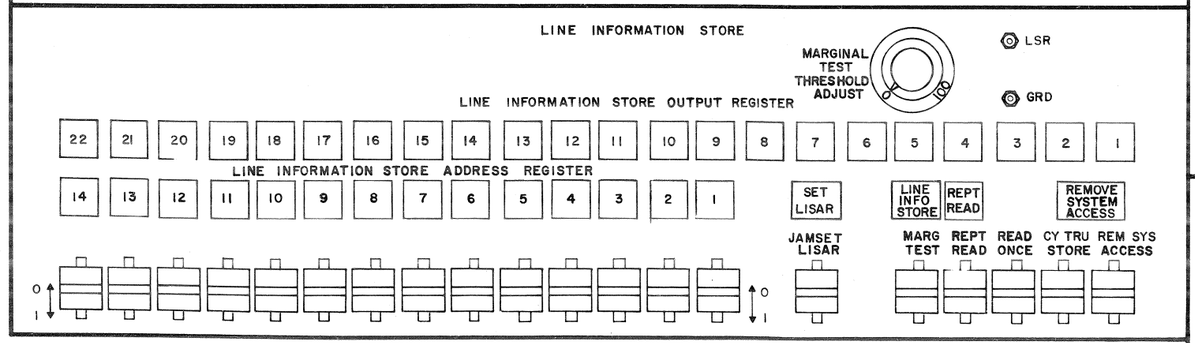
POTENTIOMETER

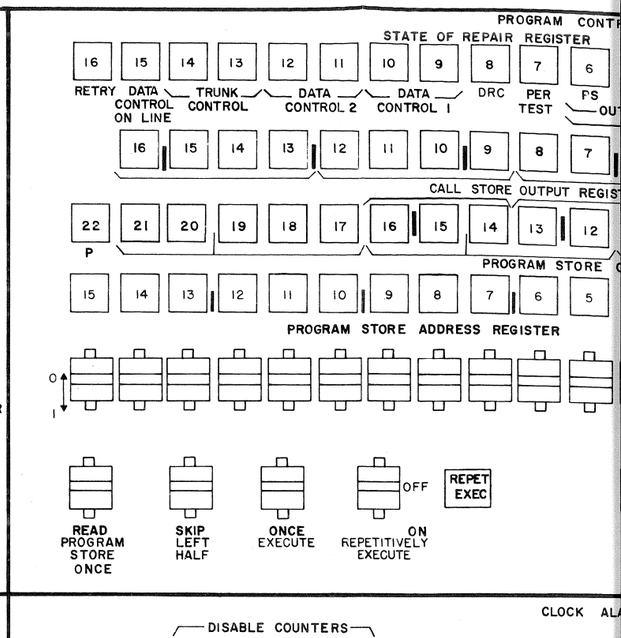
LAMPS

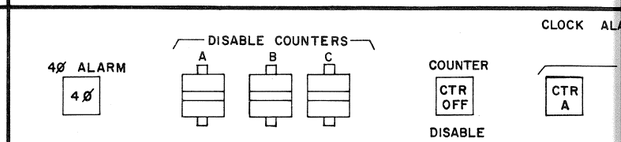
KEYS

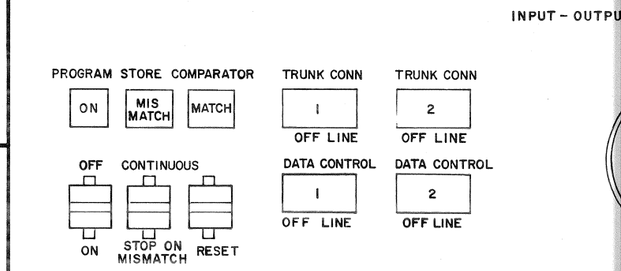


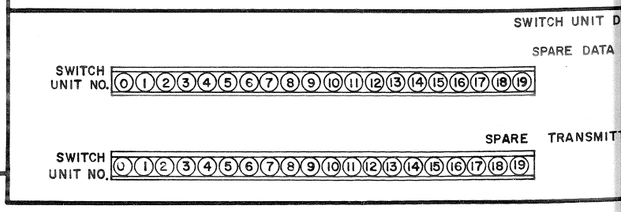












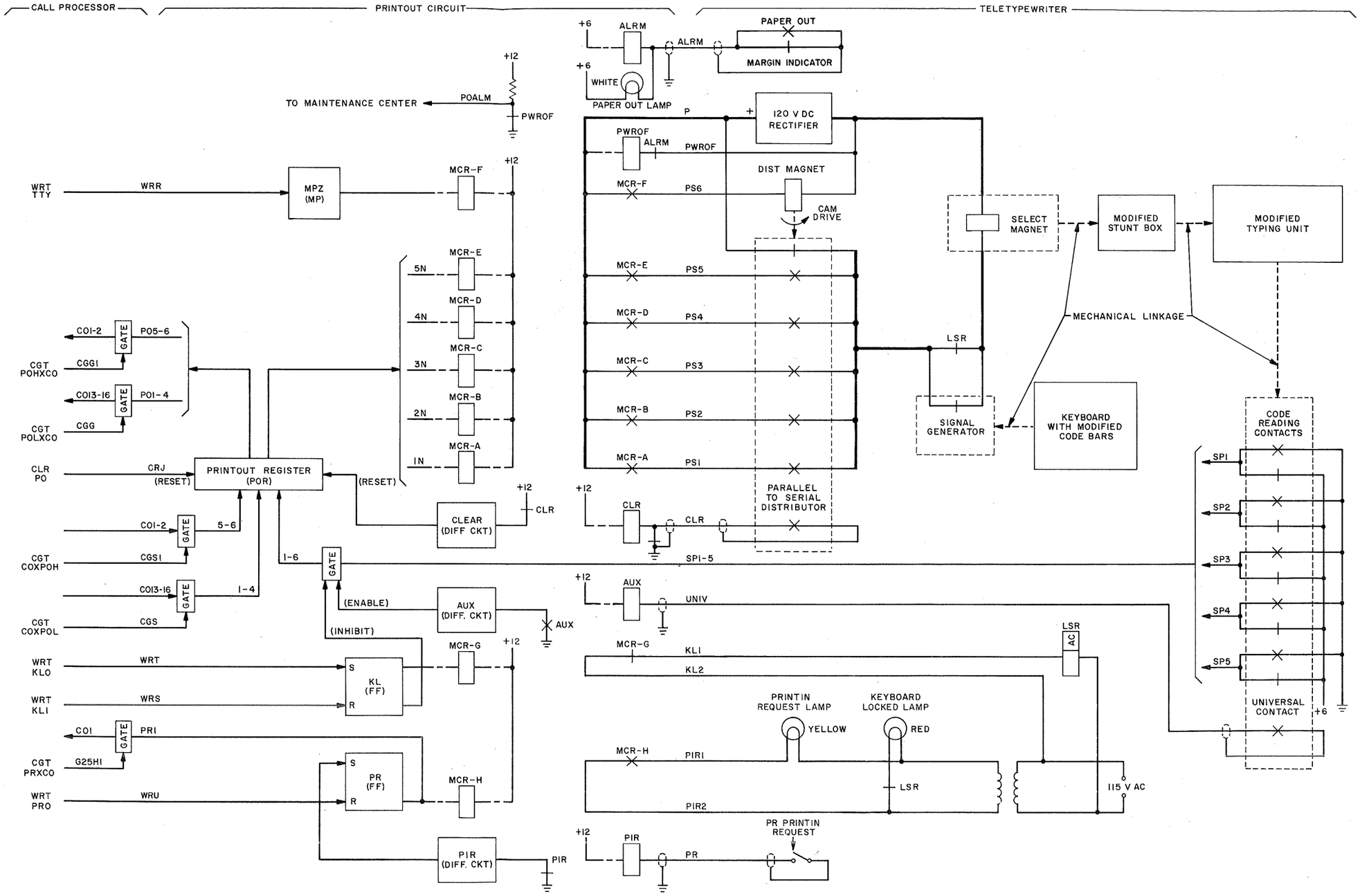


Fig. 10 – Print-Out Circuit and Teletypewriter

reading contacts to the print-out register. This prevents feedback to the print-out register.

3.07 The call processor then initiates a CGT COXPOH command. This command gates the two high order bits to the print-out register. Bit 6 is set to indicate a busy condition. Bit 5 is the high order bit of the TTY character. Then the call processor initiates a CGT COXPOL command. This command gates the four low order bits of the TTY character into the print-out register. Next the program initiates a WRT TTY command. This command sets a 25-msec monopulser which operates the MCR-F relay to start the parallel to serial distributor.

3.08 Contacts of energized MCR-F relay send current through the distributor magnet to unlock a cam drive mechanism. The cam is then allowed to make one revolution. Each of the contacts pictured in the parallel to serial distributor (Fig. 10) is operated by this cam. The top contact (normally closed) is operated first. This corresponds to the TTY start code and opens up the loop. This gets the select magnet ready for action. Then each of the next five contacts is operated in sequence. The contact associated with lead PS5 closes the loop through to the MCR-E contact. The MCR-E contact will be closed if the corresponding relay is operated. The relay is operated if bit 5 of the print-out register is a 1. Therefore depending on the state of the print-out register the loop may be opened or closed at this time. Then the contact associated with the PS4 is closed and bit 4 of the print-out register will determine whether the loop is open or closed. Thus, the character in parallel form in the print-out register is sent serially over the loop. The select magnet responds to this serially coded character and directs the typing unit to print the proper character. The typing unit and the stunt box are modified so the No. 101 ESS TTY code can be used instead of the standard TTY code.

3.09 The bottom contact of the parallel to serial distributor is closed during the middle of the cam revolution, and it is opened again at the end of the revolution. This causes the CLR relay to operate and then to release. The release of this relay is used by the CLEAR differentiating circuit to reset the print-out register. The call processor checks bit 6 of the print-out register once each scan to see if the character has been processed. It uses a CGT POHXCO command to gate the busy idle bit to the CO and checks for an idle print-out register. The call processor sends another teletype character to the print-out register when it is idle. Thus, a message is printed out character by character until a complete message has been formulated.

D. Print Characters In

3.10 The keyboard, signal generator, select magnet, stunt box, and typing unit are used to print a character in. This results in the character being typed and the code reading contacts being opened or closed according to the bit structure of the character. The code bars in the keyboard have been modified so that the No. 101 ESS TTY code is used. Each bit of the TTY code for a character is associated with a code reading transfer contact. Therefore, a ground or battery signal is sent out on the SP- lead. The universal contact is operated to gate the character by operating the AUX relay. The operation of this relay sends a ground through the AUX differentiating circuit to enable the gate. The character is then gated into the print-out register.

3.11 Once each scan, the call processor sends the command CGT POHXCO to check the busy-idle bit. If the busy-idle bit is a 1, the call processor sends a CGT POLXCO command. This gates the remaining bits of the TTY character to the call processor. If the busy idle bit is a 0, the call processor steps a counter which is used as a timer. When the timer is stepped to a point where about 30 seconds have elapsed, the call processor assumes that the print-in message has been discontinued and makes the print-out circuit and TTY available for print-out messages.

3.12 A print-in request (PR) button is provided so the maintenance man can interrupt a long string of print-out messages to print in a message. When this button is pressed, the PIR relay is operated. The operation of this relay is transmitted through the PIR differentiating circuit to set the PR flip-flop. The PR flip-flop being set operates the MCR-H relay. This in turn lights a yellow lamp on the TTY keyboard. When the print-out message has been typed, the call processor uses a CGT PRXCO command to check if the print-in request button has been pressed. This

gates the state of the PR flip-flop to the CO. If a print-in request has been made, the call processor sends a WRT KLO command to set the KL flip-flop. This unlocks the keyboard and extinguishes the red lamp. The maintenance man then prints his message into the call processor. A period is always used to terminate TTY messages. The call processor recognizes the period, gives a print-out response, and continues with the print-out messages which had been interrupted.

E. Teletypewriter Control

3.13 The format of TTY messages to and from the call processor is shown in Fig. 11. The top line of the print-out contains three words. The first word contains three characters and the other words contain four characters each. The next four lines contain one word each. The meaning of the words in the format is covered in a maintenance manual. The format itself is a necessary consideration in the control of TTY print-out messages.

3.14 There are two types of TTY characters. The Xs in the format represent only legal characters (see Table A). Communication between the No. 101 ESS and the maintenance personnel uses an alphabet composed of these 16 legal characters. The 16 remaining characters are referred to as functional characters. For instance, when a format is printed out, three legal characters are printed to form the first word. Then a ***space*** character is sent to the teletypewriter. The ***space*** character performs the function of making the space but nothing is actually printed on the paper. The four characters associated with word 2 are printed out and then another space is sent. Then the four characters associated with word 3 are printed out. Another functional character called ***carriage return, line feed*** (CR, LF) is used to position the teletypewriter so that word 4 may be printed out. The ***space*** and the ***carriage return, line feed*** are the most frequently used functional characters.

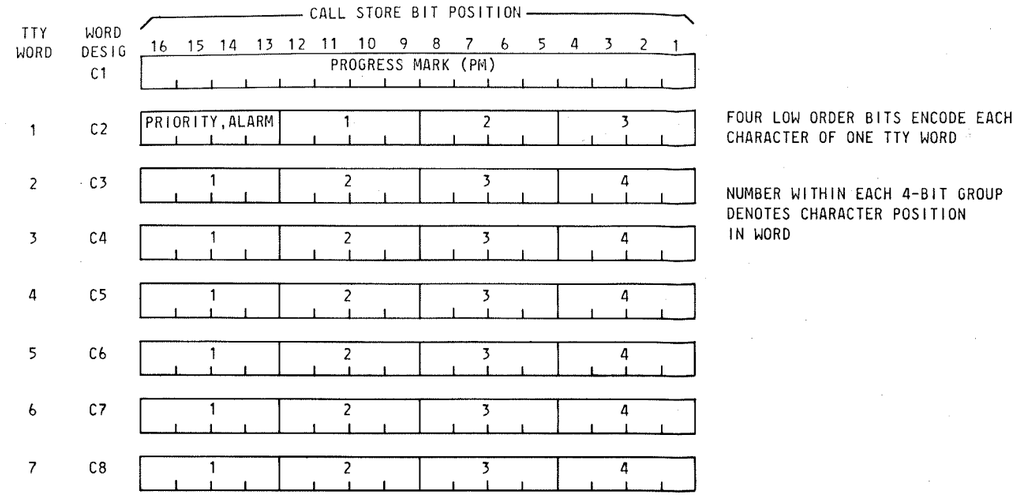
3.15 Table A indicates that some letters are included in the functional character category. These letters are used to form instructional (intermediate) messages from the call processor to the maintenance personnel. One such message is ILLEGAL. The word ILLEGAL is printed out in English, 1 being used for I, and it is used to inform the maintenance man that the message which he has just printed in is not a valid one. Other examples of instructional messages can be found in the maintenance manual under the heading ***Formats.***

TABLE A

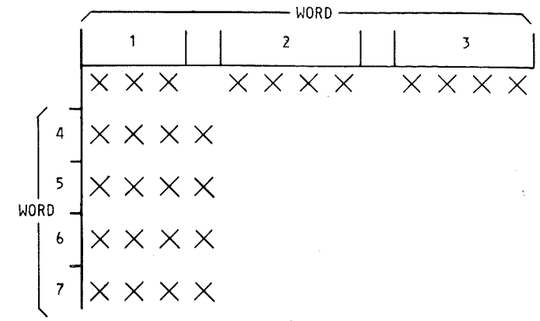
NO. 101 ESS TTY CODE

TTY CODE	OCTAL	TTY CHARACTER	
00000	00	DASH (—)	Legal TTY Characters
00001	01	1	
00010	02	2	
00011	03	3	
00100	04	4	
00101	05	5	
00110	06	6	
00111	07	7	
01000	10	8	
01001	11	9	
01010	12	0	
01011	13	M	
01100	14	S	
01101	15	C	
01110	16	T	
01111	17	R	
10000	20	B	Functional TTY Characters
10001	21	CR,LF	
10010	22	PERIOD(.)	
10011	23	A	
10100	24	E	
10101	25	D	
10110	26	F	
10111	27	G	
11000	30	SPACE	
11001	31	H	
11010	32	K	
11011	33	L	
11100	34	CR,LF,BELL	
11101	35	X	
11110	36	Y	
11111	37	Z	

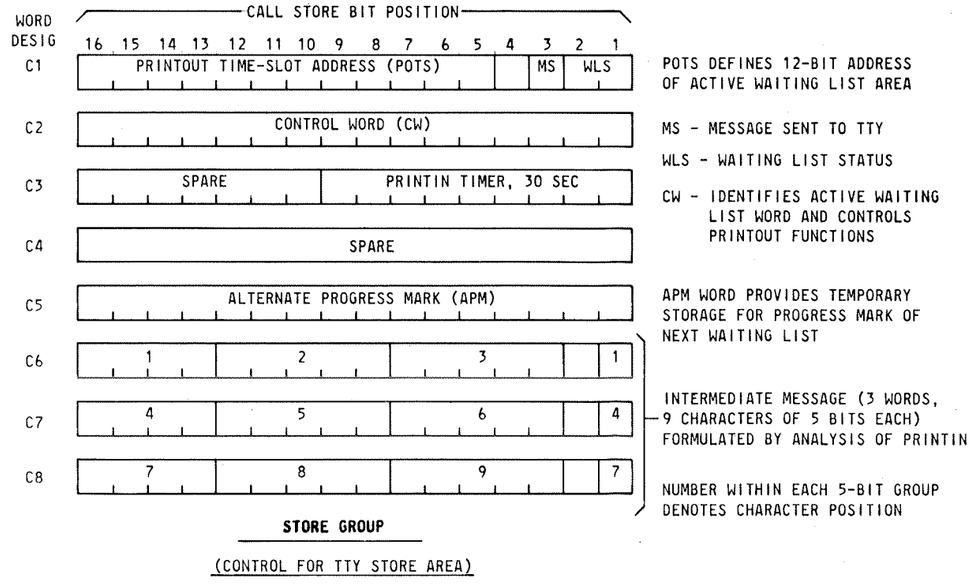
3.16 Legal characters and functional characters are formulated in the call processor in entirely different ways. The high order bit of all legal characters is a 0. The high order bit of all functional characters is a 1. Since legal characters always contain a zero in the high order bit, only the four low order bits need be stored. The messages are stored in the TTY waiting list (Fig. 11) in the call store. A com-



WAITING LIST IN TTY STORE AREA (1 OF 16)



TTY MESSAGE PRINTOUT FORMAT



STORE GROUP

(CONTROL FOR TTY STORE AREA)

PROGRESS MARK ENTRY	DEFINITION
BEN	END OF SCAN FOR PRINTING ROUTINES
BPM20	CONTROLS STANDARD FORMAT PRINTOUT
BPM21	CONTROLS ALL PRINTIN
BPM22	CONTROLS TTY CHECK ROUTINE
BPM23	CONTROLS ALL INTERMEDIATE MSG PRINTOUT
BPM25	CONTROLS TIME OF DAY PRINTOUT

PROGRESS MARK DEFINITIONS

Fig. 11 – TTY Message Formulation

plete message format fills one waiting list group. There are 16 waiting list groups. They are used to store both print-in messages and print-out messages.

3.17 Each waiting list group contains eight words, and word C1 contains a progress mark. This progress mark identifies the type of message which is contained in the waiting list group. Word C2 contains the first TTY word consisting of three characters in bits 1 through 12. Bits 13 through 16 are reserved for priority and alarm code status. Words C3 through C8 of the waiting list group contain words 2 through 7 of the TTY format.

3.18 Only the four low order bits of each character are stored in the waiting list group. The high order bit and the busy-idle bit are furnished to the TTY through programming instructions with the command CGT COXPOH. The four low order bits of the characters are read from the waiting list group to the CO. Then the CO is shifted to the left so that the desired character is placed in bits 13 through 16. Now the four low order bits are gated from the CO to the TTY (CGT COXPOL).

3.19 The ***space*** and ***carriage return, line feed*** characters must be sent between the words. These characters are stored permanently in the program store. The STA command is used to gate these functional characters from the program store to the CO, then the character is gated into the print-out register (POR).

3.20 The program uses an eight-word section called the store group (Fig. 11) to control the format of TTY messages. On printout, control word C2 is used to count the characters as they are printed out and to insert ***spaces*** and ***carriage return, line feed characters*** at the proper places, to address the proper word of the waiting list, and to control the number of places to shift the CO so that the proper character is shifted into bits 13 through 16. The control word is updated every time a character is sent so it will be ready for the next character.

3.21 On printin, the control word is used to steer characters into the waiting list group location. The functional characters are not stored since they have meaning in reference to the TTY only.

3.22 The last three words of each store group are used to store intermediate messages (ILLEGAL, etc). The need for one of these messages is recognized by analyzing the print-in message for errors, etc. When an intermediate message is to be sent, it is first loaded from the program store into the intermediate message words. These words require five bits for each character since the high order bit is quite significant when spelling a word using both functional and legal characters. The message is loaded so that the high order bit of the first character is in bit 1 and the low order bits are in bits 13 through 16 (see Fig. 11). The word is read into the CO and the busy-idle bit is set. The first character is then gated to the TTY. The word is then shifted to the left five places and written back into the call store. The second character is now in position for the next scan. In this way the intermediate message is printed out.

3.23 There are five progress marks and one entrance to the printin routine which are used as shown in Fig. 11. The print-out, printin, and intermediate progress marks are self-evident. The check routine progress mark is used to type every teletypewriter character upon request. The time of day print-out progress mark is used to print the time of day at the end of every TTY message sequence.

3.24 The TTY is the link between the maintenance man and the No. 101 ESS. The maintenance program formulates messages and directs them to the message waiting list. The message is then printed out. The maintenance man prints messages into the message waiting list. When the message is complete, it is directed to the maintenance request program where it is acted upon.

4. TEST POINT COMPARATOR

A. General

4.01 The test point comparator (Fig. 12) is used to compare corresponding test points in the on-line and off-line data, digit, and sender controls. Since these units operate in synchronism at all times, the test points being compared should agree during each clock interval. A mismatch is an indication of trouble, and use of the test point comparator permits the identification of troubles in the circuits being tested.

4.02 The test point comparator circuit contains both low level logic circuits and transistor resistor logic circuits. These circuits are designated by L and T, respectively.

B. Test Probes

4.03 The test probes are high impedance circuits. The high impedance is necessary to prevent loading effects by the test probes from disturbing the potential of the test points. The output of the test probes is the inverse of the voltage detected at the test point.

C. Timing and Control

4.04 The 8-phase clock supplies the timing signals to the comparator. The timing interval during which the comparison is desired is selected by the TEST PHASE switch on the TEST POINT COMPARATOR panel.

4.05 Two μsec before the time interval specified by the switch, the RES1 pulse is produced which resets the COM1 and COM2 flip-flops. The strobe (STR) pulse is then produced during the specified time interval to strobe IC1 and IC2. If the test point voltage is positive when STR is generated, IC- produces a ground output setting the flip-flop COM-. If the test point voltage is at ground, IC- produces a positive voltage and COM- remains in its reset condition.

D. Conditions Existing on Mismatch

4.06 The COM1 and 2 flip-flops feed the match ***and*** gates MAT1 and MAT2. These gates are connected in such a manner that an output is produced only when the two test points being measured are different. For example, if test point A is at ground and B is positive, MAT1 will produce a ground output which sets flip-flop ERR turning on the ERR lamp. The outputs of COM1, COM2, and ERR disable ***and*** gate GA and enable ***and*** gate GB to turn on lamp B. The lamp which is turned on indicates which test point had the positive voltage.

4.07 Once the ERR flip-flop has been set, ***and*** gate DEL is enabled at the following phase 3, setting flip-flop DER. The ground potential, which appears on the reset side of DER, disables ***and*** gates IRAB and IAG preventing further change of the address in the data and digit store address registers.

E. Conditions Existing on Match

4.08 If the potentials appearing at the two test points are the same, gates MAT1 and 2 produce no output to set flip-flops ERR and DER. The ground at the set side of ERR disables gates GA and GB and keeps lamps A, B, and ERR turned off.

4.09 The positive voltage on the reset side of DER partially enables ***and*** gates IRAB and IAG. The clock pulse produced at phase 4 completes the enabling of IRAB which results in the resetting of the address register flip-flops R11 through R29. The pulse occurring at phase 5 then completes the enabling of IAG. The output of IAG enables ***and*** gates G11 through G29 and gates the address from the data control circuits to the address registers.

5. DRAWING REFERENCES

5.01 The following SD drawings and associated circuit descriptions (CDs) give additional information. These are not attached.

Maintenance Center Circuit	SD-1H052-01
Print-Out Circuit	SD-1H060-01
Maintenance Teletypewriter Connecting Circuit	SD-1H068-01
Test Point Comparator Circuit	SD-1H059-01

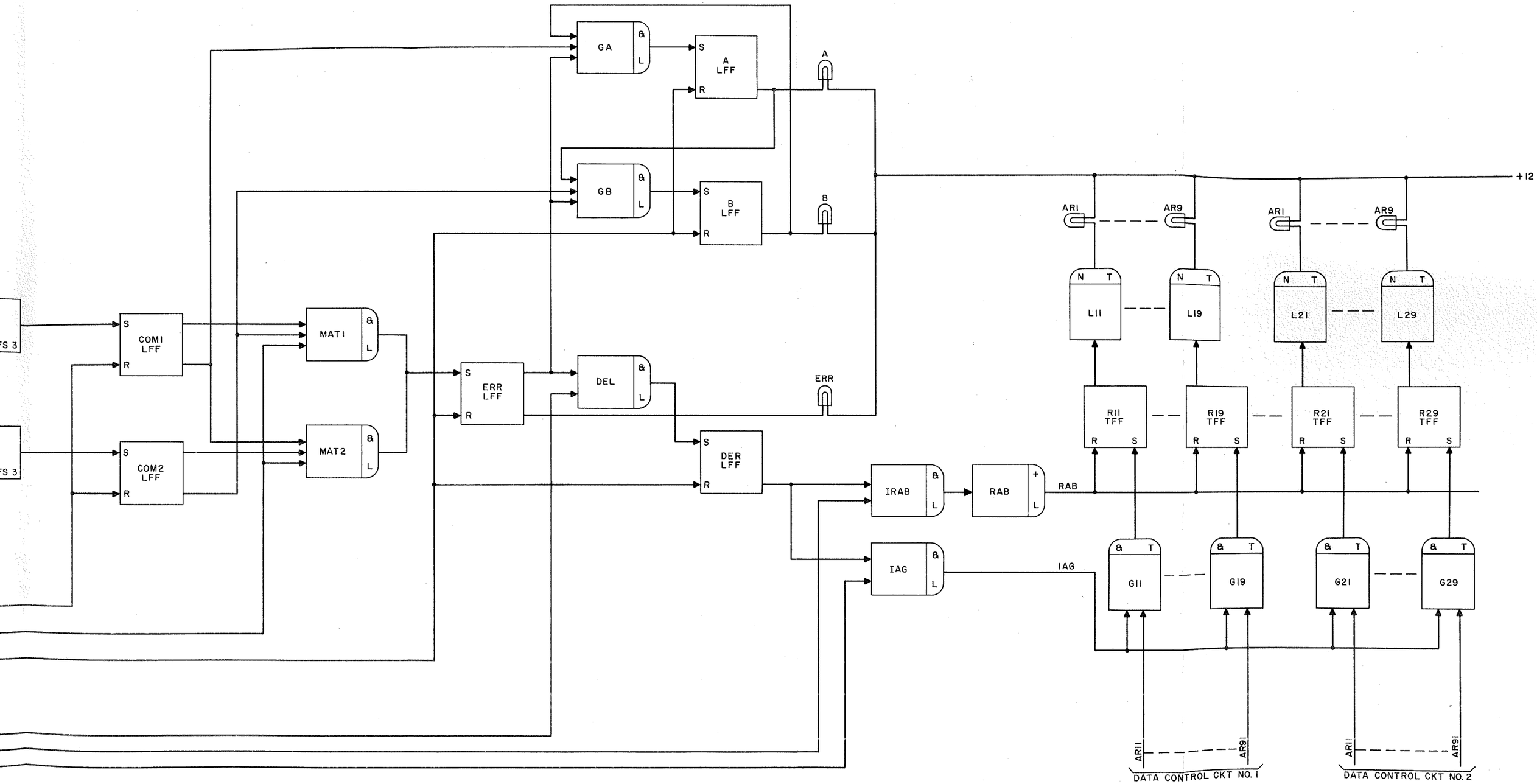
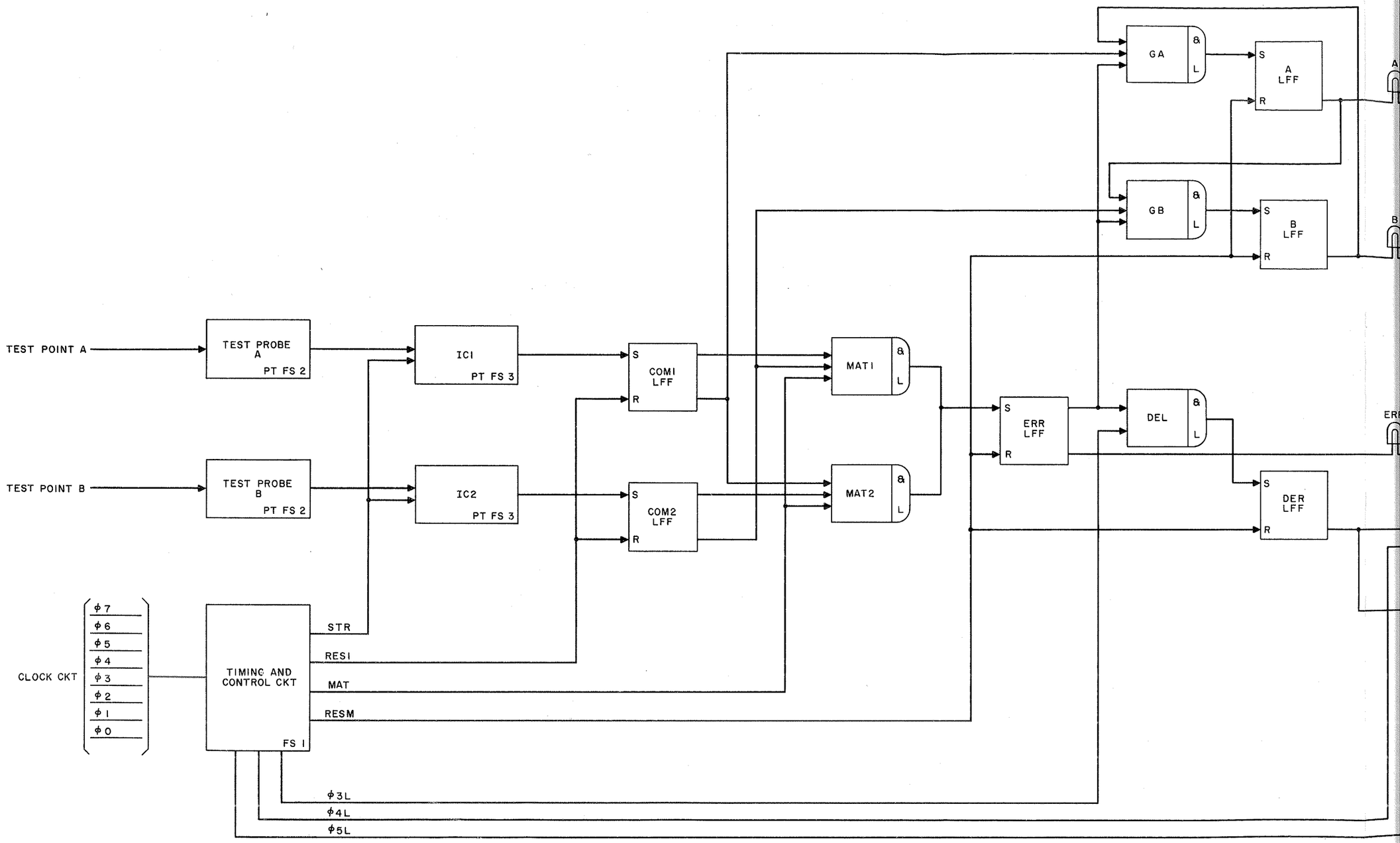


Fig. 12 – Test Point Comparator


TEST POINT A
TEST PROBE A
PT FS 2
ICI
PT FS 3
S
COMI LFF
R
MATI
&
L
GA
S
A LFF
R
GB
S
B LFF
R
S
ERR LFF
R
DEL
S
DER LFF
R
TEST POINT B
TEST PROBE B
PT FS 2
IC2
PT FS 3
S
COM2 LFF
R
MAT2
CLOCK CKT
φ7
φ6
φ5
φ4
φ3
φ2
φ1
φ0
TIMING AND CONTROL CKT
FS 1
STR
RESI
MAT
RESM
φ3L
φ4L
φ5L