MAINTENANCE PROGRAMS
DESCRIPTION OF SYSTEM OPERATION
NO. 101 ELECTRONIC SWITCHING SYSTEM

CONTENTS PAGE

CONTENTS PAGE

CONTENTS PAGE

1. GENERAL

1.01 The maintenance program is used to check all the circuits in the No. 101 ESS except individual line circuits, attendant circuits, and parts of the maintenance center. This includes the time division switches, the various types of stores, the registers, counters, comparators, shift registers, and all of the various wired logic. Operational tests are performed on this equipment through use of the maintenance programs and the call processor equipment. These tests are performed periodically by interspersing them with call processing activity.

1.02 These tests can be broken up into three categories: those that test the call processor equipment, those that test the input-output equipment, and those that test the switch units. The call processor equipment is tested at the end of every call store scan. The on-line call processor directs the testing upon itself and its redundant counterpart. The input-output equipment is also tested at the end of the call store scan. These tests are performed on such equipment as the digit control, sender control, trunk connector, digit receivers, digit receiver connector, and parts of the data control circuitry. The switch unit tests are performed after each sector scan. The switch unit tests also cover the data receivers and transmitters and parts of the data control. The central office trunks and digit trunks are tested by the trunk maintenance program on a per sector basis.

2. CALL PROCESSOR MAINTENANCE, ORGANIZATION

A. General

2.01 The call processor consists of a program control (PC) and its associated call store (CS).

Note: In this context it is customary to use *PC* as meaning the combination of program control logic and its associated program store. However, in order to make certain operations clear, the associated call store (CS) is separately identified.

This equipment is redundant, so there is an "other program control" (OPC) and an "other call store" (OCS). The OPC and the OCS are the off-line portions of the call processor. For instance, if PC1 is on line, then PC2 is the OPC. The same program control and call store are always associated with each other. The line information store (LIS) is not redundant. Each PC has access to it. If the LIS goes out of service, some of the special services which make use of the LIS are lost to the customer while other services are given to all extensions and all calling restrictions are suspended. However, basic call processing continues.

2.02 The call processor maintenance can be divided into three categories: on-line tests, off-line tests, and LIS tests. The on-line tests are used to discover trouble in the PC or the CS. If a trouble is discovered, no attempt is made to isolate it; the PCs are simply switched. For instance, if PC1 is on line and it discovers a trouble during the on-line maintenance program, it will effect a switch of program controls. Now PC2 becomes the on-line PC, and PC1 becomes the OPC. However, the switch of program controls does not take place immediately. Most of the tests are arranged so that a failure will result in a retry of all the on-line maintenance. The second failure effects the switch of PCs.

2.03 The OPC and OCS are tested under the control of the on-line system. In this case, the tests are diagnostic in function. Troubles are not only detected, but a print-out message is printed out on the teletypewriter (TTY) to tell where the trouble is located.

2.04 The LIS tests are also diagnostic in function. A failure in the LIS will result in a maintenance printout to help locate the trouble.

2.05 The call processor tests require a relatively long time. It is not possible to perform all the call processor tests at the end of every scan. Therefore, a portion of the tests are performed on each scan. It takes 256 scans to completely test the call processor.

B. On-Line Program Control Tests (Every Scan)

2.06 Some on-line testing is done at the end of each scan. The entry for this testing is EOSTC (see Fig. 1). When call processing is complete for a particular scan, the EOSTC entry is used to enter the program control maintenance routines. First, the on-line program store is tested. Nine transfer commands are performed, each one transferring to the next. If any part of the program store address or output equipment is in trouble, one of the transfer commands will not be performed properly. The result will be a transfer error, a parity error, or a program loop which, after a 2-second time-out, causes a switch of program controls.

2.07 Next, a series of clear and gate commands is performed. A word is read into the call store output register (CO) and gated through several gating paths back to the CO. Several of these gating path loops are performed around the CO. Four different words are gated through the various gating path loops. After each test, the test word is used to advance to the next test. A failure will result in a 2-second time-out, and a switch of program control will take place.

2.08 Next, the clear commands are tested. Here all bits of the registers associated with the clear command are set to one. Then the register is cleared and its contents is gated to the CO. The CO is checked for all zeros. A failure in the clear command test results in a WRT EB1 command. The WRT EB1 command sets bit 1 of the on-line error register and starts a retry of the on-line PC tests. A failure of the retry will cause a PC switch.

C. End-of-Scan Test Monitor

2.09 If the clear command tests are successful, the program proceeds to a transfer vector called BGMON. The purpose of this routine is to direct the program to the various tests which do not take place on every scan. Some of these tests take place once every 16 scans and others take place once every 256 scans. The BGMON routine uses an 8-bit binary counter to determine which test to perform on a particular scan. The counter is called the scan counter. It is located in the call store in the maintenance control record, word C1, bits 1 through 8.

2.10 Fig. 2 is a table which outlines the various tests that are performed and the order in which they are performed. The command translator test takes place every 16 scans. The first column contains 16 different tests concerned with the OPC, and each takes place once every 256 scans. The rest of the columns are concerned with on-line PC maintenance, on-line CS maintenance, OCS maintenance, and LIS tests.

2.11 The columns (Fig. 2, Table B) correspond to bits 1 through 4 of the scan counter (transfer vector 1). For all columns other than the first column, the high order bits (Fig. 2, Table A) have no effect on determining the test to be performed. When the low order bits (transfer vector 1) equal 0000, one of the tests in column 1 must be chosen. Bits 5 through 8 of the scan count are used to determine which one of these tests is to be selected. Depending upon the scan count, one of 29 tests will be performed.

D. On-Line Program Control Tests (Per Scan)

2.12 The first group of tests to consider in the on-line PC tests are TX1, TCNS1, and TOCT. These tests check the command translators and the command logic portions of the PC. A failure in these tests results in a WRT EB1 command which forces a retry of all the on-line tests.

E. On-Line Call Store Tests

2.13 The CS tests consist of reading and writing test words into various addresses in the store. The access equipment and the output equipment are tested separately. The access equipment is further subdivided into three parts, one part for each matrix. Sixteen end-of-scan tests are performed to fully test the eight rows and eight columns of a matrix.

2.14 Each row or column test consists of testing eight addresses of the CS. A common routine called CMS1N is used for this function for both the on-line CS and the OCS.

2.15 If the on-line CS is being tested, a failure is noted by marking the logic flip-flop equal to one (SET LF). The logic flip-flop is checked during the on-line CS monitor to determine if an error has been detected. Failure of the access tests results in a retry of the on-line tests. A second failure results in a PC switch.

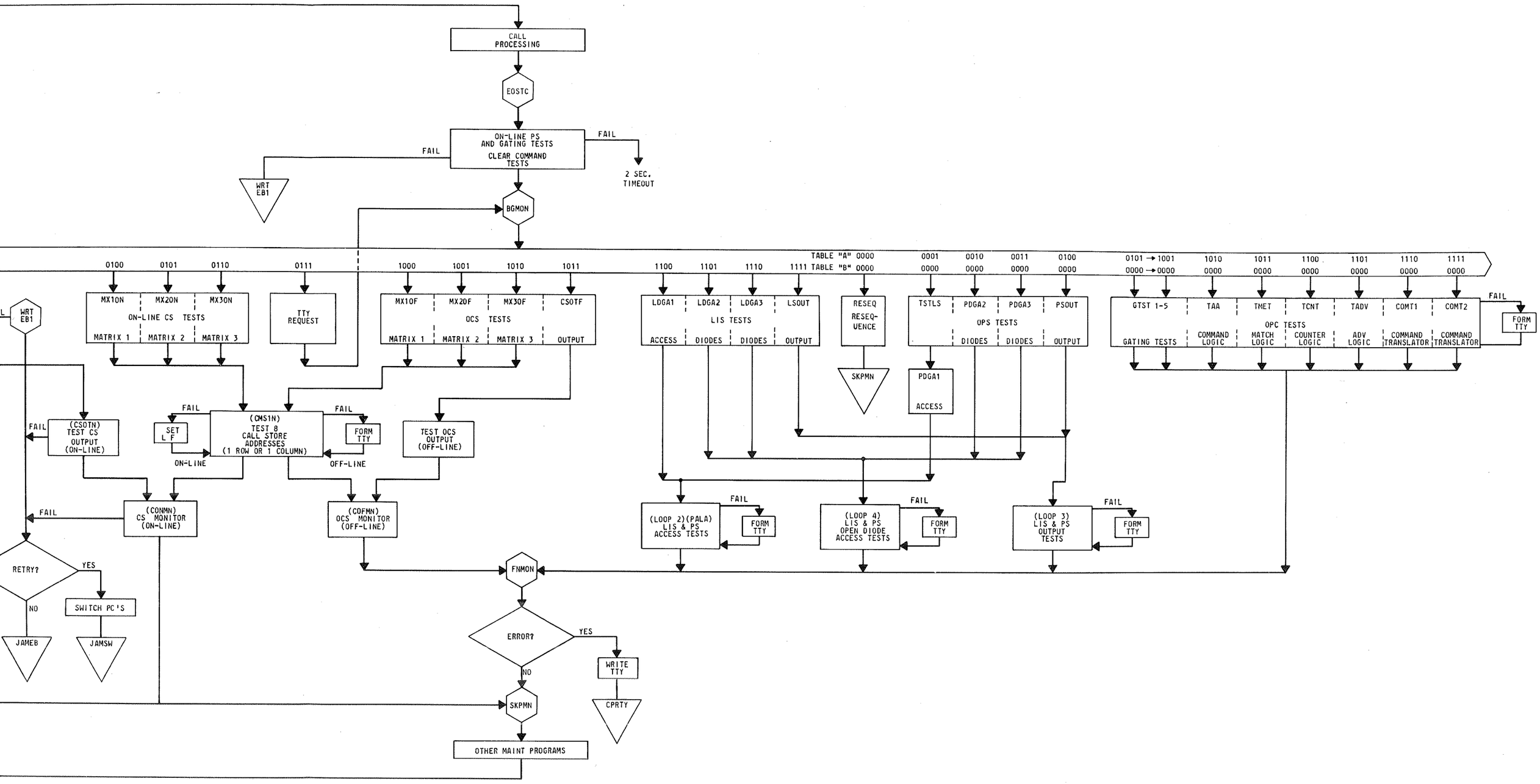


Fig. 1 – Call Processor Maintenance Program

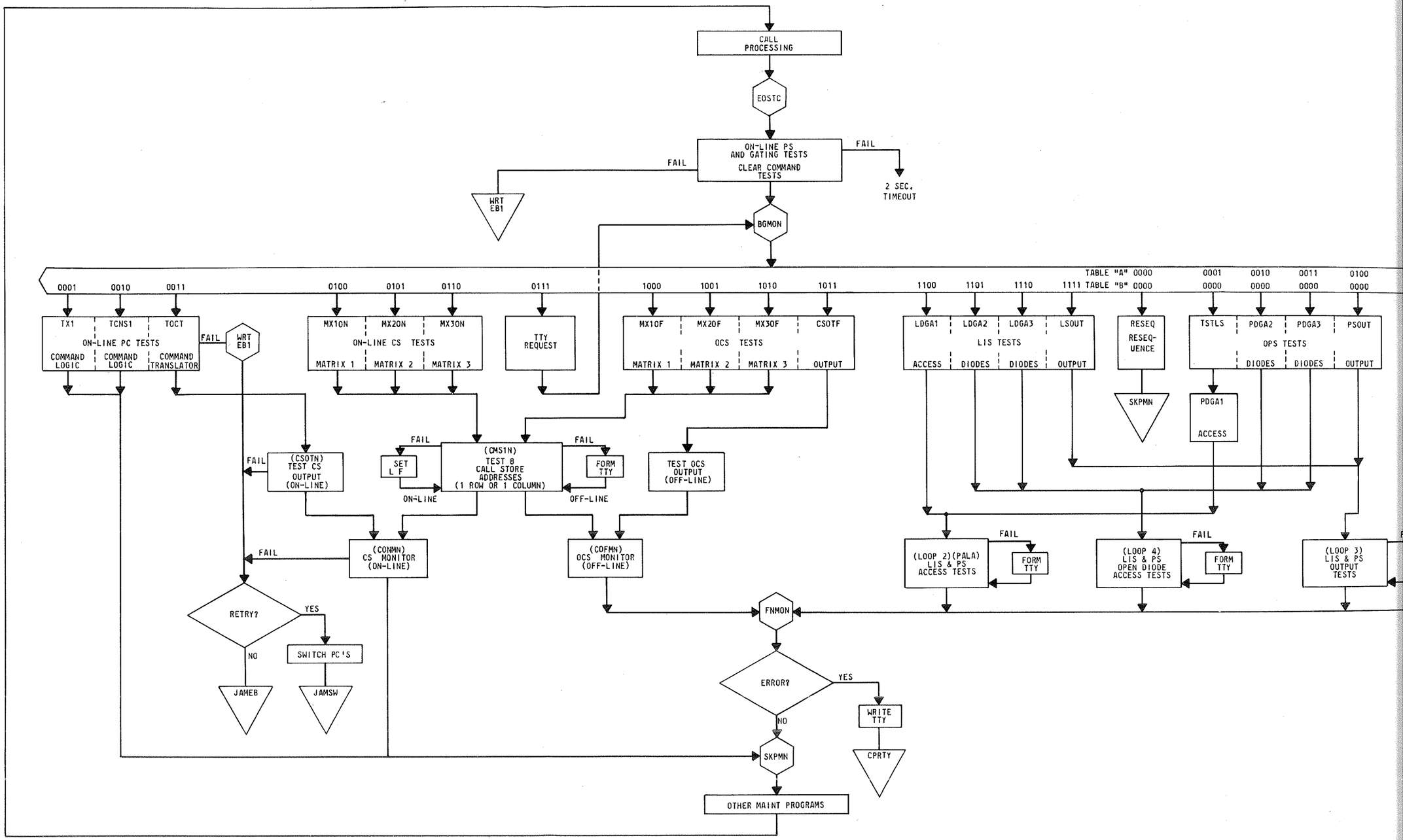

CALL PROCESSING
EOSTC
ON-LINE PS AND GATING TESTS CLEAR COMMAND TESTS
FAIL
2 SEC. TIMEOUT
WRT EB1
BGMON
0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 TABLE "B" 0000
TABLE "A" 0000 0001 0000 0010 0000 0011 0000 0100 0000
TX1 TCNS1 TOCT
ON-LINE PC TESTS
COMMAND LOGIC
COMMAND LOGIC
COMMAND TRANSLATOR
MX10N MX20N MX30N
ON-LINE CS TESTS
MATRIX 1 MATRIX 2 MATRIX 3
TTY REQUEST
MX10F MX20F MX30F CSOTF
OCS TESTS
MATRIX 1 MATRIX 2 MATRIX 3 OUTPUT
LDGA1 LDGA2 LDGA3 LSOUT
LIS TESTS
ACCESS DIODES DIODES OUTPUT
RESEQ
RESEQ-UENCE
SKPMN
TSTLS PDGA2 PDGA3 PSOUT
OPS TESTS
PDGA1
ACCESS
DIODES DIODES OUTPUT
(CSOTN) TEST CS OUTPUT (ON-LINE)
SET L F
(CMS1N) TEST 8 CALL STORE ADDRESSES (1 ROW OR 1 COLUMN)
FORM TTY
ON-LINE
OFF-LINE
TEST OCS OUTPUT (OFF-LINE)
(CONMN) CS MONITOR (ON-LINE)
(COFMN) OCS MONITOR (OFF-LINE)
(LOOP 2)(PALA) LIS & PS ACCESS TESTS
(LOOP 4) LIS & PS OPEN DIODE ACCESS TESTS
(LOOP 3) LIS & PS OUTPUT TESTS
RETRY?
YES
NO
SWITCH PC'S
JAMEB
JAMSW
FNMON
ERROR?
WRITE TTY
CPRTY
SKPMN
OTHER MAINT PROGRAMS

TABLE B

TABLE "A"	1/256 SCAN TESTS	0000 OFF-LINE PC TESTS	0001 COMMAND LOGIC	0010 COMMAND LOGIC	0011 COMMAND TRANSLATOR & CS OUTPUT	0100 CS ACCESS MATRIX 1	0101 CS ACCESS MATRIX 2	0110 CS ACCESS MATRIX 3	0111 TTY REQUEST	1000 OCS ACCESS MATRIX 1	1001 OCS ACCESS MATRIX 2	1010 OCS ACCESS MATRIX 3	1011 OCS OUTPUT	1100 LIS ACCESS	1101 LIS ACCESS (PLANE DIODES)	1110 LIS ACCESS (WORD DIODES)	1111 LIS OUTPUT
0000	RESEQUENCE	1 RESEQ	2 TX1	3 TCNS1	4 TOCT & CSOTN	5 MX1ON (COL 1)	6 MX2ON (COL 1)	7 MX3ON (COL 1)	8	9 MX1OF (COL 1L	10 MX2OF (COL 1)	11 MX3OF (COL 1)	12 CSOTF	13 LDGA1	14 LDGA2	15 LDGA3	16 LSOUT
0001	LONG SHIFT PS ACCESS	17 TSTLS PDGA1	18 TX1	19 TCNS1	20 TOCT & CSOTN	21 MX1ON (ROW 1)	22 MX2ON (ROW 1)	23 MX3ON (ROW 1)	24	25 MX1OF (ROW 1)	26 MX2OF (ROW 1)	27 MX3OF (ROW 1)	28 CSOTF	29 LDGA1	30 LDGA2	31 LDGA3	32 LSOUT
0010	PS ACCESS (PLANE DIODES)	33 PDGA2	34 TX1	35 TCNS1	36 TOCT & CSOTN	37 MX1ON (COL 2)	38 MX2ON (COL 2)	39 MX3ON (COL 2)	40	41 MX1OF (COL 2)	42 MX2OF (COL 2)	43 MX3OF (COL 2)	44 CSOTF	45 LDGA1	46 LDGA2	47 LDGA3	48 LSOUT
0011	PS ACCESS (WORD DIODES)	49 PDGA3	50 TX1	51 TCNS1	52 TOCT & CSOTN	53 MX1ON (ROW 2)	54 MX2ON (ROW 2)	55 MX3ON (ROW 2)	56	57 MX1OF (ROW 2)	58 MX2OF (ROW 2)	59 MX3OF (ROW 2)	60 CSOTF	61 LDGA1	62 LDGA2	63 LDGA3	64 LSOUT
0100	PS OUTPUT	65 PSOUT	66 TX1	67 TCNS1	68 TOCT & CSOTN	69 MX1ON (COL 3)	70 MX2ON (COL 3)	71 MX3ON (COL 3)	72	73 MX1OF (COL 3)	74 MX2OF (COL 3)	75 MX3OF (COL 3)	76 CSOTF	77 LDGA1	78 LDGA2	79 LDGA3	80 LSOUT
0101	GATING TESTS	81 GTST1	82 TX1	83 TCNS1	84 TOCT & CSOTN	85 MX1ON (ROW 3)	86 MX2ON (ROW 3)	87 MX3ON (ROW 3)	88	89 MX1OF (ROW 3)	90 MX2OF (ROW 3)	91 MX3OF (ROW 3)	92 CSOTF	93 LDGA1	94 LDGA2	95 LDGA3	96 LSOUT
0110		97 GTST2	98 TX1	99 TCNS1	100 TOCT & CSOTN	101 MX1ON (COL 4)	102 MX2ON (COL 4)	103 MX3ON (COL 4)	104	105 MX1OF (COL 4)	106 MX2OF (COL 4)	107 MX3OF (COL 4)	108 CSOTF	109 LDGA1	110 LDGA2	111 LDGA3	112 LSOUT
0111		113 GTST3	114 TX1	115 TCNS1	116 TOCT & CSOIN	117 MX1ON (ROW 4)	118 MX2ON (ROW 4)	119 MX3ON (ROW 4)	120	121 MX1OF (ROW 4)	122 MC2OF (ROW 4)	123 MX3OF (ROW 4)	124 CSOTF	125 LDGA1	126 LDGA2	127 LDGA3	128 LSOUT
1000		129 GTST4	130 TX1	131 TCNS1	132 TOCT & CSOTN	133 MX1ON (COL 5)	134 MX2ON (COL 5)	135 MX3ON (COL 5)	136	137 MX1OF (COL 5)	138 MX2OF (COL 5)	139 MX3OF (COL 5)	140 CSOTF	141 LDGA1	142 LDGA2	143 LDGA3	144 LSOUT
1001		145 GTST5	146 TX1	147 TCNS1	148 TOCT & CSOTN	149 MX1ON (ROW 5)	150 MX2ON (ROW 5)	151 MX3ON (ROW 5)	152	153 MX1ON (ROW 5)	154 MX2ON (ROW 5)	155 MX3ON (ROW 5)	156 CSOTF	157 LDGA1	158 LDGA2	159 LDGA3	160 LSOUT
1010	COMMAND LOGIC	161 TAA	162 TX1	163 TCNS1	164 TOCT & CSOTN	165 MX1ON (COL 6)	166 MX2ON (COL 6)	167 MX3ON (COL 6)	168	169 MX1ON (COL 6)	170 MX2ON (COL 6)	171 MX3ON (COL 6)	172 CSOTF	173 LDGA1	174 LDGA2	175 LDGA3	176 LSOUT
1011	MATCH LOGIC	177 TMET	178 TX1	179 TCNS1	180 TOCT & CSOTN	181 MX1ON (ROW 6)	182 MX2ON (ROW 6)	183 MX3ON (ROW 6)	184	185 MX1ON (ROW 6)	186 MX2ON (ROW 6)	187 MX3ON (ROW 6)	188 CSOTF	189 LDGA1	190 LDGA2	191 LDGA3	192 LSOUT
1100	COUNTER LOGIC	193 TCNT	194 TX1	195 TCNS1	196 TOCT & CSOTN	197 MX1ON (COL 7)	198 MX2ON (COL 7)	199 MX3ON (COL 7)	200	201 MX1ON (COL 7)	202 MX2ON (COL 7)	203 MX3ON (COL 7)	204 CSOTF	205 LDGA1	206 LDGA2	207 LDGA3	208 LSOUT
1101	ADV LOGIC	209 TADV	210 TX1	211 TCNS1	212 TOCT & CSOTN	213 MX1ON (ROW 7)	214 MX2ON (ROW 7)	215 MX3ON (ROW 7)	216	217 MX1ON (ROW 7)	218 MX2ON (ROW 7)	219 MX3ON (ROW 7)	220 CSOTF	221 LDGA1	222 LDGA2	223 LDGA3	224 LSOUT
1110	COMMAND TRANSLATOR	225 COMT1	226 TX1	227 TCNS1	228 TOCT & CSOTN	229 MX1ON (COL 8)	230 MX2ON (COL 8)	231 MX3ON (COL 8)	232	233 MX1ON (COL 8)	234 MX2ON (COL 8)	235 MX3ON (COL 8)	236 CSOTF	237 LDGA1	238 LDGA2	239 LDGA3	240 LSOUT
1111		241 COMT2	242 TX1	243 TCNS1	244 TOCT & CSOTN	245 MX1ON (ROW 8)	246 MX2ON (ROW 8)	247 MX3ON (ROW 8)	248	249 MX1ON (ROW 8)	250 MX2ON (ROW 8)	251 MX3ON (ROW 8)	252 CSOTF	253 LDGA1	254 LDGA2	255 LDGA3	256 LSOUT
		OPC TESTS	ON-LINE TESTS							OCS TESTS				LIS TESTS			

Fig. 2 – Normal Test Sequence of Call Processor Tests

2.16 The information in the scan count is used to direct the program to one of the three CS access matrix tests which correspond to a column in Fig. 2 and to one of the eight row tests or one of the eight column tests. The difference between all the various access tests is simply a question of which address is used.

2.17 The on-line CS output tests (CSO1N) are performed during the same scan as the TCNS1 test. The output tests simply check that the read function is inhibited during the write phase. A failure results in a retry of the on-line equipment.

F. Other Call Store Tests

2.18 The OCS tests use the same routine (CMS1N) as the on-line CS tests. The difference is that a failure causes the formation of a transient failure TTY message. After the test is completed, FNMON is entered. Here the TTY message is printed out and a complete (CP) retry is started. The use of the scan count to dictate which OCS test to perform is similar to the on-line CS tests.

G. Line Information Store and Other Program Store Tests

2.19 The LIS tests are divided into three types. First, access equipment of the LIS is tested. This equipment includes the translators but is not a thorough test of the diodes themselves. Second is a two-part test for open diodes in the LIS access circuitry. The third category is the LIS output tests. Fig. 1 shows that the other program store (OPS) tests use the same test routines as the LIS plus an additional routine to verify that long shifts between the call store output registers can be made. These tests, except for the long shift test, consist of reading selected addresses which are reserved for maintenance purposes. A failure of any of these tests results in the formation of a TTY message. These messages are completed and printed out upon entry of the FNMON entry, and a CP retry is started.

2.20 The OPS tests use the same routines for testing and are organized in the same way as the LIS tests. However, these tests are performed once every 256 scans.

H. Other Program Control Tests

2.21 The other tests in the 0000 column are also performed only once every 256 scans. All of them produce a teletype message on failure, and result in a CP retry. These tests are unique in that both program controls are used to accomplish them. Test routines in the OPS are directed by the on-line program control to be executed. The on-line program control keeps track of these executions through a device called a marker. These markers are generated by the off-line PC at various intervals of the program. They consist of WRT ET1 commands. This command marks bit 2 of the on-line error register to a one. The on-line PC checks for these bits at appropriate intervals. If a marker is not detected at the proper time, it is an indication of trouble.

2.22 The same routines which were used for the end-of-scan on-line program control tests are used for the off-line program control tests. A failure of these tests results in a WRT EB1 command. Since these routines are physically located in the off-line store, the WRT EB1 command will set bit 3 of the on-line error register. The on-line system checks for these errors between execute commands.

3. ERROR PATHS OF PROGRAM CONTROL MAINTENANCE

A. General

3.01 Failure of any test results in a retry or a 2-second time-out. The retry is performed so transient errors will be ignored. If a failure occurs in the on-line PC or CS, a retry of all on-line tests is performed. A second failure (failure during the on-line retry) causes a PC switch. Some on-line PC test failures cause a 2-second time-out. In this case a PC switch is performed without a retry.

3.02 Failure of off-line tests results in a transient failure TTY printout followed by a complete (CP) retry. A CP retry is a retry of both on- and off-line tests. A CP retry is also performed following a PC switch.

B. On-Line Retry

3.03 Fig. 3 shows the error paths of PC maintenance. Both on-line and CP retries are shown. The entry CPEST is used for retries.

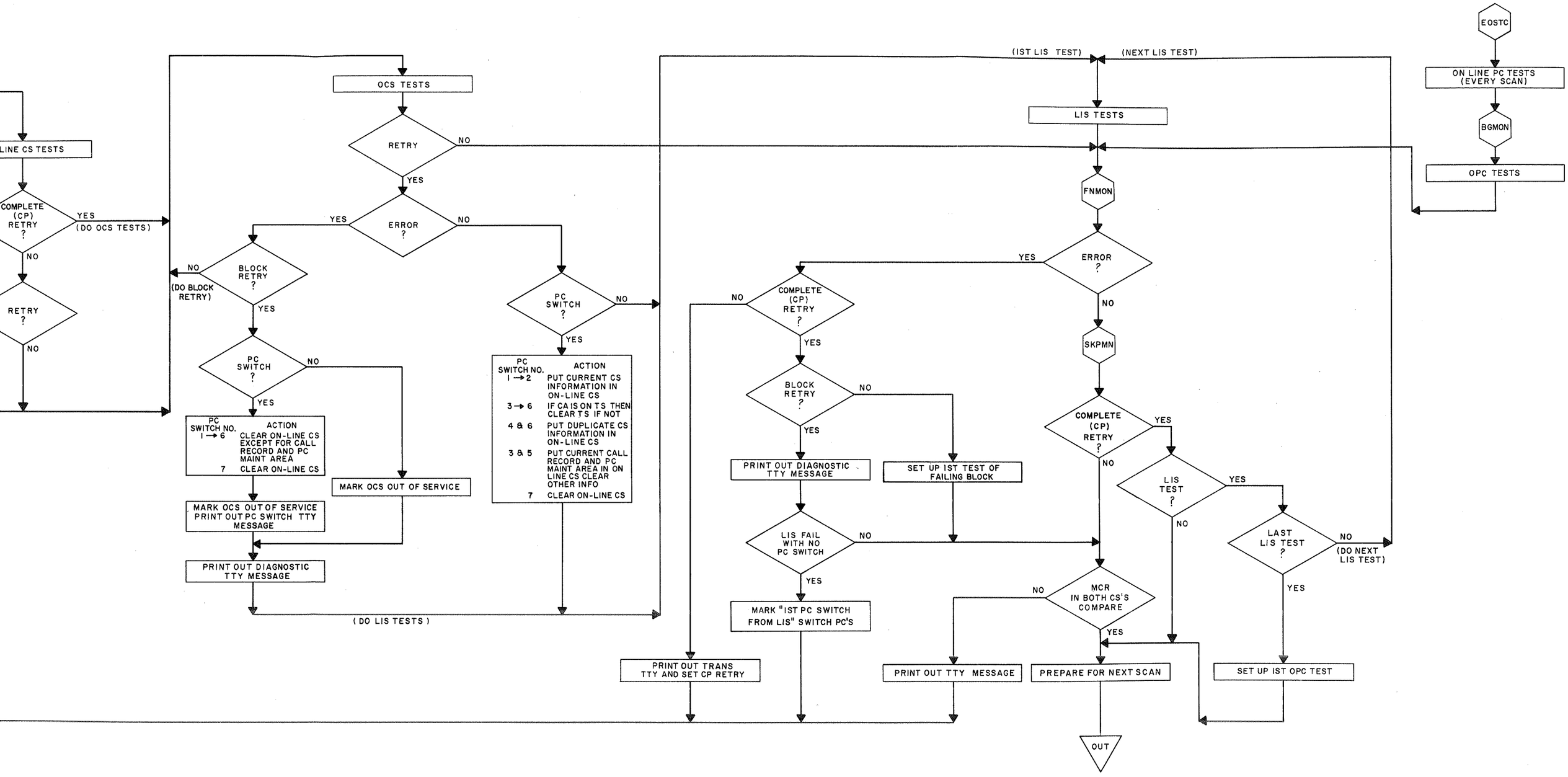
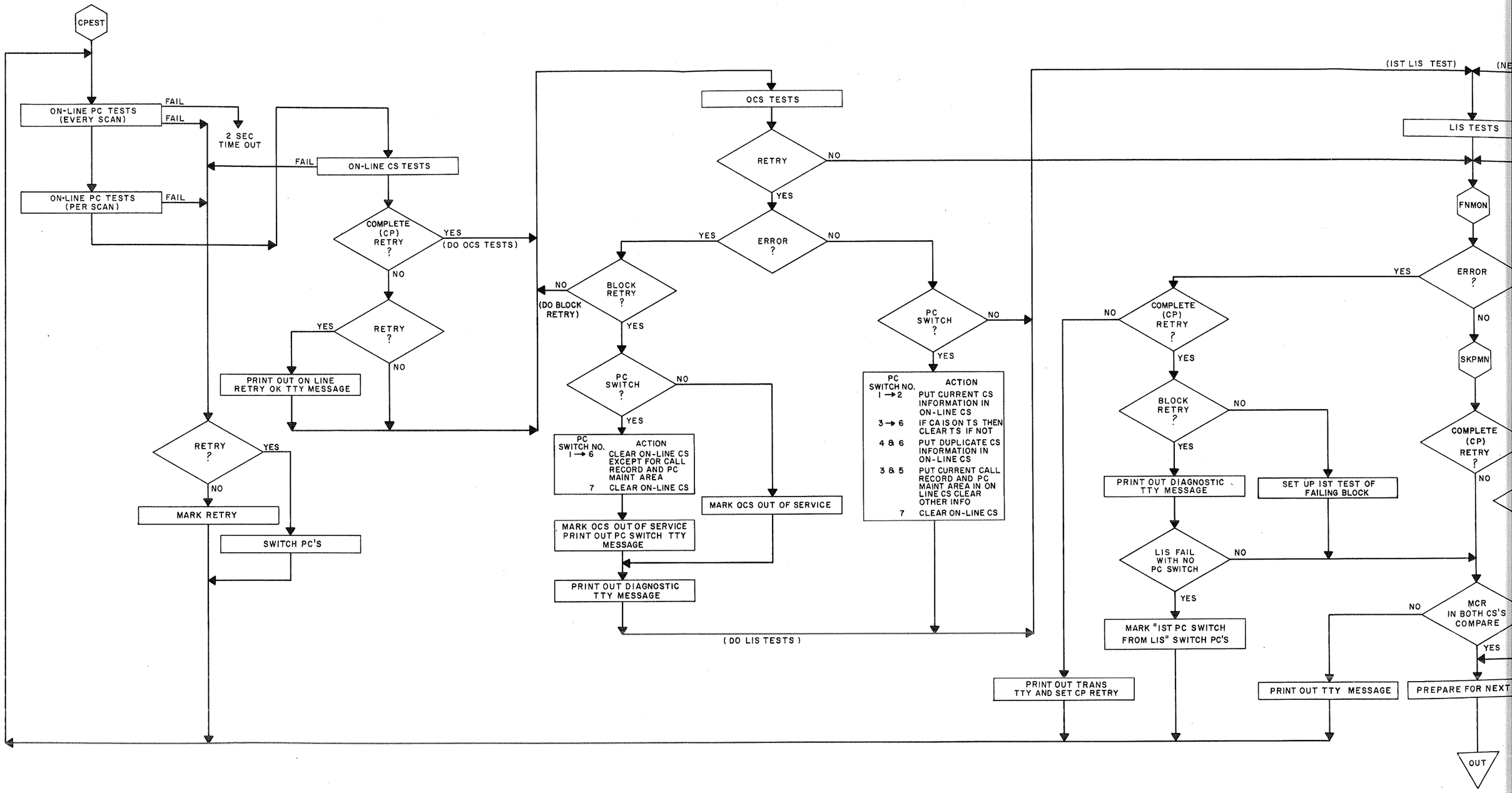


Fig. 3 – PC Maintenance — Error Paths


CPEST
ON-LINE PC TESTS (EVERY SCAN)
FAIL
FAIL
2 SEC TIME OUT
ON-LINE PC TESTS (PER SCAN)
FAIL
FAIL
ON-LINE CS TESTS
COMPLETE (CP) RETRY ?
YES (DO OCS TESTS)
NO
RETRY ?
YES
PRINT OUT ON LINE RETRY OK TTY MESSAGE
NO
RETRY ?
YES
NO
MARK RETRY
SWITCH PC'S
OCS TESTS
RETRY
NO
YES
ERROR ?
YES
NO
BLOCK RETRY ?
NO
(DO BLOCK RETRY)
YES
PC SWITCH ?
NO
YES
PC SWITCH NO. 1 → 6 ACTION CLEAR ON-LINE CS EXCEPT FOR CALL RECORD AND PC MAINT AREA
7 CLEAR ON-LINE CS
MARK OCS OUT OF SERVICE PRINT OUT PC SWITCH TTY MESSAGE
PRINT OUT DIAGNOSTIC TTY MESSAGE
MARK OCS OUT OF SERVICE
PC SWITCH ?
NO
YES
PC SWITCH NO. 1 → 2 ACTION PUT CURRENT CS INFORMATION IN ON-LINE CS
3 → 6 IF CA IS ON TS THEN CLEAR TS IF NOT
4 & 6 PUT DUPLICATE CS INFORMATION IN ON-LINE CS
3 & 5 PUT CURRENT CALL RECORD AND PC MAINT AREA IN ON LINE CS CLEAR OTHER INFO
7 CLEAR ON-LINE CS
PRINT OUT TRANS TTY AND SET CP RETRY
(DO LIS TESTS)
(IST LIS TEST)
(NE
LIS TESTS
FNMON
ERROR ?
YES
NO
SKPMN
COMPLETE (CP) RETRY ?
NO
YES
COMPLETE (CP) RETRY ?
NO
YES
BLOCK RETRY ?
NO
YES
PRINT OUT DIAGNOSTIC TTY MESSAGE
SET UP IST TEST OF FAILING BLOCK
LIS FAIL WITH NO PC SWITCH
NO
YES
MARK "IST PC SWITCH FROM LIS" SWITCH PC'S
MCR IN BOTH CS'S COMPARE
NO
YES
PRINT OUT TTY MESSAGE
PREPARE FOR NEXT
OUT

EOSTC is used to start the on-line PC tests which are performed on every scan exactly as if this were a normal PC maintenance scan. Then the first per scan on-line test is performed. A decision (not shown) as to whether retry is in progress is made after the test. The next per scan test is performed because this is a retry. The same action takes place after each on-line PC test.

3.04 The on-line CS tests are performed after the on-line PC tests are completed. First, the eight column tests of matrix 1 are performed. Then the eight row tests of matrix 1 are performed. Matrices 2 and 3 are tested in the same way, and then the on-line CS output test is performed. A failure of any on-line test results in a PC switch either through the 2-second time-out or because the retry had failed.

3.05 If all tests are successful during the on-line retry, a TTY message to this effect is printed out and PC maintenance will continue as for a complete retry.

C. Complete Retry

3.06 A complete (CP) retry consists of an on-line retry followed by a retry of all off-line tests. The decision "CP Retry?" following the on-line CS tests is used to enter the OCS tests during a CP retry.

3.07 The OCS tests include all column and row tests of matrices 1, 2, and 3 and the OCS output test. Fig. 3 is an equivalent representation of the OCS retry and failure path structure of the OCS tests. If any OCS test fails, the failure is noted so that a column, row, or output printout can be made after all OCS tests have been performed.

3.08 Two courses of action are taken at the completion of the OCS retry, depending on whether the OCS tests failed or not. If no error occurred during the OCS tests, the LIS tests are started. However, if the CP retry is the result of a PC switch, a routine is entered to exchange CS information. During normal call processing, the on-line CS contains current call store information. Periodically, the information in the OCS is updated. This information is called the duplicate call store information. After a PC switch the duplicate call store information is found in the on-line CS (this was the OCS before the PC switch). After the first or second PC switch, the current call store information is put in the on-line CS and the duplicate call store information is put in the OCS.

> ***Note:*** For a PC switch to be counted, the PC must pass all its tests. Also the OCS tests must pass before any information is exchanged.

3.09 All PC switches after the second are considered to be multiple switches. This means that there is a good possibility that the failure is caused by some erroneous information in the call store. After seven PC switches the information in the on-line CS is cleared in an effort to clear the trouble. On the third, fourth, fifth, and sixth PC switches less drastic measures are taken. If after the third, fourth, fifth, or sixth PC switch, the call store address register (CA) contains the address of a time slot, the current call store information is put in the on-line CS. The time slot, whose address was in the CA, is then cleared. The reason for this is that the information in that time slot may have been causing the trouble. If the CA does not contain a time slot (TS) address, one of two other actions is taken. After the third or fifth PC switch, the current call store information is put in the on-line CS, but all areas except the call records and the PC maintenance area are cleared. After the fourth or sixth PC switch, the duplicate information is left in the on-line CS. After the OCS tests are successfully completed, the LIS tests are started.

3.10 If the OCS tests failed, the tests of the OCS block of circuits are performed again (block retry). If the block retry is successful, the LIS tests are performed. If the block retry fails, one of two courses of action is taken depending on whether the CP retry is the result of a PC switch. In both cases the OCS is marked bad, a diagnostic TTY message is printed out, and the LIS tests are started. With the OCS marked out of order, out of service, and in trouble, the reroute list and the lines waiting for a time slot list which are stored in the OCS cannot be used. Therefore, the services provided by these lists are denied. The OCS is tested by the PC maintenance program, but no further TTY messages or retries result from its fail-

ure. When the trouble is cleared, the OCS is still marked out of service until a TTY request puts it back on line.

3.11 If the CP retry was the result of a PC switch and the block retry fails, no attempt is made to exchange call store information. After the third, fourth, fifth, and sixth PC switches all areas except the call records and the PC maintenance area are cleared in the on-line CS. After the seventh PC switch, the entire on-line CS is cleared.

3.12 The first LIS test is performed following the OCS tests during a CP retry. At the completion of this test, FNMON is entered. If the first test was successful, the next LIS test is performed. Each LIS test enters FNMON, and if the test is successful the next LIS test is performed.

3.13 When all LIS tests have been successfully performed, the scan count is set to the first OPC test and PC maintenance is complete for this scan. On the following scan, the program control maintenance is entered with the normal end of scan entry EOSTC, and the on-line PC tests which take place every scan are performed. After these tests have been successfully performed, the first OPC test is started. FNMON is entered at the completion of the first OPC test. If the test is successful, the scan count is set to the next OPC test. On succeeding scans, each OPC test is performed.

3.14 If an LIS test fails, a block retry of the LIS is started. If the block retry fails, a diagnostic TTY message is printed out, the PCs are switched, and another CP retry is started. If an LIS test fails during the CP retry and LIS block retry following the PC switch, the LIS is marked bad and the scan count is set to the first OPC test. The call processing program is denied use of the LIS. If the LIS passes the retries following the PC switch, the OPC (the one used during the failing LIS test) is marked out of service.

3.15 If an OPC test fails, a block retry of the OPC tests is made. The scan count is set to the first OPC test, and the PC maintenance is completed for this scan. On the next scan the first OPC test is performed. On subsequent scans each OPC test is performed, one per scan. If an OPC test fails the OPC block retry, a diagnostic TTY message is printed out and the OPC is marked out of order, out of service, and in trouble. The call processing program is permitted to use the OCS and LIS, but PCs cannot be switched unless trouble conditions in the on line equipment force it or the maintenance man requests it.

4. DESCRIPTION OF INDIVIDUAL END-OF-SCAN TESTS

A. Command Translator Tests

4.01 The command translator tests have the entry TOCT for on-line testing. There are two types of commands used in the No. 101 ESS. One type uses bits 17 through 21 of the program store output register (PSOR). The other type of command uses bits 12 through 21 of the PSOR (see Fig. 4). It will be noted that the first type of command uses translators 1 and 2. These translators generate leads TB0 through TB7 and TA0 through TA3, respectively. This is matrix 1. Fig. 4 shows the commands.

4.02 Some of the spaces in matrix 1 contain commands which are in parentheses. These spaces represent combinations which enable the other five matrices. These other five matrices are enabled by leads TC7 and TC10 through TC13 of translator 5. Bits 12 through 16 and 21 enable translators 3 and 4. These translators are common to matrices 2, 3, 4, 5, and 6.

4.03 Actually a gate is associated with each command. The inputs to these gates are the leads shown. The command translator tests are actually tests of the five translators. The most likely trouble is that one of the gates in the translator will be shorted or its output lead will go open due to connector trouble. The result of a short is possibly having two command gates fire at the same time. For instance (referring to Fig. 4), if the TB0 lead were always grounded due to a shorted transistor in the translator, and the command MRT were given, then the 1BT gate would also fire. If the command CTF were given, the 2BT gate would fire in error. In other words, the four commands which are activated by lead TB0 in the first column of matrix No. 1 would be erroneously activated by any command that used a TA0 through TA3 lead output from translator 2.

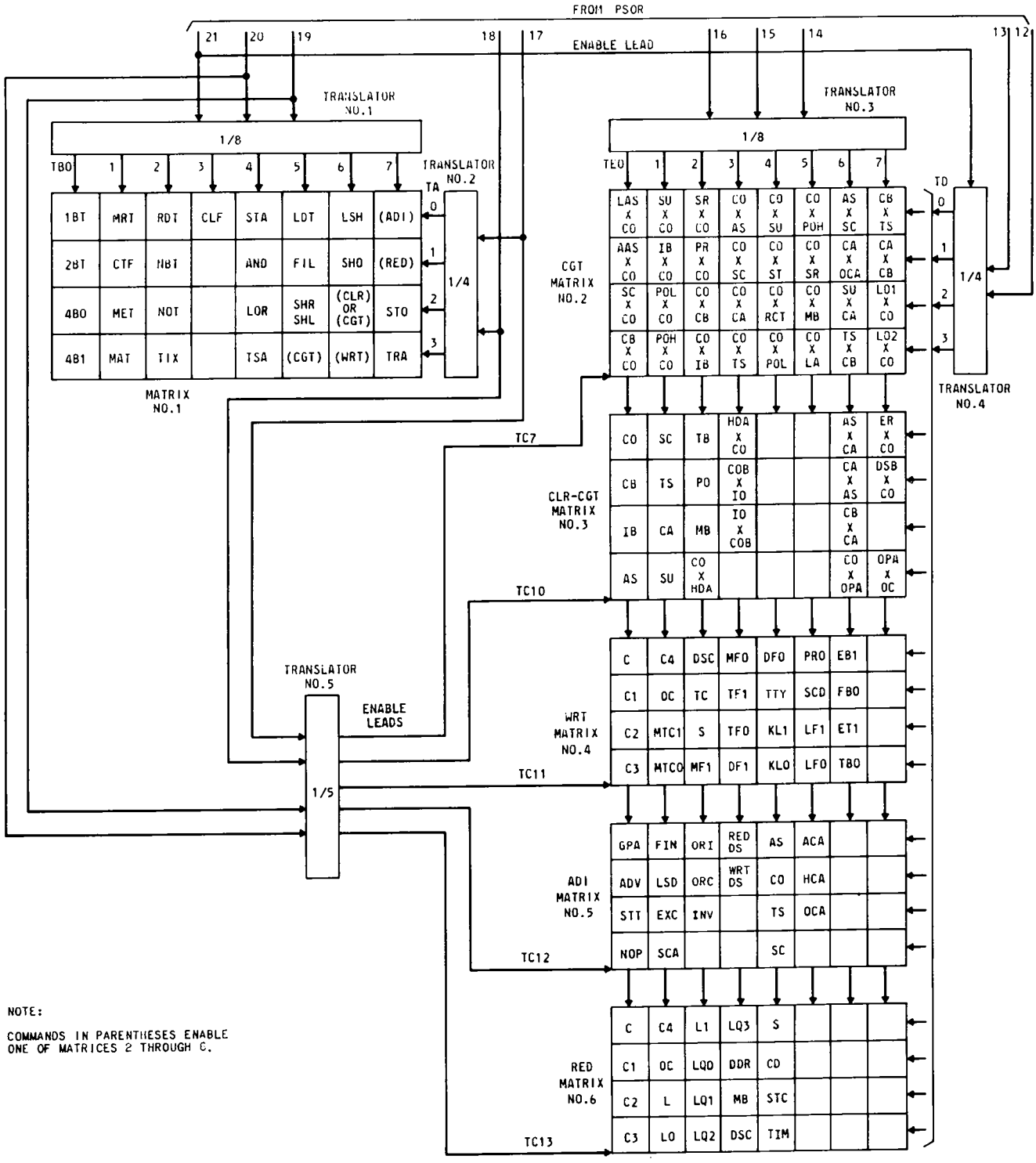


Fig. 4 – Command Translator Diagram

4.04 The command translator tests are set up to detect this type of failure. For instance, the first test is to give a command for a FIL command and to check for the simultaneous occurrence of commands AND, SHR, CGT LAS x CO, and RED C. Looking at Fig. 4, matrix 1, notice that the FIL command is located at coordinates TB5 and TA1. The AND and the RED C (the C occurring in matrix No. 6) commands are both located on row TA1. If leads TB4 or TB7 were permanently grounded, these commands would occur simultaneously with the FIL. The SHR and the CGT LAS x CO commands are both located in column TB5. If the lead TA2 or TA3 were permanently grounded, one of these commands would be erroneously executed with the FIL command. Note that the CGT LAS x CO command is located in the CGT matrix. This matrix is enabled by lead TC7, so actually the lead TC7 is tested for an erroneous ground. Bits 12 through 16 will all be zero so that the CGT LAS x CO command is chosen. The same is true of the RED C command, and here lead TC13 is checked for ground. Of course, this small segment of the test is only testing a small part of these translators. Many more tests are necessary to completely test the matrices.

4.05 The following test is used to check for a simultaneous occurrence of these commands. First the various registers must be set up to detect the errors. For instance, all zeros are written into word C. When the FIL command is given at a later time, the RED C command falsely operated will write all zeros into the CO. Next the add-shift register is cleared. If the CGT LAS x CO command is erroneously given with the FIL command, then zeros will be written into the CO. Next, a test word is written into the CO and the MB. The FIL command is executed and the CO is matched with the incoming message buffer (MB). Since the FIL command does not affect the CO, a match should be made. If any of the four commands mentioned above were executed falsely, the match would not be obtained. The AND command, CGT LAS x CO command, and the RED C command would all write zeros into the test word. The SHR command would shift the test word. If any of these four commands are erroneously executed, the test word in the CO would be changed and a match between the CO and the MB is not made. A WRT EB1 command is generated for the no match condition and will result in a retry of the on-line equipment. If a match is obtained, the testing is continued.

4.06 The TOCT program is used to test the command translators of the on-line PC. This program tests for double translation of commands. The preceding description is a sample of a check for double firing of commands. The PC is set up so that simultaneous occurrence of commands will be picked up when a particular command is executed. Operation of any one of the selected commands indicates a double firing of the command translator. This results in a WRT EB1 command during which bit 1 of the error register is set. This causes a retry of the on-line equipment. A second failure results in a PC switch.

4.07 The COMT1 and COMT2 routines are used for diagnostic checks of the off-line command translator. These programs are used to direct the execution of the TOCT program in the off-line PC. An error in the OPC causes a WRT EB1 command. Since the WRT EB1 command is given from the OPC, it results in bit 3 of the error register being marked equal to a one. This bit is in the on-line error register. The COMT1 and COMT2 programs are designed to check bit 3 to determine if an error has been detected. Detection of an error results in the formulation of a TTY message and in a complete retry. The TOCT routine is broken up into a series of tests. After each group of tests, a marker is generated. This marker consists of a WRT ET1 command. The WRT ET1 command results in setting bit 2 of the on-line error register. After an appropriate number of execute commands are counted, the COMT1 and COMT2 routines look for a marker. These markers also serve as a guide to which group of tests has been performed successfully and which group has failed. This information is used to generate the TTY message. The COMT1 routine checks matrices 1 and 2 of the command translator. The COMT2 routine checks matrices 3 through 6.

B. Command Logic Tests

4.08 The on-line command logic tests are performed by the routines TX1 and TCNS1. A failure of either results in a WRT EB1 command. Bit 1 of the on-line error register is set. This causes an on-line retry.

4.09 The off-line command logic tests are performed by the routines TAA (command logic), TMET (match logic), TCNT (counter logic), and TADV (advance logic). The on-line PC directs the execution of the command logic programs in the OPC. A test failure results in a WRT EB1 command being executed in the OPC. This causes bit 3 of the on-line error register to be set. The on-line program checks this bit periodically. If it is set, a transient failure TTY message is formed. At the completion of the test the FNMON routine is used to print out the TTY message and to enter the CP retry mode. The TAA and TMET routines are used by the on-line PC to execute the TX1 routine in the OPC. The TCNT and TADV routines are used to execute the TCNS1 routine.

4.10 The TAA off-line program of command logic executes approximately half of the TX1 commands. First, the gating of the program store output register is checked. This tests the ability to gate from the left-hand side of the program store output register to the right-hand side. Commands which are complementary in binary number are gated from the left- to the right-hand side of the output register to ensure that this very important gating function is working properly.

4.11 Next, the FIL command is checked to ensure the ability to change bits 6 through 10 of the address for conditional transfers which require this large a change. Bits 12 through 16 of the program store output register are stored in the transfer buffer. When a conditional transfer command is received, the contents of the transfer buffer are gated to bits 6 through 10 of the address register checking this function.

4.12 The conditional transfer commands are checked for their ability to transfer upon the proper conditions and to not transfer when those conditions are not present. When a conditional command is checked for its ability to transfer, all the other conditional transfer command conditions are set for no transfer. Then a conditional transfer is checked to ensure that it does not transfer when conditions are not met.

4.13 Next the TX1 command is tested under transfer conditions and ***not transfer*** conditions. The function of the TX1 command is to gate bits 12 through 16 of the program store output register to bits 1 through 5 of the program store address register, provided the time slot counter is greater than 2. If the time slot counter is less than 2, the next sequential instruction is executed. It is not necessary to set the time slot counter to all possible configurations since the logic which recognizes a count greater than 2 is simplified. If any bit from 3 through 6 is a one, the condition is satisfied. Four conditions are used to detect this. They are making the TS equal to: 100000, 010000, 001000, and 000100. If the two low order bits are both one, the condition is also satisfied. The TS counter is set to 000011 to check this condition. Two words are used to check the conditions which do not satisfy the requirements for transfer. They are the TS equal to: 000001 and 000010.

4.14 The rough MET test is actually a part of the match logic. It is performed here to check the transfer apparatus more than to check the match logic circuitry. The function of the MET command is to transfer if bits 1 through 8 of the CO match bits 2 through 9 of the message buffer (MB) and if the bit 10 of the MB is equal to a zero. If these conditions are not satisfied, the next sequential instruction is performed. The rough MET test sets the MB bit number 10 equal to a zero and then sets all ones in the CO and in the corresponding bits of the MB. This condition should cause a transfer. Then all zeros are placed in the CO and the MB, and the MET command is performed again. This condition should also cause a transfer. Nonmatching words are placed in the CO and then the command is tested for not transferring. This tests all the circuitry involved in the transfer itself and about 60 per cent of the circuitry in the match circuit. A more complete test of the match circuitry is performed in the TMET (match logic) program which will be discussed later.

4.15 Next the shift control counter is tested for proper operation. The philosophy of this test will be discussed in the counter tests (see Part D).

4.16 The program shift register circuitry including the CO and the shift control logic is tested next. Three commands are used to check this circuitry: the shift (right) to zero (SH0) command, the shift right (SHR) command, and the shift left (SHL) command. The function of the SH0 command is to shift the binary word to the right until either a zero appears in bit 1 of the CO or until the number of shifts which had appeared in the shift control counter have been executed, whichever occurs first. Test words are placed in the CO, and SH0 commands are given. The command is checked to ensure that the proper number of shifts have taken place. The test words are chosen so that all possible shift configurations are performed.

4.17 The SHR and SHL commands are used to shift the contents of the CO to the right or to the left by the number of places which appear in the address of the commands. These tests are performed on test words which contain the greatest and least number of alterations between ones and zeros. In the CO, a particular bit is exercised only when the bit being shifted into it is different from the bit which it had previously held. A test word which contains alternating ones and zeros exercises the CO to the greatest extent. One which contains all ones or all zeros exercises CO to the least extent.

4.18 The 4B1 and the 4B0 commands are tested next. The 4B1 command is tested for a transfer condition when the four low order bits of the CO are all ones. It is tested for a not transferred condition when the four low order bits of the CO equal 0111, 1011, 1101, and 1110. The 4B0 command is tested for no transfer when the low four order bits of the CO are equal to all zeros. It is tested for transfer when the low four order bits of the CO equal 1000, 0100, 0010, and 0001.

4.19 The NOT and NBT commands are tested next. The NOT command transfers when the CO is equal to all zeros. The NBT command effects a transfer when the call store buffer (CB) is equal to all zeros. Both these commands are tested for no transfer when any single bit of the appropriate register is equal to a one, and for transfer when all bits are equal to zero.

4.20 The AND and LOR commands are tested next. The AND logic causes a CO bit to be reset if the corresponding bit in the program store output register (PSOR) is equal to zero. This is tested by setting the CO to all ones; then an AND command is executed where the address is equal to all ones. A check is made to ensure that none of the bits in the CO have been reset. Then an AND command is executed where the address is all zeros. A check is made to ensure that all bits are reset.

4.21 The LOR logic is used to set a bit in the CO when the program store output register is a one. First, the CO is reset to all zeros, and a LOR command is performed where the address is all zeros. A check is made to ensure that none of the bits in the CO have been set. Then a LOR command is performed where the address is all ones. A check is made to ensure that all the bits in the CO have been set.

C. Match Tests

4.22 The TMET routine (MET – MAT test) is used to execute the second portion of the TX1 program in the off-line store. This test checks the match logic. The comparator circuit is tested in this routine. Two commands, match extension (MET) and match attendant (MAT) commands, are used to activate a comparator circuit.

4.23 The MET command transfers if bit 10 of the MB equals zero, and if bits 1 through 8 of the CO are equal to bits 2 through 9 of the MB. This command is first checked for no transfer with bit 10 of the MB equal to one and with the appropriate CO and MB bits matching. Then the rough MET test is repeated inasmuch as match condition is set up for all zeros in the two registers, and again with all ones in the two registers, the MB 10 bit being equal to zero. The MB then is set to all zeros and tested for a no transfer with the COs equal to all zeros except for a single bit being equal to one. This test is repeated with the single one moved to each of the CO bit positions. Then the MB is set to all ones with bit 10 equal to zero and is compared to the CO where all bits except one are equal to ones.

The single zero is moved to each of the CO bit positions.

4.24 The MAT command function is to transfer when bits 1 through 5 of the CO equal bits 2, 3, 4, 5, 6, and 7 of the MB while bit 10 of the MB equals one. First, the MAT command is tested with matching CO and MB conditions but with bit 10 of the MB equal to zero. The MAT command should not transfer. Then the appropriate bits in the MB and CO are made equal to zero with bit 10 of the MB equal to one. The MAT command is performed to indicate a transfer. Next, tests are made with all bits of the CO equal to zero except for a single bit equal to one while the MB equals all zeros. The no transfer condition is tested for the single one being placed in all active bits of the CO. Then the corresponding bits of the MB and CO are set equal to all ones with bit 10 of the MB equal to one, and transfer condition is tested. Then a series of five tests are used where a lone zero in the CO is tested for mismatch so the MAT command does not transfer.

D. Counter Tests

4.25 The TCNT routine (counter tests) directs the execution of the TCNT1 routine in the off-line store. The add shift counter (AS), the call store output register (CO), and the call store address register (CA) counter are tested during this routine. The discussion which follows also applies to the shift control counter (SC) and the time slot counter (TS) which are actually tested in earlier tests.

4.26 A counter can be completely tested by satisfying the following three conditions: (1) each individual bit must be incremented when all lower bits are equal to one; (2) no bit is incremented if any of the lower bits is a zero; and (3) each bit will count to either zero or one.

4.27 The first test increments the counter when it contains all ones. This tests the ability of each bit to be incremented from a one to a zero. It also satisfies the condition that all individual bits must be incremented when all lower order bits are equal to one (see Table A).

4.28 Table A shows the five tests for a 4-bit counter. The second through the fifth test, test each bit's ability to be incremented from zero to one. They also test that none of the bits will be incremented if any lower order bit is a zero.

E. Advance Command Tests

4.29 The TADV routine (ADV test) executes the second half of the TCNT routine in the OPC. In this routine the SCA command and the advance (ADV) command are checked. The SCA command is used to jam set the call store address register (CA) to the first system scratch location and to execute the next sequential instruction. This command is executed and the CA is checked to make sure that the proper address has been jammed into it.

4.30 The ADV command is a conditional transfer command which performs a great number of operations. The transfer condition is satisfied when the TS is greater than 2. Under these conditions the function of the ADV command is to add one to the 10 high order bits of the CA and to clear the two lower bits of the CA, to decrement the TS by one, to read the call store, to gate bits 2 through 8 of the CO to bits 2 through 8 of the PA, and to jam set the remaining bits of the PA as follows:

Bits 1, 11, 12, and 14 are set equal to zero; and bits 9, 10, and 13 are equal to one.

This effectively sets the program store address register (PA) equal to the address of the proper

TABLE A

FOUR-BIT COUNTER TESTS

	1ST TEST	2ND TEST	3RD TEST	4TH TEST	5TH TEST
Jam Counter to:	1111	1110	1101	1011	0111
Add one:	+1	+1	+1	+1	+1
Result:	0000	1111	1110	1100	1000

progress mark under call processing conditions. An ADV command is executed with the TS greater than 2, and the aforementioned operations are checked.

4.31 Then the time slot counter (TS) is set equal or less than 2, and an advance command is issued to ensure that the PA is jammed set to 60 octal. This corresponds to the address of the end of sector routine.

4.32 A further condition which affects the ADV command is whether the TS is even or odd. When the TS is even, the call store buffer (CB) is checked to ensure that it has been cleared. When the TS is odd, the ten high order bits of the CA are gated to the CB, and the contents of the TS are gated to bits 1 through 6 of the CB. These conditions have been added to the ADV command to aid in programing conference type calls.

F. Call Store Tests

4.33 Each call store must be tested to ensure that its access equipment and its output equipment are working properly. The access equipment consists of three diode matrices. Each matrix is fed by two 1-out-of-8 translators and renders 64 outputs. One such diode matrix is shown in Fig. 5. The active components which are most likely to fail and affect the operation of the matrix are: the translators and their associated transistor switch, the switch diodes, and the matrix diodes.

4.34 If a translator gate has failed in such a way that its transistor switch is held open, the read-write cycle for addresses using that associated row or column will not work. In other words, any memory winding which is fed by this switch will not have current passed through it. Referring to Fig. 5, it can be seen that each switch is associated with a horizontal row of memory windings or a vertical column of memory windings.

4.35 Any translator gate which is affected in such a way that its associated switch is shorted will result in a division of the read or write current, and one of the memory windings associated with the shorted switch will receive current falsely. For instance, if the first row switch is shorted and an address is read which involves the intermediate row switch and the intermediate column switch, there will be a division of current such that the center memory winding will receive current and the top center memory winding will also receive current. Similarly, the switch diode will permit the passage of the read current or the write current it normally blocks when it is shorted. This causes a false read current or a false write current, depending upon which diode is shorted.

4.36 Similarly, shorted matrix diodes allow a division of current such that false read or write currents pass through their memory winding when other locations are addressed. For instance, if the diode in column 8, row 1 which passes the read current is shorted, the associated memory winding will receive some write current every time the eighth column switch is activated for writing. If the write diode in the same location were shorted, it would allow false read currents to course through the memory winding whenever the eighth column switch was fired for reading. Open switch diodes would deny the corresponding row, or column, from receiving drive. Open matrix diodes would deny read or write current to the memory winding associated with them. The exact result from a shorted switch or diode depends upon the margins of the particular system and the division of current. The result may range from double reading or writing to no reading or writing or intermittent reading or writing. The following discussion assumes double reading or writing will always occur.

4.37 With these criteria in mind the CS access tests were designed so that any of this equipment which fails will produce a TTY message. Briefly, the test consists of eight row tests and eight column tests. A row test consists of testing every location in a particular column. Each column switch is handled in this way until eight row tests have been performed. The column tests are the exact converse of this. It can be seen then that each matrix diode is tested twice for a total of 128 tests per matrix.

4.38 The call store has no reserved test locations. Therefore, the desired test addresses contain call processing information which must be saved and restored at the end of each test. Eight addresses are tested at a time. First, the word in each test address is stored in

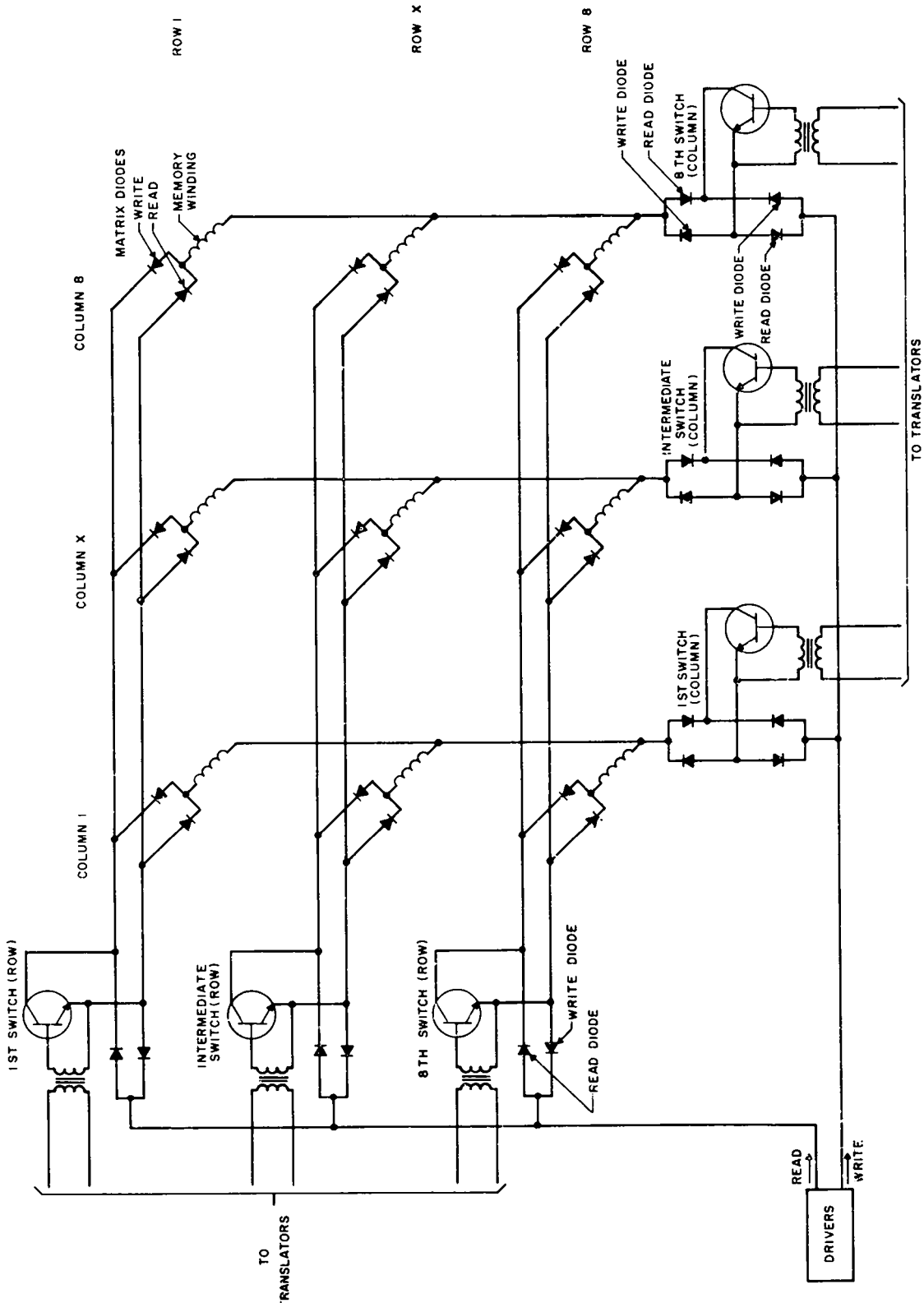


Fig. 5 – Access Matrix for Call Store

a scratch location and a test word is loaded into each test address. There are eight different test words. Next, the store is addressed to the first test address, its word read into the CO, and it is matched against the expected test word which had been placed in the message buffer (MB). A nonmatching condition results in the formulation of a TTY message. Each test word is read from its test address in this manner and the call processing information is restored to them. A complete TTY printout includes the results of eight of these test procedures (tests of 64 addresses). In order to appreciate how these tests locate troubles in the equipment listed above, each type of trouble will be considered independently.

4.39 The translator gate and associated switch, when open, will result in an entire row or column indicating a fault. This is because the affected row or column is unable to pass read and write currents and all zeros appear in the CO at the time of test. A shorted switch or associated translator gate is more complicated.

4.40 Assume the intermediate row switch is shorted. When the first test word is written into the store using the first row test, it is also written into the location associated with the intermediate row and tested column. The second word is also written into the intermediate row location when it is placed in the store. After all eight test words have been written into the store, the intermediate row location will contain the last test word. When these test words are read from the store to the CO, the memory winding associated with the intermediate row switch will also be pulsed. This causes the combination of the ones in the first test word and the last test word to appear in the CO, and a mismatch occurs on the first test word. When this result is rewritten into the store, it is also rewritten into the intermediate location. Now it contains a random arrangement which is different from all the test words. Therefore, every test in every row test will be found in error. When the column tests are performed, eight test addresses corresponding to the eight columns are performed for each column test. The column test for the faulty row will pass. The other column tests are marginal, but assuming double reading and writing, will pass.

4.41 Open diodes will result in the affected row, column, or individual crosspoint showing an error due to the inability to read or write properly for those addresses. Shorted diodes are not as predictable. Consider the write diode of a switch. If the eighth row switch write diode is shorted, every row test will insert the proper test words; but when the words are read for testing, the eighth word will be superimposed upon the first word and the first word test will fail. Also, by destructive readout, the eighth word will be destroyed causing the eighth word test to fail. The other word tests will pass. If a switch diode other than the eighth were shorted, only the word test involving that row would fail. This is because the word is destroyed during subsequent read-write cycles before it is tested.

4.42 When the read diode in the eighth row switch is shorted, however, a more subtle discrepancy results. Here the eight row test words are written into the store. The location of the eighth memory winding of the column will receive each test word but will wind up with the proper eighth word written into it at the end of the loading process. When the words are read up to the CO, one might expect that all tests would pass since the proper word appeared in the eighth address at the time of loading. However, after each test address is read, the rewrite cycle writes the test word back into the selected address and into the eighth test address. At the eighth test when this word is read into the CO, a mismatch is found, pinpointing the defective read diode of the switch. Similar results are obtained with column switch diodes with the exception that here the column tests must be applied to pinpoint the shorted diode.

4.43 The matrix diodes have similar effects. Open matrix diodes show a mismatch for the affected crosspoint. Shorted write diodes render failures for the faulty crosspoint. If the faulty crosspoint is associated with the eighth test location, the first and eighth tests will fail. Shorted read diodes render failures of only the faulty crosspoint on both row and column tests.

4.44 The output tests of the CO are simple in comparison to the access tests. First, all zeros are written into a test address and that

address is read. The CO is then checked to ensure that all zeros have been written into it. Each bit is checked individually and if any of the bits contain a one, the exact bit at fault is pinpointed, thereby isolating the defective circuitry. Next, all ones are written into a test address and that address is read into the CO. The CO is checked for an all one condition. Any zero falsely written into the CO will be identified as above. The output tests also test the ability of the store to inhibit the read cycle during WRT C commands.

G. Line Information and Program Store Tests

4.45 The LIS and PS are twistor stores. The basic store unit consists of two 1-out-of-8 translators feeding a plane selection diode matrix and two 1-out-of-8 translators feeding a word selection diode matrix. Each diode matrix feeds a 1-out-of-4096 core matrix. Each core activates four words. One of these four words is selected by the quadrant bits. The PS contains two such units and has a 15-bit address. The LIS contains one such unit and has a 14-bit address. Bits 1 through 6 describe the word selection, bits 7 and 8 describe the quadrant selection, and bits 9 through 14 describe the plane selection. In the PS, bit 15 describes which unit is being used. The LIS and PS are tested using common routines. These routines are broken into four sections: the access test, the plane selection open diode test, the word selection open diode test, and the output tests. Just prior to the PS access tests, a test of the long shift function is performed to verify its operation because it is used in PS tests.

4.46 The access test consists of three parts: the quadrant test, the plane matrix test, and the word matrix test. Tables B, C, and D show listings of the address used in these tests and the bit configuration of the low order 16 bits used in these tests. The quadrant tests require testing four words. These are the last words in each quadrant. First quadrant 0 is read and "STAed" to the CO. The CO is compared with the MB. The test word shown in Table B is divided in two sections. Both halves of this word are the same. One half of this word is placed in bits 2 through 9 of the MB and a MET test is performed. Then the word is shifted eight places and the MET test is performed again. If both MET tests match, the test is successful. The word is then shifted to the right one place in the MB and the second quadrant is tested. A failure of any of these words indicates that the quadrant selection equipment is at fault.

4.47 The plane selection access tests consist of reading test words from a column and a row of the diode matrix crosspoints. Any translator gate which is open will be detected since the test word will not be read from the store. Any shorted translator gate will result in either a double output which will destroy the test word or insufficient drive current to read the word. In any event, all rows or columns will fail except that row or column associated with the shorted translator gate. Note that the seventh row is held constant while the rows are varied and the seventh column is held constant while the columns are varied.

TABLE B

QUADRANT TESTS

OCTAL ADDRESS	STORE LOCATION	TEST WORD (16 BITS)			
	Program Store A				
37477	63A63 (quad 0)	1100	1100	1100	1100
37577	63A63 (quad 1)	0110	0110	0110	0110
37677	63B00 (quad 2)	0011	0011	0011	0011
37777	63B00 (quad 3)	1001	1001	1001	1001
	Program Store B				
77477	127A63 (quad 0)	1100	1100	1100	1100
77577	127A63 (quad 1)	0110	0110	0110	0110
77677	127B00 (quad 2)	0011	0011	0011	0011
77777	127B00 (quad 3)	1001	1001	1001	1001

TABLE C

PLANE MATRIX TESTS

OCTAL ADDRESS	STORE LOCATION	TEST WORD (16 BITS)			
	Program Store A				
03777	07B00	1110	0000	1110	0000
07777	15B00	1110	0001	1110	0001
13777	23B00	1110	0010	1110	0010
17777	31B00	1110	0011	1110	0011
23777	39B00	1110	0100	1110	0100
27777	47B00	1110	0101	1110	0101
33777	55B00	1110	0110	1110	0110
34377	56B63	1110	1000	1110	1000
34777	57B00	1110	1001	1110	1001
35377	58B63	1110	1010	1110	1010
35777	59B00	1110	1011	1110	1011
36377	60B63	1110	1100	1110	1100
36777	61B00	1110	1101	1110	1101
37377	62B63	1110	1110	1110	1110
	Program Store B				
43777	71B00	1110	0000	1110	0000
47777	79B00	1110	0001	1110	0001
53777	87B00	1110	0010	1110	0010
57777	95B00	1110	0011	1110	0011
63777	103B00	1110	0100	1110	0100
67777	111B00	1110	0101	1110	0101
73777	119B00	1110	0110	1110	0110
74377	120B63	1110	1000	1110	1000
74777	121B00	1110	1001	1110	1001
75377	122B63	1110	1010	1110	1010
75777	123B00	1110	1011	1110	1011
76377	124B63	1110	1100	1110	1100
76777	125B00	1110	1101	1110	1101
77377	126B63	1110	1110	1110	1110

TABLE D

WORD MATRIX TESTS

OCTAL ADDRESS	STORE LOCATION	TEST WORD (16 BITS)			
	Program Store A				
37707	63B56	1111	0000	1111	0000
37717	63B48	1111	0001	1111	0001
37727	63B40	1111	0010	1111	0010
37737	63B32	1111	0011	1111	0011
37747	63B24	1111	0100	1111	0100
37757	63B16	1111	0101	1111	0101
37767	63B08	1111	0110	1111	0110
37770	63B07	1111	1000	1111	1000
37771	63B06	1111	1001	1111	1001
37772	63B05	1111	1010	1111	1010
37773	63B04	1111	1011	1111	1011
37774	63B03	1111	1100	1111	1100
37775	63B02	1111	1101	1111	1101
37776	63B01	1111	1110	1111	1110
	Program Store B				
77707	127B56	1111	0000	1111	0000
77717	127B48	1111	0001	1111	0001
77727	127B40	1111	0010	1111	0010
77737	127B32	1111	0011	1111	0011
77747	127B24	1111	0100	1111	0100
77757	127B16	1111	0101	1111	0101
77767	127B08	1111	0110	1111	0110
77770	127B07	1111	1000	1111	1000
77771	127B06	1111	1001	1111	1001
77772	127B05	1111	1010	1111	1010
77773	127B04	1111	1011	1111	1011
77774	127B03	1111	1100	1111	1100
77775	127B02	1111	1101	1111	1101
77776	127B01	1111	1110	1111	1110

4.48 The word selection access equipment is tested in exactly the same way. Note that the test word used is simply incremented by adding one to the MB. This scheme is also used by the programmer to advance the address to the next test. Shorted diodes are also diagnosed by these tests. The shorted diode will cause erroneous readings for both the row tests and the column tests. All tests will fail except those tests associated with the coordinates of the shorted diode. This is the result of the shorted diode depriving drive current to the other crosspoints.

4.49 The open diode tests require a test of all matrix crosspoints (see Table E). The crosspoint containing the open diode will read all zeros into the output register. These tests require that at least one of the bits be equal to one in the test locations but do not require reserved locations. The open diode tests are associated with two routines, 64 tests per routine. One tests the word matrix and the other tests the plane matrix.

4.50 Table F shows the addresses and test words associated with the output tests for the program store and line information store.

TABLE E

OPEN DIODE TEST

TESTS	PROGRAM STORE A		PROGRAM STORE B	
	OCTAL ADDRESS	STORE LOCATION	OCTAL ADDRESS	STORE LOCATION
Word Matrix Open Diode Tests	00300	00B00	40300	64B00
	00301	00B01	40301	64B01
	00302	00B02	40302	64B02
	00303	00B03	40303	64B03
	–	–	–	–
	–	–	–	–
	–	–	–	–
	–	–	–	–
	–	–	–	–
	00374	00B60	40374	64B60
	00375	00B61	40375	64B61
	00376	00B62	40376	64B62
	00377	00B63	40377	64B63
Plane Matrix Open Diode Tests	00700	01B63	40700	65B63
	01300	02B00	41300	66B00
	01700	03B63	41700	67B63
	02300	04B00	42300	68B00
	02700	05B63	42700	69B63
	–	–	–	–
	–	–	–	–
	–	–	–	–
	–	–	–	–
	36300	60B00	76300	124B00
	36700	61B63	76700	125B63
	37300	62B00	77300	126B00
	37700	63B63	77700	127B63

TABLE F

OUTPUT TESTS

OCTAL ADDRESS	STORE LOCATION	TEST WORD				
	Program Store A					
37466	63A54		0000	0000	0000	0000
37465	63A53		1111	1111	1111	1111
37566	63A54		0000	0000	0000	0000
37565	63A53		1111	1111	1111	1111
37666	63B09		0000	0000	0000	0000
37665	63B10		1111	1111	1111	1111
37766	63B09		0000	0000	0000	0000
37765	63B10		1111	1111	1111	1111
	Program Store B					
77466	127A54		0000	0000	0000	0000
77465	127A53		1111	1111	1111	1111
77566	127A54		0000	0000	0000	0000
77565	127A53		1111	1111	1111	1111
77666	127B09		0000	0000	0000	0000
77665	127B10		1111	1111	1111	1111
77766	127B09		0000	0000	0000	0000
77765	127B10		1111	1111	1111	1111
	Line Information Store					
37464	63A52	0	0000	0000	0000	0000	0000
37465	63A53	1	1111	1111	1111	1111	1111
37564	63A52	0	0000	0000	0000	0000	0000
37565	63A53	1	1111	1111	1111	1111	1111
37664	63B11	0	0000	0000	0000	0000	0000
37665	63B10	1	1111	1111	1111	1111	1111
37764	63B11	0	0000	0000	0000	0000	0000
37765	63B10	1	1111	1111	1111	1111	1111

Each quadrant contains a word with all zeros and a word with all ones. Each word is tested to ensure the ability of all bits of the output equipment to assume a zero or one state. These tests show the locations of any defective bits in a TTY printout. All four quadrants are tested since the output equipment is different for all four quadrants.

4.51 The PS requires that these tests be performed twice, one on each half of the store. Two additional addresses are tested to determine the ability of bit 15 to distinguish between the two store halves.

4.52 The test word for all access tests consists of two 8-bit words, and bits 1 through 8 should equal bits 9 through 16. If a failure to

match is detected on either of the two halves but not both, it is assumed that an output test has failed. This guards against the possibility of one bit of the output equipment indicating an access test failure.

H. Gating Tests

4.53 The clear and gate (CGT) commands are tested by using the routines GTST1 through GTST5. The ability to gate ones is tested by gating all ones from register to register. The last register is checked for an all ones condition. A printout indicates which bits are zero if a failure occurs. Then the registers are set to all ones, and all zeros are gated from register to register. A printout indicates which bits are one if a failure occurs.

5. SWITCH UNIT, DATA CONTROL, AND TRUNK MAINTENANCE PROGRAMS

5.01 The switch unit maintenance program tests the switch units on a per sector basis (see Fig. 6). Each switch unit area (sector) of the store contains a maintenance time slot (MTS) which is used to control switch unit testing. Each switch unit, therefore, is tested when its particular sector is being addressed by the program.

5.02 The data control (DC) maintenance program is used to test the input/output equipment which is common to all switch units. This includes the data control, the digit control, the sender control, the data store (DS), the digit receivers (DDR), and the digit receiver connec-

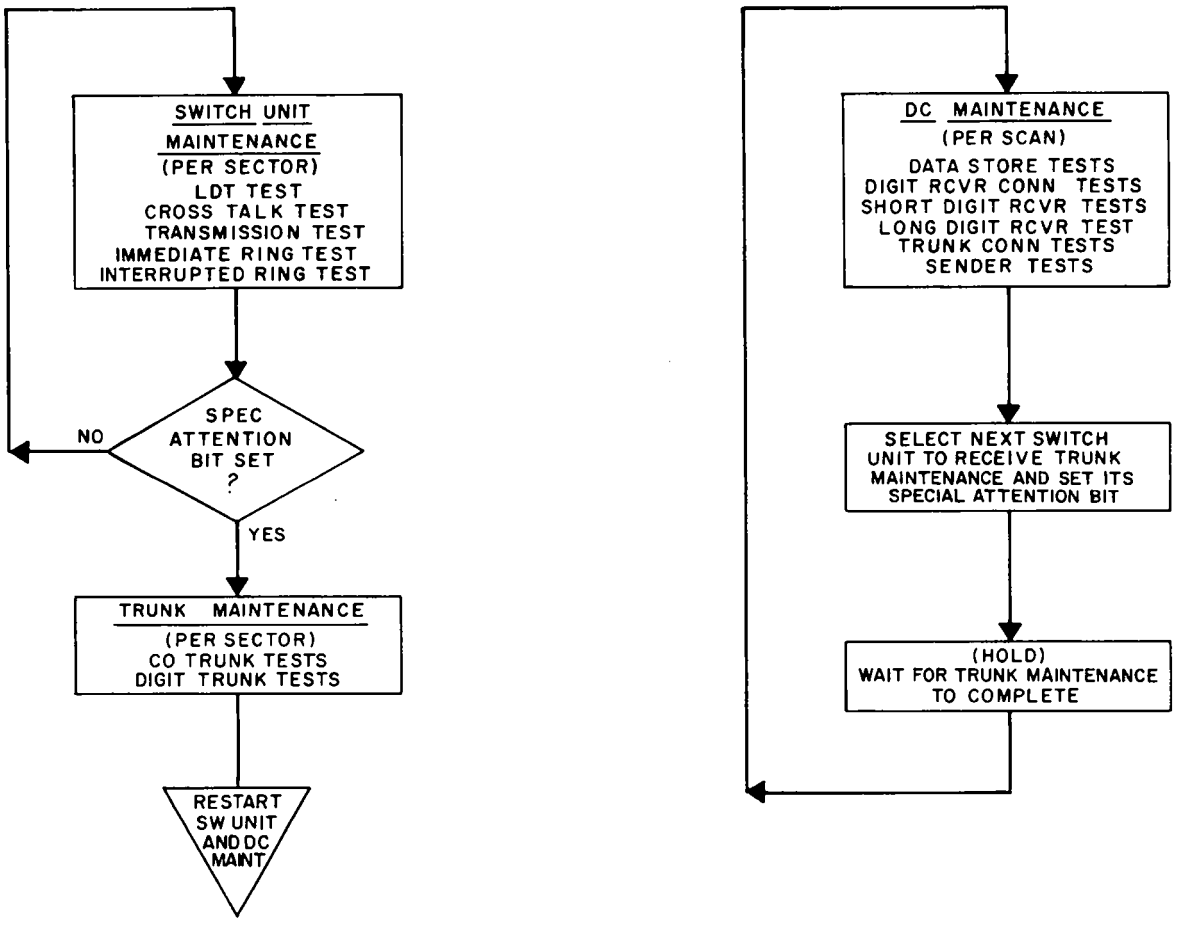


Fig. 6 – Relationship Between Switch Unit, Data Control, and Trunk Maintenance Programs

tors (DRC) as well as the trunk connectors (TC). These tests are performed during the end-of-scan portion of the program. They are independent of the individual switch unit tests.

5.03 The trunk maintenance is used to test the conference circuit, central office (CO) trunks, and digit trunks on a per sector basis. These trunks are associated with particular switch units, but they are not tested as part of the regular switch unit maintenance. Trunk maintenance is performed on one switch unit at a time as directed by the DC maintenance program. At the completion of the DC maintenance cycle, the next switch unit to perform trunk maintenance is selected. The special attention bit in the MTS for that switch unit is set and the DC maintenance waits for trunk maintenance to finish.

5.04 Trunk maintenance will not start until the selected switch unit completes its maintenance cycle and checks the special attention bit in its MTS. The special attention bit being set directs the selected switch unit to go into the trunk maintenance program and perform tests on its CO trunks and digit trunks. When trunk maintenance has been completed, the special attention bit is reset and the switch unit is allowed to start its normal switch unit maintenance.

5.05 While trunk maintenance is going on, DC maintenance is in the hold state. Therefore, time is used during each scan for either trunk maintenance or DC maintenance. When trunk maintenance is complete, the DC maintenance is allowed to start its normal cycle. In this way, trunk maintenance is performed on each switch unit one after the other at the completion of each DC maintenance cycle.

6. SWITCH UNIT MAINTENANCE — SUCCESS PATHS

A. General

6.01 The switch units are tested by sending outgoing messages from the control unit. These messages direct the switch unit to connect test lines to the time division bus in various combinations. The test lines are arranged to give on- and off-hook supervision back to the control unit in response to conditions that they receive from the bus. The on- and off-hook signals reach the control unit in the form of incoming messages. They are examined by the control unit to determine the success or failure of the test.

6.02 Two test lines are used. Test line 1 (the listener) contains one test circuit and is arranged to detect audio signals from the bus and to send off-hook supervision to the scanner when the audio signal is above a certain preset level. Test line 2 contains two test circuits. The first circuit is used to send an audio signal onto the bus and to detect the sampling rate on its time division switch. An indication of proper sampling is an off-hook signal to the scanner. The second circuit is used to detect a ringing signal from the bus. When ringing is present, it sends an off-hook signal to the scanner. By using these three test circuits, it is possible to check over-all operation of the switch unit.

6.03 Switch unit maintenance is entered from the beginning of sector program. The address of the maintenance time slot (MTS) is loaded into the call store address register (CA). The entrance for the switch unit maintenance program is BEGIN (see Fig. 7). BEGIN is a routine which reads the dispatch code from the first word of the MTS. This dispatch code is used by a transfer vector to direct the switch unit maintenance to the proper switch unit test. The start of the switch unit maintenance cycle is the entrance called ENTER. Here a time slot is selected for use throughout this particular switch unit maintenance cycle. The scanner is switched at this time if conditions warrant it.

B. Load Data Trunk Tests

6.04 The first switch unit maintenance test is the load data trunk (LDT) command test. Since the method employed in all switch unit maintenance tests is to send messages to the switch unit, the LDT command is tested first. The LDT command loads the data store with the outgoing message associated with the switch unit under test. The gating paths and logic used by the LDT command and the three words of the data store associated with this switch unit are tested for their ability to transfer and store outgoing message words. An LDT command is given followed by three read data store (RED DS) commands, one for each word of the outgoing message. Each of these words is

RING TEST

TRANSMISSION TEST

TRANSMISSION TEST
T WAIT
(53)

INTERRUPTED RING TEST

INTERRUPTED RING WAIT
INTWT
(06)

2ND INTERRUPTED RING WAIT
INTWT1
(07)

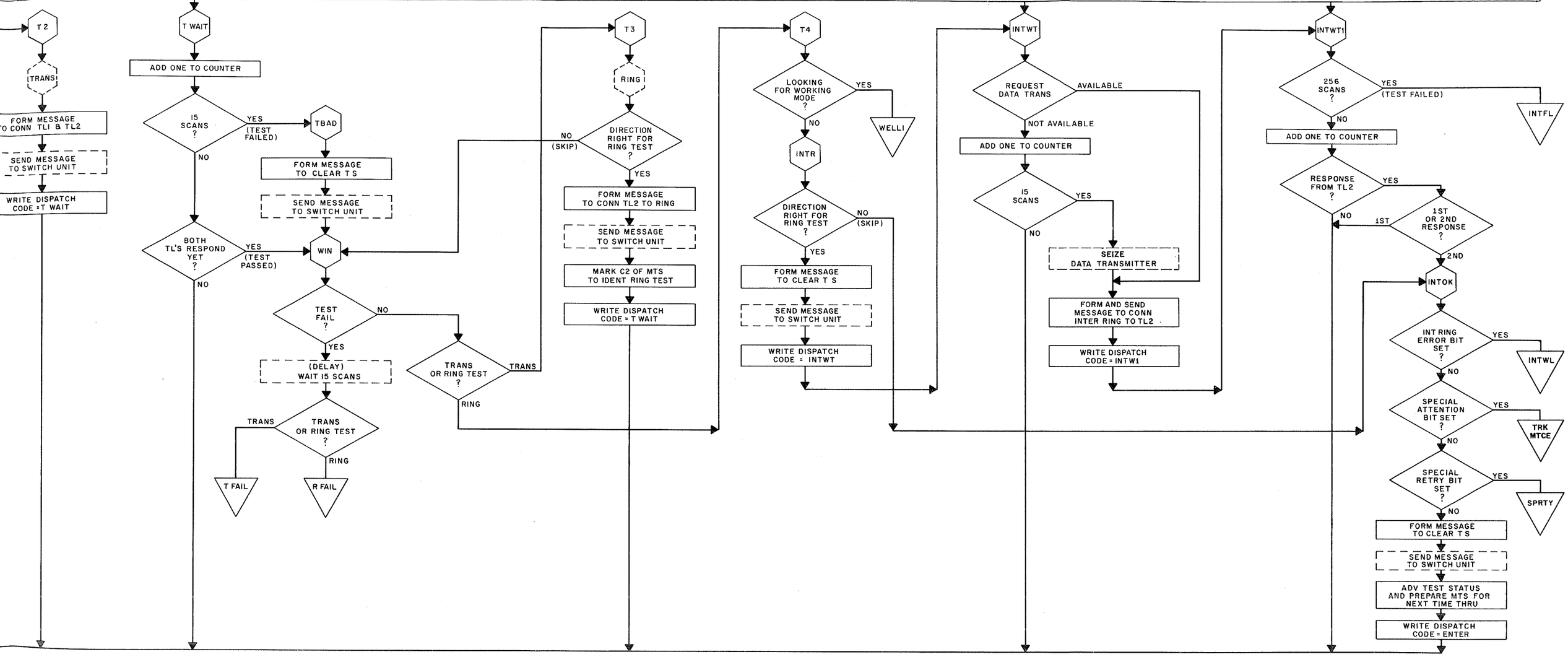
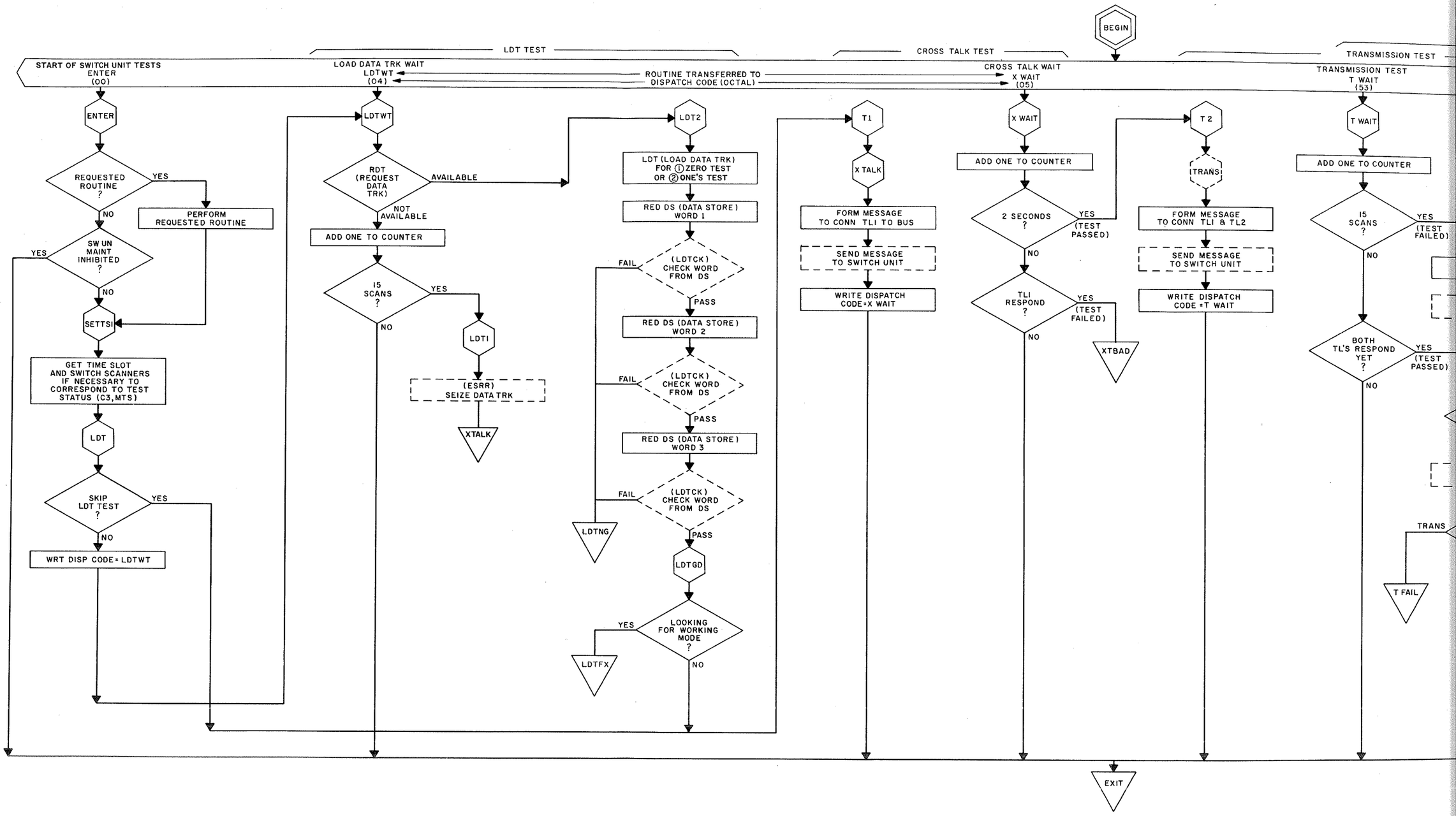


Fig. 7 – Switch Unit Maintenance — Success Paths


BEGIN
LDT TEST
CROSS TALK TEST
TRANSMISSION TEST
START OF SWITCH UNIT TESTS
ENTER
(00)
LOAD DATA TRK WAIT
LDTWT
(04)
ROUTINE TRANSFERRED TO
DISPATCH CODE (OCTAL)
CROSS TALK WAIT
X WAIT
(05)
TRANSMISSION TEST
T WAIT
(53)
ENTER
REQUESTED ROUTINE ?
YES
PERFORM REQUESTED ROUTINE
NO
SW UN MAINT INHIBITED ?
YES
NO
SETTSI
GET TIME SLOT AND SWITCH SCANNERS IF NECESSARY TO CORRESPOND TO TEST STATUS (C3,MTS)
LDT
SKIP LDT TEST ?
YES
NO
WRT DISP CODE = LDTWT
LDTWT
RDT (REQUEST DATA TRK)
AVAILABLE
NOT AVAILABLE
ADD ONE TO COUNTER
15 SCANS ?
YES
NO
LDTI
(ESRR) SEIZE DATA TRK
XTALK
LDT2
LDT (LOAD DATA TRK) FOR ① ZERO TEST OR ② ONE'S TEST
RED DS (DATA STORE) WORD 1
FAIL
(LDTCK) CHECK WORD FROM DS
PASS
RED DS (DATA STORE) WORD 2
FAIL
(LDTCK) CHECK WORD FROM DS
PASS
RED DS (DATA STORE) WORD 3
FAIL
(LDTCK) CHECK WORD FROM DS
PASS
LDTNG
LDTGD
YES
LOOKING FOR WORKING MODE ?
NO
LDTFX
T1
X TALK
FORM MESSAGE TO CONN TLI TO BUS
SEND MESSAGE TO SWITCH UNIT
WRITE DISPATCH CODE=X WAIT
X WAIT
ADD ONE TO COUNTER
2 SECONDS ?
YES
(TEST PASSED)
NO
TLI RESPOND ?
YES
(TEST FAILED)
NO
XTBAD
T 2
TRANS
FORM MESSAGE TO CONN TLI & TL2
SEND MESSAGE TO SWITCH UNIT
WRITE DISPATCH CODE = T WAIT
T WAIT
ADD ONE TO COUNTER
15 SCANS ?
YES
(TEST FAILED)
NO
BOTH TL'S RESPOND YET ?
YES
(TEST PASSED)
NO
TRANS
T FAIL
EXIT

tested to ensure that all bits have been loaded and read from the store properly. Two LDT commands are tested. One outgoing message contains mostly zeros; the other outgoing message is complementary and contains mostly ones.

6.05 It is interesting to note that all the testing up to this point may have taken place during one sector scan or may have required as many as 15 scans. This variation in timing is due to the availability of an outgoing data trunk. The routine called LDTWT is used to accomplish this (see Fig. 7). Note that if the data trunk is not available, the counter located in word 2 of the MTS is incremented by 1. Then the counter is examined to determine if 15 scans have taken place. If 15 scans have taken place, the data trunk is seized and the test is omitted. If 15 scans have not taken place, the program is directed to EXIT (EXIT returns the program to call processing). This technique is used repeatedly throughout the switch unit, DC, and trunk maintenance programs.

C. Crosstalk, Transmission, and Ring Tests

6.06 Next is the crosstalk test, the first test which actually sends a message to the switch unit. Note that after the LDT test has been completed the crosstalk test is entered immediately. A message is formed to connect test line 1 to the bus. An LDT command is then performed to send the message to the switch unit. Once this is done the dispatch code XWAIT is written. The EXIT entry is used to return to the call processing portion of this sector. XWAIT is entered on the next scan in this sector. The counter is incremented by one and checked to see if 2 seconds have elapsed. Note that this test is actually in two parts. The first part, consisting of sending the message, is performed during the same sector as the completion of the LDT test. The second part consists primarily of waiting.

6.07 In this case test line 1 (listener) is connected to a bus with nothing else in the time slot. An off-hook message indicates the presence of crosstalk and failure of the test. If no off-hook message has been received at the end of 2 seconds, the test is considered to have passed.

6.08 The beginning of the transmission test is now started by forming a message to connect test line 1 and circuit one of test line 2 together on the bus. The message is sent, and the dispatch code is written TWAIT. The transmission test consists of sending an audio signal from test line 2 to test line 1. An off-hook message is generated by test line 2 if it is being sampled properly. Test line 1 should be receiving the audio signal, and it should also go off-hook. Therefore, TWAIT is designed to look for responses from both test lines. If it does not receive both responses within 15 scans, the test line is considered to have failed.

6.09 When responses from both test lines are received, the program proceeds to the ring test, more properly called the immediate ring test. This test is only performed on half of the switch unit maintenance cycles. It depends upon the direction of transmission (see 6.11). If the test cannot be performed, the program skips the ring tests. If the test is to be performed, the program waits up to 15 scans for a data transmitter. If at the end of this time, a data transmitter is still not available, the program seizes one and proceeds with the test. A message is sent to the switch unit to connect circuit two of test line 2 with ringing. The dispatch code is again made equal to TWAIT. TWAIT is used for both the transmission test and the ring test. With the ring test, circuit two of test line 2 should go off-hook because ringing is received from the bus. Test line 1 should go on-hook because it has been removed from the time slot and, therefore, can no longer respond to audio signals. Responses from test lines 1 and 2 are required for success of this test. Circuit one of test line 2 also goes back on-hook because it is no longer being sampled, but this response is ignored.

D. Interrupted Ring Test

6.10 When both responses have been received, the program proceeds to the interrupted ring test. A message is sent to connect circuit two of test line 2 to interrupted ring. During this test, it is necessary that both an off- and an on-hook message from circuit two of test line 2 be received within the time of 256 scans. This demonstrates that the interrupted ring is functioning properly. At the successful completion of this test the special attention bit is checked.

If it has been set by the DC maintenance program, the trunk maintenance is entered. If it has not been set, the clean up duties which are required at the end of the switch unit maintenance cycle are performed. These consist of clearing the time slot in the switch unit, clearing the various bits in the MTS in preparation for the next switch unit maintenance cycle, writing the dispatch code ENTER so that on the next scan the test will be started again, and advancing the status of the switch unit maintenance.

E. Test Status

6.11 The three status bits in the MTS determine in which one of eight different modes the switch unit tests are going to be performed. The switch unit has two buses. Either bus can be chosen by selecting an odd or even time slot. The time slot selection takes place during the ENTER routine based on the bus status bit in the MTS. There are also two scanners, but only one scanner is active at a time. The scanners can be switched from the control unit by sending a special message designed for this purpose. The scanner status bit is switched after trunk maintenance has been performed on the switch unit. The scanner is switched during the ENTER routine according to the scanner status bit. The third variable is the direction of transmission. That is, during the transmission test, is test line 1 the A party or the B party? Is the direction of transmission from the A party to the B party or from the B party to the A party? Both directions are used to test the A and B party translators. The scan point numbers of test lines 1 and 2 are complementary to facilitate the testing of the translators.

6.12 At the end of each cycle the direction of transmission bit or the bus status bit is changed, rendering four different combinations of bus and direction modes. The scanner status bit is changed periodically by the trunk maintenance routine. In total there are eight separate modes as determined by the 3-bit status word in the MTS.

7. SWITCH UNIT MAINTENANCE — FAILURE PATHS

A. General

7.01 From the standpoint of failure paths, switch unit maintenance is broken into three blocks (see Fig. 8). The first block consists of LDT command tests; the second block consists of crosstalk, transmission, and ring tests; and the third block consists of interrupted ring tests. The failure paths are entered from a failure of any particular test in the switch unit maintenance. They permit retry of the switch unit maintenance and subsequent switching of equipment in an effort to find a working mode.

B. Load Data Trunk Test Failures

7.02 When an LDT test fails, the entrance LDTNG is used. The retry bit is set and a transient TTY message is printed out, indicating a failure of the LDT command tests. The dispatch code at this point is LDTWT. On the next scan the LDT tests are performed again. If they pass this test, normal switch unit maintenance tests continue. If they fail again, the error bit is set, the 20-minute timer is inhibited, and the CHANGE routine is entered. The CHANGE routine is entered in such a way that the data control (DC) and the program control (PC) will be changed to all possible configurations. First the DC is changed and the LDT tests are performed upon the next scan. Failure here results in a PC switch and another retry of the LDT tests on the following scan. Failing this, the DC is changed back again and on the following scan the LDT tests are performed once again. Failing this, the change routine recognizes that all possible configurations of DC and PC have been made. Therefore, the program is directed to the DIE routine.

7.03 The DIE routine is used when all possible configurations of the control unit affecting this test have been made and none have been found successful. A teletype message is printed out informing the maintenance man of this situation. Maintenance on this switch unit is inhibited. The DIE routine also enables the DC maintenance and maintenance on the other switch units. This is confusing because DC maintenance and maintenance on the other switch units have not been inhibited during this sequence of events. However, the DIE routine is entered from a great number of failure paths, and some of the failures do result in switch unit maintenance being inhibited on all other switch units and DC maintenance being inhibited. In this case, however, trouble with the data store and the LDT command will probably result in

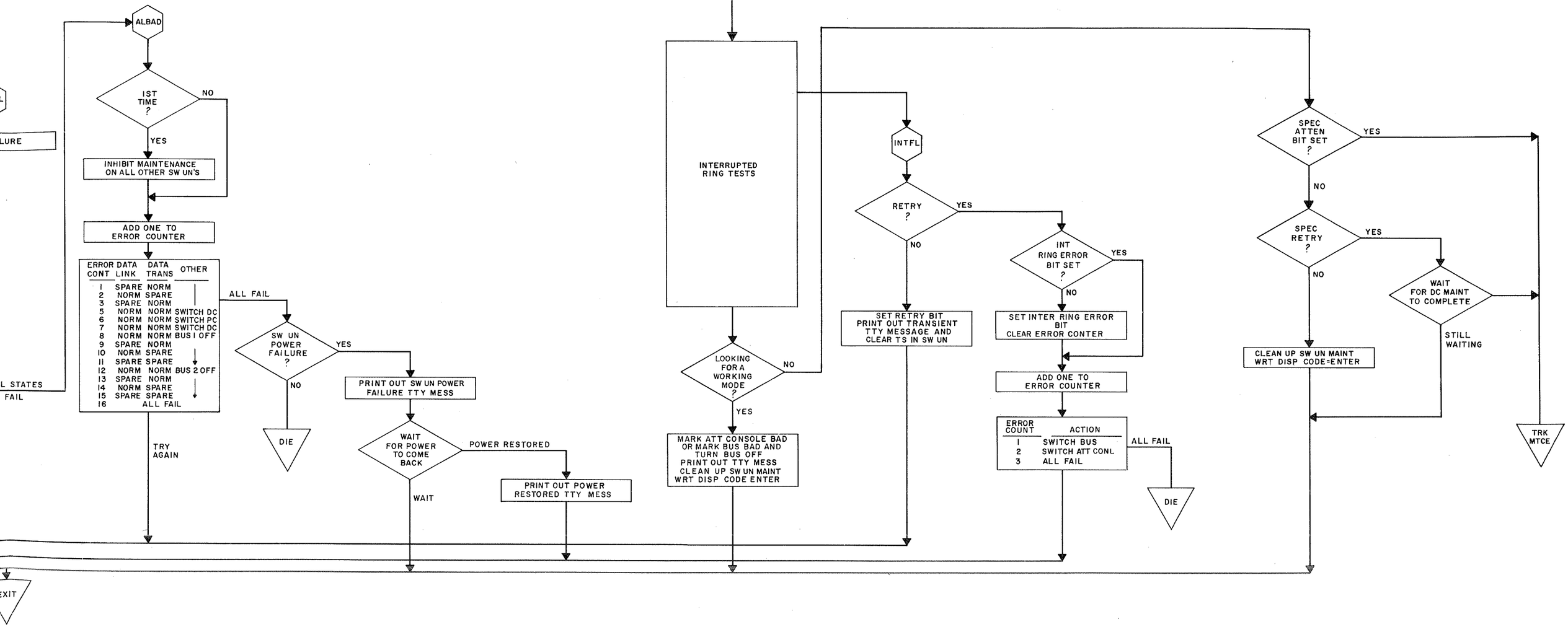
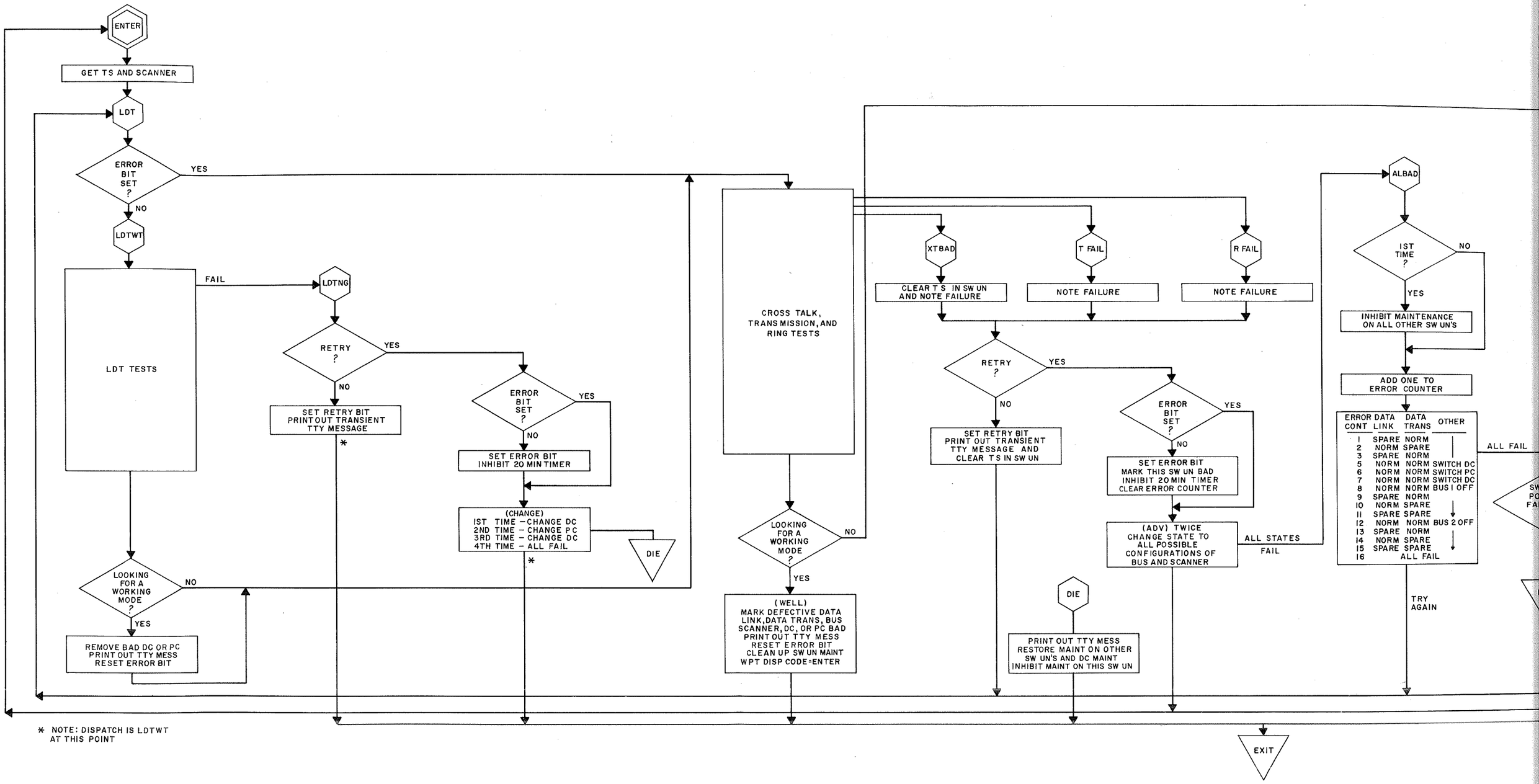


Fig. 8 – Switch Unit Maintenance — Failure Paths



* NOTE: DISPATCH IS LDTWT AT THIS POINT

failures of more than one switch unit since this circuitry is common to all switch units. The DC maintenance also performs tests on the data store so it is desirable, in this case, to let all maintenance continue.

7.04 Usually a working mode will be found before all combinations of DC and PC have been tried. A successful test results in asking the question, "Has a working mode been found?" Actually, this is a decision to determine whether this is a normal successful completion of tests or a successful retry, as distinguished from a successful test where equipment has been switched to achieve this success. Referring to Fig. 8 it will be noted that the error bit is set only when equipment is to be switched. When a working mode is found, it is necessary to identify the bad DC or PC, mark it bad, and send a TTY message to the maintenance man so that he may repair it. After this is done, normal maintenance is continued.

C. Crosstalk, Transmission, and Ring Test Failures

7.05 A failure of the crosstalk, transmission, or immediate ring tests also results in a retry. After the first failure, the retry bit is set and a transient TTY message identifying the failure is printed out. Then switch unit maintenance is started again using the same time slot and scanner. The retry goes to the beginning of switch unit maintenance because the failure could have occurred in the LDT portion of the equipment after the LDT test has been completed. The retry starts at the beginning of all tests because if the failure was due to the data store or the LDT command logic it will be identified as such. If the failure was associated with the crosstalk, transmission, or ring tests and it fails the retry, the error bit will be set, the switch unit marked bad, the 20-minute timer inhibited, and the error counter cleared. Then the advance routine will be used to change the bus and scanner status bits, and the program will be directed to the ENTER routine. Here the time slot or scanner is changed according to the status bits. The error bit being set directs the program to retry the crosstalk, transmission, and ring tests, skipping the LDT test. Each time the block fails, the status is changed until all four combinations of bus and scanner have been tried.

7.06 At this point the program is directed to the ALBAD entry. The first time the ALBAD is entered, maintenance is inhibited on all other switch units. Then the error counter is incremented by 1 and a routine is entered which switches equipment around in 16 different states. The data link and data transmitter spare units are brought into play, the DC is switched, the PC is switched, the power is turned off bus 1, and the power is turned off bus 2. Each failure results in the stepping of the error counter and the switching to a new mode. When all these things have been tried and the failure still occurs, the DIE routine is entered. This indicates total failure of this switch unit. DC maintenance and maintenance on all other switch units are restored. This switch unit is marked bad, its maintenance is inhibited, and a TTY message is printed out to this effect.

7.07 If the crosstalk, transmission, and ring tests find a working mode, the WELL routine is entered and the defective data link, data transmitter, bus, scanner, DC, or PC is marked bad. A TTY message is printed out to identify the bad piece of equipment. The error bit is reset, switch unit maintenance is cleaned up in preparation for a new switch unit maintenance cycle, the dispatch code is changed to ENTER, and call processing is continued.

D. Interrupted Ring Test Failures

7.08 The interrupted ring test tests the interrupted ring logic and is performed as a separate block because a failure can only be cured by switching attendant circuits. Any other failure affecting this circuit would be located by earlier tests. The order of this test then enables it to pinpoint the additional equipment which it tests. The first failure of the interrupted ring test results in the setting of the retry bit and the printing out of a transient TTY message. Then the switch unit maintenance program is directed to the beginning of its tests to retry through the LDT test, the crosstalk, transmission, ring tests, and finally the interrupted ring test. If the other tests are successful and the interrupted ring test fails, the error bit is set, the error counter is cleared and incremented by 1, and a routine is entered wherein the bus and the attendant console are switched. This is because the interrupted ring logic is located in both the bus circuitry and the attendant console

circuitry. First, the buses are switched and the crosstalk, transmission, immediate ring, and interrupted ring tests are performed again. Failure of the interrupted ring tests results in the error counter being incremented and the attendant console being switched. The crosstalk, transmission, and ring tests are performed once more. If the interrupted ring test fails again, the DIE routine is entered indicating total failure of this switch unit.

7.09 If the interrupted ring test succeeds, however, the defective attendant console or the bus is marked bad and a TTY message is printed out pinpointing the defective equipment. Preparations are made to start normal switch unit maintenance testing on this switch unit once more.

8. TRUNK MAINTENANCE — SUCCESS PATHS

A. Conference Test

8.01 Trunk maintenance tests the conference circuit, the CO trunks, and the digit trunks associated with one switch unit (see Fig. 9). Trunk maintenance is entered after the switch unit, which has been selected by the DC maintenance, completes its cycle of testing.

8.02 On the conference test, the program searches for a pair of mating time slots. If they are not available, it skips the conference test and begins the central office trunk tests. When a pair of mating time slots is obtained, a message is sent to connect test line 1 and circuit one of test line 2 for a conference. If the message cannot be sent, the program again skips to the central office trunk tests. If the message can be sent, the program will wait 1 second for a response from listening test line 1. If a response is not received during this time, the test fails (CNFNG). If a response is received, the program proceeds to the central office trunk tests.

B. Central Office Trunk Tests

8.03 The trunk maintenance routine selects a digit receiver (DDR) and a CO trunk. It seizes the CO trunk through the trunk connector circuit and writes the dispatch code equal to TOHWT. On the following scan the off-hook message from the switch unit line pack associated with this CO trunk is expected. If it is not received within 8 seconds, a failure is indicated. When the off-hook response does come, the data store is loaded with a compressed dialed number using the load sender command sequence. The telephone number which is loaded into the data store is that of a special trunk circuit which is located in the central office. This number will be outpulsed to the central office.

8.04 When sending is complete, a sending complete message should be sent to the program control. The trunk maintenance routine waits for this message. If it is not received within 16 seconds, a failure is indicated. When it does come, a further waiting period is initiated. This waiting period is necessary because the test circuit in the central office takes a certain amount of time to respond. When it does respond, it sends a tone out on the central office trunk.

8.05 Test line 1 (listener) is connected at the switch unit to the central office trunk at the end of the waiting period. Test line 1 should go off-hook upon receiving the audible tone from the CO trunk. If this response is not received in 8 seconds, the test is considered to have failed. When it is received, the program checks a special test point in the maintenance center which is activated by the special trunk circuit in the central office. If this test point is set, it is further proof that the proper number has been outpulsed by the sender through the trunk connector to the CO trunk.

8.06 Finally, the program checks the double seize bit. Because the trunk is seized at this time, the double seize bit should be one. If the bit is zero, the test fails.

C. Digit Trunk Tests

8.07 The trunk maintenance is then directed to the digit trunk test. A digit trunk is selected, digit trunk and DDR are connected by the digit receiver connector (DRC), and a message is formed to connect test line 1 to the digit trunk at the switch unit. When this happens, dial tone is given from the DDR through the digit trunk to test line 1. Therefore, test line 1 should go off-hook. The trunk maintenance program waits for up to 15 scans for this response to occur. If it does not occur, a failure is indicated.

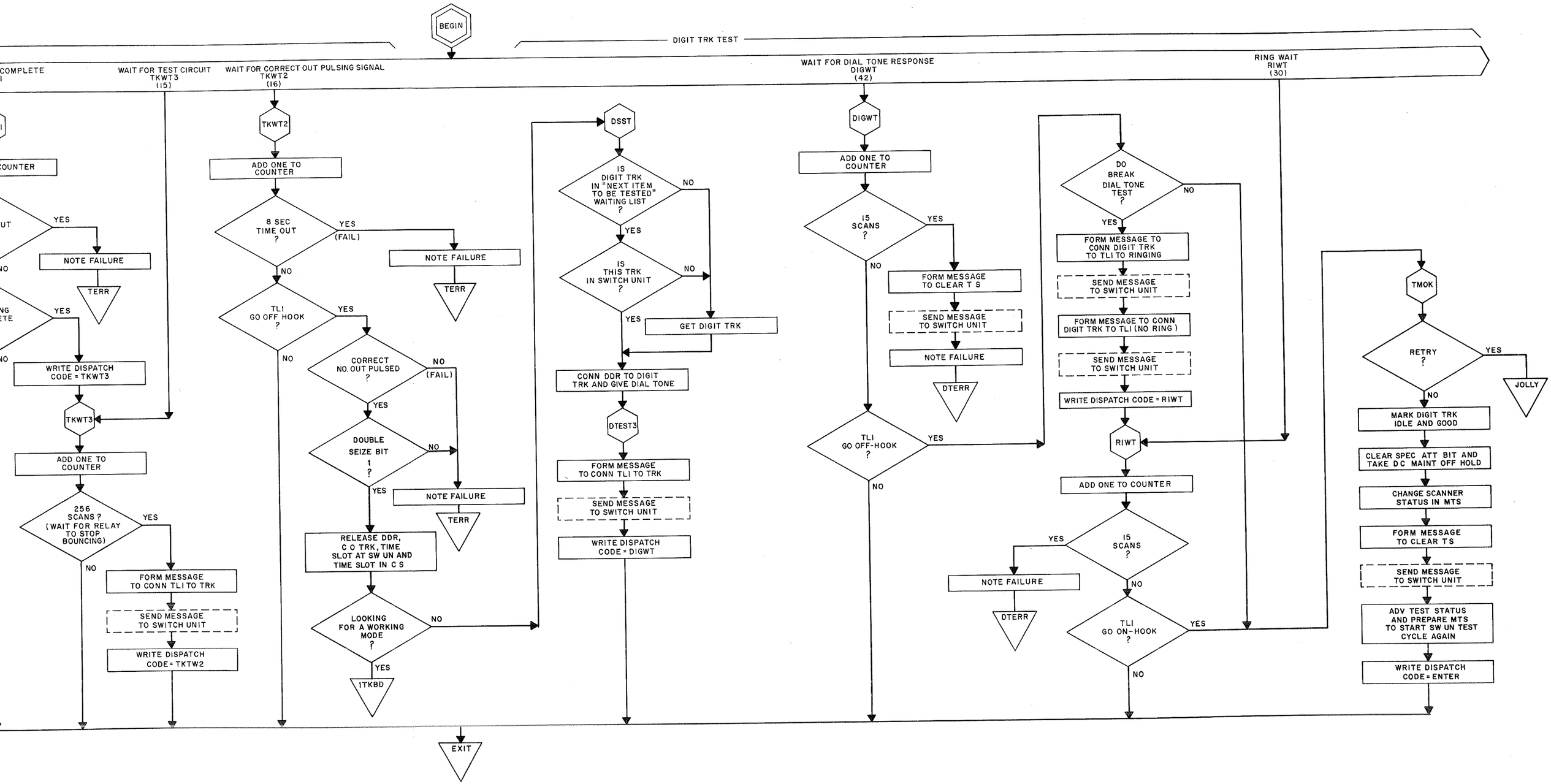


Fig. 9 – Trunk Maintenance — Success Paths

CONFERENCE TEST

C O TRK TEST

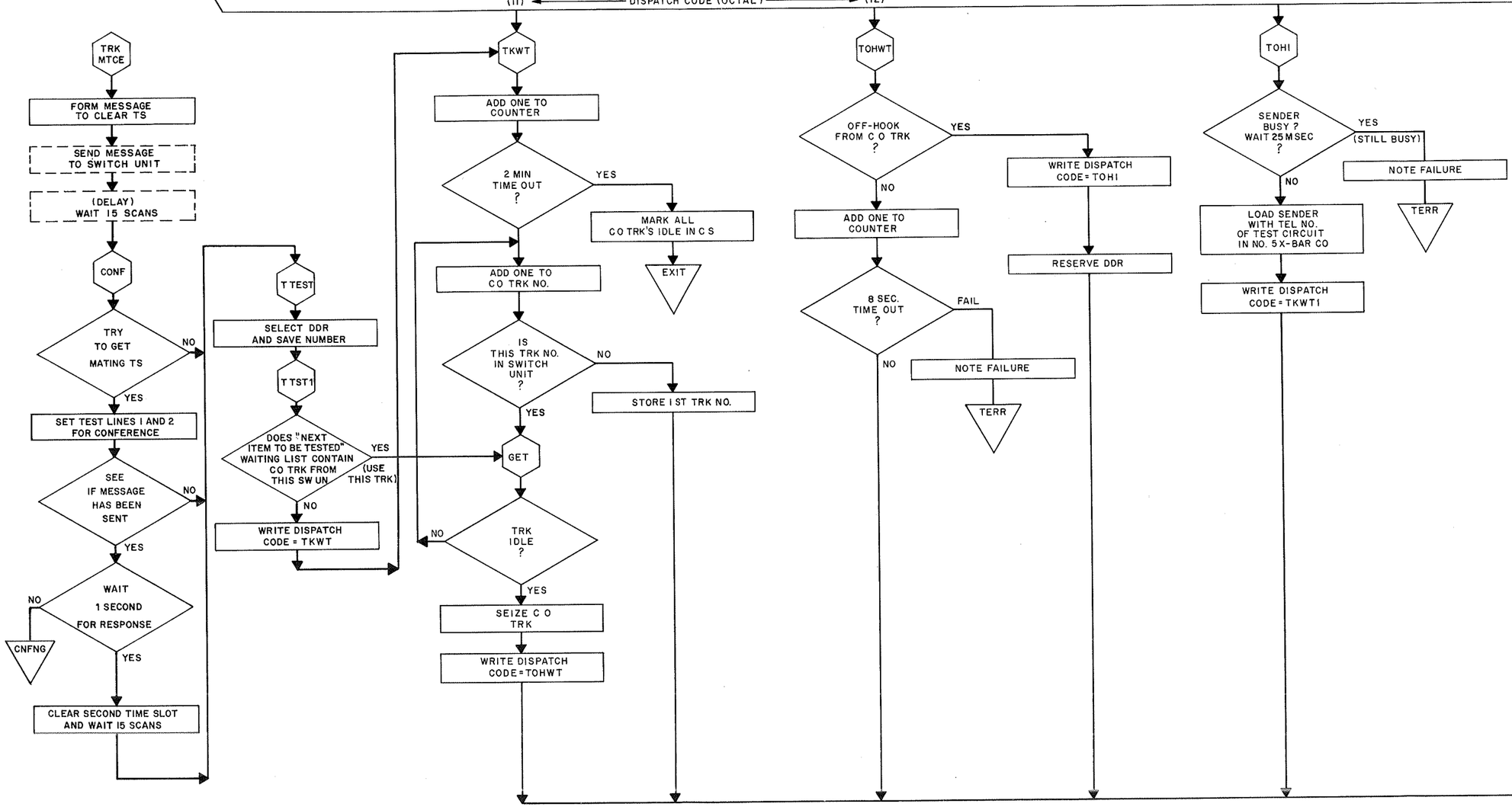
WAIT FOR C O TRK
TKWT
(11)

ROUTINE TRANSFERRED TO
DISPATCH CODE (OCTAL)

TRK OFF-HOOK WAIT
TOHWT
(12)

WAIT FOR SENDER
TOHI
(13)

WAIT FOR SENDING COMPLETE
TKWTI
(14)



8.08 The program determines if the break dial tone test, performed on alternate scans, is to be done. If the test is not performed, the program moves to the end of trunk maintenance. If the test is performed, a burst of ringing is sent in the time slot which connects the digit trunk and test line 1. This is accomplished by sending a message to connect ringing to the time slot and then by sending a message to remove it. This burst of ringing acts like a digit being dialed into the digit trunk and should break dial tone. Test line 1 should, therefore, go back on hook. When it does, trunk maintenance has been successfully completed. At this point, the special attention bit is cleared and the DC maintenance is taken off hold status. The MTS is cleaned up in preparation for this switch unit to start its maintenance cycle once again.

9. TRUNK MAINTENANCE — FAILURE PATHS

A. General

9.01 Trunk maintenance, while testing the conference circuit, the CO trunks, and the digit trunks, uses both the switch unit and the input/output equipment (see Fig. 10). Therefore, when trunk maintenance fails, a retry is directed both to the switch unit maintenance and the DC maintenance. Trunk maintenance uses the special retry bit in the MTS and a special configuration of retry bits in the DCMA to control this retry of both switch unit maintenance and DC maintenance. These bits are set upon the first failure of trunk maintenance, and both the DC maintenance and the switch unit maintenance are started in the special retry mode. The switch unit maintenance is faster than the DC maintenance so at the end of switch unit maintenance the special retry bit is checked. If it is set, as it will be for a special retry, the switch unit maintenance for this particular switch unit goes into a special holding state and waits for the special attention bit to be set by the DC maintenance. When the DC maintenance has been completed, the special attention bit is set and the retry is directed to the trunk maintenance program. If trunk maintenance is successful, the special retry bit is reset during the clean up phase of the trunk maintenance, and all testing proceeds as before. If trunk maintenance fails a test again, an attempt is made to find a working mode without further reference to switch unit and DC maintenance.

B. Conference Test Failures

9.02 If the conference test causes a second failure, the conference denial bit is set, the TTY prints out a failure message, and the program advances to the central office tests.

C. Central Office Trunk Test Failures

9.03 If a CO trunk test causes the second failure, the error bit is set and a retry of CO trunk tests is made with a new CO trunk.

9.04 A third failure results in releasing both trunks at the trunk connector and the switch unit. If the failure was the result of not getting an off-hook message from the switch unit after seizing the CO trunk, the assumption is made that the central office is giving slow dial tone. A TTY message is printed out to this effect and both switch unit and DC maintenance cycles are started again. Any other CO trunk failure results in the error counter being incremented by one. Then the CHANGE routine is entered in such a way that the trunk connector (TC), the DC, and the PC are switched into all possible configurations.

9.05 If the CO trunk test continued to fail for all eight combinations of TC, DC, and PC, the DIE routine is entered indicating a total failure. If a working mode is found, however, the defective central office trunk or trunk connector is marked bad, a printout to this effect is made, and switch unit and DC maintenance are started again.

D. Digit Trunk Test Failures

9.06 If the digit trunk test fails, a special retry is initiated. A second digit trunk failure results in the error bit being set, the error counter being incremented, and the digit trunk test being retried with a new digit trunk. The third failure results in changed DDRs, and the fourth results in changing the digit receiver connectors (DRC). This is accomplished by changing to a DDR in the other DRC. A fifth failure results in changing the DC. At this point the error counter is jammed to seven so that the next failure will produce an error count of eight. A sixth failure results in changing the PC and in jamming error counter to 15. One more failure indicates that all combinations have been tried, and the DIE routine is entered.

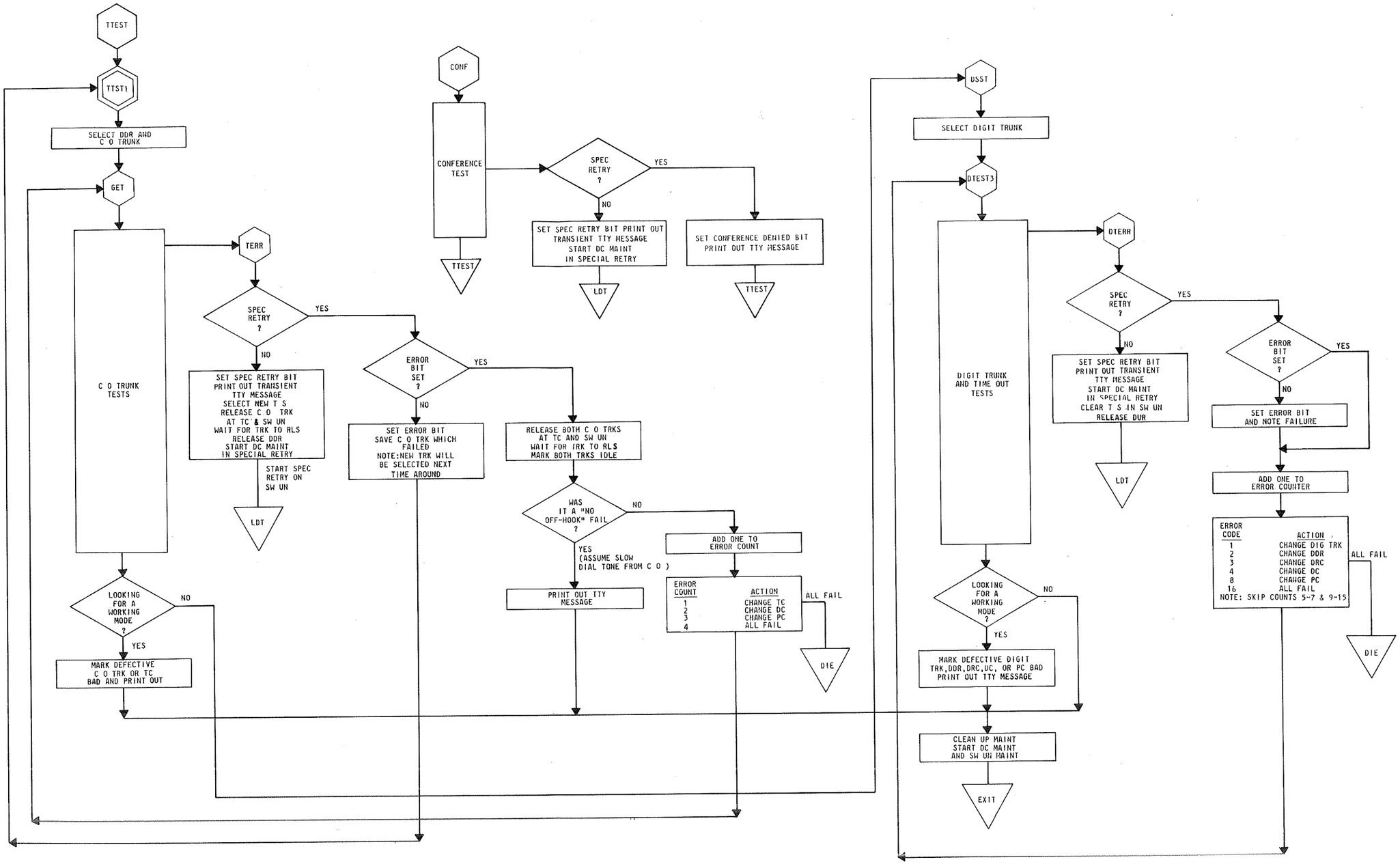


Fig. 10 – Trunk Maintenance — Failure Paths

9.07 If a working mode is found, the defective digit trunk, DDR, DRC, DC, or PC is marked bad and a TTY message is printed out. At this point the switch unit maintenance and DC maintenance are started once again.

10. DATA CONTROL MAINTENANCE — SUCCESS PATHS

A. General

10.01 The DC maintenance tests the data store, the load sender commands, the DRCs, the DDRs, the trunk connector, and the sender. These tests use the same transfer vector as switch unit and trunk maintenance use. The tests are entered at the end of scan maintenance with the FINAL entry which sets the call store address register (CA) to the address of the data control maintenance area (DCMA) and enters the program flow through the transfer vector located at BEGIN. When the control unit is initially turned on, an initialization procedure is performed after the FINAL entry before regular testing is started.

B. Data Store and Interface Tests

10.02 The DC maintenance cycle begins with the START entry (see Fig. 11). The first test uses the RWDs entry and tests the data store and interface circuits. The WRT DS and the RED DS commands are used to load a test word into word 1, DDR No. 0 area of the data store. This is an unused area of the store. The RED DS command is used to retrieve this word and it is compared with the expected value. Then the word is inverted and the process is repeated. This test checks the output of the data store circuitry and the RED DS.

10.03 The ADT1 routine is used to check the address circuitry of the data store and the WRT S, RED S, LSD, and WRT SCD commands. These commands are used to load words 3, 5, and 6 of DDR No. 0 with test words. The RED DS command is used to retrieve the test words and check their accuracy. Then the procedure is repeated using DDR No. 47. This checks the data store address circuitry except for the circuitry associated with bit 8.

C. Digit Receiver Connector Tests

10.04 Following this the digit receiver connector (DRC) is tested. This test makes use of a circuit similar to that used in test line 2 of the switch unit. The test circuits involved are the digit trunk appearances used by the dial pulse generator. These trunks appear on both DRCs, and their digit trunk numbers are complementary. When the time division switches associated with these trunks are fired at the proper rate by the DRC, they activate test points interrogated by the test point reader.

10.05 The DRC tests are performed for both equipped and unequipped digit receivers. The DRC test first checks to determine if the dial pulse generator is connected. It should not be connected at this time. If it is connected, a WRT DSC command is used to tear down the connection between the digit receiver which was last used with the dial pulse generator. The test points are checked again, and if the test points indicate that the dial pulse generator is still connected to a DRC, the test fails. If not, a transient TTY message is printed out and the test is continued. A digit receiver is selected, and it is connected to the dial pulse generator. The test points are interrogated again to ensure that the dial pulse generator is correctly connected. If it is not, a failure is indicated. The preceding routine is performed for all unequipped digit receivers and then for one equipped digit receiver. If the equipped digit receiver passes the test, the program progresses to the next series of tests.

D. Digit Receiver Tests

10.06 Next the DDR tests are performed. Here the dial pulse generator is used to dial various digit messages into the DDR. The DDR stores the digits in the data store by use of the digit control logic. When the digit message is completely received, it is forwarded to the digit completed register (DCR). The program must take this dialed message from the DCR and check it against the digits which were sent out. This entire series of tests is performed once for each of the two dial pulse generator entrances.

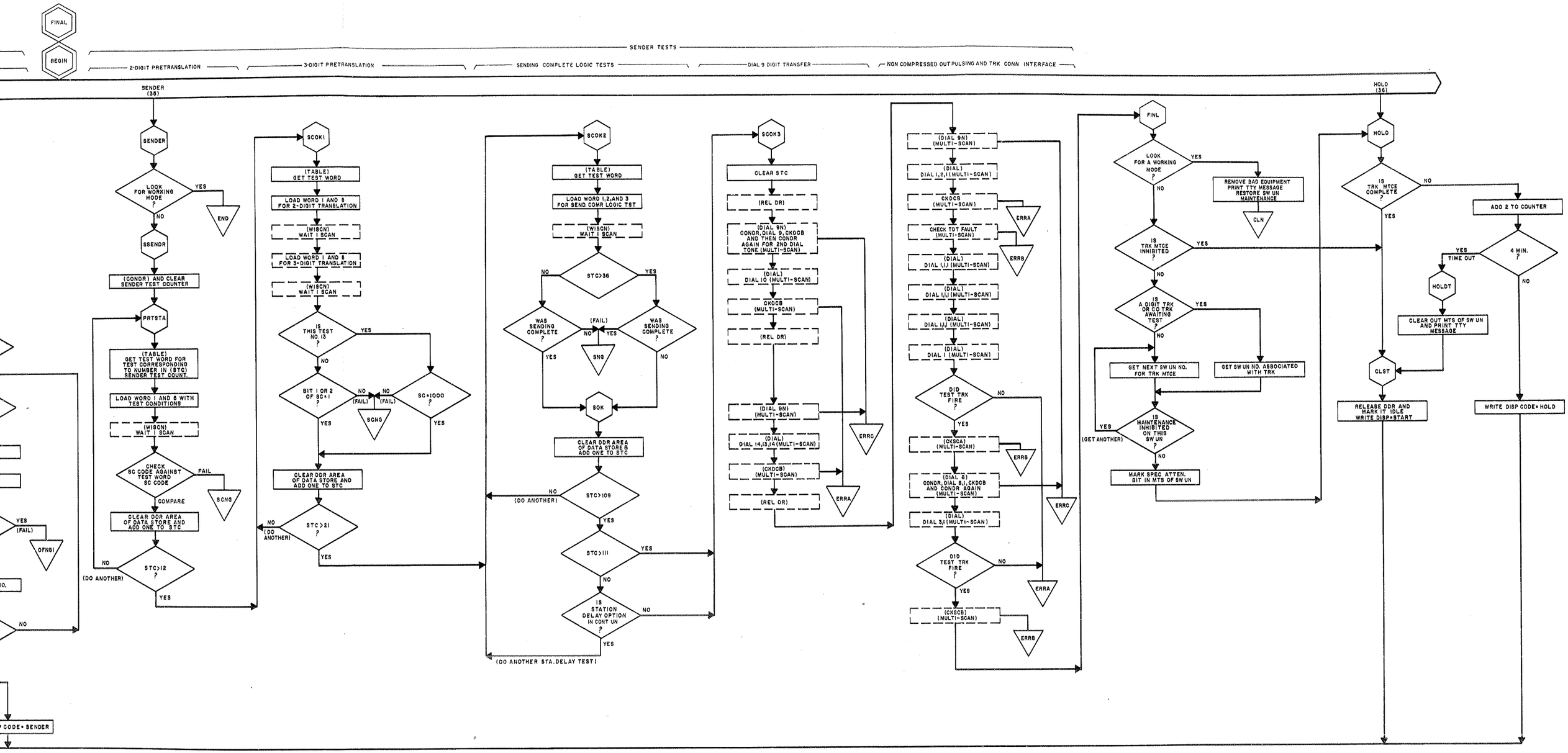


Fig. 11 – Data Control Maintenance — Success Paths

DATA STORE AND INTERFACE

START

REQUESTED ROUTINE ? — YES → REQ ROUTINE

NO

(RWDS) WRT TEST WORD IN DATA STORE & REQ DS REPEAT USING TEST WORD INVERTED (USES DDR NO.0,WORD1) — FAIL → DSFI

(SNSSY) IS SENDER STUCK SSY ? — SENDER STUCK SSY → SSS

NO

(ADTI) PERFORM WRT S,REQ S, LSD, AND WRT SCD COMMANDS TO LOAD WORDS 3,1,&6 OF DDR AREA IN DATA STORE AND CHECK WITH REQ DS COMMAND (USES DDR NO.0 ON 1ST TEST AND DDR NO.47 ON 2ND TEST) — FAIL → NGDS

1ST TEST ? — YES → NO

NO

LOOK FOR A WORKING MODE ? — NO → YES

YES

END

DIGIT REC CONN AND SHORT DDR TESTS

EDRC

DIAL PLS GEN CONNECTED ? — YES (NOT GOOD) — UNEQUIPPED DIGIT RECEIVER

NO

PRINT TTY MESSAGE — YES → CAN IT BE RELEASED ? — NO → FDRC

HAVE ALL BEEN TESTED ? — YES → BDRC

NO

GET A DDR AND CONNECT TO THE D P GEN THEN CHECK TO INSURE THE DIGIT RECEIVER CONN IS SAMPLING THE D P GEN CORRECTLY (MULTI-SCAN) — FDCI

BDRC

DIAL PLS GEN CONNECTED ? — YES (NOT GOOD) — EQUIPPED DIGIT RECEIVER

NO

PRINT TTY MESSAGE — YES → CAN IT BE RELEASED ? — NO → FDCI

GET A DDR AND CONNECT TO THE D P GEN THEN CHECK TO MAKE SURE THE DIGIT REGIEVER CONN IS SAMPLING THE D P GEN CORRECTLY (MULTI-SCAN) — DRC FAILED

PDRC

SHRT DDR TEST

(DIAL) DIAL 9 (MULTI-SCAN)

(CK DCB) CHECK DIALING COMPLETED BUFFER FOR 9 (MULTI-SCAN) — FAIL → DRF

(REL DR)

(CON DR)

(DIAL)247 (MULTI-SCAN)

(CKDCB) (MULTI-SCAN) — FAIL → DRF

(REL DR)

(DIAL)247 (CKDCB) (REL DR) — DRF

LOOK FOR A WORKING MODE ? — YES → DO LONG DDR TEST ON THIS DDR

NO

HAVE 23 SHORT DDR TESTS BEEN COMP ? — NO → DO ANOTHER WITH NEXT DDR

YES → GO TO LONG DDR TEST

LONG DDR TESTS

LODR

LONG DDR TEST
CONDR-DIAL 10-CKDCR-LELDR
THEN CONDR-DIAL 1,6-CKDCR-LELDR
THEN CONDR-DIAL 7,3,DPS-CKDCR-LELDR
THEN CONDR-DIAL 11 -CKDCR-LELDR
THEN CONDR-DIAL 12 -CKDCR-LELDR
THEN CONDR-DIAL 8,9,6-CKDCR-LELDR
THEN CONDR-DIAL 14,9-CKDCR-LELDR
THEN CONDR-DIAL 13 -CKDCR-LELDR
THEN CONDR-DIAL 15 -CKDCR-LELDR
(MULTI-SCAN)

CHECK TIME OUT OF DDR — FAIL → TONG

PASS

LOOK FOR A WORKING MODE ? — YES → END

NO

SPEC RETRY ? — YES → NO

NO

2ND — GO AGAIN WITH OTHER D P G — 1ST TIME THRU ? — YES → EDRC

WAS TEST PERFORMED ON A DIGIT REC CONN WHICH WAS MARKED BAD ? — YES → MARK DRC GOOD MARK ASSOC DDR'S GOOD + IDLE

NO

WRT DISP CODE + TRCT

TRUNK CONNECTOR TESTS

X-POINT TESTS

TRCT (32)

TRCT

CHECK DOUBLE SEIZE FLIP FLOP — SET (FAIL) → DS BNGO

RESET

IS WRT TC OR SENDER LOGIC ACCESS STUCK ON ? — YES → WTCNG

NO

GET TEST TRUNK!

TEST	SW UN NO.	TRK NO.	
1 ST	0	16	RELEASE
2 ND	1	17	
3 RD	2	18	
4 TH	3	37	
5 TH	4	38	
6 TH	5	45	
7 TH	6	64	
8 TH	7	65	
9 TH	24	15	SEIZE
10 TH	25	17	
11 TH	26	18	
12 TH	27	27	
13 TH	28	36	
14 TH	29	45	
15 TH	30	54	
16 TH	31	66	

HAS TEST TRK FIRED ? — NO (FAIL) → XPNG

YES

IS TEST COUNT>8 — YES → RELEASE TEST TRK

NO

SEIZE TEST TRK

HAS TEST TRK FIRED ? — YES (FAIL) → DFNG1

NO

ADD 1 TO TEST COUNT

IS TESTS COMP ? — NO (DO ANOTHER)

YES

WRT DISP CODE + TRCT

RANDOM DOUBLE FIRING TESTS

TRCTA (33) TRCTB (34)

TRCTA

CLEAR SW UN

TRCTB

IS THIS AN ACTIVE SW UN ? — NO → YES

GET 1ST C.O TRK NO. FOR THIS SW UN

DFLI

TRK IDLE ? — NO (SKIP TEST) → YES

YES

SEIZE TRK

RELEASE TRK

HAS ANY TEST TRK FIRED ? — YES (FAIL) → DFNG2

NO

ADD ONE TO TRK

LAST C.O TRK IN THIS SW UN ? — NO (DO ANOTHER) → YES

FINSU

SW UN NO. + >31 — YES → NO

WRT DISP CODE + TRCTB

YES (SKIP TEST)

YES (SKIP TEST)

ERIC

10.07 The digits to be outpulsed from the dial pulse generator are loaded into it one digit at a time. The DIAL subroutine takes as many as three digits and forwards them to the dial pulse generator, one at a time, with a three-scan waiting period between each digit. Another subroutine of the DDR test is the CKDCB which checks the dialing completed register against the expected test digit message. This is a multiscan routine inasmuch as it has a waiting period built into it. The RELDR subroutine is used to send a message to the DRC which releases the DDR and the dial pulse generator connection. The CONDR subroutine connects the DDR to the dial pulse generator through the digit receiver connector.

10.08 There are two DDR tests, the short DDR test and the long DDR test. The short DDR test is performed on 23 DDRs per cycle of the DC maintenance. The last DDR to receive the short DDR test is then given the long DDR test. The short DDR test consists of dialing 9 and then checking the dialing completed buffer (digit completed register) to ensure that the 9 is received. The DDR and dial pulse generator connection is released and then reconnected to re-establish dial tone. A 247 is then dialed and checked. Finally the DDR is released.

10.09 The block labeled ***Long DDR Tests*** in Fig. 11 shows the steps taken to test the ten digit messages of the long DDR test. These tests check the ability of the digit receiver to receive both dial pulse and multifrequency digits. They check the ability of the digit control logic to store and forward digit messages of different types (1, 2, and 3 digit messages).

10.10 The time-out test comes at the end of the DDR tests and checks that system time operates correctly when a DDR is seized and held waiting or seized and used for dialing.

E. Trunk Connector Tests

10.11 Following this, the trunk connector tests are performed. The trunk connector is a translator which allows any CO trunk to be seized or released from either the program control or the sender control circuitry. The gating path from the sender control to the trunk connector circuit is not checked during these tests but is checked during later sender tests. The trunk connector contains three translators. Each distinct combination of leads from these three translators is terminated in an AND gate which sets or resets a flip-flop to either seize or release a trunk. Each AND gate, therefore, has three leads, one from each translator. In order to test the trunk connector, 16 test trunks have been set aside for maintenance purposes. The first eight test trunks have an AND gate on the release crosspoints and nothing on the seize crosspoints. The last eight test trunks have an AND gate on the seize crosspoints and nothing on the release crosspoints. All 16 AND gates are ORed into a test point on the test point reader. These 16 test trunk appearances have been chosen so that each distinct output lead of all three translators will be exercised by using them.

10.12 The trunk connector tests are performed in four groups of tests. The first tests involve the state of the double seize flip-flop. If the double seize flip-flop is set, the test fails.

10.13 The second tests check the access circuits of the trunk connector. If either the WRT TC or sender logic access is stuck on, the test fails.

10.14 The third tests use the 16 test trunks to check that the matrix leads of the trunk connector are neither open nor shorted. Each test trunk has a seize and a release crosspoint. Only one of these crosspoints, for each test trunk, has an AND gate to detect firing of the crosspoint. Eight of the test trunks fire only on release and the other eight fire only on seize. The tests are performed in two parts: a crosspoint test and a double firing test. In the crosspoint test, the test trunk is seized or released as required to cause firing, and the crosspoint is checked to determine that firing did occur. In the double firing test, the test trunk is again selected, but the action (seize or release) applies to the crosspoint which cannot detect firing. Hence, any firing is from another trunk and indicates a failure. When both tests have been successfully completed for one test trunk, another test trunk is selected until all 16 have been used in the tests.

10.15 The last category of trunk connector tests is the random double firing tests. If any lead from any of the three translators in the trunk connector circuit is permanently grounded, multiple firing of the CO trunks will result. If the lead is open, the same condition arises. The double fire test is performed in two modes depending upon whether the switch unit associated with the group of trunks tested is active or spare. With active switch units all idle, central office trunks (tie trunks excluded) are seized and then released. The test points are interrogated to see if any test trunk crosspoint has fired. The test trunks will not normally fire during the tests because they are always marked busy and will be bypassed. After one switch unit has been processed in this way, the next switch unit is processed.

10.16 Eventually, all active switch units will have been processed and the second mode of double firing test begins. Here all CO trunks and all the line trunks with the exception of test trunks are seized and then released. After each seizure and release of a trunk, the test point is checked to determine that no test trunk has fired. When all 56 trunks have been processed, the next switch unit is processed. Note that no switch unit with a number greater than 27 is tested. This is because some types of special tie trunks require an auxiliary trunk appearance. These auxiliary trunk appearances are located in the highest numbered switch units.

F. Sender Tests

10.17 The sender tests check the pretranslator, the sender complete logic circuit, the dial 9 digit transfer feature, the noncompressed dialing out-pulsing circuitry, and the sender control to trunk connector gating paths, all of which are part of the sender control logic.

10.18 The function of the pretranslator is to generate a 4-bit sender complete (SC) code. This code is used by the sender complete logic to recognize when to stop outpulsing. The SC code is generated for 9-type (central office) and 8-type (tie line) calls. The first digit stored, therefore, is always an 8 or 9 when this circuitry is activated. The second digit is examined when the incoming digit position counter (IDPC) equals 0000 or 0001. In processing calls the IDPC always equals 0001 when this takes place. In maintenance testing, however, 0000 is used. The low order bits of the SC code are set according to Table G. The third digit generates the high order bits of the SC code as shown in Table G when the IDPC equals 0000 or 0010.

TABLE G

TWO-DIGIT PRETRANSLATION

2nd DIGIT DIALED	LOW ORDER SC BITS
10 (Zero)	01
1	10
2,3,4,5,6,7,8,9,11 or 0[1]	11
12,13,14 or 15	00
3rd DIGIT DIALED	**HIGH ORDER SC BITS**
10 (Zero)	01
1	10
2,3,4,5,6,7,8,11 or 0[1]	11
12,13,14 or 15	00

[1] Equipment blank (not a dialable digit).

10.19 This process might be called 2-digit translation. On a 9X11-type call (where X equals any digit from 2 through 9) a process called 3-digit translation is employed. Here the SC code after 2-digit translation is 1011. When the fourth digit is registered, it is checked to see if it is a one. With the SC code equal to 1011, if the fourth digit is equal to one, the SC code is made equal to 1000.

10.20 First, the standard 2-digit translation part of the circuitry is checked using tests 1 through 12 as shown in Table H. The method used is to load test conditions into words 1 and 5 of the DDR area in the data store. The test conditions for each test are obtained by using a subroutine called TABLE. Then there is a delay of one scan to give the circuitry time to register the SC code. Then a RED DS command is used to extract the SC code. This code is checked against the expected SC code. The digit receiver area of the store is cleared and the sender test counter is incremented by one. TABLE is consulted again for the conditions of the next test.

TABLE H

TWO-DIGIT PRETRANSLATION TEST CONDITIONS

TEST	2nd DIGIT	3rd DIGIT	IDPC	EXPECTED SC CODE
1	10 (Zero)	10 (Zero)	0000	0101
2	1	1	0000	1010
3 - 8	a[1]	a[1]	0000	1111
9	12	12	0000	0000
10	2	2	0011	0000
11	2	2	0100	0000
12	2	2	1000	0000

[1] a = 2,3,5,8,9, or 0.

TABLE J

THREE-DIGIT PRETRANSLATION TEST CONDITIONS

TEST	2nd DIGIT	3rd DIGIT	4th DIGIT	IDPC	EXPECTED SC CODE
13	0[1]	1	1	0000	1000
14-17	0[1]	1	"a" [2,3]	0000	1011
18	1[2]	1	1	0000	1010
19	10 (Zero)[2]	1	1	0000	1001
20	0[1]	0 [1,2]	1	0000	1111
21	0[1]	1	1	0100[2]	1011

[1] Equipment blank gives same effect as dialed digits 2 through 9.

[2] Condition which does not satisfy 3-digit translation.

[3] Digit "a" = 3,5,9, or 0 (could be 2,4,6,7,8, or 11).

10.21 When the sender test counter reaches a count greater than 12, the 3-digit pretranslation circuitry is checked. The subroutine TABLE is used to get the test conditions for this test. Words 1 and 5 are loaded for the preliminary translation, that is, the 2-digit translation phase. A delay of one scan is initiated to allow the SC code for 2-digit translation to take place. Then words 1 and 5 are loaded with the 3-digit translation conditions (see Table J). After a delay of one scan, the SC code is extracted from the data store and checked to determine if the circuitry has worked properly. On the thirteenth test or the first test of the 3-digit pretranslation, the conditions which satisfy the 3-digit translation are given. Tests 14 through 21 are arranged so that all conditions except one are fulfilled for the satisfactory 3-digit translation. Therefore, in tests 14 through 21, the SC code for the second and third digits should equal the 2-digit pretranslation code.

10.22 Next the sending complete logic test is made. There are 12 sets of AND gates which recognize sender complete conditions. For example, on a 9X11-type call three digits are outpulsed, so when the outgoing digit position counter (ODP) equals 0100, the SC code equals 1000, and bit C9 equals 1, a sending complete signal should be generated. In normal circuit operation this signal is transmitted through the digit completed register. This is a rather time consuming process. In order to facilitate maintenance, a circuit has been developed to set the SR bit when a sending complete signal is generated and the OPR bit equals 0 (this will never happen under normal calling conditions). Therefore, in these tests the conditions for a sending complete signal are set up and the SR bit is checked after a 1-msec wait.

10.23 Three of the twelve sets of AND gates generate a sending complete signal for two different conditions. Therefore, 15 tests (tests 22 through 36) are made which should generate sending complete signals. If the sending complete is not generated, these tests fail. Tests 37 through 109 give conditions where all but one of the conditions for a sending complete signal are given. In these cases, no sending complete code should be generated. Tests 110 and 111 test the station delay option. These tests are skipped if the station delay option is not supplied in the machine.

10.24 Next the digit transfer for an outside call is tested. When a 9 is dialed, it is sent to the dialing completed buffer (digit completed register) to inform the control unit that a 9-type or central office trunk call is coming in. Following this, the next digit, in the case of a zero (operator) call, or the next three digits are sent to the control unit via the digit completed register. The line information store is consulted to determine whether or not the extension making the call is restricted. This circuitry is checked by dialing a 9 and checking that the 9 is forwarded to the digit completed register. Then a zero (10) is dialed and checked in the digit completed register. Following this, a 9 followed by a 14 followed by a 13, followed by a 14 is dialed into the DDR through the dial pulse generator. The 9 is checked in the dialing completed register and then the 14-13-14 is checked in the digit completed register. If either the 9 or the digits which follow are not forwarded to the control unit via the digit completed register, the test fails.

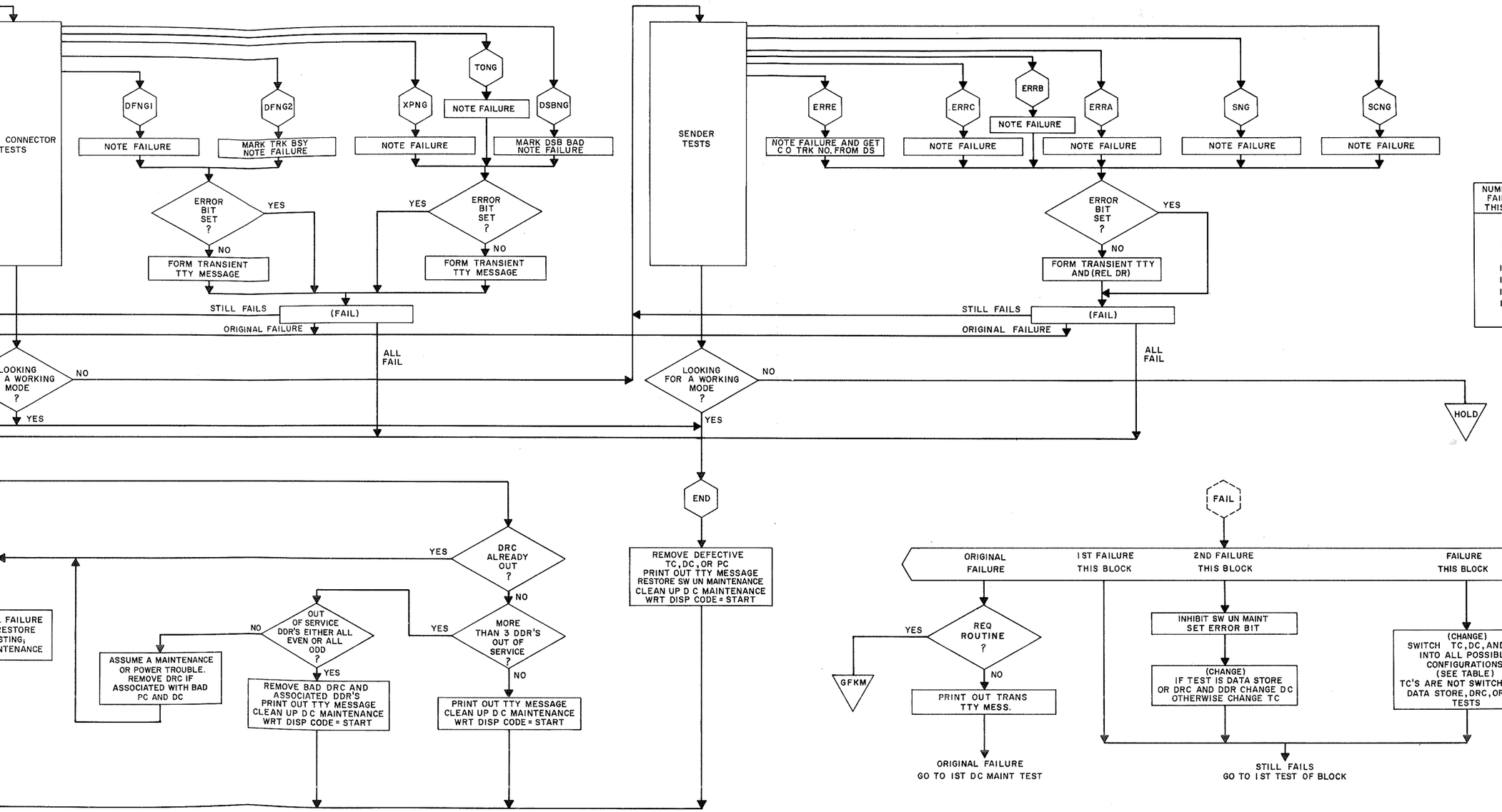
10.25 The last test is the regular sender test and checks the noncompressed dialing outpulsing logic and the gating path between the sender control circuitry and the trunk connector. First the sender is loaded with trunk information and checked to see that it is now busy. If it is still idle, the test fails. A 9-type call followed by 1-2-1, followed by a long string of digit ones is dialed through the dial pulse generator to the DDR. A check is made after the 121 is loaded for correct loading and premature sending complete which could be caused by faulty digit transfer (see 10.22). When all the digits except one have been dialed, the test point reader group is interrogated to determine if the correct trunk number was gated to the trunk connector. The program, when checking for premature sending complete, dials the last digit. Following the success of this test, the digits 8131 are dialed, the sender is checked to see that it is busy, the digits are checked to see that they are correct, the test trunk is checked, and sending complete is checked to see that it occurred at the correct time.

10.26 This completes the DC maintenance testing. Now the next switch unit to receive trunk maintenance is selected. The special attention bit in the MTS of that switch unit is set, and the DC maintenance goes into a hold state. When trunk maintenance is complete, the DC maintenance cycle is started again.

11. DATA CONTROL MAINTENANCE — FAILURE PATHS

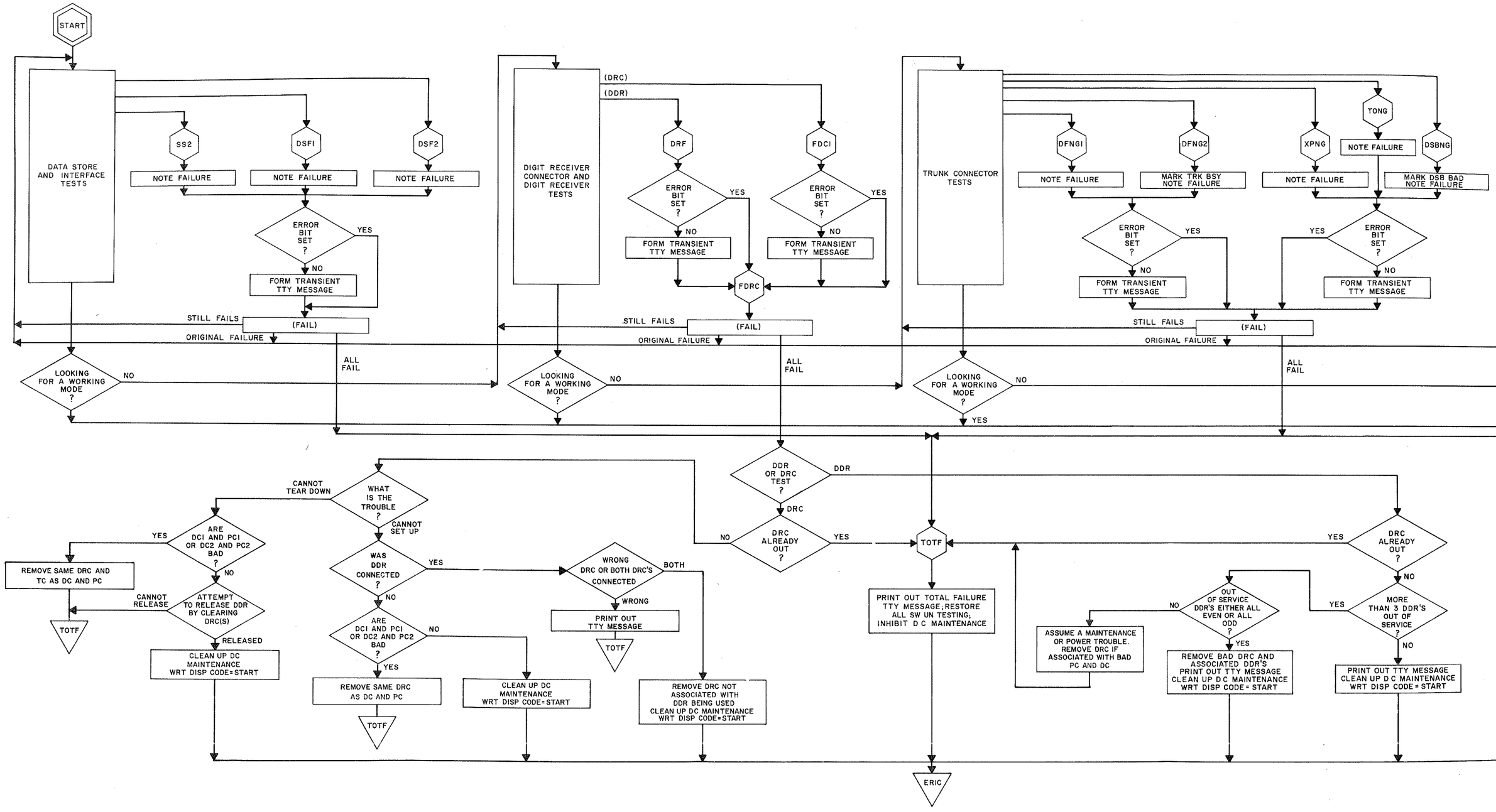
A. General

11.01 For the purpose of failure paths the DC maintenance program is broken into four blocks: data store and interface tests, digit receiver connector and digit receiver tests, trunk connector tests, and sender tests (see Fig. 12). A failure in any block results in a retry of the entire DC maintenance. The need for this is demonstrated by the following example. Assume that while the sender tests are being performed, the data store goes in trouble. Since the sender tests use the data store, a failure will result dur-



NUMBER OF FAILURES THIS BLOCK	DATA STORE DRC AND DDR TEST	TRK CONN AND SENDER TEST	EXAMPLE: TC TEST WHERE TC = DC = PC = 1		
			PC	DC	TC
2ND	CHANGE DC	CHANGE TC	1	1	2
4TH	CHANGE PC	CHANGE DC	1	2	2
6TH	CHANGE DC	CHANGE TC	1	2	1
8TH	ALL FAIL	CHANGE PC	2	2	1
10TH		CHANGE TC	2	2	2
12TH		CHANGE DC	2	1	2
14TH		CHANGE TC	2	1	1
16TH		ALL FAIL	1	1	1
			(ALL FAIL)		

Fig. 12 – Data Control Maintenance — Failure Paths


START
DATA STORE AND INTERFACE TESTS
SS2
DSF1
DSF2
NOTE FAILURE
NOTE FAILURE
NOTE FAILURE
ERROR BIT SET ?
YES
NO
FORM TRANSIENT TTY MESSAGE
STILL FAILS
(FAIL)
ORIGINAL FAILURE
LOOKING FOR A WORKING MODE ?
NO
ALL FAIL
DIGIT RECEIVER CONNECTOR AND DIGIT RECEIVER TESTS
(DRC)
(DDR)
DRF
FDCI
ERROR BIT SET ?
YES
NO
FORM TRANSIENT TTY MESSAGE
FDRC
STILL FAILS
(FAIL)
ORIGINAL FAILURE
LOOKING FOR A WORKING MODE ?
NO
ALL FAIL
TRUNK CONNECTOR TESTS
DFNG1
DFNG2
XPNG
TONG
DSBNG
NOTE FAILURE
MARK TRK BSY NOTE FAILURE
NOTE FAILURE
NOTE FAILURE
MARK DSB BAD NOTE FAILURE
ERROR BIT SET ?
YES
NO
FORM TRANSIENT TTY MESSAGE
ERROR BIT SET ?
YES
NO
FORM TRANSIENT TTY MESSAGE
STILL FAILS
(FAIL)
ORIGINAL FAILURE
ALL FAIL
LOOKING FOR A WORKING MODE ?
NO
YES
DDR OR DRC TEST ?
DDR
DRC
DRC ALREADY OUT ?
NO
YES
TOTF
PRINT OUT TOTAL FAILURE TTY MESSAGE; RESTORE ALL SW UN TESTING; INHIBIT D C MAINTENANCE
ERIC
WHAT IS THE TROUBLE ?
CANNOT TEAR DOWN
CANNOT SET UP
ARE DCI AND PCI OR DC2 AND PC2 BAD ?
YES
NO
REMOVE SAME DRC AND TC AS DC AND PC
TOTF
ATTEMPT TO RELEASE DDR BY CLEARING DRC(S)
CANNOT RELEASE
RELEASED
CLEAN UP DC MAINTENANCE WRT DISP CODE=START
WAS DDR CONNECTED ?
YES
NO
ARE DCI AND PCI OR DC2 AND PC2 BAD ?
NO
YES
REMOVE SAME DRC AS DC AND PC
TOTF
CLEAN UP DC MAINTENANCE WRT DISP CODE=START
WRONG DRC OR BOTH DRC'S CONNECTED
BOTH
WRONG
PRINT OUT TTY MESSAGE
TOTF
REMOVE DRC NOT ASSOCIATED WITH DDR BEING USED CLEAN UP DC MAINTENANCE WRT DISP CODE=START
ASSUME A MAINTENANCE OR POWER TROUBLE. REMOVE DRC IF ASSOCIATED WITH BAD PC AND DC
OUT OF SERVICE DDR'S EITHER ALL EVEN OR ALL ODD ?
NO
YES
REMOVE BAD DRC AND ASSOCIATED DDR'S PRINT OUT TTY MESSAGE CLEAN UP D C MAINTENANCE WRT DISP CODE=START
DRC ALREADY OUT ?
YES
NO
MORE THAN 3 DDR'S OUT OF SERVICE ?
NO
PRINT OUT TTY MESSAGE CLEAN UP D C MAINTENANCE WRT DISP CODE=START

ing the sender tests. A data store failure, however, is identified only during the data store tests. Therefore, if the sender test failure did not result in a retry of the entire DC maintenance, improper handling of this failure would result.

B. FAIL Subroutine

11.02 All tests in DC maintenance use the FAIL routine. Each block is identified by a code (argument) called ARG. Upon failure, the ARG code is stored, identifying the block which failed. The FAIL routine is entered. Using the ARG bits and the three retry bits, the FAIL routine determines which course of action to take (see Fig. 12). On the first failure or the original failure a transient failure TTY message is printed out identifying the test which failed. The DC maintenance is retried starting with the data store and interface tests.

11.03 If the second failure occurs in the same block, the switch unit maintenance is inhibited on all switch units, the error bit is set, the CHANGE routine is entered, and the block of tests which failed is retried. If the original failure was in a different block from the second failure, then the branch shown as "First Failure — This Block" is used to retry this block of equipment. As a result, a block must fail twice to initiate a change of equipment. This also holds true in the case of a special retry initiated from trunk maintenance.

11.04 The CHANGE subroutine is entered in such a way that the trunk connector is not changed for the data store and interface failures or DRC and DDR failures, but it is changed for trunk connector failures and sender failures. (See the table in Fig. 12.) When all combinations of the TC, DC, and PC have been tried, all test blocks except the DRC and DDR test block enter the total failure (TOTF) routine and a total failure TTY message is printed out. All switch unit testing is restored and DC maintenance is inhibited.

C. Digit Receiver and Digit Receiver Connector Failures

11.05 In the case of the DRC and DDR tests an additional step is taken. When the all-fail condition is recognized and a DRC is already out, the TOTF routine is entered. If a DDR has failed, the DCMA is interrogated to see if more than three digit receivers are marked bad. If not, a TTY message indicating that this DDR is bad is printed out. The DC maintenance is cleaned up in preparation to start normal testing again, and a dispatch code is written equal to START so that on the next scan normal DC maintenance continues.

11.06 If more than three digit receivers are bad, they are checked to see if they are all in the same DRC (all even or all odd). If they are, the DRC is assumed to be bad. It is removed from service and its associated DDRs are marked bad. A TTY message to this effect is printed out. The DC maintenance is cleaned up, and the dispatch code written equal to START so that normal DC maintenance can continue on the next scan.

11.07 If more than three DDRs are bad, and they are associated with both DRCs, it will be a case of a power bus failure condition when like numbered TCs, DCs, PCs, and DRCs fail (a fuse trouble or a dial pulse generator trouble). Since the program control maintenance is much faster than the DC maintenance, the DC and PC will be marked bad before the DRC is tested. Therefore, a bad DRC of like number indicates a power bus failure. Recognizing this condition, the DRC, its associated DDRs, the TC, the CO trunks, and digit trunks associated with the bad bus will be removed from service. A power failure TTY message will be printed out, switch unit maintenance will be enabled, and further DC maintenance will be inhibited.

11.08 When the TOTF routine is entered with an indicated DRC trouble, the program determines if a DRC is already out. If it is, a failure printout is made, switch unit maintenance is restored, and DC maintenance is inhibited.

11.09 If a DRC is not already out, the program will act to isolate the failure. The program will act in one of three ways. If the DRC connection was not torn down but can be cleared, the connection will be torn down and DC maintenance cleaned up so that it can continue on the next scan. If a definite trouble exists involving a DRC, the DRC will be removed from service and DC maintenance cleaned up. If a trouble exists

involving both DRCs, switch unit maintenance will be enabled and DC maintenance will be inhibited from further tests.

11.10 In any case, if a working mode is found, the defective TC, DC, or PC is removed from service. A TTY message is printed out, switch unit maintenance is restored in all switch units, and DC maintenance is restarted on the next scan.

12. CONCLUSION

12.01 This is how the No. 101 ESS performs maintenance routines upon itself at a very high rate of speed. When a trouble is found, the defective piece of equipment is switched out of service and teletypewriter messages are provided for maintenance. The program control maintenance does a very precise job in its diagnostic printouts. In the switch unit, DC and trunk maintenance, a large block of equipment is normally involved. In any case, service is restored to the customer by switching the defective equipment out of service.

12.02 It is important to note, however, that most equipment is duplicated. With the exception of DDR, CO trunks, tie trunks, and digit trunks, there are two of everything. Once a failure has occurred, the system is highly vulnerable. If a second trouble develops in the equipment block which has no serviceable counterpart, a complete failure develops. This, of course, means that either one PBX customer is out of service or all PBX customers connected to this control unit are out of service.

12.03 If both PCs are in trouble, the problem is even more difficult. The prime tool to maintain the machine is no longer available. Other types of total failure stop call processing, but at least the maintenance program is available for maintenance. This tool of maintenance programming places a rigid requirement on diagnosing and correcting troubles as soon as possible.