J1H011A SWITCH UNIT DATA RECEIVER CIRCUIT TESTS USING 124A TEST SET SD-1H070-01 NO. 101 ELECTRONIC SWITCHING SYSTEM

1. GENERAL

1.01 This section describes a method for testing the data receiver circuit when there are indications from the control unit teletypewriter or other sources that this circuit is the cause of switch unit failures.

This test should be performed only on the data receiver circuit associated with the off-line bus.

1.02 The tests covered are:

A. Over-All Data Receiver Circuit Test: This test checks all functions of the data receiver circuit. The two timing signals, one to the scanner circuit and one to the data distributor circuit, are tested. Also, a comparison is made between the data signals of the on-line and off-line data receiver circuits using a strobe derived from the on-line circuit. Successful completion of this test assumes the data receiver circuit under test is operating properly and Test B need not be made.

B. Timing Circuit Test: This test checks all the timing logic in the data receiver circuit by using the frequency indicator function of the test set.

Caution: Part of this section requires connections to the on-line data receiver circuit. Use extreme caution when making these connections.

1.03 Certain tests require the assistance of the control unit. Test messages, when required to perform these tests, must be originated by an appropriate ***manual request*** teletypewriter print-in.

1.04 The control unit must be notified whenever an inadvertent disruption of service occurs as a result of testing. This includes blown fuses in both on-line and off-line circuits.

1.05 *Lettered Steps:* A letter a, b, c, etc, added to a step number in Part 4 of this section indicates an action which may or may not be required depending on test conditions. The condition under which a lettered step or series of lettered steps should be made is given in the ACTION column, and all steps governed by the same condition are designated by the same letter within a test. Where a condition does not apply, all steps designated by that letter should be omitted.

2. APPARATUS

All Tests

2.01 124A test set, SD-1H070-01.

2.02 M3BP cord, power cable, 6 feet long (for patching power from switch unit to test set).

2.03 Three W1BD cords (test lead, 8 feet long equipped with test point contact spring and pin plug).

2.04 731A (key, extractor) tool (for CP removal).

3. PREPARATION

STEP	ACTION	VERIFICATION
All Tests		
1	Connect power to test set.	
2	Request control unit print-in test message 1. *Note:* The test message is required to guarantee data traffic for various tests in this section.	

4. METHOD

STEP	ACTION	VERIFICATION
	A. Over-All Data Receiver Circuit Test	
	Note: Proper verification for all parts of Test A constitutes a complete and successful test of the data receiver circuit.	
3	On test set — Connect INPUT C to TP3 at 29C14 (CP254).	
4	Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 800.	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. *Note:* On no verification, proceed to Test B.
6	Move INPUT C to TP5 at 29C14 (CP254).	
7	Operate SYNC DELAY to 40K.	On 0-4 scale — PULSE FREQ reads 0.9 to 1.2. *Note:* On no verification, proceed to Test B.
8	Connect INPUT A to TP2 at 29D8 (CP307).	
9	Connect INPUT B to TP2 at 29D8 (CP307) of other data receiver circuit (located in other bay).	
10	Move INPUT C to TP3 at 29C14 (CP254) of other data receiver circuit.	
11	Operate K1 to COMPARATOR.	
12	Operate SYNC DELAY to 800.	

STEP	ACTION	VERIFICATION
13	Operate RST3 key momentarily	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a bad CP251, 307, or 308 at 29D11, 29D8, and 29D2, respectively. When replacement of these circuit packs fails to give verification, the difficulty may be failure of the timing reset function. This possibility is best checked by substituting, one at a time, the two CP87 cards that receive the reset pulse. These are at 29C20 and 29C23.
14	Remove leads from: TP2 at 29D8 (BAY 1) TP2 at 29D8 (BAY 2) TP3 at 29C14	
15	Request control unit remove test message transmission.	
16a	If no further tests are to be made at this time — Remove test set power connection to switch unit.	
	B. Timing Circuit Test	
3	On test set — Connect INPUT C to TP6 at 29C14 (CP254).	
4	Operate SYNC DELAY to 40K.	
5	Operate K1 to PULSE FREQ.	On 0-4 scale — PULSE FREQ reads 2.0 to 2.1. ***Note:*** No verification indicates a bad CP254 at 29C14.
6	Move INPUT C to TP1 at 29C17 (CP87).	On 0-4 scale — PULSE FREQ reads 0.9 to 1.2. ***Note:*** No verification indicates a bad CP87 at 29C17.
7	Move INPUT C to TP5 at 29C14 (CP254).	On 0-4 scale — PULSE FREQ reads 0.9 to 1.2. ***Note:*** No verification indicates a bad CP254 at 29C14.
8	Move INPUT C to TP3 at 29C20 (CP87).	

STEP	ACTION	VERIFICATION
9	Operate SYNC DELAY to 4K.	On 0-4 scale — PULSE FREQ reads 2.8 to 3.1. ***Note:*** No verification indicates a bad CP87 at 29C20.
10	Move INPUT C to TP3 at 29C23 (CP87).	
11	Operate SYNC DELAY to 800.	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a bad CP87 at 29C23.
12	Move INPUT C to TP3 at 29C14 (CP254).	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a bad CP254 at 29C14.
13	Remove INPUT C from TP3 at 29C14.	
14	Request control unit remove test message transmission.	
15	Remove test set power connection to switch unit.	