J1H011A SWITCH UNIT CLOCK CIRCUIT TESTS USING 124A TEST SET SD-1H070-01 NO. 101 ELECTRONIC SWITCHING SYSTEM

1. GENERAL

1.01 The clock circuit provides timing pulses to the switch store, line number translator, bus clamp and interbus switch, ring-ring-back logic, and data distributor circuits. Therefore, when it is suspected that common trouble exists in these circuits, it is advisable to perform the tests in this section. These tests must also be performed when the control unit teletypewriter indicates clock circuit failure.

Before performing this test, observe the clock failure lamps CLKD1 and CLKD2, which, when lighted, indicate failure of the oscillators in clock circuits 1 and 2, respectively. When CLKD2 is lighted, do not operate S6 key (on transfer and alarms circuit key module). Failure to heed this warning will remove power from clock 1 and disable the complete switch unit.

1.02 The tests covered are:

A. Clock Oscillator Test: This test checks the output frequencies from the two clock circuit oscillators. It also checks the clock transfer functions initiated by the transfer and alarms circuit. In addition, by utilizing the transfer and alarms circuit lamp module, the alarm features of the circuit are tested.

B. Output Pulse Frequency Test: This test checks the frequency of the output pulses appearing on all leads leaving the clock circuit pulse stages.

1.03 The state of two lamps, CLKD1 and CLKD2, located on the transfer and alarms circuit lamp module, is used to indicate the condition of the two clock oscillator circuits. The lamps are automatically lighted on failure of clock oscillators 1 and 2, respectively. However, due to the possibility of faulty equipment in the alarm detecting circuits, partly located on the oscillator circuit packages, an independent frequency check must be made on each oscillator circuit. Therefore, Test A, involving both clock oscillators, must be performed when either clock circuit 1 or 2 is tested.

1.04 Test B may be performed on either clock circuit 1 or 2. It concerns those parts of the clock circuits that are associated with bus 1 or bus 2.

1.05 Control unit maintenance must be notified whenever service interruptions occur as a result of testing. Clock transfers, blown fuses, and any other action producing an alarm message to the control unit must be reported.

1.06 The tests in this section use only the frequency indicator portion of the switch unit test set. The state of all test set lamps should be ignored.

1.07 ***Lettered Steps:*** The letters a, b, c, etc, added to a step number in Part 4 of this section indicate an action which may or may not be required depending on local conditions. The condition under which a lettered step or series of lettered steps should be made is given in the ACTION column, and all steps governed by the same condition are designated by the same letter within a test. Where a condition does not apply, all steps designated by that letter should be omitted.

2. APPARATUS

All Tests

2.01 124A test set, SD-1H070-01.

2.02 M3BP cord, power cable, 6 feet long (for patching battery from switch unit to test set).

2.03 W1BD cord (test lead, 8 feet long, equipped with test point contact spring and pin plug).

2.04 731A (key, extractor) tool (for CP removal).

3. PREPARATION

STEP	ACTION	VERIFICATION
All Tests		
1	Connect power to test set.	
2	On test set — Operate K1 to PULSE FREQ.	
3	Operate SYNC DELAY to 400K.	
4	Request inhibit of switch unit maintenance routine to this switch unit.	

4. METHOD

STEP	ACTION	VERIFICATION
	A. Clock Oscillator Test	
	Caution: When testing the clock oscillator (CP139), use care when making connections to CP139 test points. The circuit under test may be on-line.	
5	Connect INPUT C to TP5 at 37A2 of clock circuit 1 (BAY 1).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a faulty CP139 at 37A2 of clock circuit 1.
6	Move INPUT C to TP5 at 37A2 of clock circuit 2 (BAY 2).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a faulty CP139 at 37A2 of clock circuit 2.
7	Move INPUT C to TP2 at 37A2 (CP139) of clock circuit 2 (BAY 2).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a faulty CP139 at 37A2 of clock circuit 2.
8	On transfer and alarms circuit key module at 25D2 (BAY 2) — Operate S6 key.	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. On transfer and alarms circuit lamp module — CLKD1 lamp lights. ***Note:*** No verification indicates a faulty CP139 at 37A2 of clock circuit 2.
9	On transfer and alarms circuit key module at 25D2 (BAY 2) — Operate S7 key.	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. On transfer and alarms circuit lamp module — CLKD1 lamp extinguished.
10	Remove INPUT C from TP2 at 37A2.	

STEP	ACTION	VERIFICATION
11	Connect INPUT C to TP2 at 37A2 (CP139) of clock circuit 1 (BAY 1).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a faulty CP139 at 37A2 of clock circuit 1.
12	Repeat Steps 8 and 9.	
13	Remove INPUT C from TP2 at 37A2.	
14a	If no further tests are to be made at this time — Remove test set power connection from switch unit.	
15a	Request enable of switch unit maintenance routine.	

B. Output Pulse Frequency Test

5	On test set — Connect INPUT C to each of the following test points, in turn:	
	TP8 at 37A77 TP5 at 37A11 TP2 at 37A11 TP3 at 37A11	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a faulty CP140 at 37A11.
	TP8 at 37A14 TP6 at 37A14 TP2 at 37A14	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a faulty CP140 at 37A14.
	TP3 at 42A14 TP1 at 42A14 TP2 at 42A14 TP4 at 42A14	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a faulty CP20 at 42A14.
6	Remove INPUT C from TP4 at 42A14.	
7	Remove test set power connection from switch unit.	
8	Request enable of switch unit maintenance routine.	