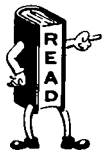
J1H011A SWITCH UNIT SWITCH STORE CIRCUIT TESTS USING 124A TEST SET SD-1H070-01 NO. 101 ELECTRONIC SWITCHING SYSTEM

1. GENERAL

1.01 This section describes a method for testing the switch store circuit when there are indications from the control unit teletypewriter or other sources that this circuit is the cause of switch unit failures.



This test should be performed only on the switch store associated with the off-line bus. This bus must remain powered.

1.02 The tests covered are:

A. Binary Counter Recycle: This test checks for correct recycle period of the binary counter circuit. It also tests the synchronizing pulses developed within switch store 1 only. This is a brief test, designed to verify the operation of the binary counter with respect to those outputs used by the data distributor circuit.

B. Switch Store Input Test: This test checks that the associated data distributor circuit is providing proper signals to operate the switch store circuit.

C. Switch Store Output Test: This test checks the ability of the switch store circuit to provide storage for the input message and also to read out the stored contents at the correct rate. In effect, this test briefly checks the over-all performance of the switch store for a particular time slot address.

D. Clock Pulse Amplifiers: This test checks the clock pulse amplifiers for correctly timed output signals.

E. Binary Counter Stages: This test checks that each binary counter stage advances at the proper time.

F. Horizontal Drive to Memory Array: This test checks the timing of all horizontal driver stages.

G. Vertical Drive with Recirculate Removed: This test checks the ability of each vertical access bit register stage to be set to a 0 or 1 state by signals from the data distributor circuit. It also checks the output driver gates.

H. Vertical Drive Recirculate Test: This test checks the ability of the switch store circuit to destructively read the memory array contents, detect the readout action, and rewrite the same information into the memory array on application of the next write pulse. The scope of this test is limited by the number of time slots to which the message is addressed.

I. Vertical Access to All Time Slots: This test checks the ability of the circuit to store a bit in every time slot of each vertical column. No test messages are required. The bits are placed in the store by a manually placed, momentary ground on the vertical access circuit packs.

Caution: The proximity of the switch store to on-line circuits makes it imperative that extreme caution be used when attaching test set leads.

1.03 Part 4 of this section is chronologically arranged to provide an initial over-all test of the switch store circuit by performing Tests A, B, and C. Subsequent tests examine the circuit in more detail.

1.04 Tests should be made in their order of presentation.

1.05 Certain tests require the assistance of the control unit. Test messages, when required, must be originated by the appropriate manual request teletypewriter print-in.

1.06 The control unit must be notified whenever an inadvertent disruption of service occurs as a result of testing. This includes blown fuses in both on-line and off-line circuits.

1.07 *Lettered Steps:* The letters a, b, c, etc, added to a step number in Parts 3 and 4 of this section, indicate an action which may or may not be required depending on local conditions. The condition under which a lettered step or series of lettered steps should be made is given in the ACTION column, and all steps governed by the same condition are designated by the same letter within a test. Where a condition does not apply, all steps designated by that letter should be omitted.

2. APPARATUS

All Tests

2.01 124A test set, SD-1H070-01.

2.02 M3BP cord, power cable, 6 feet long (for patching battery from switch unit to test set).

2.03 731A (key, extractor) tool (for CP removal).

Tests A, D, E, F, I

2.04 W1BD cord (test lead, 8 feet long, equipped with test point contact spring and pin plug).

Tests B, C, G, H

2.05 W25B cord, testing cord, 6 feet long (for patching switch unit test position to 25 terminal test set connector, INPUTS 1-24).

Tests C, F, H, I

2.06 Two P1U cords (test lead, 10 inches long, equipped with pin plugs).

Tests C, G, H

2.07 R42 circuit pack, AUX BOARD A (special circuit pack for insertion between switch unit test position and test set INPUTS 1-24).

Tests C, H, I

2.08 W1BE cord (test lead, 10 inches long, equipped with test point contact spring and alligator clip).

3. PREPARATION

STEP	ACTION	VERIFICATION
All Tests		
1	Connect power to test set.	
2	On test set — Operate K1, K2, and K3 keys to positions PULSE FREQ, SEP, and DTR2 respectively.	

4. METHOD

STEP	ACTION	VERIFICATION
	A. Binary Counter Recycle	
3	On test set — Operate SYNC DELAY to 8K.	
4	Connect INPUT C to TP2 at 37B14 (CP15).	On 0-8 scale — PULSE FREQ reads 6 to 6.5. *Note:* No verification indicates trouble in circuits covered in Tests D or E.

STEP	ACTION	VERIFICATION
5	Move INPUT C to TP2 at 42C23 (CP217) of switch store 1 (BAY 1).	On 0-8 scale — PULSE FREQ reads 6 to 6.5. *Note:* No verification indicates a faulty CP217 at 42C23 in switch store 1. When the circuit under test is switch store 1, the binary counter may be at fault. In this case, proceed to Test E.
6	Remove INPUT C from TP2 at 42C23.	
7a	If no further tests are to be made at this time — Remove test set power connection.	
	B. Switch Store Input Test	
3	Connect test position, located in 29B20, to test set INPUTS 1-24 connector.	
4	Rotate DIAL A to test message 1.	
5	Operate DIAL A keys to test message 1.	
6	Request test message 1 be transmitted to switch unit from control unit.	
7	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. *Note:* Failure of verification indicates a faulty data distributor or data receiver circuit.
8	Rotate DIAL A to test message 2.	
9	Operate DIAL A keys to test message 2.	
10	Request removal of test message.	
11	Request test message 2 be transmitted to switch unit from control unit.	
12	Repeat Step 7.	
13	Repeat Steps 8 through 12 for test message 3.	
14	Move test connector from 29B20 to 29B23.	
15	Rotate DIAL A to test message 5.	
16	Operate DIAL A keys to test message 5.	
17	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. *Note:* Failure of verification indicates a faulty data distributor or data receiver circuit.

STEP	ACTION	VERIFICATION
18	Request removal of test message.	
19	Request test message 1 be transmitted to switch unit from control unit.	
20	Rotate DIAL A to test message 4.	
21	Operate DIAL A keys to test message 4.	
22	Repeat Step 17.	
23	Repeat Steps 18 through 22 for test message 3 from the control unit with test message 6 on DIAL A keys.	
24	Request removal of test message transmission.	
25	If no further tests are to be made at this time — Remove test set power connection.	

C. Switch Store Output Test

Note: When Test C has been successfully completed, it is assumed the switch store circuit is functioning properly for the particular time slot contained in the test message from the control unit.

3	Using AUX BOARD A — Connect test position, located in 42D6, to test set INPUTS 1-24 connector.	
4	On test set — Connect INPUT C to M3.	
5	Operate SYNC DELAY to 40K.	
6	Rotate DIAL A to test message 4.	
7	Operate DIAL A keys to test message 4.	
8	Request test message 1 be transmitted from control unit to switch unit.	
9	After confirmation of message transmission — On data distributor circuit associated with switch store under test — Connect TP6 at 33A17 to ground.	
10	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* No verification proves trouble within the switch store circuit. Proceed with successive tests.

STEP	ACTION	VERIFICATION
11	Remove ground from TP6 at 33A17.	
12	Rotate DIAL A to test message 5.	
13	Operate DIAL A keys to test message 5.	
14	Request removal of test message transmission.	
15	Request test message 2 be transmitted from control unit to switch unit.	
16	Repeat Steps 9 and 10.	Same as Steps 9 and 10.
17	Remove ground from TP6 at 33A17.	
18	Repeat Steps 14 through 17 for test message 3 from the control unit with test message 6 on DIAL A.	
19	Remove test connection at 42D6.	
20	Request removal of test message transmission.	
21a	If no further tests are to be made at this time — Remove test set power connection.	
	D. Clock Pulse Amplifiers	
3	On test set — Operate SYNC DELAY to 400K.	
4	Connect INPUT C to TP1 at 42A6 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a faulty CP20 at 42A6.
5	Move INPUT C to TP2 at 42A6 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a faulty CP20 at 42A6.
6	Move INPUT C to TP3 at 42A6 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates faulty CP20 at 42A6.
7	Move INPUT C to TP4 at 42A6 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates faulty CP20 at 42A6.

STEP	ACTION	VERIFICATION
8	Move INPUT C to TP1 at 42A10 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates faulty CP20 at 42A10.
9	Move INPUT C to TP2 at 42A10 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates faulty CP20 at 42A10.
10	Move INPUT C to TP4 at 42A10 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates faulty CP20 at 42A10.
11	Move INPUT C to TP3 at 42A2 (CP21).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates faulty CP21 at 42A2.
12	Remove INPUT C from TP3 at 42A2.	
13a	If no further tests are to be made at this time — Remove test set power connection.	
	E. Binary Counter Stages	
3	On test set — Operate SYNC DELAY to 8K.	
4	Connect INPUT C to TP6 at 42C23 (CP217) on switch store 1 (in BAY 1).	On 0-8 scale — PULSE FREQ reads 6 to 6.5. *Note:* No verification indicates a faulty CP217 at 42C23, switch store 1. When the circuit under test is switch store 1, the trouble may be within the binary counter of switch store 1.
5	Operate SYNC DELAY to 400K.	
6	Move INPUT C to TP8 at 37A11 (CP140).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a faulty clock circuit.
7	Move INPUT C to TP1 at 42A6 (CP20).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a faulty CP20 at 42A6.

STEP	ACTION	VERIFICATION
8	Move INPUT C to TP3 at 42A2 (CP21).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a faulty CP21 at 42A2.
9	Move INPUT C to TP2 at 37A23 (CP15).	On 0-4 scale — PULSE FREQ reads 1.4 to 1.6. ***Note:*** No verification indicates a faulty CP15 at 37A23 or CP16 at 37A20.
10	Move INPUT C to TP2 at 37B2 (CP15).	On 0-4 scale — PULSE FREQ reads 0.7 to 0.9. ***Note:*** No verification indicates a faulty CP15 at 37B2 or CP16 at 37A20.
11	Operate SYNC DELAY to 80K.	
12	Move INPUT C to TP2 at 37B5 (CP15).	On 0-8 scale — PULSE FREQ reads 3.6 to 4.2. ***Note:*** No verification indicates a faulty CP15 at 37B5 or CP16 at 37A20.
13	Operate SYNC DELAY to 40K.	
14	Move INPUT C to TP2 at 37B8 (CP15).	On 0-4 scale — PULSE FREQ reads 2.2 to 2.8. ***Note:*** No verification indicates a faulty CP15 at 37B8 or CP16 at 37A20.
15	Move INPUT C to TP2 at 37B11 (CP15).	On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a faulty CP15 at 37B11 or CP16 at 37A20.
16	Operate SYNC DELAY to 8K.	
17	Move INPUT C to TP2 at 37B14 (CP15).	On 0-8 scale — PULSE FREQ reads 6 to 6.5. ***Note:*** No verification indicates a faulty CP15 at 37B14 or CP16 at 37A20.
18	Remove INPUT C from TP2 at 37B14.	
19a	If no further tests are to be made at this time — Remove test set power connection.	

F. Horizontal Drive to Memory Array

3	On test set — Operate SYNC DELAY to 80K.	

STEP	ACTION	VERIFICATION
4	Connect INPUT C, in turn, to each of the following test points.	
	TP1 at 42B10 TP4 at 42B10	On 0-8 scale — PULSE FREQ reads 7.0 to 8.0. ***Note:*** No verification indicates a faulty CP18 at 42B10.
	TP1 at 42B14 TP4 at 42B14	On 0-8 scale — PULSE FREQ reads 7.0 to 8.0. ***Note:*** No verification indicates a faulty CP18 at 42B14.
	TP1 at 42B18 TP4 at 42B18	On 0-8 scale — PULSE FREQ reads 7.0 to 8.0. ***Note:*** No verification indicates a faulty CP18 at 42B18.
	TP1 at 42B22 TP4 at 42B22	On 0-8 scale — PULSE FREQ reads 7.0 to 8.0. ***Note:*** No verification indicates a faulty CP18 at 42B22.
5	Remove INPUT C from TP4 at 42B22.	
6	Operate K1 to COMPARATOR.	
7	Connect INPUT E to M4.	
8	Connect INPUT $\overline{C}$ to TP5 at 37A14 (CP140).	
9	Connect INPUT B to GRD.	
10	Connect INPUT A, in turn, to each of the following test points. After each connection, operate RST3, momentarily, then check for verification. TP1 at 42B10 TP4 at 42B10 TP1 at 42B14 TP4 at 42B14	On release of RST3 — OK lamp remains lighted. ***Note:*** No verification indicates a bad circuit pack to which INPUT A is connected.
11	Move INPUT C to TP5 at 37A11.	
12	Repeat Step 10 for each of the following. TP1 at 42B18 TP4 at 42B18 TP1 at 42B22 TP4 at 42B22	Same as Step 10.
13	Operate K1 to PULSE FREQ.	
14	On test set — Operate SYNC DELAY to 40K.	

STEP	ACTION	VERIFICATION
15	Connect INPUT C, in turn, to each of the following test points.	
	TP1 at 42A18 TP6 at 42A18	On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a faulty CP19 at 42A18.
	TP1 at 42A22 TP6 at 42A22	On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a faulty CP19 at 42A22.
	TP1 at 42B2 TP6 at 42B2	On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a faulty CP19 at 42B2.
	TP6 at 42B6	On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a faulty CP19 at 42B6.
16	Remove INPUT C from TP6 at 42B6.	
17a	If no further tests are to be made at this time — Remove test set power connection.	

G. Vertical Drive with Recirculate Removed

3	Ground TP3 at 42A6.	
4	Using AUX BOARD A — Connect test position located in 42D6, to test set INPUTS 1-24 connector.	
5	Rotate DIAL A to test message 4.	
6	Operate DIAL A keys to test message 4.	
7	Request test message 1 be transmitted to switch unit from control unit.	
8	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. ***Note:*** No verification indicates a trouble in one of the vertical access stages. Proceed with Step 15a to assist in isolating the faulty stage.
9	Request removal of test message transmission.	
10	Rotate DIAL A to test message 5.	
11	Operate DIAL A keys to test message 5.	
12	Request test message 2 be transmitted to switch unit from control unit.	

STEP	ACTION	VERIFICATION
13	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. *Note:* On failure of Step 13, proceed with Step 15a.
14	Repeat Steps 9 through 13 for test message 6 on DIAL A with test message 3 from the control unit.	Same as Step 13. *Note:* On failure of Step 14, proceed with Step 15a. Successful verification for Steps 8, 13, and 14 indicates successful completion of Test G. Proceed to Step 20.
15a	If Steps 8, 13, or 14 failed to verify — Operate DIAL A keys 1 and 2 to amber.	
16a	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. *Note 1:* Verification of Step 16a (with DIAL A keys 1 and 2 at amber) indicates a faulty CP17 at 37C2. *Note 2:* When the DIAL A keys are operated to the amber position, they are in a "don't care" state. A verification under these conditions localizes the difficulty to the circuit pack associated with these particular DIAL A keys.
17a	Restore DIAL A keys 1 and 2 to their original positions.	
18a	Repeat Steps 15a to 17a for the remaining DIAL A keys according to the sequence given in Table A. *Note:* Operate DIAL A keys to amber, two at a time, followed by a momentary operation of RST1. After each operation check for verification, then restore the keys to their original positions before proceeding to the next two keys.	On release of RST1 key — MSG IND 1 lamp lighted.

TABLE A

DIAL A KEYS TO AMBER	LOCATION OF CP17 UNDER TEST
3,4	37C6
5,6	37C10
7,8	37C14
9,10	37C18
11,12	37C22
13,14	37D2
15,16	37D6
17,18	37D10
19,20	37D14
21	37D18

STEP	ACTION	VERIFICATION
19b	If Steps 15a through 18a resulted in a circuit pack replacement — Repeat Steps 6 through 14 before proceeding to other tests.	
20	Request removal of test message transmission.	
21	Remove test connection at 42D6.	
22	Remove ground from TP3 at 42A6.	
23c	If no further tests are to be made at this time — Remove test set power connection.	
	H. Vertical Drive Recirculate Test	
3	On test set — Operate SYNC DELAY to 40K.	
4	Connect INPUT C to M3.	
5	Rotate DIAL A to test message 4.	
6	Operate DIAL A keys to test message 4.	
7	Using AUX BOARD A — Connect test position, located in 42D6, to test set INPUTS 1-24 connector.	
8	Request test message 1 be transmitted from control unit to switch unit.	
9	After confirmation of message transmission — On data distributor circuit — Connect TP6 at 33A17 to ground. *Note:* Step 9 removes subsequent messages from the switch store input.	
10	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* Failure of Step 10 indicates a trouble in one of the vertical access stages. Proceed with Step 17a to assist in isolating the faulty stage.
11	Rotate DIAL A to test message 5.	
12	Operate DIAL A keys to test message 5.	
13	Remove ground from TP6 at 33A17.	
14	Request removal of test message transmission.	

STEP	ACTION	VERIFICATION
15	Request test message 2 be transmitted from control unit to switch unit.	
16	Repeat Step 9.	
17	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** On failure of Step 17, proceed with Step 19a.
18	Repeat Steps 11 through 17 for test message 6 on DIAL A with test message 3 from the control unit.	Same as Step 17. ***Note:*** On failure of Step 18, proceed with Step 19a. Successful verification of Steps 10, 17, and 18 indicates the requirements for Test J have been met, and this test may be concluded by proceeding to Step 23.
19a	If Steps 10, 17, or 18 failed to verify — Operate DIAL A keys 1 and 2 to amber.	
20a	Operate RST1 key momentarily. ***Note:*** If during Steps 19a and 20a, replacement of a CP is made, it is necessary to remove ground from TP6 at 33A17 for a period of about 2 seconds to allow entry of the test message for retest.	On release of RST1 key — MSG IND 1 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** Verification indicates a faulty CP17 at 37C2.
21a	Repeat Steps 19a and 20a, observing notes, for the remaining DIAL A keys according to the sequence given in Table A. ***Note:*** Operate DIAL A keys to amber, two at a time, followed by a momentary operation of RST1. After each operation check for verification, then restore the keys to their original positions before proceeding with the next two keys.	On release of RST1 key — MSG IND 1 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** When the DIAL A keys are operated to the amber position, they are in a "don't care" state. A verification under these conditions localizes the difficulty to the circuit pack associated with these particular DIAL A keys.

TABLE A

DIAL A KEYS TO AMBER	LOCATION OF CP17 UNDER TEST
3,4	37C6
5,6	37C10
7,8	37C14
9,10	37C18
11,12	37C22
13,14	37D2
15,16	37D6
17,18	37D10
19,20	37D14
21	37D18

STEP	ACTION	VERIFICATION
22b	If Steps 19a through 21a resulted in a circuit pack replacement — Repeat Steps 6 through 18 before proceeding to other tests.	*Note:* If no particular CP17 seems at fault, and yet verification cannot be obtained, it is suggested that the strobe pulse be checked by replacing CP21 at 42A2. The 3A memory may be at fault when certain horizontal or vertical areas in the store are at fault.
23	Request removal of test message transmission.	
24	Remove ground from TP6 at 33A17.	
25	Remove test connection at 42D6.	
26c	If no other tests are to be made at this time — Remove test set power connections.	

I. Vertical Access to All Time Slots

3a	If testing switch store 1 — Disconnect (but do not remove) CP108 at 30D19 and 26D19 in BAY 3.	
4b	If testing switch store 2 — Disconnect (but do not remove) CP108 at 30A7 and 26A7 in BAY 4.	
5	On test set — Operate SYNC DELAY to 400K.	
6	Connect INPUT C to M4.	
7	Connect INPUT +HV to TP3 at 37C2 (CP17).	
8	Ground, momentarily, TP3 at 37C2 (CP17).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP17 at 37C2.
9	Ground, momentarily, in turn, the following: TP1 at 42A10 (CP20) TP2 at 42A10 (CP20) TP4 at 42A10 (CP20)	PULSE FREQ reads 0.

STEP	ACTION	VERIFICATION
10	Repeat Steps 7, 8, and 9 for each of the following: TP2 at 37C2 TP3 at 37C6 TP2 at 37C6 TP3 at 37C10 TP2 at 37C10 TP3 at 37C14 TP2 at 37C14 TP3 at 37C18 TP2 at 37C18 TP3 at 37C22 TP2 at 37C22 TP3 at 37D2 TP2 at 37D2 TP3 at 37D6 TP2 at 37D6 TP3 at 37D10 TP2 at 37D10 TP3 at 37D14 TP2 at 37D14 TP3 at 37D18	Same as Steps 7, 8, and 9. *Note:* No verification indicates a bad CP17 to which INPUT +HV is connected at time of failure. Failure at all points indicates a bad CP21 at 42A2.
11	Remove INPUT +HV from TP3 at 37D18.	
12	Replace the two CP108 packs in BAY 3 or BAY 4.	
13	Remove test set power connection.	