J1H011A SWITCH UNIT LINE NUMBER TRANSLATOR CIRCUIT TESTS USING 124A TEST SET SD-1H070-01 NO. 101 ELECTRONIC SWITCHING SYSTEM

1. GENERAL

1.01 This section describes a method for testing the line number translator circuit when there is an indication from the control unit teletypewriter or other sources that this circuit is the cause of switch unit failures.

These tests should be performed only on the line number translator circuit associated with the off-line bus. The bus must be removed from call processing but bus power must be retained.

1.02 The tests covered are:

A. Timing Circuit and Ring-Ringback Drivers: This test checks the timing circuit output frequencies. It also checks the operation of the ring-ringback interface logic when ring and ringback bits are simulated in the switch store. Under these same conditions, a check is made on the ring and ringback driver stages.

B. Memory Register in Static State: This test checks that each memory register stage gives a proper response to the reset pulse.

C. Pulse Frequency Test for H0 and V0 Driver Stages: This test checks that the H0 and V0 driver stages produce pulses at the clock frequency.

D. Static State Test for H- and V- Drivers: This test checks the idle state of the H- and V-driver stages when no information is present in the switch store.

E. Pulse Frequency Test for H- and V- Drivers: This test checks that each horizontal and vertical driver stage will produce time division enabling pulses on receipt of appropriate control unit messages.

F. Resonant Circuit and Capacitor Discharge Switch: This test checks the ability of the resonant circuit and capacitor discharge switch to produce output pulses at the proper rate and amplitude.

1.04 The METHOD portion of this section is divided into two parts headed 4. METHOD and 5. METHOD. These two parts are identical except for equipment locations. 4. METHOD must be applied when testing line number translator circuit 1 only and 5. METHOD applied when testing line number translator circuit 2 only.

1.05 ***Caution: During the performance of this test it is required that a series of momentary connections be made to the off-line switch store circuit. Be sure these connections are made to the correct test points.***

1.06 Certain tests in this section require the assistance of the control unit. Test messages required to perform these tests must be originated by an appropriate ***manual request*** teletypewriter print-in.

1.07 The control unit must be notified if an inadvertent disruption of service occurs as a result of testing. This applies to blown fuses in both on- and off-line circuits.

1.08 *Lettered Steps:* A letter a, b, c, etc, added to a step number in Parts 4 and 5 of this section, indicates an action which may or may not be required depending on test conditions. The condition under which a lettered step or series of lettered steps should be made is given in the ACTION column, and all steps governed by the same condition are designated by the same letter within a test. Where a condition does not apply, all steps designated by that letter should be omitted.

2. APPARATUS

All Tests

2.01 124A test set, SD-1H070-01.

2.02 M3BP cord, power cable, 6 feet long (for patching battery from switch unit to test set).

2.03 Two W1BD cords (test lead, 8 feet long, equipped with test point contact spring and pin plug).

2.04 Three P1U cords (test lead, 10 inches long, equipped with pin plugs).

2.05 731A (key, extractor) tool (for CP removal).

Tests A, E

2.06 W9B cord, testing cord, 6 feet long (for patching various switch unit test points to 9 terminal test connector, INPUTS 25-32).

3. PREPARATION

STEP	ACTION	VERIFICATION
All Steps		
1	Connect power to test set.	
2	Request a print-in at the control unit to inhibit the maintenance program to this switch unit.	
3	On the switch store circuit associated with the line number translator circuit under test — Ground, in turn, TP1, TP2, and TP4 at 42A10, momentarily.	

4. METHOD (For line number translator circuit 1 only)

STEP	ACTION	VERIFICATION
	A. Timing Circuit and Ring-Ringback Drivers	
4	On test set — Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 400K.	
6	Connect INPUT C to TP3 at 38D16 (CP103).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP103 at 38D16.
7	Move INPUT C to TP3 at 18D16 (CP103).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP103 at 18D16.
8	Move INPUT C to each of the following test points, in turn. TP1 at 38D10 (CP104) TP2 at 38D10 TP3 at 38D10 TP4 at 38D10	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP104 at 38D10.

STEP	ACTION	VERIFICATION
9	Move INPUT C to each of the following test points, in turn. TP1 at 18D10 (CP104) TP2 at 18D10 TP3 at 18D10 TP4 at 18D10	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP104 at 18D10.
10	Move INPUT C to TP1 at 38D13 (CP220).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP220 at 38D13.
11	Move INPUT C to TP1 at 18D13 (CP220).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP220 at 18D13.
12	Connect INPUTS 25-32 to the switch store circuit in BAY 1 as follows: TEST SET INPUT — SWITCH STORE TEST POINT 25 — TP2 at 42A6 (CP20) 26 — TP1 at 37B11 (CP15) 27 — TP1 at 37B8 (CP15) 28 — TP1 at 37B5 (CP15) 29 — TP1 at 37B2 (CP15) 30 — TP1 at 37A23 (CP15)	
13	Operate DIAL B key 25 to red.	
14	Operate K2 to SEP.	
15	Operate DIAL B keys 26 through 30 to the positions shown in Table A for switch unit time slot number 10. ***Note:*** If time slot number 10 cannot be used for any reason, any other time slot may be used.	
16	Connect M2 to TP8 at 37D10 (CP17) in BAY 1, momentarily.	
17	Operate SYNC DELAY to 8K.	
18	Move INPUT C to TP5 at 38D13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6. ***Note:*** No verification indicates a bad CP220 at 38D13.

STEP	ACTION	VERIFICATION
19	Move INPUT C to TP5 at 18D13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6. ***Note:*** No verification indicates a bad CP220 at 18D13.
20	Connect M2 to TP7 at 37D10 (CP17) in BAY 1, momentarily.	
21	Connect M2 to TP9 at 37D13 (CP17) in BAY 1, momentarily.	
22	Move INPUT C to TP5 at 38D13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds and recycles. ***Note:*** No verification indicates a bad CP220 at 38D13.
23	Move INPUT C to TP5 at 18D13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds and recycles. ***Note:*** No verification indicates a bad CP220 at 18D13.
24	Move INPUT C to M4.	
25	Connect INPUT +HV to TP5 at 38D16 (CP103).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds and recycles. ***Note:*** No verification indicates a bad CP103 at 38D16 or CP108 at 30D19.
26	Move INPUT +HV to TP5 at 18D16 (CP103).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds and recycles. ***Note:*** No verification indicates a bad CP103 at 18D16 or CP108 at 26D19.
27	Remove INPUT +HV from TP5 at 18D16.	
28	Operate K4 to V.	
29	Connect INPUT −HV to TP5 at 30D19 (CP108).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds and recycles. ***Note:*** No verification indicates a bad CP108 at 30D19.
30	Move INPUT −HV to TP5 at 26D19 (CP108).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds and recycles. ***Note:*** No verification indicates a bad CP108 at 26D19.
31	Remove INPUT −HV from TP5 at 26D19.	
32	Remove connections made in Step 12.	

STEP	ACTION	VERIFICATION
33a	If no further tests are to be made at this time — Remove power connection between test set and switch unit.	
34a	Request control unit to enable maintenance routine to this switch unit.	

B. Memory Register in Static State

4	On test set — Operate K1 to COMPARATOR.	
5	Connect INPUT E to MULT 2.	
6	Connect INPUT B to MULT 2.	
7	Connect GRD to MULT 2.	
8	Connect INPUT A, in turn, to each of the following test points. After each connection, operate RST3 key momentarily and check verification. TP1, TP2, TP5, TP6 at 38D19 (CP107) TP1, TP2, TP5, TP6 at 38D22 (CP107) TP1, TP2, TP5, TP6 at 18D19 (CP107) TP1, TP2, TP5, TP6 at 18D22 (CP107)	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a bad CP107 in the location under test.
9	Remove INPUT A from TP6 at 18D22.	
10a	If no further tests are to be made at this time — Remove power connection between test set and switch unit.	
11a	Request control unit to enable maintenance routine to this switch unit.	

C. Pulse Frequency Test for H0 and V0 Driver Stages

4	Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 400K.	
6	Operate K4 to H.	
7	Connect INPUT C to M4.	
8	Connect INPUT −HV to TP2 at 34D7 (CP106).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP106 at 34D7 or CP102 at 34D19.

STEP	ACTION	VERIFICATION
9	Move INPUT −HV to TP2 at 22D7 (CP106).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP106 at 22D7 or CP102 at 22D19.
10	Disconnect (but do not remove) the CP106 at 34D7 and 22D7.	
11	Operate K4 to V.	
12	Move INPUT −HV to TP4 at 42D7 (CP105).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP105 at 42D7 or CP102 at 42D19.
13	Move INPUT −HV to TP4 at 14D7 (CP105).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP105 at 14D7 or CP102 at 14D19.
14	Remove INPUT −HV from TP4 at 14D7.	
15	Replace the CP106 at 34D7 and 22D7.	
16a	If no further tests are to be performed at this time — Remove power connection between test set and switch unit.	
17a	Request control unit to enable maintenance routine to this switch unit.	

D. Static State Test for H- and V- Drivers

4	On transfer and alarms circuit in BAY 2 — Operate S3 key momentarily.	On transfer and alarms circuit — SS1 lamp lighted.
5	Disconnect (but do not remove) the circuit packs (CP105) in the following locations: 42D7 14D7 42D10 14D10 42D13 14D13 42D16 14D16	
6	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS1 lamp extinguished.
7	Connect INPUT A to M4.	
8	Connect INPUT B to S+12.	
9	Connect INPUT E to GRD.	
10	Operate K4 to H.	
11	Operate K1 to COMPARATOR.	

STEP	ACTION	VERIFICATION
12	Connect INPUT −HV, in turn, to each of the test points listed in Table B for driver gates HD1 through HD15 — Perform this test on both A PARTY and B PARTY locations — After making each connection, momentarily operate RST3 key and check for verification.	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a bad CP106 in the location under test. If, after replacement and retest, there is no verification, Table B lists the location of the associated translator gates, and memory register stages that may be at fault.
13	On transfer and alarms circuit in BAY 2 — Operate S3 key momentarily.	On transfer and alarms circuit — SS1 lamp lighted.
14	Replace the circuit packs (CP105) removed in Step 5.	
15	Disconnect (but do not remove) the circuit packs (CP106) in the following locations: 34D7 34D10 34D13 34D16 22D7 22D10 22D13 22D16	
16	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS1 lamp extinguished.
17	Move INPUT B from S+12 to GRD.	
18	Operate K4 to V.	
19	Connect INPUT −HV, in turn, to each of the test points listed in Table C for driver gates VD1 through VD15 — Perform this test on both A PARTY and B PARTY locations — After making each connection, momentarily operate RST3 key and check for verification.	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a bad CP105 in the location under test. If, after replacement and retest, there is no verification, Table C lists the location of the associated translator gates and memory register stages that may be at fault.
20	Remove INPUT −HV from switch unit.	
21	Remove patches between test jacks on test set.	
22a	If no further tests are to be performed at this time — On transfer and alarms circuit in BAY 2 — Operate S3 key momentarily.	On transfer and alarms circuit — SS1 lamp lighted.
23a	Replace the circuit packs (CP106) removed in Step 15.	

STEP	ACTION	VERIFICATION
24a	On transfer and alarms circuit — Operate S5 key momentarily.	On transfer and alarms circuit — SS1 lamp extinguished.
25a	Remove power connection between test set and switch unit.	

E. Pulse Frequency Test for H- and V- Drivers

4a	If this test is being performed as a sequel to Test D — Proceed to Step 9.	
5	On transfer and alarms circuit in BAY 2 — Operate S3 key momentarily.	On transfer and alarms circuit — SS1 lamp lighted.
6	Disconnect (but do not remove) the circuit packs (CP106) in the following locations: 34D7 34D10 34D13 34D16 22D7 22D10 22D13 22D16	
7	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS1 lamp extinguished.
8	Operate K4 to V.	
9	Connect INPUT C to M2.	
10	Operate SYNC DELAY to 40K.	
11	Operate K1 to PULSE FREQ.	
12	Operate K2 to SEP.	
13	Operate K3 to DTR2.	
14	Connect INPUTS 26 through 30 to the switch store circuit in BAY 1 as follows:	

TEST SET INPUT	SWITCH STORE TEST POINT
26	TP1 at 37B11
27	TP1 at 37B8
28	TP1 at 37B5
29	TP1 at 37B2
30	TP1 at 37A23

STEP	ACTION	VERIFICATION
15	Operate DIAL B keys 26 through 30 to the positions shown in Table A for switch unit time slot 10. *Note:* If time slot number 10 cannot be used for any reason, any other time slot may be used for this test.	
16	Operate RST2 key momentarily.	On release of RST2 key — MSG IND 2 lamp lighted.
17	Connect INPUT 25 to M4.	
18	Operate DIAL B key 25 to red.	
19	Connect INPUT −HV to TP5 at 42D7 (CP105).	
20	Operate RST2 key momentarily.	On release of RST2 key — MSG IND 2 lamp remains extinguished.
21	Request control unit to type in appropriate manual request test messages to cause the extension number 281 to appear as both A and B parties in time slot selected in Step 15 — The TTY type-in for this arrangement consists of the four TTY characters 8181 in the fourth word of a TMx type message.	On receipt of first test message — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* No verification indicates a bad CP105 at 42D7, CP102 at 42D19, or CP107 at 38D22.
22	Move INPUT −HV to TP5 at 14D7 (CP105).	
23	Operate RST2 key momentarily.	On release of RST2 key — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* No verification indicates a bad CP105 at 14D7, CP102 at 14D19, or CP107 at 18D22.
24	Repeat Steps 20 and 21 for each of the vertical drivers VD2 through VD15 as listed in Tables C and D — The appropriate TTY request to energize a particular vertical driver (VD-) is listed in Table D — The test point location for checking this particular driver is given in Table C — Perform this test on both A and B party locations as shown in Table C — Operate RST2 key momentarily before checking for verification.	On release of RST2 key — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* No verification indicates a bad CP105 in the location under test. If, after replacement and retest, there is no verification, Table C lists the location of the associated translator gates and memory register stages that may be at fault.
25	On transfer and alarms circuit in BAY 2 — Operate S3 key momentarily.	On transfer and alarms circuit — SS1 lamp lighted.
26	Replace circuit packs (CP106) removed in Step 6.	

STEP	ACTION	VERIFICATION
27	Disconnect (but do not remove) the circuit packs (CP105) in the following locations: 42D7 42D10 42D13 42D16 14D7 14D10 14D13 14D16	
28	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS1 lamp extinguished.
29	Operate K4 to H.	
30	Repeat Steps 20 and 21 for each of the horizontal drivers HD1 through HD15 — The appropriate TTY request to energize a particular horizontal driver (HD-) is listed in Table E — The corresponding test point for checking this particular driver is listed in Table B — Perform this test in both A and B party locations as shown in Table B — Operate RST2 key momentarily before checking for verification.	On release of RST2 key — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a bad CP106 in the location under test. If, after replacement and retest, there is no verification, Table B lists the location of the associated translator gates and memory register stages that may be at fault.
31	On transfer and alarms circuit in BAY 2 — Operate S3 key momentarily.	On transfer and alarms circuit — SS1 lamp lighted.
32	Replace circuit packs (CP105) removed in Step 27.	
33	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS1 lamp extinguished.
34	Request control unit to remove test message transmission.	
35	Remove connections made in Step 14.	
36	Remove INPUT −HV from switch unit.	
37b	If no further tests are to be performed at this time — Remove power connection between test set and switch unit.	
38b	On the switch store associated with the line number translator under test — Ground, in turn, TP1, TP2, and TP4 at 42A10, momentarily.	

STEP	ACTION	VERIFICATION
	F. Resonant Circuit and Capacitor Discharge Switch	
4	On test set — Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 400K.	
6	Connect INPUT C to M4.	
7	Connect INPUT +HV to TP1 at 30D22 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 30D22 or CP220 at 38D13.
8	Move INPUT +HV to TP6 at 30D22 (CP109).	PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 30D22 or CP220 at 38D13.
9	Move INPUT +HV to TP1 at 26D22 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 26D22 or CP220 at 18D13.
10	Move INPUT +HV to TP6 at 26D22 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 26D22 or CP220 at 18D13.
11	Remove INPUT +HV from TP6 at 26D22.	
12	Operate K4 to N.	
13	Connect INPUT −HV to TP4 at 30D22 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 30D22.
14	Move INPUT −HV to TP4 at 26D22 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 26D22.
15	Move INPUT −HV to TP1 at 30D19 (CP108).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP108 at 30D19.
16	Move INPUT −HV to TP1 at 26D19 (CP108).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP108 at 26D19.
17	Remove INPUT −HV from TP1 at 26D19.	

STEP	ACTION	VERIFICATION
18	Remove power connection between the test set and switch unit.	
19	Request control unit to enable switch unit maintenance.	

5. METHOD (For line number translator circuit 2 only)

STEP	ACTION	VERIFICATION
	A. Timing Circuit and Ring-Ringback Drivers	
4	On test set — Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 400K.	
6	Connect INPUT C to TP3 at 38A10 (CP103).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP103 at 38A10.
7	Move INPUT C to TP3 at 18A10 (CP103).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP103 at 18A10.
8	Move INPUT C to each of the following test points, in turn: TP1 at 38A16 (CP104) TP2 at 38A16 (CP104) TP3 at 38A16 (CP104) TP4 at 38A16 (CP104)	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP104 at 38A16.
9	Move INPUT C to each of the following test points, in turn: TP1 at 18A16 (CP104) TP2 at 18A16 (CP104) TP3 at 18A16 (CP104) TP4 at 18A16 (CP104)	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP104 at 18A16.
10	Move INPUT C to TP1 at 38A13 (CP220).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP220 at 38A13.
11	Move INPUT C to TP1 at 18A13 (CP220).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP220 at 18A13.

STEP	ACTION	VERIFICATION
12	Connect INPUTS 25-32 to the switch store circuit in BAY 2 as follows: TEST SET INPUT — SWITCH STORE TEST POINT 25 — TP2 at 42A6 (CP20) 26 — TP1 at 37B11 (CP15) 27 — TP1 at 37B8 (CP15) 28 — TP1 at 37B5 (CP15) 29 — TP1 at 37B2 (CP15) 30 — TP1 at 37A23 (CP15)	
13	Operate DIAL B key 25 to red.	
14	Operate K2 to SEP.	
15	Operate DIAL B keys 26 through 30 to the positions shown in Table A for switch unit time slot number 10. ***Note:*** If time slot number 10 cannot be used for any reason, any other time slot may be used.	
16	Connect M2 to TP8 at 37D10 (CP17) in BAY 2, momentarily.	
17	Operate SYNC DELAY to 8K.	
18	Move INPUT C to TP5 at 38A13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6. ***Note:*** No verification indicates a bad CP220 at 38A13.
19	Move INPUT C to TP5 at 18A13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6. ***Note:*** No verification indicates a bad CP220 at 18A13.
20	Connect M2 to TP7 at 37D10 (CP17) in BAY 2, momentarily.	
21	Connect M2 to TP9 at 37D13 (CP17) in BAY 2, momentarily.	
22	Move INPUT C to TP5 at 38A13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds, and recycles. ***Note:*** No verification indicates a bad CP220 at 38A13.

STEP	ACTION	VERIFICATION
23	Move INPUT C to TP5 at 18A13 (CP220).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds, and recycles. ***Note:*** No verification indicates a bad CP220 at 18A13.
24	Move INPUT C to M4.	
25	Connect INPUT +HV to TP5 at 38A10 (CP103).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds, and recycles. ***Note:*** No verification indicates a bad CP103 at 38A10 or CP108 at 30A7.
26	Move INPUT +HV to TP5 at 18A10 (CP103).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds, and recycles. ***Note:*** No verification indicates a bad CP103 at 18A10 or CP108 at 26A7.
27	Remove INPUT +HV from TP5 at 18A10.	
28	Operate K4 to V.	
29	Connect INPUT −HV to TP5 at 30A7 (CP108).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds, and recycles. ***Note:*** No verification indicates a bad CP108 at 30A7.
30	Move INPUT −HV to TP5 at 26A7 (CP108).	On 0-8 scale — PULSE FREQ reads 5.9 to 6.6 for 1 second, then reads 0 for 3 seconds, and recycles. ***Note:*** No verification indicates a bad CP108 at 26A7.
31	Remove INPUT −HV from TP5 at 26A7.	
32	Remove connections made in Step 12.	
33a	If no further tests are to be made at this time — Remove power connection between test set and switch unit.	
34a	Request control unit to enable maintenance routine to this switch unit.	

B. Memory Register in Static State

4	On test set — Operate K1 to COMPARATOR.	
5	Connect INPUT E to MULT 2.	
6	Connect INPUT B to MULT 2.	
7	Connect GRD to MULT 2.	

STEP	ACTION	VERIFICATION
8	Connect INPUT A, in turn, to each of the following test points. After each connection, operate RST3 key momentarily and check verification. TP1, TP2, TP5, TP6 at 38A7 (CP107) TP1, TP2, TP5, TP6 at 38A4 (CP107) TP1, TP2, TP5, TP6 at 18A7 (CP107) TP1, TP2, TP5, TP6 at 18A4 (CP107)	After release of RST3 key — OK lamp remains lighted. *Note:* No verification indicates a bad CP107 in the location under test.
9	Remove INPUT A from TP6 at 18A4.	
10a	If no further tests are to be made at this time — Remove power connection between test set and switch unit.	
11a	Request control unit to enable maintenance routine to this switch unit.	

C. Pulse Frequency Test for H0 and V0 Driver Stages

4	Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 400K.	
6	Operate K4 to H.	
7	Connect INPUT C to M4.	
8	Connect INPUT −HV to TP2 at 34A19 (CP106).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP106 in location 34A19 or CP102 in location 34A7.
9	Move INPUT −HV to TP2 at 22A19 (CP106).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP106 at 22A19 or CP102 at 22A7.
10	Disconnect (but do not remove) the CP106 at 34A19 and 22A19.	
11	Operate K4 to V.	
12	Move INPUT −HV to TP4 at 42A19 (CP105).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP105 at 42A19 or CP102 at 42A7.
13	Move INPUT −HV to TP4 at 14A19 (CP105).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. *Note:* No verification indicates a bad CP105 at 14A19 or CP102 at 14A7.
14	Remove INPUT −HV from TP4 at 14A19.	
15	Replace the CP106 at 34A19 and 22A19.	

STEP	ACTION	VERIFICATION
16a	If no further tests are to be performed at this time — Remove power connection between test set and switch unit.	
17a	Request control unit to enable maintenance routine to this switch unit.	
	D. Static State Test for H- and V- Drivers	
4	On transfer and alarms circuit in BAY 2 — Operate S4 key momentarily.	On transfer and alarms circuit — SS2 lamp lighted.
5	Disconnect (but do not remove) the circuit packs (CP105) in the following locations: 42A19 42A16 42A13 42A10 14A19 14A16 14A13 14A10	
6	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS2 lamp extinguished.
7	Connect INPUT A to M4.	
8	Connect INPUT B to S+12.	
9	Connect INPUT E to GRD.	
10	Operate K4 to H.	
11	Operate K1 to COMPARATOR.	
12	Connect INPUT −HV, in turn, to each of the test points listed in Table F for driver gates HD1 through HD15 — Perform this test on both A PARTY and B PARTY locations — After making each connection, momentarily operate RST3 key and check for verification.	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a bad CP106 in the location under test. If, after replacement and retest, there is no verification, Table F lists the location of the associated translator gates and memory register stages that may be at fault.
13	On transfer and alarms circuit in BAY 2 — Operate S4 key momentarily.	On transfer and alarms circuit — SS2 lamp lighted.
14	Replace the circuit packs (CP105) removed in Step 5.	
15	Disconnect (but do not remove) the circuit packs (CP106) in the following locations: 34A19 22A19 34A16 22A16 34A13 22A13 34A10 22A10	

STEP	ACTION	VERIFICATION
16	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS2 lamp extinguished.
17	Move INPUT B from S+12 to GRD.	
18	Operate K4 to V.	
19	Connect INPUT −HV, in turn, to each of the test points listed in Table G for driver gates VD1 through VD15 — Perform this test on both A PARTY and B PARTY locations — After making each connection, momentarily operate RST3 key and check for verification.	After release of RST3 key — OK lamp remains lighted. *Note:* No verification indicates a bad CP105 in the location under test. If, after replacement and retest, there is no verification, Table G lists the location of the associated translator gates and memory register stages that may be at fault.
20	Remove INPUT −HV from switch unit.	
21	Remove patches between test jacks on test set.	
22a	If no further tests are to be performed at this time — On transfer and alarms circuit in BAY 2 — Operate S4 key momentarily.	On transfer and alarms circuit — SS2 lamp lighted.
23a	Replace the circuit packs (CP106) removed in Step 15.	
24a	On transfer and alarms circuit — Operate S5 key momentarily.	On transfer and alarms circuit — SS2 lamp extinguished.
25a	Remove power connection between test set and switch unit.	

E. Pulse Frequency Test for H- and V- Drivers

4a	If this test is being performed as a sequel to Test D — Proceed to Step 9.	
5	On transfer and alarms circuit in BAY 2 — Operate S4 key momentarily.	On transfer and alarms circuit — SS2 lamp lighted.
6	Disconnect (but do not remove) the circuit packs (CP106) in the following locations: 34A19, 22A19; 34A16, 22A16; 34A13, 22A13; 34A10, 22A10	
7	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS2 lamp extinguished.
8	Operate K4 to V.	

STEP	ACTION	VERIFICATION
9	Connect INPUT C to M2.	
10	Operate SYNC DELAY to 40K.	
11	Operate K1 to PULSE FREQ.	
12	Operate K2 to SEP.	
13	Operate K3 to DTR2.	
14	Connect INPUTS 26 through 30 to the switch store circuit in BAY 2 as follows: TEST SET INPUT — SWITCH STORE TEST POINT 26 — TP1 at 37B11 27 — TP1 at 37B8 28 — TP1 at 37B5 29 — TP1 at 37B2 30 — TP1 at 37A23	
15	Operate DIAL B keys 26 through 30 to the positions shown in Table A for switch unit time slot 10. *Note:* If time slot number 10 cannot be used for any reason, any other time slot may be used for this test.	
16	Operate RST2 key momentarily.	On release of RST2 key — MSG IND 2 lamp lighted.
17	Connect INPUT 25 to M4.	
18	Operate DIAL B key 25 to red.	
19	Connect INPUT −HV to TP5 at 42A19 (CP105).	
20	Operate RST2 key momentarily.	On release of RST2 key — MSG IND 2 lamp remains extinguished.
21	Request control unit to type in appropriate manual request test messages to cause the extension number 281 to appear as both A and B parties in time slot selected in Step 15 — The TTY type-in for this arrangement consists of the four TTY characters 8181 in the fourth word of a TMx type message.	On receipt of first test message — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* No verification indicates a bad CP105 at 42A19, CP102 at 42A7, or CP107 at 38A4.
22	Move INPUT −HV to TP5 at 14A19 (CP105).	
23	Operates RST2 key momentarily.	On release of RST2 key — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. *Note:* No verification indicates a bad CP105 at 14A19, CP102 at 14A7, or CP107 at 18A4.

STEP	ACTION	VERIFICATION
24	Repeat Steps 20 and 21 for each of the vertical drivers VD2 through VD15 as listed in Tables G and D — The appropriate TTY request to energize a particular vertical driver (VD-) is listed in Table D — The test point location for checking this particular driver is given in Table G — Perform this test on both A and B party locations as shown in Table G — Operate RST2 key momentarily before checking for verification.	On release of RST2 key — MSG IND 2 lamp lighted. On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a bad CP105 in the location under test. If, after replacement and retest, there is no verification, Table G lists the location of the associated translator gates and memory register stages that may be at fault.
25	On transfer and alarms circuit in BAY 2 — Operate S4 key momentarily.	On transfer and alarms circuit — SS2 lamp lighted.
26	Replace circuit packs (CP106) removed in Step 6.	
27	Disconnect (but do not remove) the circuit packs (CP105) in the following locations. 42A19 42A16 42A13 42A10 14A19 14A16 14A13 14A10	
28	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS2 lamp extinguished.
29	Operate K4 to H.	
30	Repeat Steps 20 and 21 for each of the horizontal drivers HD1 through HD15 — The appropriate TTY request to energize a particular horizontal driver (HD-) is listed in Table E — The corresponding test point for checking this particular driver is listed in Table F — Perform this test in both A and B party locations as shown in Table F — Operate RST2 key momentarily before checking for verification.	On release of RST2 key — On 0-4 scale — MSG IND 2 lamp lighted. PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a bad CP106 in the location under test. If, after replacement and retest, there is no verification, Table F lists the location of the associated translator gates and memory register stages that may be at fault.
31	On transfer and alarms circuit in BAY 2 — Operate S4 key momentarily.	On transfer and alarms circuit — SS2 lamp lighted.
32	Replace circuit packs (CP105) removed in Step 27.	
33	On transfer and alarms circuit in BAY 2 — Operate S5 key momentarily.	On transfer and alarms circuit — SS2 lamp extinguished.

STEP	ACTION	VERIFICATION
34	Request control unit to remove test message transmission.	
35	Remove connections made in Step 14.	
36	Remove INPUT −HV from switch unit.	
37b	If no further tests are to be performed at this time — Remove power connection between test set and switch unit.	
38b	On the switch store associated with the line number translator under test — Ground, in turn, TP1, TP2, and TP4 at 42A10, momentarily.	
	F. Resonant Circuit and Capacitor Discharge Switch	
4	On test set — Operate K1 to PULSE FREQ.	
5	Operate SYNC DELAY to 400K.	
6	Connect INPUT C to M4.	
7	Connect INPUT +HV to TP1 at 30A4 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 30A4 or CP220 at 38A13.
8	Move INPUT +HV to TP6 at 30A4 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 30A4 or CP220 at 38A13.
9	Move INPUT +HV to TP1 at 26A4 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 26A4 or CP220 at 18A13.
10	Move INPUT +HV to TP6 at 26A4 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 26A4 or CP220 at 18A13.
11	Remove INPUT +HV from TP6 at 26A4.	
12	Operate K4 to N.	

STEP	ACTION	VERIFICATION
13	Connect INPUT −HV to TP4 at 30A4 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 30A4.
14	Move INPUT −HV to TP4 at 26A4 (CP109).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP109 at 26A4.
15	Move INPUT −HV to TP1 at 30A7 (CP108).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP108 at 30A7.
16	Move INPUT −HV to TP1 at 26A7 (CP108).	On 0-4 scale — PULSE FREQ reads 2.9 to 3.3. ***Note:*** No verification indicates a bad CP108 at 26A7.
17	Remove INPUT −HV from TP1 at 26A7.	
18	Remove power connection between the test set and switch unit.	
19	Request control unit to enable switch unit maintenance.	

Attached: Tables A through G

TABLE A

TIME SLOT ASSIGNMENTS

SWITCH UNIT TIME SLOT NUMBER	TTY TIME SLOT NUMBER		DIAL B KEY SETTINGS R = RED, G = GREEN				
	BUS 1	BUS 2	26	27	28	29	30
1	2	3	G	G	G	G	R
2	4	5	G	G	G	R	G
3	6	7	G	G	G	R	R
4	8	9	G	G	R	G	G
5	10	11	G	G	R	G	R
6	12	13	G	G	R	R	G
7	14	15	G	G	R	R	R
8	16	17	G	R	G	G	G
9	18	19	G	R	G	G	R
10	20	21	G	R	G	R	G
11	22	23	G	R	G	R	R
12	24	25	G	R	R	G	G
13	26	27	G	R	R	G	R
14	28	29	G	R	R	R	G
15	30	31	G	R	R	R	R
16	32	33	R	G	G	G	G
17	34	35	R	G	G	G	R
18	36	37	R	G	G	R	G
19	38	39	R	G	G	R	R
20	40	41	R	G	R	G	G
21	42	43	R	G	R	G	R
22	44	45	R	G	R	R	G
23	46	47	R	G	R	R	R
24	48	49	R	R	G	G	G
25	50	51	R	R	G	G	R

TABLE B

HORIZONTAL TRANSLATOR NO. 1, BAY 3

DRIVER GATE UNDER TEST	A PARTY		B PARTY	
	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION
HD1	TP1 at 34D7 (CP106)	34D19 (CP102), 38D19 (CP107)	TP1 at 22D7 (CP106)	22D19 (CP102), 18D19 (CP107)
HD2	TP3 " "	" "	TP3 " "	" "
HD3	TP4 " "	" "	TP4 " "	" "
HD4	TP2 " 34D10 (CP106)	" "	TP2 " 22D10 (CP106)	" "
HD5	TP1 " "	" "	TP1 " "	" "
HD6	TP3 " "	" "	TP3 " "	" "
HD7	TP4 " "	" "	TP4 " "	" "
HD8	TP2 " 34D13 (CP106)	34D22 (CP102) "	TP2 " 22D13 (CP106)	22D22 (CP102) "
HD9	TP1 " "	" "	TP1 " "	" "
HD10	TP3 " "	" "	TP3 " "	" "
HD11	TP4 " "	" "	TP4 " "	" "
HD12	TP2 " 34D16 (CP106)	" "	TP2 " 22D16 (CP106)	" "
HD13	TP1 " "	" "	TP1 " "	" "
HD14	TP3 " "	" "	TP3 " "	" "
HD15	TP4 " "	" "	TP4 " "	" "

TABLE C

VERTICAL TRANSLATOR NO. 1, BAY 3

DRIVER GATE UNDER TEST	A PARTY		B PARTY	
	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION
VD1	TP5 at 42D7 (CP105)	42D19 (CP102), 38D22 (CP107)	TP5 at 14D7 (CP105)	14D19 (CP102), 18D22 (CP107)
VD2	TP1 " "	" "	TP1 " "	" "
VD3	TP2 " "	" "	TP2 " "	" "
VD4	TP4 " 42D10 (CP105)	" "	TP4 " 14D10 (CP105)	" "
VD5	TP5 " "	" "	TP5 " "	" "
VD6	TP1 " "	" "	TP1 " "	" "
VD7	TP2 " "	" "	TP2 " "	" "
VD8	TP4 " 42D13 (CP105)	42D22 (CP102) "	TP4 " 14D13 (CP105)	14D22 (CP102) "
VD9	TP5 " "	" "	TP5 " "	" "
VD10	TP1 " "	" "	TP1 " "	" "
VD11	TP2 " "	" "	TP2 " "	" "
VD12	TP4 " 42D16 (CP105)	" "	TP4 " 14D16 (CP105)	" "
VD13	TP5 " "	" "	TP5 " "	" "
VD14	TP1 " "	" "	TP1 " "	" "
VD15	TP2 " "	" "	TP2 " "	" "

TABLE D

TEST MESSAGE — VERTICAL

VERTICAL DRIVER UNDER TEST	TTY PRINT-IN	LINE NO. IN A AND B PARTY
VD1	8181	EXT 281
VD2	8282	" 282
VD3	8383	" 283
VD4	8484	" 284
VD5	8585	" 285
VD6	8686	" 286
VD7	8787	" 287
VD8	8888	" 288
VD9	8989	" 289
VD10	8080	" 290
VD11	8M8M	" 291
VD12	8S8S	" 292
VD13	8C8C	" 293
VD14	8T8T	" 294
VD15	8R8R	" 295

TABLE E

TEST MESSAGE — HORIZONTAL

HORIZONTAL DRIVER UNDER TEST	TTY PRINT-IN	LINE OR TRUNK NO. IN A AND B PARTY
HD1	1-1-	9th CO TRK (SP16)
HD2	2-2-	25th " " (SP32)
HD3	3-3-	EXT 200
HD4	4-4-	" 216
HD5	5-5-	" 232
HD6	6-6-	" 248
HD7	7-7-	" 264
HD8	8-8-	" 280
HD9	9-9-	" 296
HD10	0-0-	" 312
HD11	M-M-	" 328
HD12	S-S-	" 344
HD13	C-C-	" 360
HD14	T-T-	" 376
HD15	R-R-	" 392

TABLE F

HORIZONTAL TRANSLATOR NO. 2, BAY 4

DRIVER GATE UNDER TEST	A PARTY		B PARTY	
	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION
HD1	TP1 at 34A19 (CP106)	34A7 (CP102), 38A7 (CP107)	TP1 at 22A19 (CP106)	22A7 (CP102), 18A7 (CP107)
HD2	TP3 " "	" "	TP3 " "	" "
HD3	TP4 " "	" "	TP4 " "	" "
HD4	TP2 " 34A16 (CP106)	" "	TP2 " 22A16 (CP106)	" "
HD5	TP1 " "	" "	TP1 " "	" "
HD6	TP3 " "	" "	TP3 " "	" "
HD7	TP4 " "	" "	TP4 " "	" "
HD8	TP2 " 34A13 (CP106)	34A4 (CP102) "	TP2 " 22A13 (CP106)	22A4 (CP102) "
HD9	TP1 " "	" "	TP1 " "	" "
HD10	TP3 " "	" "	TP3 " "	" "
HD11	TP4 " "	" "	TP4 " "	" "
HD12	TP2 " 34A10 (CP106)	" "	TP2 " 22A10 (CP106)	" "
HD13	TP1 " "	" "	TP1 " "	" "
HD14	TP3 " "	" "	TP3 " "	" "
HD15	TP4 " "	" "	TP4 " "	" "

TABLE G

VERTICAL TRANSLATOR NO. 2, BAY 4

DRIVER GATE UNDER TEST	A PARTY		B PARTY	
	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION	TEST POINT LOCATION	ASSOCIATED TRANSLATOR GATE AND MEMORY REGISTER LOCATION
VD1	TP5 at 42A19 (CP105)	42A7 (CP102), 38A4 (CP107)	TP5 at 14A19 (CP105)	14A7 (CP102) 18A4 (CP107)
VD2	TP1 " "	" "	TP1 " "	" "
VD3	TP2 " "	" "	TP2 " "	" "
VD4	TP4 " 42A16 (CP105)	" "	TP4 " 14A16 (CP105)	" "
VD5	TP5 " "	" "	TP5 " "	" "
VD6	TP1 " "	" "	TP1 " "	" "
VD7	TP2 " "	" "	TP2 " "	" "
VD8	TP4 " 42A13 (CP105)	14A4 (CP102) "	TP4 " 14A13 (CP105)	14A4 (CP102) "
VD9	TP5 " "	" "	TP5 " "	" "
VD10	TP1 " "	" "	TP1 " "	" "
VD11	TP2 " "	" "	TP2 " "	" "
VD12	TP4 " 42A10 (CP105)	" "	TP4 " 14A10 (CP105)	" "
VD13	TP5 " "	" "	TP5 " "	" "
VD14	TP1 " "	" "	TP1 " "	" "
VD15	TP2 " "	" "	TP2 " "	" "