ELECTRONIC DIAL TONE SPEED REGISTER (EDTSR) SD-3B504-01

DESCRIPTION

1. GENERAL

1.01 The electronic dial tone speed register (EDTSR) (Fig. 1 and 2) automatically originates test calls on 1 to 128 spare line circuits to monitor the number of calls on which dial tone is delayed more than 3 seconds.

> ***Warning: This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case, the user at his own expense will be required to take whatever measures may be required to correct the interference.***

1.02 This section is reissued to cover features provided by the addition of switches on CP10 and CP16 per Issue 13B of SD-3B504-01. The following features have been added:

(a) Line indication

(b) Line retest

(c) Delay identification and hold on delay

(d) Dial tone test

(e) Faulty calls peg count.

Revision arrows have been used to denote significant changes.

1.03 The number of test calls and the number of calls on which dial tone is delayed more than 3 seconds is transmitted to registers and/or a centralized data-gathering point, such as Engineering and Administrative Data Acquisition System (EADAS). This data is subsequently used to calculate percent dial tone delay by class of service for use in both office service indexes and traffic engineering applications.

1.04 The EDTSR will handle eight classes of service and is applicable to loop start and ground start circuits, including those involving coin service. The EDTSR requires two wires for connection to a line circuit. It is compatible with all types of electromechanical central offices.

1.05 Switches and indicators are provided for monitoring and checking proper operation of the EDTSR. These switches and indicators and their functions are shown in Tables A and B.

A. Remote Registration

1.06 The output relay board (CP15) is connected to a 405 data set for remote registration. With this remote registration feature, there is a limit of 50 ohms dc conductor resistance. Also, the EDTSR unit is put into the remote mode by operating the LR/LS/RC switch on CP10 to the RC position.

B. Precise or Nonprecise Dial Tone Arrangement

1.07 Precise and nonprecise dial tone arrangements, ranging from drawing Issues 6 through 11AC, are shown in Table C.

1.08 Several types of dial tone are used in the Bell System. The precise tone plan consists of pure tones at 350 Hz and 440 Hz, with close tolerances on both frequency and amplitude. This type is called precise dial tone. All older types are called nonprecise dial tone. The older dial tone is usually either 600 Hz modulated by 120 Hz or 160 Hz with harmonics. All the older types vary widely in both frequency and amplitude because they are usually obtained from

electromechanical rotating motor generators whose speed fluctuates with load and also because of the tone distribution network employed.

Precise Tone Arrangement

1.09 When the local office ringing and tone supply is arranged for precise tone operation, the EDTSR unit must also be arranged for precise dial tone operation. Prior to Issue 9B of SD-3B504-01, the EDTSR was equipped with CP13 line access boards and CP14 dial tone detector. Line access board CP17 may be used for additions or maintenance in the EDTSR.

1.10 On Issue 9B or later, the EDTSR is equipped with CP17 line access boards and CP16 dial tone detector. When all lines are associated with precise dial tone, wiring option J must be installed on CP16.

Nonprecise Tone Arrangement

1.11 When the local office is arranged for nonprecise tone operation, the EDTSR unit must also be arranged for nonprecise dial tone. All EDTSRs are equipped with CP17 line access boards and CP16 dial tone detector. Wiring option J on CP16 is omitted.

Precise and Nonprecise Combination Arrangement

1.12 Central offices having some lines for speed testing with precise dial tone and some with nonprecise dial tone are considered to have all nonprecise tone, and wiring option J is omitted.

2. DESCRIPTION

A. Physical Description

2.01 The EDTSR is a modular unit which contains circuit packs for line access, control, maintenance, and +5 volt power. Power is obtained from −48 volt central office battery. The EDTSR requires approximately 13 inches of space on a standard 23-inch frame.

B. Functional Description

2.02 A block diagram of the EDTSR is shown in Fig. 3. It may be helpful to refer to Fig. 3 for the discussion that follows.

2.03 The EDTSR consists of line access circuits, control circuits, maintenance circuits, and output circuits.

2.04 The master clock (CP11) is a sequential circuit which is controlled by a free-running crystal oscillator. The circuit provides the timing signals required for the EDTSR.

2.05 The line access circuits (CP13 or CP17) consist of one to sixteen circuit packs, each of which contain eight line switches. Each switch is assigned to a line circuit.

2.06 The line sequencer (CP10) scans the line access circuits and causes them to operate the assigned line circuits in a sequential order. The line sequencer is controlled by timing signals from the master clock (CP11).

2.07 The line assignment multiplexer (CP5) monitors programming pins on each circuit pack. If the program pin associated with a particular line switch is strapped to ground, the line sequencer will not attempt to make a test call with that line switch and will skip the next line.

2.08 Dial tone from an operated line circuit is coupled through the line access circuit and an isolation transformer to the dial tone detector (CP14 or CP16). The output of the dial tone detector is monitored by the delay peg count gate and then sent to the class-of-service gates.

2.09 The 3-second timer generates a pulse at the end of the 3-second period which gates the test call and delay peg count gates.

2.10 The test call fault detector receives inputs from the loop current multiplexer and clock signals from the master clock. If loop current is not present, a signal is sent to the display selector so that a visual indication of the failure can be shown. The same signal is sent to the faulty line register and the faulty call counter so that the line switch number where the fault condition occurred can be recorded, and the faulty call counter may be scored.

2.11 The line access circuits (CP13 or CP17) contain class-of-service strapping terminals which are arranged for binary programming by the user. This binary output is multiplexed (CP6) and decoded to decimal (CP5). The output is applied to the class-of-service gates.

2.12 The class-of-service gates (CP5) direct the test and delay peg count to relay outputs

associated with the class of service assigned by the line access circuit. The outputs of these relays operate the message registers ▶or score peg counts at a remote location.◀

2.13 The maintenance panel test call and test call delay counters (CP9) monitor peg count outputs selected by the class-of-service multiplexer. The contents of these counters are monitored via the display multiplexer and selector.

2.14 ▶The line register (P/O CP8) records the line number of the line switch during a test call.◀ The line number is obtained from the line sequencer, converted to binary coded decimal, and stored in the faulty line register.

2.15 The faulty call counter (P/O CP8) is incremented each time a test call cannot be completed because of a fault condition. The total number of test calls attempted can be determined by adding the number of faulty calls to the number of ▶total◀ calls.

2.16 The display circuit (P/O CP8) displays two 3-digit numbers. This circuit monitors the test call and test call delay counters or the faulty line register and faulty call counter via the display multiplexer. A toggle switch is used to select the information shown in the display. The display circuit also contains fault indicators which are lighted when a fault condition is encountered.

3. OPERATION

3.01 The EDTSR originates a test call at a preset rate of 4, 6, 8, or 16 seconds on lines assigned for speed of dial tone measurement. The test call rate, which is programmed into the EDTSR via wire-wrap cross-connections on the master clock circuit pack (CP11), establishes the number of test calls per hour 900, 600, 450, or 225.

3.02 During the first 375 milliseconds of each test call, the EDTSR tests for the presence of loop current. If the test fails, an indication of the failure and the line number experiencing the failure can be determined by indicators on the front of CP2. Any peg counts associated with invalid test calls are blocked from being transmitted to the message registers. The faulty call counter is incremented 3 seconds after the test call starts.

3.03 If the test call passes the preliminary test, a 150- to 200-millisecond time-out starts when a tone is detected. At the end of this time-out, the EDTSR releases the line but stores in its memory that dial tone was present. Three seconds after the test call was started, the dial tone detector output memory is interrogated to determine whether dial tone was present during the test call. At this point, the total calls and class-of-service outputs associated with this line are scored. If dial tone is not detected within 3 seconds, the total and delayed call outputs are scored.

3.04 After terminating a test call, the line sequencer begins scanning the connections to the programming pins on the line access cards for the next assigned subscriber line circuit in the sequence. The next line seizure is made approximately 1, 3, 5, or 13 seconds after the beginning of line scanning (depending on the call rate), and the sequence of events repeats itself.

3.05 The EDTSR has eighteen outputs. There are two outputs for each class of service, one for test call peg count and one for test call delay peg count. The remaining two outputs are for total calls and total delays in all classes of service. These outputs can be used to drive mechanical registers to store peg counts, or they may be transmitted to electronic data gathering systems, such as EADAS.

3.06 ▶For Issue 13B, the output for the eighth class of service is strapped to provide a peg count for faulty calls.◀

4. MAINTENANCE

4.01 To facilitate maintenance of the lines connected to the EDTSR, a designation card (Fig. 4) is mounted on the unit as shown in Fig. 1 and 2. (For clear view of card mounted, see Fig. 5.) The following information may be recorded on this card: equipment location of each line, class of service, whether wired for ground start, and lines not assigned. These assignments should be entered in pencil, on a job basis, so they may be changed by erasing and entering the changed information.

4.02 The EDTSR unit does not require routine maintenance. If the unit fails, the trouble condition can normally be eliminated by circuit pack replacement. Refer to Section 252-100-301 for trouble locating information regarding the EDTSR unit.

TABLE A

SWITCH	LOCATION	FUNCTION
TOTAL CALLS DELAYED CALLS LINE NO. FAULTY CALLS	CP2	Selects display on digital readout of test and delay call counts or test line identification and faulty call count.
FAULTY CONDITIONS CLEAR ALARM CUT-OFF	CP2	Clears LCF, SOD, and line register displays. Retires the office audible and visual alarms.
SOD ON-OFF	CP2	When operated to SOD ON, lights SOD indicator and activates office alarm when a 3-second delay occurs. Also causes line register to hold line number and stops machine.
CLASS OF SERVICE SELECT COUNTER CLEAR	CP2	Selects class of service for digital readout. Clears the test delay and faulty call counters.
DTC DTT*	CP14 or CP16	Prevents detection of dial tone (DTC) or applies 500 Hz signal (DTT).
LR/LS/RC	CP10	LR and LS are local run and local stop; RC allows the EDTSR to be controlled remotely.
RPT TST* ADV*	CP10	Holds a line for repeated testing (RPT TST) or advances to next line (ADV).

*Provided on Issue 13B or later of SD-3B504-01.

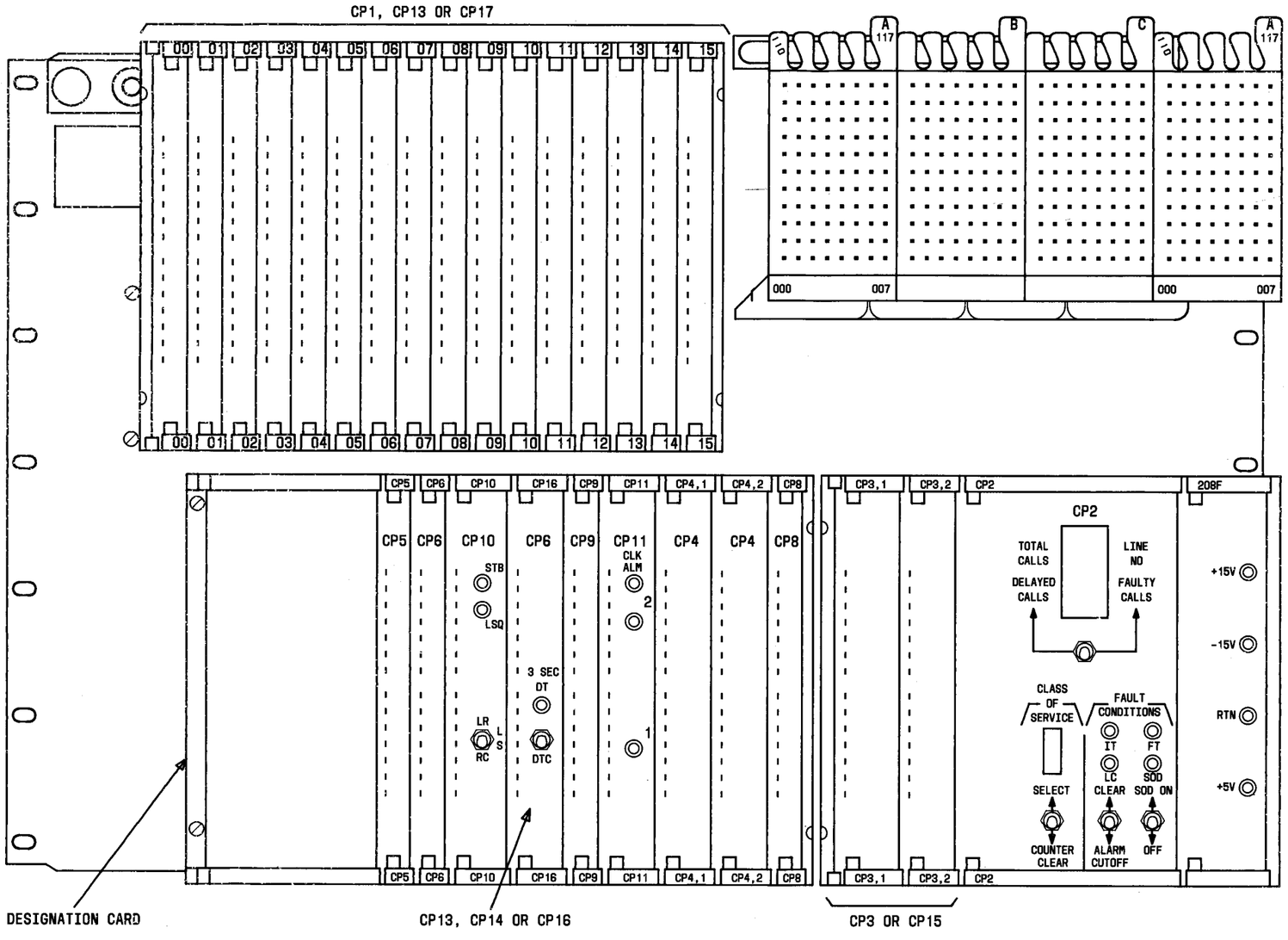
TABLE B

INDICATOR*	LOCATION	FUNCTION
LC SOD	CP2	Lighted when line has no current. Lighted when SOD switch is ON and a 3-second delay occurs.
STB	CP10	Lighted when not making test and flashing when the line sequencer is scanning.
LSQ	CP10	Lighted when the line sequencer exceeds the scanning period for an assigned line switch. The EDTSR must be restored to local stop when this indicator is lighted.
3 SEC DT	CP14 or CP16	Flashes when the 3-second pulse is generated by CP14 or CP16. Lighted when dial tone has been detected.

* Fault Conditions

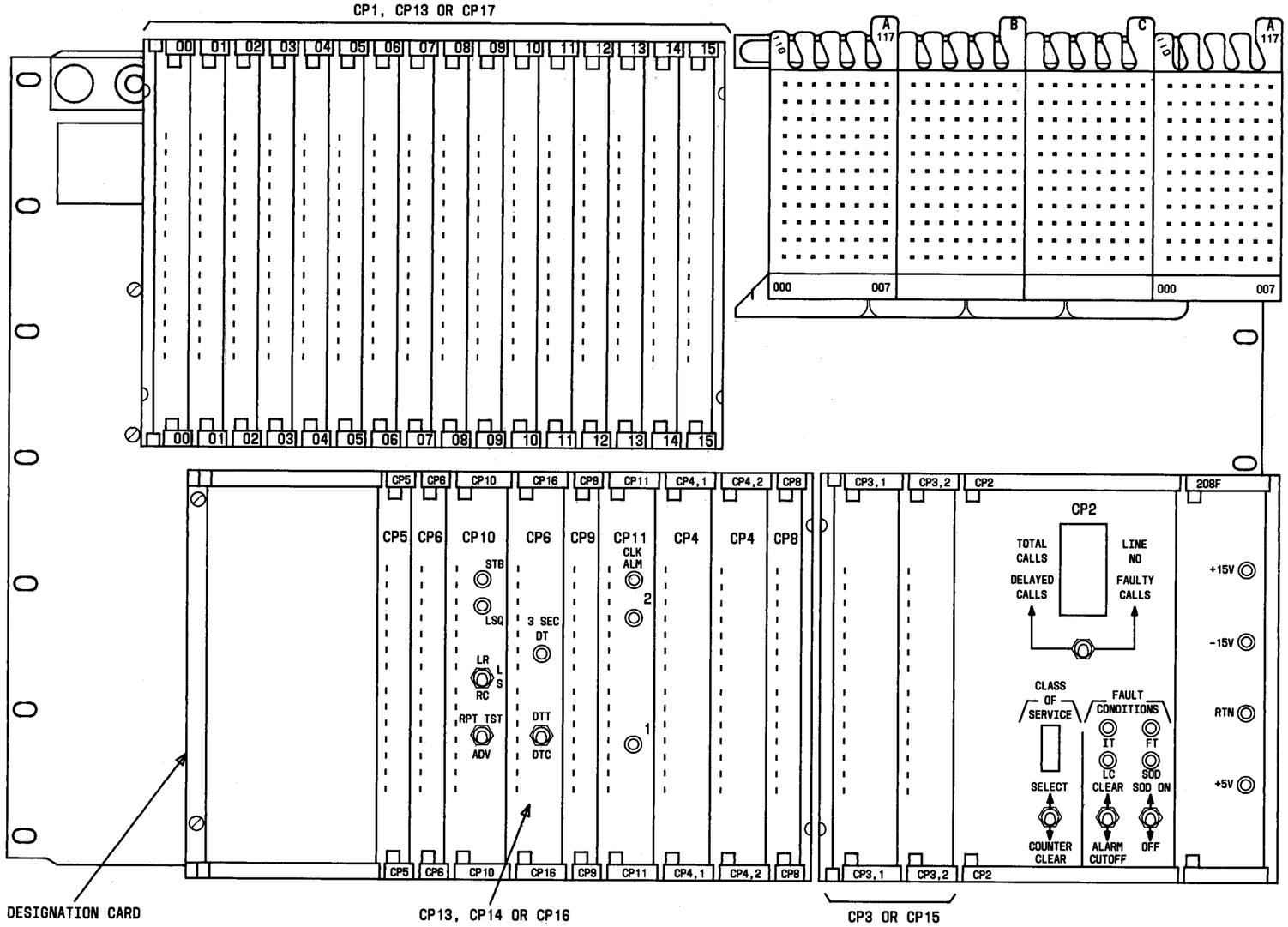
TABLE C

DRAWING ISSUE	CP IN SLOT 17	NOTES
Issues 7AC	CP14	Precise dial tone arrangement.
Issues 8-11AC	CP16 "J" option	Precise dial tone arrangement.
Issue 6	CP7	Precise or nonprecise dial tone arrangement rated MD.
Issue 7AC	CP16	Nonprecise dial tone arrangement.
Issue 8-11AC	CP16	Nonprecise dial tone arrangement.
Issue 8-11AC	CP14	Precise and nonprecise dial tone arrangement.



NOTE:
THE +15V AND -15V OUTPUTS ON THE 208F UNIT ARE NOT CONNECTED

Fig. 1—Electronic Dial Tone Speed Register (Issue 12A, SD-3B504-01 or Earlier)



NOTE:
THE +15V AND -15V OUTPUTS ON THE 208F UNIT ARE NOT CONNECTED

Fig. 2—Electronic Dial Tone Speed Register (Issue 13B, SD-3B504-01 or Later)

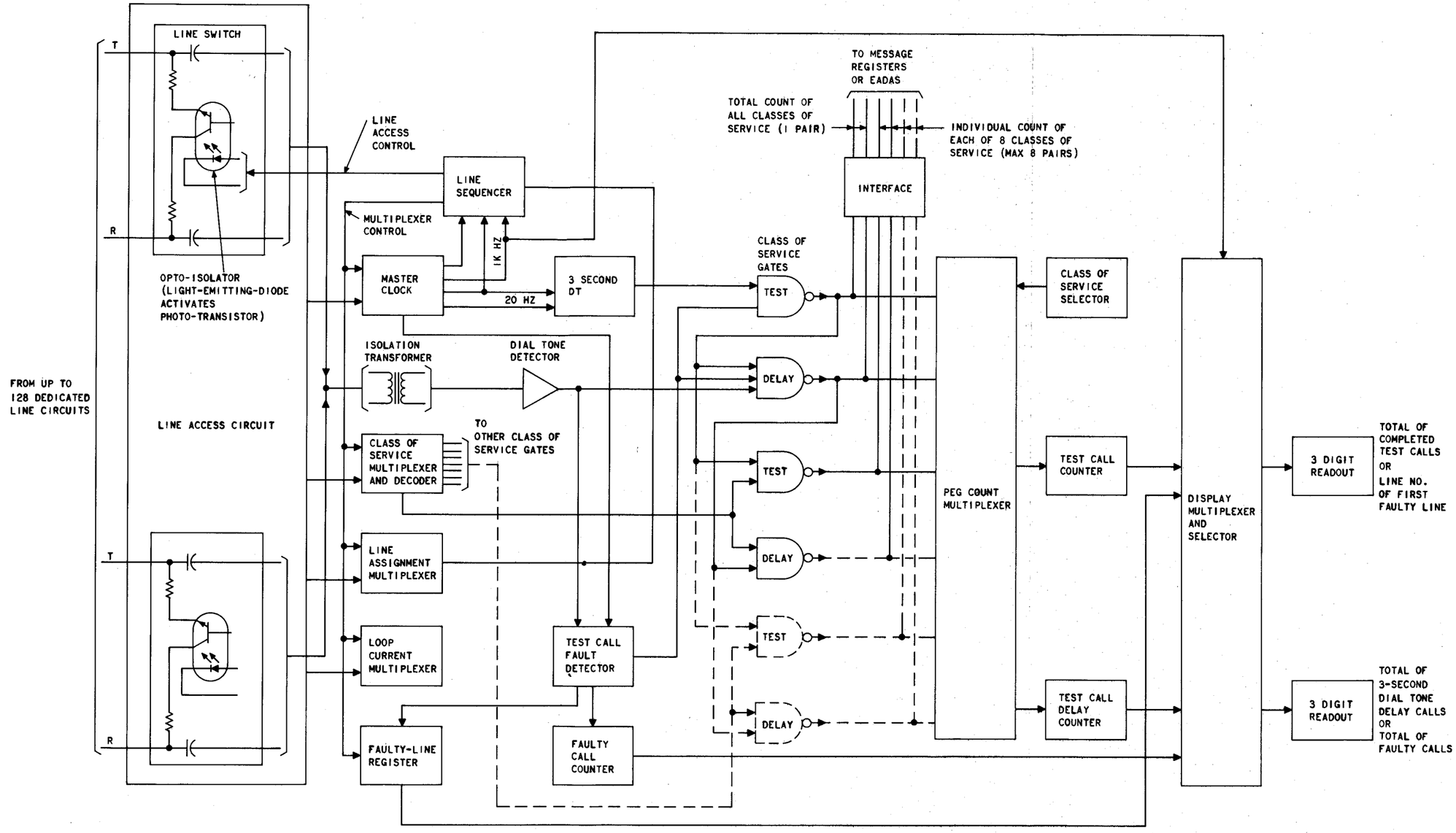


Fig. 3—EDTSR Block Diagram

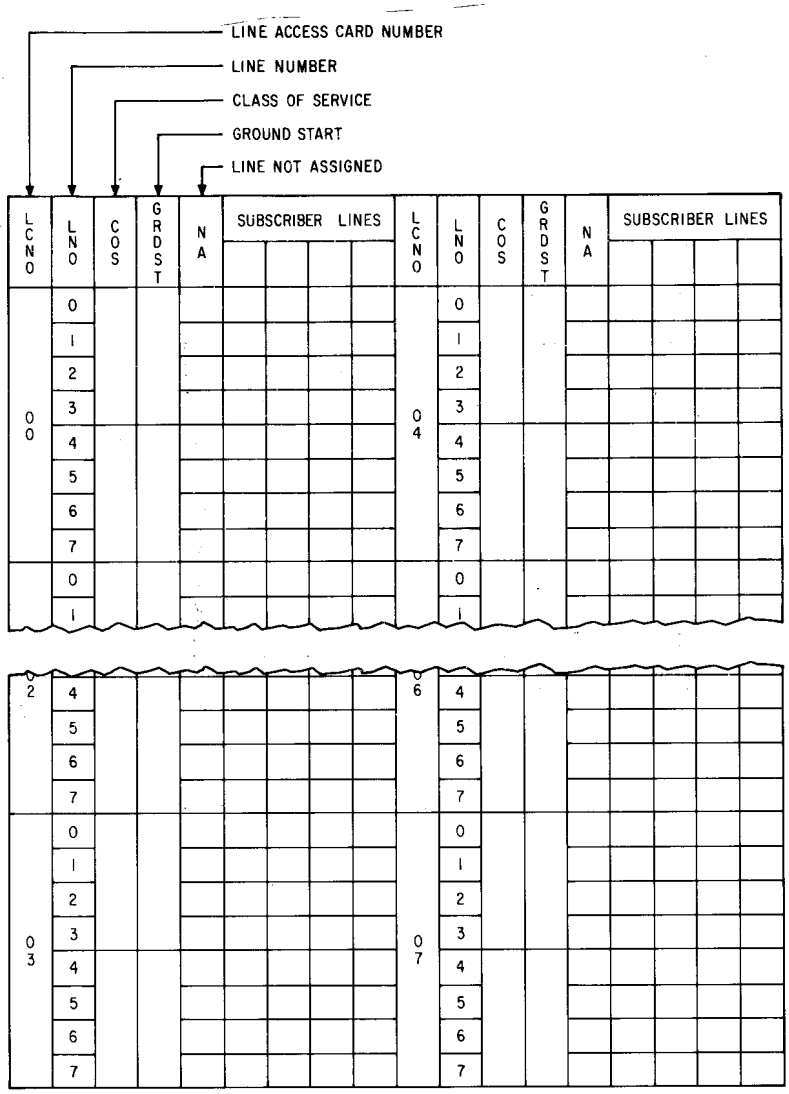


Fig. 4—Example of Designation Card

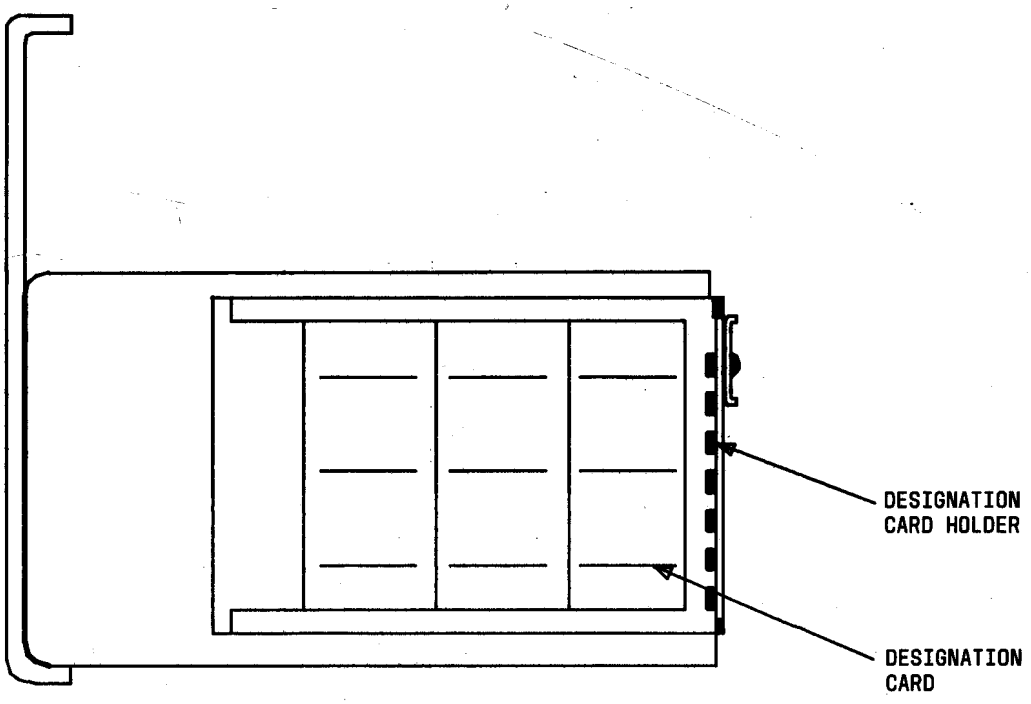


Fig. 5—View of Designation Card Mounted