ENGINEERING AND ADMINISTRATIVE DATA ACQUISTION SYSTEM NETWORK MANAGEMENT (EADAS/NM) DESCRIPTION

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1. GENERAL

1.01 The Engineering and Administrative Data Acquisition System/Network Management (EADAS/NM) is a computerized system which allows centralized, real-time surveillance and control of all levels of the switching hierarchy from regional centers to selected end offices within predefined segments of the network. By analyzing traffic data as it is being gathered from all types of switching machines (via EADAS or peripheral bus computers), EADAS/NM monitors the status of critical switching machine and trunk group functions and reports immediately when potential congestion is evident.

1.02 Whenever this section is reissued, the reasons for reissue will be listed in this paragraph.

1.03 EADAS/NM employs either a Digital Equipment Corporation (DEC*) PDP 11/70 processor and peripherals or a PDP 11/45 processor and peripherals to provide the following features:

- ***Real-time surveillance of switching and trunk group interaction.*** This function is accomplished by performing calculations at five-minute intervals on the most recently acquired register data, by analyzing the status of selected discretes and alarms and then reporting any specific exceptions to the network manager for possible action.

- ***A new network status display system which is driven by the calculated exceptions found in the five-minute data analysis and by the status of selected discretes and alarms.*** This display system consists of cathode ray tube (CRT) terminal devices, and a modular wall display board.

- ***Centralized, remote network management control capability using the interactive mode of the CRTs.*** This enables the responsible network manager to institute control measures quickly when required to maintain and protect the call carrying capacity of the network.

1.04 A block diagram of the total EADAS/NM system configuration with the PDP 11/70 computing system is shown in Fig. 1. Fig. 2 is a block diagram of the total EADAS/NM system configuration with the PDP 11/45 computing system. Substantial savings have been realized by integrating

EADAS with the network management system (EADAS/NM). The terminal equipment at the switching locations and the dedicated data links, which together amount to the major cost of these systems, will be shared.

1.05 Manual controls are centralized in the EADAS/NM center, although full over-ride capability remains at each office. CRT terminal keyboards, rather than hardware consoles, are used to insert and remove controls. For end offices, control commands are passed through EADAS into the respective office via the EADAS traffic data converter (ETDC). For toll offices, the volume of control options may be so large that the reverse channel on the E2A telemetry link is used rather than the ETDC.

1.06 A typical example of a network management center layout for an EADAS/NM installation is shown in Fig. 3.

2. TYPES OF DATA COLLECTED

2.01 The EADAS/NM collects two categories of data—measures and discretes.

A. Measures

2.02 Measures are five-minute summaries of peg count and usage traffic data transferred to EADAS/NM directly from peripheral bus computers (PBCs) and basic EADAS computers. The EADAS computers obtain unprocessed data from EADAS traffic data converters (ETDCs), pollable data terminals, and No. 1 Electronic Switching System (ESS) terminals. EADAS/NM performs arithmetic operations on this data to convert the data to quantities more meaningful to network managers such as marker peg count, attempts per circuit per hour (ACH), completions per circuit per hour (CCH), and percent overflow. Measures are stored for 20 minutes and can be displayed on the CRT for intervals of 0 through 5, 0 through 10, 0 through 15, or 5 through 20 minutes.

B. Discretes

2.03 Discretes consist of office status information such as sender delay, dynamic overload control (DOC) received, and sender queue low/high. Discretes are received either directly into EADAS/NM via E2A links to No. 4A/4M crossbar or large crossbar tandem machines or via data collection computers such as EADAS. Discretes are collected at 20-second intervals. They may be printed on the monitor, but stored only for 20 seconds.

3. SOFTWARE SUBSYSTEMS

3.01 The EADAS/NM has three software subsystems which use the measures- and discretes-type data to drive various types of displays. These subsystems are: exception subsystem, monitor subsystem, and demand subsystem.

A. Exception Subsystem

3.02 The exception subsystem provides continuous network surveillance and alerts the network management force of abnormal network conditions. Every five minutes, it performs calculations on the collected measures and compares the results to predefined user assigned thresholds. Calculation results, which exceed their thresholds, activate user-assigned indicators on the wall display board. Also, calculation results and other related information can optionally be printed on one of the receive-only printers (ROPs) known as the exception printer. Additionally, a one-second contact closure can be activated to operate a user-provided audible exception alarm. Further, the current state of the discretes is used to activate user-assigned display board indicators every 20 seconds.

B. Monitor Subsystem

3.03 The monitor subsystem provides a flexible and versatile method of automatically monitoring a limited quantity of data that is of special interest to a network manager. For example, a trunk group affected by a traffic control may be monitored for excessive occupancy or conversely, too few attempts. The monitor subsystem provides the user with an expanded calculation set (as compared to the exception subsystem) and a more flexible thresholding arrangement. Monitor calculation results outside specific threshold limits may activate wall display board indicators, print messages on the second ROP (known as the monitor printer), or activate the audible alarm—all at the discretion of the network manager. Also, a printed history of the status of discretes of special interest to the network manager can be obtained using the monitor subsystem.

C. Demand Subsystem

3.04 The demand subsystem is used to analyze and control abnormal network conditions. It consists of up to five DATASPEED ® 40 station arrangements in a keyboard, display, printer (KDP) configuration. These are used interactively to retrieve, analyze, and display measures, calculation results, and discretes for the network manager. This is done using a variety of generic display formats. Each of these formats is designed to present a unique aspect of the data. This subsystem provides the network manager with essentially unlimited flexibility in analyzing the data collected by the system. In addition, the CRTs are used to provide a centralized capability of taking controls and a means of updating the nongeneric reference data base of the system.

4. DISPLAY SYSTEM

4.01 The display system consists of two major components. A ***wall display board*** is used to alert the network manager to exception conditions. The ***CRT terminal devices*** are used to obtain detailed data from the computer.

A. Wall Display Board

4.02 The wall display board (Fig. 4) is manufactured by Ferrante-Packard, LTD., and consists of an array of luminescent, reflective, electromagnetically controlled indicators. The maximum number of indicators which can used per wall display board is 4095. These are arranged in columns, with each column having up to four panels. The maximum number of columns is eight with each column containing a maximum of 512 indicators.

4.03 A standard display layout has been designed for all EADAS/NM. Sufficient flexibility has been designed into the wall display board in order to allow a given display to meaningfully reflect local network configurations.

4.04 The wall display board consists of two types of columns. ***Internal columns*** reflect exception conditions in offices of the EADAS/NM cluster intra-EADAS/NM cluster trunk groups. ***External columns*** reflect trunk group exceptions from offices of the EADAS/NM cluster out to the world as well as limited machine status for switches outside the EADAS/NM cluster. A typical wall display board might have four to six internal columns and four to six external columns. For example, an EADAS/NM for the 201 numbering plan area (NPA) of Northern New Jersey might be arranged as shown in Fig. 5.

4.05 Each internal column is 36 inches in width, and each external column is 22 inches in width. Columns are 88 inches in height and consist of up to four standard panels. Each panel is 22 inches in height.

B. Cathode Ray Tube (CRT) Terminal Devices

4.06 The CRT terminal devices are system standard DATASPEED 40 station arrangements (Fig. 6) in a KDP configuration. They can be obtained for table top or pedestal mounting.

4.07 Transmission to and from the DATASPEED 40 will be asynchronous at 1200 baud via standard 202T data sets. The printer is a line-at-a time device which through selection of the PRINT LOCAL/PRINT ON LINE keys, will copy either the data currently being displayed on the CRT (actually stored in the display logic circuits) or the data currently being transmitted (received). A maximum of five DATASPEED 40 station arrangements can be accommodated per EADAS/NM center.

5. CENTRAL UNIT EQUIPMENT (PDP 11/70)

A. Equipment Layout

5.01 The EADAS/NM CU consists of five computer cabinets, free-standing disk memory, a free-standing DECwriter, and optionally a table top card reader as shown in Fig. 7. The drawer configuration as related to the five computer cabinets is shown in Fig. 8. No cabinets or drawers are optional. Two or three other computer cabinets are provided, as part of the same equipment lineup, to house the WECo equipment.

5.02 The five basic computer cabinets house the DEC PDP 11/70 CU hardware. This includes the processor, 256 K words (512 K bytes) of core memory, a nine-track 800 bpi magnetic tape unit, and other associated equipment as shown in Fig. 7 and 8. The WECo hardware in the other computer cabinets includes the E2A telemetry, data sets, alarm circuit, wall display board drive circuit, telemetry computer translators (TCTs), power distribution, interfaces, etc.

B. Power Requirements

5.03 The computer room should be supplied with three-phase WYE 115/208 vac ±10%, 60 Hz ±1%. The power distribution to each cabinet and free-standing peripheral is shown in Table A. An individual circuit breaker must be supplied for each cabinet and free-standing peripheral. The neutral must not be connected to the frame of any equipment or to the protective ground except at the building's main electrical service entrance. Recommendations are provided on phase assignment to provide a reasonably balanced load. Only the RP04 disk is a true three-phase device. The processor cabinet and the memory cabinet require two of the three phases.

5.04 Where commercial power is reliable, it is often reasonable to supply the entire system from commercial power with the ability to switch to essential power (an engine alternator set) in the event of a power failure. Commercial power is guaranteed to average 60 Hz from which EADAS/NM derives its time-of-day clocking from the line frequency. In the event of a power failure, the EADAS/NM system must be rebooted. Generally, this can be accomplished from the disk in about five minutes after power is restored. In rare circumstances it may be necessary to reboot from magnetic tape. This requires about 45 minutes. A power outage will result in false carrier failure indications to PBCs and Electronic Translator System (ETSs), and possibly the loss of the last five-minute data summaries. This backup power arrangement should be used where the engine alternator set is guaranteed to meet the relatively severe 60 Hz ±1% frequency requirement of the disk. Most KS engine alternator sets can be modified to meet this requirement. It is recommended that the sets be modified.

5.05 Where the frequency requirement cannot be met, a three-phase inverter meeting the frequency requirement is recommended to power the disk only. The rest of the system can be operated on commercial power. For reliability, the entire system may be powered from inverters. It must be understood that much of the effectiveness of EADAS/NM may be lost during a power outage even if EADAS/NM is maintained on uninterruptable power unless the PBCs and data collection systems are also operated on uninterruptable power. Also the KDPs, ROPs, and wall display board must be quickly restored to operation if the center is to be effective. During a long power outage, a loss of air conditioning may be of concern since the disk operation is guaranteed to only 90°F (32°C).

C. Alarms

5.06 The EADAS/NM uses the BD04 disk interrupt and alarm circuit (SD-3B219-01) to implement the alarm functions. The disk interrupt portion of the BD04 is not used. A cable carrying EIA level signals connects the BD04 to the alarm driver circuit pack in the EADAS/NM data terminal circuit. The BD04 detects ac low, dc low, software major, software exception, and program caught in loop conditions. The EADAS/NM alarm conditions and the expected responses are listed in Table C. A typical software major alarm would be the detection of repeated DQ11 failures resulting in the DQ11 being switched off-line. As indicated in Table C, both the audible and major visible alarms will be triggered by a major alarm. The user will reset the audible alarm by an audible alarm reset switch on the alarm panel. When the trouble has been cleared, the user will reset the major visible alarm by typing the appropriate message on the DECwriter.

5.07 The exception alarm is what the BD04 circuit refers to as a minor alarm. The selection of which exceptions trigger the exception alarm, is left to the user's descretion. Only critical exceptions should be assigned to the exception alarm. In addition to the audible and visual alarms listed in Table C, the exception alarm causes a loop closure of one-second duration of the remote exception alarm leads which can be used to remote a user-selected alarm to the network management center.

5.08 The program timer alarm is intended as a check on whether the program is caught in a loop. It is often referred to as a "sanity alarm". The EADAS/NM software is designed to reset the program timer at one-second intervals. The loop hardware timer times for a 1 1/2-to-2 1/2 second interval. If the software does not reset the timer before the expiration of the 1 1/2-to-2 1/2 second interval, the audible and major visible alarms will be activated.

Major Alarm Status

5.09 The alarm circuit provides visible and audible alarms when specified malfunctions occur within the CU. Major alarms may be activated

by both software and hardware conditions. When a major alarm is detected, the major alarm indicator is illuminated and the audible SONALERT alarm is activated on the alarm panel.

5.10 The ac low and dc low are two major alarms that indicate malfunctions in the DEC power supplies. When detected, the appropriate indicator is illuminated along with the major alarm audio and visual indicators. These conditions will cause the computer to fatally malfunction. Power to the alarm circuit +24 volt is indicated by the power indicator. The EADAS/NM software is monitored by the alarm circuit, and if not functioning, a major alarm is activated.

Exception Alarm Status

5.11 Exception alarms, when detected, activate the exception alarm indicator and the audible alarm. Minor alarms in network management are considered exception alarms and are software activated. When such a situation exists, the exception alarm indicator is illuminated and the audible alarm activated for a short period of time.

5.12 Both major and exception alarms can be remotely located from the CU. These remote alarms can be deactivated by switching the major and exception alarm switches to the CUTOFF position.

D. PDP 11/70 processor

5.13 The PDP 11/70 is the most powerful computer in the PDP 11 family. It is designed to operate in large, sophisticated, high-performance systems. Therefore, the PDP 11/70 is adaptable to EADAS/NM.

5.14 The PDP 11/70 contains, as an integral part of the central processor unit, the following hardware features and expansion capabilities:

(1) Cache memory organization to provide very fast program execution speed and high system throughput

(2) Memory management for relocation and protection in multi-user, multi-task environments

(3) Ability to access up to two million bytes of main memory (1 byte = 8 bits)

(4) Optional high-speed, mass storage controllers as an integral part of the PDP 11/70 processor, to provide dedicated paths to high performance storage devices

5.15 The PDP 11/70 processor performs all arithmetic and logical operations required in the system. Memory management is standard with the basic computer, allowing expanded memory addressing, relocation, and protection. Also standard is a UNIBUS map which translates UNIBUS addresses to physical memory addresses. The cache memory contains 2048 bytes of fast, bipolar memory that buffers the data from main (core) memory.

5.16 The PDP 11/70 system has an expanded internal implementation of the PDP 11 architecture for greatly improved systems throughput. All the memory is on its own high data rate bus. The internal high-speed input-output controllers for mass storage devices have direct connections through the cache to memory for transferring data. The processor has a direct connection to the cache memory system for very high-speed memory access.

E. Core Memory

5.17 The EADAS/NM configuration utilizes 256K words (512 K bytes) of core memory. Some of the core memory is provided by the processor code and the remainder is provided by MEM1, MEM2, and MEM3 (Fig. 1). The lowest 35K of core memory contains the EADAS/NM operating system which is essentially a UNIX operating system with modifications required to handle the unique input/output requirements of EADAS/NM. Modifications to UNIX include the addition of drivers for the TCTs, wall display board, DATASPEED 40 KDPs and ROPs, the alarm circuit and the DQ11 interfaces to basic EADAS.

Memory Organization

5.18 A memory can be viewed as a series of locatons with a number (address) assigned to each location. Because PDP 11 memories are designed to accommodate both 16-bit words and 8-bit bytes, the total number of addresses does not correspond to the number of words. An 8K-word memory can contain 16K bytes and consist of 037777 octal locations. Words always start at even-numbered locations.

5.19 Certain memory locations have been reserved by the system for interrupt and trap handling, processor stacks, general registers, and peripheral device registers.

Parity

5.20 Parity is used extensively in the PDP 11/70 to ensure the integrity of information. All memory has byte parity. Parity for both data and addresses is generated on transfers to memory and is checked on all transfers from memory. Registers are provided within the processor to provide information on the location of parity errors, types of errors, and other relevant information so that software can respond to the situation, take corrective action, and log the occurrence of errors.

Address Space

5.21 Three separate address spaces are used with the PDP 11/70. The main memory uses 22 bits for a physical memory space of over four million bytes. The UNIBUS uses an 18-bit address for a UNIBUS space of 256K bytes. The computer program uses a 16-bit virtual address for a program virtual space of 64K bytes.

F. Cache Memory

5.22 The cache memory is a small, high-speed memory that maintains a copy of automatically selected portions of main memory for faster access to instructions and data. A computer system using cache memory appears the same as a conventional system with core memory except that the execution of programs is much faster. The only difference is in the system timing. There are no changes in programming. The cache memory is completely transparent to all programs. The programs are treated as if there were one continuous bank of memory.

5.23 The main memory is replaced by a combination of cache memory plus main memory. The cache system simulates a system having a large amount of fast memory. The cache uses a small amount of very fast semiconductor memory. The main memory uses slower core memory. The key to the effectiveness of a cache memory is the algorithm which automatically and dynamically transfers the data most needed to the fast memory.

5.24 Whenever a request is made to retrieve data from memory, the cache circuitry checks to see if that data is already in the cache. If the data is in the cache, it is retrieved from the cache memory and no main memory read is required. If the data is not in cache memory, four bytes are retrieved from main memory and stored in the cache with the requested word or byte being passed directly to the central processor. When a request is made to write data into memory, it is written both in the cache memory and in the main memory assuring that main memory is always updated immediately.

5.25 The key to the effectiveness of the PDP 11/70's cache memory is in its size. Because it holds 2,048 bytes (1,024 words) at any given point in time, and because programs tend to use localized sections of code and data, the PDP 11/70 cache memory already contains the next needed data word a very high percentage of the time.

5.26 The fundamental concern in using cache memory is excution speed. This is affected by the speeds of fast memory (cache) and slow memory (core) and by the percentage of times memory references will find the data within the cache memory and, therefore, allow faster execution.

G. UNIBUS Structure

5.27 The UNIBUS is a common, high-speed data path that interconnects the processor and all devices within the CU. It is a 120 conductor flexprint cable (white in color) that weaves through the devices that are a part of the CU. The UNIBUS provides the communications path for address, data, and control information for all devices on the UNIBUS through its bidirectional lines. Therefore, the same device registers can be used for input and output functions.

5.28 Devices communicate on the UNIBUS in a master-slave relationship. During any UNIBUS operation, one device has control of the UNIBUS. This device, called the master, controls the UNIBUS when communicating with another device, called the slave. The relationship is dynamic; thus the central processor as master could send control information to a disk (slave) which then could obtain the UNIBUS as a master and communicate with memory, the slave.

5.29 The UNIBUS is used by the processor and input/output devices connected to the UNIBUS. A priority structure determines which device has control of the UNIBUS at any given instant of time. Therefore, every device capable of becoming master has an assigned priority; and when two devices request the UNIBUS at the same time, the device with the higher priority will receive control first.

5.30 All UNIBUS bidirectional lines use negative logic and all unidirectional lines use positive logic. All other system device logic is positive.

5.31 All devices attach to the UNIBUS by paralleling off the desired signal and control lines as the lines are passed serially through the device enroute to the UNIBUS terminator (located on the end of the UNIBUS section). The only information which is not attained in this manner comes over the bus grant (BG) lines which are serially passed through the devices requiring these signals as they are physically arranged on the UNIBUS in distance from the processor. Fig. 1 shows a typical EADAS/NM CU UNIBUS structure. Fig. 9 shows the UNIBUS sequence of apparatus.

5.32 Fig. 10 shows a UNIBUS bidirectional line and all devices have either a UNIBUS receiver IC (380) or a UNIBUS driver IC (8881). On a data out (DATO) transfer, the driver of one device (i.e., PDP 11 processor) and the receiver of another device (i.e., channel interface drawer) are enabled. This allows the data in the processor to be passed to where the address line instructs it to go. The address lines basically control which device is enabled. The control lines tell whether the 380 UNIBUS receiver or the 8881 driver is enabled, indicating the direction of the data transfer.

H. TWU16 Magnetic Tape

5.33 The EADAS/NM system uses the TWU16 magnetic tape subsystem. This provides industry standard recording formats with program selectable densities of 1600 and 800 bpi. EADAS/NM uses the 800 bpi format. The magnetic tape unit is used to load the EADAS/NM generic program into the computer system. It is recommended that the system be backed up on magnetic tape at least once per week. This ensures that a backup system containing relatively current data base information is available in case of a failure which scribbles the disk. Also, the magnetic tape subsystem serves as the input medium for the DEC-supplied diagnostic programs. Both the WECo supplied generic programs and the DEC supplied diagnostic programs are on 800 bpi density tape.

5.34 The TWU16 magnetic tape system is a fully integrated, high-performance magnetic tape storage system that is specifically designed to operate the DEC's PDP 11 computers. Reading and writing are performed at 45 inches per second with a transfer rate of 72,000 characters per second. Each reel contains a nine-track data storage magnetic tape that can store up to 40 million characters.

5.35 Each vertical frame of the nine-track tape represents one character and contains eight data bits plus one parity bit. Since the 16-bit PDP 11 word contains two 8-bit bytes, one byte corresponds to one tape character for efficient data storage.

I. RWP04 Moving Head Disk

5.36 The EADAS/NM system uses an RWP04 moving head disk subsystem (Fig. 11) with a single drive. The single drive has a formatted data capacity of 88 million bytes. About one-half of this capacity is used by a typical EADAS/NM system. More than one-third of the capacity used will contain data base information. Another one-third of the capacity will contain programs directly supporting the more than 40 EADAS/NM display pages. The remaining one-third of the capacity will contain other programs. The removable disk pack offers the flexibility of unlimited off-line storage capacity.

5.37 The RWP04 moving head disk subsystem operates at a transfer rate of 403,000 words per second (2.5 microseconds per word). The average access time is 36 milliseconds, which includes the time for head positioning and rotation latency. Data transfers can be made in block sizes of from 1 to 65,536 words. The system utilizes a first-in/first-out, 66 word data buffer to facilitate smooth UNIBUS data flow.

5.38 Parity checking is performed on both data and control information transfers for increased reliability. The controller also detects and flags memory parity errors. The disk system interrupts the processor on completion of a command and on error conditions. Extensive error indicators exist

for easy on-line diagnosis and numerous status indicators give complete program control.

J. LA36-CA DECwriter II

5.39 In the EADAS/NM system the LA36-CA DECwriter's primary functions involve testing. It is used as the input/output terminal during the running of the off-line DEC diagnostic programs and for some on-line EADAS/NM system tests.

5.40 The LA36-CA DECwriter II (Fig. 12) is loaded with many practical and functional operator features. It has 30-character per second throughput accomplished by a 60 Hz catchup mode which is activated any time that more than one character is in the 16-character buffer. Also featured are quiet operation, infinitely variable vertical forms adjustment, variable forms width, and multi-part forms capability.

5.41 The LA36-CA DECwriter II prints from a set of 64 characters at speeds up to 30 characters per second. It can receive at either 110, 150, or 300 baud, depending on the switch setting. The stated EADAS/NM data rate is 300 baud.

K. DL11-A Serial Line Interface

5.42 The DL11-A serial line interface is a character-buffered communications interface that performs two basic operations of receiving and transmitting asynchronous data between the CU and the LA36-CA DECwriter II console. When receiving data, the interface converts an asynchronous serial character from the LA36-CA DECwriter II console into the parallel character required for transfer to the UNIBUS. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When transmitting data, a parallel character from the bus is converted to a serial line for transmission to the LA36-CA DECwriter II console. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operate through two related registers: a control and status register for command and monitoring functions, and a data buffer register for storing data prior to transfer to the bus or the LA36-CA DECwriter console.

L. BD04 Disk Interrupt Driver and Alarm Circuit

5.43 The BD04 disk interrupt driver and alarm circuit (SD3B219-01) allows the processor to indicate alarm conditions detected by the software within the CU. The alarm circuit also monitors the program base level loop time to verify that it is less than 2.0 seconds. A provision is also added for the processor to reset all generated alarm conditions by entering a command on the DECwriter.

5.44 In addition to the software-detected alarms, the alarm circuit has circuitry to detect any ac or dc low asserted on the UNIBUS. This will illuminate the respective failure lamp on the alarm panel.

5.45 The minor alarm feature of the alarm circuit is used in the EADAS/NM system to provide for an audible exception alarm in the network management center.

5.46 The disk interrupt feature is not used in the EADAS/NM system.

5.47 See 5.06 through 5.12 for additional information on alarms.

M. DH11-AA Asynchronous 16-Line Multiplexer

5.48 The DH11-AA asynchronous 16-line multiplexer connects the PDP 11 to 16 asynchronous serial communications lines operating with individually programmable parameters.

5.49 The DH11 multiplexer uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the silo. The bottom of the silo is a register which is addressable from the UNIBUS.

5.50 The transmitter in the DH11 also uses double buffered MOS/LSI units. They are loaded directly from message tables in the PDP11 memory by means of single-cycle direct memory transfers—non processor request (NPR). The current addresses and data byte counts of the message table for each line are stored in semi-conductor memories located in the DH11. This reduces the UNIBUS time required for NPR transfers to one NPR cycle per character transmitted.

5.51 The DH11-AA consists of all modules necessary to implement a 16-line asynchronous multiplexer. An externally mounted 5 1/4 inch level conversion and distribution panel with its own power supply that is mounted near the top of cabinet 5, and a data cable between the logic in the double system unit and the level conversion/distribution panel.

N. DQ11-DA Synchronous Line Interface

5.52 The DQ11-DA synchronous line interface is a double-buffered single-line synchronous interface which is compatible with the 209 data set or equivalent. The interface provides parallel-to-serial and serial-to-parallel data conversion, level conversion, character recognition, error detection, and modem control for full-duplex data communications operating at 9600 baud.

5.53 Transmit and receive data transfers between the PDP 11 UNIBUS and the DQ11-DA synchronous line interface are handled as NPRs. These are direct memory or device access data transfers without processor supervision. As an NPR device, the DQ11-DA synchronous line interface provides extremely fast access to the PDP 11 UNIBUS and can transfer data at exceptionally high rates once it gains control. The PDP 11 processor state is not affected by types of transfers since they occur on a cycle steal basis.

5.54 The DQ11-DA synchronous line interface contains diagnostic-controlled, self-testing facilities to ensure both the quality of the data converters and control logic, and to minimize on-line malfunctions.

O. DR11-C Interface

5.55 The DR11-C interface is a general purpose interface between the UNIBUS and the peripheral equipment, such as the wall board display and an interface to E2A terminals via TCT(s) in the EADAS/NM data terminals circuit SD-3B230-01. It provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between the CU and the external device. The interface also includes status and control bits that may be controlled by either the CU program or the external device for command, monitoring, and interrupt functions.

5.56 The interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

5.57 The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

5.58 The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the external device.

5.59 The interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

5.60 If an output operation is specified, information from the UNIBUS is stored in a 16-bit register. Once this buffer has been loaded under program control, the outputs are available to the external device until the register is loaded with new data from the bus. Upon transfer of data to the buffer register, a "new data ready" control signal is supplied to indicate to the external device that data has been loaded.

5.61 When an input operation is specified, the DR11-C provides 16 lines of input to UNIBUS transmitters. This permits data from the external device to be read into the bus. A control signal "data transmitted" informs the device that input lines have been read.

P. DB11-A Bus Repeater

5.62 The DB11-A UNIBUS extender allows physical and electrical extension of the UNIBUS. Each DB11-A allows a 50-foot extension in the bus length and will drive 19 extra bus loads. Therefore, the addition of one DB11-A bus repeater allows a total of up to 38 devices (excluding the DB11-A) for a net gain of 18 bus loads. Most PDP 11 options that interface to the UNIBUS are one bus load.

5.63 All UNIBUS signals are carried through from one side to the other by the DB11-A.

Inclusion of a UNIBUS extender in the PDP 11 system imposes no operational changes and no timing restrictions. The operation is transparent to programming and there are no addressable registers. The UNIBUS cycle time is unaffected for devices on the same side of the extender and increase a maximum of 375 nsec for devices on the opposite sides.

Q. H312A Null Modem

5.64 The H312-A null modem allows a user to connect a terminal device to a computer without the use of two modems as would normally be required. It consists of two female 25-pin data-phone sockets mounted on a printed circuit board with the 15 most commonly used wires brought out to split lugs in the center of the board. The split lug allows the user to interconnect the two sockets in any way he/she wishes as long as the pins used are on the split lug interconnection points.

R. KW11-L Line Clock

5.65 The KW11-L line clock divides time into intervals of 16 2/3 milliseconds or 20 milliseconds, determined by the line frequency of 60 Hz or 50 Hz. The accuracy of the clock period is that of the frequency source.

5.66 The KW11-L line clock operates in either the interrupt mode or the noninterrupt mode. In the interrupt mode, an interrupt is generated for each cycle of the line frequency. In the noninterrupt mode, the program checks a monitor bit for timing information.

5.67 All EADAS/NM timing is obtained from the line clock operating in the interrupt mode. With an input line frequency of 60 Hz, the clock generates an interrupt every 16 2/3 milliseconds. Since the accuracy of the clock frequency is that of the frequency source, if the input frequency does not average 60 Hz, it will occasionally be necessary to reenter the time of day into the system.

S. CR11 Card Reader (Optional)

5.68 The CR11 card reader reads EIA standard 80-column punched data cards at 300 cards per minute. Cards are read by column beginning with column 1. A read command starts the card moving part the read station. Once a card is in motion, all 80 columns are read. Column information is read in one of two program-selected modes: compressed or image. In the compressed mode, the 12 information bits in one column are automatically decoded and transferred into the least significant half of the card reader data buffer (CRB2) as 8-bit compressed code. In the image mode, the 12 bits of a column are transferred directly into CRB1 so that zone 9 is transferred into CRB bit 0 and zone 12 is transferred into CRB bit 11. A punched hole is interpreted as binary 1 and the absence of a hole as binary 0.

T. Data Sets

5.69 The 108D, 202T, and 209A data sets are used in the EADAS/NM for interfacing the CU with various data collection and receiving devices via dedicated facilities.

108D Data Set

5.70 The CU has the capability of interfacing with ETS controls via the channel 2 teletypewriter port of the No. 4 Crossbar ETS switching machine. A maximum of 16 No. 4 Crossbar machines may connect to the CU. The information is transmitted from the CU with the use of a DH11-AA asynchronous 16-line multiplexer. The DH11-AA asynchronous 16-line multiplexer interfaces to a 108D data set with the use of DM11-DB circuit boards on the DH11 distribution panel and a standard interconnection E1A cable per channel.

202T Data Set

5.71 The EADAS/NM provides the capabilities of interfacing a minimum of two and a maximum of five DATASPEED Model 40 KDPs and two ROPs with the CU. These units are interfaced with the CU via a 202T data set and a dedicated two-wire 1200-baud facility.

5.72 The EADAS/NM CU has the capability of interfacing with a maximum of eight TCTs. Each TCT can be connected to a maximum of four E2A remote units via a multiport data bridge. The CU uses are DR11-C general purpose interface to interface with one TCT. The TCT is connected to a 202T data set which connects to a 1200-baud, dedicated four wire, unconditioned, 3002-type data facility.

209A Data Set

5.73 Interconnection between the EADAS/NM CU and a maximum of six remote or colocated EADAS systems is accomplished with the use of DQ11-DA interfaces. Remoted EADAS systems are interfaced to EADAS/NM CUs with the use of 209A data sets and dedicated line facilities, while colocated EADAS systems are directly connected with null modems.

6. CENTRAL UNIT EQUIPMENT (PDP 11/45)

A. Equipment Layout

6.01 A typical equipment layout of the EADAS/NM central unit (CU) is shown in Fig. 13. Fig. 14 shows the drawer configuration for the CU. The EADAS/NM is a coordinated lineup of DEC cabinets, housing all the necessary DEC and Western Electric Company (WECo) equipment. Depending on the number and types of data sources and switching machines being accommodated, the CU consists of a minimum of five cabinets or a maximum of seven cabinets. Of the five basic cabinets, four house the basic DEC CU hardware, including the processor, 128K words of core memory, a dish memory, a 9-track 800 bpi magnetic tape unit, and other assorted equipment always required. One cabinet contains WECo equipment. A sixth cabinet is required for additional DEC hardware when data is being received from more than two EADAS installations. A seventh cabinet is needed to house additional WECo equipment (E2A telemetry, data sets, etc.) as the EADAS/NM approaches its maximum configuration.

6.02 In addition to the cabinet lineup, the CU encompasses a free-standing disk memory, an optional table-top-mounted punched card reader, and a free standing DECwriter.

B. AC Power Distribution

6.03 An EADAS/NM System of maximum size is comprised of eight cabinets (five DEC and three WECo). Each cabinet has its own ac power distribution for the devices contained within the cabinet. The ac input power to each cabinet is 120 Vac/60 Hz and is supplied from an external 30-amp circuit breaker via a power cord which is directly tied to a power controller. The power controller is located in the top or bottom of each cabinet and distributes switched and unswitched ac power to the ac outlets mounted vertically along each side of the rear of the cabinet. When the rear of any cabinet is opened, these outlets will be displayed with the switched ac running vertically along the right side and the unswitched along the left side.

6.04 The power controller may be either locally or remotely controlled as determined by its LOCAL/OFF/REMOTE switch mounted on the controller. The recommended method as provided with the system is for remote control (LOCAL/OFF/REMOTE switch to REMOTE) which is provided by the OFF/ON/PANEL LOCK switch on the PDP 11 processors switch register. OFF-ON control for each cabinet is only provided for the switched ac power outlets (right side) when the LOCAL/OFF/REMOTE switch is set to REMOTE.

6.05 When the OFF/ON/PANEL LOCK switch is set to the ON or PANEL LOCK position, a ground is provided from the processor to the power controllers in each cabinet via a three-conductor cable which originates on the back of the processor drawer and terminates in the WECo miscellaneous (MISC) cabinet. The power controllers sense this ground and energize the power-on relay which applies power to the switched ac outlets and thus the devices within the cabinet. All devices requiring ac power are connected to switched ac power except the RP11-CE moving head disk. Refer to manuals of equipment which are not connected to switched ac power for recommended procedures of shutting down and turning on these devices.

6.06 One lead of the three-conductor cable is dedicated to detect a thermal overload in any of the power controllers. Activation of any thermal overload switch will place a ground on the designated lead which is sensed by the remaining thermal overload detectors causing the power-on relays in all the switched ac power within the CU.

C. Alarms

6.07 The EADAS/NM CU is equipped with an alarm circuit to indicate error conditions or possible error conditions. These error conditions are detected by monitoring various hardware and software functions which are key factors indicating the ability of the CU to execute the EADAS/NM software system. When errors are detected, they are signified by an indicator lamp indicating the type or error (major or minor), the cause of the alarm in some cases, and an audible alarm.

6.08 Major alarms are those alarms which block the basic operation of the CU to a point where the CU is not functioning or where a major section of the critical circuitry is inoperative. The following alarms are classified as major alarms:

- AC Low
- DC Low
- Software failure
- Software designated alarm conditions.

6.09 The alarm circuit also provides for the remote display of alarm conditions (optional). A relay contact closure is provided for each of the following when remote alarms are desired:

- Major alarm
- Major audible alarm
- Exception audible alarm

When the remote alarm feature is used, the MAJOR CUT-OFF and EXCEPTION CUT-OFF switches on the alarm panel must be in their normal positions or the remote alarm feature is disabled. The +24 volt power supply is considered a major alarm condition because it is the source of power for the alarm circuit. A failure of the power supply would not activate any audible or visual alarm unless the remote alarm feature is provided. However, for such failures the +24 volt POWER lamp on the power panel would be extinguished.

6.10 An alarm tree as shown in Fig. 15 shows the structure of the alarm circuit. When multiple alarm setting conditions are present, refer to Fig. 15 to determine which failures have an effect on other parts of the alarm circuit. AC LOW, DC LOW, and Program Timeout Alarms would be activated. Restoring the AC LOW condition to normal would clear the DC LOW condition and program time-out alarms.

D. PDP11/45 Processor

6.11 The EADAS/NM system CU utilizes a DEC PDP 11/45 mini-computer and its peripherals to control and monitor the network. The CU of the system controls the associated peripherals via a high speed, bidirectional, asynchronous bus called UNIBUS. The CU provides the user with a variety of input/output mediums and the necessary interfacing circuits to establish direct communications with EADAS system and the prescribed switching machines in the switching network.

6.12 The PDP 11/45 processor is a 16-bit processor capable of running applications requiring up to 124K words of addressable memory space. The processor is connected to all the system components and peripherals by means of the UNIBUS. The processor connects to the UNIBUS as a subsystem and controls the allocation of the UNIBUS for the peripherals, performs arithmetic and logic operations, and performs instruction decoding.

6.13 A multilevel automatic priority interrupt system permits the processor to respond automatically to conditions outside the system or in the processor itself. The interrupt priorities of the devices on the UNIBUS are independent, allowing adjustment of system behavior in response to real-time conditions. This is done by dynamically changing the priority level of the service routines. Therefore, higher priority devices may seize bus cycles from lower priority devices when polling for the processor status.

6.14 The EADAS/NM system employs a total of 128K words of core memory. Each memory unit operates independently of other units through its own controller which interfaces directly to the UNIBUS. The CU uses MF11-U and MM11-U memory units which contain 16K words of core memory per unit. An external device may use the UNIBUS to read or write core memory completely independent of and simultaneously with the central processor.

6.15 In addition to the 128K words of core memory the EADAS/NM system uses a 20 million word RP03 moving head disk memory as a mass storage device. The RP03 disk is a free-standing disk memory which interfaces with the UNIBUS through a RP11-CE controller. The unit is placed at an interrupt priority level so that the device can make data transfers to and from other units without direct control of the central processor. In the system this facility is used when a CRT in the Network Management Center requests data directly from the data base on the RP03 disk memory.

E. UNIBUS Structure

6.16 Refer to 5.27 through 5.32. Fig. 2 shows a typical EADAS/NM CU UNIBUS structure and Fig. 16 shows the UNIBUS sequence of apparatus.

F. DL11-A Controller and LA36 CA DECwriter II Console

6.17 The DL11-A controller is a character-buffered communications interface that performs two basic operations of receiving and transmitting asynchronous data between the CU and the LA36-CA DECwriter II console (Fig. 12). When receiving data, the interface converts an asynchronous serial character from the LA36-CA DECwriter II console into the parallel character required for transfer to the UNIBUS. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When transmitting data, a parallel character from the bus is converted to a serial line for transmission to the LA36-CA DECwriter II console. Because the two data transfer units (receive and transmitter) are independent, they are capable of simultaneous two-way communication. The receiver and transmitter each operate through two related registers: a control and status register for command and monitoring functions, and a data buffer register for storing data prior to transfer to the bus or the LA36-CA DECwriter II console.

6.18 The LA36-CA DECwriter II console prints from a set of 64 characters at speeds up to 30 characters per second. Data entry is made from either a 97- or 128-character keyboard. It produces an original on a standard 9 7/8 inch wide, tractor-driven, continuous form. The LA36-CA DECwriter II console can receive at either 110, 150, or 300 baud, depending on the switch setting. The standard EADAS/NM data rate is 300 baud.

G. RP11-CE Moving Head Disk and Controller

6.19 The RP11-CE is a complete mass storage system using a magnetic disk pack with 20 data surfaces and a moving read/write head assembly. The RP11-CE includes a control unit and a RP03 moving head disk. This disk system is expandable up to 8 drives, each drive having a capacity of 20,480,000 16-bit words. Access times are 29 msec average lateral (cylinder to cylinder) and 12.5 msec half rotation. Record lengths of one through 65,536 words may be accessed with one read, write, or write check commands.

6.20 The EADAS/NM system requires one controller and one disk drive.

H. BD04 Disk Interrupt Driver and Alarm Circuit

6.21 Refer to 5.43 through 5.47.

I. Core Memory

6.22 A memory can be viewed as a series of locations, with a number (address) assigned to each location. The PDP 11 memories are designed to accommodate both 16-bit words and 8-bit bytes. Therefore, a 4096-word memory can contain 8192 bytes and consist of 017777 octal locations. Words always start at even-numbered locations.

6.23 PDP 11/45 word is divided into a high byte and a low byte. Low bytes are stored at even-numbered memory locations and high bytes at odd-numbered locations.

J. DH11-AA Asynchronous 16-Line Multiplexer

6.24 Refer to 5.48 through 5.51.

K. DB11-A UNIBUS Extender

6.25 Refer to 5.62 and 5.63.

L. DQ11-DA Synchronous Line Interface

6.26 Refer to 5.52 through 5.54.

M. TM11 Magnetic Tape

6.27 The TM11 is a magnetic tape system used for writing, reading, and storing large volumes of data programs in a serial manner. The system writes in a compatible format for downstream processing. The TU10 magnetic tape unit accommodates 10 1/2-inch tape reels that contain up to 2400 feet of tape. Each reel can contain over 180 million bits of data stored on 9 tracks.

6.28 The TM11 employs read after write error checking to verify that proper data is written on the tape. Should a tape dropout be detected, appropriate action can be taken to insure no loss of data.

6.29 Tape motion is controlled by vacuum columns and a servo-controlled single capstan. The nine-track system uses 1/2-inch wide mylar base tape which is coated on one side with an iron oxide composition. The method of recording is non-return-to-zero (NRZ). The nine-track tape includes eight data channels and a lateral parity channel at a density of 800 bits per inch (bpi). The load and end points of the tape are marked by reflective strips which are detected by photo diodes. About 10 inches of blank tape is wound on a reel and precedes the beginning of tape (BOT) strip and follows the end of tape (EOT) strip; a gap of about 3 inches is left from the load point before writing can begin.

6.30 Each computer word contains two 8-bit tape characters. Record blocks are separated by 3/4-inch gaps. In the standard format, the tape contains from 18 to 2,048 characters.

N. CR11 Card Reader (Optional)

6.31 Refer to 5.68.

O. DR11-C Interface

6.32 Refer to 5.55 through 5.61.

P. Data Sets

6.33 Refer to 5.69 through 5.73.

7. PRINCIPLES OF OPERATION

A. Interface to Data Accumulation System

7.01 The EADAS/NM System can be equipped with up to six apparatus Fig. 2s of SD-3B229-01 or SD-3B237-01 to accommodate up to six data accumulator systems. The data accumulator system may be either a basic EADAS or a non-Bell computing system meeting the requirements. Each apparatus Fig. 2 of SD-3B229-01 or SD-3B237-01 consists of one DQ11-DA serial synchronous line interface and a DQ11-KA crystal clock arranged for a 9600 baud rate.

7.02 The DQ11-DA is a double-buffered, single-line synchronous interface. At the UNIBUS interface, data is transfered in parallel over the UNIBUS between the DQ11-DA and core memory using direct memory access in both the send and receive modes.

7.03 Data between DQ11-DA(s) is transmitted serially and synchronously at 9600 baud. The clocking is obtained from the DQ11-KA crystal clock even when data sets are used. The data accumulator system accumulates traffic register counts and transmits them to EADAS/NM at five-minute intervals as accumulated counts for the previous five-minute clock interval.

7.04 Basic EADAS systems report discrete (office status) information from No. 1 crossbar, No. 5 crossbar, and small crossbar tandem offices to EADAS/NM every 20 seconds. Outside supplier systems equivalent to the basic EADAS system may also report discrete data at 6400 bits maximum.

7.05 The EADAS/NM transmits reverse controls to basic EADAS for the control of small crossbar tandem, No. 5 crossbar, and No. 1 crossbar offices. Outside supplier systems cannot institute controls from EADAS/NM.

7.06 The EADAS/NM data accumulator system protocol is nonstandard. The messages always consist of an eight-character header and may be followed by a body message. A body message consists of two synch characters, a start of header character, a variable number of message characters and two block check characters. All characters consist of eight bits.

B. Interface To E2A Telemetry

7.07 The EADAS/NM system can be equipped with up to eight DR11-C general purpose interfaces to accommodate up to eight TCTs. Each TCT can serve up to four E2A remotes. Therefore, a fully equipped EADAS/NM system can interface 32 E2A remotes. At the UNIBUS interface, data is transferred in parallel. The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between the CU and TCT.

7.08 The EADAS/NM polls the E2A remotes to obtain status information on No. 4A/4M toll crossbar and large crossbar tandem offices (those equipped with a traffic supervisory cabinet). The EADAS/NM also sends reverse controls over the E2As to the offices it polls. A group report command (used for polling) consists of only one word. A relay output command consists of three words.

C. Interface to KDPs, ROPs, and Record File Data Port

7.09 A DH11-AA asynchronous serial line multiplexer (MULT1) is always provided along with two DM11-DC line adapaters (LA1, LA2) to interface from two to five KDPs, two ROPs, and possibly a record file data port.

7.10 The record file data port is used to update the data base in the computer. The record file data port generally will consist of a console and a storage device, typically a magnetic tape cartridge, cassette. The console and storage device permits the operator to make data base changes off-line and then batch load the changes into the computer, retaining a magnetic tape record of the changes made. The storage unit that interface to the computer should be identical to the KDP interface. It should operate half duplex at 1200 baud, halt upon removal of secondary carrier, restart when secondary carrier is reapplied, and supply secondary carrier to the computer when in the receive mode.

7.11 The DH11-AA asynchronous serial line multiplexer (MULT1) is supplemented with a modem control (MC) apparatus. Modem control is required to control the EIA interface leads for half duplex operation. Half duplex operation was dictated by the early versions of the model 40 KDPs which were half duplex devices.

7.12 In EADAS/NM the KDPs connecting to the LA1 and LA2 line adapters via data sets are the network management force's primary interface to the system. Display pages can be demanded by the KDP user and displayed on the CRT screen of the KDP. These display pages provide information in the form of five-minute traffic summaries and calculations performed on the traffic data. The KDP user may institute traffic controls via the keyboard portion of the KDP. The printer portion of the KDP can be used to obtain a hard copy of data displayed on the CRT screen.

7.13 Two ROPs are connected to the LA2 line adapter via data sets. One ROP is dedicated to printing exception reports which are common to all EADAS/NM installations. The thresholds of the exception reports are established by the user. The other ROP (monitor) prints three types of messages. The first type of message consists of all ETS channel 2 teletypewriter messages, which includes both those originating from EADAS/NM and those originating from the backup ETS teletypewriter. The second type of message consists of a periodic listing of discretes for an office being monitored. This type of message is intended to be used as a tool for monitoring the effect of controls which have been instituted. The third type of message is highly flexible set of exception messages. These messages are limited in number (maximum 64), but are more easily varied than the exceptions available from the exception printer.

D. Interface to ETS-PBC Links

7.14 The two DH11-AA asynchronous serial line multiplexers for MULT2 and MULT3 operate like the DH11-AA asynchronous serial line multiplexer for MULT1 except that they lack modem control. Up to 16 ETS-PBC offices can be accommodated by EADAS/NM. The first eight ETS-PBC offices are accommodated by MULT2 and the last eight ETS-PBC offices are accommodated by MULT3. MULT3 is provided on an optional basis depending on the number of ETS-PBC offices to be accommodated.

7.15 Each DH11-AA asynchronous serial line multiplexer is equipped with a DH11 distribution panel mounted near the top of the cabinet containing MULT2 and MULT3. The distribution panels may each be equipped with up to four line adapters. Each line adapter has four channels which accommodate two ETS-PBC offices. The first line adapter (LB1) for MULT2 is equipped as follows:

(a) Channel 0 connects to the first ETS

(b) Channel 1 connects to the PBC corresponding to the first ETS

(c) Channel 2 connects to the second ETS

(d) Channel 3 connects to the PBC corresponding to the second ETS.

7.16 Connections from the line adapters are made through 108D data sets in the EADAS/NM data terminals circuit to the 110 baud links to the ETS channel 2 teletypewriter ports. A backup teletypewriter terminal located in either the ETS office or remote may also be connected as a second channel 2 teletypewriter port. If an attempt is made to simulaneously use the ETS link from both sources, character interleaving from the two sources is possible, through character mutilation will not

occur. A message entered into the ETS from one source is echoed on the alternate port. In EADAS/NM the echoed message will appear as a printout on the monitor ROP as previously described. The ETS link is used to enter reverse controls into the ETS computer.

7.17 Connections from the line adapters are made through 202T data sets in the EADAS/NM data terminals circuit to the 1800 baud links to PBCs. The PBCs transmit five-minute register data to EADAS/NM.

8. MAINTENANCE

8.01 Through careful planning and design of the CU, the maintenance problems associated with equipment having more than one manufacturer have been avoided. This has been accomplished by having DEC manufacture and supply all equipment closely coupled with the computer operations and WECo manufacture and supply the remaining equipment such as data sets and associated equipment.

8.02 The maintenance of the WECo equipment consists almost entirely of replacing faulty circuit packs. This equipment houses relatively simple circuitry that is repeated many times and, therefore, should not be too difficult to maintain.

8.03 The DEC portion of the CU involves sophisticated, high speed electronic circuitry, and mechanical equipment requiring preventive and corrective maintenance.

8.04 The TELCO craftperson is expected to maintain the equipment produced by WECo and also perform trouble sectionalizing tests to isolate troubles to the DEC equipment.

8.05 The electronics in the CU equipment have a high reliability compared to the mechanical subsystems. In light of this, the possibility of supplying additional or standby disk and tape drives shall be considered for periods of preventive and corrective maintenance.

9. REFERENCES

9.01 The following is a list of sections containing information on the Engineering and Administrative Data Acquisition System/Network Management.

SECTION	TITLE
252-116-301	Central Unit Maintenance Operation Procedures EADAS/NM
252-116-302	Central Unit Trouble Sectionalizing EADAS/NM
252-116-303	Wall Display Board Assignment Guidelines EADAS/NM
252-116-501	Wall Display Board Tests EADAS/NM
252-116-502	Tests of 4A ETS and EADAS Interfaces EADAS/NM

TABLE A

EADAS/NM CENTRAL UNIT POWER DISTRIBUTION

EQUIPMENT	CABINET OR PERIPHERAL	THERMAL CIRCUIT BREAKER REQUIRED	RECEPTACLE REQUIRED (NEMA) [SEE TABLE B]	VOLTS PER PHASE TO NEUTRAL	PHASE(S) CONNECTED TO RECEPTACLE	AMPS PER PHASE PF UNCORR	POWER DISS. (WATTS)	POWER SOURCE
CENTRAL UNIT EQUIPMENT	RP04	20A	L21-20R	115	A, B, C	6	2100	Refer to CD-3B237-01
	CAB 1	30A	L5-30R	115	A	8	900	
	CAB 2	30A	L21-30R	115	A, C (See Note 1)	12	2600	
	CAB 3	30A	L21-30R	115	A, B (See Note 1)	15	3450	
	CAB 4	30A	L5-30R	115	B	8	850	
	CAB 5	30A	L5-30R	115	C	5	550	
	DECwriter CONSOLE	15A	5-15R	115	C	3	300	
	CARD READER	15A	5-15R	115	B	6	600	
DATA TERMINALS EQUIPMENT	CAB B	30A	L5-30R	115	B	6	600	
	CAB C (1ST)	30A	L5-30R	115	C	6	600	
	CAB C (2ND)	30A	L5-30R	115	C	6	600	
NETWORK MANAGE-MENT CENTER EQUIPMENT	KDP (1ST)	15A	5-15R	115	C	3	360	
	KDP (2ND)	15A	5-15R	115	C	3	360	
	ROP (1ST)	15A	5-15R	115	C	3	260	
	ROP (2ND)	15A	5-15R	115	A	2	260	
	WALL DISPLAY BOARD	15A	5-15R	115	B	1	115	
	KDP (3RD)	15A	5-15R	115	A (See Note 2)	3	360	
	KDP (4TH)	15A	5-15R	115	B (See Note 2)	3	360	
	KDP (5TH)	15A	5-15R	115	C (See Note 2)	3	360	

Note 1: It is recommended that all 3 phases be supplied to these two cabinets to allow for future growth and to supply cabinet outlets useful for powering test equipment.

Note 2: These items must not be connected to an inverter having only a 15KW rating. Refer to CD-3B237-01.

TABLE B

RECEPTACLE CROSS REFERENCE GUIDE

NEMA CODE	HUBBLE CODE*
L21-20R	2510
L5-30R	2610
L21-30R	2810

* HARVEY HUBBLE ®

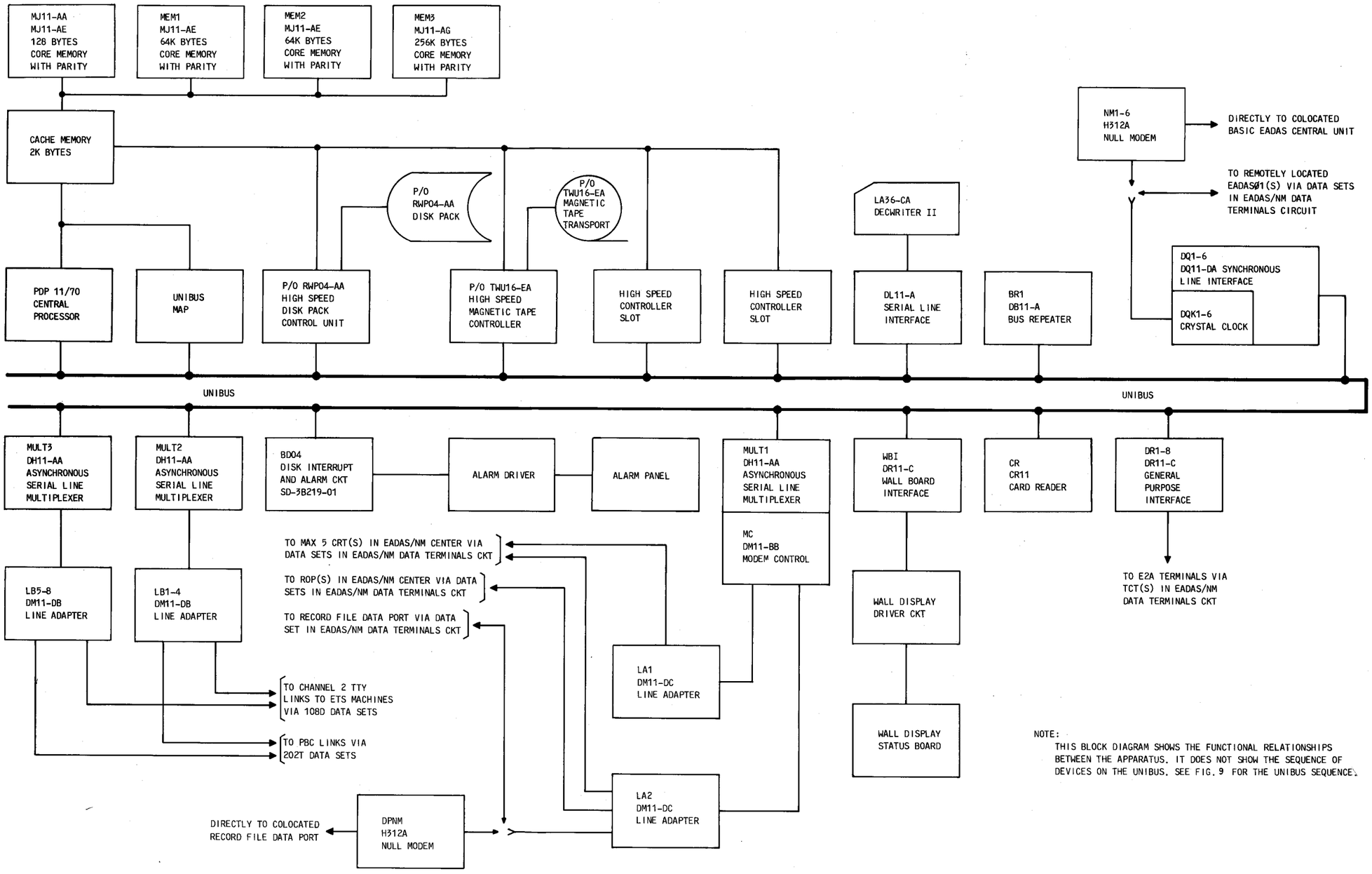
TABLE C

EADAS/NM ALARM CONDITIONS AND EXPECTED RESPONSES

ALARM CONDITION	SOFTWARE ADDRESS (IF ANY)	RESPONSE	
		AUDIBLE	VISIBLE (LAMPS)
SOFTWARE MAJOR	764410	YES	MJ
EXCEPTION ALARM	764412	YES*	EXCEPT*
PROGRAM RESET	764414	RESET	ALL RESET
PROGRAM TIMER	764416	YES**	MJ**
AC LOW		YES	AC LOW MJ
DC LOW		YES	DC LOW MJ
+24 V FAIL		NO	+24 OUT
AUDIBLE RESET SWITCH		OFF	AUDIBLE DISABLE

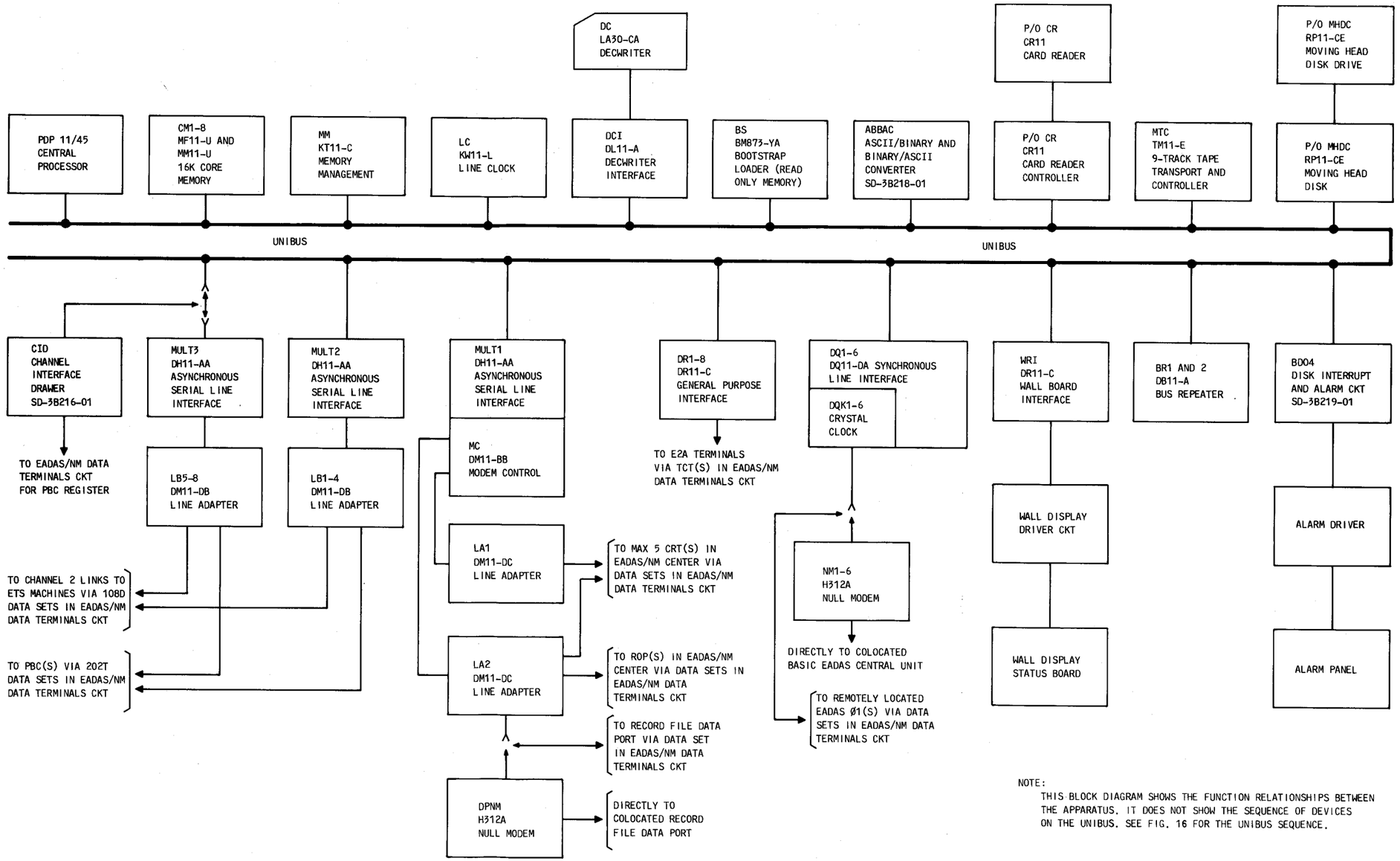
* 1 sec duration under software control.

** Alarm occurs if address is not read (or accessed somehow) for 2.0 sec. (nominal).



NOTE:
THIS BLOCK DIAGRAM SHOWS THE FUNCTIONAL RELATIONSHIPS BETWEEN THE APPARATUS. IT DOES NOT SHOW THE SEQUENCE OF DEVICES ON THE UNIBUS. SEE FIG. 9 FOR THE UNIBUS SEQUENCE.

Fig. 1—Block Diagram of EADAS/NM with PDP 11/70



NOTE:
THIS BLOCK DIAGRAM SHOWS THE FUNCTION RELATIONSHIPS BETWEEN THE APPARATUS. IT DOES NOT SHOW THE SEQUENCE OF DEVICES ON THE UNIBUS. SEE FIG. 16 FOR THE UNIBUS SEQUENCE.

Fig. 2—Block Diagram of EADAS/NM with PDP 11/45

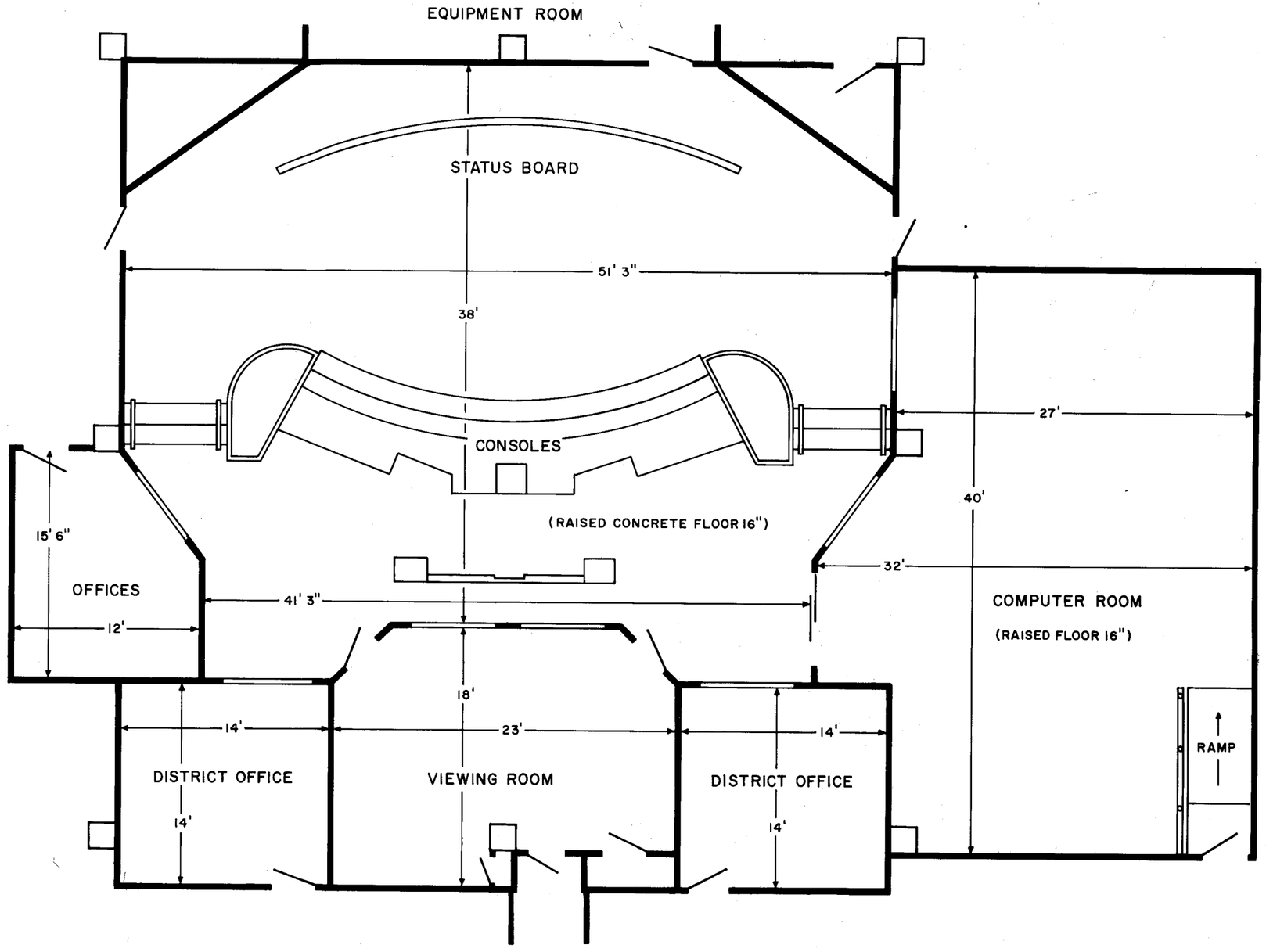


Fig. 3—Typical Example of EADAS/NM Center Layout

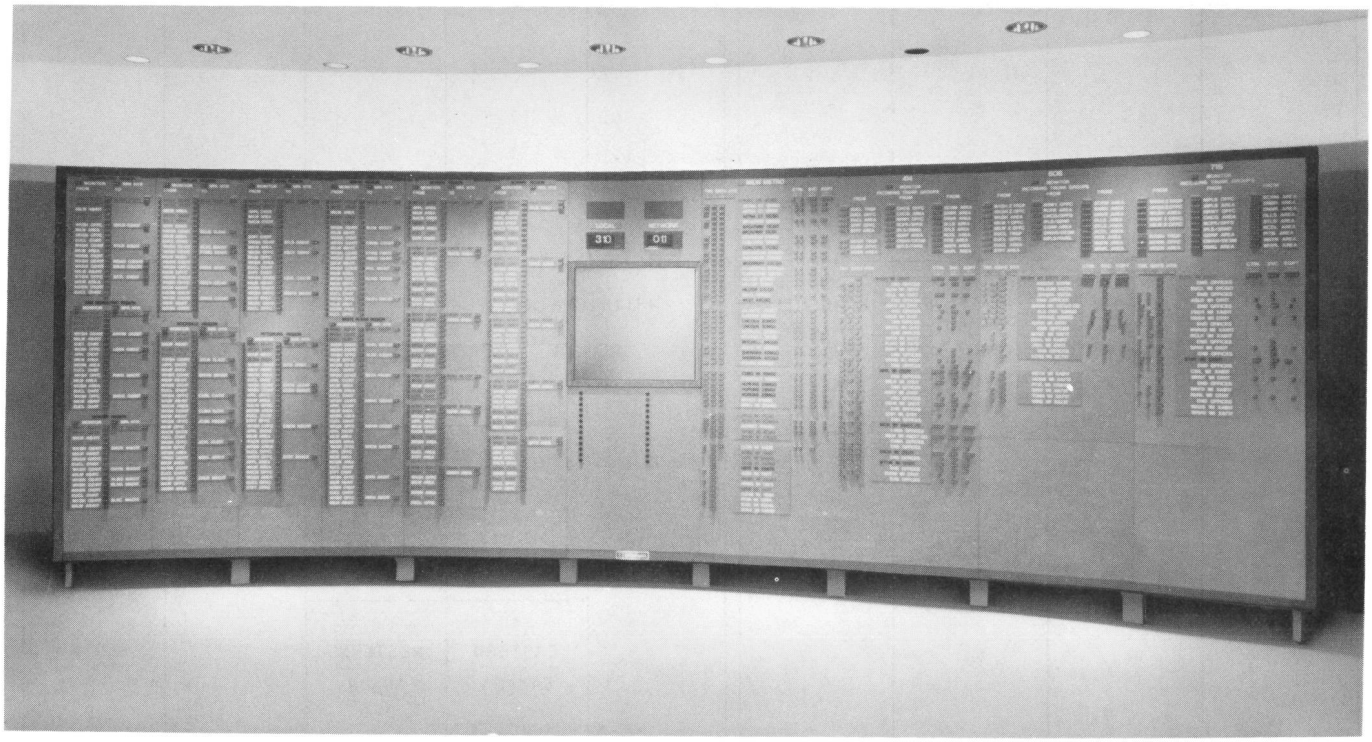


Fig. 4—Typical Example of Wall Display Board

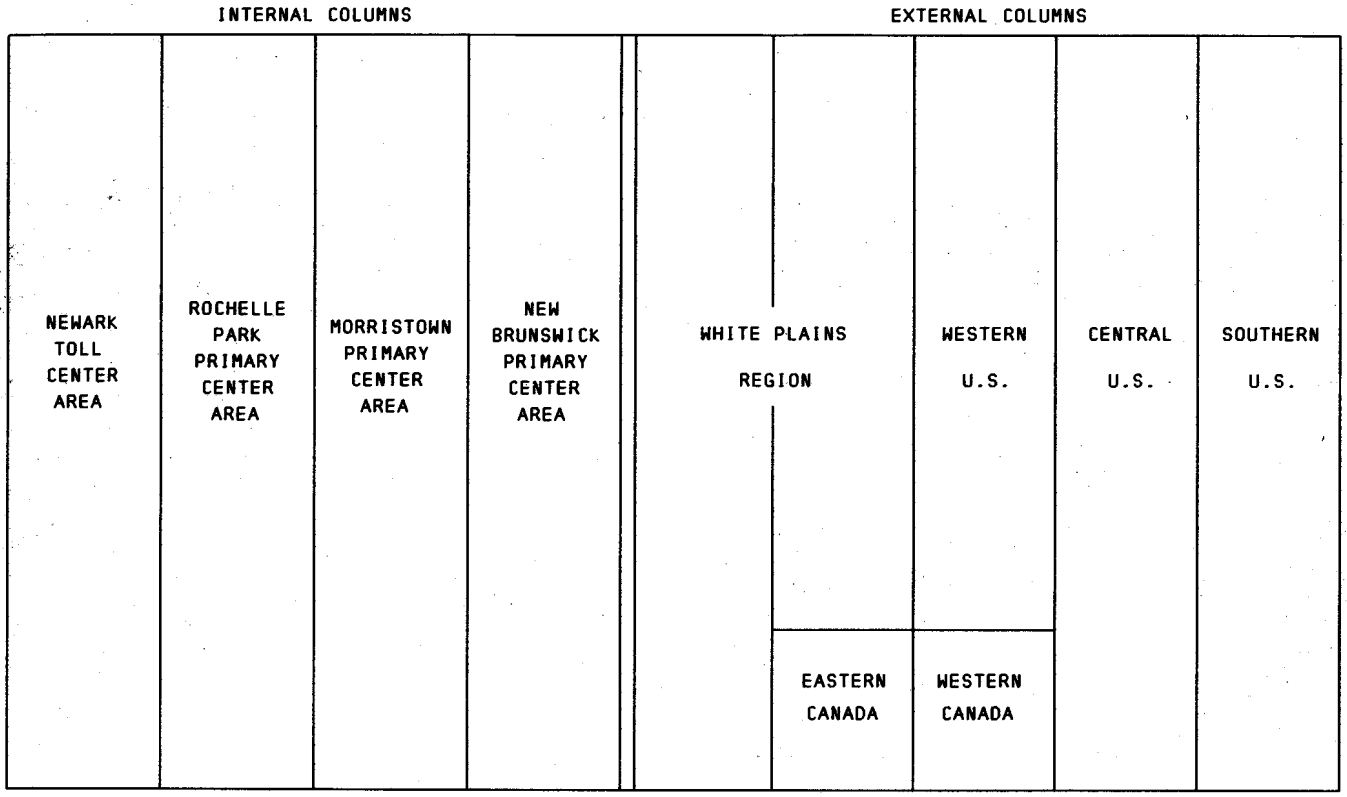


Fig. 5—Possible Wall Display Configuration for 201 NPA

Fig. 6—DATASPEED 40 KDP Operator Console

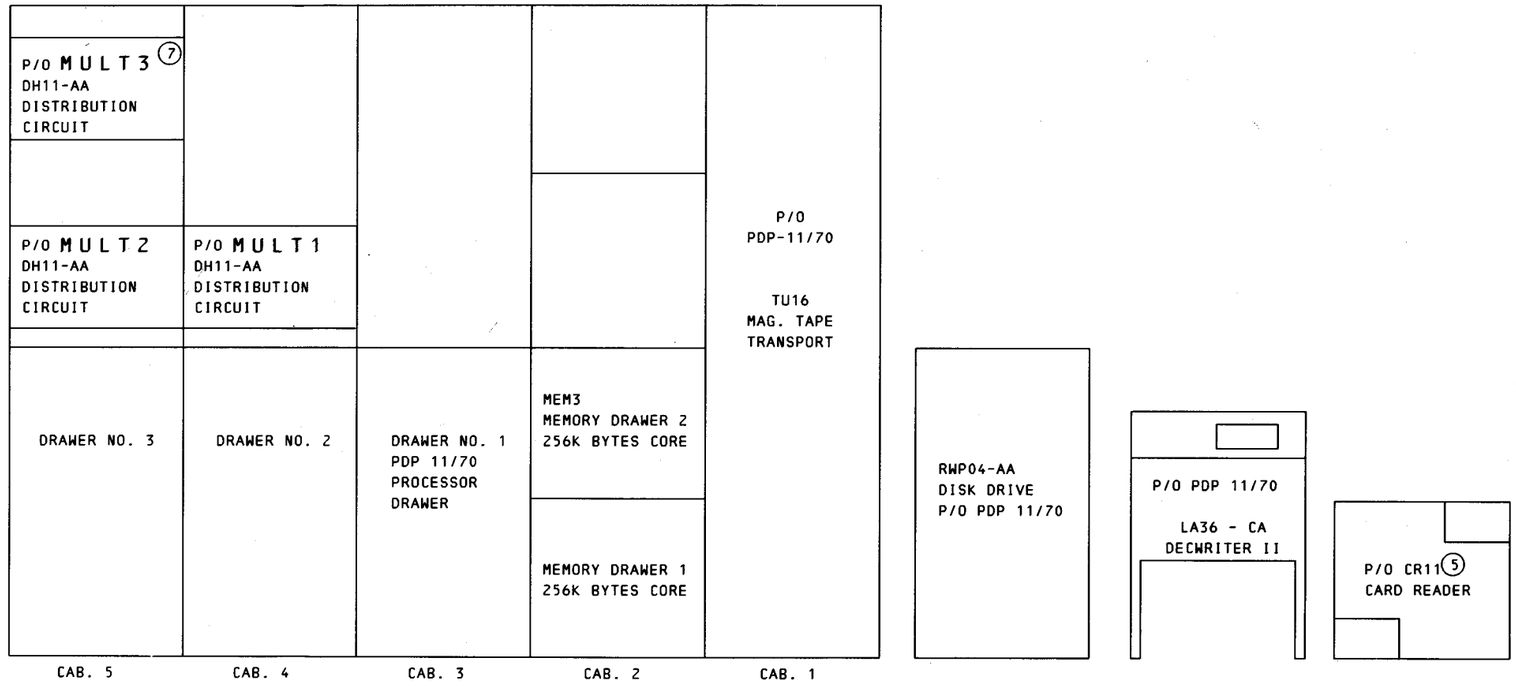


Fig. 7—Typical Equipment Layout for EADAS/NM Central Unit with PDP 11/70

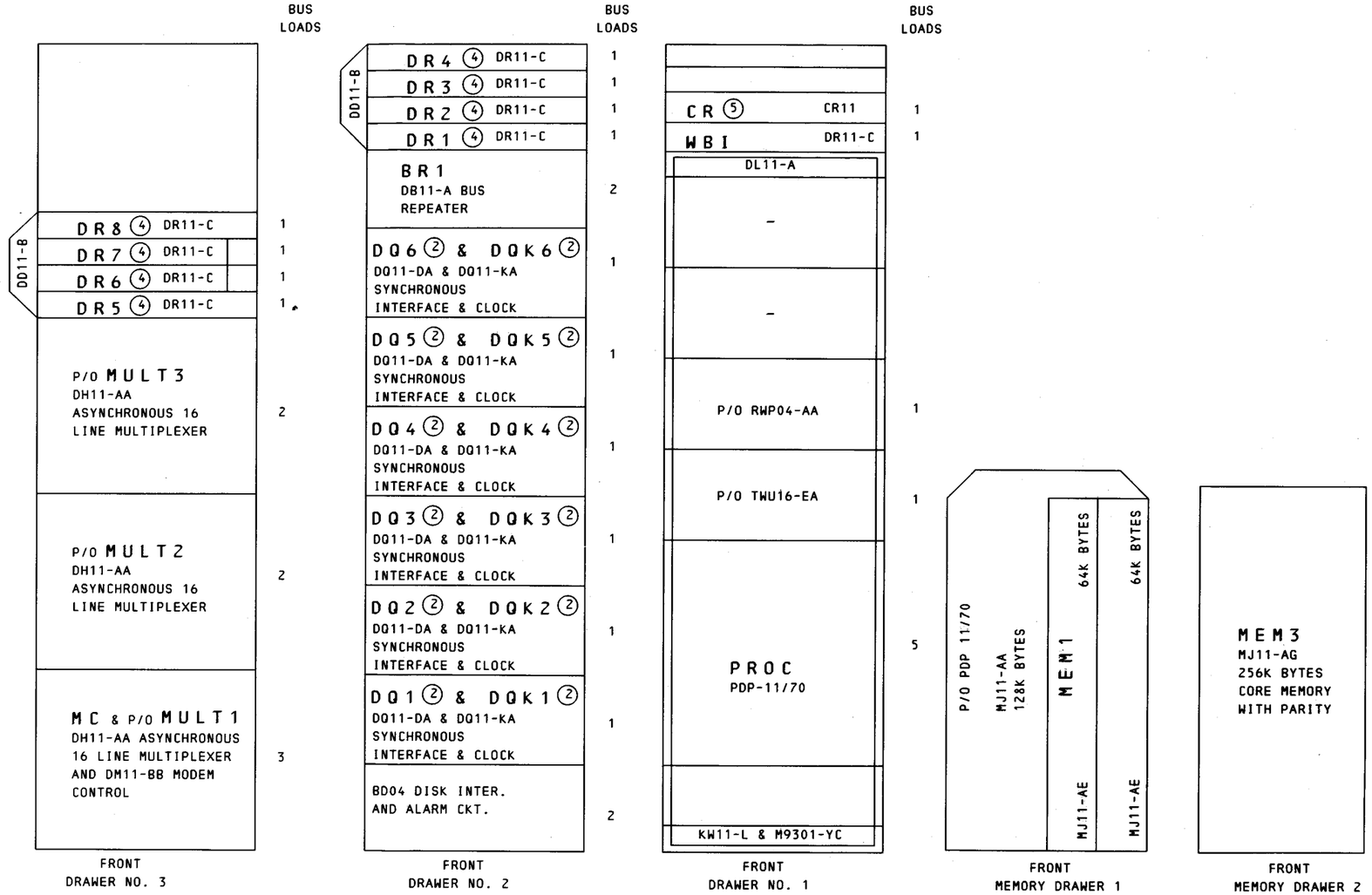
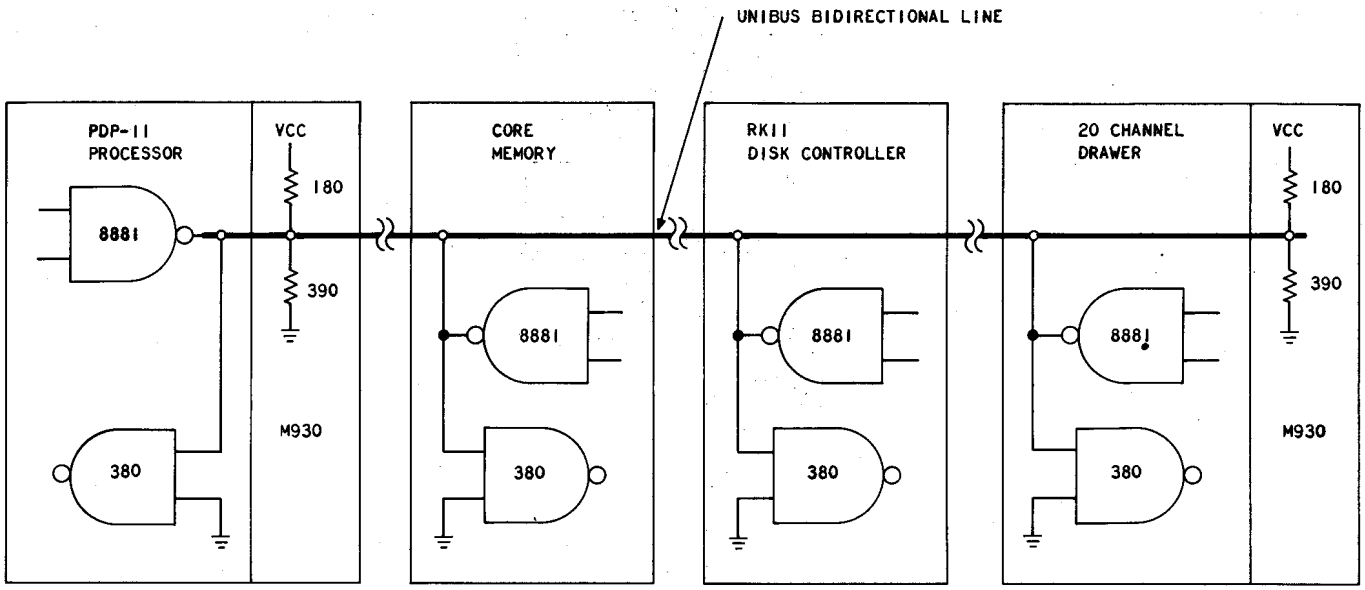


Fig. 8—Drawer Configuration for EADAS/NM Central Unit with PDP 11/70

	CPU
	TWU16-EA
	RWP04-AA
	DL11-A
	DR11-C
(5)	CR11
	BD04
(2)	DQ11-DA
(2)	DQ11-DA
(2)	DQ11-DA
(2)	DQ11-DA
(2)	DQ11-DA
(2)	DQ11-DA
	DB11-A
(4)	DR11-C
(4)	DR11-C
(4)	DR11-C
(4)	DR11-C
	DH11-AA & DM11-BB
	DH11-AA
(7)	DH11-AA
(4)	DR11-C
(4)	DR11-C
(4)	DR11-C
(4)	DR11-C

Fig. 9—UNIBUS Sequence of Apparatus for PDP 11/70



NOTES:
1. DATA LINE 1 (DO1) IS SHOWN ON THE ABOVE EXAMPLE OF A UNIBUS BIDIRECTIONAL LINE.
2. DATO EXAMPLE: PROCESSOR 8881 AND 20 CHANNEL DRAWER 380 ARE ENABLED.
3. DATI EXAMPLE: CORE MEMORY 8881 AND PROCESSOR ARE ENABLED.
4. CONTROL OF WHICH 380IC AND 881IC IS ENABLED IS DETERMINED BY THE UNIBUS MASTER AND WHICH ADDRESS AND CONTROL LINES ARE ASSERTED.

Fig. 10—UNIBUS Bidirectional Line

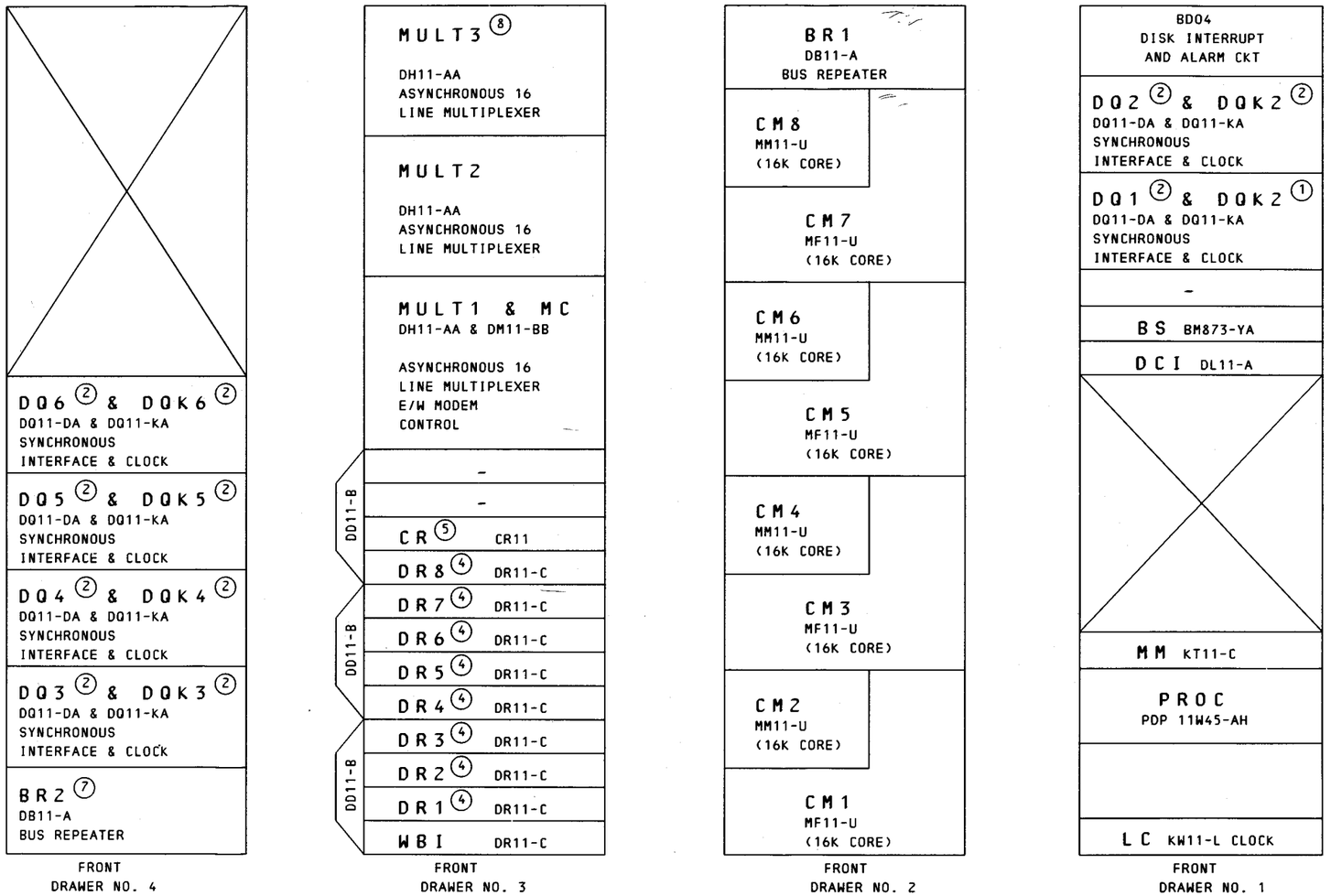
Fig. 11—RP04 Moving Head Disk

Fig. 12—LA36 DECwriter II

<table>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>DRAWER
NO. 3</td><td>DRAWER
NO. 4
(OPTIONAL*)</td><td rowspan="2">RP11-CE
DISK
CONTROLLER</td><td>TU10
MAGNETIC
TAPE
TRANSPORT</td><td></td></tr>
<tr><td>MULT3 ⑧ MUX
DH11-AA DISTRIBUTION
CIRCUIT</td><td rowspan="3">DRAWER
NO. 2</td><td rowspan="3">TM11
MAGNETIC
TAPE
CONTROLLER</td><td rowspan="3">DRAWER
NO. 1</td></tr>
<tr><td>MULT2 MUX
DH11-AA DISTRIBUTION
CIRCUIT</td><td></td></tr>
<tr><td>MULT1 MUX
DH11-AA DISTRIBUTION
CIRCUIT</td><td></td></tr>
<tr><td>CAB. 5</td><td>CAB. 4</td><td>CAB. 3</td><td>CAB. 2</td><td>CAB. 1</td></tr>
</table>

* DRAWER NO. 4 PROVIDED WITH THIRD DQ11-DA WITH DQ11-KA SYNCHRONOUS LINE INTERFACE WITH CRYSTAL CLOCK

Fig. 13—Typical Equipment Layout for EADAS/NM Central Unit with PDP 11/45



* DRAWER NO. 4 PROVIDED WITH THIRD DQ11-DA WITH DQ11-KA SYNCHRONOUS LINE INTERFACE WITH CRYSTAL CLOCK

Fig. 14—Drawer Configuration for EADAS/NM Central Unit with PDP 11/45

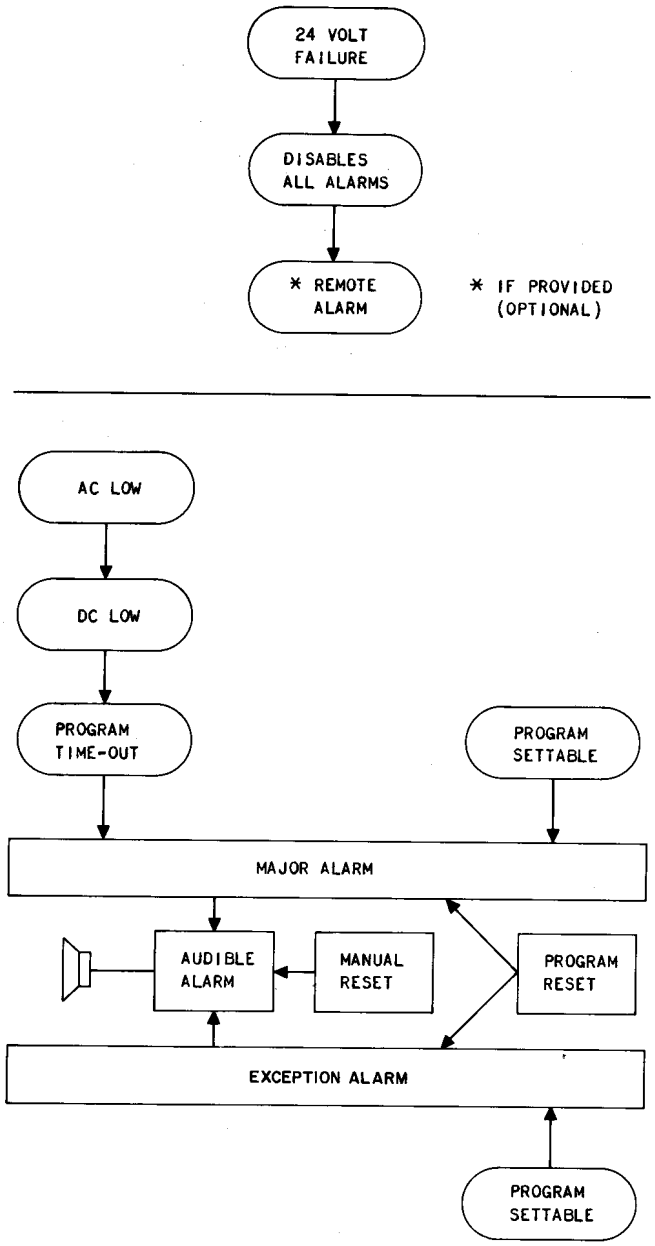


Fig. 15—Alarm Tree for Alarm Circuit

	BUS LOADS
CPU (E/W KW11-L & KT11-C)	1
DL11-A	1
BM873-YA	1
DQ11 #1 (2)	1
DQ11 #2 (2)	1
BD04	2
TM11-EA	1
RP11-CE	1
MF11-U	1
MM11-U	1
MF11-U	1
MM11-U	1
MF11-U	1
MM11-U	1
MF11-U	1
MM11-U	1
DB11-A #1	2
DR11-C #1	1
DR11-C #2 (4)	1
DR11-C #3 (4)	1
DR11-C #4 (4)	1
DR11-C #5 (4)	1
DR11-C #6 (4)	1
DR11-C #7 (4)	1
DR11-C #8 (4)	1
DR11-C #9 (4)	1
CR11 (5)	1
DH11-AA #1 E/W DM11-BB	2
DH11-AA #2	2
DH11-AA #3	2
DB11-A #2 (7)	2
DQ11 #3 (2)	1
DQ11 #4 (2)	1
DQ11 #5 (2)	1
DQ11 #6 (2)	1

Fig. 16—UNIBUS Sequence of Apparatus for PDP 11/45