CENTRAL UNIT—TROUBLE SECTIONALIZING ENGINEERING AND ADMINISTRATIVE DATA ACQUISITION SYSTEM/NETWORK MANAGEMENT (EADAS/NM)

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1. GENERAL

1.01 This section provides procedures for isolating trouble conditions associated with the EADAS/NM central unit (CU) hardware.

1.02 This issue affects the Equipment Test List.

1.03 The following Digital Equipment Corporation (DEC) documents may be referred to for

more detailed information pertaining to DEC hardware and theory of operation:

(a) Processor Handbook—PDP-11

(b) Peripherals and Interfacing Handbook—PDP-11

(c) UNIBUS Interfacing Manual—PDP-11

A. UNIBUS Structure

1.04 The UNIBUS is a common, high-speed data path that interconnects the processor and all devices within the CU. It is a 120 conductor flexprint cable (white in color) that is found weaving through the devices comprising the CU. The UNIBUS uses 56 lines for information with all of the remaining lines grounded to provide noise immunity. Fifty-one of the signal leads are bidirectional which includes for example: the address lines (18), data lines (16), control lines (2), and the lines dedicated to monitoring the power supplies. The remaining 5 lines are unidirectional which encompass the bus grant (BG) lines (4), and the non-processor grant (NPG) line.

1.05 All UNIBUS bidirectional lines use negative logic, and all unidirectional lines are positive logic. All other system device logic is positive.

1.06 All devices attach to the UNIBUS by paralleling off the desired signal and control lines as the lines are passed serially through the device enroute to the UNIBUS terminator (located on the end of the UNIBUS section). The only information which is not attained in this manner comes over the BG lines which are serially passed through the devices requiring these signals as they are physically arranged on the UNIBUS in distance from the processor. The block diagram in Fig. 1 shows a typical EADAS/NM CU UNIBUS structure with a PDP 11/70 computing system.

1.07 The allowable length of the UNIBUS and the number of devices which are attached to it are limited by a PDP-11 system requirement of 50 feet and 20 unit loads. A UNIBUS load is defined as one UNIBUS receiver (M784) and two UNIBUS drivers (M783) which is the approximate equivalent of one device (ie, RP04 disk controller). If additional length or loading is required as it is for EADAS/NM, a DB11-A UNIBUS extender may be added which allows an additional 50 feet and an additional 20 unit loads to be added to the UNIBUS structure. However, the DB11-A UNIBUS extender uses two unit loads, one on each section of the UNIBUS which limits each section to 18 unit loads. The UNIBUS characteristics for EADAS/NM are shown in Fig. 2 for the EADAS/NM system configuration with a PDP 11/70 computing system.

1.08 The UNIBUS can be thought of as a data link between devices. Each device is entirely self sustaining and independent of other devices within the CU. Therefore, a device can be eliminated entirely from the UNIBUS structure without affecting the operation of other devices (providing the system software doesn't address the device). When system diagnostics programs are being run, removing devices from the UNIBUS structure is a controlled parameter. The isolating ability of the devices on the UNIBUS allows maintenance personnel to sectionalize troubles.

1.09 Fig. 3 shows a UNIBUS bidirectional line. All devices attach to the UNIBUS bidirectional line with either a UNIBUS receiver IC (380) or a UNIBUS driver IC (8881). On a data out (DATO) transfer, the driver of one device (ie, PDP-11 processor) and the receiver of another device are enabled. This allows the data in the processor to be passed to the DR11-C or wherever the address lines instruct it to go. The address lines basically control which device is enabled, while the control lines tell whether the 380 UNIBUS receiver or the 8881 driver is enabled, indicating the direction of the data transfer.

1.10 To insure that the data path between devices is established and to facilitate the asynchronous method of data transfers, various control signals are used. These signals are master sync (MSYN) and slave sync (SSYN) which provide a hand-shaking between the two communicating devices. The master device (ie, processor) sends out MSYN and if the slave does not return SSYN within a few microseconds, the processor traps to location 4 which indicates the data path was not established.

1.11 The function of the UNIBUS and the various devices comprising the CU, although briefly described in this section, are described in greater detail in the DEC documents provided with the system. The operation of each device is explained in the manuals pertaining to it. The reading of the manuals supplied with EADAS will allow

maintenance personnel to become more proficient in diagnosing troubles.

B. Interrupts

1.12 Various devices other than the processor are capable of becoming bus master on a level of priority higher than the processor. These devices are classified as nonprocessor request devices (NPR). Once an NPR device becomes bus master, it may execute nonprocessor data transfers directly from the device on the NPR level (ie, a disk) to another address location (ie, core memory). These direct data transfers are done entirely without processor control and are termed NPR transfers. The following devices in the CU operate on an NPR level:

- RP04 disk controller
- TU16 9-track magtape
- DH11 multiplexer

1.13 Another form of interrupt is the bus-request (BR) structure which allows a device to interrupt a program being executed by the processor and force it into a routine to service the device making the interrupt. The processor checks for these requests between instructions and if the processor level (controlled by bits 5, 6, 7 in processor status register) is less than the level of the device requesting the interrupt, it services that device. If the processor level is equal to or greater than the device requesting service, the device must wait until the processor level is changed to such a level where it may accommodate the device. The EADAS/NM CU is comprised of numerous devices which operate on the BR level. An example of this type of device is the KW11-L line clock which operates on BR-6 level.

C. Address Structure

1.14 The address for all UNIBUS devices are shown in SD-3B229-01 and SD-3B237-01.

D. Equipment Layout

1.15 A typical equipment layout for EADAS/NM CU with a PDP 11/70 is shown in Fig. 4. This figure includes the cabinets and the system drawer configurations. This allows any device contained within the CU to be located easily. The method of naming and assigning circuit boards to various locations and the methods used for labeling and determining the pin assignments within a system drawer are shown in Fig. 5.

E. Alarms

1.16 The EADAS/NM CU is equipped with an alarm circuit to indicate error conditions or possible error conditions. These error conditions are detected by monitoring various hardware and software functions which are key factors indicating the ability of the CU to execute the EADAS/NM software system. Detected errors are signified by an indicator lamp indicating the type of error, in some cases the cause of the error, and an audible alarm.

1.17 Major alarms are those which impede the basic operation of the CU to a point where the CU is not functioning or where a major section of critical circuitry is inoperative. The following alarms are classified as major alarms:

- AC low
- DC low
- Program loop failure
- Software designated alarm conditions

1.18 The alarm circuit also makes provisions for the remote display of alarm conditions (optional). The alarm circuit provides a relay closure for each of the following alarm conditions:

- Major alarm
- Major audible alarm
- Exception alarm
- Exception audible alarm

Note 1: The major cutoff and exception cutoff switches must be in the NORMAL position, otherwise all the remote alarms are disabled.

Note 2: The +24 volt T&R power supply is considered a major alarm because it is the source of power for the alarm circuit. A failure of the power supply is not signified

without the remote alarm option. However, the +24 volt power on lamp will not be illuminated.

1.19 An alarm tree shown in Fig. 6 can be used to determine the cause of an alarm when multiple alarm conditions are indicated. This only happens when a failure occurs in the AC LOW/DC LOW/program timeout branch. Reference to the alarm tree diagram will clarify the alarm structure.

F. AC Power Distribution

1.20 An EADAS/NM system of maximum size is comprised of eight cabinets (5 DEC, 3 WECo). Each cabinet has its own ac power distribution for the devices contained within the cabinet. Four of the five DEC cabinets are supplied with 120 Vac/60 Hz power from an extended 30-ampere circuit via a power cord directly to a power controller. The power controller is located in each cabinet and distributes switched and unswitched power to the ac outlets within the cabinet. The 3 WECo cabinets receive power in much the same way except that the ac power is distributed through circuit breakers.

1.21 The power controller may be controlled either locally or remotely as determined by the LOCAL/OFF/REMOTE switch mounted on the controller. The recommended method is for remote control from the OFF/ON/PANEL LOCK switch on the PDP-11 processor switch register. When the LOCAL/OFF/REMOTE switch is set to REMOTE, the OFF/ON control for each cabinet controls only the switched ac power outlets. When the OFF/ON/PANEL LOCK switch is in the ON or PANEL LOCK position, a ground is provided from the processor to the power controllers in each cabinet via a three-conductor cable which originates on the back of the processor drawer and terminates in the final DEC cabinet. The ground energizes the relay in the power controllers which applies ac power to the switched ac outlets and thus the devices within the cabinet. All devices requiring ac power are connected to switched ac power except the TU10 magtape transport, the RP04 moving head disk, and the three WECo data set and TCT cabinets.

Caution: The OFF/ON/PANEL LOCK switch does not completely remove power from the CU. To remove all power from the CU the circuit breaker on the power supply for the processor must be disabled. As an indication of complete lack of power, the fans in the processor stop operating.

1.22 The three-conductor cable also has one lead dedicated to detect a thermal overload in any of the power controllers. Activation of any thermal overload switch will place a ground on the designated lead which is detected by the remaining thermal overload detectors and disables the power on relays in all the cabinets and shuts down all the switched ac power within the CU.

1.23 ***Lettered Steps:*** A letter a, b, c, etc, added to a step number in this section indicates a procedure which may or may not be required depending on local conditions. The condition under which a lettered step, or a series of lettered steps, should be made is given in the SYMPTOM/CONDITION or PROCEDURE column, and all steps governed by the same condition are designated by the same letter within a procedure. Where a condition does not apply, all steps designated by that letter should be omitted.

2. APPARATUS

2.01 Tektronix 453 oscilloscope (or equivalent) equipped with two P6010 voltage probes.

2.02 KS-14510 portable volt-ohm-milliammeter (VOM), or equivalent, equipped with test leads.

2.03 Test connector.
DEC H315A modem test connector.

3. POWER FAILURE—TROUBLE SECTIONALIZING

A. Initial AC Power Check

3.01 The following procedure allows maintenance personnel to isolate and determine the cause of troubles associated with ac power failures. AC power failures are usually recognized by one or more of the following symptoms.

- AC LOW lamp on alarm panel lighted.
- PDP-11 switch register lamps not pulsating.

- Device lamps fail to illuminate—channel active, disk display, tape transport, etc.
- Program fails to execute.
- Cabinet fans are not operating.
- Any other ac power failure symptoms.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
1	AC power is missing from power supply cabinets.	Check that all AC (amber) lamps on power controller are lighted.
2	AC (amber) lamp on power controller is not lighted.	Check the source of ac power (30 amp circuit breakers).
3		Reset circuit breakers on power controllers to ON position.
4	Circuit breaker trips after resetting. ***Probable Cause:*** One or more of the devices associated with the power controller is causing an overload condition.	Remove all ac plugs from outlets, reset circuit breaker, and systematically replace ac plugs until the device that trips the circuit breaker is found.
5	Circuit breaker trips with no devices plugged into it. ***Probable Cause:*** Trouble in power controller or there is a short circuit on the ac power distribution outlets.	Refer to DEC engineering drawings and troubleshoot.
6		Verify source of ac power and check that external circuit breaker is not tripped.
7	AC (amber) lamp still is not lighted or power is missing from cabinets.	Verify that all H720E power supplies of the system have their LOCAL/REMOTE switch set to LOCAL (except the processors supply should be set to REMOTE).
8		Verify that all power controllers have their LOCAL/OFF/REMOTE switch set to REMOTE.
9		Verify that all devices that require ac power are connected to the switched ac outlets (right side) with the exception of RP04 disk and the TU16 tape transport.
10		Verify that the 3-conductor cable is connected from the processor drawer to all 860A power controllers and that it terminates in the EADAS miscellaneous circuits cabinet.
11		Verify that ground is being provided from the OFF/ON/ PANEL LOCK switch to all power controllers when the switch is in either the ON or PANEL LOCK position.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
12		Using a VOM, check for ground at pin 2 of J1 on the processor drawer.
13	Ground is not present. ***Probable Cause:*** 1. P3 is not secured to J2 on the processors drawer H720E power supply. 2. Processor drawer has a thermal overload. 3. OFF/ON/PANEL LOCK switch is defective. 4. Defective wiring between P3 and J1.	Refer to DEC engineering drawings and troubleshoot.
14	Simulate the ground from the OFF/ON PANEL LOCK switch.	Set the REMOTE/LOCAL switch on the processors H720E power supply to LOCAL position.
15	System is operational with exception of processor drawer. ***Probable Cause:*** Same as for Step 13.	Same as for Step 13.
16	One of the other cabinets is not operational. ***Probable Cause:*** Defective power controller detection circuit.	Set the LOCAL/OFF/REMOTE switch on the power controller to LOCAL and check for power at cabinet. Refer to DEC engineering drawings.
17	Thermal overload condition exists—switched ac is missing. ***Probable Cause:*** Too much heat.	At the processor H742 power supply, remove the P2 connector from the J1 socket and measure the voltage at lead 2 and ground. If the VOM indicates 0 volts, a thermal overload condition exists.
18	One of the cabinets is causing the thermal overload condition.	Place the OFF/ON/PANEL LOCK switch in the OFF position.
19	Thermal overload condition exists.	Systematically isolate the cabinet causing the overload condition by removing the 3-conductor cables connected to each power controller and setting the LOCAL/OFF/REMOTE switch to the LOCAL position.
20	Cabinet fans and devices in cabinet receive ac power.	If cabinet receives ac power with LOCAL/OFF/REMOTE switch set to LOCAL, the thermal overload condition is not caused by this cabinet. Repeat Step 18 until a cabinet is found that will not become activated when the LOCAL/OFF/REMOTE switch is in the LOCAL position.
21	Cabinet fans and devices in cabinet are not activated with the power controllers switch set to the LOCAL position.	Refer to DEC engineering drawings for troubleshooting.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
	Probable Cause: Thermal overload or false ground on lead 2 of the 3-conductor cable.	

B. DC LOW

3.02 The EADAS/NM CU has one UNIBUS line which is designated DC LOW. This lead is present on all UNIBUS connectors on pin BF1 (purple lead). The DC LOW signal is asserted (0-volt) when a power supply within the CU has allowed its output voltages to drop below operational level or has completely failed. The DC LOW line monitors basically the +5V and -15V output of all the H720E power supplies. If DC LOW is asserted without the occurrence of an AC LOW, the processor will detect this and initialize all devices and registers. This halts the processor from executing instructions which cause a program time-out alarm. A DC LOW alarm indication will be given for a DC LOW condition.

3.03 If an AC LOW condition occurs before a DC LOW, the processor will enter a power failure routine. Refer to DEC documentation for a power failure sequence. If noise spikes are present on the DC LOW lead, it will cause the processor to send initialize (INIT) instructions to devices and halt the execution of the software. Therefore, the existence of noise on the DC LOW line is of the same significance as a DC LOW condition. A blown fuse in any power supply will also cause a DC LOW condition.

C. AC LOW

3.04 A second UNIBUS lead is used to monitor the ac input to the power supplies within the CU. This lead is designated AC LOW and can be accessed on all UNIBUS connectors on pin BF2 (yellow lead). AC LOW is asserted when a power supply detects the ac input power has dropped below 95 volts or is not within the 47-63-Hz range. Additional causes could be due to:

- AC power source created major ac voltage fluctuation.
- AC power distribution problem.
- Defective AC LOW detection circuit.
- An operated ac circuit breaker.

3.05 An AC LOW condition will cause a DC LOW condition and will have all the symptoms of a DC LOW plus additional symptoms. When an AC LOW condition is present, both AC LOW and DC LOW alarm indications are given. Refer to DEC H720E Power Supply Manual for information on AC LOW or DC LOW detection circuits. Use the AC LOW procedure for AC LOW troubles.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
1	AC LOW alarm indication.	Perform Trouble Sectionalizing Procedure A (initial ac power check).
2	AC LOW still exists.	Using a VOM, measure the ac voltage at CU cabinets (Fig. 4). Measure at spare receptacles in rear of cabinet. AC voltage should indicate 115 ±12 volts.
3	AC LOW still exists.	Prepare 453 oscilloscope to measure 115 volt 60-Hz signal as shown in Fig. 7. ***Important—Use an X10 voltage probe.*** Connect voltage probe to spare outlet in cabinet. Trace should appear on oscilloscope as shown in Fig. 7.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
4	AC LOW still exists. ***Probable Cause:*** Malfunction of power supplies within the CU.	Using a VOM, measure the output of each supply to determine which supply is asserting AC LOW. Refer to DEC engineering drawings for troubleshooting.

D. AC LOW or DC LOW Using UNIBUS Termination Method (See 4.05 and 4.06)

3.06 The UNIBUS termination method (see Part 4) can be used to isolate the cause of DC LOW and AC LOW signals when asserted on the UNIBUS. Since all power supplies parallel this information on two UNIBUS lines, the concept is to isolate the device causing trouble by decreasing the length of the system UNIBUS and isolating various device power supplies from asserting these signals. The UNIBUS is terminated in various places until the trouble is located. The following procedure is a typical example showing AC LOW or DC LOW trouble sectionalizing using UNIBUS termination method:

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
1	AC LOW or DC LOW alarm condition exists.	At the processor drawer, operate the OFF/ON/PANEL LOCK switch to OFF.
2		At the RP04 disk controller, terminate the UNIBUS with a M9302 UNIBUS terminator. (See 4.05-4.06.) Prepare VOM to measure +3.5 volts and connect to AC LOW or DC LOW signal lead (BF2 or BF1 respectively) on M9302 UNIBUS terminator. (Connect other VOM lead to ground).
3		***Caution: Before turning power on, make sure UNIBUS cable is not grounded to frame.*** At the processor drawer, operate the OFF/ON/PANEL LOCK switch to ON and observe VOM. VOM should indicate 0 or +3.5 volts. If the VOM indicates +3.5 volts, the trouble is beyond the RP04 disk controller. See Fig. 1 for UNIBUS structure, then refer to Step 5. If VOM indicates 0 volt, the trouble is in the RP03 disk controller, or closer to the processor. Refer to Fig. 1 and go to Step 6.
4		At the processor drawer, operate the OFF/ON/PANEL LOCK switch to OFF. Remove the M9302 UNIBUS terminator from the RP04 disk controller and restore original UNIBUS connection to normal. Remove VOM connection.
5	VOM indicates +3.5 volts in Step 3, CORRECTIVE ACTION column.	(1) At the processor drawer, operate the OFF/ON/PANEL LOCK switch to OFF.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
		(2) Remove the M9302 UNIBUS terminator from RP04, and reconnect the original section of UNIBUS cable. (3) Slide out system drawer No. 1 and remove panel. Remove the UNIBUS from the rear of the drawer and replace with a M9302 UNIBUS terminator. (4) Prepare VOM to measure +3.5 volts and connect to BF2 (AC LOW) or BF1 (DC LOW) pin (other VOM lead to ground). (5) At the processor drawer, operate the OFF/ON/PANEL LOCK switch to ON. (6) If VOM indicates 0 volts, power supply in system drawer No. 1 is cause of trouble. (7) If VOM indicates +3.5 volts, systematically delete system units from the UNIBUS structure according to UNIBUS structure (Fig. 1) until the AC LOW or DC LOW signal is no longer present (+3.5 volts present). The unit deleted, which causes the VOM to indicate +3.5 volts, is the cause of the malfunction due to a faulty power supply or a short on the DC LOW or AC LOW lead. Refer to DEC engineering drawings for trouble-shooting.
6	VOM indicates 0 volts in Step 3 CORRECTIVE ACTION column.	(1) At the processor drawer, operate the OFF/ON/PANEL LOCK switch to OFF. (2) Remove the M9302 UNIBUS terminator from RP04 and reconnect the original section of UNIBUS cable. (3) Slide out system drawer No. 2 and remove panel. Remove the UNIBUS from rear of the drawer and replace with M9302 UNIBUS terminator. (4) Prepare VOM to measure +3.5 volts and connect to BF2 (AC LOW) or BF1 (DC LOW) pin (other VOM lead to ground). (5) At the processor drawer, operate the OFF/ON/PANEL LOCK switch to ON. (6) If VOM indicates 0 volts, power supply in drawer No. 2 is cause of failure.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
		(7) If VOM indicates +3.5 volts, systematically add system drawer and/or units according to UNIBUS structure (Fig. 1) until the AC LOW or DC LOW signal is asserted (0 volts). The system or unit which causes the 0 volt signal to be asserted is causing the malfunction. Refer to DEC engineering drawings for trouble-shooting.

4. DEVICE MALFUNCTIONS—TROUBLE SECTIONALIZING

A. UNIBUS Termination and Device Isolation

4.01 The structure of the CU, based on the UNIBUS, presents an easy method of isolating malfunctioning devices within the CU by allowing them to be removed from the system structure. The UNIBUS is the means for interdevice communication. Therefore, removing a device from the UNIBUS structure is allowable as long as that device is not required for the processor to execute the program. When the UNIBUS is to be terminated, always remove the power, terminate the device, and then restore power.

4.02 If an illegal instruction is executed, such as an odd address, time-out errors, false addresses, or reserved instruction, the processor will halt and trap to location 000004 (octal). When this happens, address 000006 will be displayed on the address register of the console and audible and visual alarms will be activated. When the processor traps to address 000004 it is usually an indication of a software trouble, although a device failure may also cause it to trap.

4.03 Before a device is removed from the UNIBUS structure, maintenance personnel should refer to Fig. 1 to determine the structure of the UNIBUS cable. The device can then be removed by performing the following steps:

(a) Remove system power.

(b) At the device to be removed, physically remove the UNIBUS cable at the input connector.

(c) Remove the UNIBUS cable connection at the input of the adjacent device (electrically).

(d) Connect the UNIBUS cable removed in Step (b) to the input UNIBUS connector of the device the UNIBUS cable was removed from in Step (c).

(e) Restore system power.

4.04 Fig. 8 is a typical example of device isolation. It shows how a device is removed from the UNIBUS structure. In this case, the BD04 alarm circuit is being isolated. ***Power should always be removed before, and restored after the device is isolated.***

4.05 Another method of isolating faulty devices associated with the UNIBUS is to terminate the UNIBUS with a M9302 UNIBUS terminator. This isolates sections of the UNIBUS, rather than a single device. The UNIBUS is sectionalized by simply removing the UNIBUS output of a device where the UNIBUS is desired to be sectionalized, and placing a M9302 UNIBUS terminator in the vacant connector. The UNIBUS structure will then contain all devices from the processor to the device where the M9302 UNIBUS terminator is inserted. Moving the M9302 UNIBUS terminator electrically toward or away from the processor (depending on whether trouble condition is still present), can isolate the particular device causing the trouble. The device can then be isolated as described in 4.03 and 4.04.

4.06 Fig. 9 is a typical example of device termination. It shows how a section of the UNIBUS is terminated. In this case, the UNIBUS is terminated at the moving head disk. ***Power should always be removed before, and restored after, the section of UNIBUS has been terminated.***

B. Diagnosing System Troubles

4.07 Maintenance personnel should become thoroughly familiar with the structure of the UNIBUS to assist in diagnosing system malfunctions. The following list contains pertinent facts concerning the UNIBUS.

- UNIBUS is in three sections:
  - (a) Main UNIBUS—before DB-11A bus extender
  - (b) UNIBUS extension—after each DB-11A bus extender (2)
- Various devices create their own UNIBUS:
  - (a) RJP04 disk controller to RP04 disk
  - (b) TJU16 magtape controller to TU16 transport
- The WECo cabinets are not directly tied to the UNIBUS in any way.
- UNIBUS is connected between devices as outlined in UNIBUS structure diagram.
- UNIBUS runs from front to rear in all system drawers.
- Be sure power is ***off*** before removing any UNIBUS cables.
- After a UNIBUS cable is removed, be sure the cable is not shorted to ground before applying power.

4.08 The detection of device failure within the CU is not always clearly defined. Troubles are sometimes detected by knowing what a device or program should do and seeing that it is not doing what it should. This type of trouble detection is developed with experience but does not provide an easy method to determine device failure. Therefore, to determine the operational ability of the CU, a magnetic tape of diagnostic programs is supplied as part of the system. The uses of the programs are outlined in the program listings which are supplied with the system.

4.09 If the diagnostic programs cannot be loaded into core memory, a UNIBUS related trouble is indicated and devices must be deleted from the UNIBUS structure until the diagnostic programs can be loaded and executed.

C. Loading and Executing DEC Diagnostic Programs

4.10 The following procedure describes the method used to load and execute the DEC diagnostic programs. The programs are stored on 9-track magtape which must be read into core memory.

Caution: If any diagnostic procedures are to be run on RP04 disk unit, the EADAS/NM programs must be stored on 9-track magtape and removed from the tape transport. If disk unit diagnostics are not to be run, operate the WRITE PROTECT switch on the disk unit to prevent accidentally destroying the program. See Section 252-116-301 for operating procedures.

STEP	ACTION	VERIFICATION
1	Remove 9-track magtape from transport and mount the magtape containing diagnostic programs.	
2	At processor— Set HALT/ENABLE switch to HALT.	
3	Momentarily depress START switch (CU is initialized).	
4	Operate LOAD ADRS switch.	

STEP	ACTION	VERIFICATION
5	Set SWITCH REGISTER swiches to: 17765000 (001 111 111 110 101 000 000 000).	
6	Operate LOAD ADRS switch.	ADDRESS REGISTER indicates— 17765000 (001 111 111 110 101 000 000 000).
7	Set HALT/ENABLE switch to ENABLE.	
8	Depress START switch.	
	Note 1: Diagnostic programs are read into core memory.	
	Note 2: Refer to DEC documentation associated with diagnostic programs to obtain information regarding their use.	

D. Fault Isolation of Wall Display Board

4.11 In the event of an apparent wall display board malfunction, it is necessary to determine whether the failure is related to the wall display board or to the processor. Isolate the trouble as follows:

STEP	ACTION	VERIFICATION
1	Obtain release of CU from traffic personnel.	
	Note: Run the WLTST program using the user's manual to verify the existence of a trouble. If blocks of indicators flip while other blocks do not flip, suspect the voltage regulator or the wall display board driver circuit of overheating and turning itself off. Monitor the +5V output, if this is suspected. If isolated indicators flip and small groups flip, suspect the parity disable function of being inoperative. This function is disabled by a strap on the edge connector of the Ferranti Packard wall display board from terminal 42, to 43.	
2	Disconnect the wall display board from processor and connect wall display board test set to the wall display board.	
3	Perform tests outlined in Section 252-116-501.	
4a	If wall display board tests fail, the trouble is isolated to the wall display board.	
5b	If wall display board tests indicate no malfunction of the wall display board, the trouble is in either the processor, DR11-C interface, wall	

STEP	ACTION	VERIFICATION
	display board driver circuit, cables, or the parity check circuit of the Ferranti Packard wall display board. (See note after Step 1.)	
6b	Perform diagnostic procedures for the DR11-C. (See 4.10 for procedures.) Be sure to sync system first.	When diagnostic procedures fail— Trouble is isolated to processor or interface. When diagnostic procedures pass— This indicates the processor and interface are operating properly.
7c	If DR11-C diagnostic procedures pass— The fault is probably in the wall display board driver circuit. Replace the wall display board driver circuit.	
8c	Run the WLTST program using the user's guide.	
9d	If the WLTST program indicates no existance of a trouble— The fault was in the replaced wall display board driver circuit. Restore system to normal condition. End of test.	
10e	If the replaced wall display board driver circuit in Step 7c does not correct the problem or if no replacement was available— Operate HALT/ENABLE switch to HALT. ***Note:*** Steps 11e through 15e loads a diagnostic program to check the wall display board. The diagnostic program writes to the wall display board repeatedly to facilitate testing with the oscilloscope.	
11e	Set SWITCH REGISTER switches to 1000 (001 000 000 000) (address).	
12e	Operate LOAD ADRS switch.	ADDRESS REGISTER lamps indicate 1000 (001 000 000 000).
13e	Set SWITCH REGISTER switches to 012700 (000 001 010 111 000 000) (data).	
14e	Lift DEP switch.	DATA REGISTER lamps indicate 012700 (000 001 010 111 000 000).
15e	Repeat Steps 11e through 14e using addresses and data in Table A.	

STEP	ACTION	VERIFICATION
16e	Set SWITCH REGISTER switches to 1000 (001 000 000 000).	
17e	Operate LOAD ADRS switch.	ADDRESS REGISTER lamps indicate 1000 (001 000 000 000).
18e	Operate HALT/ENABLE switch to ENABLE.	
19	Operate START switch.	
20f	If indicators on wall display do not flip— Connect oscilloscope to 115 Vac near the front of cabinet B.	
21f	Set oscilloscope controls as shown in Fig. 10.	
22f	Connect oscilloscope EXT SYNC to pin 620 on miscellaneous terminal strip with P6010 voltage probe.	
23f	Connect other P6010 voltage probe to pin 018 on miscellaneous terminal strip in cabinet B (front).	Level will fluctuate between -5V and +5V at a frequency of about one second. Trace indicated on oscilloscope as shown in Fig. 10.
24f	Repeat Step 23f using pins listed in Table B.	Fluctuations should be observed on all pairs of leads. ***Note:*** Each test to a higher pin number will indicate a decrease in frequency by a factor of 2, except terminals 620, 621, 022, and 122.
25g	If trace indicated in Fig. 10 does not appear on oscilloscope in Steps 23f or 24f— Disconnect the cable connector connected to the input of the wall display driver circuit.	
26g	Set oscilloscope controls as shown in Fig. 11.	
27e	If the replaced wall display board driver circuit in Step 7c does not correct the problem or if no replacement was available— Connect the P6010 voltage probe in the connector terminal C.	Trace appeared on the oscilloscope as shown in Fig. 11.
28g	If trace indicated in Fig. 11 does not appear on oscilloscope in Step 23f or 24f— Repeat Step 27e for terminals K, NN, U, L, N, R, T, W, X, Z, AA, BB.	Trace appeared on oscilloscope as shown in Fig. 11. Levels will fluctuate between ground and +5V.

STEP	ACTION	VERIFICATION
29h	If trace appeared in Step 28g— Wall display driver circuit pack faulty.	
30i	If trace did not appear in Step 28g— Cabling from DR11-C to wall display driver circuit pack faulty.	
31	Replace faulty equipment and restore system to normal condition.	

E. Fault Isolation of Model 40 CRTs and Associated Circuitry

4.12 To determine if the Model 40 CRT or associated circuitry has or has not failed, perform the following procedures.

1. Select an operational CRT near the suspected nonoperational CRT and disconnect cable connectors from both CRTs. Log out on both CRTs before starting. If the CRTs are not logged out, it may be necessary to kill a process before the computer will recognize the CRT. See the user's manual for assistance. If a group of four or more CRTs are inoperative, suspect the DEC equipment. Run diagnostics on the DH11.

2. Connect the cable of the operational CRT-port to the suspected nonoperational CRT and attempt operation.

3. If suspected CRT is still nonoperational, it is faulty and shall be repaired.

4. If the suspected CRT is operational, the CRT is not faulty. Continue to Step 5.

5. Remount the cable connectors to original positions.

6. At DH11 distribution panel (cabinet 05)—After syncing and powering down the system, disconnect the two cable connectors from the M970 circuit boards associated with the two CRTs.

7. Connect the cable of the suspected CRT to the circuit board associated with operational CRT.

8. If suspected CRT is still nonoperational, the channel connecting CRT to circuit board is faulty. The trouble on the channel can be isolated further by interchanging cables at the data sets.

9. If suspected CRT is operational, the cable is not faulty. Remount cable connectors to original position and continue to Step 10.

10. If the DEC equipment is faulty, refer the problem to DEC. Further trouble isolation should proceed as follows with or without DEC present. The following steps describe how to interchange M970 and M594 circuit boards with power removed.

11. Obtain release of CU from traffic department for halt condition.

12. Sync the system and halt the CU by operating the HALT/ENABLE switch to HALT. Turn off the disk. Turn off the power switch on the processor.

13. Interchange the two M594 circuit boards at the DH11 distribution panel associated with the two CRTs.

14. If the suspected CRT is still nonoperational after rebooting, repeat the test interchanging the M970 circuit boards associated with the channels.

15. If the suspected CRT is operational, the replaced circuit board is faulty. Have DEC replace the faulty circuit board and restore circuits to original condition.

16. Restore CU by turning on disk, operating HALT/ENABLE switch to ENABLE, and rebooting according to the user's manual.

F. ROP Test

4.13 The operation of the DATASPEED 40 receive-only printer (ROP) links may be verified by performing the following ROP test which causes a 59 character print-out on both ROPs.

STEP	SYMPTOM OR CONDITION	CORRECTIVE ACTION
1	At DATASPEED 40 KDP— Type: **ROPTEST**	DATASPEED 40 CRT displays— **Select one of the following: ≡** **x = exception printer (PORT 5) ≡** **m = monitor printer (PORT 6) ≡** **b = both printers ≡**
2	Type: **x**, **m**, or **b** depending on which printer is to be tested.	DATASPEED 40 ROP responds— **ROP TEST:** **!"#$%&*+,-./Ø123456789:;<=>?@ABCDEF GHIJKLMNOPQRSTUVWXYZ[\]^~**

G. Fault Isolation of Data Transmission Facilities for Communications From EADAS to EADAS/NM

4.14 If a problem is suspected in the intercomputer communication and the computers are collocated, check the null-modem connection to ensure proper connection between the computers. If the computers are remotely located, ensure that the connection to the data set is properly made.

4.15 If all the connections are properly made, a check of the data transmission facilities (DQ) is required. Disconnect the DQ from the null-modem (if EADAS is collocated) or the 209A data set (if EADAS is remotely located). Terminate the disconnected cable with the test connector (2.03). Run the following DQ11 loop/link test.

Note: If a 209 data set is used, it will be necessary to reoption the DQ11 for 209A data set not provided per SD-3B237-01 note 310, before the diagnostic test is performed.

4.16 The DQ11 loop/link test tests the ability of the DQ11 to transmit and receive. Using a DEC H315A modem test connector (or equivalent EIA loop-around), a single DQ11 can be tested. Using the 209A data sets in appropriate loop-around modes, portions of the data link can be tested (loop test) with option YM provided in the 209 data set. By connecting the channel between the basic EADAS and EADAS/NM, a complete end-to-end test can be carried out (link test). These tests should be run on the DECwriter. The steps required to perform the above two tests are the same except that on the link test, Step 2 is omitted.

STEP	ACTION	VERIFICATION
1	At DECwriter— Terminate any programs in progress by typing **STOP** and depressing the RETURN key.	DECwriter responds— **sync done**
2a	If performing the loop test— Remove cable at modem (null-modem or 209A data set) and insert DEC H315A modem test connector into end of cable.	
3	At DECwriter— Type: **DQMSG**	

STEP	ACTION	VERIFICATION
4	Depress LF key.	DECwriter responds— **loop test from eadas/nm to eadas via dq-11 channel (0-5)=**
5	Type: **n**	**n** represents the EADAS link being tested (0 through 5). The program will execute two seperate processes to receive and transmit messages. DECwriter responds— **DQRMSG:FD=x** **DQRMSG:FD=x CHANNEL y** **ENTER 'STOP' TO TERMINATE TEST** **ENTER TEST MESSAGE:** **x** represents either 2 or 3. **y** represents the channel number being tested.
6	Type a line of text material.	The program will transmit the text and if successful, the DECwriter will respond— **TX OK** **MESSAGE FROM CHANNEL y** Line of text material. **ENTER TEST MESSAGE**
7	Type: **STOP**	
8	Depress RETURN key.	DECwriter responds— **TEST TERMINATED** **FUNCTION:**
9	Remove the DEC H315A modem test connector from cable and insert cable into the modem.	
10b	If the test was successful— Suspect the troubles at the modem, in the connections between the modem or data sets, or in the hardware on the basic EADAS machine.	
11c	If the test was not successful— Suspect the trouble at the DQ11 and run the diagnostics on the DQ11 to isolate the trouble.	

STEP	PROCEDURE

H. TCT Tests

1 Set the KS-20937 E2A digital simulator test set close to the first TCT to be tested and plug in power cord.

2 Connect the List 8 TCT test cable between the test set and the J2 connector of TCT to be tested.

3 Set the switches on the test set as follows:
MESSAGE LENGTH WORDS to 1
RCU to OFF
WORD 1 (bits 1-17) to UP
SYSTEM to E2A
PARITY to B
BIT RATE (bits/sec) to 1200
MODE to ANSWER
ENABLE to NORMAL
DISPLAY ERROR WORD to ON
DISPLAY WORD SELECT to ALL
POWER to ON

Note: If the ERROR WORD indicator lights during a test, the error condition must be corrected. Before continuing the test, momentarily depress the RECEIVE CLEAR button.

4 At the DECwriter—
In response to the function message—
Type: **tct <return>**

Response: **tct number?**

5 Type: **0 <return>**

Response: **add or delete?**

6 Type: **a <return>**

Response: **function =**

7 Type: **tcttest <return>**

Response: **tct acceptance and maintenance test**
tct number?

8 Type: **0 <return>**

Response: **testing/dev/tct0**
enter h for help
enter 0 for exit

STEP	PROCEDURE

hit rubout to end test
test?

9 Type: **h <return>**

Response: **h---help**
0---exit
1---single tx
2---multiple tx
3---single rx
4---not used
5---rx timeout
6---parity error check
7---multiple rex
8---tx(1)-rx
9---tx(3)-rx
10---tx timeout

test?

Single Transmit Test

This test verifies the computer output to TCT input interface. Data words will be transmitted one at a time from the computer to the TCT and then forwarded to and displayed on the test set. The following data words should be used to verify the interface. Along with each data word is given the contents of the word expected to be displayed on the test set indicators. See Table C.

10 Type: **1 <return>**

Response: **single tx test**
hit cr to tx next word
tx'd word printed

Response: 0 000 000 000 000 000

11 Compare word received on test set with INFORMATION and PARITY bits shown in Table C.
After each word has been compared—
Type: **<return>**

Response: **(next word)**

12 After all four word are received and checked—
Type: **<rubout>**

Response: **test?**

STEP	PROCEDURE

Multiple Word Transmit Test

This test verifies that the TCT can handle multiple word transmissions. Sixteen word transmissions (a logic one being shifted one bit at a time through an otherwise all zero data field) should be cycled with a one second delay between cycles. When the words are transmitted from the computer via the TCT to the test set, the RECEIVE INFORMATION indicators 2 thru 17 should light up momentarily one at a time from left to right (2 to 17). Bit 1 should be OFF for the first transmission, but ON for the following 15 transmissions of each cycle and for the one second interval between cycles. The E2A CONT indicator should be ON for the first 15 transmissions and OFF for the 16th transmission of each cycle and for the one second interval between cycles. By rotating the DISPLAY WORD SELECT switch from position 1 to 16 each of the 16 received words can be visually checked and verified.

13 Type: **2 <return>**

Response: **multiple word tx test**
tx group of sixteen words
with one bit set starting
with bit 0 and shifting
to bit 15 with one second
pause between cycles

14 Observe and verify automatic test operation.
Rotate the DISPLAY WORD SELECT switch and check each of the 16 received words.

15 After all words are received and checked—
Type: **<rubout>**

Response: **test?**

Single Word Receive Test

This test verifies the TCT output to computer input interface. The TCT is enabled by the computer to transmit one word at a time (content unimportant) to the test set and then to receive a one word reply from it for each word transmitted. The reply from the test set is then passed on via the TCT to the computer and the results printed on the DECwriter. The switch arrangements for WORD 1 for each reply from the test set as well as the data and status words printed out on the DECwriter for each of these replies is given in Table D.

16 Set WORD 1 switches on test set per first word in Table D.

17 At DECwriter—
Type: **3 <return>**

Response: **receive single word**
hit cr to receive next
character

STEP	PROCEDURE

18 Type: <return>

Response: **0 000 000 000 000**

19 Set up next word on the test set.

20 Type: <return>

Response: (Associated word printed on DECwriter).

Note: Test set receives 1st word of Table C for all tests.

21 Complete words listed in Table D—
Type: <rubout>

Response: **test?**

Receive Timeout Test

This test verifies the station fail time-out circuitry.

22 At test set—
Set the MODE switch to ONCE.

23 Set the WORD 1 switches to all ones (bits 1-17 up).

24 At DECwriter—
Type: **5** <return>

Response:
```
rx timeout test
hit cr to cycle
should get read failure
message
if program gives no response
in five seconds, timeout
has failed and program is
hung
```

25 Type: <return>

Response:
```
read: i/o error
***read failure***
```

Note: This response indicates the proper time-out has occurred.

26 Type: <rubout>

Response: **test?**

STEP	PROCEDURE

Parity Error Check

This test verifies the parity error circuitry.

27 At test set—
Set the following switches as shown:
MODE switch to ANSWER
PARITY switch to A.
WORD 1 switches to all ones (bits 1-17 up)

28 At DECwriter—
Type: **6 <return>**

Response: **parity check test**
hit cr to cycle
should get read failure
if parity is bad

29 Type: **<return>**

Response: **read i/o error**
***** read failure*****

30 Type: **<rubout>**

Response: **test?**

Two Word Command Test

This test verifies that the TCT can handle two word command transmissions.

31 At test set—
Set the following switches as shown:
PARITY switch to B
MESSAGE LENGTH WORDS switch to 1
WORD 1 switches to all ones (bits 1-17 up)
DISPLAY WORD SELECT switch to 2.

32 Momentarily depress the RECEIVER CLEAR button to turn the RECEIVE display indicators off.

33 At DECwriter—
Type: **8 <return>**

Response: **two word tx test**
hit cr to cycle
will tx 0, 177777, and
print rx'd word

STEP	PROCEDURE
34	Type: <return> Response: **1 111 111 111 111 111** Response at test set per Table E.
35	At test set— Set DISPLAY WORD SELECT switch to 1.
36	At DECwriter— Type: <return> Response: **1 111 111 111 111 111** Response at test set per Table E.
37	Type: <rubout> Response: **test?**

Three Word Transmission Test

This test verifies that the TCT can handle three word command transmissions.

38	At test set— Set DISPLAY WORD SELECT switch to 3
39	Momentarily depress RECEIVER CLEAR button.
40	Set the switches on WORD 1 of test set as follows: 10101010101010101
41	At DECwriter— Type: **9** <return> Response: **three word test** **hit cr to cycle** **will tx 0, 177777, 52525** **and print rx'd word**
42	Type: <return> Response: **1010101010101010** Response at test set per Table E.
43	At test set— Set DISPLAY WORD SELECT switch to 2.

STEP	PROCEDURE

44 At DECwriter—
Type: <return>

Response: **1010101010101010**

Response at test set per Table E.

45 At test set—
Set DISPLAY WORD SELECT switch to 1.

46 At DECwriter—
Type: <return>

Response: **1010101010101010**

Response at test set per Table E.

47 Type: <rubout>

Response: **test?**

Transmit Time-Out Test

This test will force the TCT to time-out in both the transmit and receive modes.

48 Disconnect the List 8 TCT test cable from the TCT installed in Step 2.

49 At DECwriter—
Type: **10** <return>

Response: **tx timeout test**
hit cr to cycle
should get tx failure
with cable removed
if no response in five
seconds, timeout has failed
and program is hung.

50 Type: <return>

Response: ***write timeout failure***

51 Type: <rubout>

Response: **test?**

52 Type: **0** <return>

Response: **function?**

STEP	PROCEDURE
53	Reconnect TCT to system.

I. Fault Isolation of TCTs

4.17 If a communication problem exists in the TCT/E2A network, run the following E2A test. This program permits verification of which link or links are faulty. Refer to SD-3B230-01 sheet H1 for a block diagram of the E2A link.

STEP	ACTION	VERIFICATION
1a	At DATASPEED 40— At the directory window— Type: **TG**	
2a	Operate SEND key.	CRT displays— **TGOO TRUNK GRP PAGE DIRECTORY**
3a	At exit from CRT subsystem window— Type: **t**	
4a	Operate SEND key.	CRT cleared. Cursor returns to home position.
5	Operate HOME key.	Cursor returns to home position.
6	Operate S/R key.	REC, S/R lamps lighted.
7	Type: **E2ATEST**	
8	Operate RETURN key.	CRT displays— **E2ATEST←E2ATEST ≡** **←≡** **TCT-E2A Interface Test←≡** **TCT Number (0-7):←≡**
9	Type TCT number— **n** **n** represents TCT number 0-7	CRT displays— **n←≡** **←≡** **E2A Address:←≡**
10	From office records— Type the E2A address associated with TCT— **x** **x** represents the E2A remote number 1-32	
11	Operate RETURN key.	CRT displays— **x←≡** **Is Exception System running* (y or n)←≡**

STEP	ACTION	VERIFICATION
		Note: **x** is the E2A address associated with the TCT under test.
12b	If polling is in progress— Type: **y**	
13c	If polling is not in progress— Type: **n**	
14	Operate RETURN key.	CRT displays— **n**← ≡ **Testing/dev/tct n E2A address x** ← ≡ **Enter h for help** ← ≡ ← ≡ ← ≡ **Mode?** ← ≡ ***Note:*** In the first line of the CRT display, a **y** or **n** will appear depending on whether Step 12b or Step 13c was performed.
15	For ones/zero test— Type: **t**	
16	Operate RETURN key.	CRT displays— **t**← ≡ ← ≡ **remote ones/zeros test** ← ≡ ← ≡ **Ones test: x words received** ← ≡ ← ≡
17	For reverse controls test— Type: **c**	
18	Operate RETURN key.	CRT displays— **c**← ≡ **Control Circuit Test** **Ensure that correct hardware options are installed (see user's guide)**← ≡ **Release OK**← ≡ **Operate OK**← ≡ ← ≡ ← ≡ **Mode?**← ≡
19	Type: **x**	
20	Operate RETURN key.	CRT displays— **x**← ≡ ≡

STEP	ACTION	VERIFICATION
		←function:
21	Repeat Steps 6 through 20 for each E2A address assigned to TCT **n**.	

4.18 If more than one E2A remote is assigned to the TCT, some trouble isolation can be determined by knowing if only one remote channel is failing or if all channels on the TCT are failing.

Further isolation can be accomplished by connecting the E2A station test set to the TCT via a TCT test cable, and performing the following procedure.

STEP	ACTION	VERIFICATION
1	Set up the E2A station test set according to Table F.	
2	Repeat Steps 7 through 14 of the previous procedure using the address of a disconnected remote.	
3	Type: **p**	
4	Operate RETURN key.	DATASPEED 40 CRT displays— **p←** ≡ **←** ≡ **1 words←** ≡ **177777←** ≡ **←** ≡ **Mode?←** ≡
5	At E2A station test set— Operate all WORD 1 switches to the down position.	
6	Type: **p**	DATASPEED 40 CRT displays— **p←** ≡ **←** ≡ **1 words←** ≡ **0←** ≡ **←** ≡ **Mode?←** ≡
7	Type: **x**	DATASPEED 40 CRT displays— **x←** ≡ ≡ **← function:** ≡
8a	If there is no response— The trouble is on the computer side of the data set. Substitute the TCT under test with a spare TCT.	

STEP	ACTION	VERIFICATION
9	Repeat Steps 1 through 7.	
10b	If the trouble persists with the new TCT— Either the cable from the TCT to DRII-C is faulty or there is a DEC problem.	
11b	Run a diagnostic on the DRII-C (see 4.10).	
12c	If the diagnostic on the DRII-C passes— The cable must be faulty. Buzz test the cable.	

J. PBC Line Check Test

4.19 The PBC line check (LINECHK) test contains two subtests, LOOP I and LOOP II. The LOOP I subtest serves as a test of the entire EADAS PBC data pooling path including both software and hardware, Fig. 12. The LOOP I subtest polls a single block of data from a PBC and displays the results. The block contains data with a known pattern so the test operator is able to confirm whether the block is received or not.

4.20 The LOOP II subtest serves to test portions of the complete EADAS/NM-PBC data link. Prior to the test, transmit leads are "looped" around at some convenient point and connected to receiver leads. The assumption is made that the equipment "inside" the loop is functioning correctly whenever a string of messages, set up and transmitted by LOOP II, is returned unaltered to a receive buffer in EADAS/NM. Because of the "loop-around", the message data is forced back to EADAS/NM. Upon return, the message data is printed out and the user can readily determine if the loop test is successful.

Line Identification

4.21 The EADAS/NM can service up to 16 PBC links (L=0 through 15). The interface between the test software (LINECHK) and the 16 PBC links is provided by a DH11 interface circuit. This circuit has 16 output ports (P=0 through 15). Because of software design, only the odd numbered ports (ie, 1, 3, 5, 7, 9, 11, 13, 15) are used for PBCs. Therefore, two DH11s (DH=0,1) are required to service all 16 PC links. The relationship between PBC line number and DH port number is as follows:

L=DH times 8 + [(P-1)/2]

L is the line
DH is 0 or 1
P is the port

4.22 The transmit and receive leads must be grouped together to perform this test. This can be done either by placing the H315 modem test connector at the end of the EIA cable or by operating the RT button at the distant end of the data set. For example, if a H315 cap was placed on the EIA cable extracted from the data set associated with port 13, DH1, then the PBC line that is tested is L=14. $L = 1 \times 8 + [(13-1)/2]$ (Fig. 13). On the other hand, if the 202T RT button is pushed at a PBC connected to port 5, DH 0 in EADAS, then the associated PBC line is L=2. $L = 0 \times 8 + [(5-1)/2]$ (Fig. 14). The number L is used by the test operator as input when either the LOOP I or LOOP II subtest is executed under LINECHK.

LOOP I

4.23 The LOOP I subtest polls (ie, transmits command, receives response) a PBC for a block of data which has a known pattern. The following procedure describes the method of testing the entire EADAS/NM PBC data polling path.

STEP	ACTION	VERIFICATION
	Note: The PBC must be loaded with the 3.1 software generic or successor.	

STEP	ACTION	VERIFICATION
1	To enable the EADAS/NM data port at the PBC— At the PBC DATA SPEED 40 station, type the following command— **ENBL:DPORT:EADAS**	
2	Operate RETURN key.	
3	At EADAS/NM— Type: **LINECHK** ***Note:*** The LOOP I subtest can be run at either the EADAS/NM DECwriter or an EADAS/NM CRT following a **FUNCTION** indication.	
4	Operate RETURN key.	EADAS/NM CRT displays— **PBC LINE (0-15) =**
5	Type the line identification number (L = 0 through 15) of the PBC line being tested.	
6	Operate RETURN key.	Response— **IS EXCEPTION SYSTEM RUNNING?**
Exception System Running		
7	Type: **y**	
8	Operate RETURN key.	Response— **IS PBC L ON-LINE?**
9a	If PBC L is on-line— Type: **y**	
10a	Operate RETURN key.	
11a	Type: **SET PBC L OFF**	
12a	Operate RETURN key.	
13a	Repeat Steps 3 through 6.	
Exception System Not Running		
14	Type: **n**	
15	Operate RETURN key.	Response— The output of the LOOP I subtest is printed in two parts. The first describes the command message

STEP	ACTION	VERIFICATION
		transmitted from EADAS/NM to the PBC. The second describes the data block response from the PBC. PART 1 Response— **TEST PATTERN TRANSMITTED FOR DH11 n LINE m** **command word 1** **command word 2** **command word 3** **command word 4** **n** equals the DH11 number (0 or 1) **m** equals the remainder (0 to 7) after dividing L by 8. (For example: If L=13, then n=1 and m=5, or if L=5, then n=0 and m=5. Part 2 Response— **PATTERN RECEIVED FOR DH11 n LINE m** **1st word (401)** **2nd word (404XX)** **3rd word (XXXXX)** **4th word (XXXXX)** Words 1 through 4 represent the words in the block of data received from the PBC. When the four words have the values shown in parenthesis (x is variable) the test succeeds and implies that the entire EADAS PBC loop is operational. Otherwise, the test fails and the malfunction is in the loop.

LOOP II

4.24 The LOOP II subtest is a data throughput test of a portion of the EADAS/NM transmit and receive chain to and from a PBC. The portion of the chain tested is determined prior to the test by the position of a loop-around which connects the transmit leads to the receive leads in the data link. Figures 13 and 14 show two convenient points to insert the loop-around in the EADS/NM-PBC data link. The following procedure describes the method of performing a data throughput test of a portion of the EADAS/NM transmit and receive chain to and from a PBC. Implementation of the loop-around as shown in Fig. 13, permits the LOOP II test to test transmit and receive equipment out to the 202T data set in EADAS/NM. Implementation of the loop-around as shown in Fig. 14, permits the LOOP II test to test the 202T data set at EADAS/NM plus the physical wiring between the EADAS/NM and the PBC.

STEP	ACTION	VERIFICATION
1	At EADAS/NM DECwriter— Terminate any programs in progress by typing **STOP** and depressing the RETURN key.	EADAS/NM DECwriter responds— **FUNCTION:**

STEP	ACTION	VERIFICATION
2a	If the LOOP II test is to be performed between the DH11 and 202T data set at the EADAS/NM end of the link (Fig. 13)— Remove the EIA cable from the 202T data set corresponding to the PBC line being tested and insert DEC H315A modem test connector into end of cable.	
3b	If the LOOP II test is to be performed between the DH11 through the 202T data set at the EADAS/NM end of the link and the 202T data set at the PBC end of the link (Fig. 14)— At the rear of the 202T data set at the PBC end of the link— Depress RT key.	
4	At EADAS/NM— Type: **LINECHK** ***Note:*** The LOOP I subtest can be run at either the EADAS/NM DECwriter or an EADAS/NM CRT following a **FUNCTION:** indication.	
5	Operate RETURN key.	EADAS/NM CRT displays— **PBC LINE (0-15) =**
6	Type the line identification number (L=0 through 15) of the PBC line being tested.	
7	Operate RETURN key.	Response— **IS EXCEPTION SYSTEM RUNNING?**
Exception System Running		
8	Type: **y**	
9	Operate RETURN key.	Response— **IS PBC L ON-LINE?**
10c	If PBC L is on-line— Type: **y**	
11c	Operate RETURN key.	
12c	Type: **SET PBC L OFF**	
13c	Operate RETURN key.	
14c	Repeat Steps 4 through 7.	

STEP	ACTION	VERIFICATION
Exception System Not Running		
15	Type: **n**	
16	Operate RETURN key.	Response— The output of the LOOP II test is printed at the DECwriter in two parts. PART I The following output describes the string of message data transmitted from EADAS/NM: **TEST PATTERN TRANSMITTED** **FOR DH11 n LINE m** **MESSAGE WORD 1** **MESSAGE WORD 2** **MESSAGE WORD 3** **MESSAGE WORD 4** **n** equals the DH11 number (0 or 1). **m** equals the remainder (0 to 7) after dividing L by 8. (For example: if L=13, then N=1 and M=5 or if L=5 then N=0 and M=5.) PART II The following output describes the message data as it appears at the received end of the loop-around: **PATTERN RECEIVED FOR** **DH11 n LINE m** **1st word** **2nd word** **3rd word** **4th word** When the LOOP II test is executed and the received message words are identical to the transmitted message data, the test succeeds, otherwise, the test fails and its failure implies an equipment malfunction inside the loop.

K. Checking Alarm Circuit Using an Oscilloscope

4.25 The operation of the alarm circuit may be verified by inputting its diagnostic program and following the outlined procedure provided with the diagnostic listing. The circuit operation can also be verified by use of the PDP-11 switch register and an oscilloscope. The following procedure describes how to check the alarm circuit using an oscilloscope.

STEP	ACTION	VERIFICATION
1	At processor— Connect oscilloscope to 115 Vac outlet.	

STEP	ACTION	VERIFICATION
2	At oscilloscope— Set controls as shown in Fig. 15.	
3	Sync and halt computer.	
4	Turn off disk.	
5	Set SWITCH REGISTER switches to 764410 (111 110 100 100 001 000).	
6	Operate LOAD ADDR switch.	ADDRESS REGISTER indicates 764410 (111 110 100 100 001 000).
7	Operate DEP switch.	At alarm panel— Audible alarm sounds. MAJOR ALARM lamp lighted.
8	Disable audible alarm by operating the ALARM DISABLE switch.	Audible alarm silenced.
9a	If one of the two alarm actions occurred but not both— The trouble is at the alarm panel. Replace CPS 10.	
10a	Repeat Steps 5 through 8.	
11b	If neither alarm action occurred— Remove the cable from the Y034 circuit board in the alarm circuit. (See SD-3B229-01 for location of the Y034 circuit board in the cabinet and SD-3B219-01 for the location of the Y034 circuit board in the circuit.)	
12b	Attach P6010 voltage probe to channel 1 input of the oscillosopce and to terminal B of Y034 circuit board of alarm circuit.	
13b	Operate LOAD ADDR switch to reload address still on switch register while observing the scope.	A single 1 ms pulse should flash on the screen similar to the pulse in Fig. 15.
14c	If pulse does not flash on scope— Systematically replace circuit boards Y304 (slot B-3), M302 (slot C-3), and M105 (slot F-3). ***Note:*** Cut same address on M105 circuit board as the one being replaced.	
15c	Repeat Step 13b.	

STEP	ACTION	VERIFICATION
16d	If trace does appear on scope in Step 13b, but alarm did not set in Step 7— Check for +24 Vdc at alarm panel.	
17e	If +24 Vdc is present at alarm panel— Replace CPS 10 in alarm panel.	
18e	Repeat Steps 5 through 8.	
19f	If test still fails— Check wiring between alarm circuits and alarm panel.	
20	To test next alarm— Reconnect cable to Y034 circuit board.	
21	Restore ALARM DISABLE switch.	
22	Set SWITCH REGISTER switches to 764412 (111 110 100 100 001 010).	
23	Repeat Steps 6 through 19f except that in Step 7 VERIFICATION the EXCEPT ALARM lamp should light intead of the MAJOR ALARM lamp, and in Step 12b the P6010 voltage probe must be connected to terminal D of the Y304 circuit board of alarm circuit instead of terminal B. (See SD-3B219-01)	
Testing the Alarm Reset Function		
24	Restore ALARM DISABLE switch.	
25	Operate alarm by setting the SWITCH REGISTER switches to 764412 (111 110 100 100 001 010).	
26	Operate DEP switch.	At alarm panel— Audible alarm sounds. EXCEPT ALARM lamp lighted.
27	Set SWITCH REGISTER to 764414 (111 110 100 100 001 100).	
28	Operate DEP switch.	Audible alarm silenced. EXCEPT ALARM lamp extinguished.
29g	If the audible alarm is not silenced and the EXCEPT ALARM lamp is not extinguished— Repeat Steps 9a through 19f except that in Step 12b the P6010 voltage probe must be connected to terminal F of the Y304 circuit	

STEP	ACTION	VERIFICATION
	board of the alarm circuit instead of terminal B (see SD-3B219-01) and if circuit boards must be replaced in Step 14c, replace Y304 (slot B-3), M302 (slot D-3), and M105 (slot F-3).	
	Testing the Alarm Retriggering Function	
30	Reconnect all cables.	
31	Set SWITCH REGISTER switches to 764416 (111 110 100 100 001 110).	
32	Operate LOAD ADDR switch.	
33	Operate DEP switch, LOAD ADDR switch, DEP switch, LOAD ADDR switch in a repeated pattern for 15 seconds.	If the repetitions are less than 1.5 seconds apart— No alarms should operate. 1.5 seconds after operating the DEP switch the last time— Audible alarm sounds. MAJOR ALARM lamp lighted.
34h	If the alarms do not operate properly— Repeat Steps 9a through 19f except that in Step 12b the P6010 voltage probe must be connected to terminal J of the Y304 circuit board of the alarm circuit instead of terminal B (see SD-3B219-01), and if circuit boards must be replaced in Step 14c, replace Y034 (slot B-3), M302 (slot D-3), M306 (slot E-3), or M105 (slot F-3).	

L. AC LOW and DC LOW Alarm Checks

4.26 An AC LOW or DC LOW signal asserted on the UNIBUS will cause the audible alarm to sound, a lamp to light indicating whether it is AC LOW or DC LOW on the alarm lamp panel, and the MAJOR ALARM lamp to light. When an AC LOW or DC LOW does not cause an alarm indication to be given, perform the following procedure.

STEP	ACTION	VERIFICATION
	Note: These checks assume that an AC LOW or DC LOW condition exists.	
1	Connect oscilloscope to 115 Vac outlet and set controls as shown in Fig. 15.	
	AC LOW	
2	At disk interrupt and alarm circuit— Connect P-6010 voltage probe to channel 1 INPUT and to pin L of Y034 circuit board.	Trace appears on oscilloscope as shown in Fig. 15.

STEP	ACTION	VERIFICATION
DC LOW		
3	At disk interrupt and alarm circuit— Connect P6010 voltage probe to channel 1 and to pin N of Y034 circuit board (part of circuit wiring board).	
4a	If oscilloscope trace appears as shown in Fig. 15 but no alarm is activated— Check for +24 Vdc in alarm panel.	
5b	If +24 Vdc is present— Replace CPS10 in the alarm panel and repeat Step 2 or 3.	
6c	If trace does not appear on oscilloscope as shown in Fig. 15— Systematically replace the circuit boards Y034 (Slot B-3) and M784 (Slot C-2) and repeat Steps 2 or 3.	

TABLE A

ADDRESS	DATA
1002 (001 000 000 010)	010001 (000 001 000 000 000 001)
1004 (001 000 000 100)	010037 (000 001 000 000 011 111)
1006 (001 000 000 110)	167772 (001 110 111 111 111 010)
1010 (001 000 001 000)	005200 (000 000 101 010 000 000)
1012 (001 000 001 010)	012701 (000 001 010 111 000 001)
1014 (001 000 001 100)	100000 (001 000 000 000 000 000)
1016 (001 000 001 110)	005301 (000 000 101 011 000 001)
1020 (001 000 010 000)	001376 (000 000 001 011 111 110)
1022 (001 000 010 010)	000137 (000 000 000 001 011 111)
0124 (001 000 010 100)	001004 (000 000 001 000 000 100)

TABLE B

PIN NUMBERS ON MISC. TERMINAL STRIP				
	318	618	220	520
019	319	619	221	521
118	418	020	320	620
119	419	021	321	621
218	518	120	420	022
219	519	121	421	122

TABLE C

DATA WORD FROM COMPUTER						TEST SET INDICATORS							
						INFORMATION							PARITY
						B1	B2- -					- - -B-17	
0	000	000	000	000	000	0	000	000	000	000	000	0	0110010
1	111	111	111	111	111	0	111	111	111	111	111	1	1000101
1	010	101	010	101	010	0	010	101	010	101	010	1	0011111
0	101	010	101	010	101	0	101	010	101	010	101	0	1101000

TABLE D

TEST SET SWITCHES (WORD 1)																
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

TABLE E

TEST STEP	INFORMATION BITS																PARITY BITS							E2A CONT
	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17								
34	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0
36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1
42	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	1	1	0	0
44	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	1
46	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1

TABLE F

SWITCH	POSITION
Message Length Words	1
RCU	Off
Word 1 (Bits 1-17)	Up
System	E2A
Parity	B
Bit Rate (Bits/Sec)	1200
Mode	Answer
Enable	Normal
Display Error Word	On
Display Word Select	All
Power	On

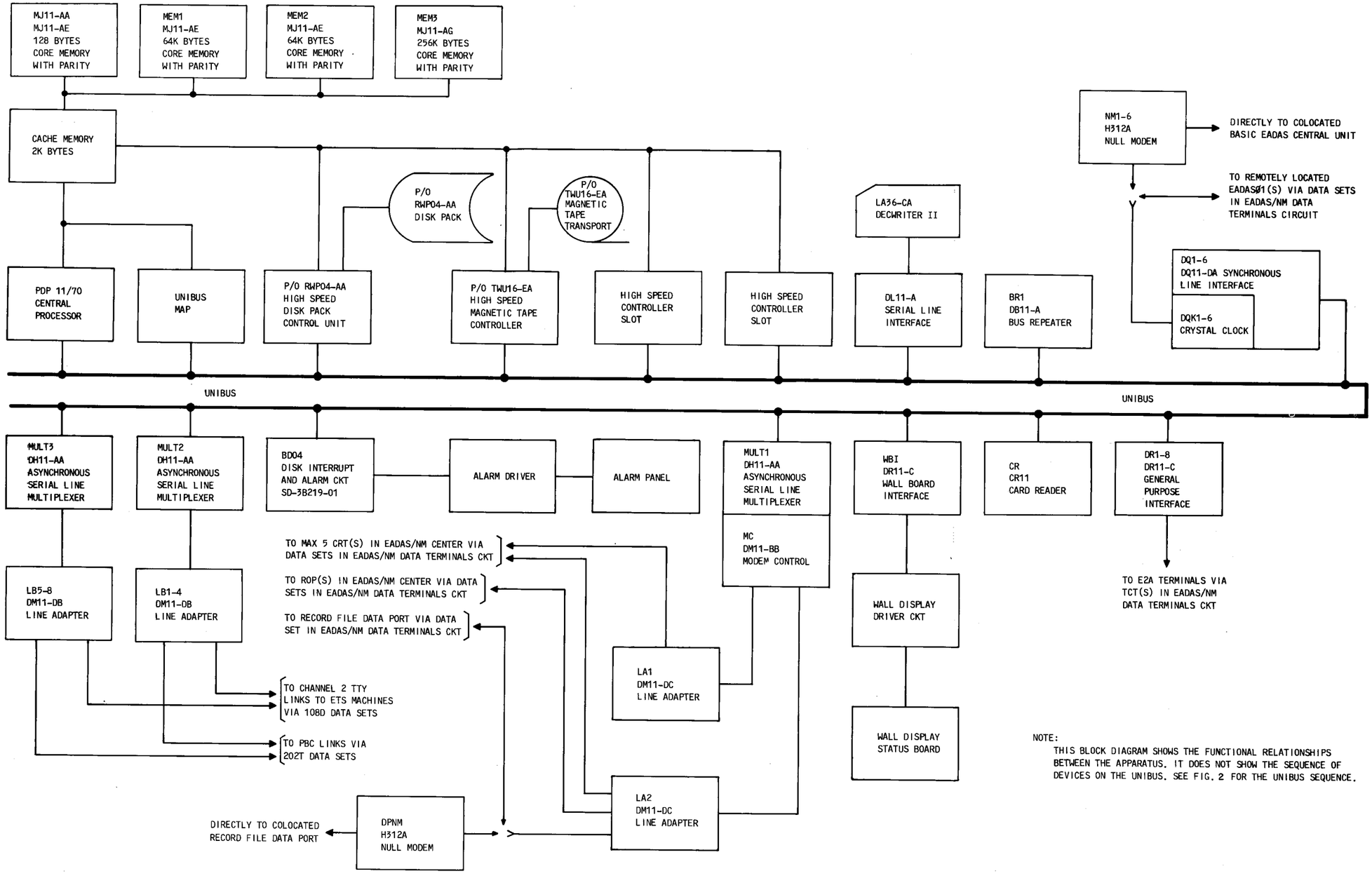
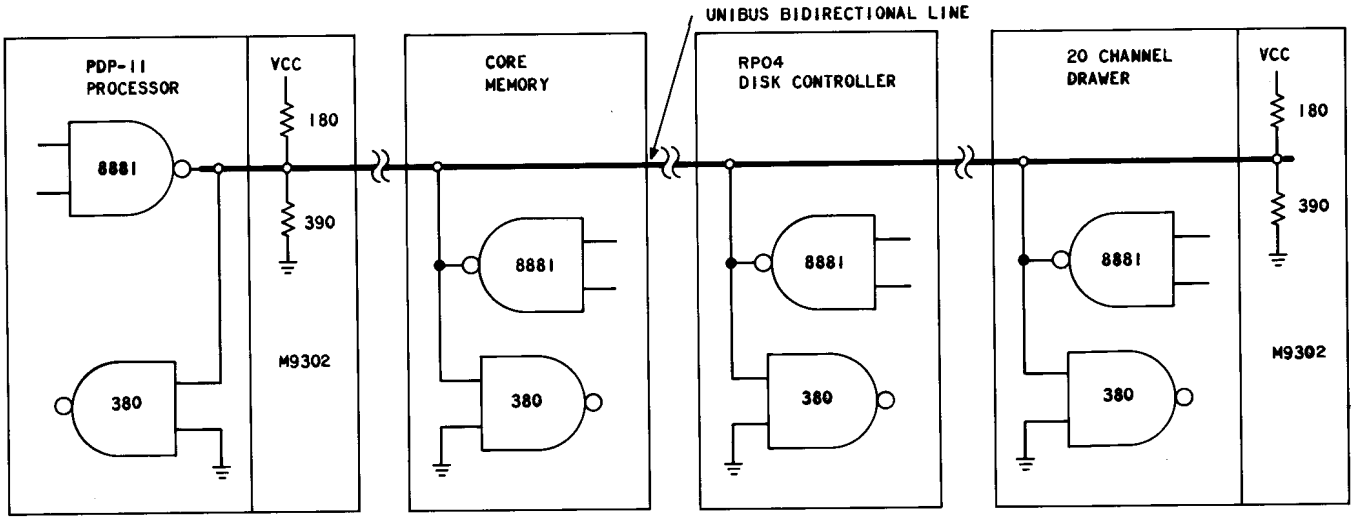


Fig. 1—EADAS/NM-Block Diagram

	CPU
	TMU16-EA
	RMP04-AA
	DL11-A
	DR11-C
⑤	CR11
	BD04
②	DQ11-DA
②	DQ11-DA
②	DQ11-DA
②	DQ11-DA
②	DQ11-DA
②	DQ11-DA
	DB11-A
④	DR11-C
④	DR11-C
④	DR11-C
④	DR11-C
	DH11-AA & DM11-BB
	DH11-AA
①	DH11-AA
④	DR11-C
④	DR11-C
④	DR11-C
④	DR11-C

Fig. 2—Unibus Sequence of Apparatus



NOTES:
1. DATA LINE 1 (DOI) IS SHOWN ON THE ABOVE EXAMPLE OF A UNIBUS BIDIRECTIONAL LINE.
2. DATO EXAMPLE: PROCESSOR 8881 AND 20 CHANNEL DRAWER 380 ARE ENABLED.
3. DATI EXAMPLE: CORE MEMORY 8881 AND PROCESSOR ARE ENABLED.
4. CONTROL OF WHICH 380IC AND 881IC IS ENABLED IS DETERMINED BY THE UNIBUS MASTER AND WHICH ADDRESS AND CONTROL LINES ARE ASSERTED.

Fig. 3—Unibus Bidirectional Line

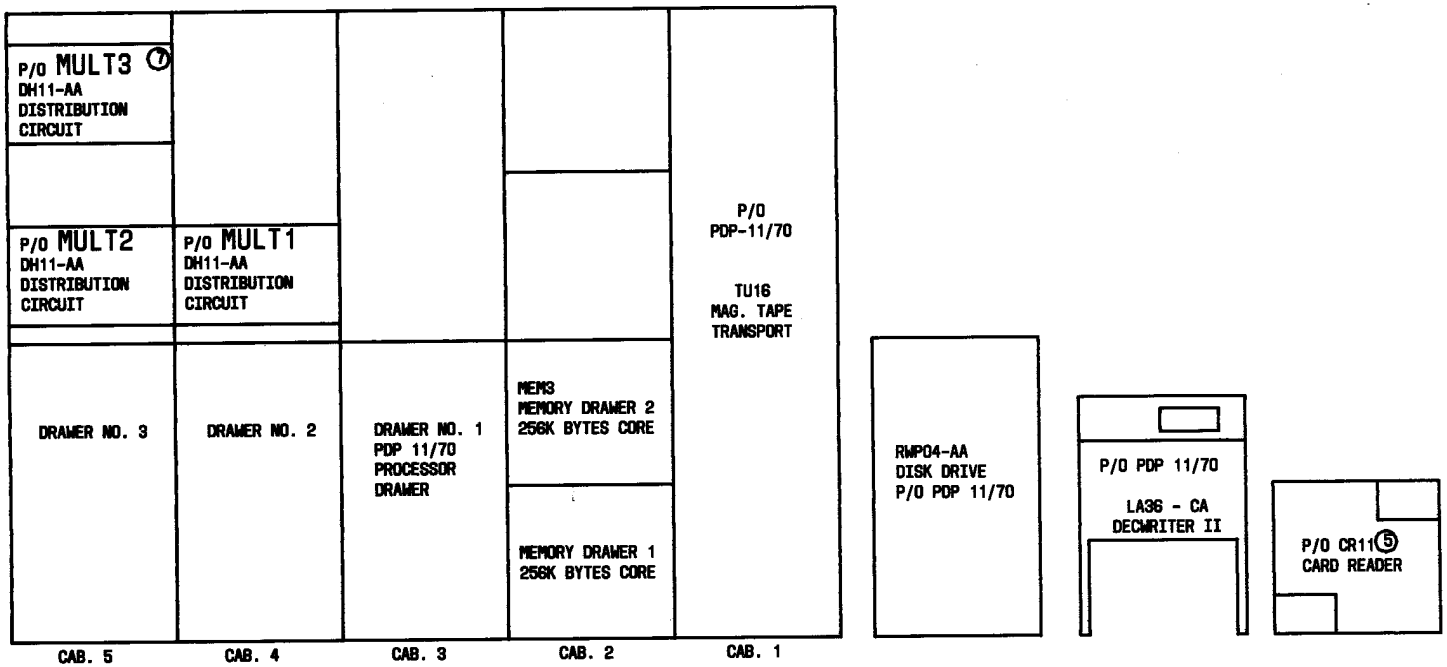


Fig. 4—Typical Equipment Layout For EADAS/NM Central Unit

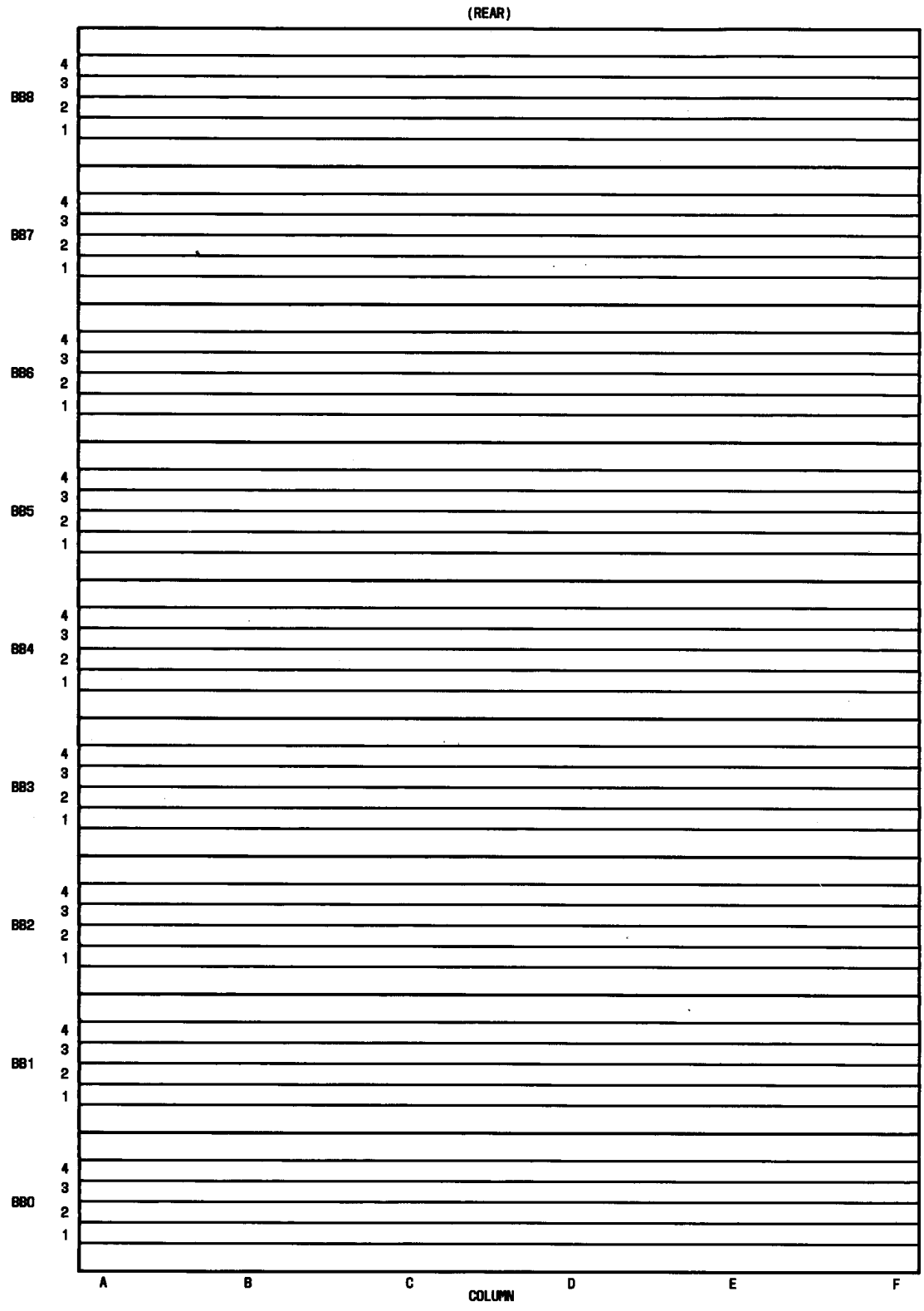


Fig. 5—Typical Equipment Drawer Nomenclature

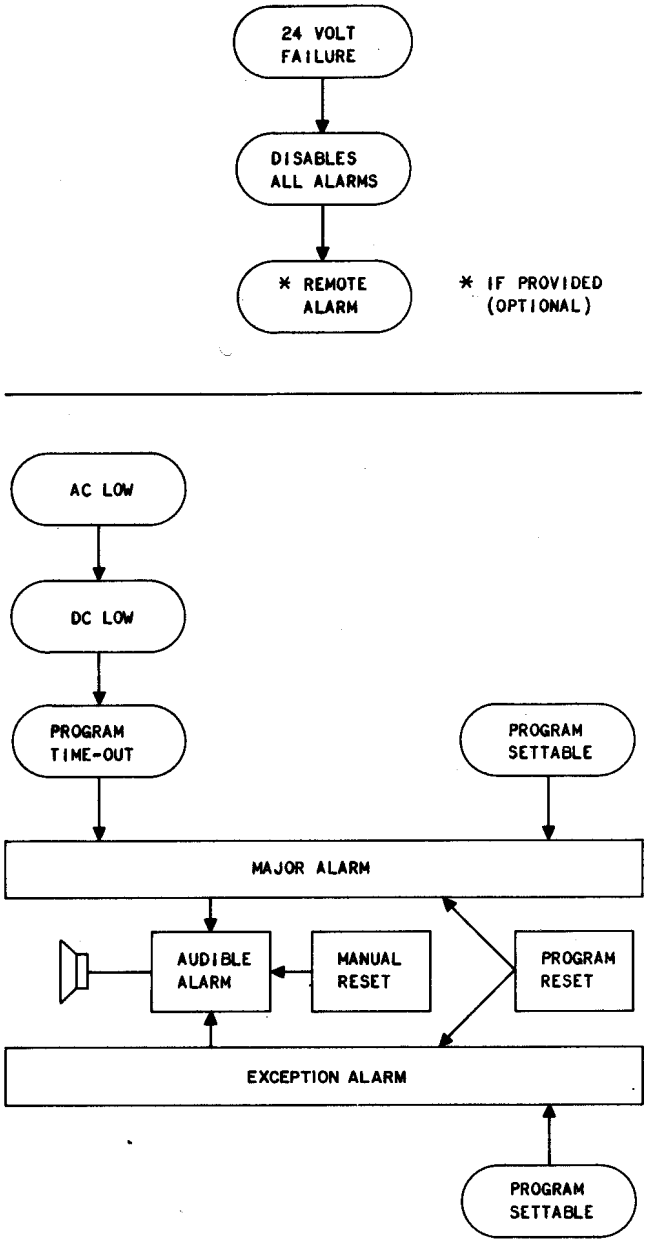


Fig. 6—Alarm Tree for Alarm Circuit

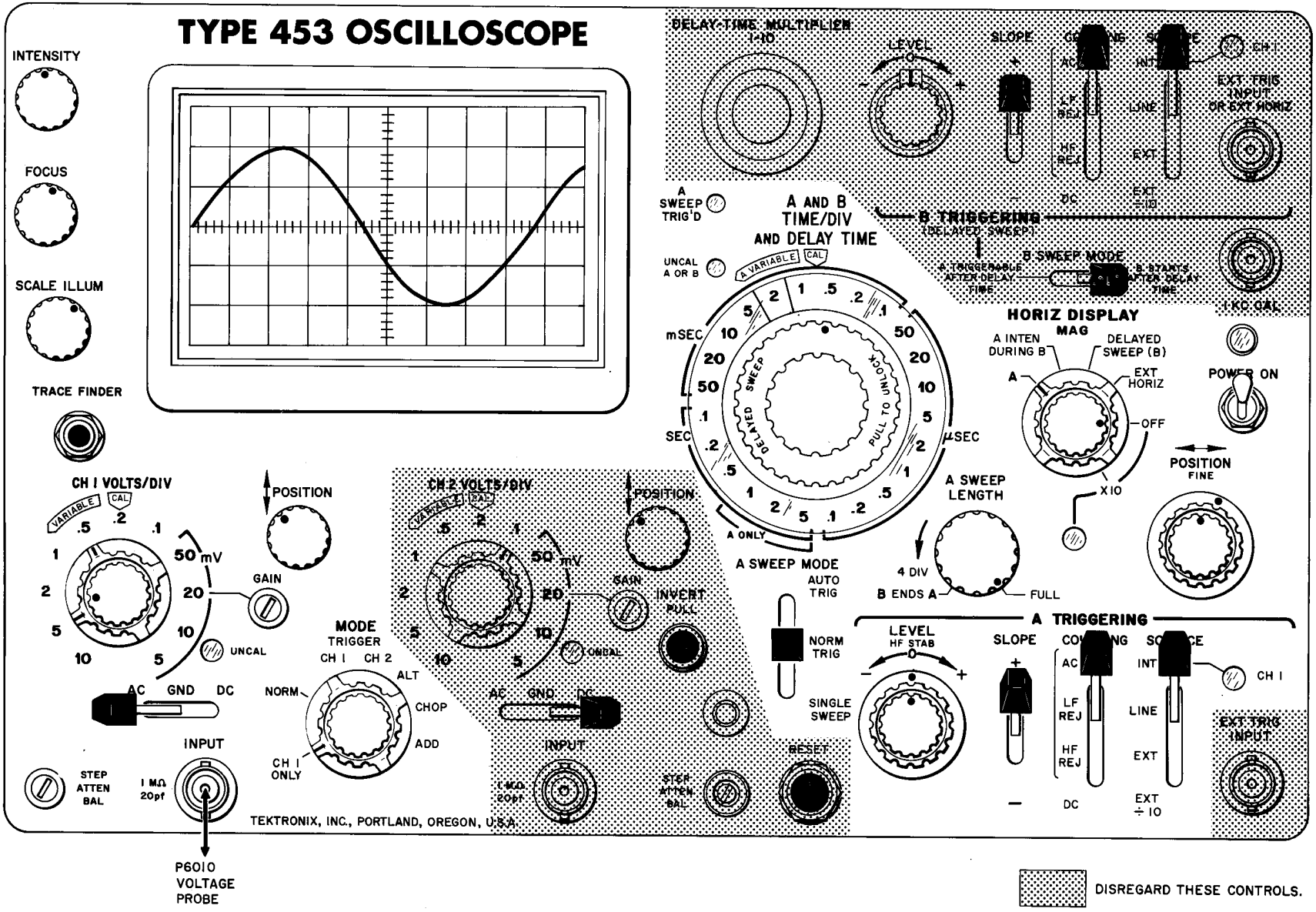
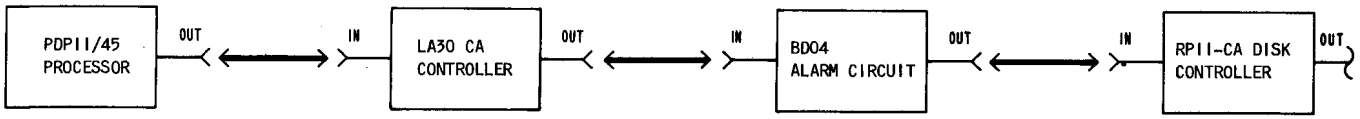
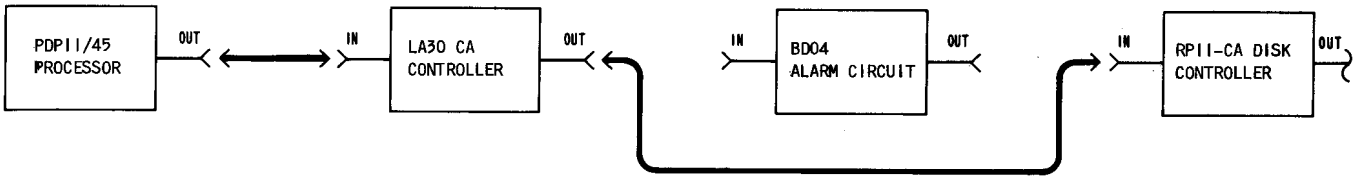


Fig. 7—Cabinet AC Check



A. EQUIPMENT CONFIGURATION BEFORE DEVICE ISOLATION



B. EQUIPMENT CONFIGURATION AFTER DEVICE ISOLATION

Fig. 8—Typical Example Showing Device Isolation From Unibus Structure

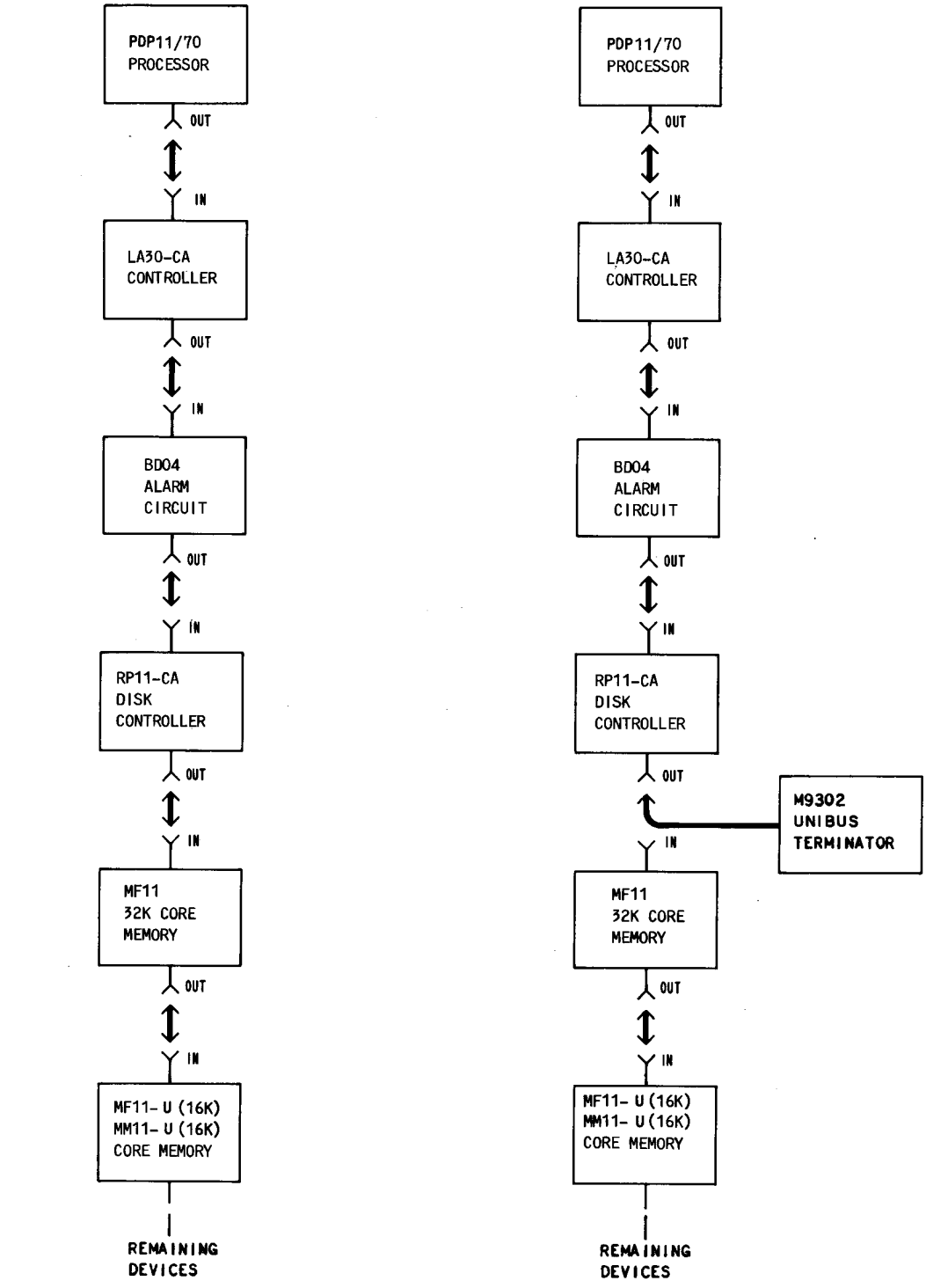


Fig. 9—Typical Example Showing Unibus Termination Method for Isolating Troubles

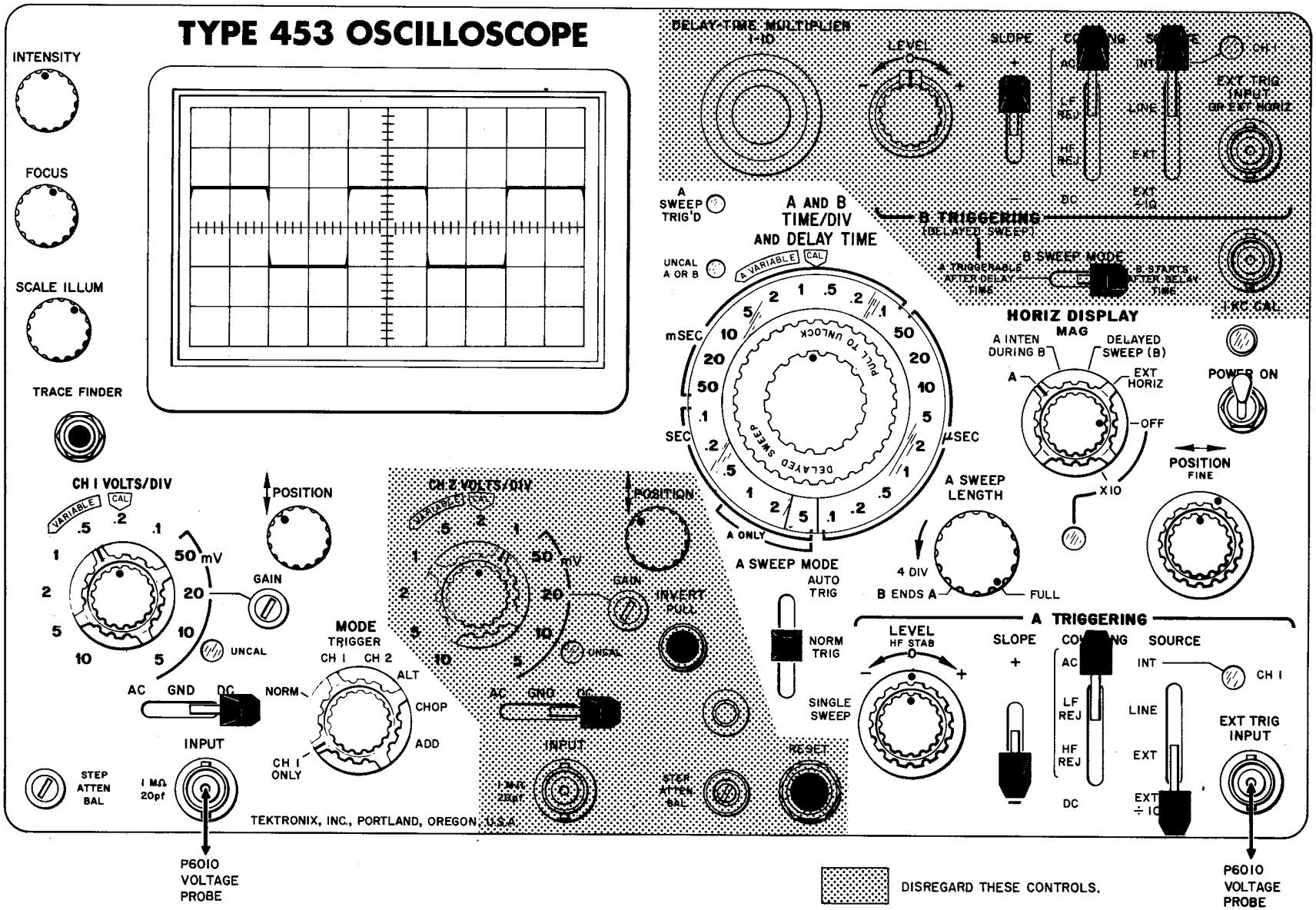


Fig. 10—Wall Board Display Check

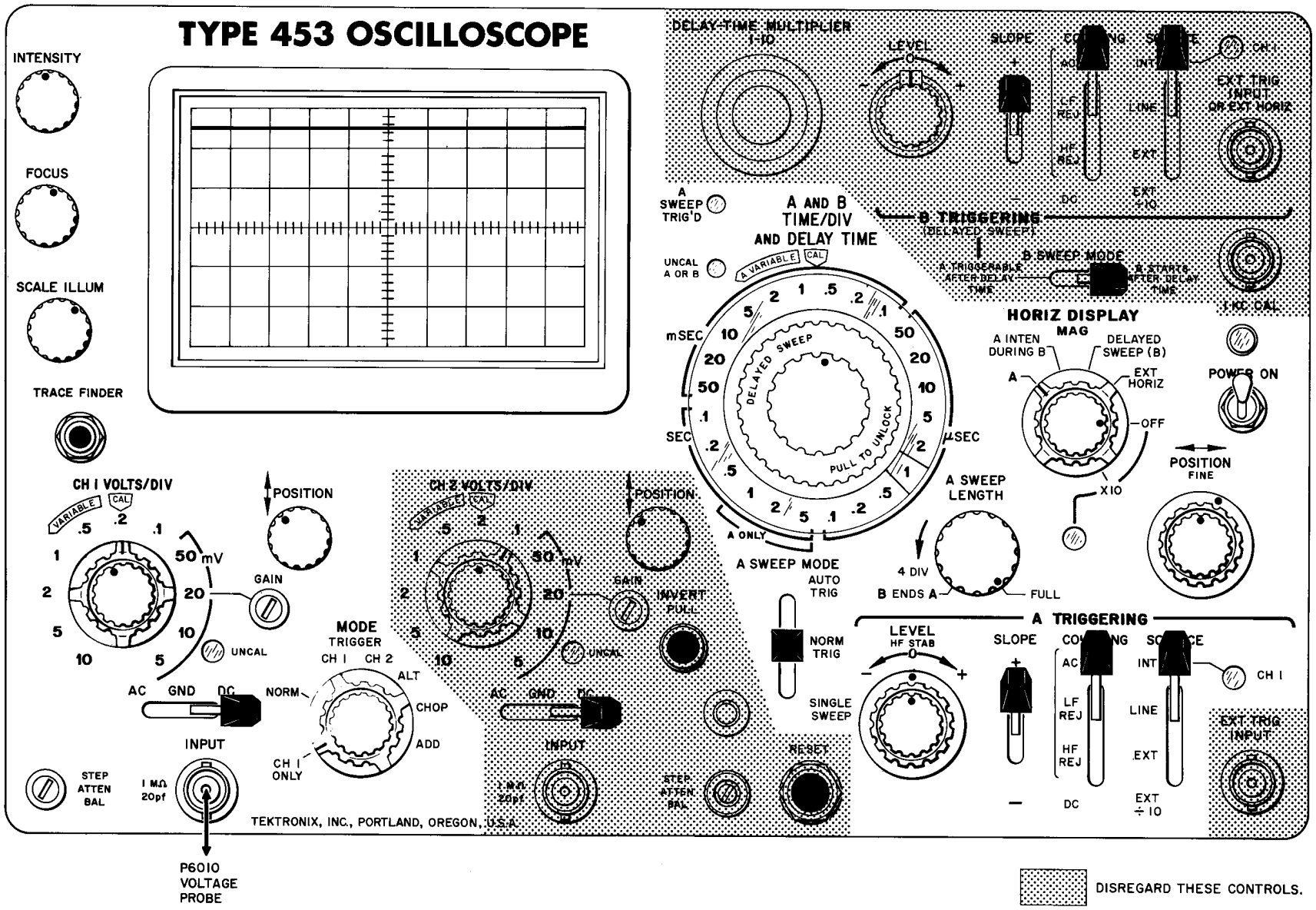


Fig. 11—5V dc Check

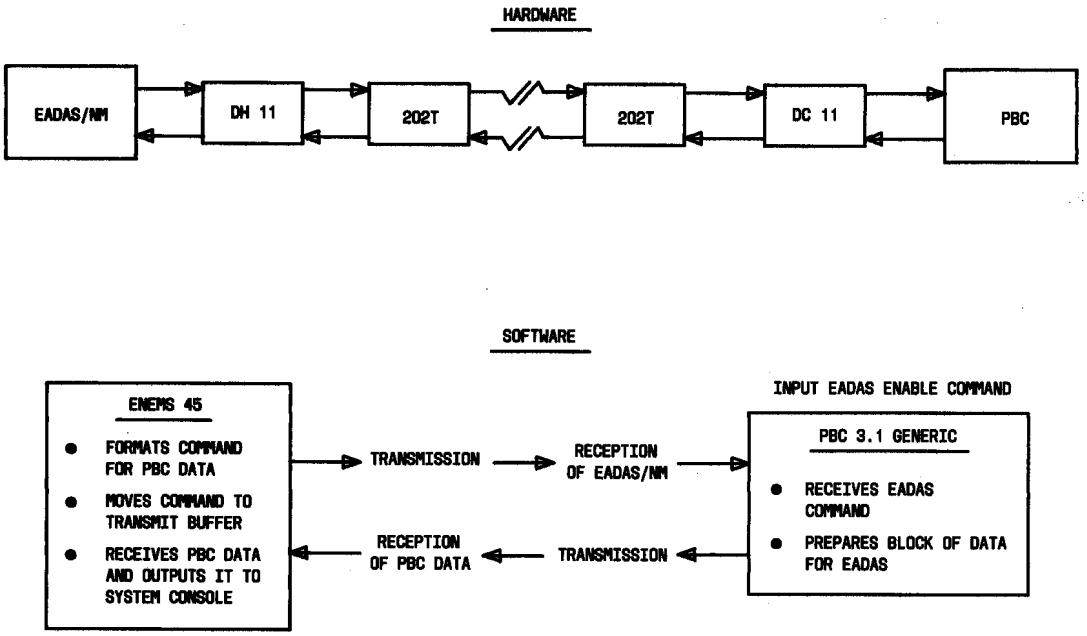


Fig. 12—Loop I Test Path

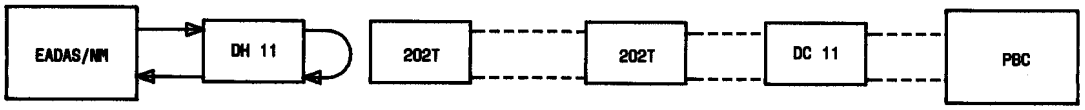


Fig. 13—Loop II Test Path Using the H315 Modem Test Connector

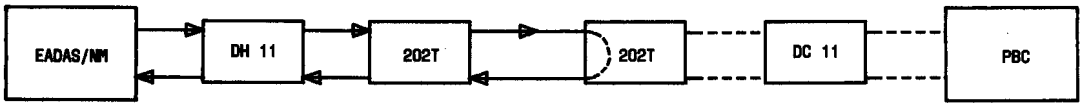
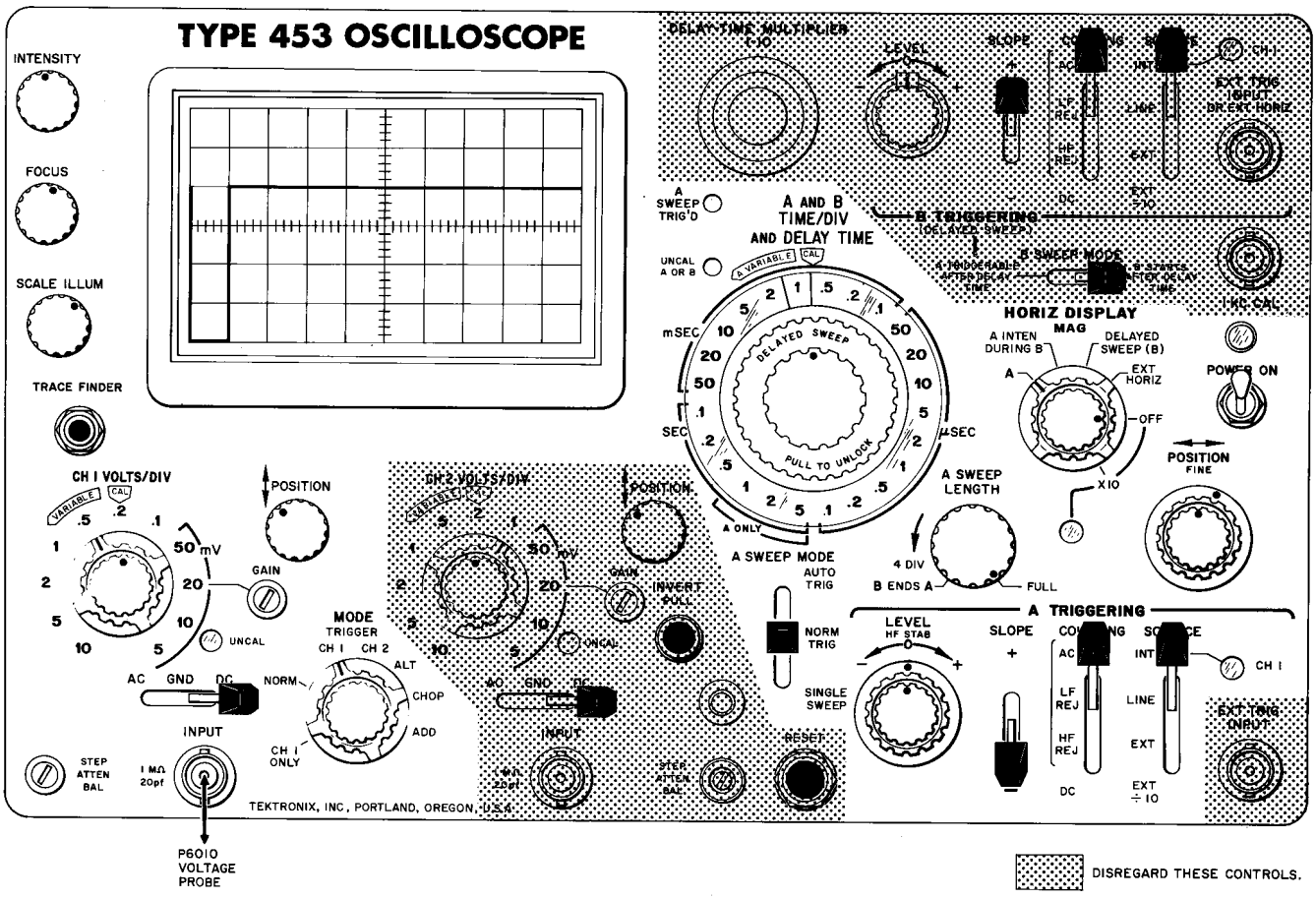


Fig. 14—Loop II Test Path Using the RT Button at the Distant End 202T Data Set



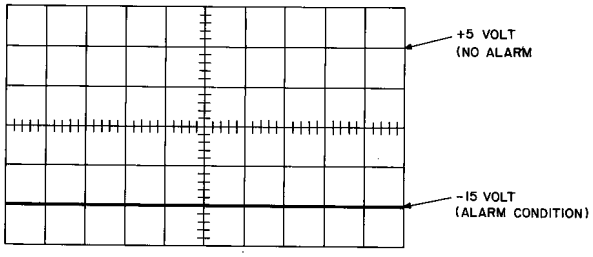


Fig. 15—Alarm Circuit Pulses