Task Oriented Practice (TOP)

1A PROCESSOR

CALL STORE/PROGRAM STORE

Developed by
The AT&T Customer Information Development and Business Translations Organization

Top Comments Hot Line
(1)-800-334-0404

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Issue 7	NOV 1993
254-251-005	TPG
TITLE PAGE	000

FIND YOUR JOB IN THE LIST BELOW	THEN GO TO
Acceptance	NTP-002
Automatic Power Monitor Test Failure, 64K Semiconductor Store J5A008A — Clear	TAP-126
Babbling Call Store/Program Store Bus — Clear	TAP-127
Circuit Pack — Semiconductor Store J5A008A or J5A010A or J5A010B — Replace	NTP-006
Demand Diagnostics — Call Store/Program Store — Perform	NTP-008
Demand Diagnostics In Slow Mode — 256K Fast Call Store/Program Store — Perform	NTP-010
Diagnostic Failure — TLP Tape Not Mounted — Clear	TAP-114
Diagnostic Failure — Using TLP Suspected Faulty Equipment List — Clear	TAP-106
Diagnostic Failure — Using Histogram 256K Semiconductor Store J5A010A or J5A010B — Clear	TAP-124
Diagnostic Failure — Using Histogram 64K Semiconductor Store J5A008A — Clear	TAP-120
Diagnostic Failure — Using Raw Data — Clear	TAP-107
Diagnostic Failure — Remove CS/PS TLP Inhibit — Clear	TAP-111
Diagnostic Failure — TLP Abort — Clear	TAP-112
Diagnostic Failure — TLP Disk Queue Full — Clear	TAP-109
Diagnostic Failure — TLP Queue Blockage — Clear	TAP-110
Diagnostic Failure — TLP Search Inhibit — Clear	TAP-115
Diagnostic Failure — TLP Tape Version X Does Not Match Version Y — Clear	TAP-113
Diagnostic Failure — TLP Tape Acquisition Error — Clear	TAP-125
Fuse Alarm — 64K Semiconductor Store J5A008A — Clear	TAP-105
Fuse Alarm — 256K Semiconductor Store J5A010A or J5A010B — Clear	TAP-123
Maintenance Philosophy	TAD-100
Manual Power Alarm — Semiconductor Store J5A008A — Test	DLP-500

FIND YOUR JOB IN THE LIST BELOW	THEN GO TO
ORED Diodes — 64K Semiconductor Store J5A008A — Check	NTP-003
ORED Diodes — 256K Semiconductor Store J5A010A — Check	NTP-007
Out-Of-Limits (OOL) Alarm — Semiconductor Store J5A008A — Clear	TAP-103
Power Switch — Semiconductor Store J5A008A or J5A010A or J5A010B — Replace	DLP-529
Power Switch Lamps — Test	DLP-501
Power Unit — Semiconductor Store J5A010A or J5A010B — Replace	NTP-005
Power Converter Alarm — Semiconductor Store J5A010A or J5A010B — Clear	TAP-121
Power Unit — Semiconductor Store J5A008A — Replace	NTP-009
Power Converter — Semiconductor Store J5A008A or J5A010A or J5A010B — Replace	NTP-004
Printout — DGN:CS/PS a PH b STF ANALY:TLPFILE: CS/PS a SUSPECTED FAULTY EQUIPMENT NOTE COLUMN CONTAINS NOTE 2	TAP-106
Printout — DGN:CS/PS a PH b STF ANALY:TLPFILE:CS/PS a NULL PACK LIST GENERATED	TAP-107
Printout — DGN:CS/PS a PH b STF ANALY:TLPFILE:CS/PS a SUMMARY DATA QUEUE ACCESS DENIED:DATA NOT RETAINED CODE 0001	TAP-109
Printout — DGN:CS/PS a PH b STF ANALY:TLPFILE:CS/PS a SUMMARY DATA QUEUE ACCESS DENIED:DATA NOT RETAINED CODE 0002	TAP-110
Printout — DGN:CS/PS a PH b STF ANALY:TLPFILE: CS/PS a SUMMARY DATA QUEUE ACCESS DENIED:DATA NOT RETAINED CODE 0004	TAP-111

FIND YOUR JOB IN THE LIST BELOW . . . . . THEN GO TO

No acceptance test procedures are required for this frame.
The readiness of this frame to become a part of the
working system was established by the successful
completion of Installation Handbook test procedures.

ACCEPTANCE

DO THE ITEMS BELOW IN THE ORDER LISTED . . . . . FOR DETAILS, GO TO

1	Test Power Control and Distribution (PCD) Frame LEDs and Disable Alarms With **PCD 0** or **PCD 1** Switches	DLP-513
2	At Store Frame 0, Unit 0 Power Switch, Rotate **ROS/OFF** Switch Clockwise to **ROS**	—
3	Wait Until **OFF NORM** and **OS** Lamps Are Lighted Before Proceeding to Item 4	—
4	On Store Unit 0, Check +**24V** ORed Diodes for Opens	DLP-506
5	At PCD Frame, Check **-48V** ORed Diodes of Store 0	DLP-508
6	At Store Unit 0 Power Switch, Rotate **ROS/OFF** Switch Counterclockwise to Normal Position	—
7	Wait Until **OFF NORM** and **OS** Lamps Are Off Before Proceeding to Item 8	—
8	At Store Unit 1 Power Switch, Rotate **ROS/OFF** Switch Clockwise to **ROS**	—
9	Wait Until **OFF NORM** and **OS** Lamps Are Lighted Before Proceeding to Item 10	—
10	On Store Unit 1, Check +**24V** ORed Diodes for Opens	DLP-506
11	At PCD Frame, Check **-48V** ORed Diodes of Store 1	DLP-508
12	At Store Unit 1 Power Switch, Rotate **ROS/OFF** Switch Counterclockwise to Normal Position	—
13	Wait Until **OFF NORM** and **OS** Lamps Are Off Before Proceeding to Item 14	—
	CAUTION: Checking for Short with Open +24V Diodes Will Degrade Service	
14	At PCD Frame, Check +**24V** ORed Diodes for Shorts in Stores 0 and 1	DLP-507
15	Repeat Items 2 Through 14 on All Equipped Call Stores and All Equipped Program Stores	—
16	At PCD Frame Bay 1 Enable Alarms	DLP-514

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	At Store Power Switch, Rotate **ROS**/**OFF** Switch Clockwise to **ROS**	—
2	When **OS** Lamp Lights, Depress **ROS**/**OFF** Switch	—
3	Replace Power Converter	DLP-509
4	At Store Power Switch, Depress **ON** Switch to Restore Power	—
5	Rotate **ROS**/**OFF** Switch Counterclockwise to Normal Position	—

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	At Store Power Switch, Rotate **ROS/OFF** Switch Clockwise to **ROS**	—
2	When **OS** Lamp Lights, Depress **ROS/OFF** Switch	—
3	Disconnect Power Unit Inputs From Semiconductor Store J5A010A or J5A010B	DLP-515
4	Remove Power Unit From Semiconductor Store J5A010A or J5A010B	DLP-512
5	Install Power Unit in Semiconductor Store J5A010A or J5A010B	DLP-510
6	Connect Power Unit Inputs to Semiconductor Store J5A010A or J5A010B	DLP-516
7	At Store Power Switch, Depress **ON** Switch	—
8	Rotate **ROS/OFF** Switch Counterclockwise to Normal Position	—

REPLACE POWER UNIT, SEMICONDUCTOR STORE J5A010A OR J5A010B

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	At Store Power Switch, Rotate **ROS**/**OFF** Switch Clockwise to **ROS**	–
2	Wait Until **OFF NORM** and **OS** Lamps Are Lighted Before Proceeding to Step 3	–
3	Replace Circuit Pack	DLP-523
4	Rotate **ROS**/**OFF** Switch Counterclockwise to Normal Position	–

REPLACE CIRCUIT PACK, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	Test Power Conversion Distribution (PCD) Frame LEDs and Disable Alarms With **PCD 0** or **PCD 1** Switches	DLP-513
2	At Store Frame 0, Call Store 0 Power Switch, Rotate **ROS/OFF** Switch Clockwise to **ROS**	—
3	Wait Until **OFF NORM** and **OS** Lamps Are Lighted Before Proceeding to Item 4	—
4	At PCD Frame, Check **-48V** ORed Diodes of Call Store 0	DLP-527
5	At Call Store 0 Power Switch, Rotate **ROS/OFF** Switch Counterclockwise to Normal Position	—
6	Wait Until **OFF NORM** and **OS** Lamps Are Off Before Proceeding to Item 7	—
7	Repeat Items 2 Through 6 on All Equipped Call Stores and All Equipped Program Stores	—
8	At PCD Frame Bay 1 Enable Alarms	DLP-514

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	At MTC Channel, Enter Message **OP:OOSUNITS!**	—
2	If Any Store Unit or Buses Are Out of Service:	
	1. Enter Message **RST:a b!** a = Unit Type (**CS**, **PS**, **CSB**, **PSB**), b = Member Number For Each Unit Out of Service	—
	2. Wait for System Response **RST:a b COMPLETED**	—
3	Perform Memory and Slave Test Semiconductor Store J5A008 or J5A010A or J5A010B	DLP-526
4	Enter Message **RST:a b!** a = Unit Type (PS or **CS**), b = Member Number to Restore Store Unit to Service	—
5	Wait for System Response, **RST:a b COMPLETED**	—

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	At Store Power Switch, Rotate **ROS/OFF** Switch Clockwise to **ROS**	—
2	When **OS** Lamp Lights, Depress **ROS/OFF** Switch	—
3	Disconnect Power Unit Inputs From Semiconductor Store J5A008A	DLP-504
4	Remove Power Unit From Semiconductor Store J5A008A	DLP-503
5	Install Power Unit in Semiconductor Store J5A008A	DLP-502
6	Connect Power Unit Inputs to Semiconductor Store J5A008A	DLP-505
7	At Store Power Switch, Depress **ON** Switch	—
8	Rotate **ROS/OFF** Switch Counterclockwise to Normal Position	—

REPLACE POWER UNIT, SEMICONDUCTOR STORE J5A008A

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	Enter **OP:CSSTATUS!** *Response:* System Responds With Printout Indicating Status of Each CS	—
2	Select CS to be Diagnosed	
3	Diagnose CS in Normal Mode (**RST:CS** a:**TLP!**)	DLP-530
4	Diagnose Demand Phases on CS (**DGN:CS** a:**PH (24-29,91):TLP!**)	DLP-540
5	Diagnose CS Using SLOW Mode (**DGN:CS** a;**SLOW:TLP!**)	DLP-531
6	Diagnose Demand Phases on CS Using SLOW Mode (**DGN:CS** a:**SLOW:PH (24-29,91):TLP!**)	DLP-541
7	Restore CS to Service (**RST:CS** a:**TLP!**); ATP Required	DLP-542
8	Repeat Steps 2 thru 7 for each CS	
9	Enter **OP:PSSTATUS!** *Response:* System Responds With Printout Indicating Status of Each PS	—
10	Select PS to be Diagnosed	
11	Diagnose PS in Normal Mode (**RST:PS** a:**TLP!**)	DLP-530
12	Diagnose Demand Phase on PS (**DGN:PS** a:**PH (24-29,91):TLP!**)	DLP-540
13	Diagnose PS Using SLOW Mode (**DGN:PS** a;**SLOW:TLP!**)	DLP-531
14	Diagnose Demand Phases on PS Using SLOW Mode (**DGN:PS** a:**SLOW:PH (24-29,91):TLP!**)	DLP-541
15	Restore PS to Service (**RST:CS** a:**TLP!**); ATP Required	DLP-542
16	Repeat Steps 10 thru 15 for each PS	

GENERAL

The maintenance philosophy contained in this volume is based upon the design of equipment (hardware), diagnostic software and test equipment employed. Procedures are intended to aid personnel to perform trouble-clearing tasks. The degree to which these procedures accomplish this depends upon input and feedback from the user. Additions, corrections, and improvements to the data are encouraged. Manufacturer, engineering and software documentation, such as I/O Manuals, SDs, PRs, etc, which are available to the operating telephone company offices, are referred to where applicable rather than duplicating that information in the TOP. Some portions of those documents may be utilized in procedures but only as examples for purpose of explanation. Test equipment (oscilloscopes, voltmeters, etc) and the parameters involved in the circuits being tested, adjusted, or checked are usually prescribed. Setup and method of use is not described unless it is unusual or unique.

IXL PHILOSOPHY

The IXL is structured to provide fast access to those procedures pertinent to symptoms identified. Procedures unique to a particular modification of frame are identified by that frame's J number. If not so identified, the procedure would apply to all modifications.

Power problems are sensed by scan points which generate an alarm. It is assumed that the user following the aisle pilot lights can locate the frame with the power fault which was automatically powered down (1A power switch with **PWR OFF** lamp lighted and **OFF NORM** lamp off) or by reading the REPT:PA printout which would identify the frame with power fault. The precise structure of the message is given in the input/output (I/O) message manuals. Symptoms described in the IXL reflect the preceding assumptions, and indicate other conditions that are observable at the frame that would enable the user to access the proper trouble-clearing procedure. These conditions are fuse blown, lighted LEDs on converters or power function circuit packs.

In general, logic circuit failures cause the fault recovery program to request a diagnostic program. This method of requesting the diagnostic program includes the TLP option. The IXL reflects this in the printouts listed. Outside of the first two supplementary messages (ANALY:TLPFILE:), all other supplementary messages pertain to problems in generating a SUSPECTED FAULTY EQUIPMENT list and reference to procedures (TAPs) which attempt to correct the problem. If successful in generating a SUSPECTED FAULTY EQUIPMENT list, those procedures reference to the appropriate procedure [TAP-106] which tells you what to do with this list. If not successful, they reference to the next level of trouble clearing, raw data analysis [TAP-107] which is an alternative to the first and most common trouble-clearing approach.

TAP PHILOSOPHY

When documenting a procedural approach to trouble clearing, certain assumptions are made. It is assumed that one fault is being cleared at a time. When directing the user to perform an action, it is assumed that he performs that action correctly. Similarly, when directed to make replacements, the replacement part is always assumed to be good. Equipment used for testing both built-in (hardware and software) and commercial,

are assumed to be good. Only consistent fault signatures are covered.

Trouble-clearing TAPs provided for diagnostic failures are provided on three levels. Level one is [TAP-106] addressed to what to do with a software generated TLP SUSPECTED FAULTY EQUIPMENT list and provides a step-by-step procedure for replacing circuit packs one at a time, and analyzing the results. This level is straightforward and requires some familiarity with the equipment (descriptive and theory practices), maintenance channel techiques, and with diagnostic printouts.

Second level of trouble clearing is accessed from the first level TAP when TLP-generated SUSPECTED FAULTY EQUIPMENT list has been exhausted without clearing the problem or it can be accessed directly from the IXL or any of the ANALY:TLPFILE: TAPs which produce a NULL PACK TEST GENERATED RESPONSE. THIS LEVEL [TAP-107] is known as raw data analysis and describes what to do with the summary and supplemental data printed out either with or instead of the SUSPECTED FAULTY EQUIPMENT list. It is expected that this leads to an identification of faulty circuits within the SD and possibly additional suspect circuit packs not previously identified. This level of trouble clearing is more complex and requires knowledge of equipment, of maintenance channel techniques and printouts, and of SDs, PRs, etc.

Third level of trouble clearing is signal tracing using interactive diagnostics [TAP-108]. This procedure is accessible only from the previous level [TAP-107] and uses information derived in the performance of that procedure. This level of trouble clearing requires an increase in the capabilities cited in the first two levels but with additional knowledge and skill in the setup and use of test equipment (oscilloscopes, voltmeters, etc).

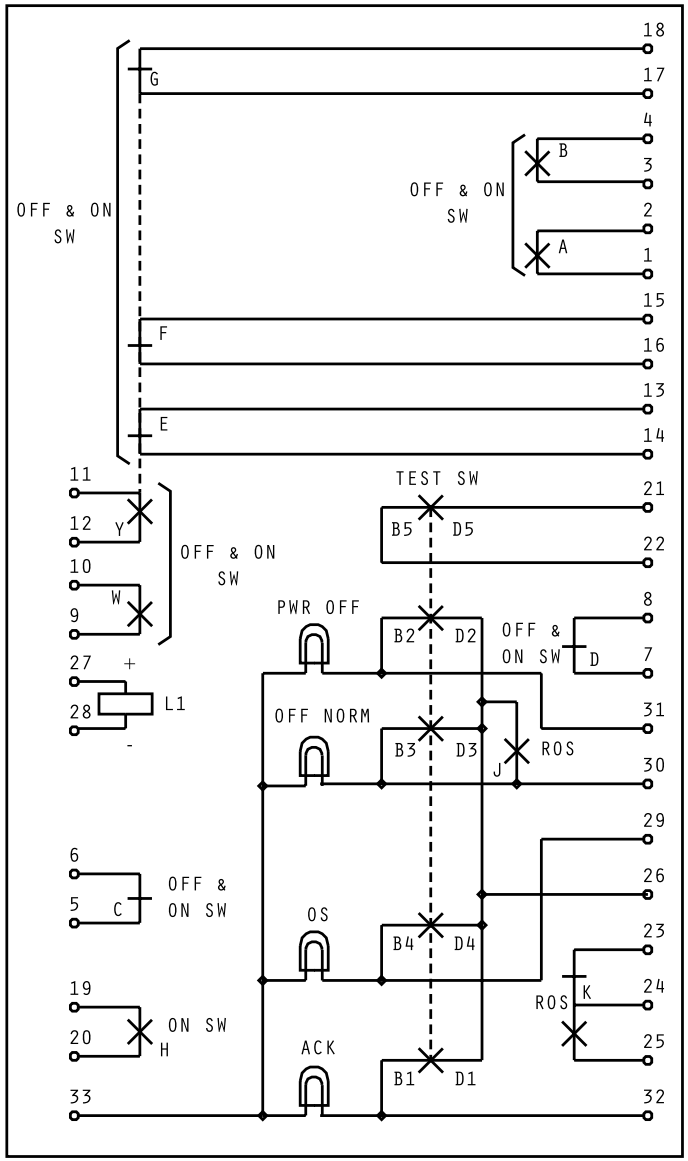
ALTERNATE METHODS

The more knowledgeable and experienced personnel may access the TOP documents at a point in trouble clearing where analyzation is completed (faulty component determined) and only repair or replacement required. Most DLPs are built to support TAPs and NTPs with preconditioning and system restoration steps covered in those level procedures (TAPs, NTPs). Therefore, access to data (DLPs) on a hunt-and-find basis is a threat to equipment operation and may compound trouble-clearing problems.

Another method of trouble clearing that may be utilized is interrupt analysis. Interrupt analysis contained in Volume AT&T 254-251-003 may produce a list of circuit packs that could cause that interrupt. Prior to changing the circuit packs, a DGN should be run with ATP expected, if DGN produces:

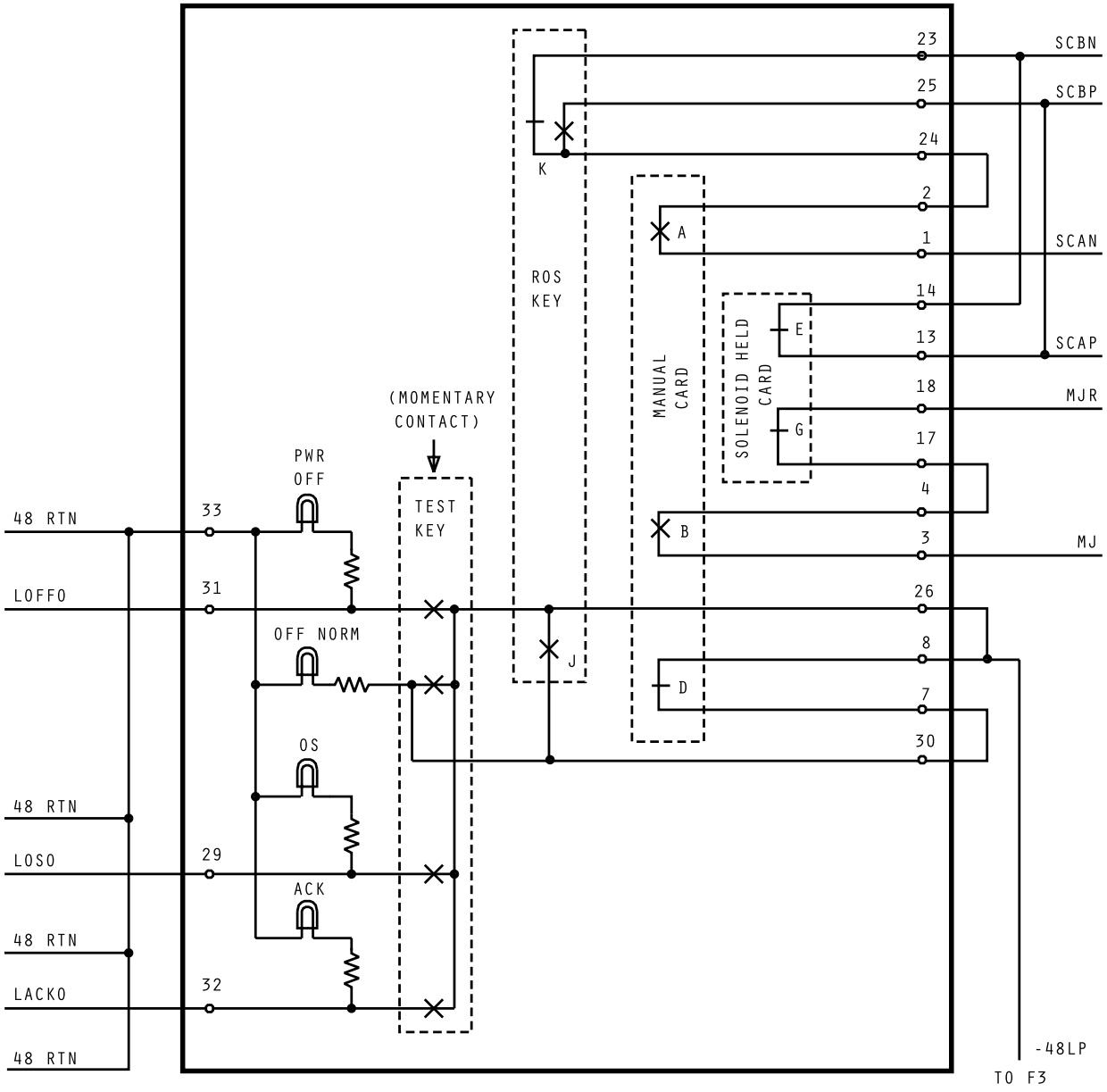
(1) ATP — First circuit packs found in interrupt analysis should be changed. Should this be the wrong circuit pack, probability is high that interrupt will occur again with same symptom. Next identified pack should be changed at this time.

(2) STF — The most suspect circuit pack is the pack that appears on both TLP pack list and list generated from analysis of interrupt.



POWER SWITCH (KS-20738)

Issue 7	NOV 1993
254-251-005	TAD
PAGE 1 of 1	101



POWER SWITCH (KS-20738, L6)

Issue 7	NOV 1993
254-251-005	TAD
PAGE 1 of 1	102

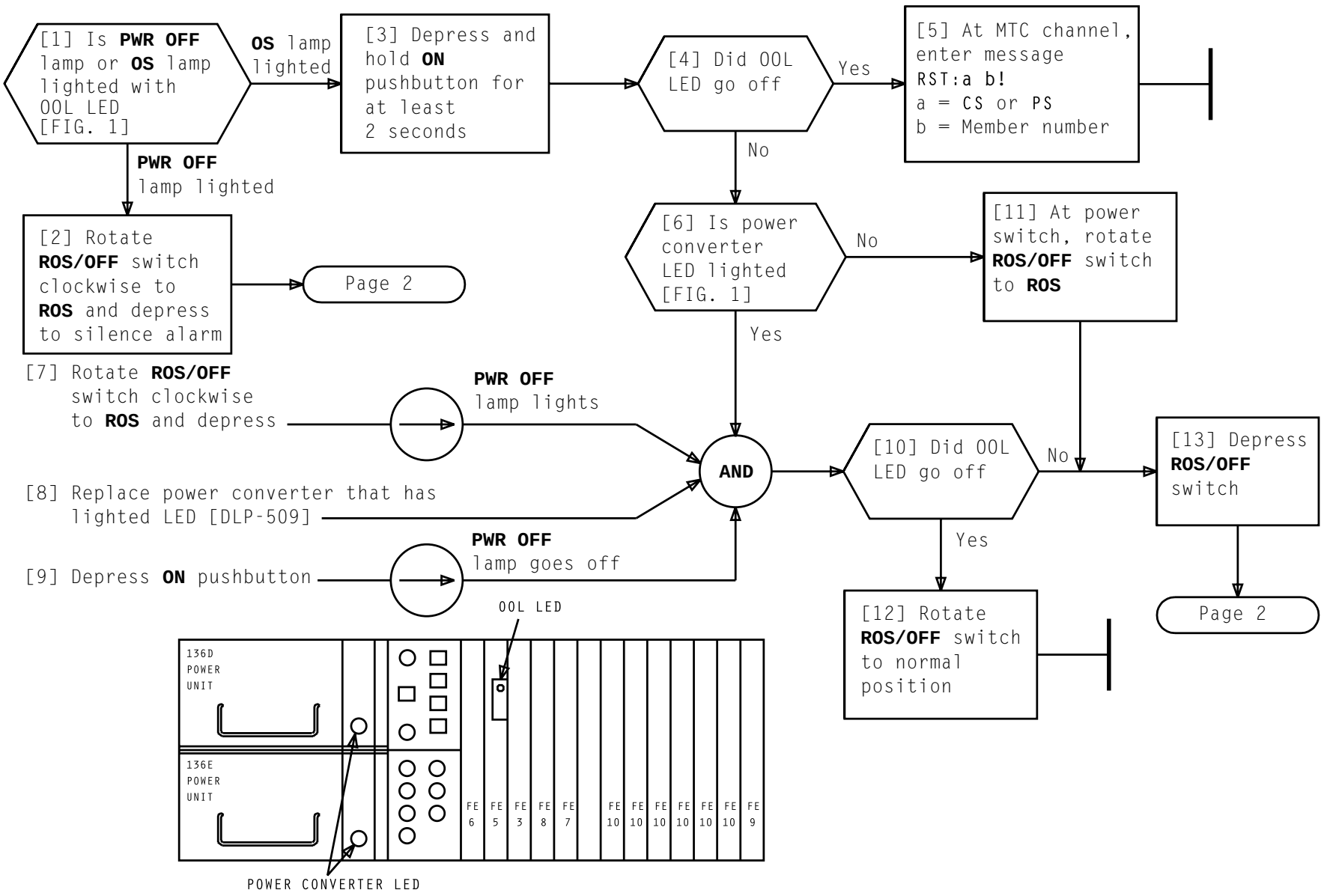
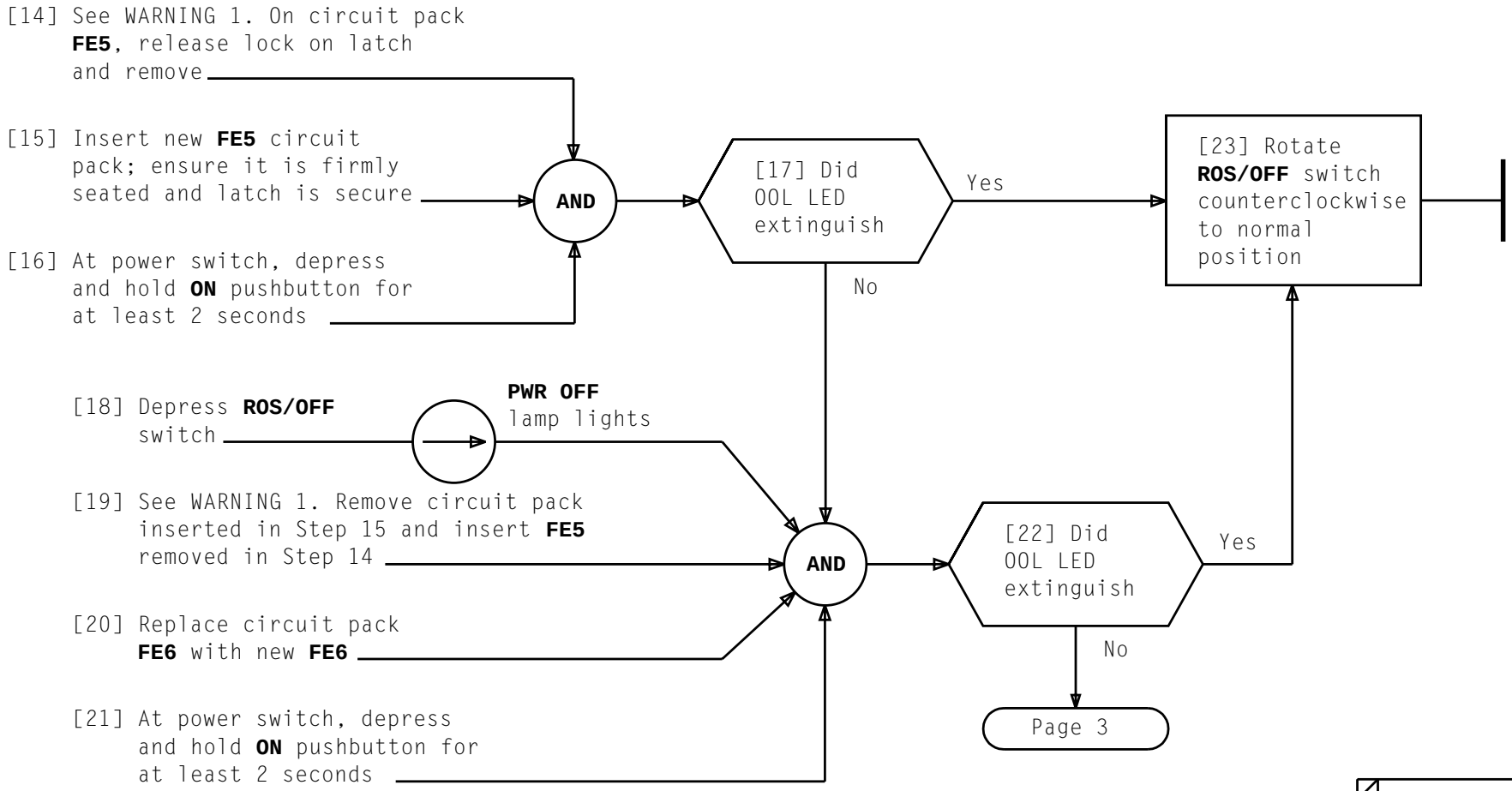


FIG. 1 — Front View, Semiconductor Store

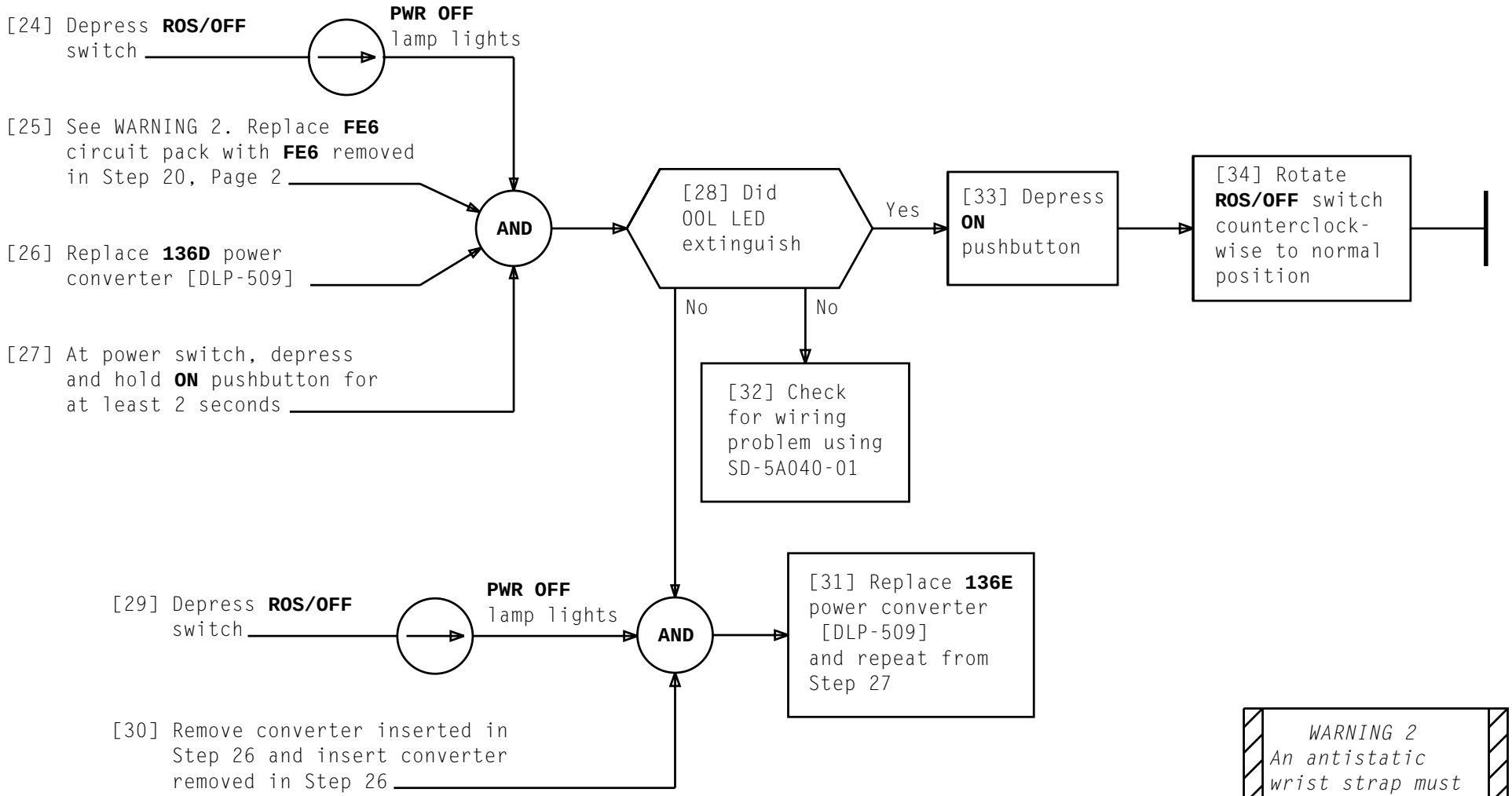
CLEAR OUT OF LIMITS (OOL) ALARM, SEMICONDUCTOR STORE J5A008A



WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

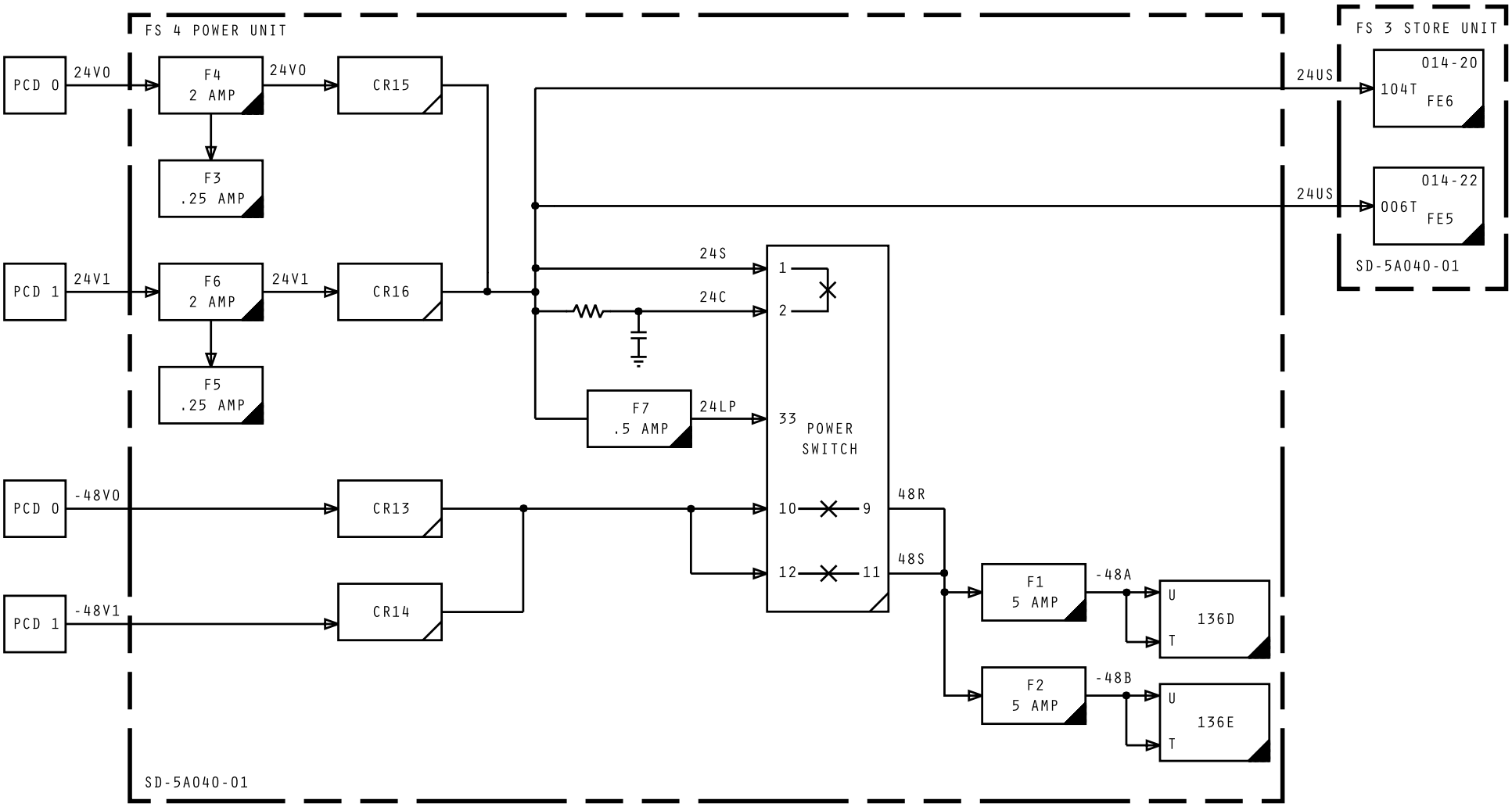
Issue 7	**NOV 1993**
254-251-005	**TAP**
PAGE 2 of 3	**103**

CLEAR OUT OF LIMITS (OOL) ALARM, SEMICONDUCTOR STORE J5A008A



WARNING 2
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR OUT OF LIMITS (OOL) ALARM, SEMICONDUCTOR STORE J5A008A



POWER ISOLATION DIAGRAM FOR 24V AND 48V FUSING, SEMICONDUCTOR STORE J5A008A

Issue 7	NOV 1993
254-251-005	ISD
PAGE 1 of 1	104

[1] Locate store with blown fuse and **PWR OFF** lamp lighted

[2] At store power switch, rotate **ROS/OFF** switch clockwise to **ROS** and depress

[3] See FIG. 1, TABLE A, and NOTES 1 and 2. Replace blown fuses

[4] Depress **ON** pushbutton

AND

[5] Did fuses blow

Yes → [7] Depress **ROS/OFF** switch → Page 2

No → [6] Rotate **ROS/OFF** switch counterclockwise to normal position

TABLE A		
FUSE	**AMPS**	**TYPE**
F1	5A	70
F2	5A	70
F3	1/4A	70
F4	2A	GBB/74
F5	1/4A	70
F6	2A	GBB/74
F7	1/2A	70

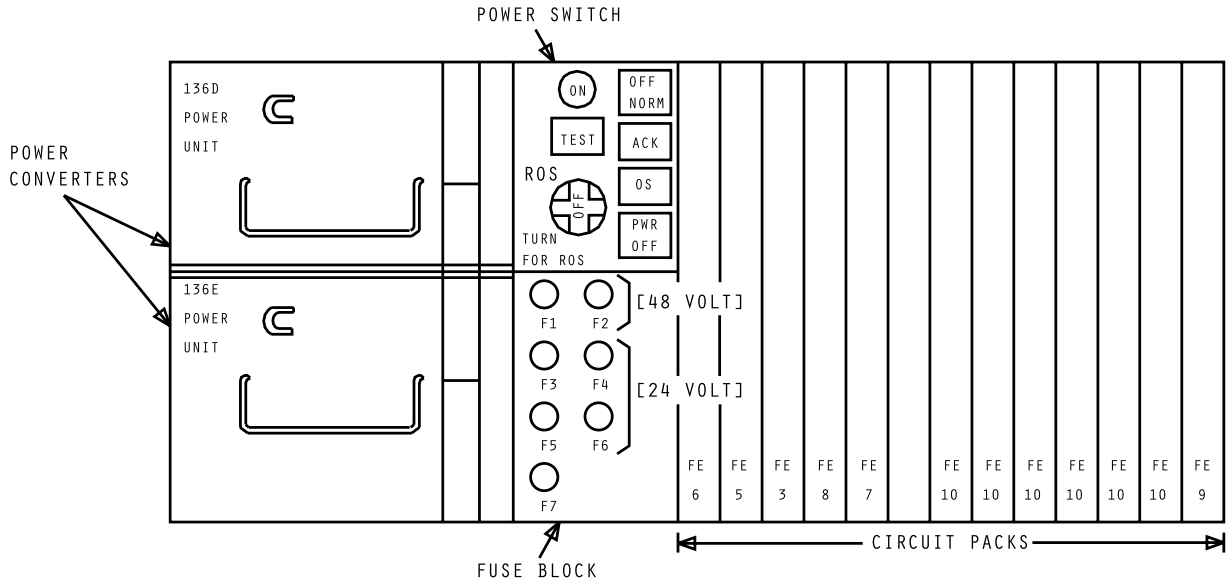
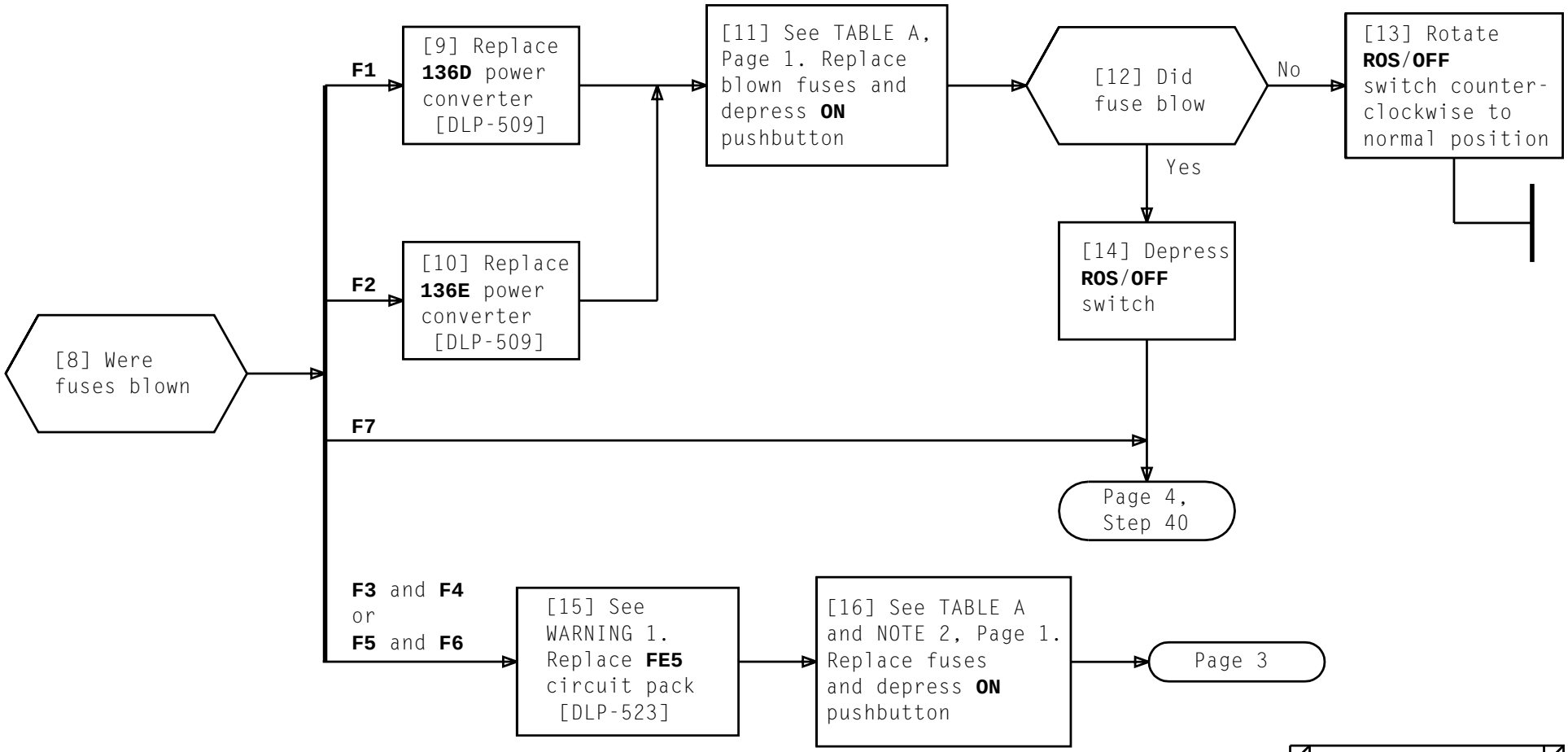


FIG. 1 — Front View, Semiconductor Store

NOTES

1. If fuse **F3** blows, fuse **F4** blows. If fuse **F5** blows, fuse **F6** blows
2. When replacing fuses **F4** and **F6**, indicator fuse (**F3** or **F5**) should be removed first and replaced last

CLEAR FUSE ALARM, SEMICONDUCTOR STORE J5A008A



WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR FUSE ALARM, SEMICONDUCTOR STORE J5A008A

[17] Did fuses blow

No

[23] Rotate **ROS/OFF** switch counterclockwise to normal position

Yes

[18] Depress **ROS/OFF** switch

[19] See WARNING 2. Replace **FE5** with circuit pack removed in Step 15, Page 2 [DLP-523]

[20] See WARNING 2. Replace **FE6** circuit pack [DLP-523]

[21] See TABLE A, Page 1, and NOTE 2, Page 1. Replace fuses and depress **ON** pushbutton

AND

No

[22] Did fuses blow

Yes

[24] Depress **ROS/OFF** switch

[25] See WARNING 2. Replace **FE6** with circuit pack removed in Step 20 [DLP-523]

[26] See FIG. 2. At store backplane, using a 793A tool, remove the three paddleboard connectors coming from power unit

AND

Page 4

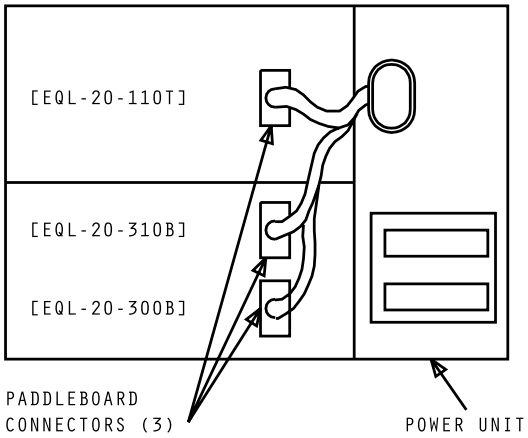
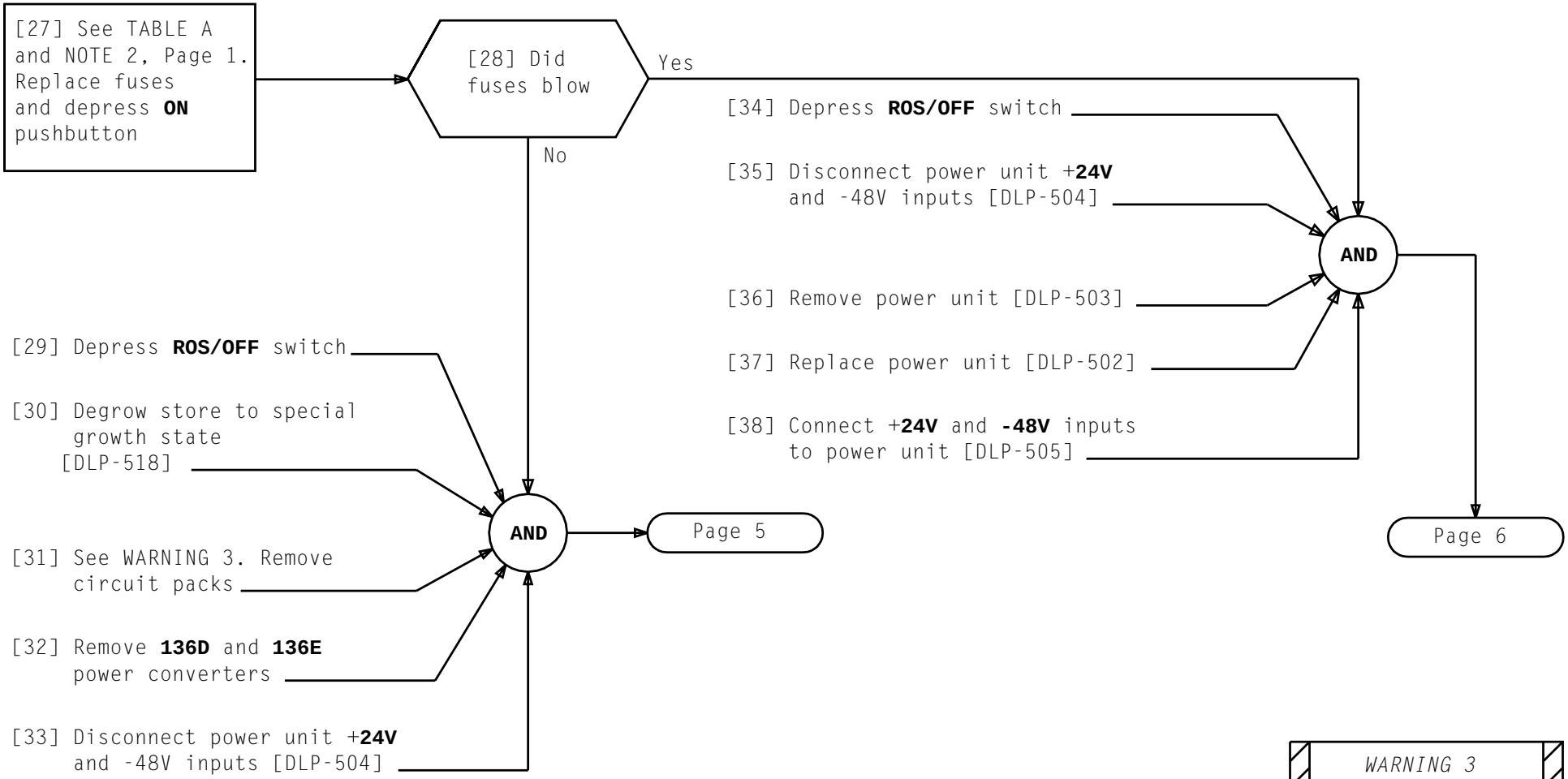


FIG. 2 – Rear View of Store Unit

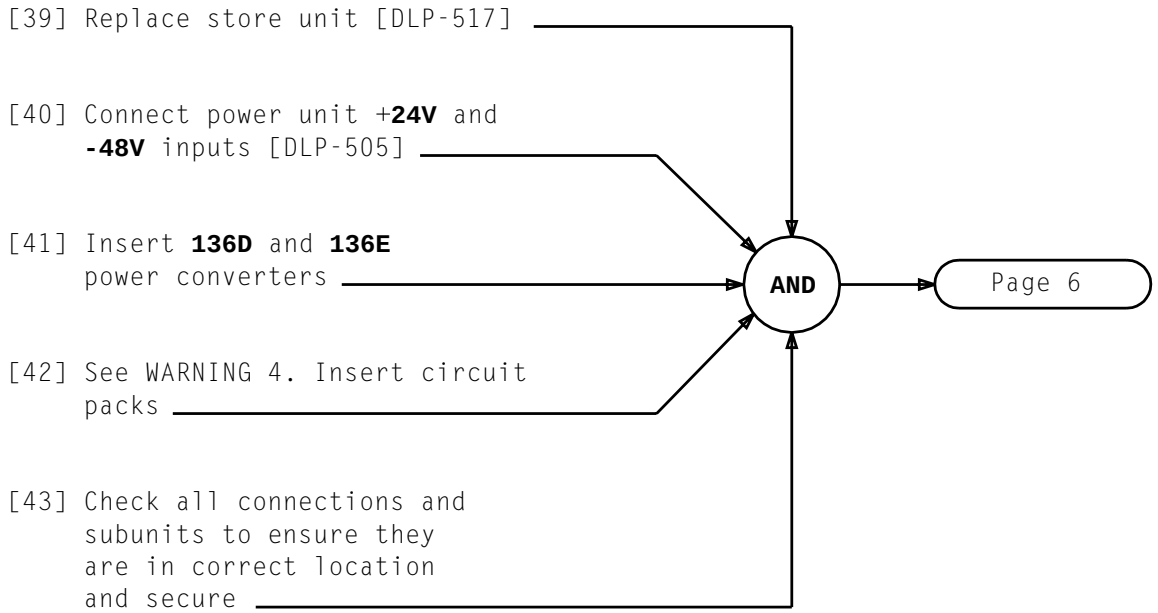
WARNING 2
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR FUSE ALARM, SEMICONDUCTOR STORE J5A008A



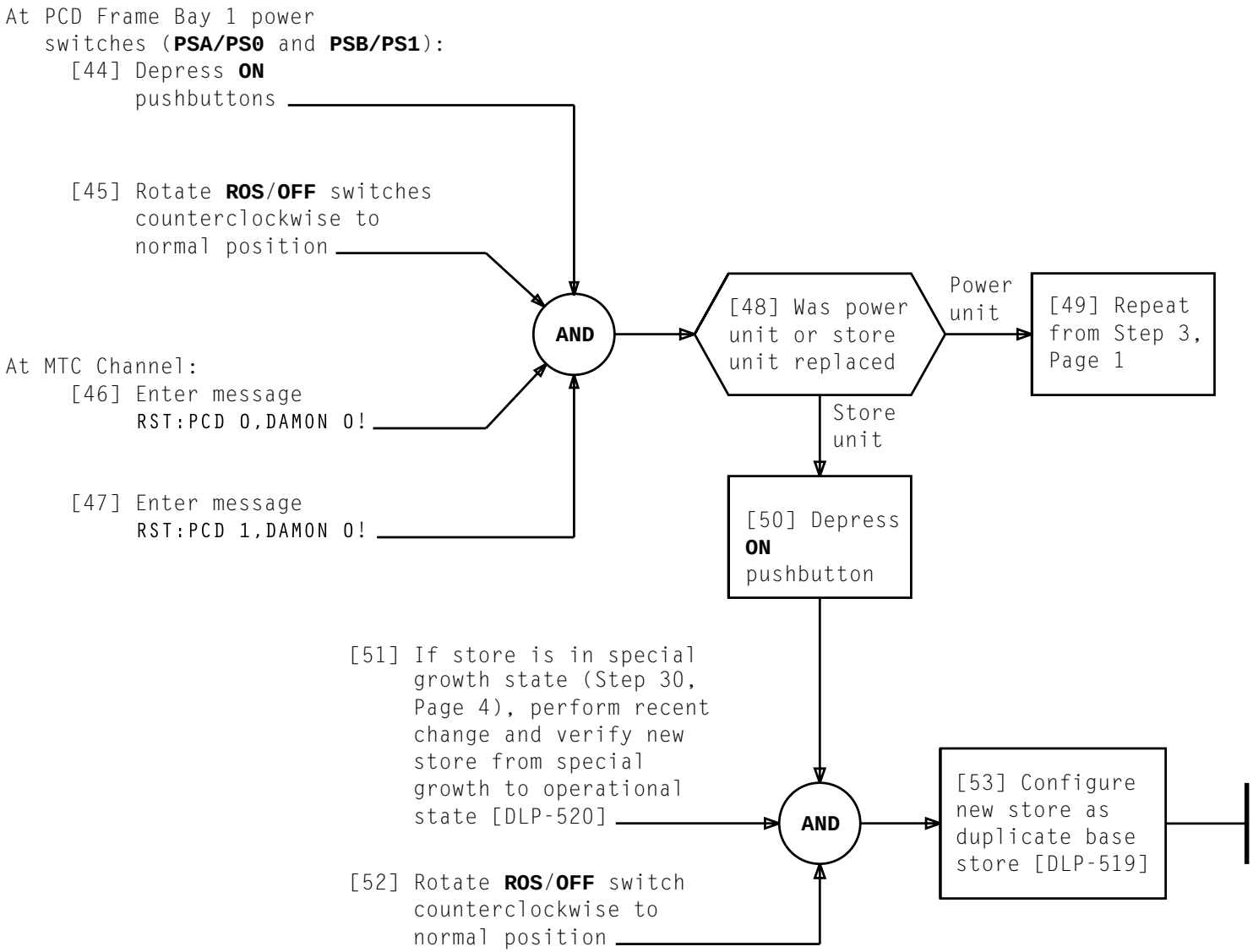
WARNING 3
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR FUSE ALARM, SEMICONDUCTOR STORE J5A008A

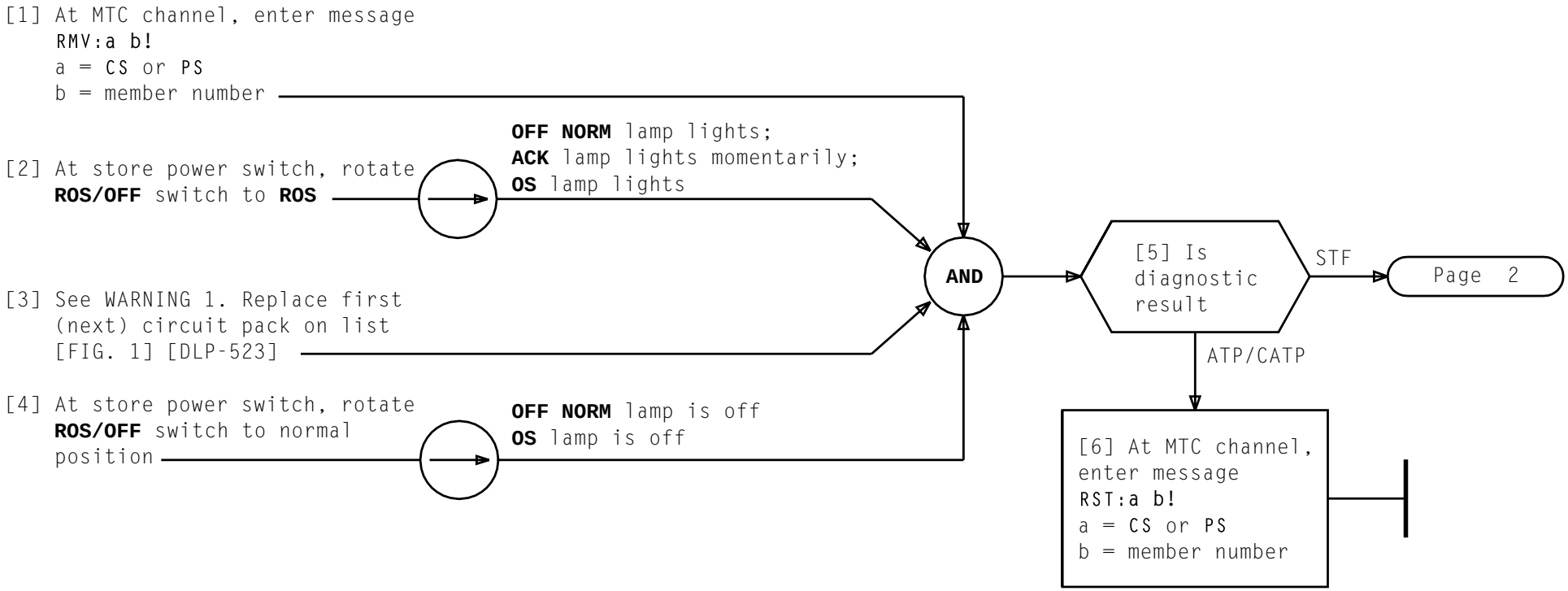


WARNING 4
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR FUSE ALARM, SEMICONDUCTOR STORE J5A008A



CLEAR FUSE ALARM, SEMICONDUCTOR STORE J5A008A



M10 ANALY:TLPFILE: PS 1 SUSPECTED FAULTY EQUIPMENT MSG IP

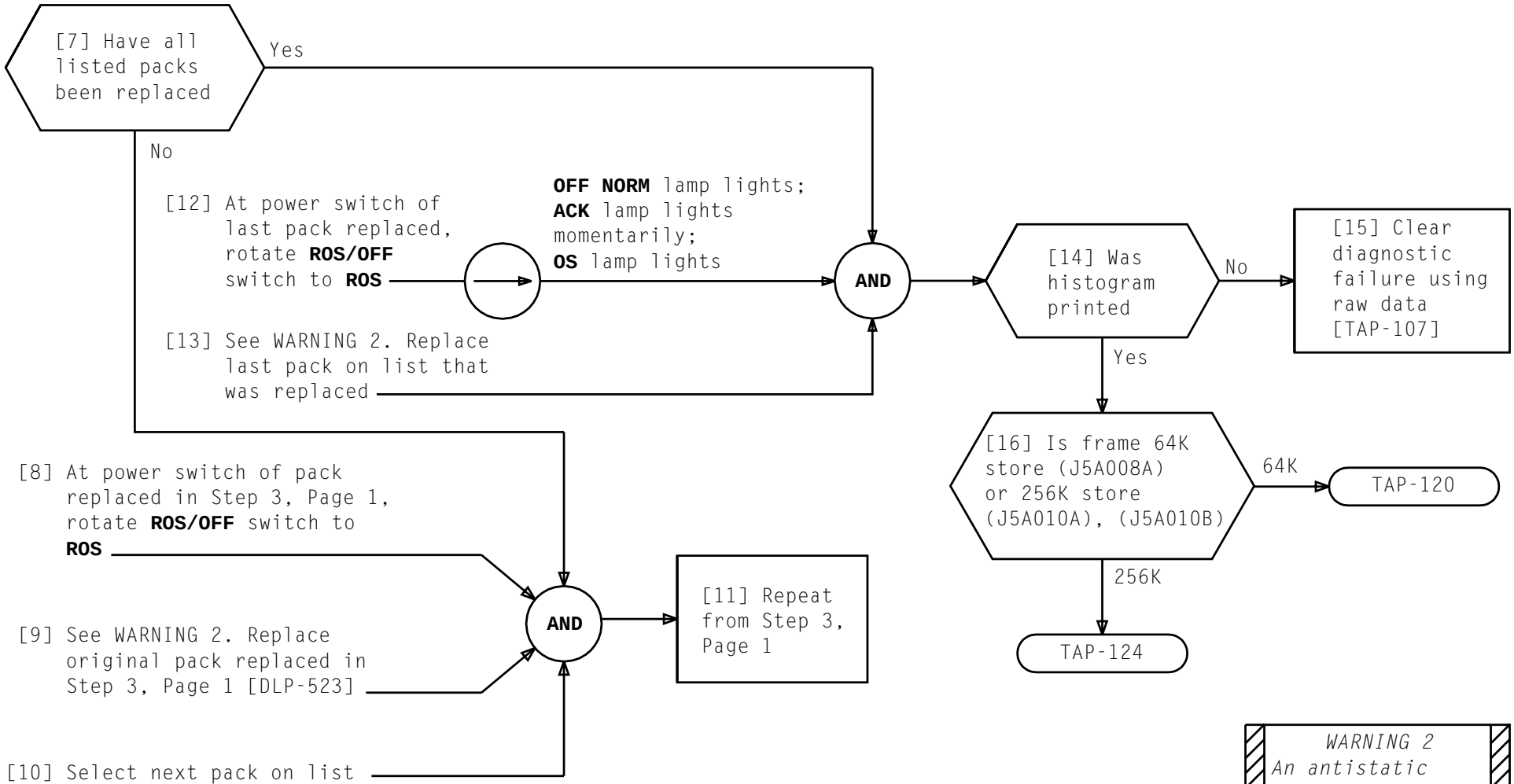
TLPFILE 1412 MFNUM 25377 ENTRY TIME 12/14/90 13:09:19

	EQPT LOC	CODE	NOTE WT	FS	SYM	SD	HELPER ID
FIRST CIRCUIT PACK →	011-22	FE0063	8	1	2	5A053	
	011-16	FE0062	8	1	1	5A053	
	011-20	FE0065	8	1	4	5A053	
	011-18	FE0064	8	1	3	5A053	
	011-07	FE0066	7	2	4	5A053	
	011-13	FE0067	7	2	7	5A053	

FIG. 1 - Sample Suspected Faulty Equipment List Printout

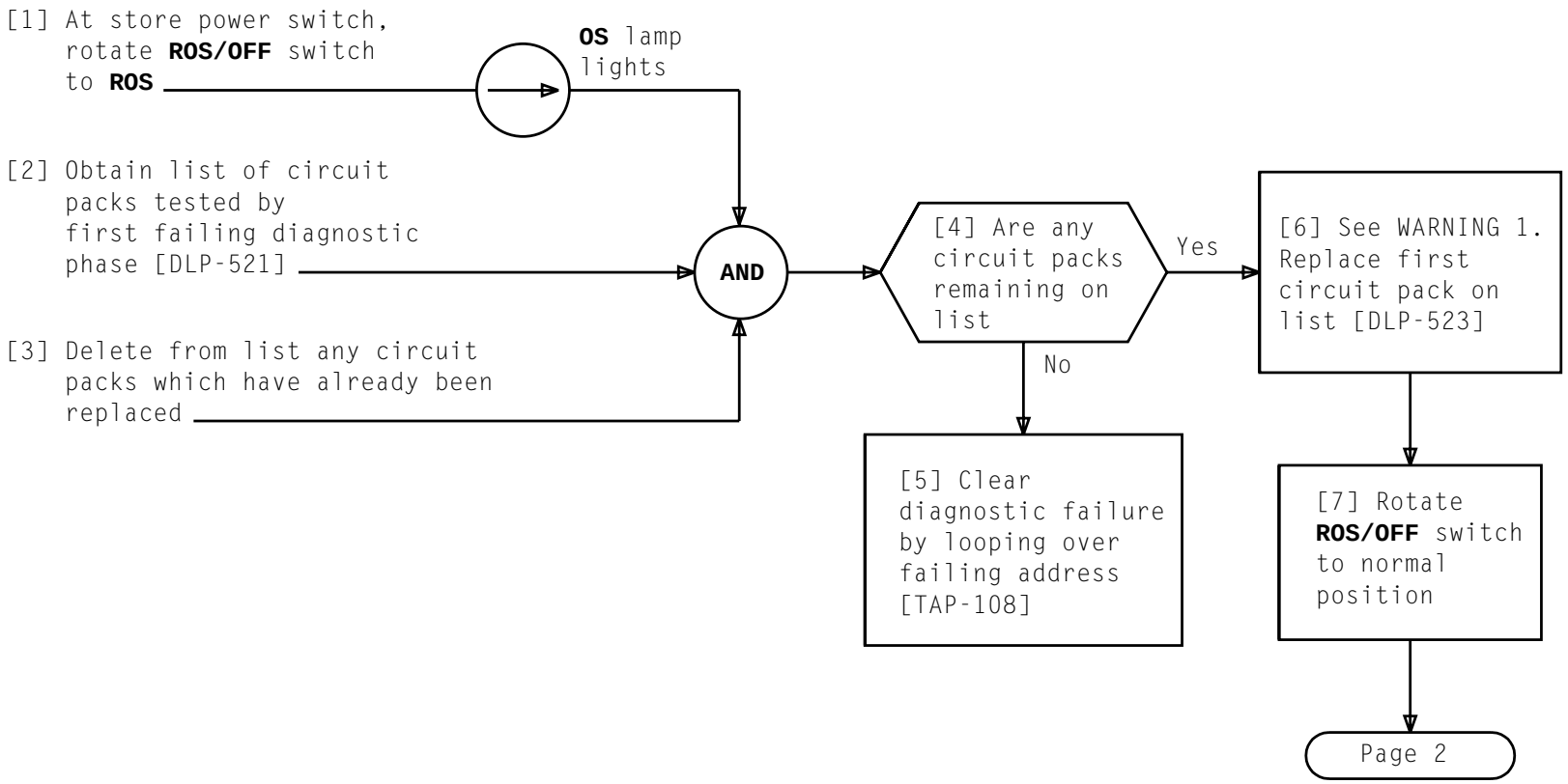
WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR DIAGNOSTIC FAILURE BY REPLACING PACKS ON TLP SUSPECT EQUIPMENT LIST



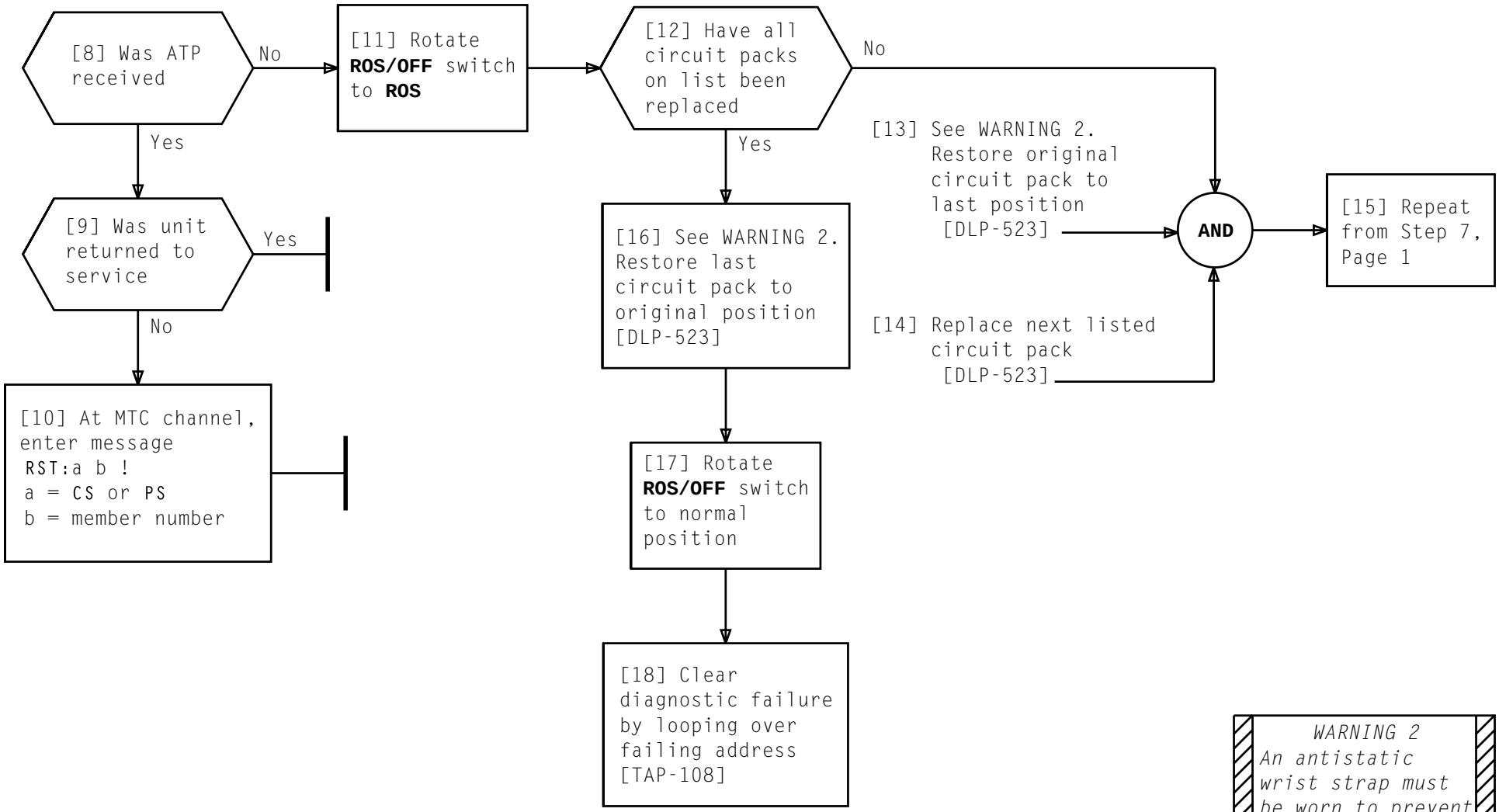
WARNING 2
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR DIAGNOSTIC FAILURE BY REPLACING PACKS ON TLP SUSPECT EQUIPMENT LIST



WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR DIAGNOSTIC FAILURE USING RAW DATA



WARNING 2
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR DIAGNOSTIC FAILURE USING RAW DATA

[1] Obtain and power up oscilloscope allowing a period for stabilization

[2] Determine looping parameters [DLP-522]

[3] See NOTE 1. Set up temporary loop over failing test per messages 1, 2, and 3 in TABLE A

AND

[4] Is first failing test raw data printed twice

No

[5] At MTC channel, enter message OP:MACLI,CLASS MTCE! [FIG. 1]

Yes

Page 2

[6] Is a subclass available

Yes

[7] Repeat from Step 2

No

[8] Wait a short period and repeat from Step 3

TABLE A

MESSAGE NUMBER	INPUT MESSAGES
1	EX:a b;START! a = CS or PS b = member number
2	EX:a b:SYNC c,ENABLE d! a = CS or PS b = member number c = LOC found in Step 2 d = failing test number
3	EX:a b;RPT 2:PH c,ADR d! a = CS or PS b = member number c = failing phase d = looping address found in Step 2 (should be a range — e to f where e = start and f = end)
4	EX:a b:PH c,ADR d! Use variables shown for message 3

```
M13 OP: MACLI
   CLASS MTCE SUBCLASS 0 4 69 0 14261252 ---
   CLASS MTCE SUBCLASS 1 NONE
   CLASS MTCE SUBCLASS 2 NONE

      AVAILABLE
      OCCUPIED
```

FIG. 1 - Sample OP:MACLI Printout

NOTE 1

To discontinue looping condition, identify MACLIENT MTCE subclass assigned to frame under test by entering message:
OP:MACLI,CLASS MTCE!
Then enter message:
STOP:MACLI,CLASS MTCE,SUBCLASS a!
where a = subclass assigned to frame under test

CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FAILING ADDRESS

[9] See FIG. 2 and CAUTION. Set up oscilloscope at CC

[10] See NOTE 1, Page 1. Set up infinite loop over failing test using messages 1, 2, and 4 in TABLE A, Page 1

AND

[11] Using frame SD and CD circuit pack data and raw data analysis information, signal trace path of failing bits to isolate and clear problem

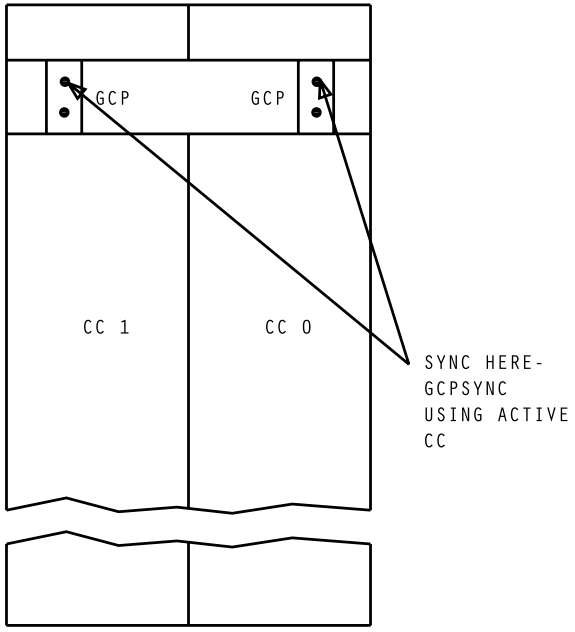
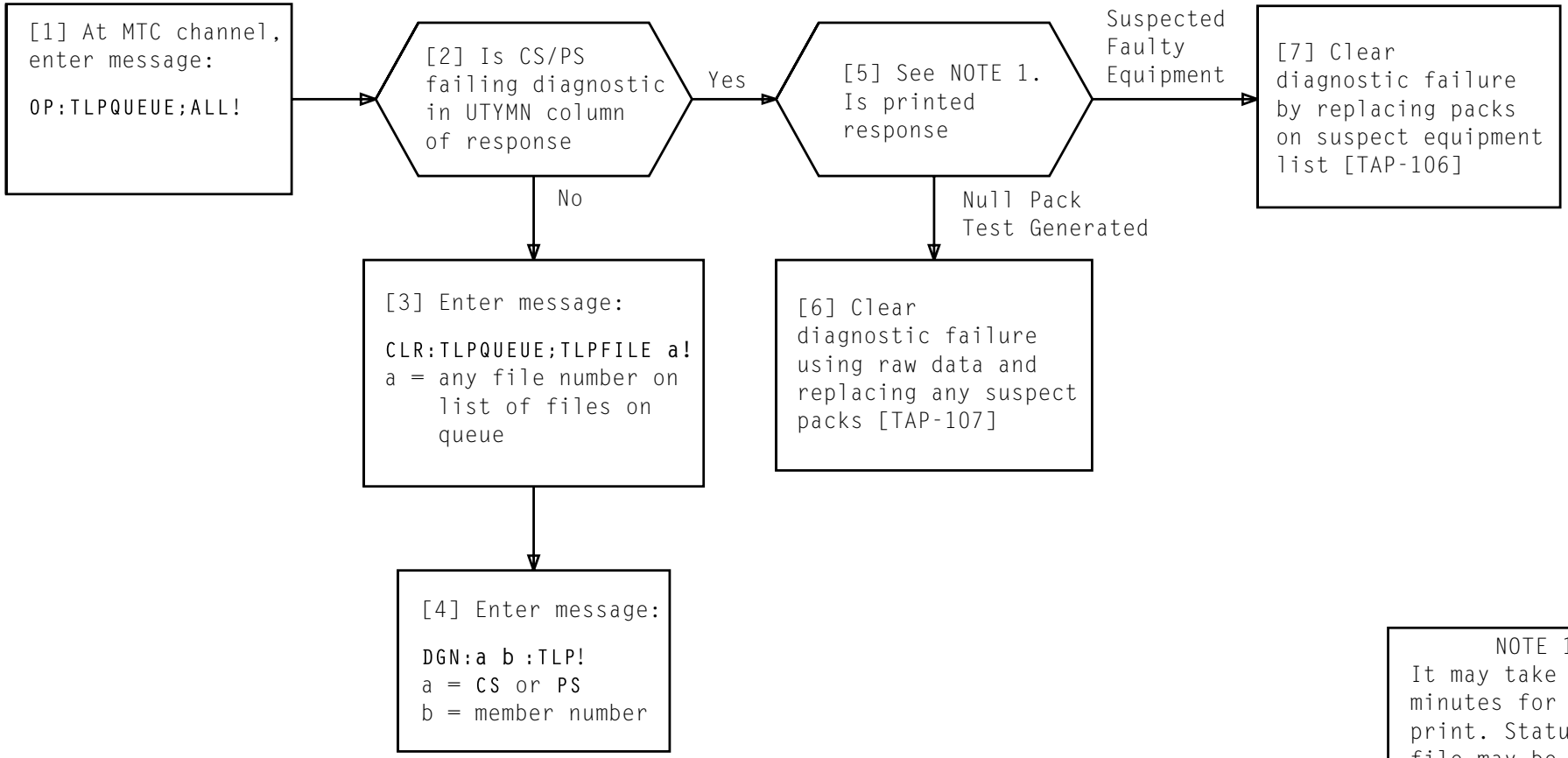


FIG. 2 – Rear View of Central Control

CAUTION
To prevent service interruption, connect scope probes first to oscilloscope and then to GCPSYN on back side of CC

CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FAILING ADDRESS



NOTE 1
It may take several minutes for list to print. Status of file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column.

CLEAR DIAGNOSTIC FAILURE, TLP DISK QUEUE FULL

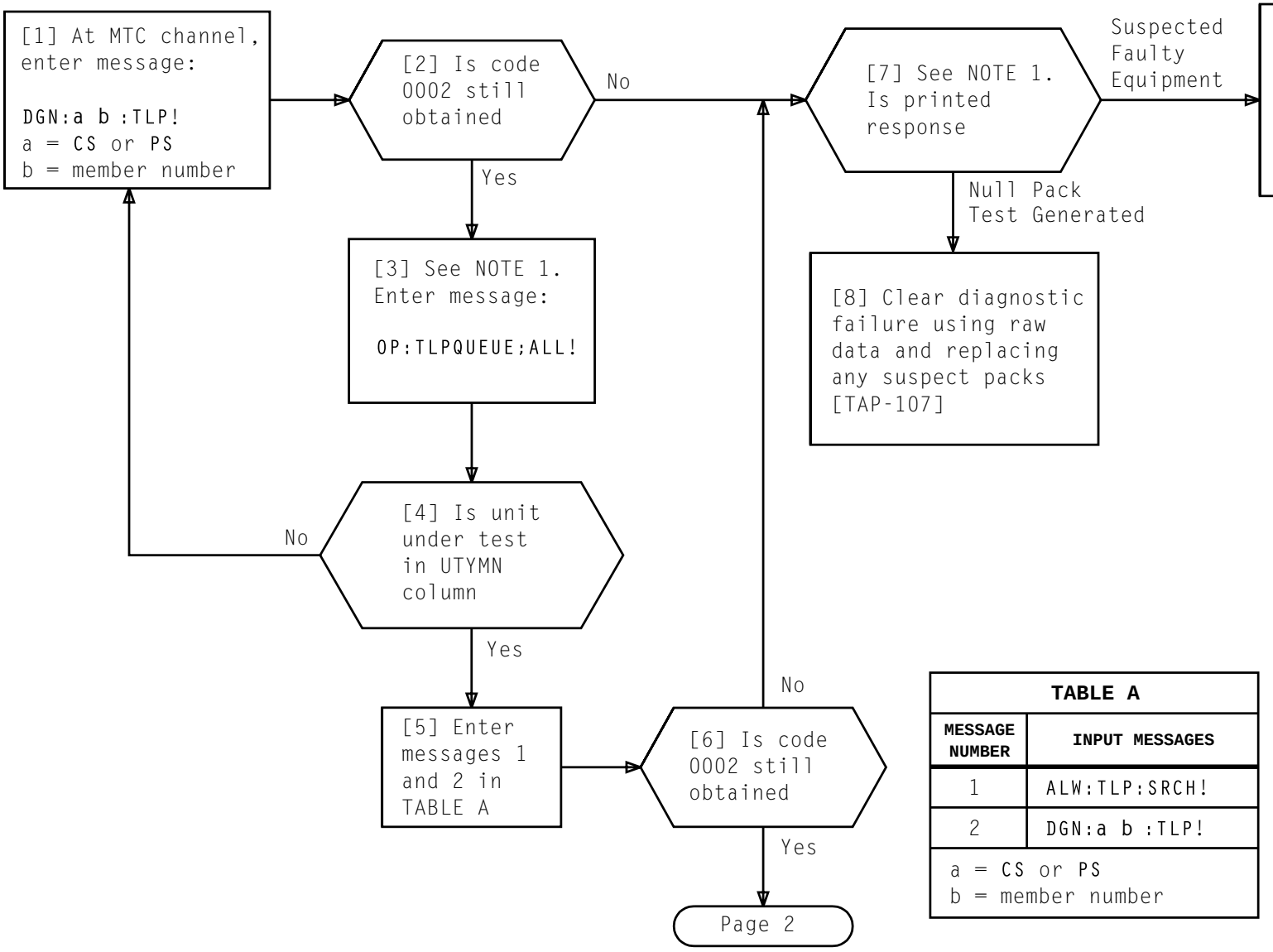


TABLE A

MESSAGE NUMBER	INPUT MESSAGES
1	ALW:TLP:SRCH!
2	DGN:a b :TLP!

a = CS or PS
b = member number

NOTE 1

It may take several minutes for list to print. Status of file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column.

CLEAR DIAGNOSTIC FAILURE, TLP QUEUE BLOCKAGE

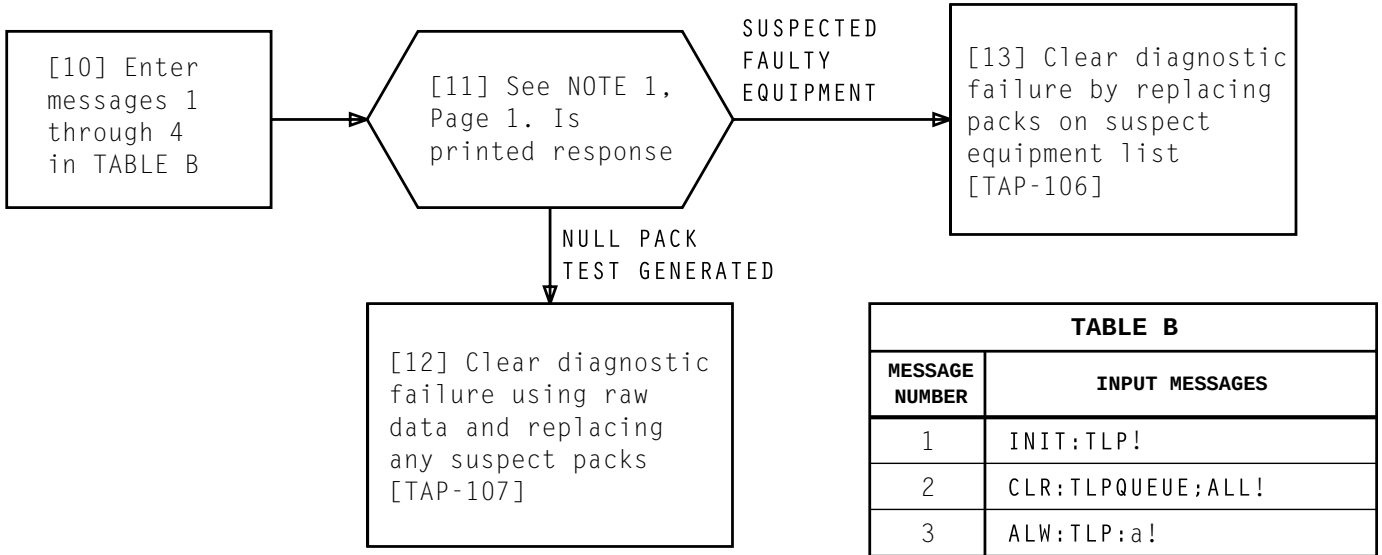
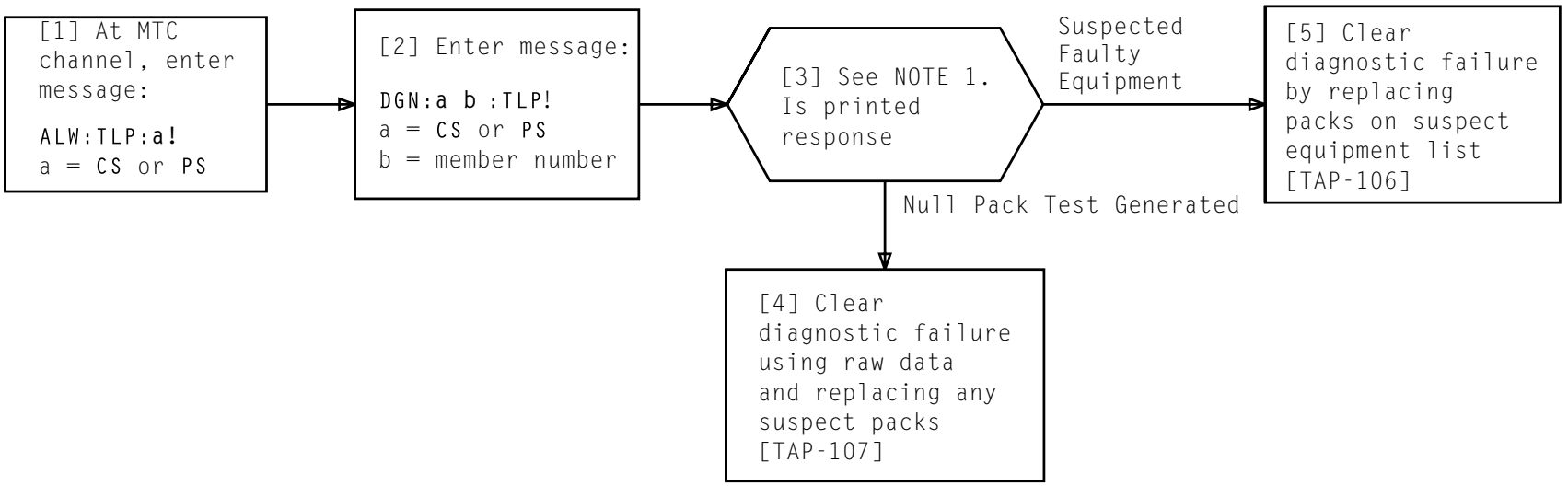


TABLE B

MESSAGE NUMBER	INPUT MESSAGES
1	INIT:TLP!
2	CLR:TLPQUEUE;ALL!
3	ALW:TLP:a!
4	DGN:a b:TLP!

a = CS or PS
b = member number

CLEAR DIAGNOSTIC FAILURE, TLP QUEUE BLOCKAGE

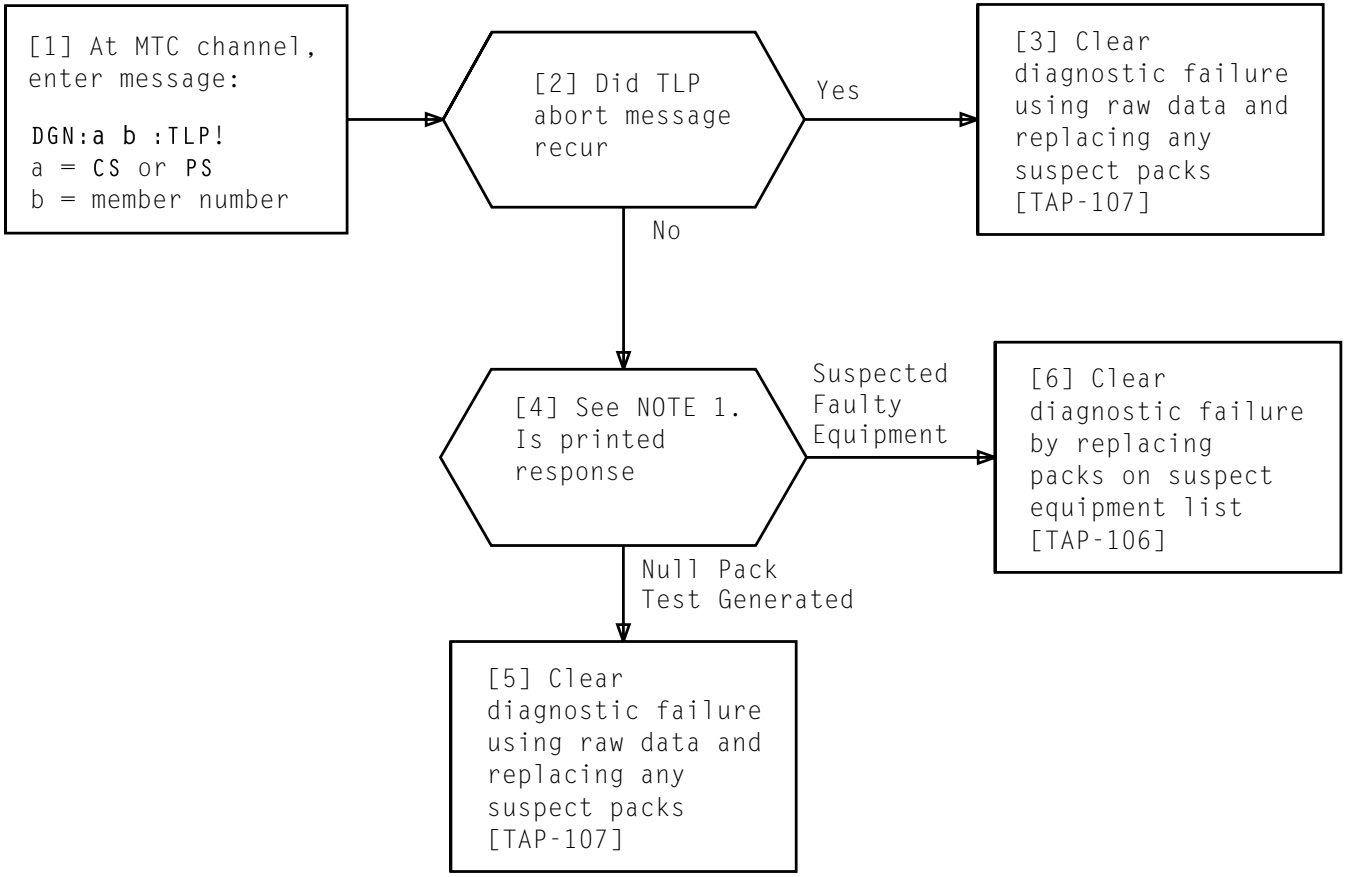


NOTE 1
It may take several minutes for list to print. Status of file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column

CLEAR DIAGNOSTIC FAILURE, REMOVE CS/PS TLP INHIBIT



NOTE 1
It may take several minutes for list to print. Status of file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column.

CLEAR DIAGNOSTIC FAILURE, TLP ABORT

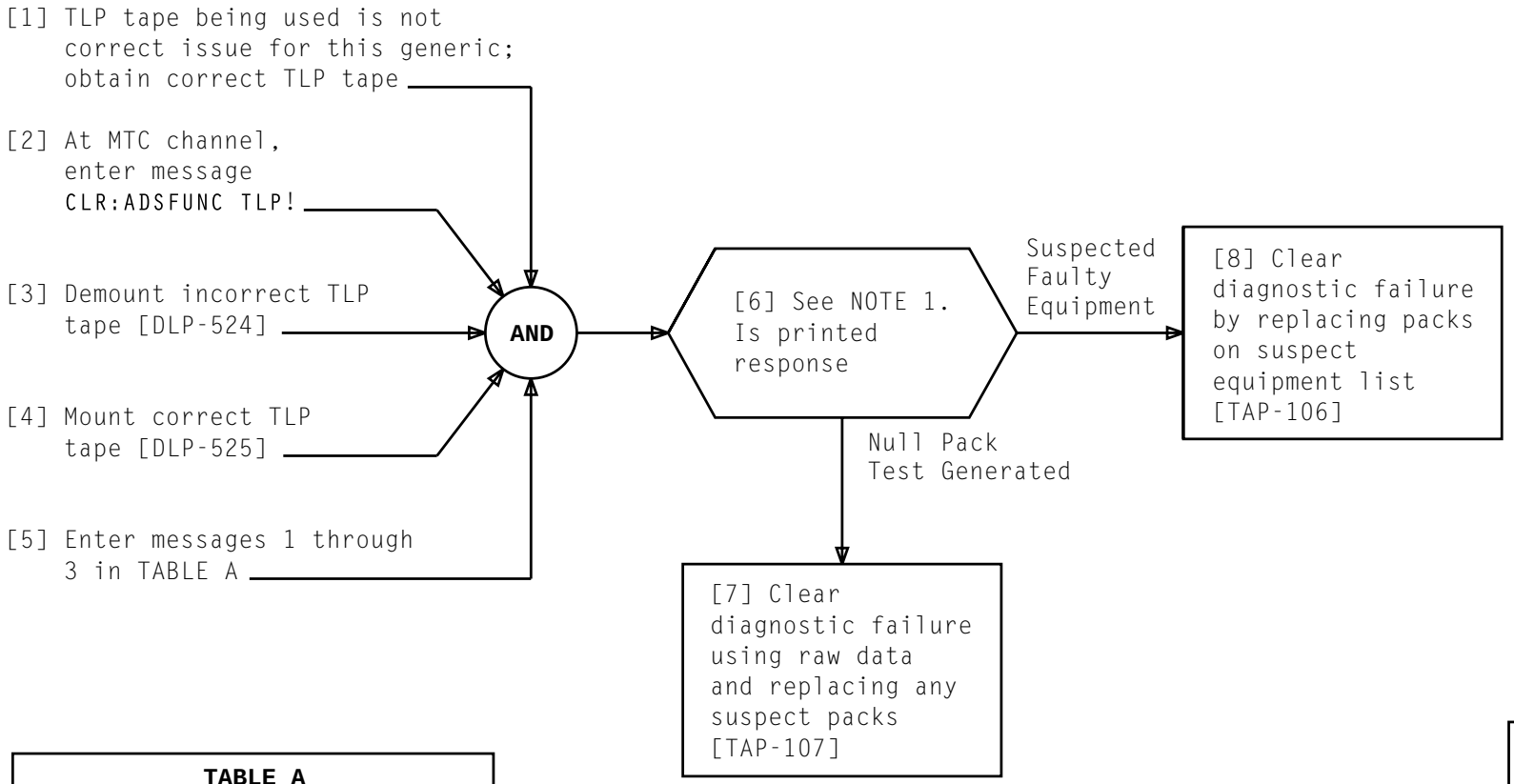


TABLE A	
MESSAGE NUMBER	**INPUT MESSAGES**
1	SET:TUC a;FUNCTION TLP!
2	ALW:TUC a:RO!
3	DGN:b c:TLP!

a = member number of TUC with TLP tape mounted
b = CS or PS
c = member number

NOTE 1
It may take several minutes for list to print. Status file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column.

CLEAR DIAGNOSTIC FAILURE, TLP TAPE VERSION X DOES NOT MATCH VERSION Y

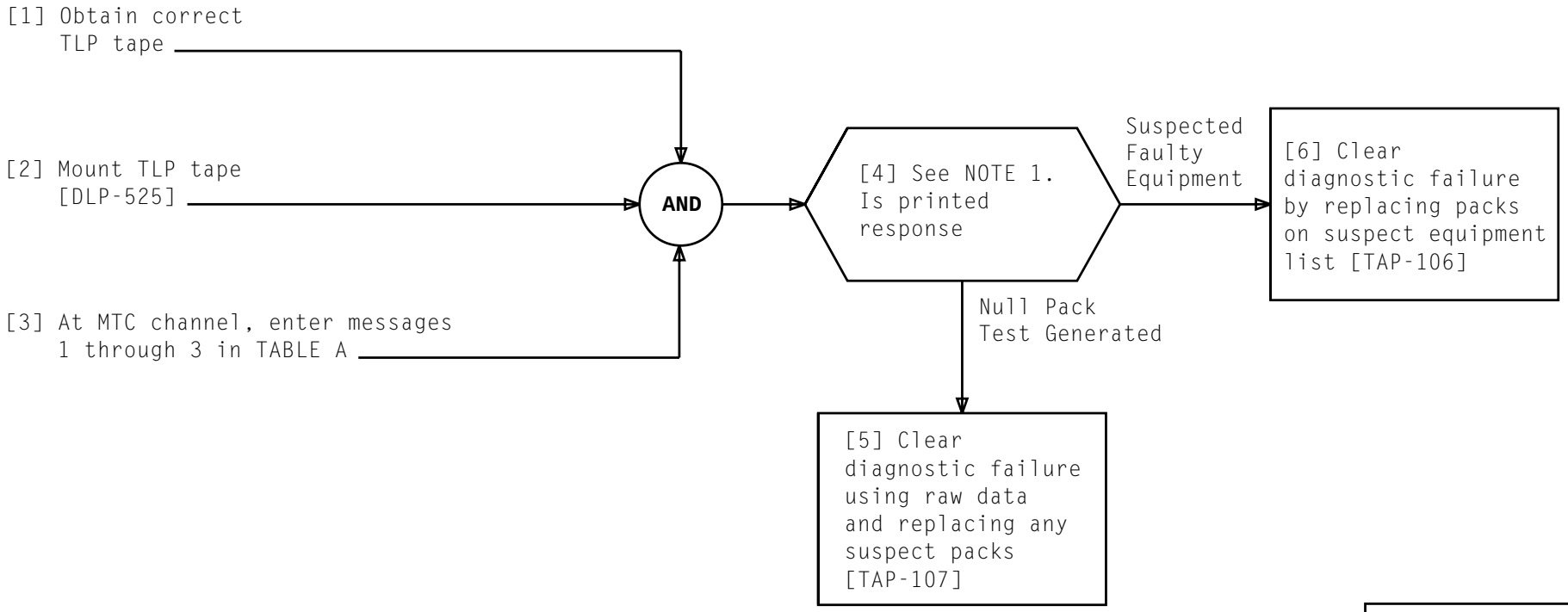


TABLE A	
MESSAGE NUMBER	**INPUT MESSAGES**
1	SET:TUC a;FUNCTION TLP!
2	ALW:TUC a :RO!
3	DGN:b c :TLP!

a = member number of TUC with TLP tape mounted
b = CS or PS
c = member number

NOTE 1
It may take several minutes for list to print. Status of your file may monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column.

CLEAR DIAGNOSTIC FAILURE, TLP TAPE NOT MOUNTED

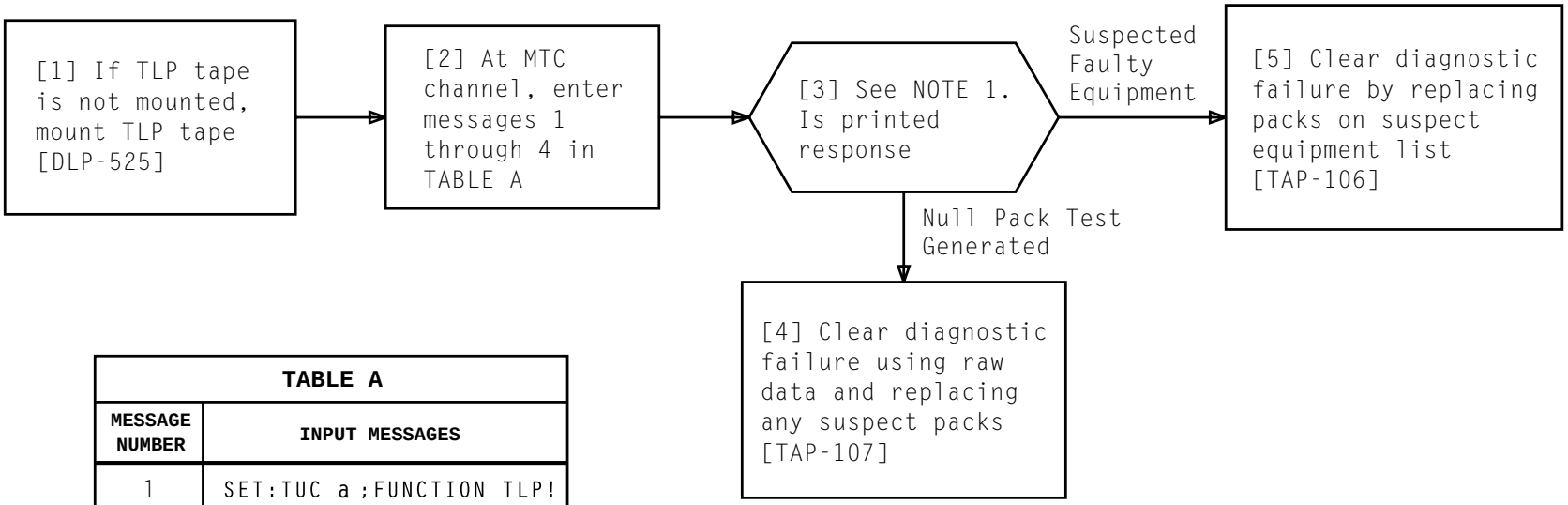


TABLE A

MESSAGE NUMBER	INPUT MESSAGES
1	SET:TUC a ;FUNCTION TLP!
2	ALW:TUC a:RO!
3	ALW:TLP:SRCH,b!
4	DGN:b c :TLP!

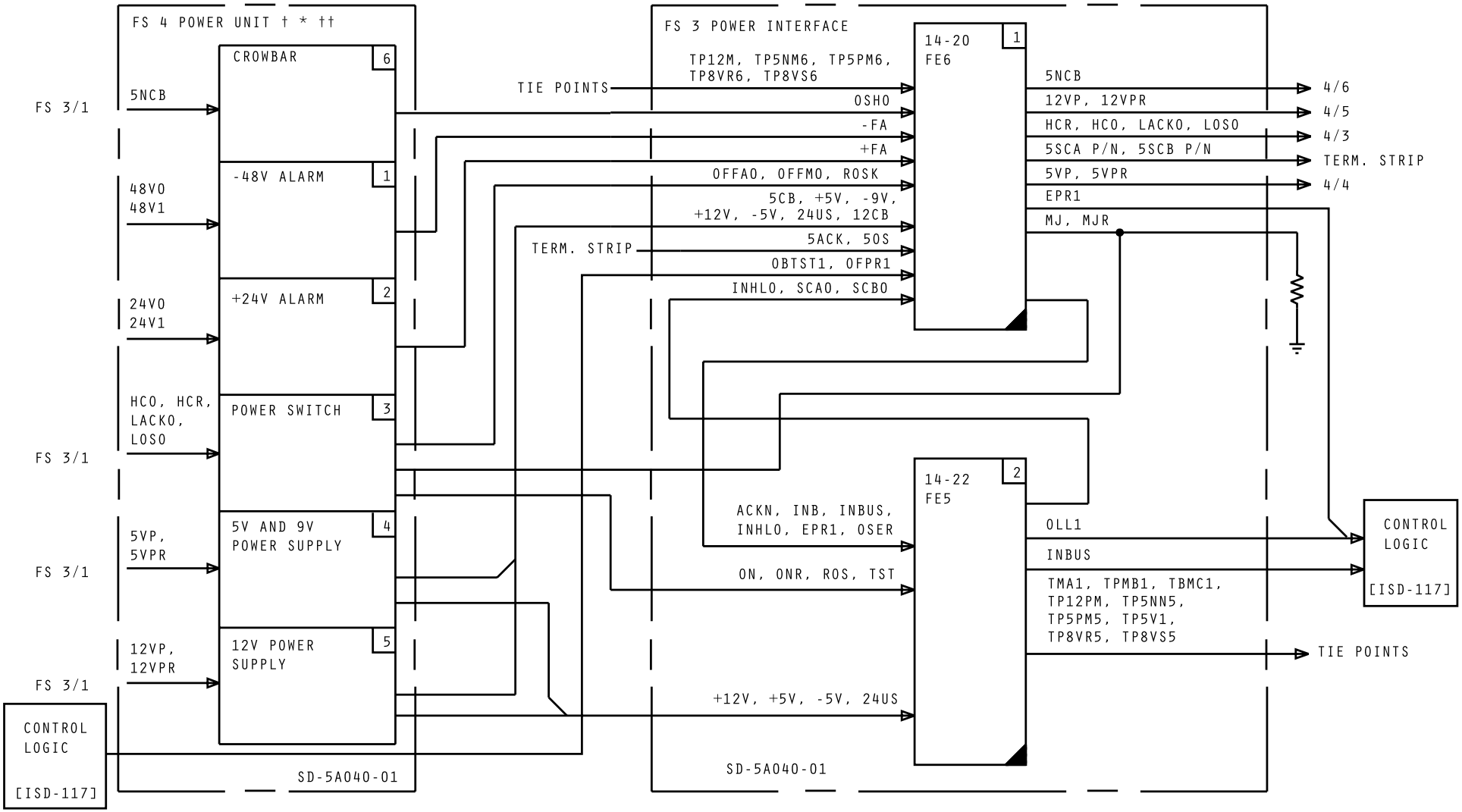
a = member number of TUC with TLP tape mounted
b = CS or PS
c = member number

NOTE 1
It may take several minutes for list to print. Status of file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column.

CLEAR DIAGNOSTIC FAILURE, TLP SEARCH INHIBITED



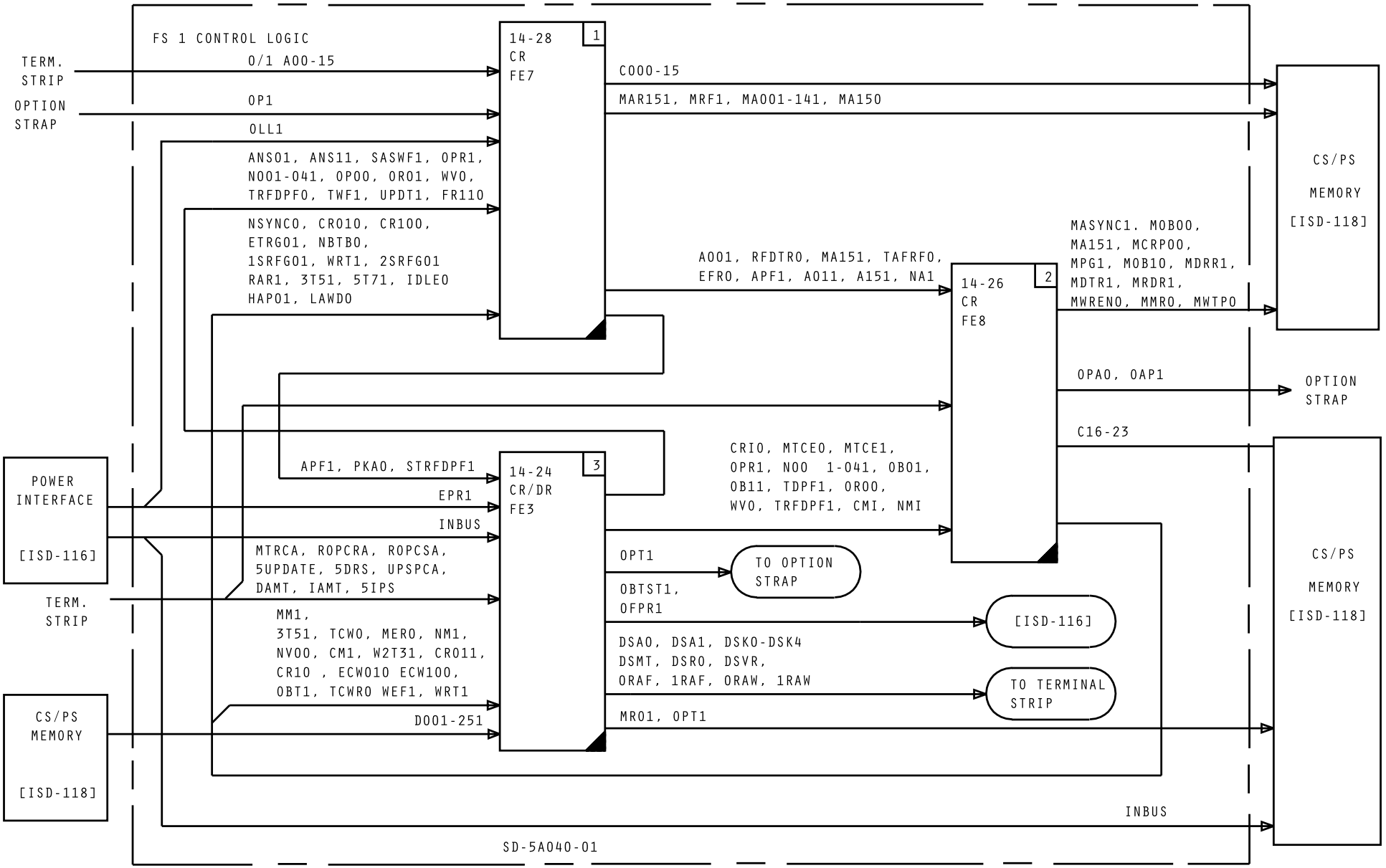
† REFERENCES TO TERMINAL STRIP MAY BE UPPER OR LOWER. REFERENCE SD AS REQUIRED

* DRAWN FOR MEMORY NUMBER 5. OTHERS SIMILAR EXCEPT FOR IDENTIFIERS

†† NUMBERS IN UPPER RIGHT CORNERS ARE FS SYMBOL NUMBERS

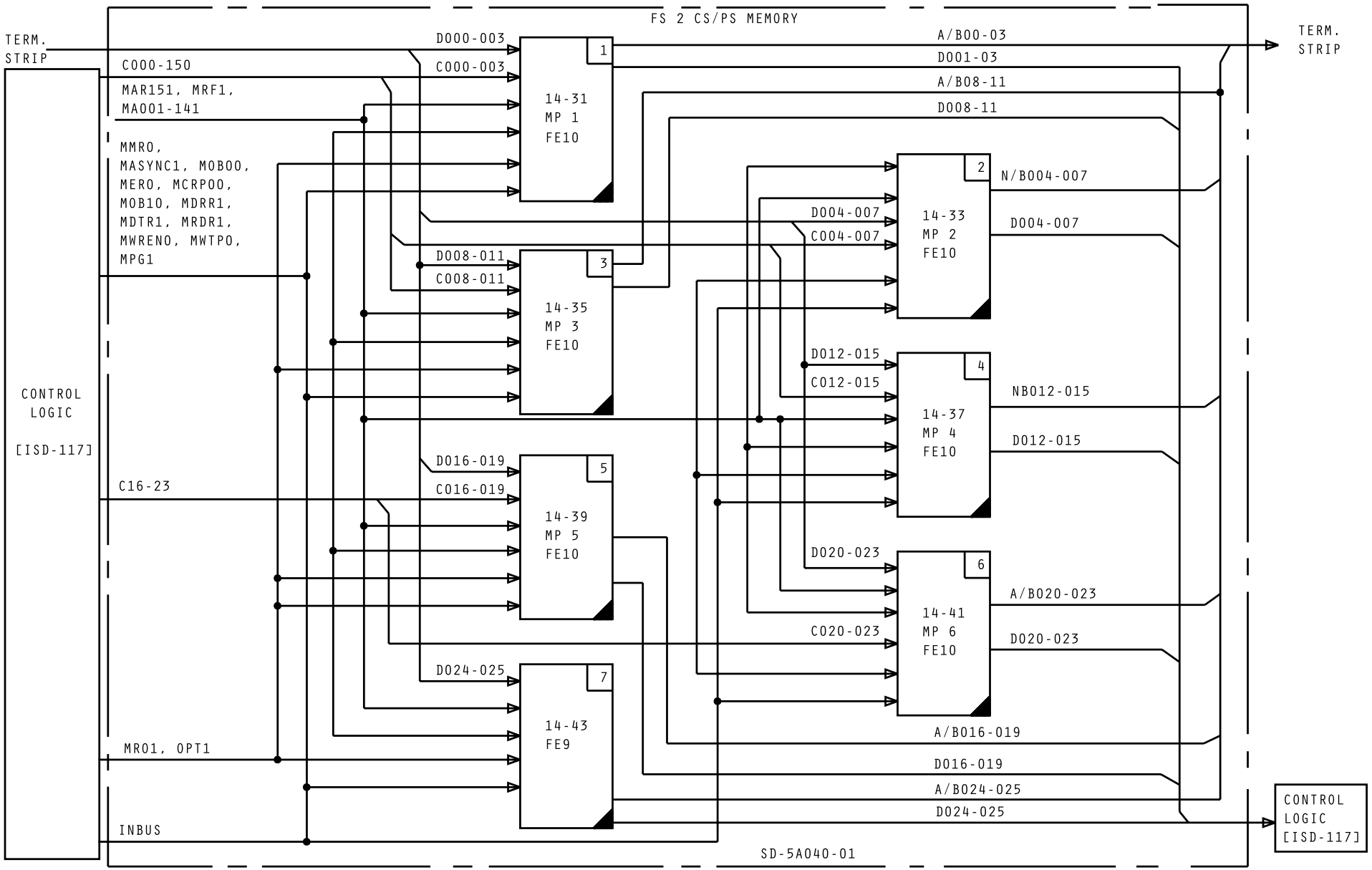
POWER INTERFACE ISOLATION DIAGRAM FOR SEMICONDUCTOR STORE J5A008A

Issue 7	NOV 1993
254-251-005	ISD
PAGE 1 of 1	116



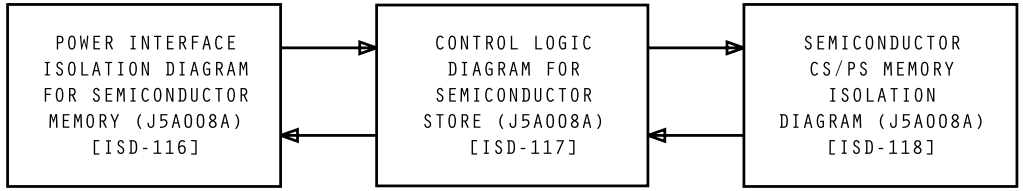
CONTROL LOGIC ISOLATION DIAGRAM FOR SEMICONDUCTOR STORE J5A008A

Issue 7	NOV 1993
254-251-005	ISD
PAGE 1 of 1	117

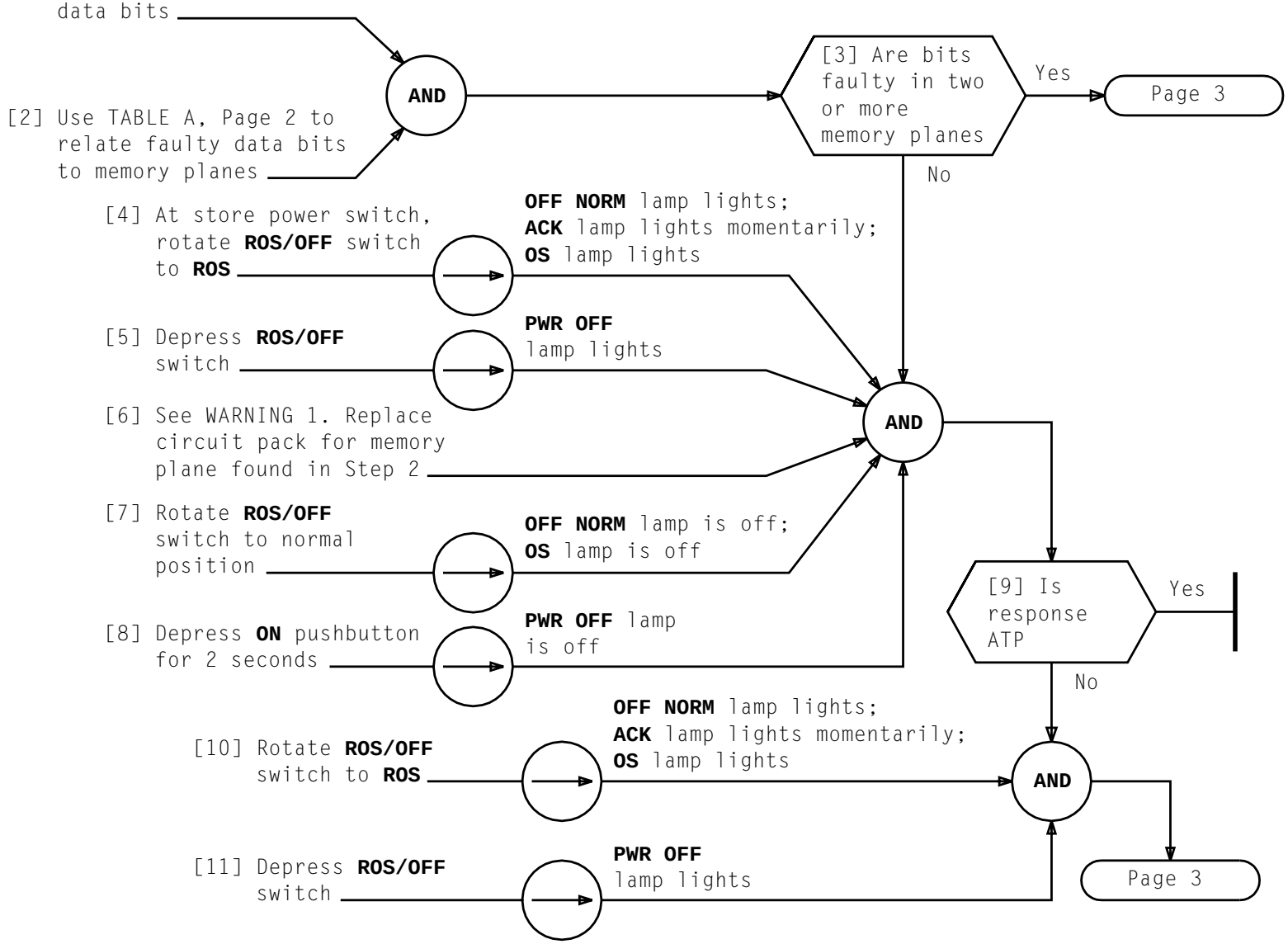


Issue 7	NOV 1993
254-251-005	ISD
PAGE 1 of 1	118

CS/PS MEMORY ISOLATION DIAGRAM, SEMICONDUCTOR STORE J5A008A



ISD LAYOUT, SEMICONDUCTOR STORE J5A008A



WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

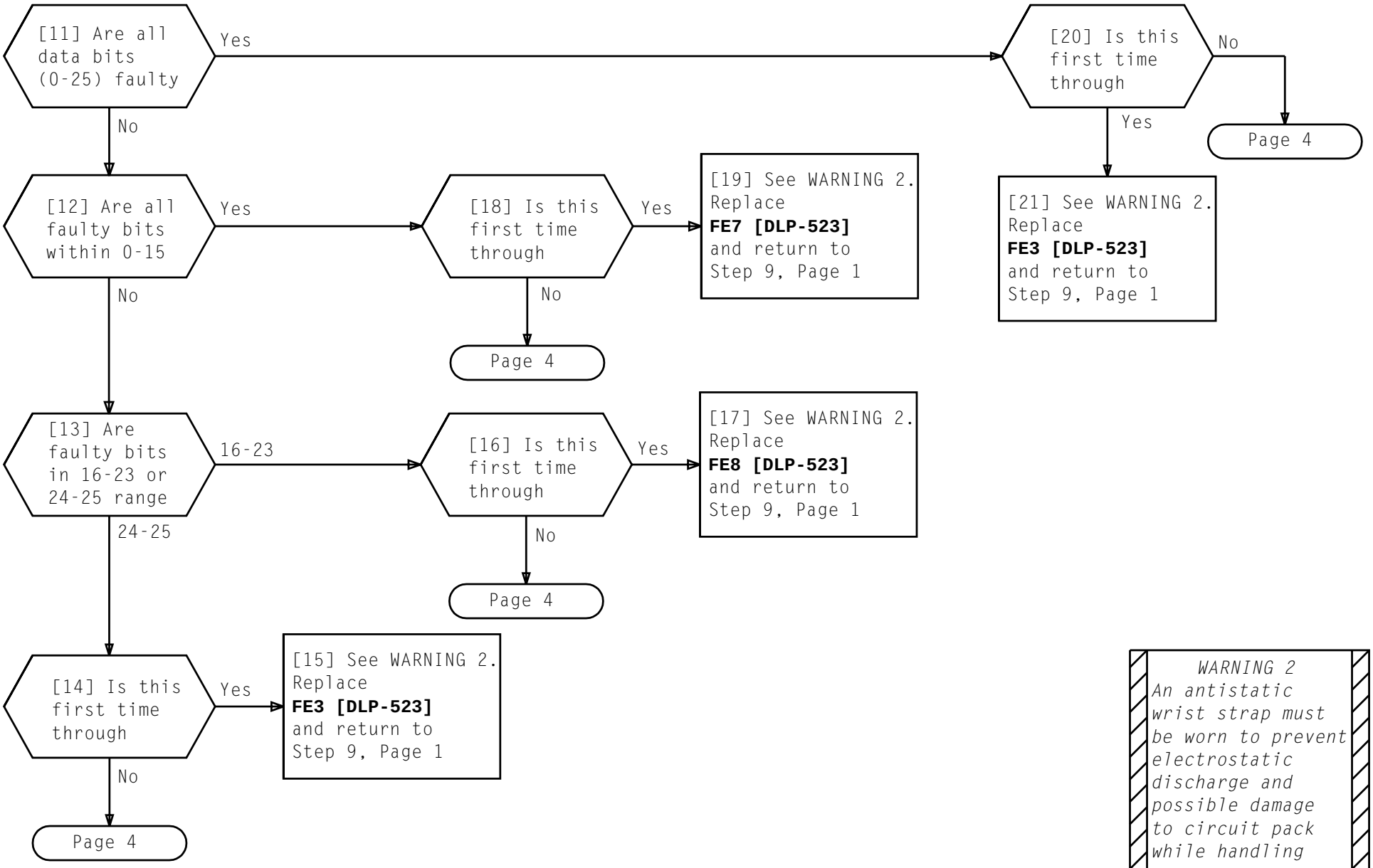
CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, SEMICONDUCTOR STORE J5A008A

TABLE A			
FAULTY DATA BITS	**MEMORY PLANE**	**CIRCUIT PACK**	**LOC**
0-3	MP 1	**FE10**	31
4-7	MP 2	↑	33
8-11	MP 3	|	35
12-15	MP 4	|	37
16-19	MP 5	↓	39
20-23	MP 6	**FE10**	41
24-25	MP 7	**FE9**	43

ADDRESS BIT	COUNT	DATA BIT		ERROR SUMMARY WORD 0	
0	0(0)	0	0	0	
1	0(0)	1	0	0	
2	0(0)	2	0	0	
3	0(0)	3	0	0	
4	0(0)	4	0	0	
5	0(0)	5	0	0	
6	0(0)	6	0	0	
7	0(0)	7	0	0	
8	0(0)	8	0	0	
9	0(0)	9	0	0	
10	0(0)	10	0	0	
11	0(0)	11	0	0	
12	1(1)	12	1	1	FAULTY DATA BITS
13	1(1)	13	1	1	
14	1(1)	14	1	1	
15	1(1)	15	1	1	
16	0(0)	16	0	0	
17	0(0)	17	0	0	
		18	0	0	
		19	0	0	
		20	0	0	
		21	0	0	
		22	0	0	
		23	0	0	
		24	0	0	PARITY 2
		25	0	0	PARITY 1

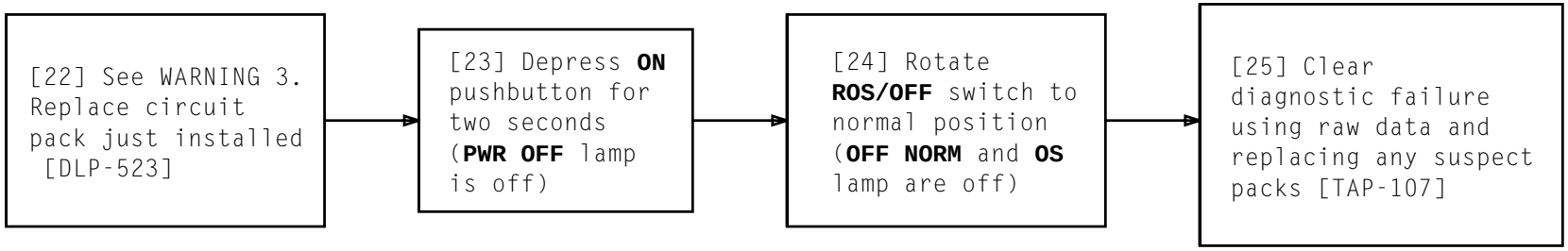
FIG. 1 — Sample of Histogram Printout

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, SEMICONDUCTOR STORE J5A008A



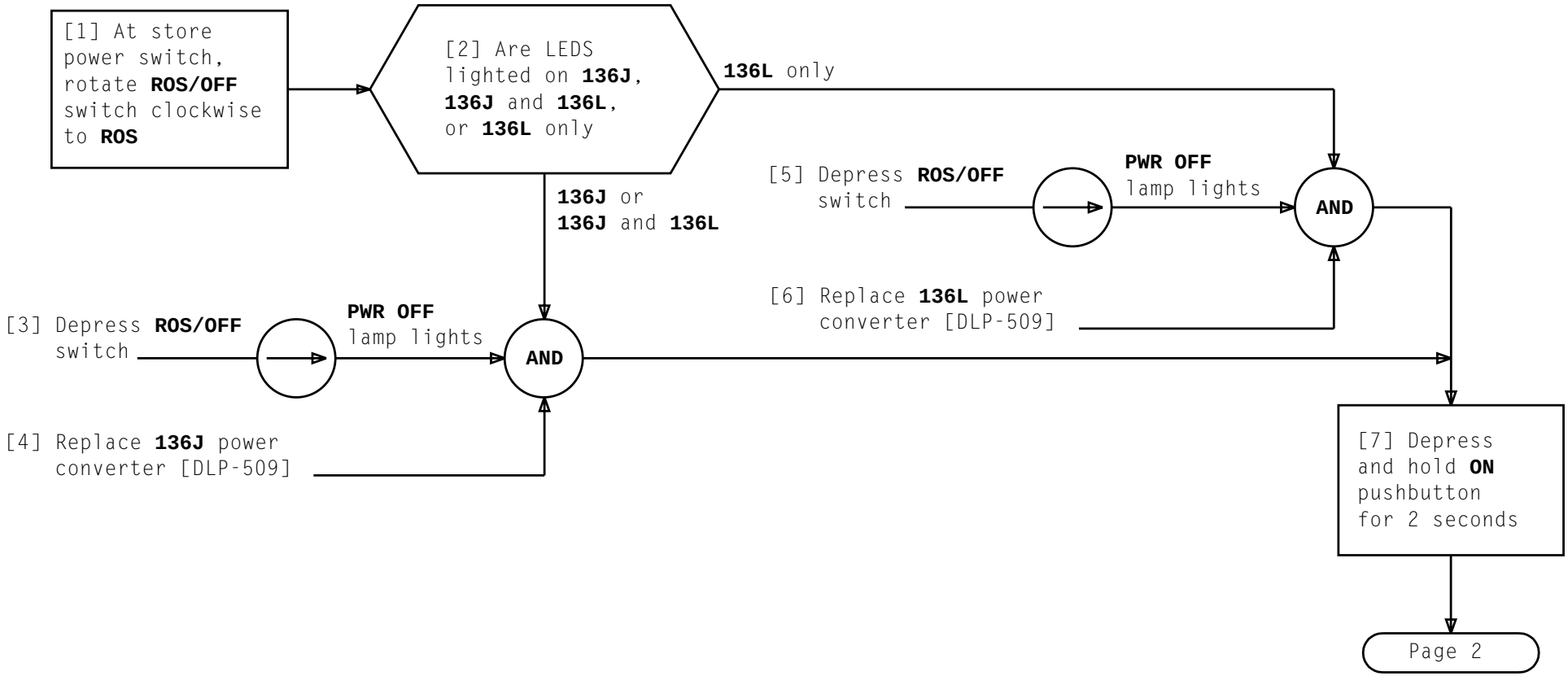
WARNING 2
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, SEMICONDUCTOR STORE J5A008A



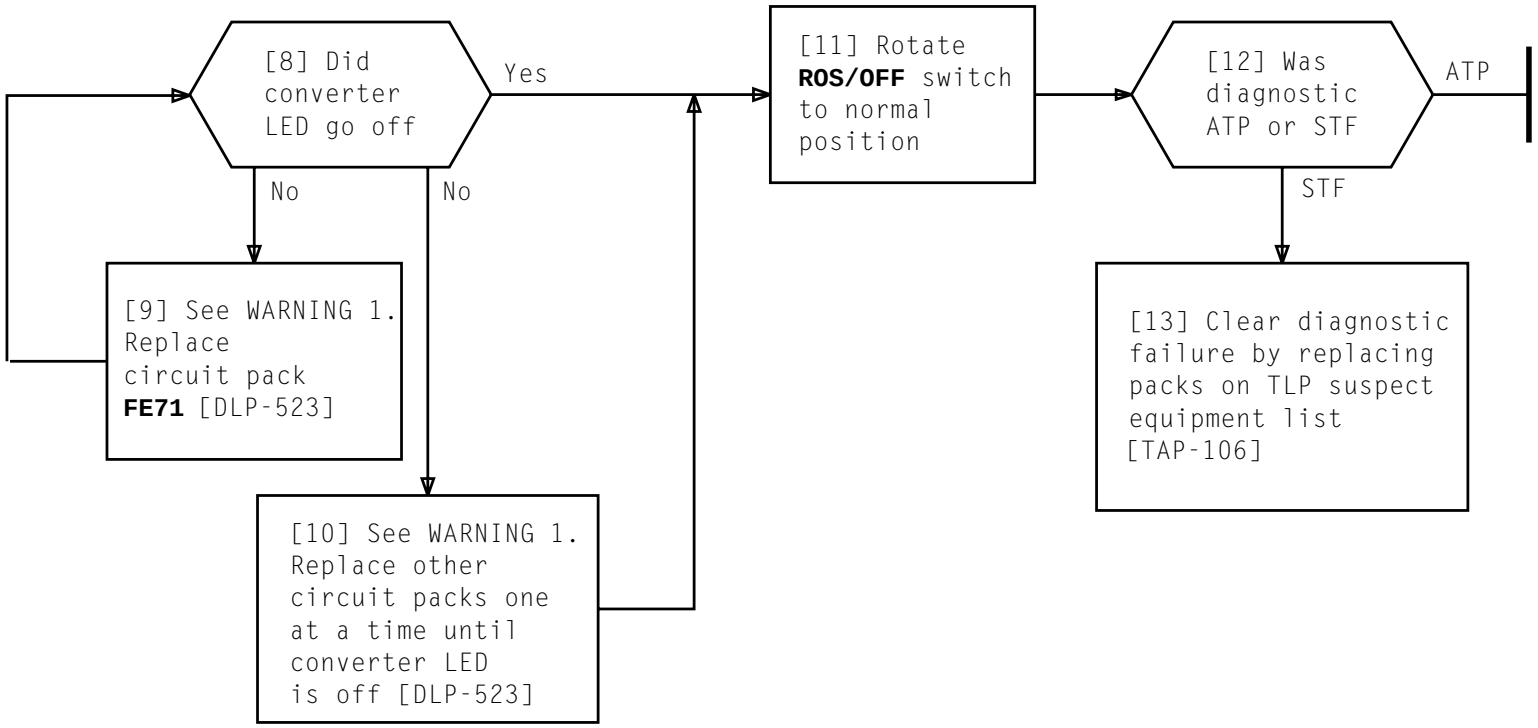
WARNING 3
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, SEMICONDUCTOR STORE J5A008A



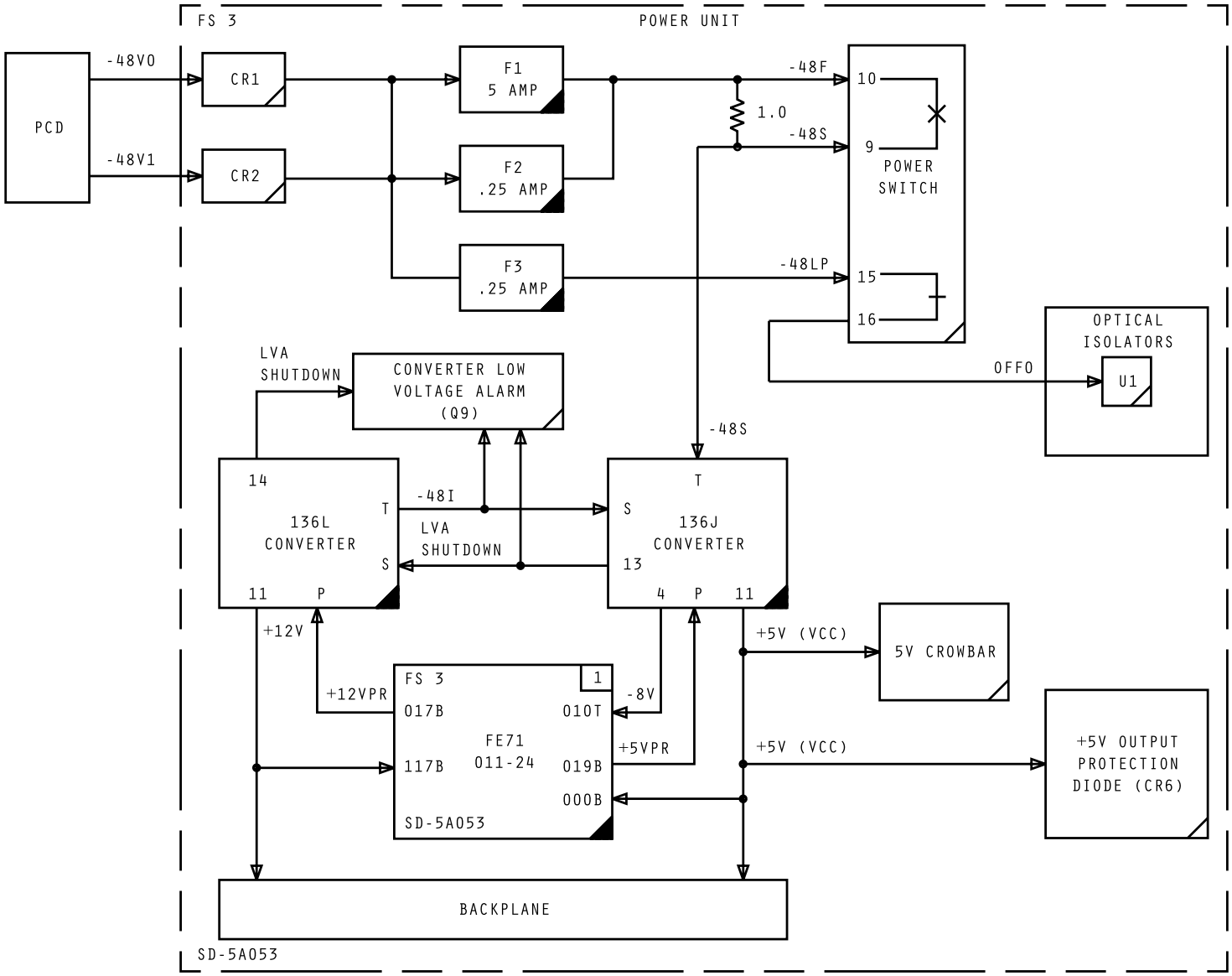
CLEAR POWER CONVERTER ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

Issue 7	NOV 1993
254-251-005	TAP
PAGE 1 of 2	121



WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit packs while handling

CLEAR POWER CONVERTER ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



Issue 7	NOV 1993
254-251-005	ISD
PAGE 1 of 1	122

POWER ISOLATION DIAGRAM FOR 256K STORE J5A010A OR J5A010B

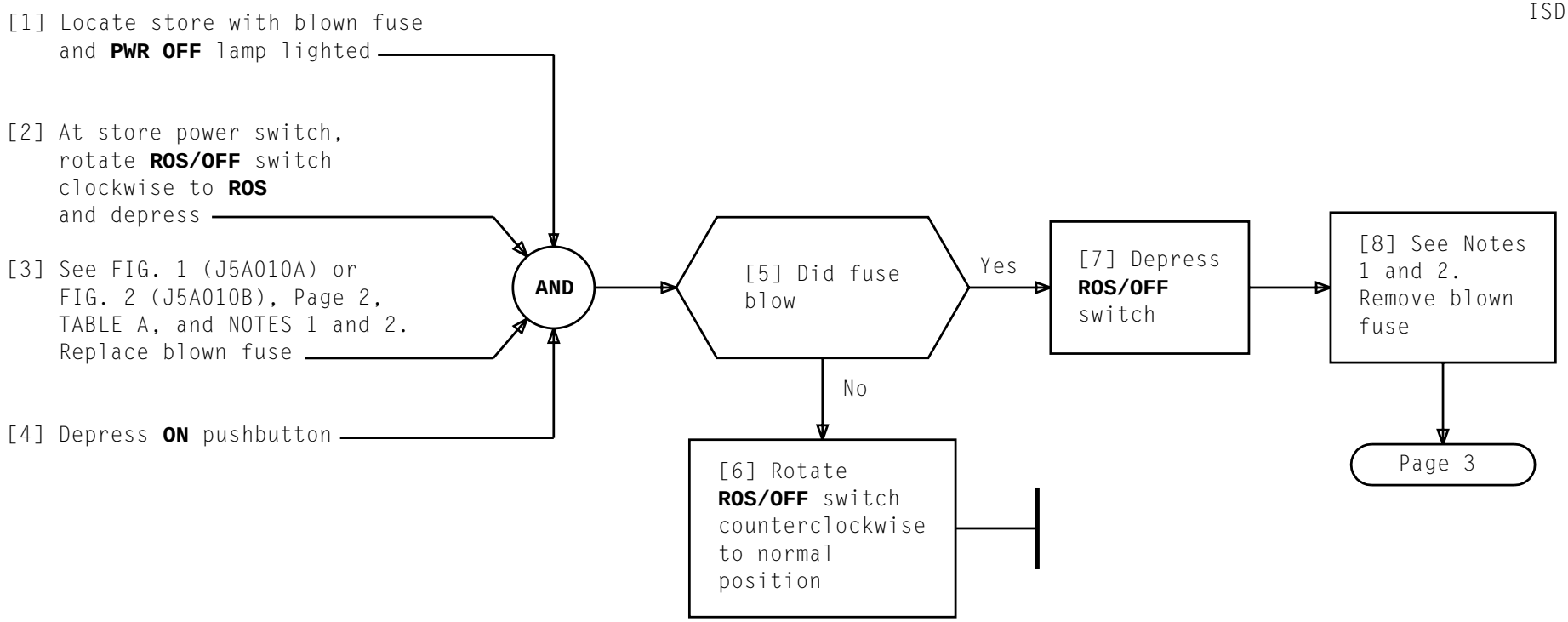


TABLE A		
FUSE	**AMPS**	**TYPE**
F1	5A	74C
F2	.25A	70F
F3	.25A	70F

NOTES
1. If fuse **F2** is blown, **F1** is also blown
2. When replacing fuses **F1** and **F2**, indicator fuse **F2** should be removed first and replaced last

CLEAR FUSE ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

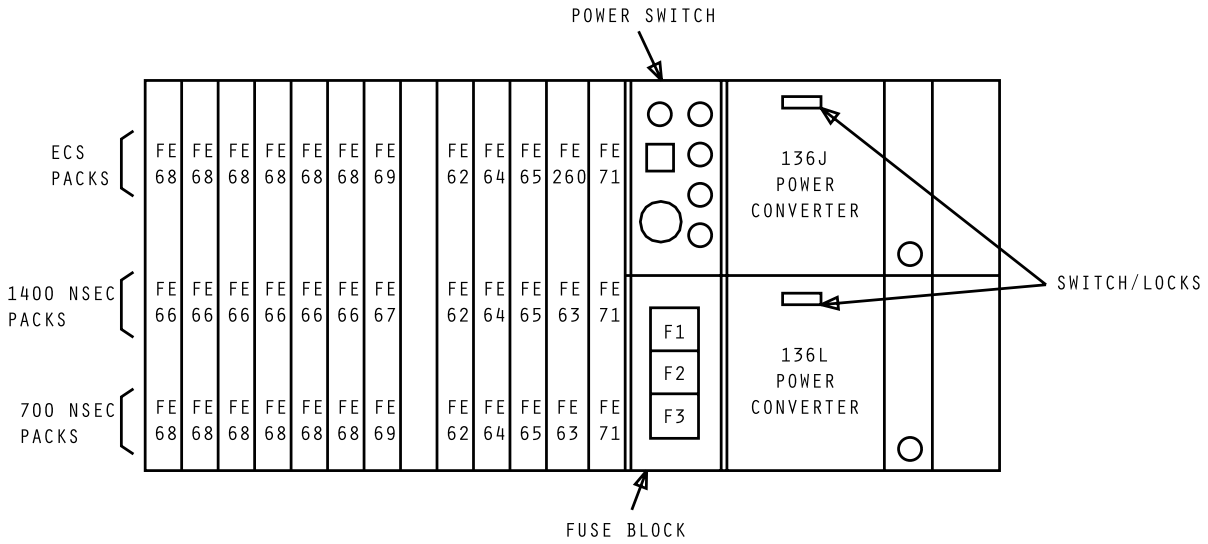


FIG. 1 — Front View, J5A010A Semiconductor Store Unit

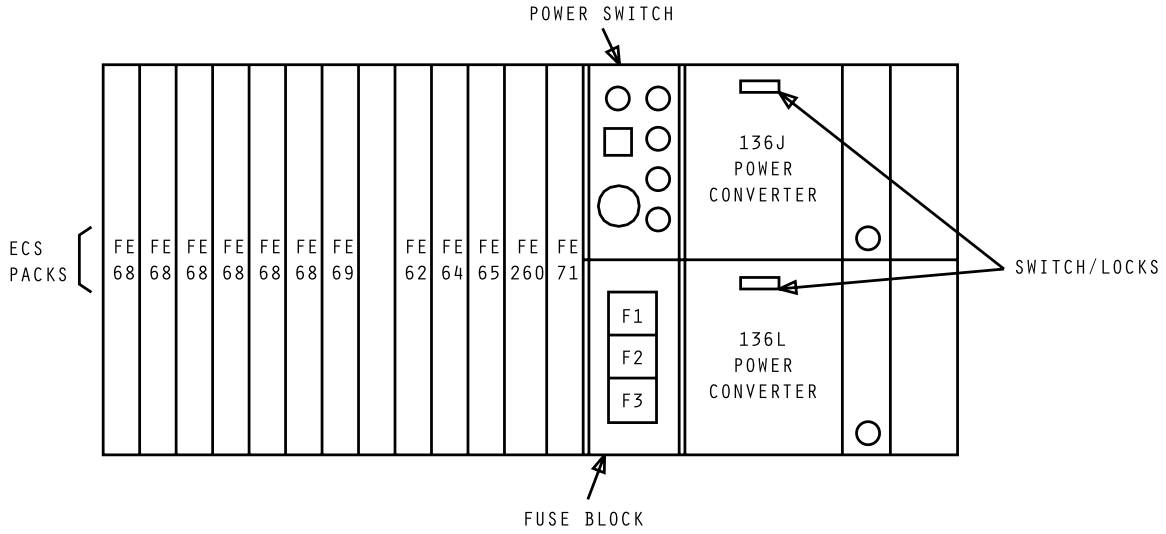
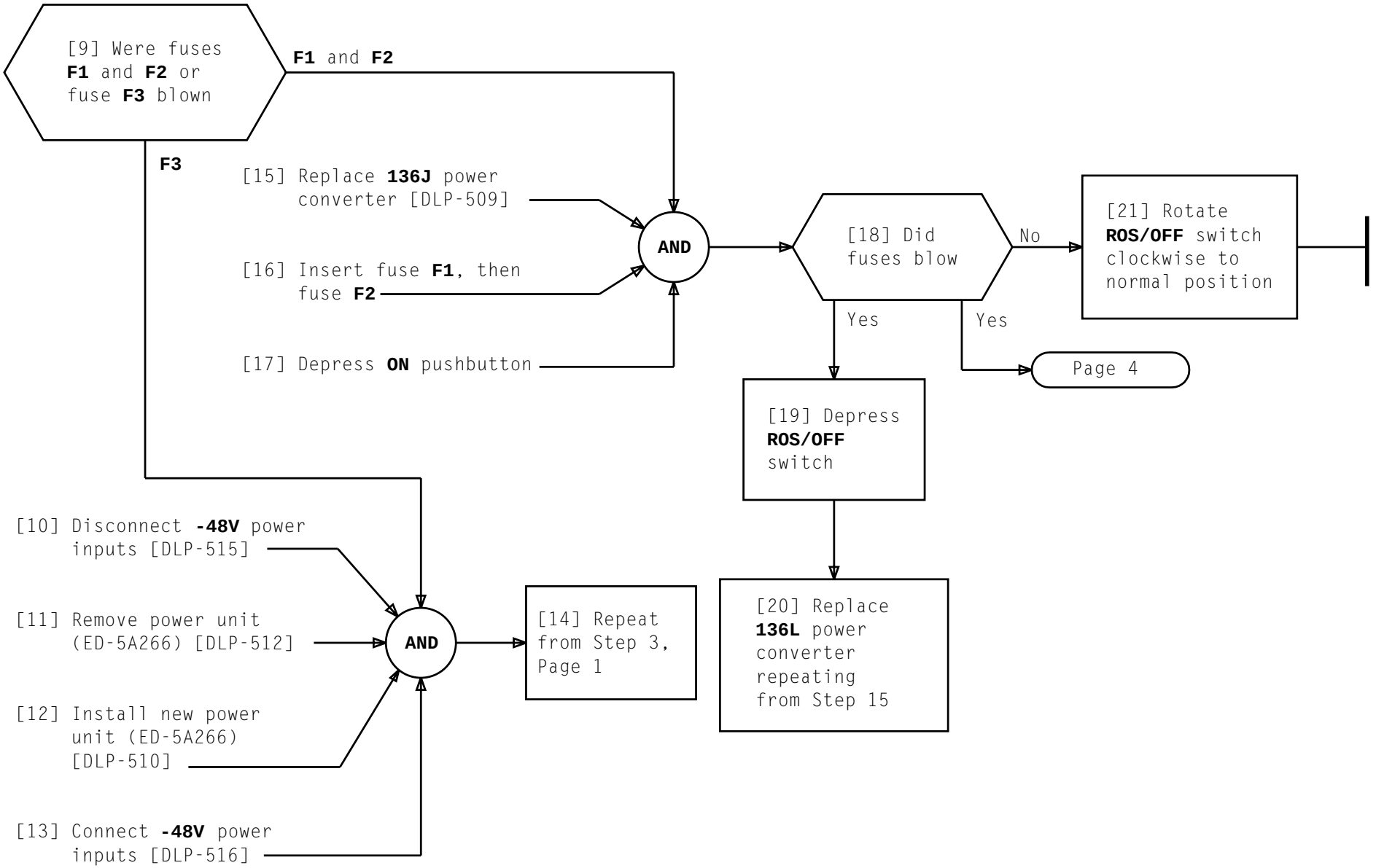
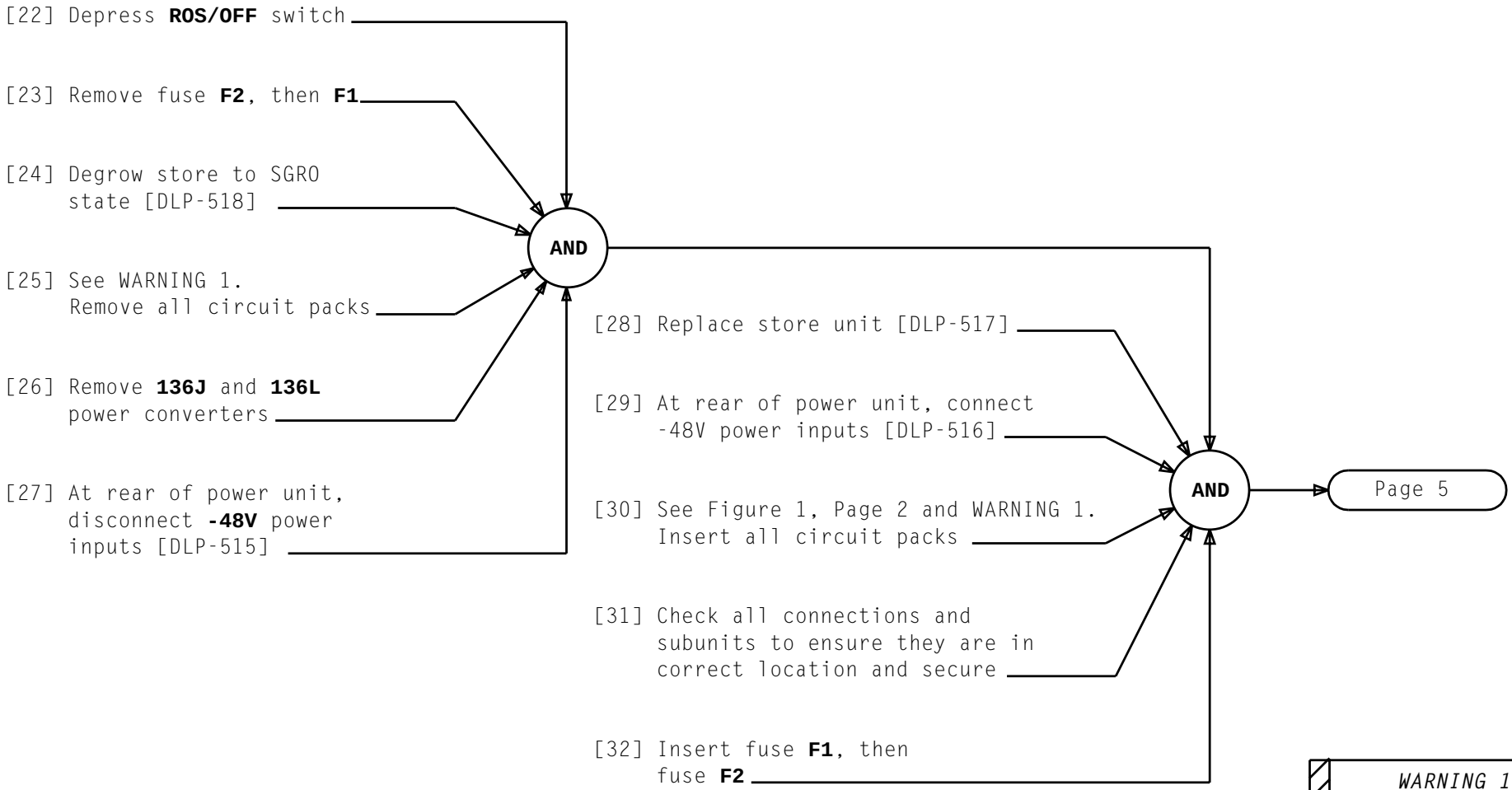


FIG. 2 — Front View, J5A010B Semiconductor Store Unit

CLEAR FUSE ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

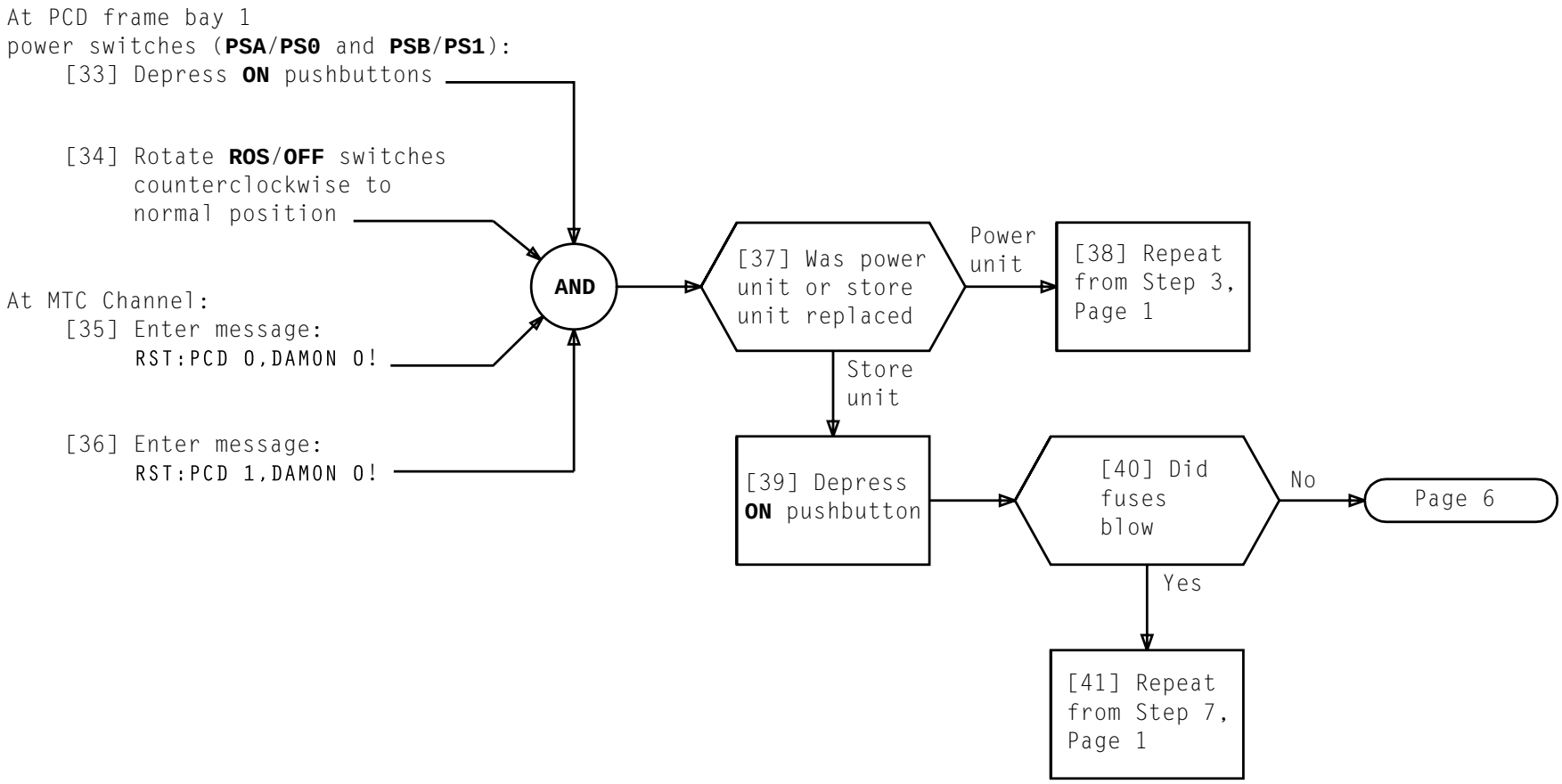


CLEAR FUSE ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

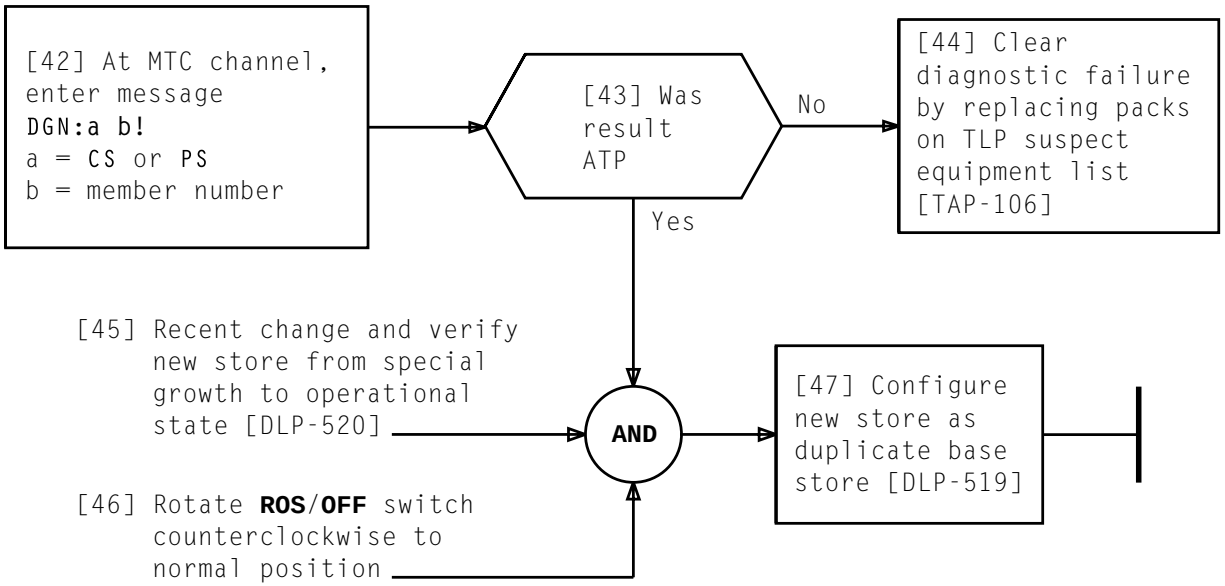


WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possble damage to circuit pack while handling

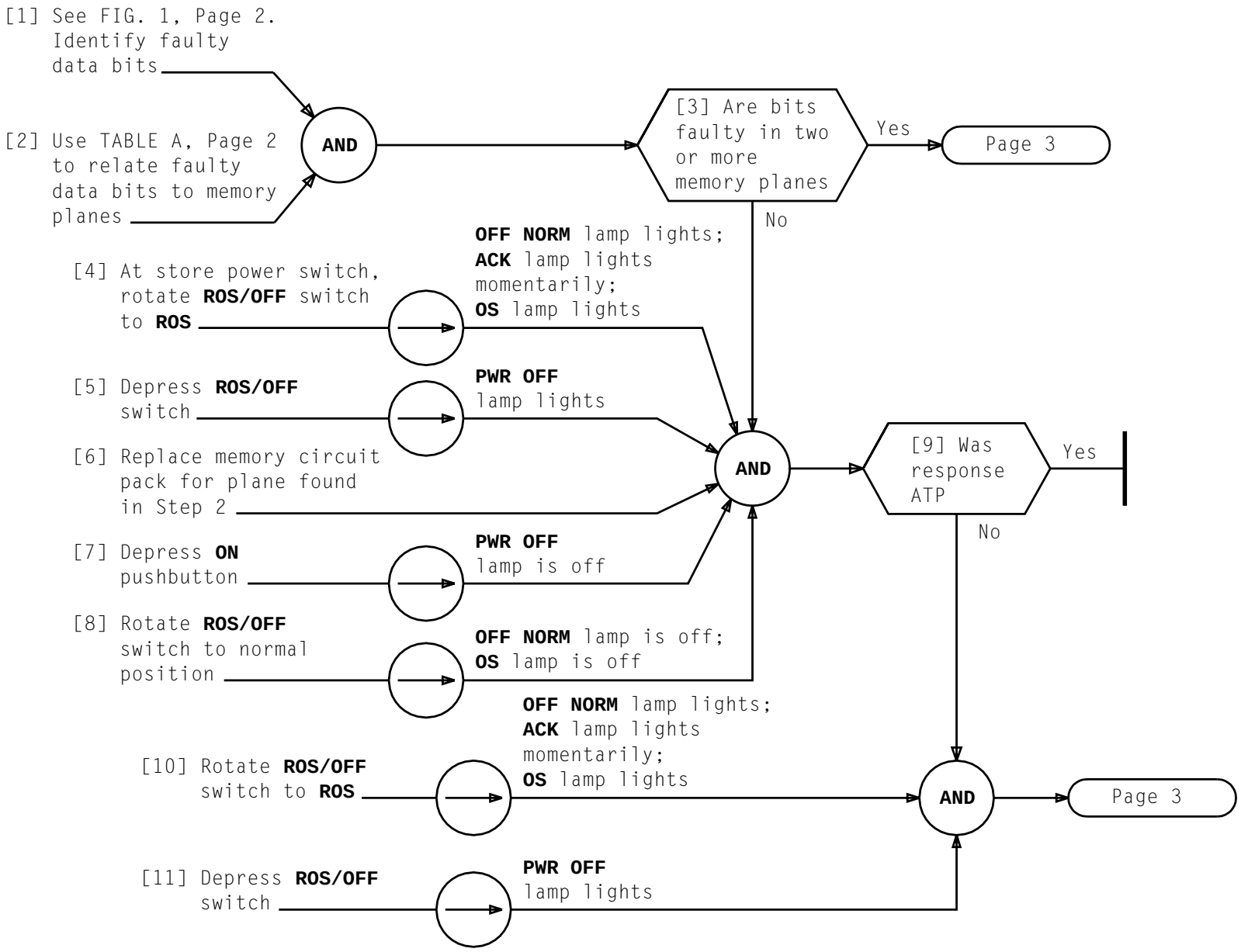
CLEAR FUSE ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



CLEAR FUSE ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



CLEAR FUSE ALARM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

TABLE A

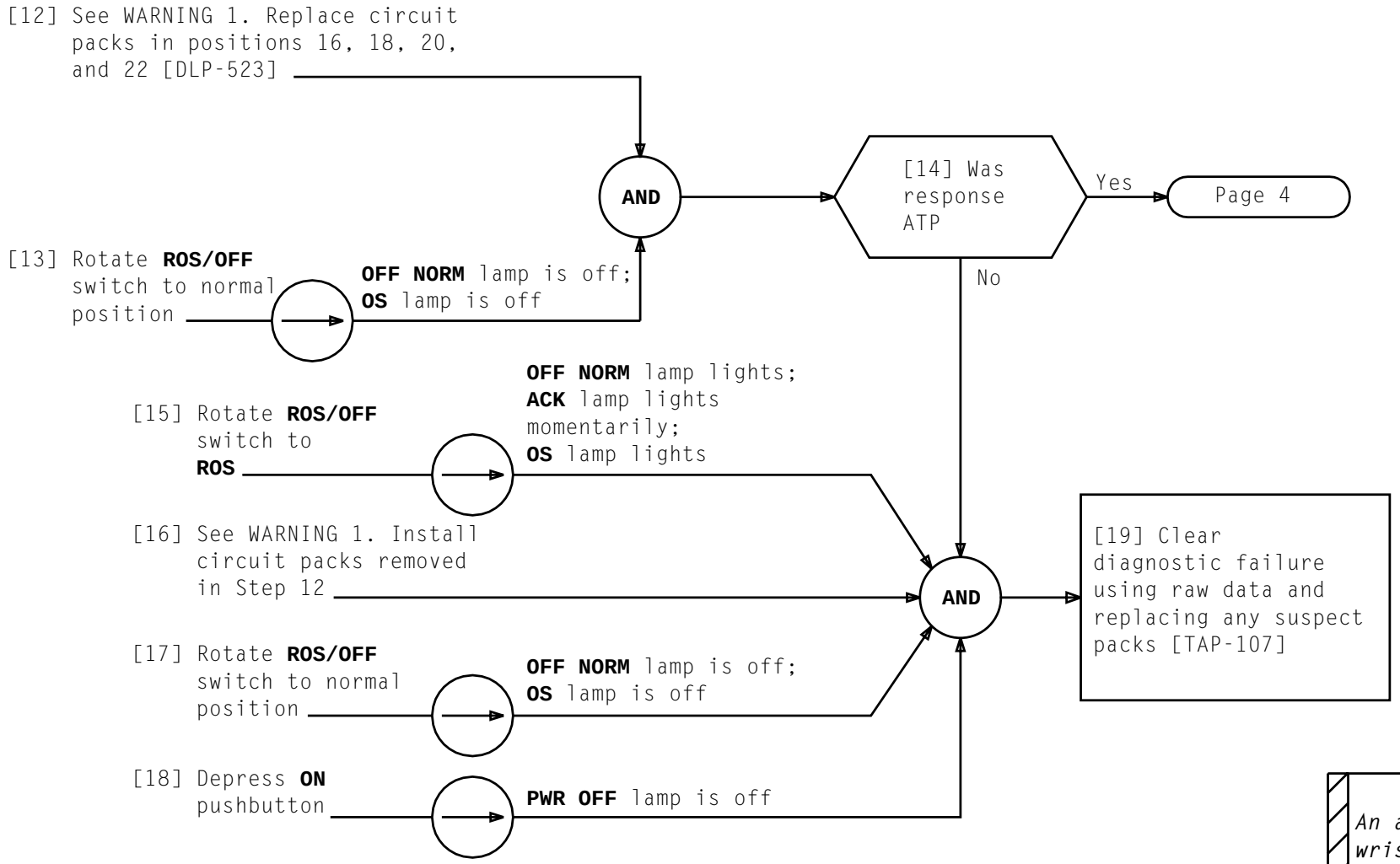
FAULTY DATA BITS	MEMORY PLANE	CIRCUIT PACKS			LOC
		1400 ns	700 ns	ECS	
0-3	MP 1	**FE66**	**FE68**	**FE68**	1
4-7	MP 2	↕	↕	↕	3
8-11	MP 3				5
12-15	MP 4				7
16-19	MP 5				9
20-23	MP 6	**FE66**	**FE68**	**FE68**	11
24-25	MP 7	**FE67**	**FE69**	**FE69**	13

NOTE: ECS and 700 ns memory packs are the same type packs

ADDRESS BIT	COUNT	DATA BIT	ERROR SUMMARY WORD 1	WORD 0	
0	0(0)	0	0	0	
1	0(0)	1	0	0	
2	0(0)	2	0	0	
3	0(0)	3	0	0	
4	0(0)	4	0	0	
5	0(0)	5	0	0	
6	0(0)	6	0	0	
7	0(0)	7	0	0	
8	0(0)	8	0	0	
9	0(0)	9	0	0	
10	0(0)	10	0	0	
11	0(0)	11	0	0	
12	1(1)	12	0	1	FAULTY DATA BITS
13	1(1)	13	0	1	
14	1(1)	14	0	1	
15	1(1)	15	0	1	
16	0(0)	16	0	0	
17	0(0)	17	0	0	
		18	0	0	
		19	0	0	
		20	0	0	
		21	0	0	
		22	0	0	
		23	0	0	
		24	0	0	PARITY 2
		25	0	0	PARITY 1

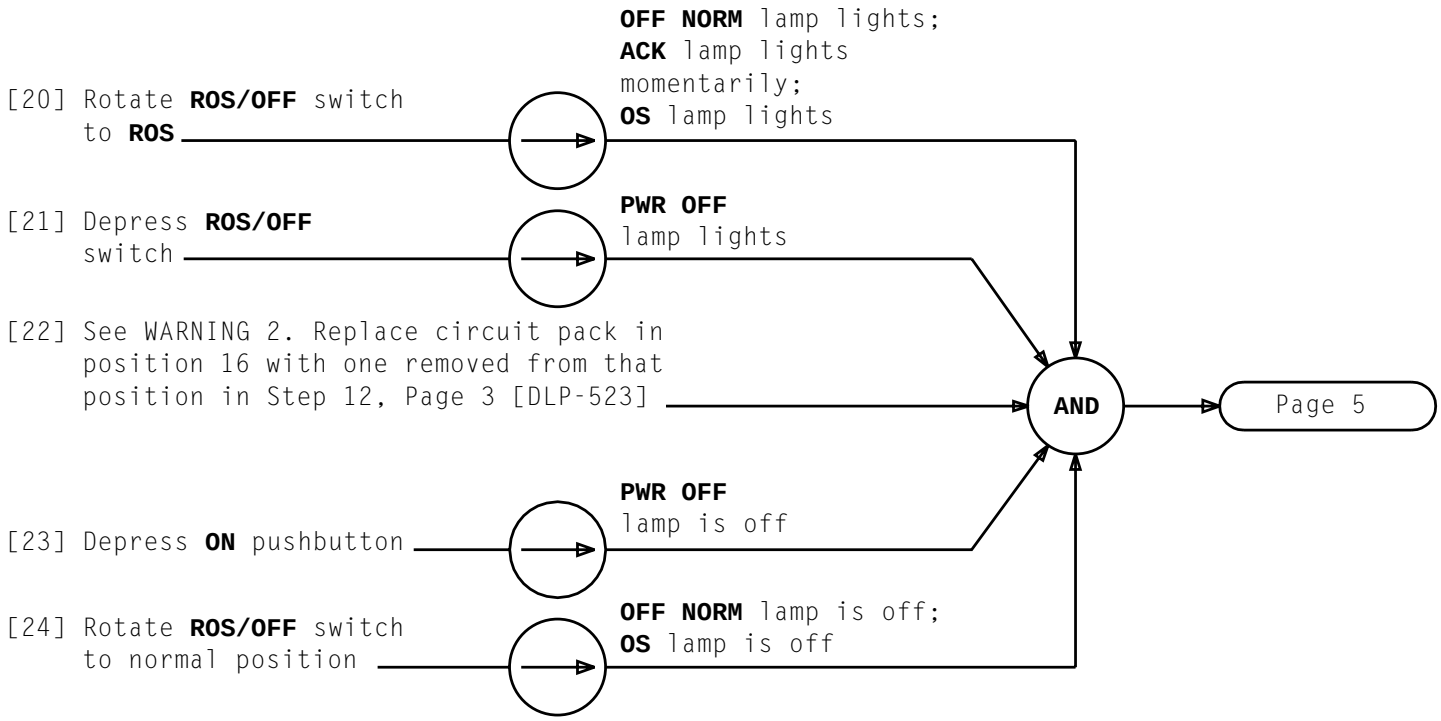
FIG. 1 — Sample of Histogram Printout

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



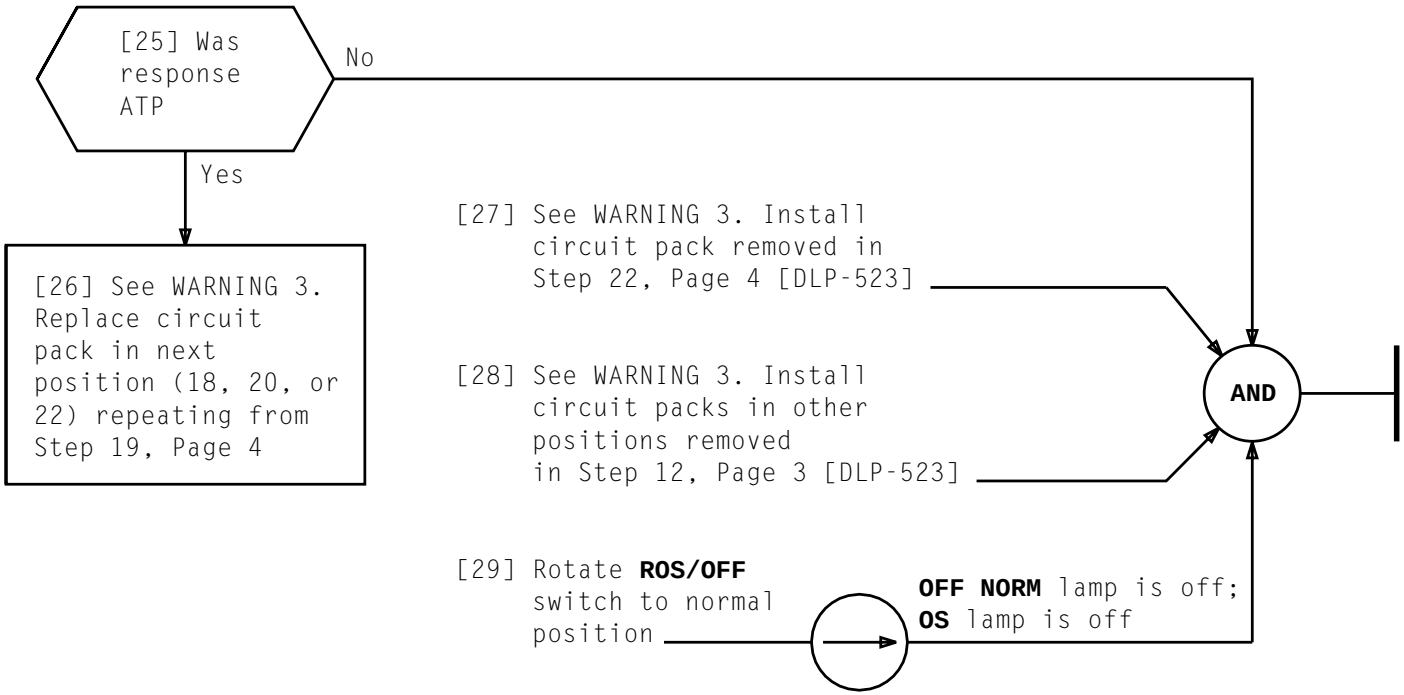
WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit packs while handling

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



WARNING 2
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit packs while handling

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



WARNING 3
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit packs while handling

CLEAR DIAGNOSTIC FAILURE USING HISTOGRAM, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

CLEAR DIAGNOSTIC FAILURE, TLP TAPE ACQUISITION ERROR

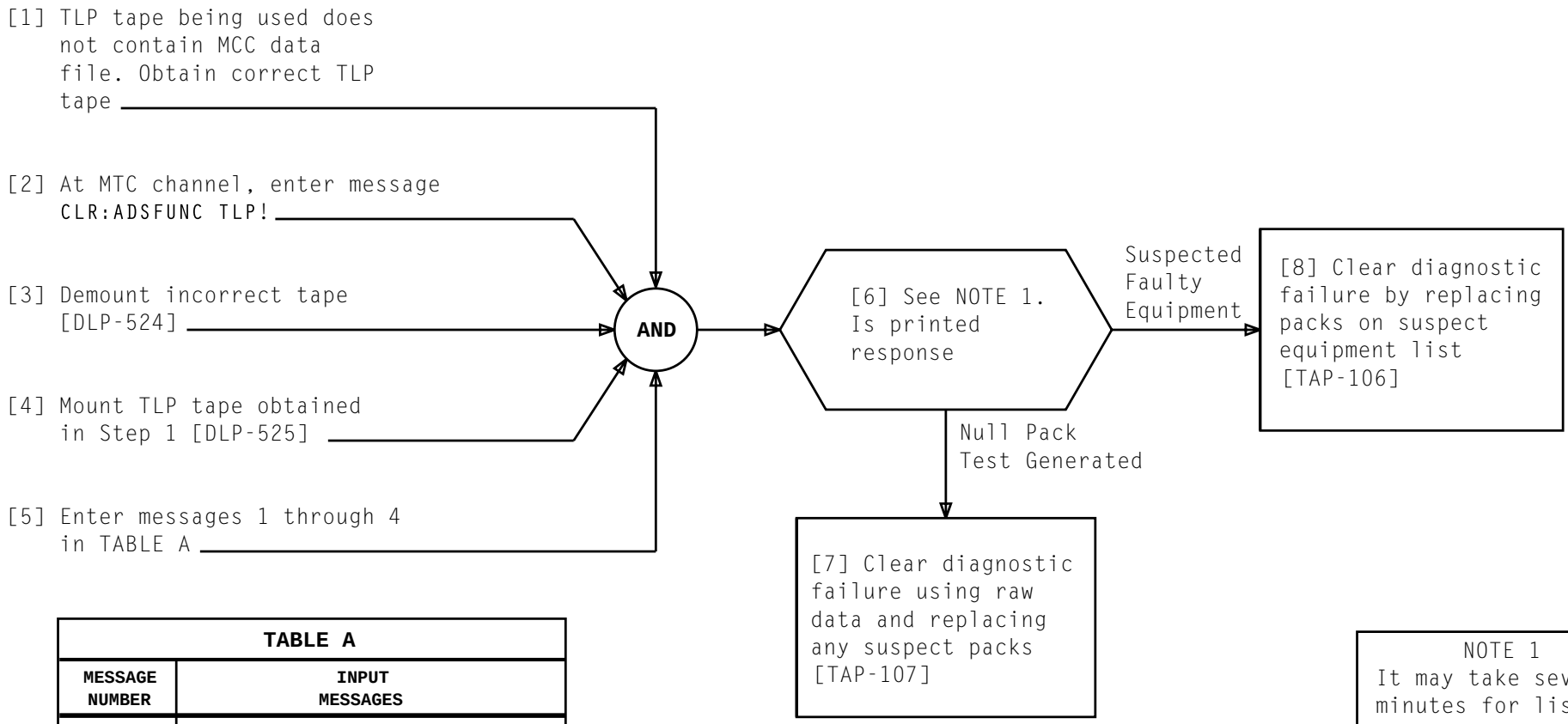


TABLE A

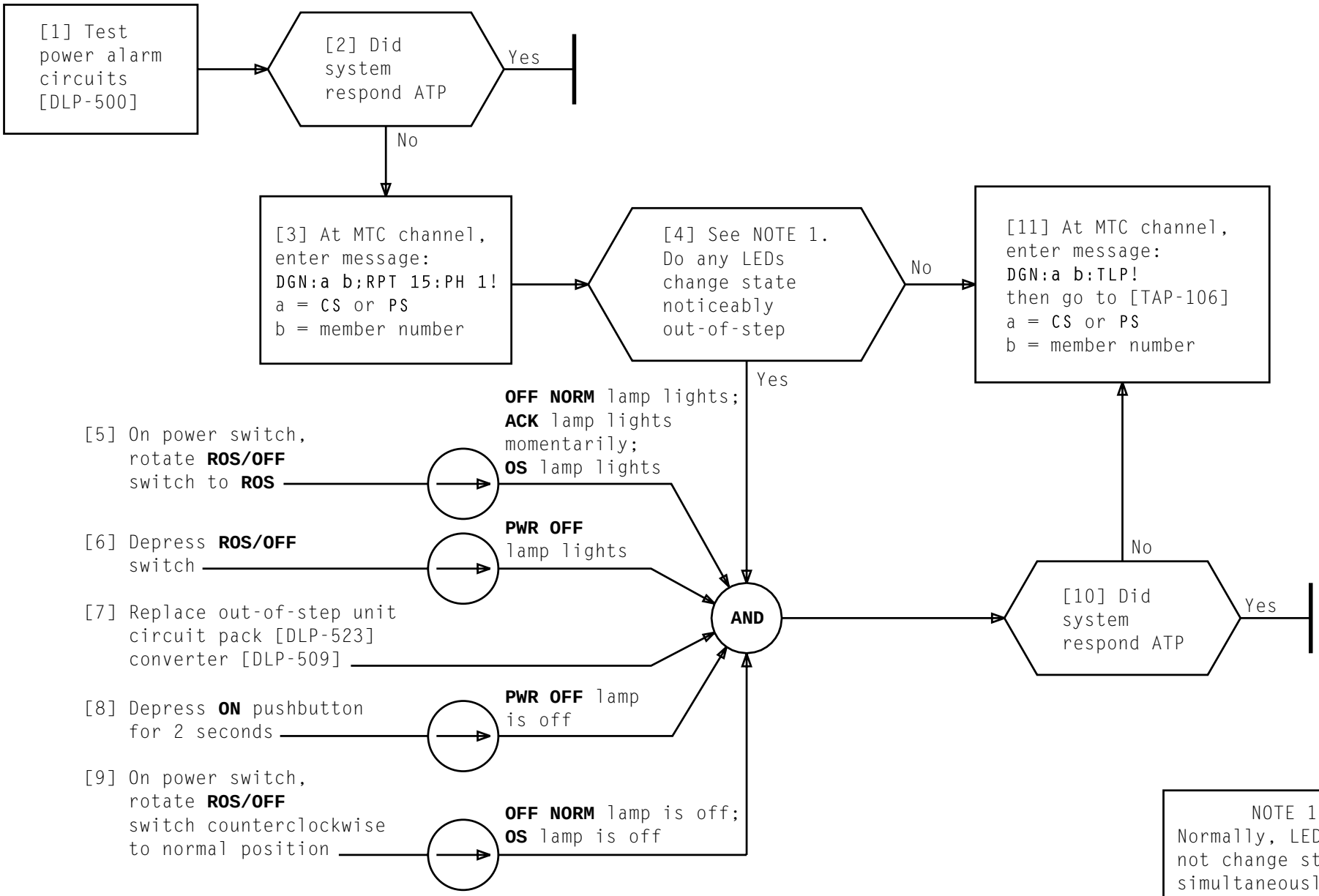
MESSAGE NUMBER	INPUT MESSAGES
1	SET:TUC a;FUNCTION TLP!
2	ALW:TUC a:RO!
3	ALW:TLP:SRCH,b!
4	DGN:b c:TLP!

a = member number of TUC with TLP tape mounted
b = CS or PS
c = member number

NOTE 1
It may take several minutes for list to print. Status of file may be monitored by entering message:

OP:TLPQUEUE;ALL!

TLP file currently being processed is indicated by asterisk in priority column



CLEAR AUTOMATIC POWER MONITOR TEST FAILURE
64K SEMICONDUCTOR STORE J5A008A

NOTE 1
Normally, LEDs do not change state simultaneously

CLEAR BABBLING CALL STORE/PROGRAM STORE BUS

[1] Does output message on printout indicate babbling is possible. TABLE A

No

Yes

[2] At power switch for store listed on printout, rotate **ROS/OFF** switch to **ROS** (**OS** lamp lighted and **OFF NORM** lamp lights)

[3] Depress the **ROS/OFF** switch (**PWR OFF** lamp lights). Output message on printout indicated per TABLE B

[4] Can probable cause be determined

Yes

[6] Is probable cause in other than store listed on prinout

Yes

No

No

No

[5] Using PCRV B-ENTRY/B-FAILED printout, determine probable cause [AT&T 234-151-003]

[7] Replace circuit packs FE66 and FE67 or FE68 and FE69 for store

Page 2

[10] Refer problem to next higher level of support

[8]At power switch for store, depress **ON** pushbutton for 2 seconds (**PWR OFF** lamp goes off)

[9] Rotate **ROS/OFF** to normal position (**OS** and **OFF NORM** lamps go off). Repeat from Step 1

TABLE A

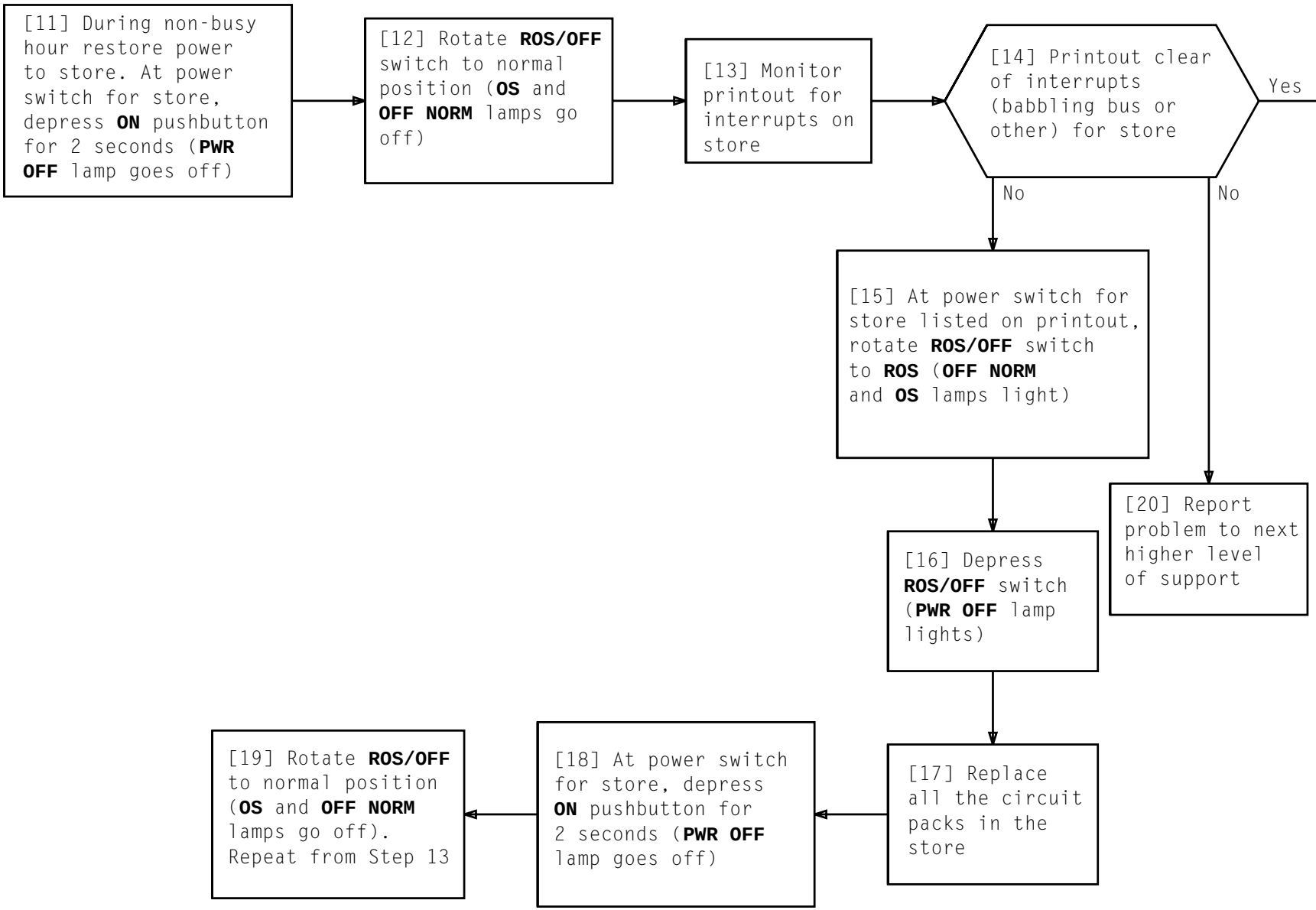
REPT: POWER DOWN a b
a b FORCED OOS - a BABBLING MAY BE POSSIBLE

a = CS or PS
b = Member number

TABLE B

REPT: a b FORCED OOS - a b BABBLING MAY BE POSSIBLE
DO NOT ATTEMPT RESTORE UNTIL SYSTEM FAULT HAS BEEN IDENTIFIED

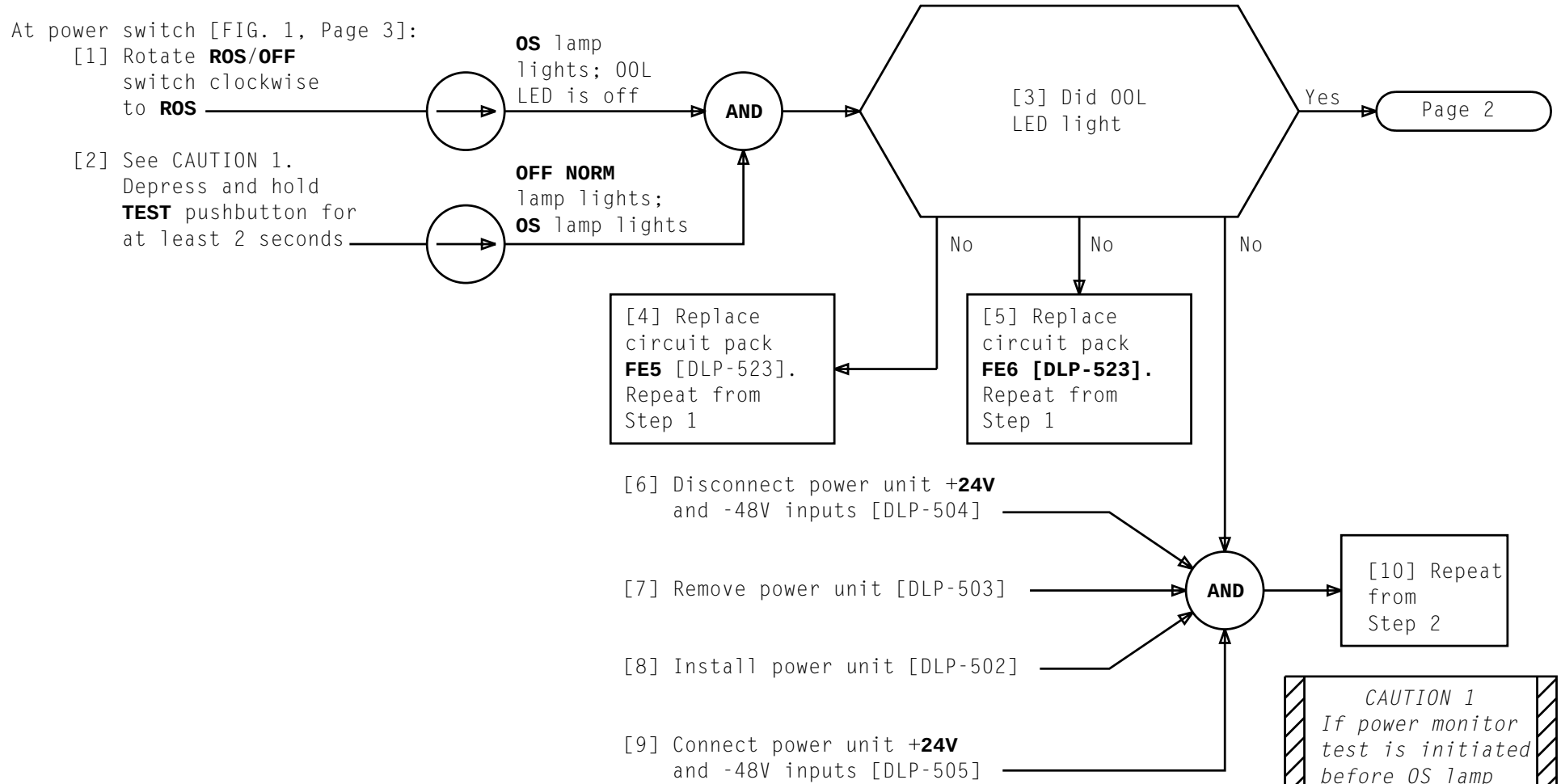
a = CS or PS
b = Member number



CLEAR BABBLING CALL STORE/PROGRAM STORE BUS

SUMMARY

Remove power; when OOL LED lights, restore power. Depress switch on **136D** converter; LEDs on **136D** and **136E** converters light. Push converter switch to up position and depress **ROS/OFF** switch. Depress **ON** pushbutton and return store to service



CAUTION 1
If power monitor test is initiated before OS lamp lights, INBUS may cause interrupt

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 1 of 3	**500**

TEST MANUAL POWER ALARM, SEMICONDUCTOR STORE J5A008A

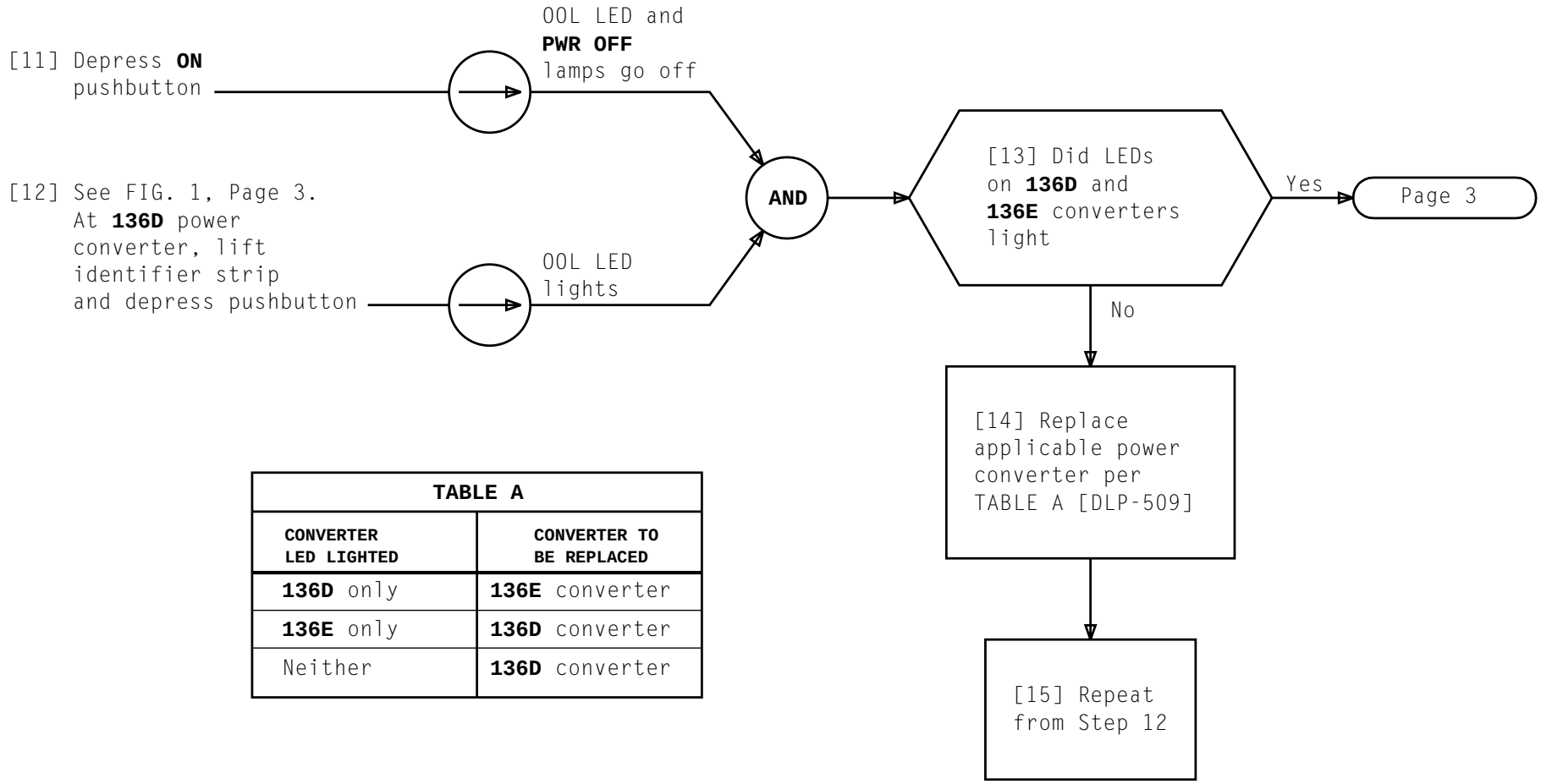


TABLE A

CONVERTER LED LIGHTED	CONVERTER TO BE REPLACED
136D only	**136E** converter
136E only	**136D** converter
Neither	**136D** converter

TEST MANUAL POWER ALARM, SEMICONDUCTOR STORE J5A008A

[16] Push switch up on **136D** converter and ensure unit is locked in

[17] At power switch, depress **ROS/OFF** switch

[18] Depress **ON** pushbutton momentarily

[19] Rotate **ROS/OFF** switch counterclockwise to normal position to return to service

PWR OFF lamp lights

OOL LED goes off

All lamps are off

AND

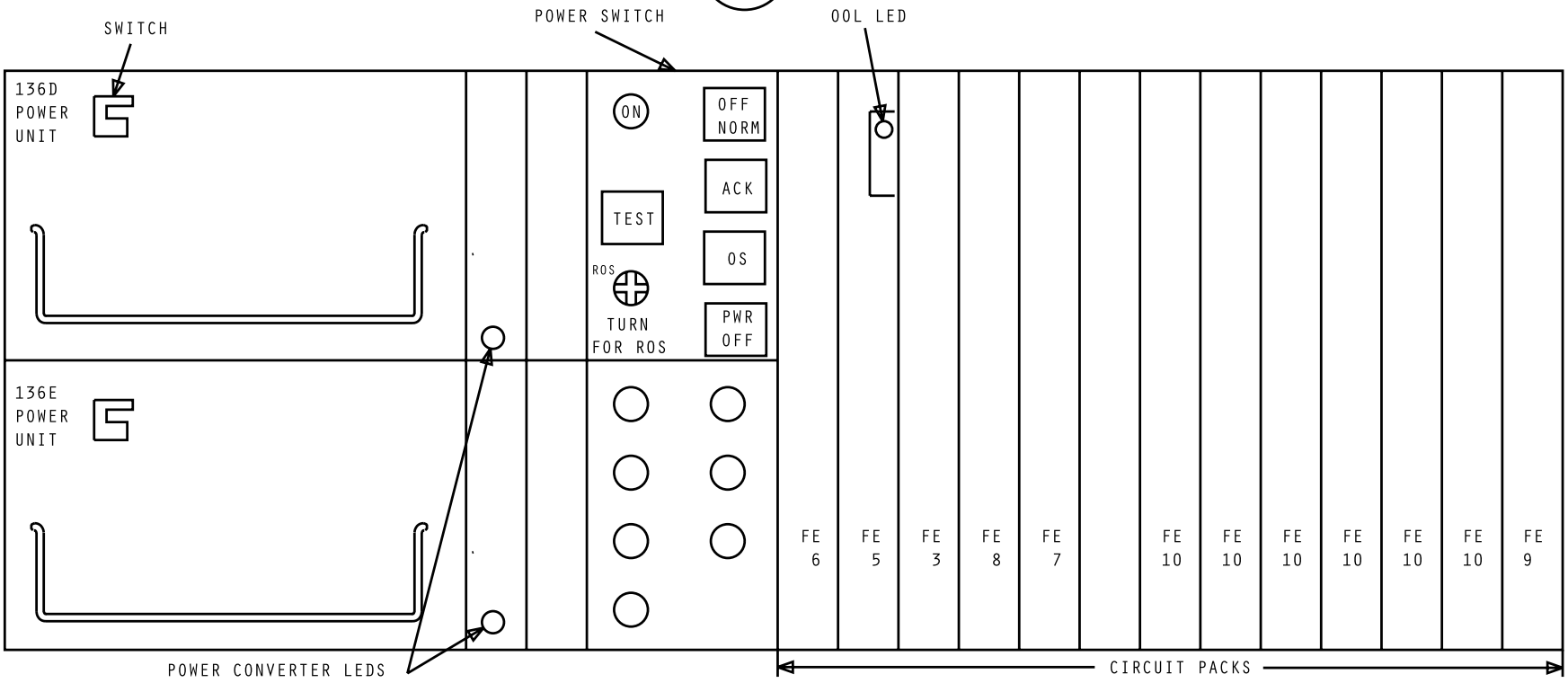
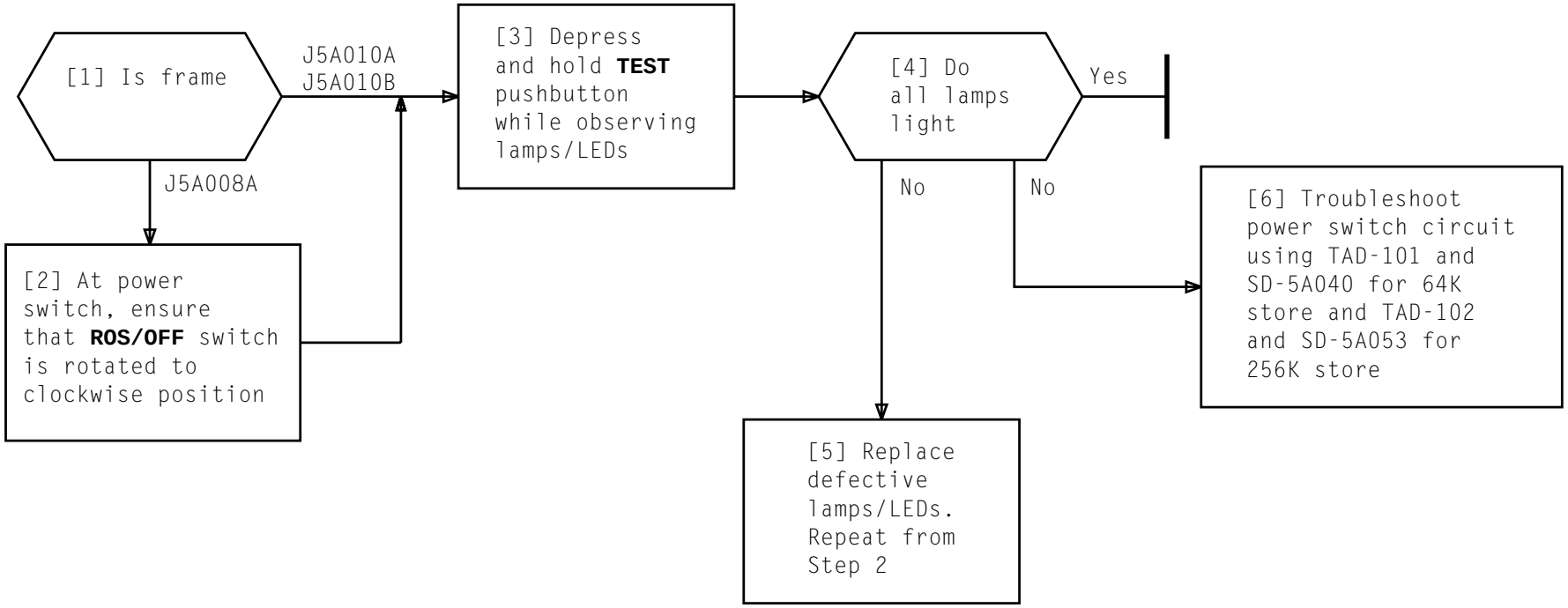


FIG. 1 — Front View Semiconductor Store

TEST MANUAL POWER ALARM, SEMICONDUCTOR STORE J5A008A



TEST LAMPS ON POWER SWITCH

At front of store:

[1] Place power unit into position using care feeding paddle boards and power leads through access hole of mounting plate

At rear of store [FIG. 1]:

[2] With power unit being supported from front, screw retaining screws into place

AND

[3] Connect power leads extending through access hole to terminal board

[4] Connect paddle boards per **EQL** stamped on side

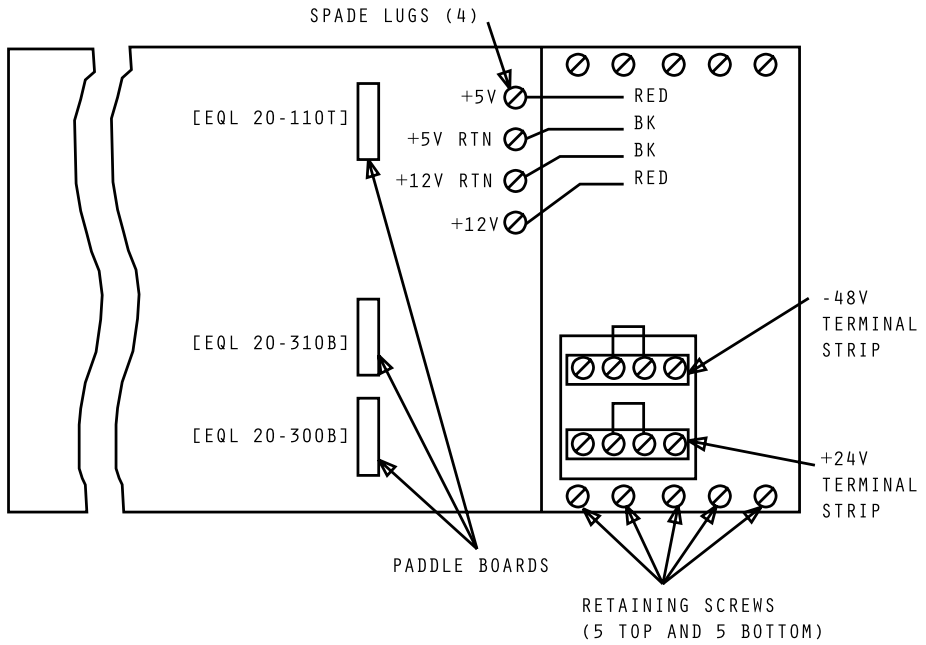


FIG. 1 — Rear View of Semiconductor Store, J5A008A

INSTALL POWER UNIT, SEMICONDUCTOR STORE J5A008A

Issue 7	NOV 1993
254-251-005	DLP
PAGE 1 of 1	502

REMOVE POWER UNIT, SEMICONDUCTOR STORE J5A008A

At rear of store unit [FIG. 1]:

[1] Disconnect paddleboards using 793A tool; note **EQL** of each connector

[2] Disconnect power leads extending from access hole

AND

At front of store:

[3] Remove **136D** power converter by depressing locking switch and pulling out with handle

[4] Remove **136E** power converter by depressing locking switch and pulling out with handle

AND

At rear of store:

[5] See WARNING 1. Remove mounting screws supporting power unit

[6] As unit is being removed, carefully feed cables through access hole

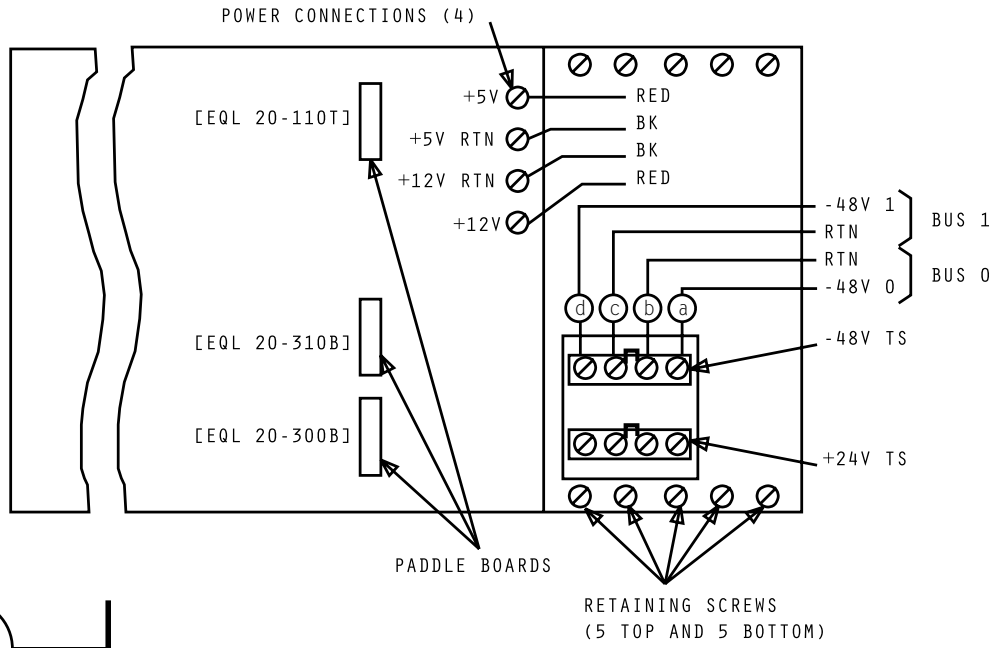
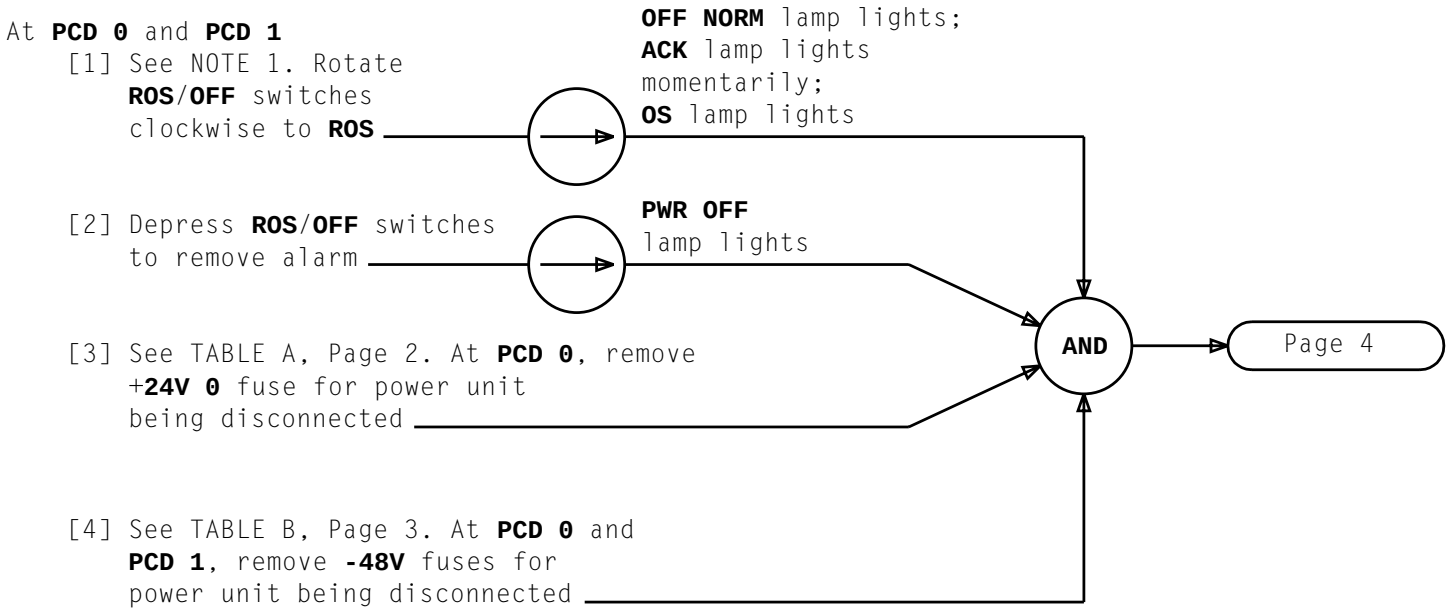


FIG. 1 — Rear View of Semiconductor Store J5A008A

WARNING 1
Power unit should be supported on front side of bay while removing retaining screws to prevent damage to power unit and surrounding equipment

SUMMARY	
For J5A008A frame; at **PCD 0**, remove +**24V 0** a**nd -48V 0** fuses; at **PCD 1**, remove **-48V 1** fuse. Remove power leads at rear of unit. If even store is being removed, +**24V** leads	going to odd store should be spliced to maintain power. Disconnect +**24V BUS 0**, then +**24V BUS 1,** then remove **-48V** leads



NOTE 1
Removal of power at **PCD 0** and **PCD 1** switches removes the audible power alarm capabilities only

DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

TABLE A							
STORE	PCD FUSE DESIGNATION	+24V BUS 0 PCD 0 FUSE POSITION	+24V BUS 1 PCD 1 FUSE POSITION	STORE	PCD FUSE DESIGNATION	+24V BUS 0 PCD 0 FUSE POSITION	+24V BUS 1 PCD 1 FUSE POSITION
CS 00, CS 01	**CS00**	123-15, 9	123-29, 9	CS 36, CS 37	**CS36**	128-15, 11	128-29, 11
CS 02, CS 03	**CS02**	123-15, 10	123-29, 10	CS 38, CS 39	**CS38**	128-15, 12	128-29, 12
CS 04, CS 05	**CS04**	123-15, 11	123-29, 11	CS 40, CS 41	**CS40**	128-15, 13	128-29, 13
CS 06, CS 07	**CS06**	123-15, 12	123-29, 12	CS 42, CS 43	**CS42**	128-15, 14	128-29, 14
CS 08, CS 09	**CS08**	123-15, 13	123-29, 13	CS 44, CS 45	**CS44**	128-15, 15	128-29, 15
CS 10, CS 11	**CS10**	123-15, 14	123-29, 14	CS 46, CS 47	**CS46**	128-15, 16	128-29, 16
CS 12, CS 13	**CS12**	123-15, 15	123-29, 15	PS 00, PS 01	**PS00**	118-15, 9	118-29, 9
CS 14, CS 15	**CS14**	123-15, 16	123-29, 16	PS 02, PS 03	**PS02**	118-15, 10	118-29, 10
CS 16, CS 17	**CS16**	123-15, 1	123-29, 1	PS 04, PS 05	**PS04**	118-15, 11	118-29, 11
CS 18, CS 19	**CS18**	123-15, 2	123-29, 2	PS 06, PS 07	**PS06**	118-15, 12	118-29, 12
CS 20, CS 21	**CS20**	123-15, 3	123-29, 3	PS 08, PS 09	**PS08**	118-15, 13	118-29, 13
CS 22, CS 23	**CS22**	123-15, 4	123-29, 4	PS 10, PS 11	**PS10**	118-15, 14	118-29, 14
CS 24, CS 25	**CS24**	123-15, 5	123-29, 5	PS 12, PS 13	**PS12**	118-15, 15	118-29, 15
CS 26, CS 27	**CS26**	123-15, 6	123-29, 6	PS 14, PS 15	**PS14**	118-15, 16	118-29, 16
CS 28, CS 29	**CS28**	123-15, 7	123-29, 7	PS 16, PS 17	**PS16**	118-15, 1	118-29, 1
CS 30. CS 31	**CS30**	123-15, 8	123-29, 8	PS 18, PS 19	**PS18**	118-15, 2	118-29, 2
CS 32, CS 33	**CS32**	128-15, 9	128-29, 9	PS 20, PS 21	**PS20**	118-15, 3	118-29, 3
CS 34, CS 35	**CS34**	128-15, 10	128-29, 10	PS 22, PS 23	**PS22**	118-15, 4	118-29, 4

DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

TABLE B

PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION
CS00	164-15, 3	164-29, 3	**CS18**	169-15, 4	169-29, 4	**CS36**	174-15, 5	174-29, 5	**PS06**	159-15, 4	159-29, 4
CS01	164-15, 11	164-29, 11	**CS19**	169-15, 12	169-29, 12	**CS37**	174-15, 13	174-29, 13	**PS07**	159-15, 12	159-29, 12
CS02	164-15, 4	164-29, 4	**CS20**	169-15, 5	169-29, 5	**CS38**	174-15, 6	174-29, 6	**PS08**	159-15, 5	159-29, 5
CS03	164-15, 12	164-29, 12	**CS21**	169-15, 13	169-29, 13	**CS39**	174-15, 14	174-29, 14	**PS09**	159-15, 13	159-29, 13
CS04	164-15, 5	164-29, 5	**CS22**	169-15, 6	169-29, 6	**CS40**	174-15, 7	174-29, 7	**PS10**	159-15, 6	159-29, 6
CS05	164-15, 13	164-29, 13	**CS23**	169-15, 14	169-29, 14	**CS41**	174-15, 15	174-29, 15	**PS11**	159-15, 14	159-29, 14
CS06	164-15, 6	164-29, 6	**CS24**	169-15, 7	169-29, 7	**CS42**	174-15, 8	174-29, 8	**PS12**	159-15, 7	159-29, 7
CS07	164-15, 14	164-29, 14	**CS25**	169-15, 15	169-29, 15	**CS43**	174-15, 16	174-29, 16	**PS13**	159-15, 15	159-29, 15
CS08	164-15, 7	164-29, 7	**CS26**	169-15, 8	169-29, 8	**CS44**	179-15, 3	179-29, 3	**PS14**	159-15, 8	159-29, 8
CS09	164-15, 15	164-29, 15	**CS27**	169-15, 16	169-29, 16	**CS45**	179-15, 11	179-29, 11	**PS15**	159-15, 16	159-29, 16
CS10	164-15, 8	164-29, 8	**CS28**	174-15, 1	174-29, 1	**CS46**	179-15, 4	179-29, 4	**PS16**	164-15, 1	164-29, 1
CS11	164-15, 16	164-29, 16	**CS29**	174-15, 9	174-29, 9	**CS47**	179-15, 12	179-29, 12	**PS17**	164-15, 9	164-29, 9
CS12	169-15, 1	169-29, 1	**CS30**	174-15, 2	174-29, 2	**PS00**	159-15, 1	159-29, 1	**PS18**	164-15, 2	164-29, 2
CS13	169-15, 9	169-29, 9	**CS31**	174-15, 10	174-29, 10	**PS01**	159-15, 9	159-29, 9	**PS19**	164-15, 10	164-29, 10
CS14	169-15, 2	169-29, 2	**CS32**	174-15, 3	174-29, 3	**PS02**	159-15, 2	159-29, 2	**PS20**	179-15, 5	179-29, 5
CS15	169-15, 10	169-29, 10	**CS33**	174-15, 11	174-29, 11	**PS03**	159-15, 10	159-29, 10	**PS21**	179-15, 13	179-29, 13
CS16	169-15, 3	169-29, 3	**CS34**	174-15, 4	174-29, 4	**PS04**	159-15, 3	159-29, 3	**PS22**	179-15, 6	179-29, 6
CS17	169-15, 11	169-29, 11	**CS35**	174-15, 12	174-29, 12	**PS05**	159-15, 11	159-29, 11	**PS23**	179-15, 14	179-29, 14

* PCD fuse designation and store designation are the same

DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

[5] See FIG. 1. Are power leads being removed from even or odd number store

Odd

Even

At rear of store:

[10] See Figure 2. Remove **+24V 0** B-lead and insulate with electrical tape

[11] Tag lead to identify and clear from terminal area

[12] Remove **+24V 0** ground D-lead and insulate with electrical tape

[13] Tag ground lead and clear from terminal area

AND

At rear of store:

[6] See FIG. 2. Remove **+24V 0** A and B leads; connect together using number 6 screw and nut; insulate with electrical tape

[7] Tag leads to identify and clear from terminal area

[8] Remove **+24V 0** ground C and D leads; connect together using number 6 screw and nut; insulate with electrical tape

[9] Tag leads to identify and clear from terminal area

AND

Page 5

STORE 0
STORE 1
STORE 2
STORE 3
STORE 4
STORE 5

FIG. 1 — Store Frame Number System

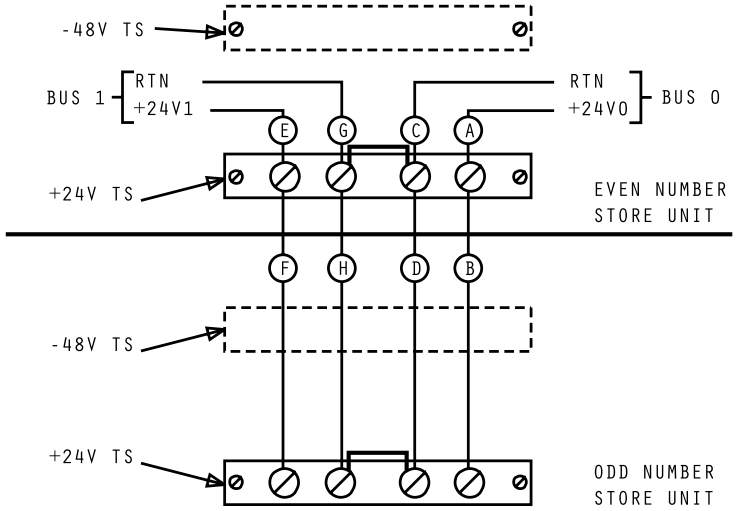
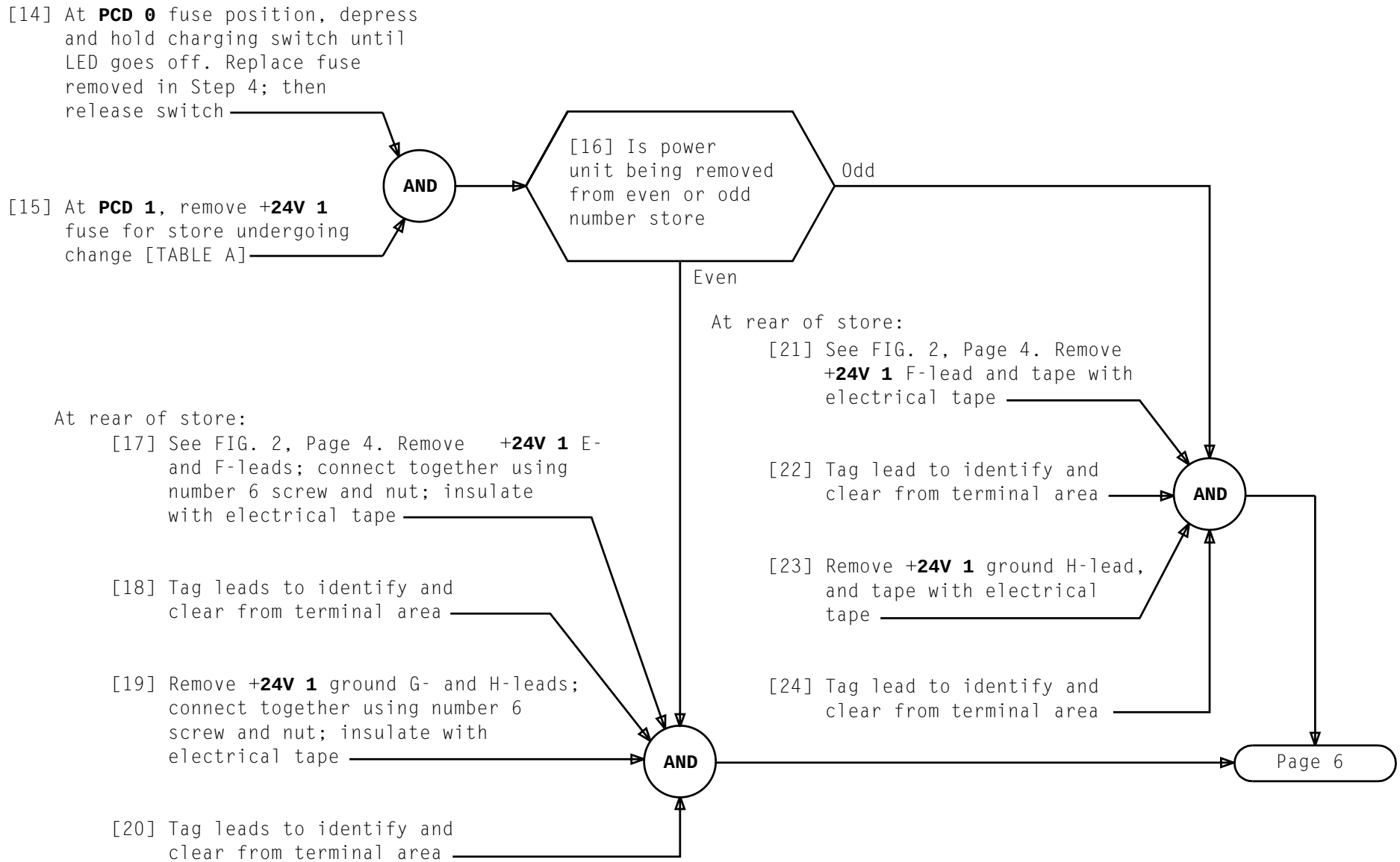


FIG. 2 — +24V Terminal Strip Connections

DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A



DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

[25] At **PCD 1** fuse position, depress and hold charging switch until LED goes off. Replace fuse removed in Step 18, then release switch

At rear of store:

[26] See FIG. 3. Remove **-48V 0** A-lead, tape and tag to identify

[27] Remove **-48V 0** RTN B-lead, tape and tag to identify

[28] Remove **-48V 1** D-lead, tape and tag to identify

[29] Remove **-48V 1** RTN C-lead, tape and tag to identify

[30] Remove all leads from terminal area

AND

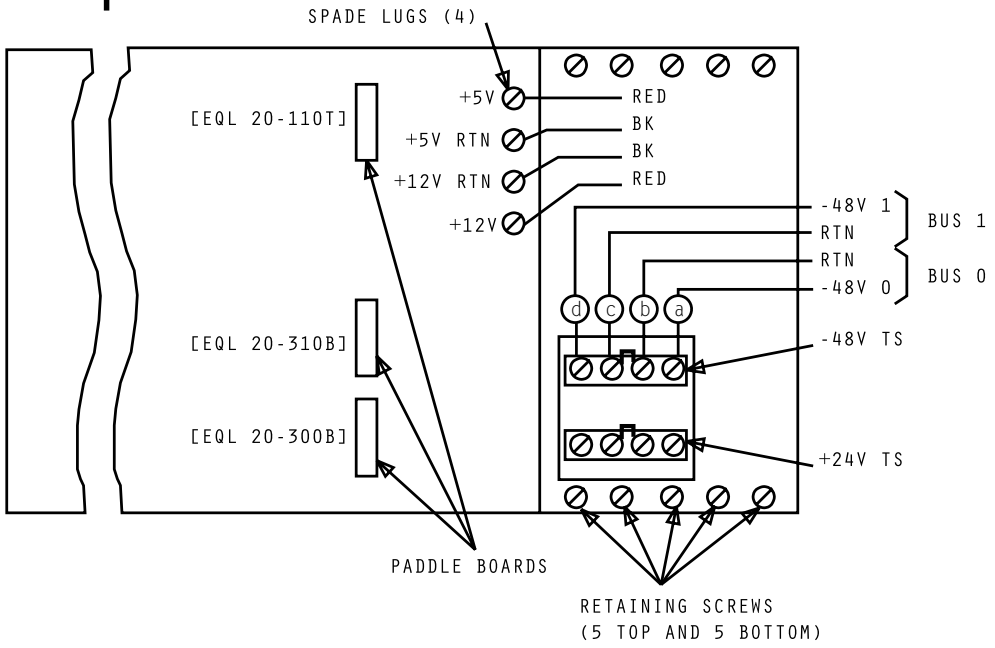


FIG. 3 – Rear View of Semiconductor Store J5A008A

DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

SUMMARY

For J5A008A frame: connect **-48V** leads, remove **PCD 0** +**24V 0** fuse and connect +**24V 0** leads. Replace **PCD 0** fuse and remove **PCD 1** +**24V 1** fuse. Connect +**24V 1** leads and install converters. Replace +**24V 1** fuse and **-48V** fuses at **PCD 0** and **PCD 1**. Restore **PCD 0** and **PCD 1** to service

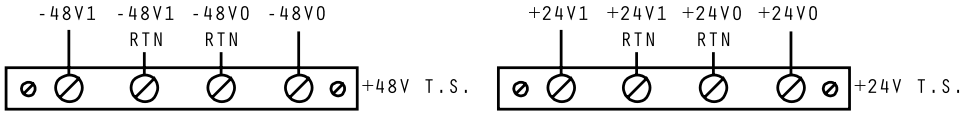


FIG. 1 — -48V and +24V Connections

At rear of store:

[1] See FIG. 1. Untape and connect **-48V 0** ground lead to terminal strip

[2] Untape and connect **-48V 0** lead to terminal strip

[3] Untape and connect **-48V 1** ground lead to terminal strip

[4] Untape and connect **-48V 1** lead to terminal strip

At **PCD 0:**

[5] See TABLE A, Page 2. Remove +**24V 0** fuse for store that power unit is being connected

AND

[6] Is store an even or odd number store [Figure 2]

Odd

Even

At rear of store:

[7] See FIG. 1. Untape +**24V 0** ground lead and connect to terminal strip

AND

[8] Untape +**24V 0** lead and connect to terminal strip

Page 3

At rear of store:

[9] See FIG. 1. Untape and disconnect spliced +**24V 0** ground leads and connect to terminal strip

[10] Untape and disconnect spliced +**24V 0** leads and connect to terminal strip

AND

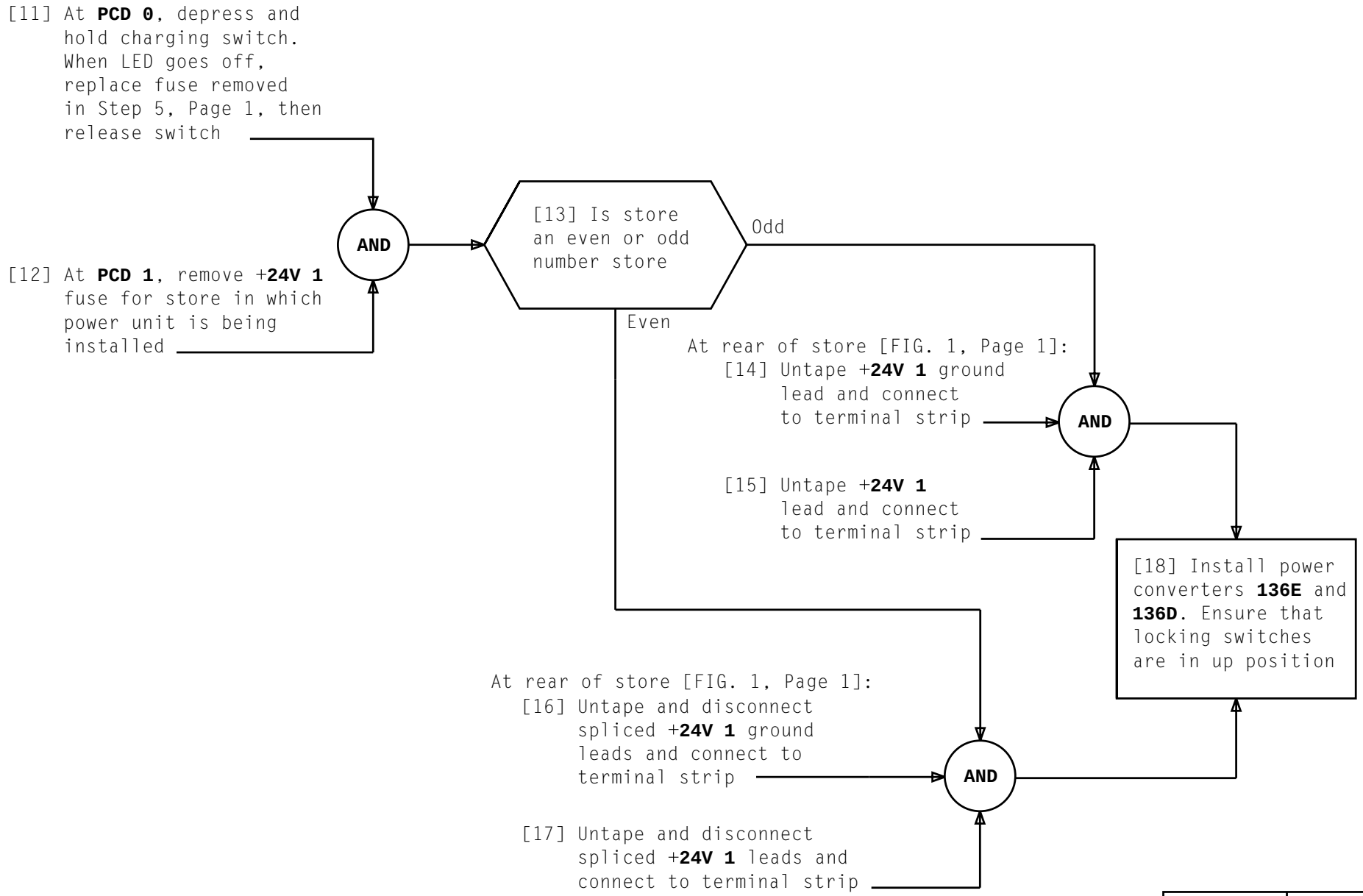
Page 3

FIG. 2 — Store Number System

CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

TABLE A							
STORE	PCD FUSE DESIGNATION	+24V BUS 0 PCD 0 FUSE POSITION	+24V BUS 1 PCD 1 FUSE POSITION	STORE	PCD FUSE DESIGNATION	+24V BUS 0 PCD 0 FUSE POSITION	+24V BUS 1 PCD 1 FUSE POSITION
CS 00, CS 01	**CS00**	123-15, 9	123-29, 9	CS 36, CS 37	**CS36**	128-15, 11	128-29, 11
CS 02, CS 03	**CS02**	123-15, 10	123-29, 10	CS 38, CS 39	**CS38**	128-15, 12	128-29, 12
CS 04, CS 05	**CS04**	123-15, 11	123-29, 11	CS 40, CS 41	**CS40**	128-15, 13	128-29, 13
CS 06, CS 07	**CS06**	123-15, 12	123-29, 12	CS 42, CS 43	**CS42**	128-15, 14	128-29, 14
CS 08, CS 09	**CS08**	123-15, 13	123-29, 13	CS 44, CS 45	**CS44**	128-15, 15	128-29, 15
CS 10, CS 11	**CS10**	123-15, 14	123-29, 14	CS 46, CS 47	**CS46**	128-15, 16	128-29, 16
CS 12, CS 13	**CS12**	123-15, 15	123-29, 15	PS 00, PS 01	**PS00**	118-15, 9	118-29, 9
CS 14, CS 15	**CS14**	123-15, 16	123-29, 16	PS 02, PS 03	**PS02**	118-15, 10	118-29, 10
CS 16, CS 17	**CS16**	123-15, 1	123-29, 1	PS 04, PS 05	**PS04**	118-15, 11	118-29, 11
CS 18, CS 19	**CS18**	123-15, 2	123-29, 2	PS 06, PS 07	**PS06**	118-15, 12	118-29, 12
CS 20, CS 21	**CS20**	123-15, 3	123-29, 3	PS 08, PS 09	**PS08**	118-15, 13	118-29, 13
CS 22, CS 23	**CS22**	123-15, 4	123-29, 4	PS 10, PS 11	**PS10**	118-15, 14	118-29, 14
CS 24, CS 25	**CS24**	123-15, 5	123-29, 5	PS 12, PS 13	**PS12**	118-15, 15	118-29, 15
CS 26, CS 27	**CS26**	123-15, 6	123-29, 6	PS 14, PS 15	**PS14**	118-15, 16	118-29, 16
CS 28, CS 29	**CS28**	123-15, 7	123-29, 7	PS 16, PS 17	**PS16**	118-15, 1	118-29, 1
CS 30, CS 31	**CS30**	123-15, 8	123-29, 8	PS 18, PS 19	**PS18**	118-15, 2	118-29, 2
CS 32, CS 33	**CS32**	128-15, 9	128-29, 9	PS 20, PS 21	**PS20**	118-15, 3	118-29, 3
CS 34, CS 35	**CS34**	128-15, 10	128-29, 10	PS 22, PS 23	**PS22**	118-15, 4	118-29, 4

CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A



CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

TABLE B											
PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION
CS00	164-15, 3	164-29, 3	**CS18**	169-15, 4	169-29, 4	**CS36**	174-15, 5	174-29, 5	**PS06**	159-15, 4	159-29, 4
CS01	164-15, 11	164-29, 11	**CS19**	169-15, 12	169-29, 12	**CS37**	174-15, 13	174-29, 13	**PS07**	159-15, 12	159-29, 12
CS02	164-15, 4	164-29, 4	**CS20**	169-15, 5	169-29, 5	**CS38**	174-15, 6	174-29, 6	**PS08**	159-15, 5	159-29, 5
CS03	164-15, 12	164-29, 12	**CS21**	169-15, 13	169-29, 13	**CS39**	174-15, 14	174-29, 14	**PS09**	159-15, 13	159-29, 13
CS04	164-15, 5	164-29, 5	**CS22**	169-15, 6	169-29, 6	**CS40**	174-15, 7	174-29, 7	**PS10**	159-15, 6	159-29, 6
CS05	164-15, 13	164-29, 13	**CS23**	169-15, 14	169-29, 14	**CS41**	174-15, 15	174-29, 15	**PS11**	159-15, 14	159-29, 14
CS06	164-15, 6	164-29, 6	**CS24**	169-15, 7	169-29, 7	**CS42**	174-15, 8	174-29, 8	**PS12**	159-15, 7	159-29, 7
CS07	164-15, 14	164-29, 14	**CS25**	169-15, 15	169-29, 15	**CS43**	174-15, 16	174-29, 16	**PS13**	159-15, 15	159-29, 15
CS08	164-15, 7	164-29, 7	**CS26**	169-15, 8	169-29, 8	**CS44**	179-15, 3	179-29, 3	**PS14**	159-15, 8	159-29, 8
CS09	164-15, 15	164-29, 15	**CS27**	169-15, 16	169-29, 16	**CS45**	179-15, 11	179-29, 11	**PS15**	159-15, 16	159-29, 16
CS10	164-15, 8	164-29, 8	**CS28**	174-15, 1	174-29, 1	**CS46**	179-15, 4	179-29, 4	**PS16**	164-15, 1	164-29, 1
CS11	164-15, 16	164-29, 16	**CS29**	174-15, 9	174-29, 9	**CS47**	179-15, 12	179-29, 12	**PS17**	164-15, 9	164-29, 9
CS12	169-15, 1	169-29, 1	**CS30**	174-15, 2	174-29, 2	**PS00**	159-15, 1	159-29, 1	**PS18**	164-15, 2	164-29, 2
CS13	169-15, 9	169-29, 9	**CS31**	174-15, 10	174-29, 10	**PS01**	159-15, 9	159-29, 9	**PS19**	164-15, 10	164-29, 10
CS14	169-15, 2	169-29, 2	**CS32**	174-15, 3	174-29, 3	**PS02**	159-15, 2	159-29, 2	**PS20**	179-15, 5	179-29, 5
CS15	169-15, 10	169-29, 10	**CS33**	174-15, 11	174-29, 11	**PS03**	159-15, 10	159-29, 10	**PS21**	179-15, 13	179-29, 13
CS16	169-15, 3	169-29, 3	**CS34**	174-15, 4	174-29, 4	**PS04**	159-15, 3	159-29, 3	**PS22**	179-15, 6	179-29, 6
CS17	169-15, 11	169-29, 11	**CS35**	174-15, 12	174-29, 12	**PS05**	159-15, 11	159-29, 11	**PS23**	179-15, 14	179-29, 14

* PCD fuse designation and store designation are the same

CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

[19] At **PCD 1**, depress and hold charging switch of +**24V 1** fuse removed in Step 12. When LED extinguishes, install switch fuse; then release

[20] See TABLE B, Page 4. At **PCD 0** and **PCD 1**, depress and hold charging switches of **-48V** fuses for store in which power is being connected. When LEDs extinguish, replace fuses; then release switch

At **PSA** and **PSB** power switches:

[21] Depress **ON** pushbutton → **PWR OFF** lamp off

[22] Rotate **ROS/OFF** switches counterclockwise to normal position → **OFF NORM** lamp is off; **OS** lamp is off

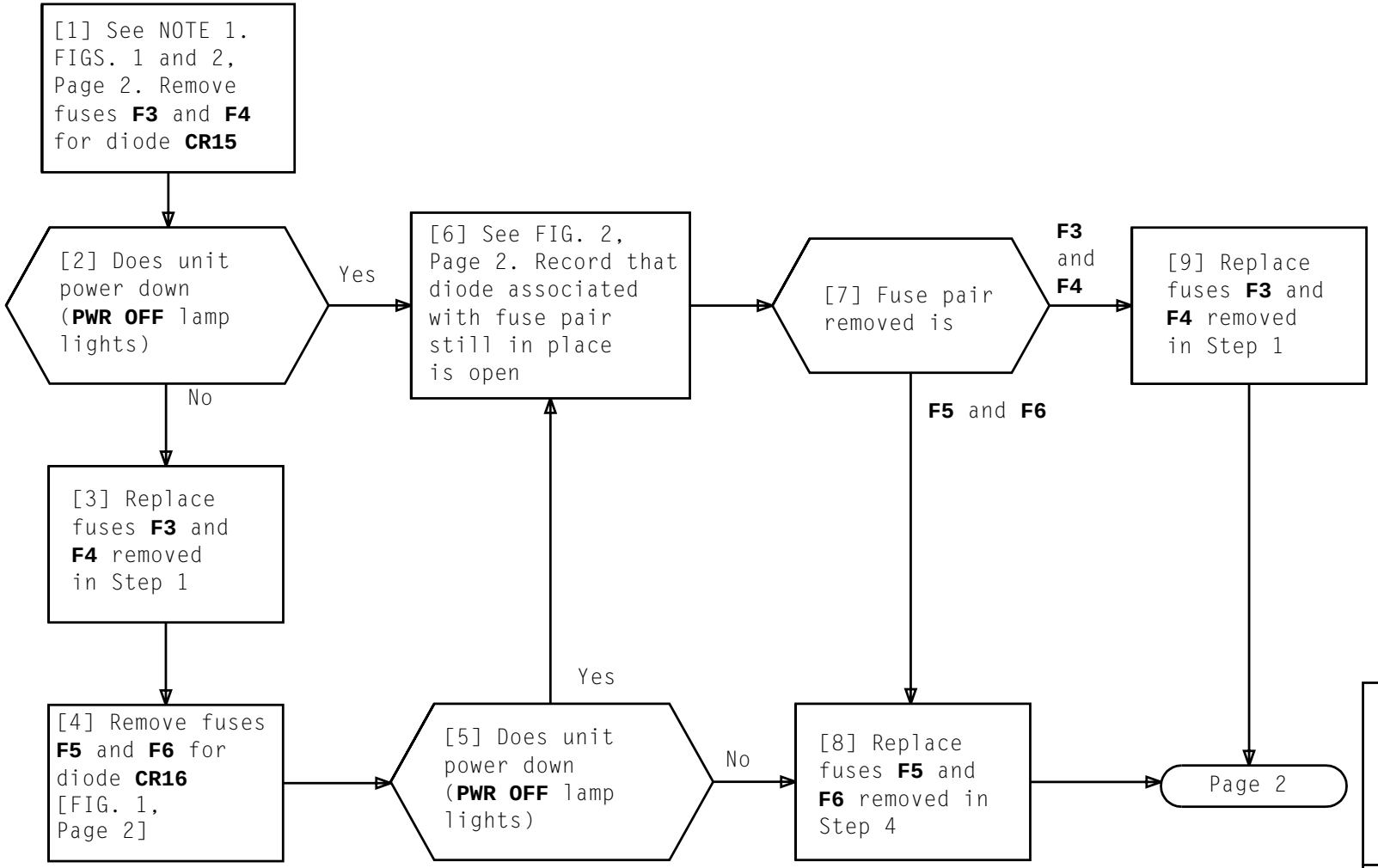
[23] At MTC channel: for each **PCD** (**0** and **1**), enter message
RST:PCD a,DAMON 0!
a = 0 or 1 → System responds
RST:PCD a DAMON 0 COMPLETED

AND

CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A008A

SUMMARY

Remove fuses **F3** and **F4**. If power stays on, replace **F3** and **F4** and remove fuses **F5** and **F6**. If unit power goes off, in either case, record that diodes of fuses in place are open. Replace last fuses removed and replace any diodes found open



NOTE 1

For fuse pair removal, indicator fuse (**F3** or **F5**) is removed first and replaced last

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 1 of 2	**506**

CHECK +24V ORED DIODES FOR OPENS, SEMICONDUCTOR STORE J5A008A

[10] See CAUTION 1. were any diodes found to be opened

No

Yes

[11] Disconnect power unit +**24V** and **-48V** input [DLP-504]

[12] Remove power unit [DLP-503]

[13] Replace open diodes [DLP-511]

[14] Install power unit back into place [DLP-502]

[15] Connect power unit +**24V** and **-48V** inputs [DLP-505]

AND

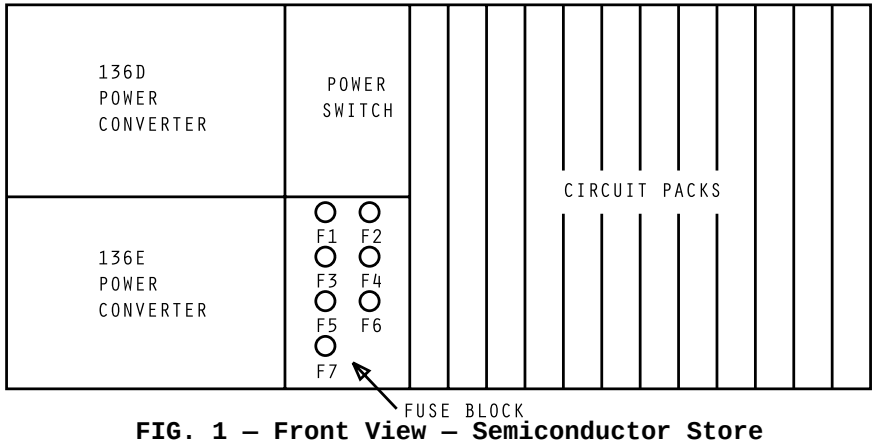
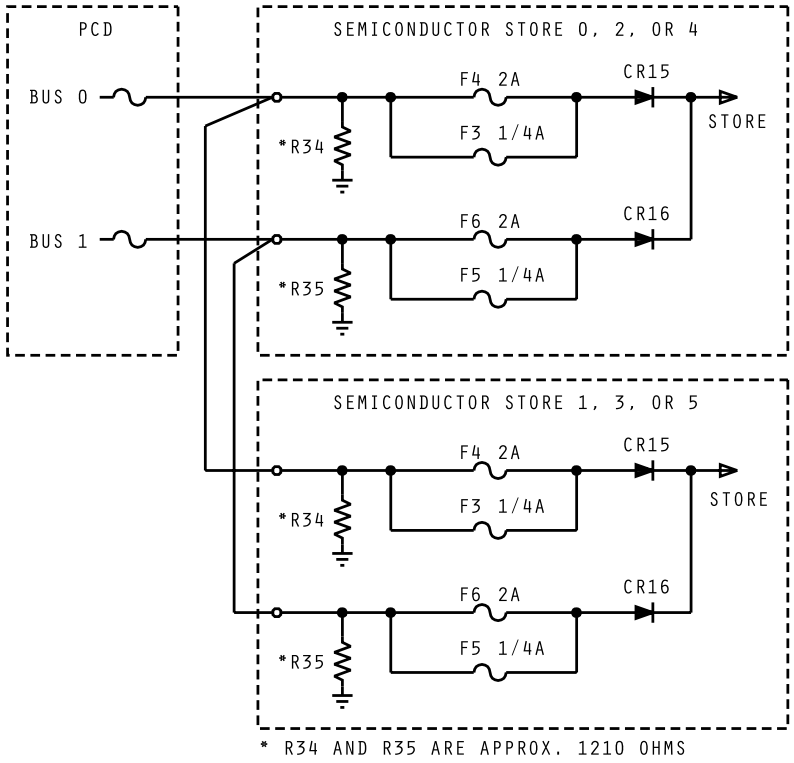


FIG. 1 — Front View — Semiconductor Store



* R34 AND R35 ARE APPROX. 1210 OHMS

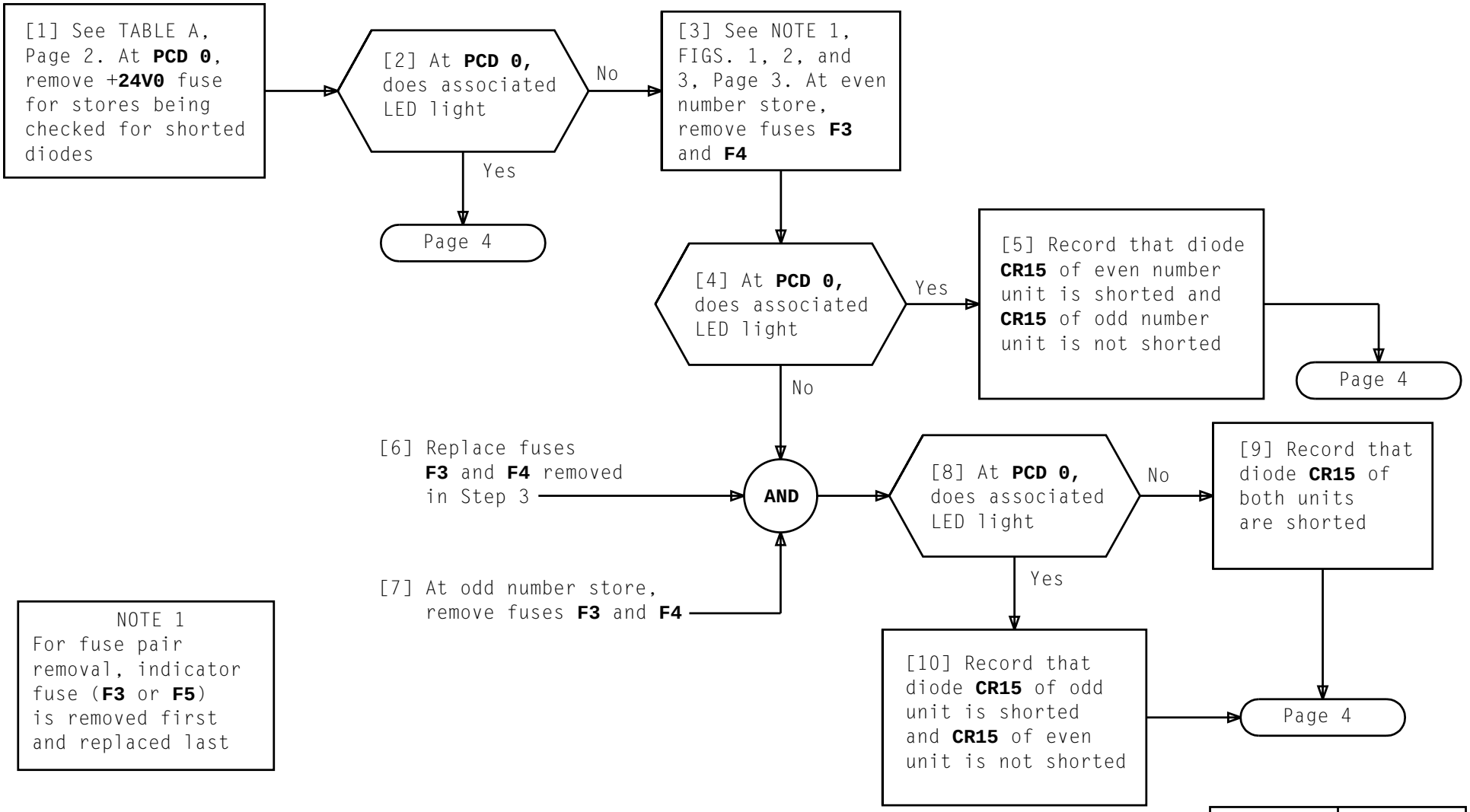
FIG. 2 — Fuse to Diode Layout

CAUTION 1
Checking for shorts with open +24V diodes degrades service

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 2 of 2	**506**

CHECK +24V ORED DIODES FOR OPENS, SEMICONDUCTOR STORE J5A008A

SUMMARY	
At **PCD 0**, remove store +**24V0** fuse; LED should light. Replace fuse and remove **PCD 1** +**24V1** fuse; LED should light.	Replace fuse; test is completed. If PCD LEDs did not light, check for shorted diodes by removing fuses **F3** and **F4**, then **F5** and **F6** on each store



NOTE 1
For fuse pair removal, indicator fuse (**F3** or **F5**) is removed first and replaced last

Issue 7	NOV 1993
254-251-005	DLP
PAGE 1 of 5	507

CHECK +24V ORED DIODES FOR SHORTS, SEMICONDUCTOR STORE J5A008A

TABLE A							
STORE	PCD FUSE DESIGNATION	+24V BUS 0 PCD 0 FUSE POSITION	+24V BUS 1 PCD 1 FUSE POSITION	STORE	PCD FUSE DESIGNATION	+24V BUS 0 PCD 0 FUSE POSITION	+24V BUS 1 PCD 1 FUSE POSITION
CS 00, CS 01	**CS00**	123-15, 9	123-29, 9	CS 36, CS 37	**CS36**	128-15, 11	128-29, 11
CS 02, CS 03	**CS02**	123-15, 10	123-29, 10	CS 38, CS 39	**CS38**	128-15, 12	128-29, 12
CS 04, CS 05	**CS04**	123-15, 11	123-29, 11	CS 40, CS 41	**CS40**	128-15, 13	128-29, 13
CS 06, CS 07	**CS06**	123-15, 12	123-29, 12	CS 42, CS 43	**CS42**	128-15, 14	128-29, 14
CS 08, CS 09	**CS08**	123-15, 13	123-29, 13	CS 44, CS 45	**CS44**	128-15, 15	128-29, 15
CS 10, CS 11	**CS10**	123-15, 14	123-29, 14	CS 46, CS 47	**CS46**	128-15, 16	128-29, 16
CS 12, CS 13	**CS12**	123-15, 15	123-29, 15	PS 00, PS 01	**PS00**	118-15, 9	118-29, 9
CS 14, CS 15	**CS14**	123-15, 16	123-29, 16	PS 02, PS 03	**PS02**	118-15, 10	118-29, 10
CS 16, CS 17	**CS16**	123-15, 1	123-29, 1	PS 04, PS 05	**PS04**	118-15, 11	118-29, 11
CS 18, CS 19	**CS18**	123-15, 2	123-29, 2	PS 06, PS 07	**PS06**	118-15, 12	118-29, 12
CS 20, CS 21	**CS20**	123-15, 3	123-29, 3	PS 08, PS 09	**PS08**	118-15, 13	118-29, 13
CS 22, CS 23	**CS22**	123-15, 4	123-29, 4	PS 10, PS 11	**PS10**	118-15, 14	118-29, 14
CS 24, CS 25	**CS24**	123-15, 5	123-29, 5	PS 12, PS 13	**PS12**	118-15, 15	118-29, 15
CS 26, CS 27	**CS26**	123-15, 6	123-29, 6	PS 14, PS 15	**PS14**	118-15, 16	118-29, 16
CS 28, CS 29	**CS28**	123-15, 7	123-29, 7	PS 16, PS 17	**PS16**	118-15, 1	118-29, 1
CS 30, CS 31	**CS30**	123-15, 8	123-29, 8	PS 18, PS 19	**PS18**	118-15, 2	118-29, 2
CS 32, CS 33	**CS32**	128-15, 9	128-29, 9	PS 20, PS 21	**PS20**	118-15, 3	118-29, 3
CS 34, CS 35	**CS34**	128-15, 10	128-29, 10	PS 22, PS 23	**PS22**	118-15, 4	118-29, 4

FIG. 1 — Store Frame Number System

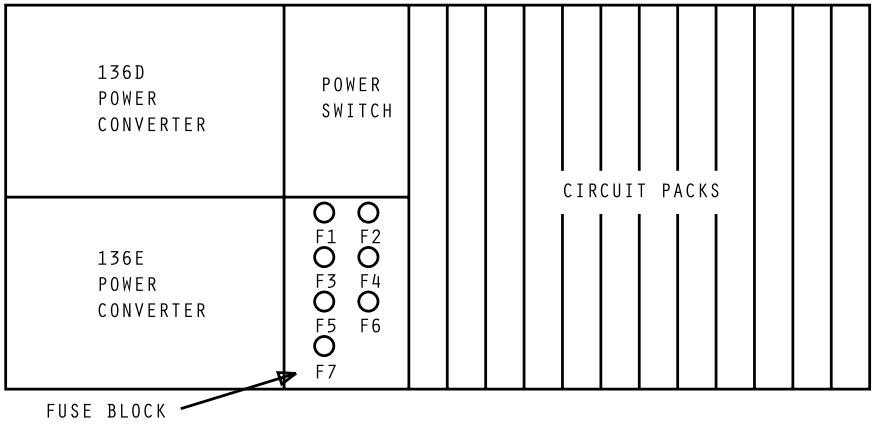


FIG. 2 — Front View, Semiconductor Store

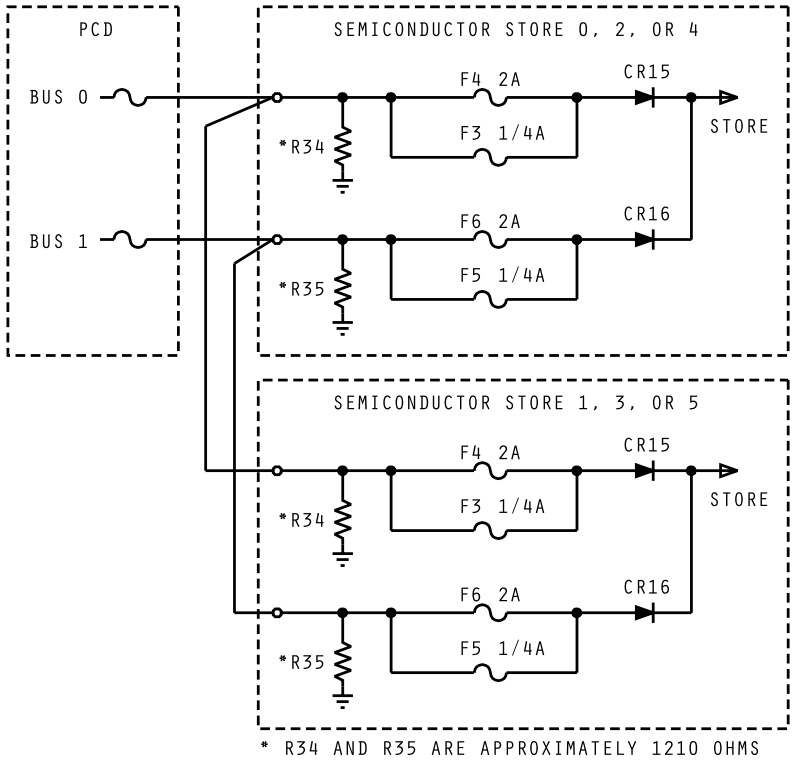
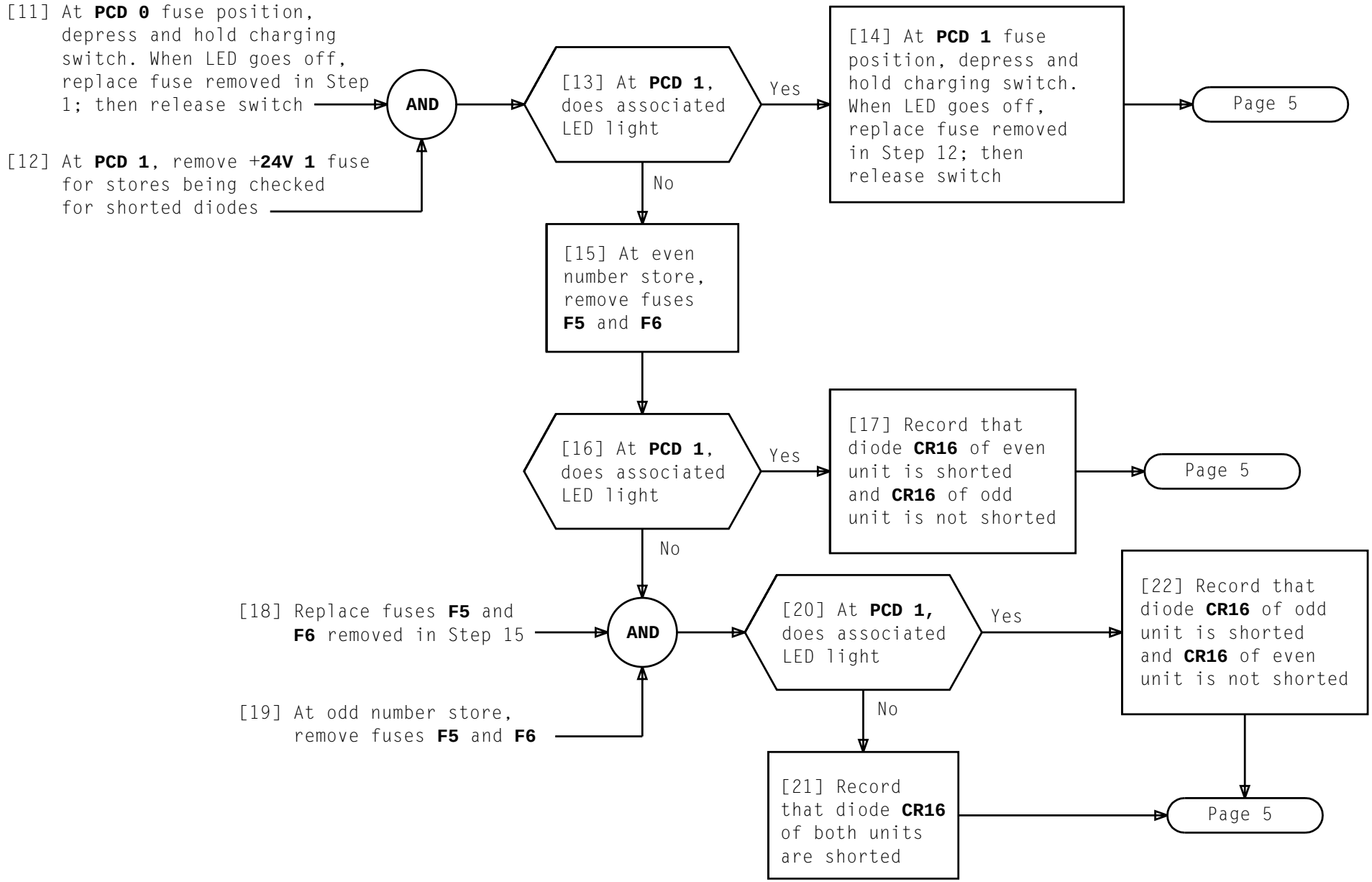
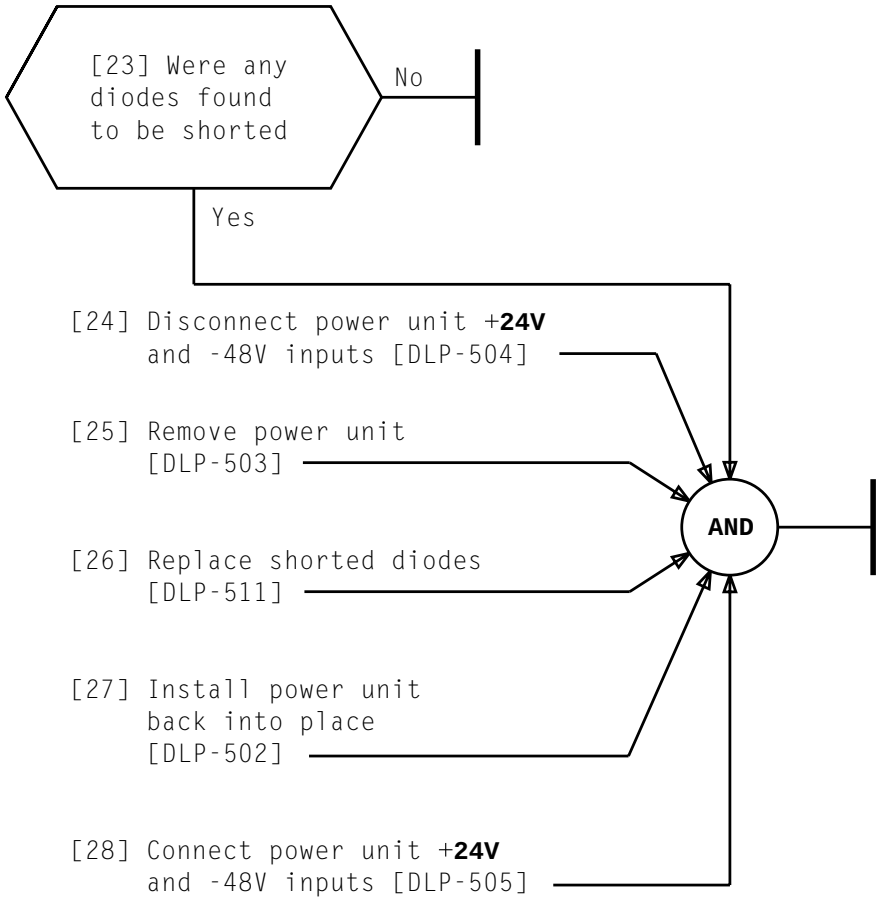


FIG. 3 — Fuse to Diode Layout

CHECK +24V ORED DIODES FOR SHORTS, SEMICONDUCTOR STORE J5A008A



CHECK +24V ORED DIODES FOR SHORTS, SEMICONDUCTOR STORE J5A008A



CHECK +24V ORED DIODES FOR SHORTS, SEMICONDUCTOR STORE J5A008A

SUMMARY

At **PCD 0**, remove **BUS 0** fuse; **PCD LED** should light and store stays up. Replace **PCD 0** fuse; remove **PCD 1** fuse. **PCD** LED should light and store stays up. Replace **PCD 1** fuse. Replace any diodes found to be open or shorted

[1] See TABLE A. At **PCD 0,** remove **BUS 0** fuse for store being checked

[2] Does LED associated with fuse light

No → [3] Record that diode **CR13** is shorted [FIG. 1]

Yes → [4] Does store power down (**PWR OFF** lamp lights)

No → [6] At **PCD 0** fuse position, depress and hold charging switch. When LED goes off, install fuse removed in Step 1; release switch

Yes → [5] Record that diode **CR14** is open [FIG. 1]

[5] → [6]

[6] → [7] Is store powered down

No → [9] See TABLE A. At **PCD 1**, remove **BUS 1** fuse for store being checked

Yes → [8] At store power switch, depress **ON** pushbutton

[8] → [9]

[9] → Page 3

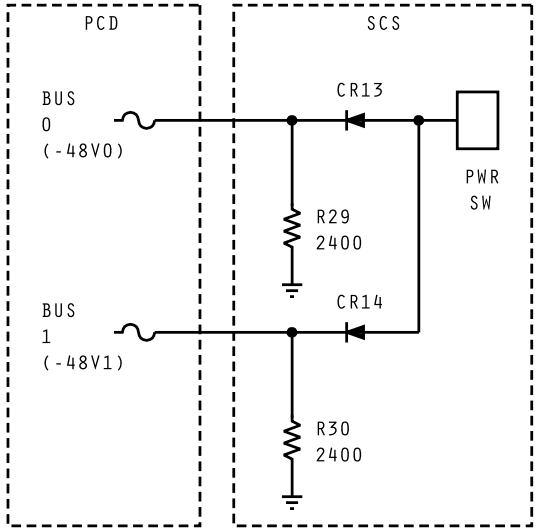


FIG. 1 – Fuse to Diode Layout

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 1 of 3	**508**

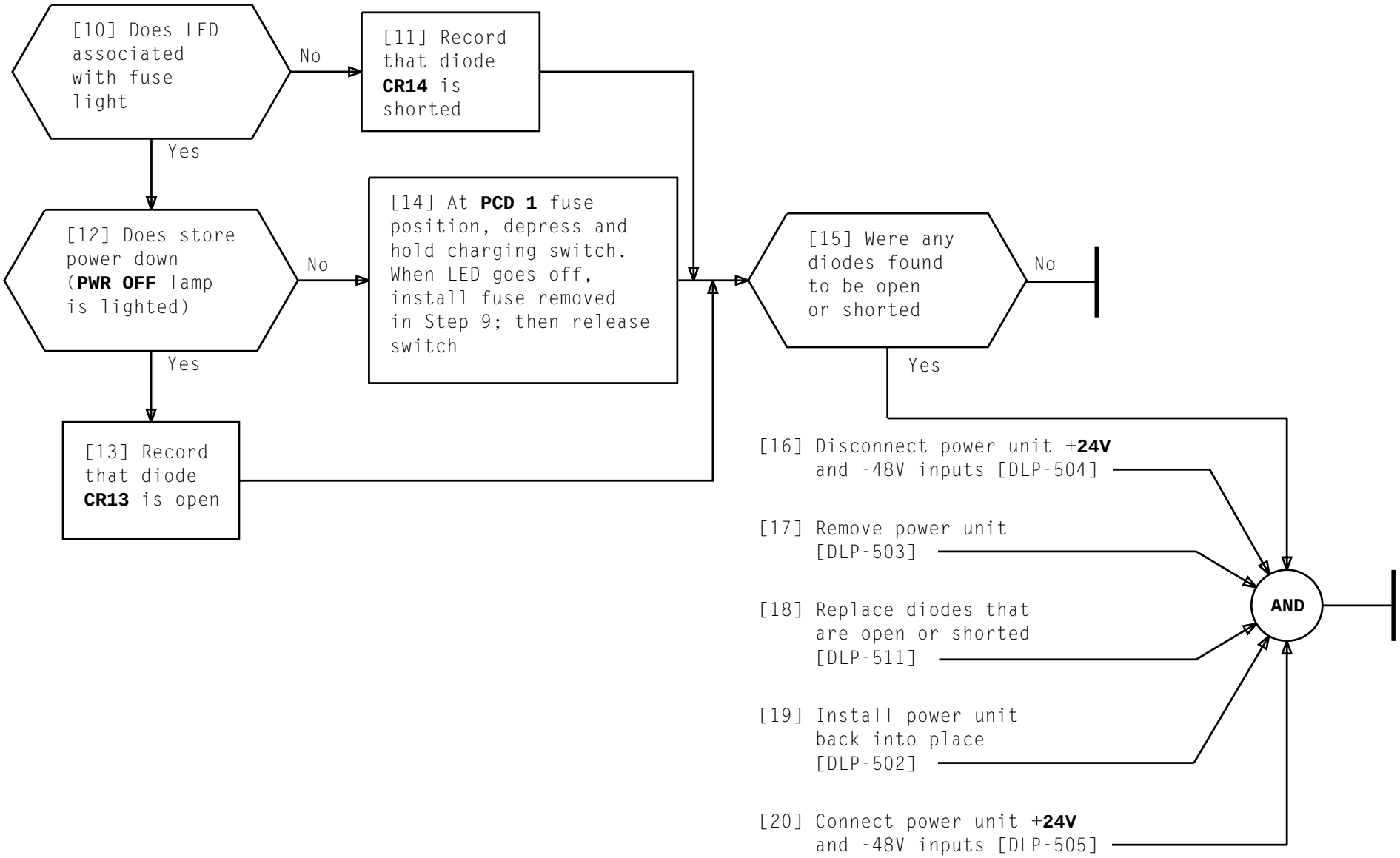
CHECK -48V ORED DIODES, SEMICONDUCTOR STORE J5A008A

TABLE A

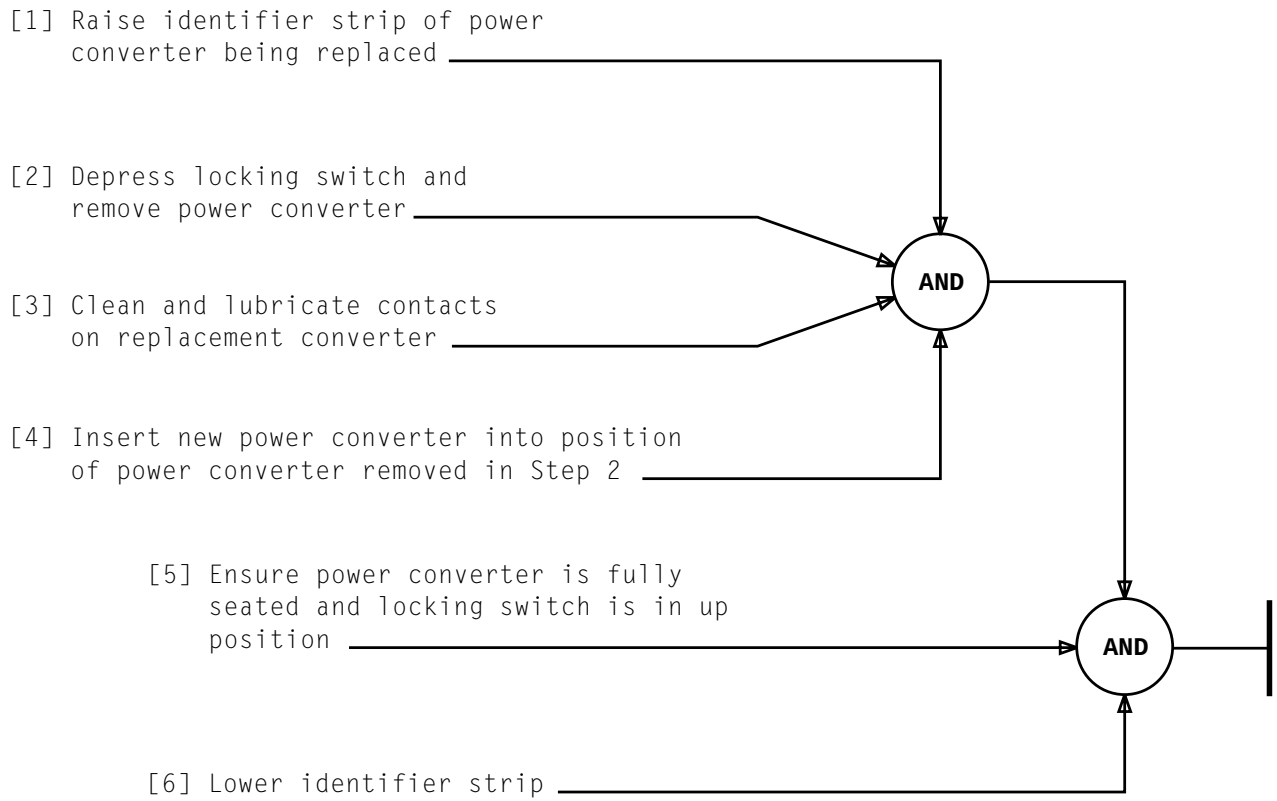
PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION	PCD FUSE DESIG*	-48V BUS 0 PCD 0 FUSE POSITION	-48V BUS 1 PCD 1 FUSE POSITION
CS00	164-15, 3	164-29, 3	**CS18**	169-15, 4	169-29, 4	**CS36**	174-15, 5	174-29, 5	**PS06**	159-15, 4	159-29, 4
CS01	164-15, 11	164-29, 11	**CS19**	169-15, 12	169-29, 12	**CS37**	174-15, 13	174-29, 13	**PS07**	159-15, 12	159-29, 12
CS02	164-15, 4	164-29, 4	**CS20**	169-15, 5	169-29, 5	**CS38**	174-15, 6	174-29, 6	**PS08**	159-15, 5	159-29, 5
CS03	164-15, 12	164-29, 12	**CS21**	169-15, 13	169-29, 13	**CS39**	174-15, 14	174-29, 14	**PS09**	159-15, 13	159-29, 13
CS04	164-15, 5	164-29, 5	**CS22**	169-15, 6	169-29, 6	**CS40**	174-15, 7	174-29, 7	**PS10**	159-15, 6	159-29, 6
CS05	164-15, 13	164-29, 13	**CS23**	169-15, 14	169-29, 14	**CS41**	174-15, 15	174-29, 15	**PS11**	159-15, 14	159-29, 14
CS06	164-15, 6	164-29, 6	**CS24**	169-15, 7	169-29, 7	**CS42**	174-15, 8	174-29, 8	**PS12**	159-15, 7	159-29, 7
CS07	164-15, 14	164-29, 14	**CS25**	169-15, 15	169-29, 15	**CS43**	174-15, 16	174-29, 16	**PS13**	159-15, 15	159-29, 15
CS08	164-15, 7	164-29, 7	**CS26**	169-15, 8	169-29, 8	**CS44**	179-15, 3	179-29, 3	**PS14**	159-15, 8	159-29, 8
CS09	164-15, 15	164-29, 15	**CS27**	169-15, 16	169-29, 16	**CS45**	179-15, 11	179-29, 11	**PS15**	159-15, 16	159-29, 16
CS10	164-15, 8	164-29, 8	**CS28**	174-15, 1	174-29, 1	**CS46**	179-15, 4	179-29, 4	**PS16**	164-15, 1	164-29, 1
CS11	164-15, 16	164-29, 16	**CS29**	174-15, 9	174-29, 9	**CS47**	179-15, 12	179-29, 12	**PS17**	164-15, 9	164-29, 9
CS12	169-15, 1	169-29, 1	**CS30**	174-15, 2	174-29, 2	**PS00**	159-15, 1	159-29, 1	**PS18**	164-15, 2	164-29, 2
CS13	169-15, 9	169-29, 9	**CS31**	174-15, 10	174-29, 10	**PS01**	159-15, 9	159-29, 9	**PS19**	164-15, 10	164-29, 10
CS14	169-15, 2	169-29, 2	**CS32**	174-15, 3	174-29, 3	**PS02**	159-15, 2	159-29, 2	**PS20**	179-15, 5	179-29, 5
CS15	169-15, 10	169-29, 10	**CS33**	174-15, 11	174-29, 11	**PS03**	159-15, 10	159-29, 10	**PS21**	179-15, 13	179-29, 13
CS16	169-15, 3	169-29, 3	**CS34**	174-15, 4	174-29, 4	**PS04**	159-15, 3	159-29, 3	**PS22**	179-15, 6	179-29, 6
CS17	169-15, 11	169-29, 11	**CS35**	174-15, 12	174-29, 12	**PS05**	159-15, 11	159-29, 11	**PS23**	179-15, 14	179-29, 14

* PCD fuse designation and store designation are the same

CHECK -48V ORED DIODES, SEMICONDUCTOR STORE J5A008A



CHECK -48V ORED DIODES, SEMICONDUCTOR STORE J5A008A



REPLACE POWER CONVERTER, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

At front of store:

[1] Place power unit into position using care feeding paddle boards and power leads through access hole of mounting plate

At rear of store [FIG. 1]:

[2] With power unit being supported from front, screw retaining screws into place

[3] Connect power leads extending through access hole to terminal board

[4] Connect paddle boards per **EQL** stamped on side

AND

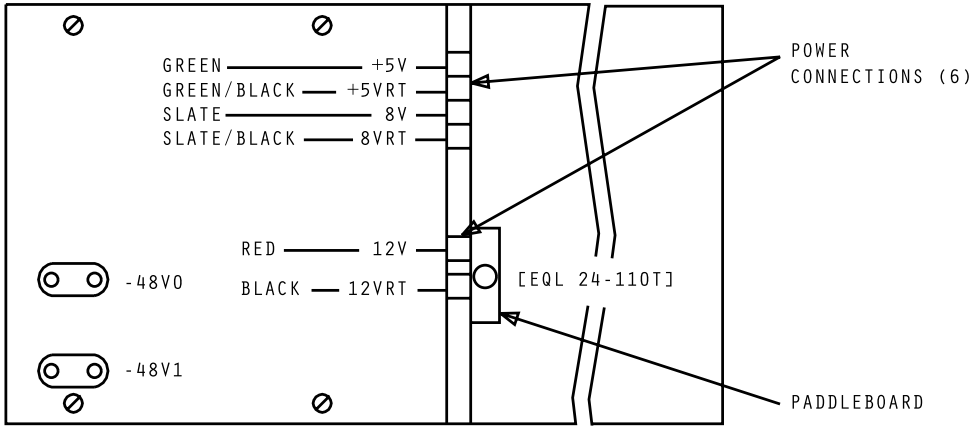
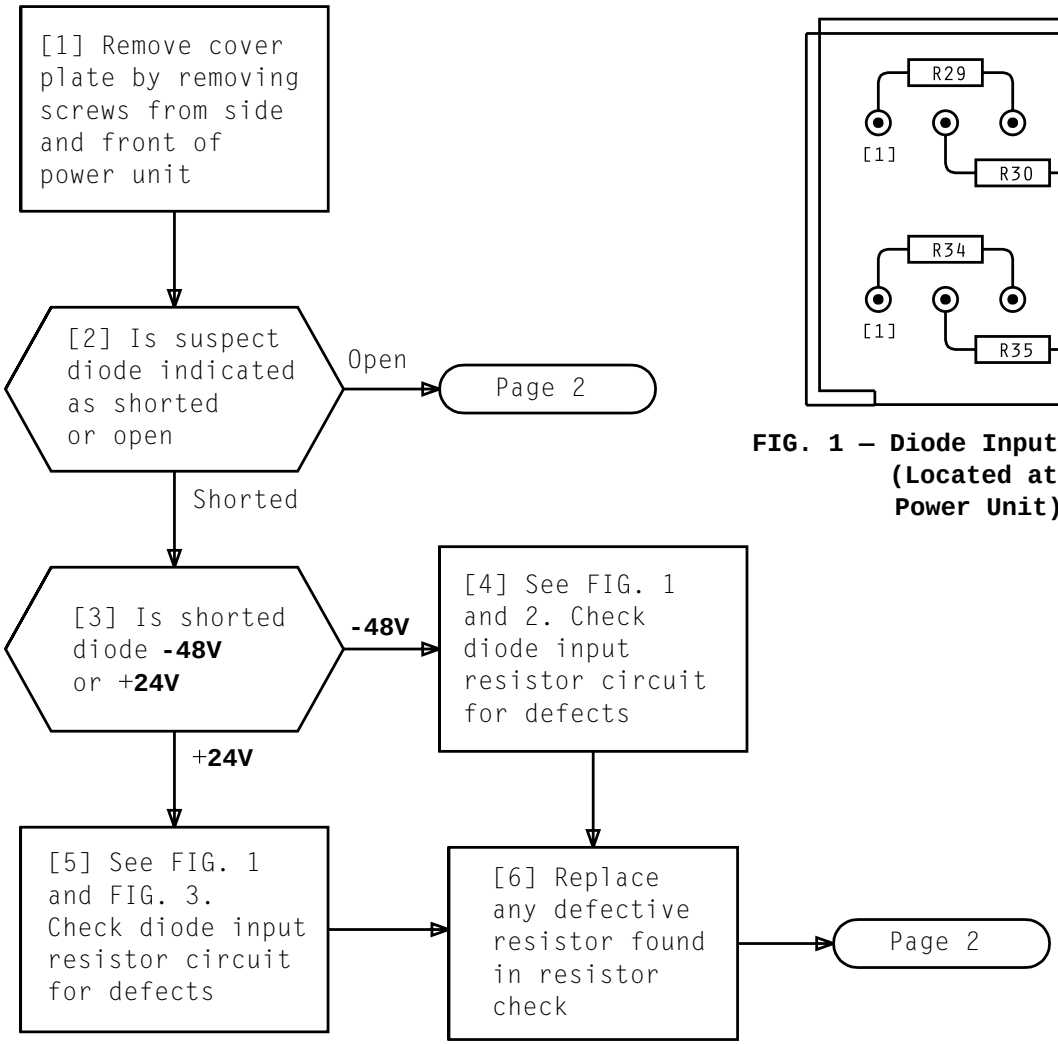


FIG. 1 — Rear View of Semiconductor Store J5A010A or J5A010B

INSTALL POWER UNIT (ED-5A266), SEMICONDUCTOR STORE J5A010A OR J5A010B

SUMMARY

If diode was shorted, check resistor circuit and replace both diodes. If diode (open or shorted) is in **+24V** circuit, replace both diodes. If diode was open and in **-48V** circuit, replace only the one diode. Check all diodes for condition and direction



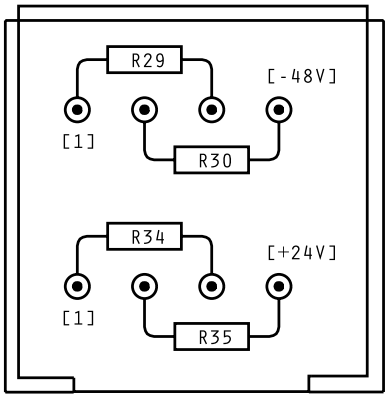


FIG. 1 — Diode Input Resistors (Located at Rear of Power Unit)

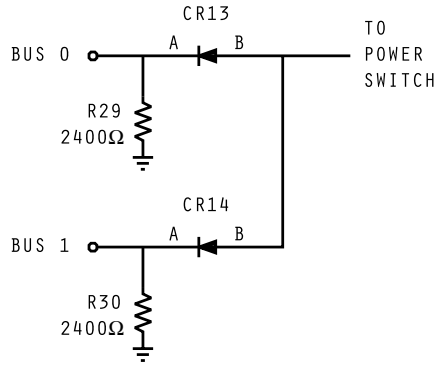


FIG. 2 — -48V Diode Circuit Layout

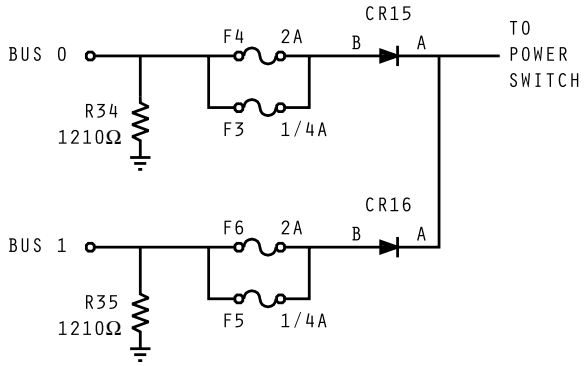


FIG. 3 — +24V Fuse to Diode Circuit Layout

Issue 7	NOV 1993
254-251-005	DLP
PAGE 1 of 3	511

REPLACE AND CHECK ORED DIODES, SEMICONDUCTOR STORE J5A008A

[7] Are diodes being replaced in **-48V** or **+24V** circuit

-48V

[8] See FIG. 4 and NOTE 1. Replace diode (**CR13** or **CR14**) checked as open or shorted

+24V

[9] See FIG. 4 and NOTE 1. Replace both diodes (**CR15** and **CR16**)

Using ohmmeter, set at **RX1**:

[10] Connect negative lead to cathode side of diode

AND

[11] Connect positive lead to anode side of diode

Meter indicates less than 10 ohms

[12] Change setting of meter to **RX10**

AND

Page 3

[13] Reverse meter leads at diode

Meter indicates more than 1000 ohms

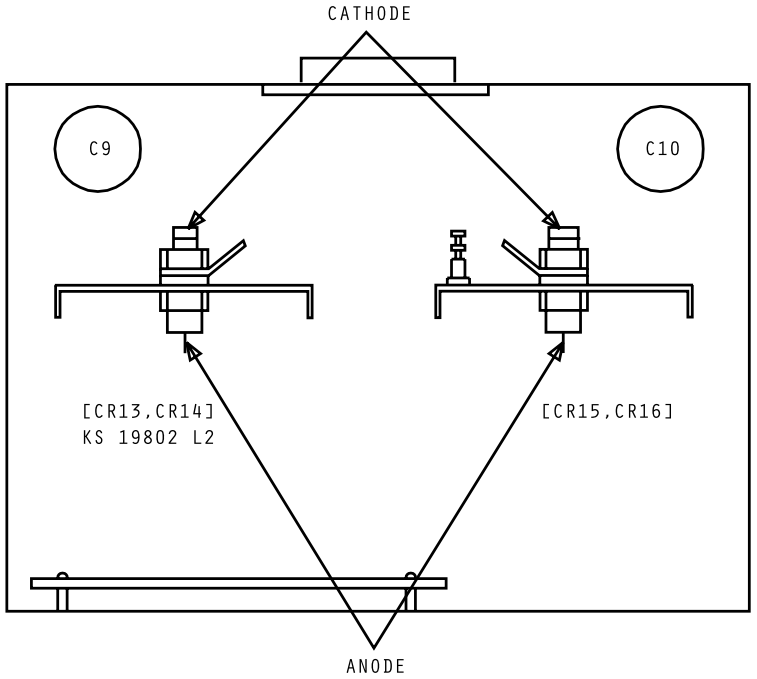
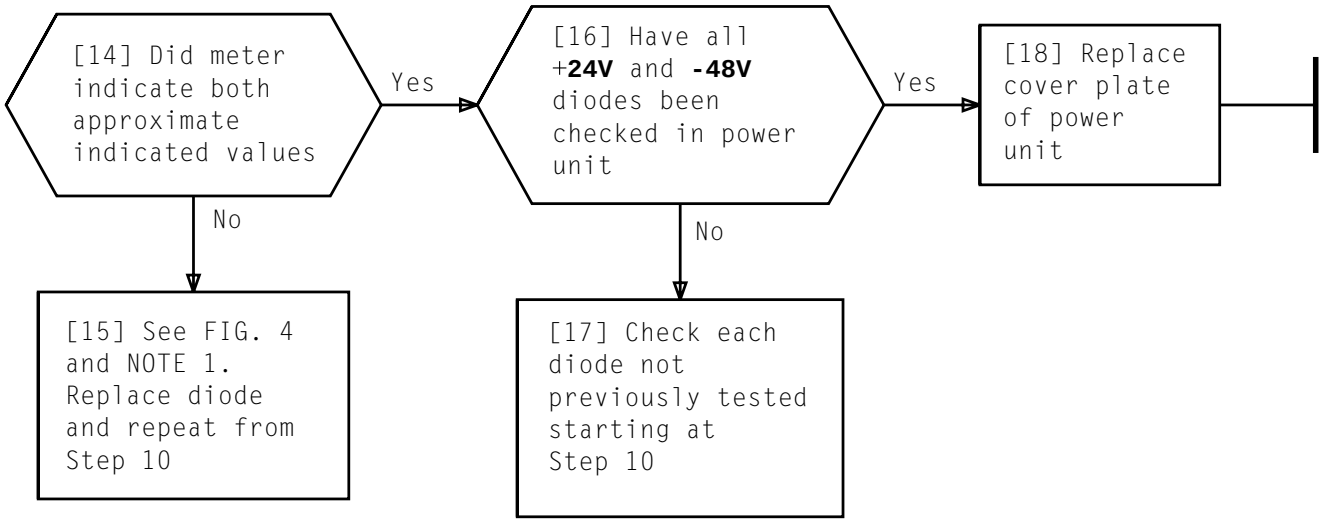


FIG. 4 — Top View of Power Unit With Cover Removed

NOTE 1
Wiring is to be removed and replaced in accordance with wiring standards

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 2 of 3	**511**

REPLACE AND CHECK ORED DIODES, SEMICONDUCTOR STORE J5A008A



REPLACE AND CHECK ORED DIODES, SEMICONDUCTOR STORE J5A008A

At rear of store unit [FIG. 1]:

[1] Disconnect paddleboards using 793A tool; note **EQL** of each connector

[2] Disconnect power leads extending from access hole

AND

At front of store:

[3] Remove **136J** power converter by depressing locking switch and pulling out with handle

[4] Remove **136L** power converter by depressing locking switch and pulling out with handle

AND

At rear of store:

[5] See WARNING 1. Remove mounting screws supporting power unit

[6] As unit is being removed, carefully feed cables through access hole

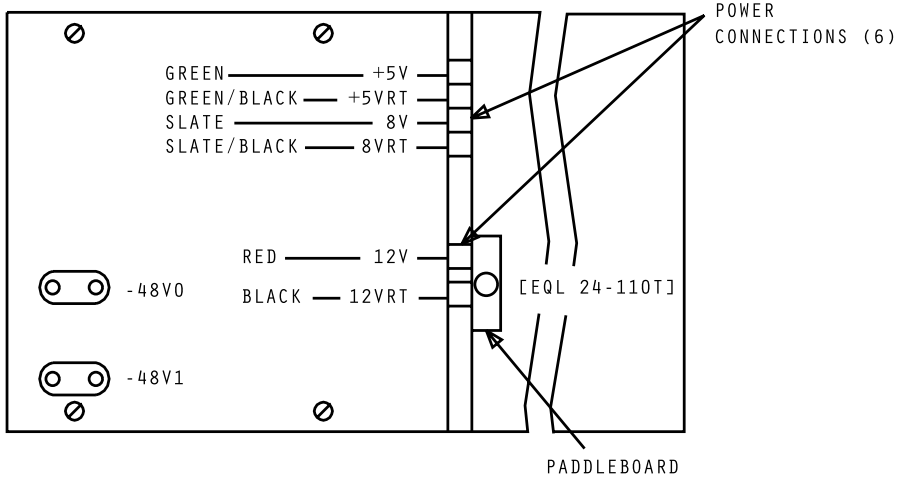
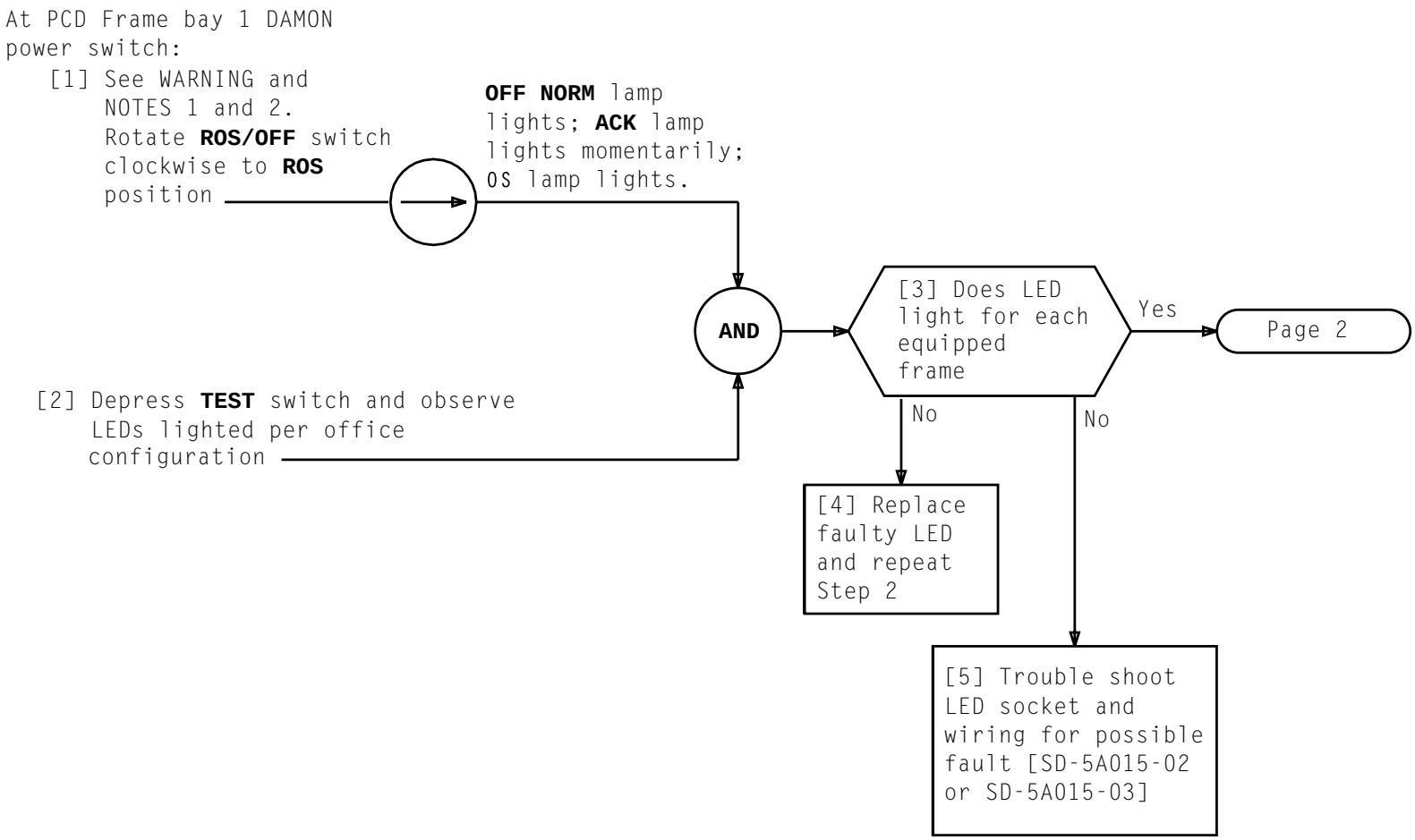


FIG. 1 — Rear View of Semiconductor Store J5A010A or J5A010B

WARNING 1
Power unit should be supported on front side of bay while removing retaining screws to prevent damage to power unit and surrounding equipment

REMOVE POWER UNIT (ED-5A266), SEMICONDUCTOR STORE J5A010A OR J5A010B

TEST PCD FRAME LEDs AND DISABLE ALARMS

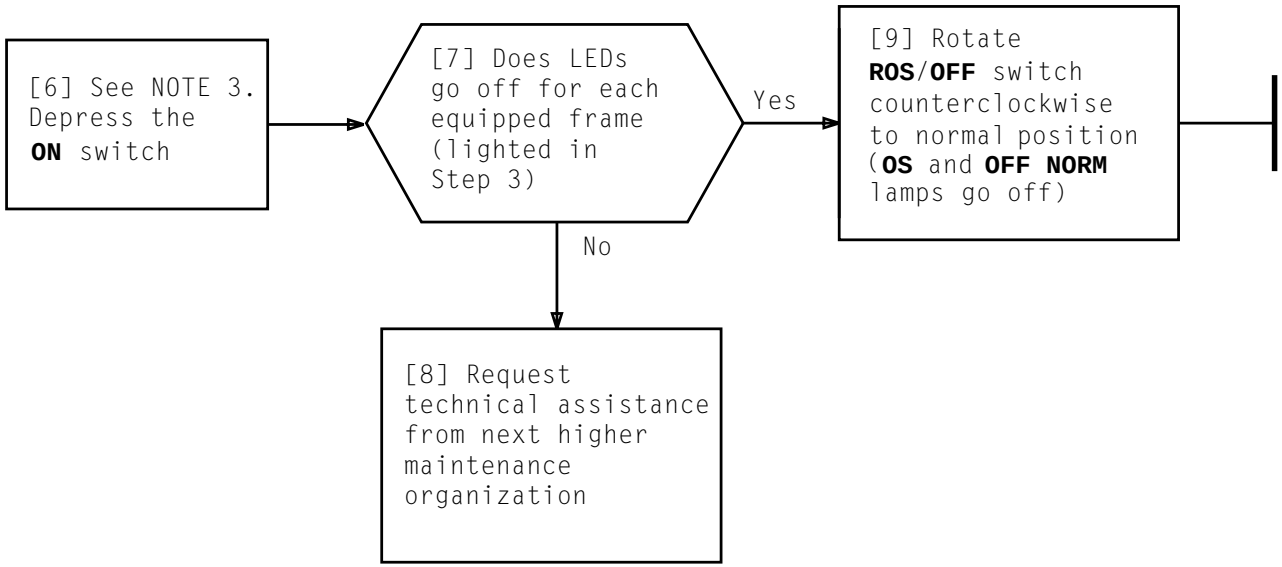


NOTES

1. Removal of power with **ROS/OFF** switch in PCD frame bay 1 does not remove power to processor frames. No system alarms are detected if a fuse should blow at PCD frame. However, LED indicators continue to function
2. Allow up to 7 minutes for yellow **OS** lamp to light.

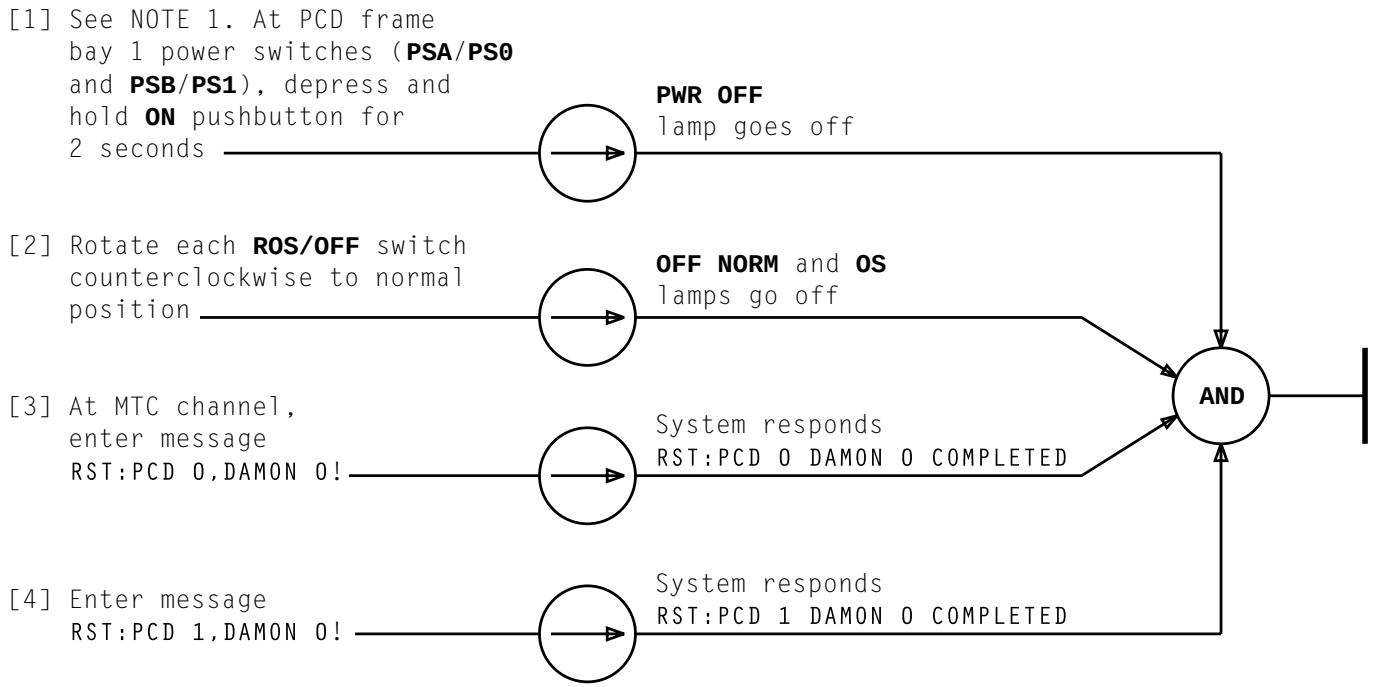
WARNING

Converters in PCD bay frames 0 and 2 must not be removed from service while performing this procedure. Do not rotate **ROS/OFF** *switch on bays 0 and 2 to* **ROS**



NOTE 3
In this Step, depressing the ON switch clears the LEDs, it does not restore power

TEST PCD FRAME LEDs AND DISABLE ALARMS

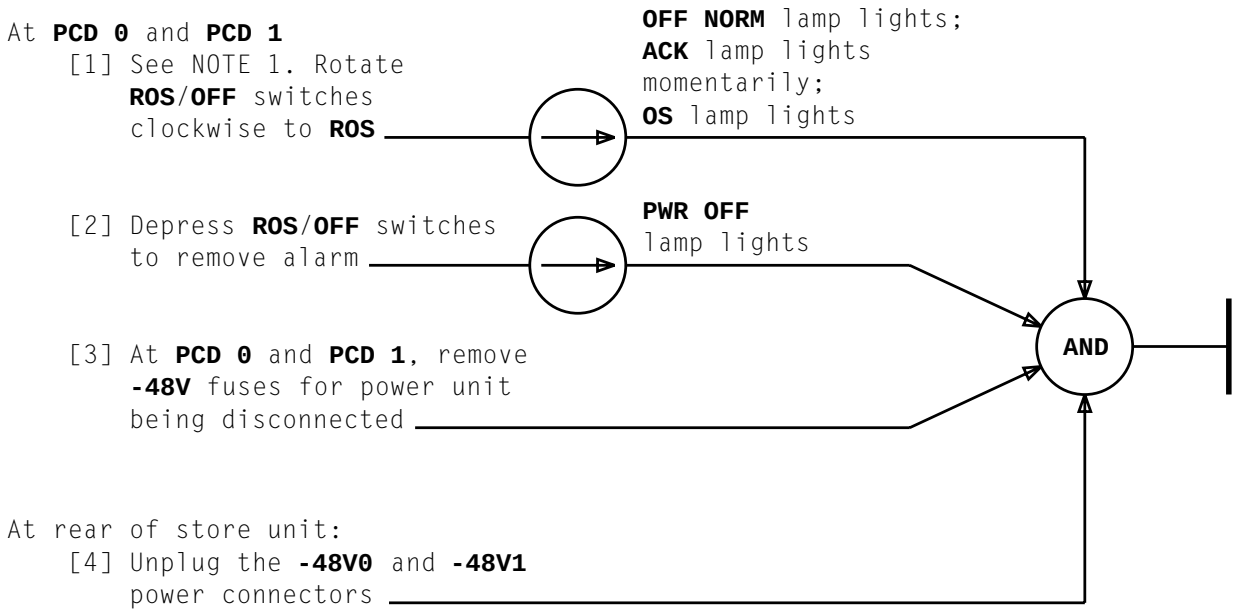


ENABLE PCD FRAME ALARMS

NOTE 1
Restoral of power with **ON** pushbuttons in PCD frame bay 1 activates system alarms for processor frames

SUMMARY

Disable alarms at **PCD 0** and **PCD 1**. For J5A010A or J5A010B frame: remove **-48V** fuses; then at frame, unplug **-48V 0** and **-48V 1** connectors



NOTE 1

Removal of power at **PCD 0 and PCD 1** switches removes audible power alarm capabilities only

DISCONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE, J5A010A OR J5A010B

SUMMARY

For J5A010A or J5A010B frame: connect **-48V0** and **-48V1** leads and restore **PCD 0** and **PCD 1** to service

At rear of store [FIG. 1]:

[1] Connect **-48V** BUS 1 cable to bottom connector of power unit

[2] Connect **-48V** BUS 0 cable to top connector of power unit

AND

[3] Install **136J** and **136L** converters and ensure they are fully seated

[4] Is PCD frame J5A007B or J5A007C

J5A007C → Page 2

J5A007B

[5] At **PCD 0** and **PCD 1**, depress and hold charge switches of **-48V** fuses for store to which power is being connected. When LEDs extinguish, replace fuses and release charge switches

Page 3

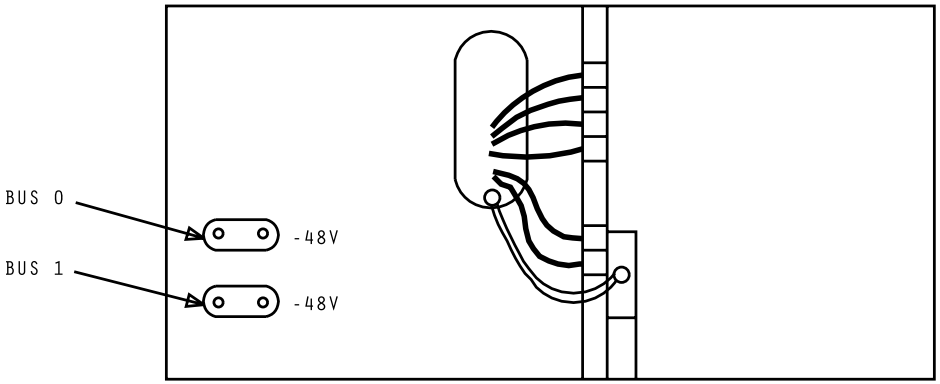
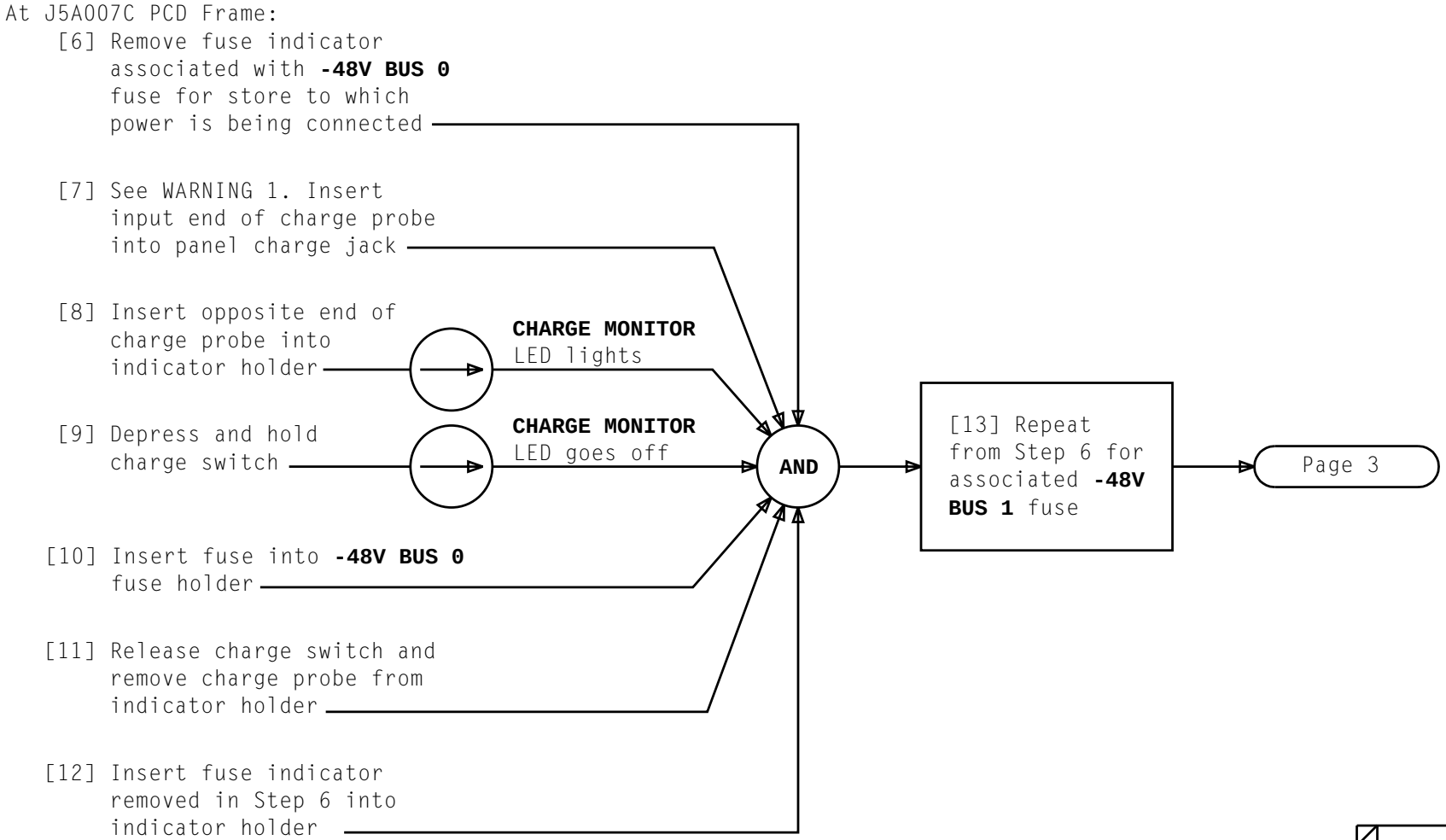


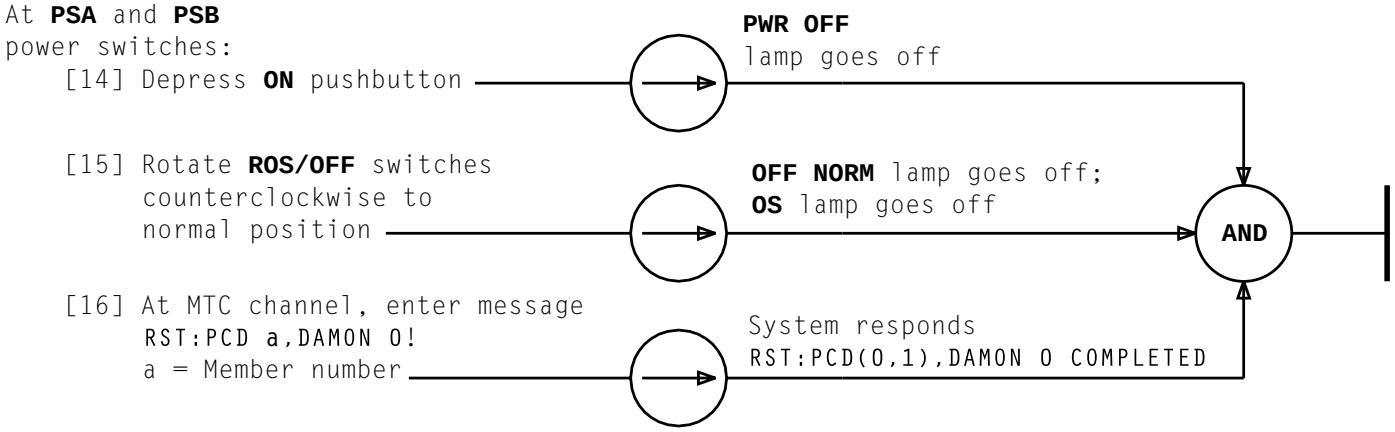
FIG. 1 — Rear View of J5A010A or J5A010B Semiconductor Store

CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A010A OR J5A010B



WARNING 1
Voltage may be present on opposite end of probe; equipment damage possible if grounded

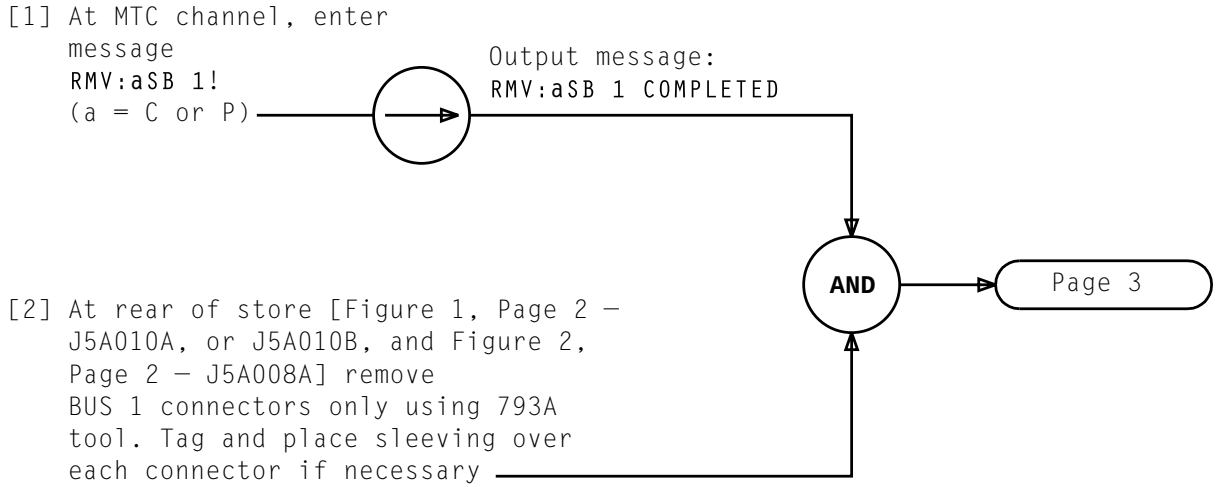
CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A010A OR J5A010B



CONNECT POWER UNIT INPUTS, SEMICONDUCTOR STORE J5A010A OR J5A010B

SUMMARY

Remove BUS 1 with RMV message and remove BUS 1 connectors. Restore BUS 1; remove BUS 0 from service. Remove BUS 0 connectors, then restore BUS 0. Replace store unit. Remove BUS 0 from service and connect leads; restore BUS 0 and remove BUS 1. Connect BUS 1 leads and restore BUS 1 to service



REPLACE STORE UNIT, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

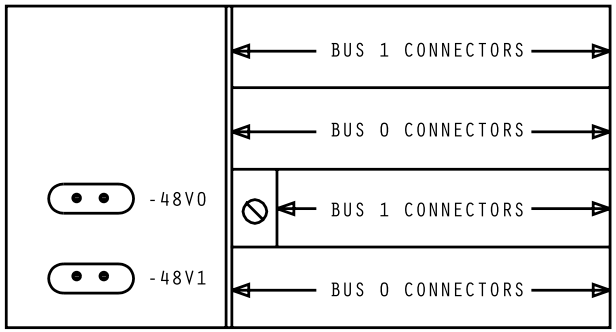


Figure 1 — Rear View, Semiconductor Store J5A010A or J5A010B

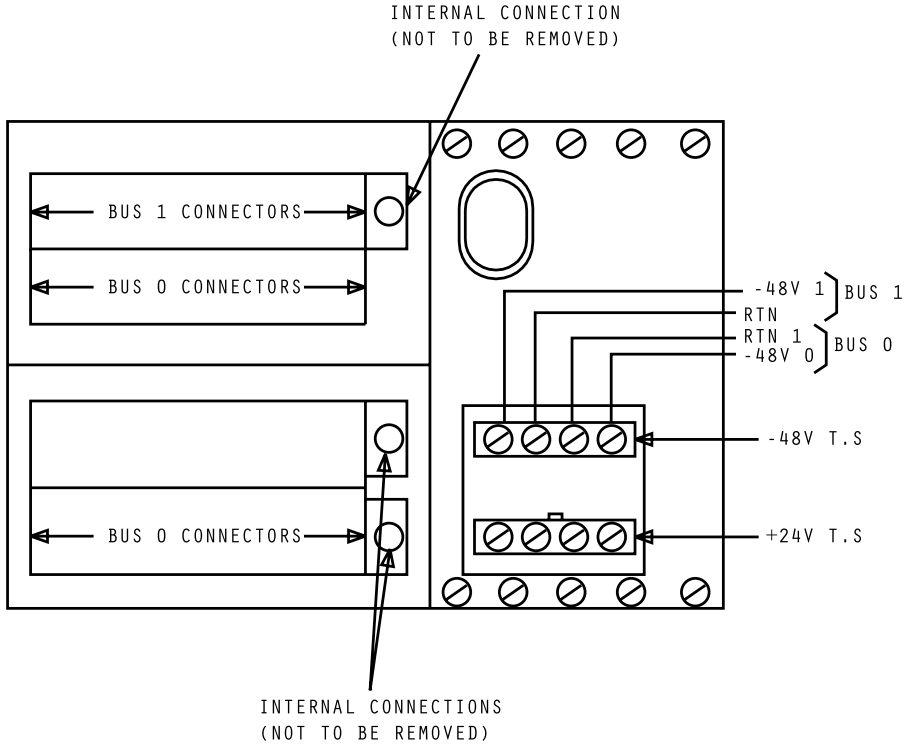
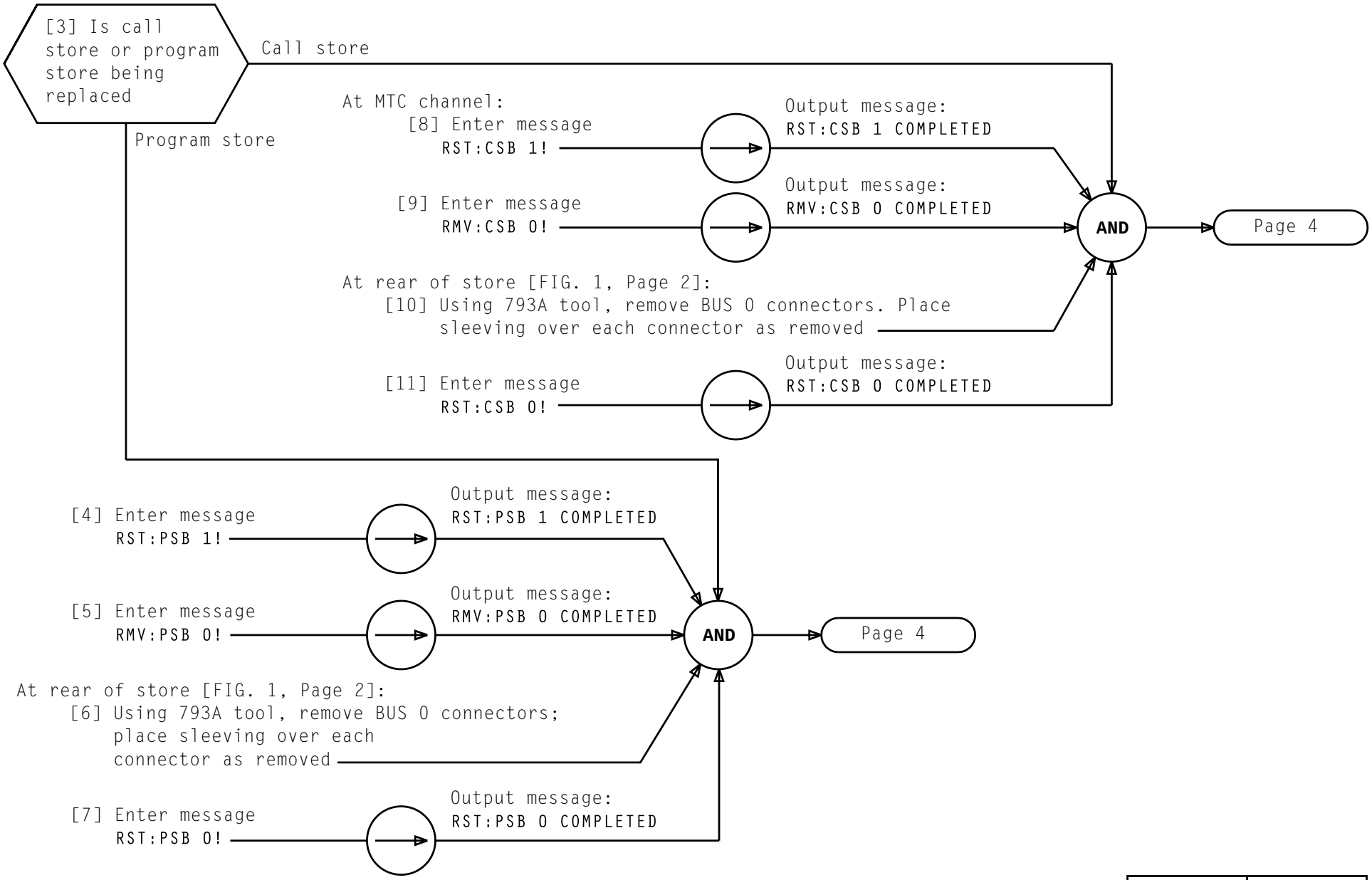


Figure 2 — Rear View, Semiconductor Store Unit J5A008A

REPLACE STORE UNIT, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



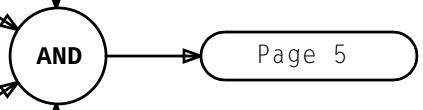
REPLACE STORE UNIT, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

[12] See WARNING 1. Remove mounting screws from both sides of store and remove unit from bay

[13] Remove store from equipment location to designated area

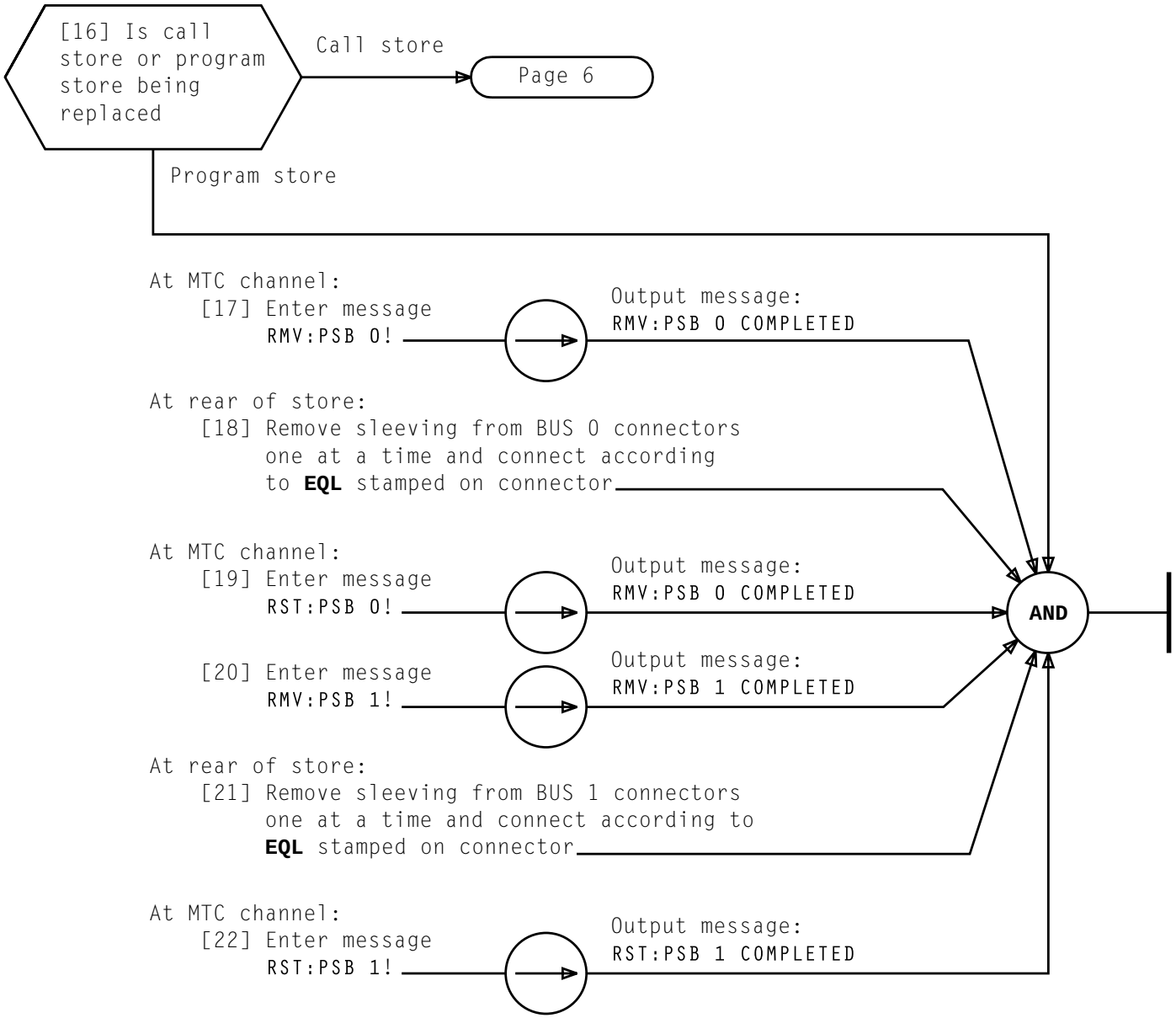
[14] Mount new store unit in bay using mounting screws removed in Step 12

[15] Check unit for damage, connectors, slots, and other areas subject to electrical failure

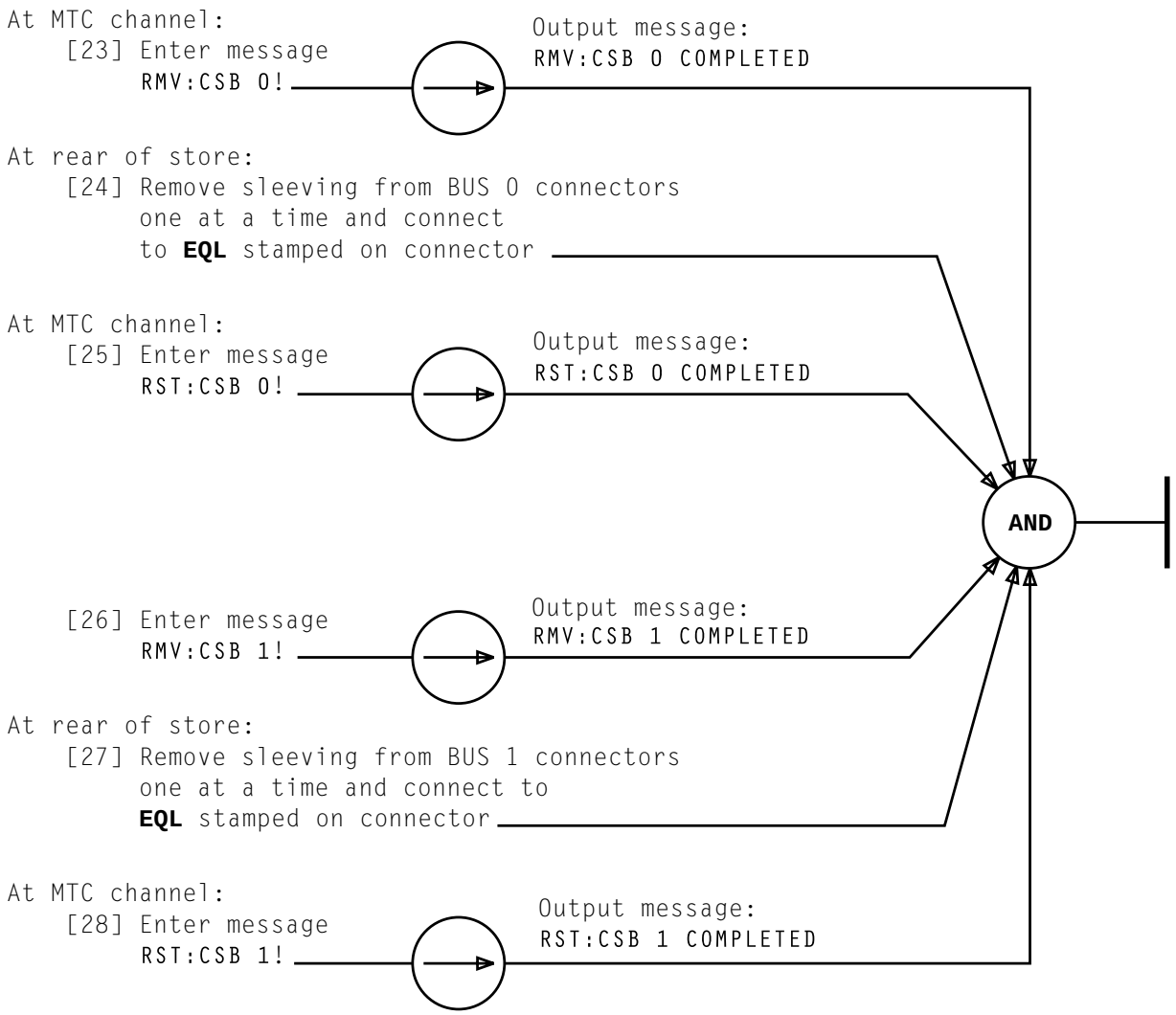


WARNING 1
Store unit should be supported during removal of mounting screws to ensure unit being removed and surrounding units are not damaged

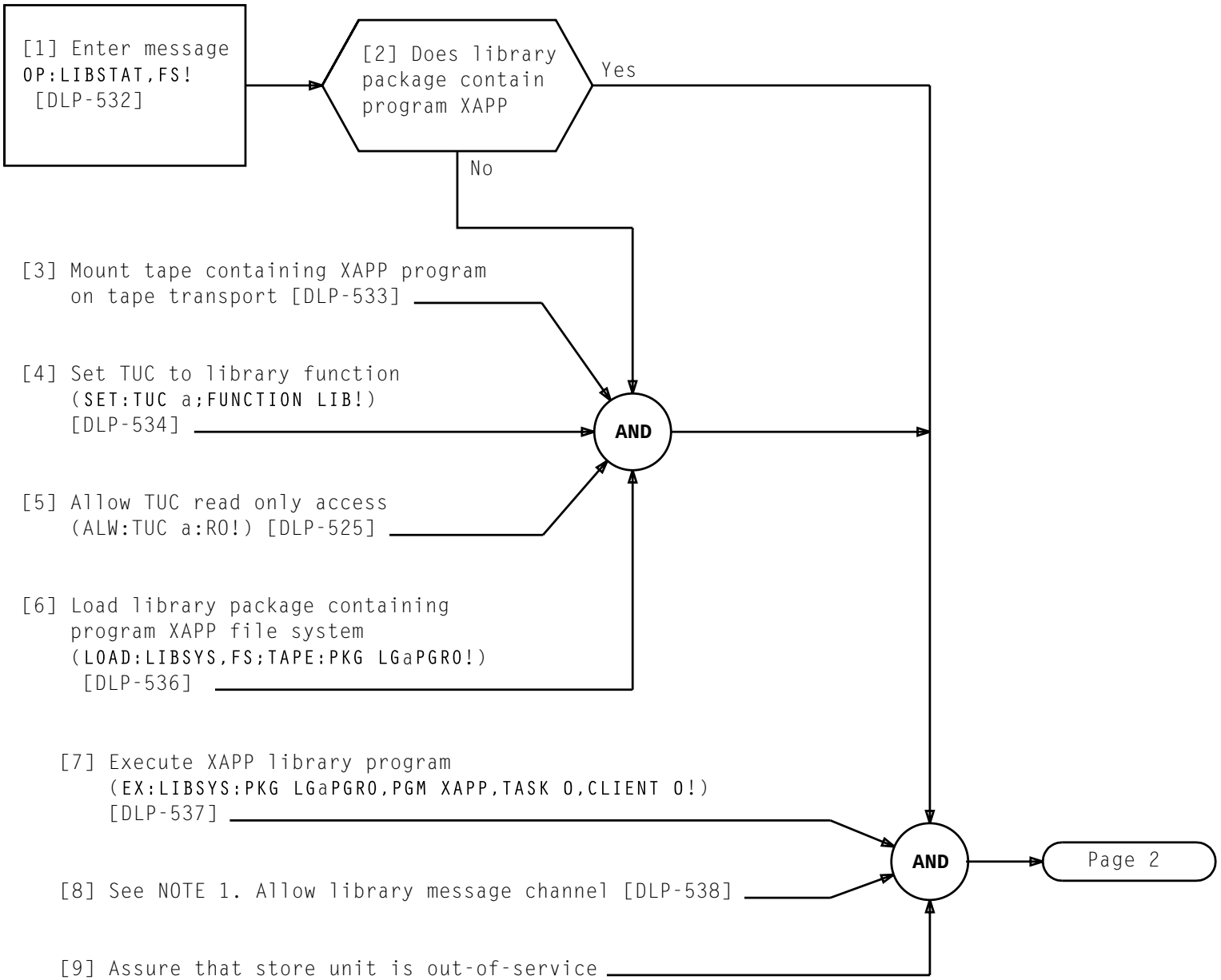
REPLACE STORE UNIT, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



REPLACE STORE UNIT, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



REPLACE STORE UNIT, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



NOTE 1
XAPP library program times out after 2 hours of inactivity. If XAPP does time out, items 7 and 8 must be performed before using XAPP input messages

DEGROW STORE TO SPECIAL GROWTH STATE

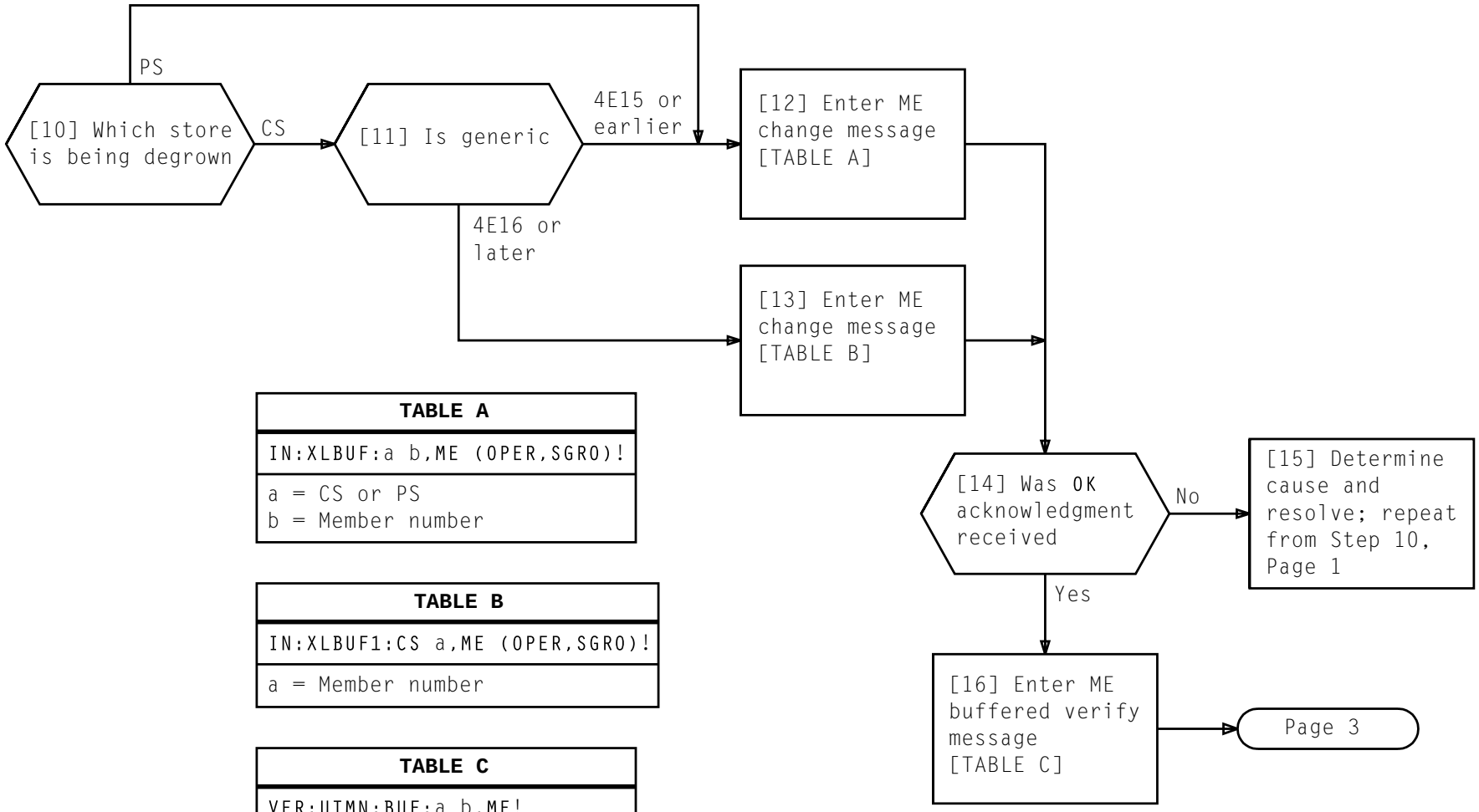


TABLE A
IN:XLBUF:a b,ME (OPER,SGRO)!
a = CS or PS b = Member number

TABLE B
IN:XLBUF1:CS a,ME (OPER,SGRO)!
a = Member number

TABLE C
VER:UTMN;BUF:a b,ME!
a = CS or PS b = Member number

DEGROW STORE TO SPECIAL GROWTH STATE

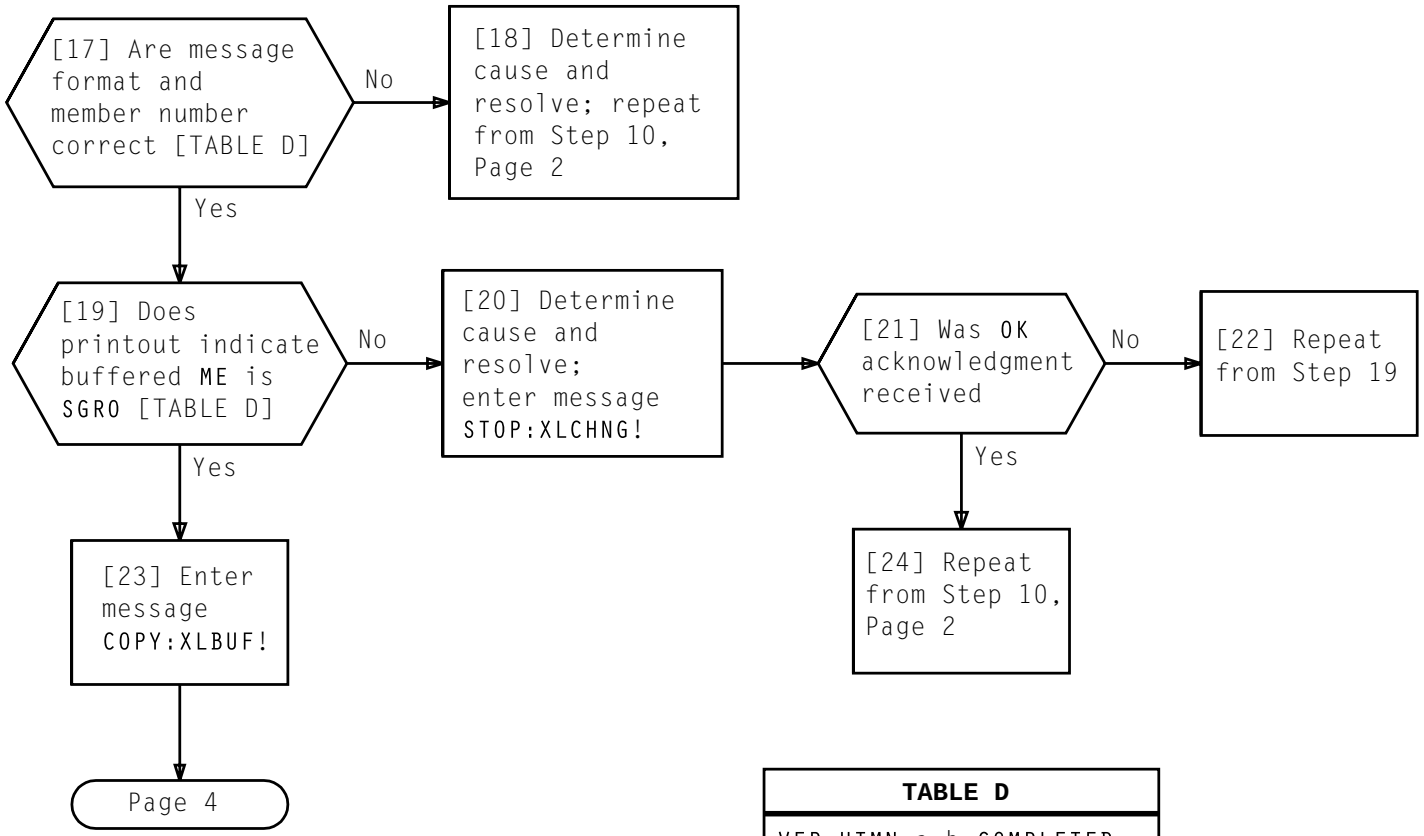


TABLE D
VER:UTMN,a b COMPLETED TRANSLATOR ADR = TRANSLATOR SIZE = BUFFERED DATA ME SGRO
a = CS or PS b = Member number

DEGROW STORE TO SPECIAL GROWTH STATE

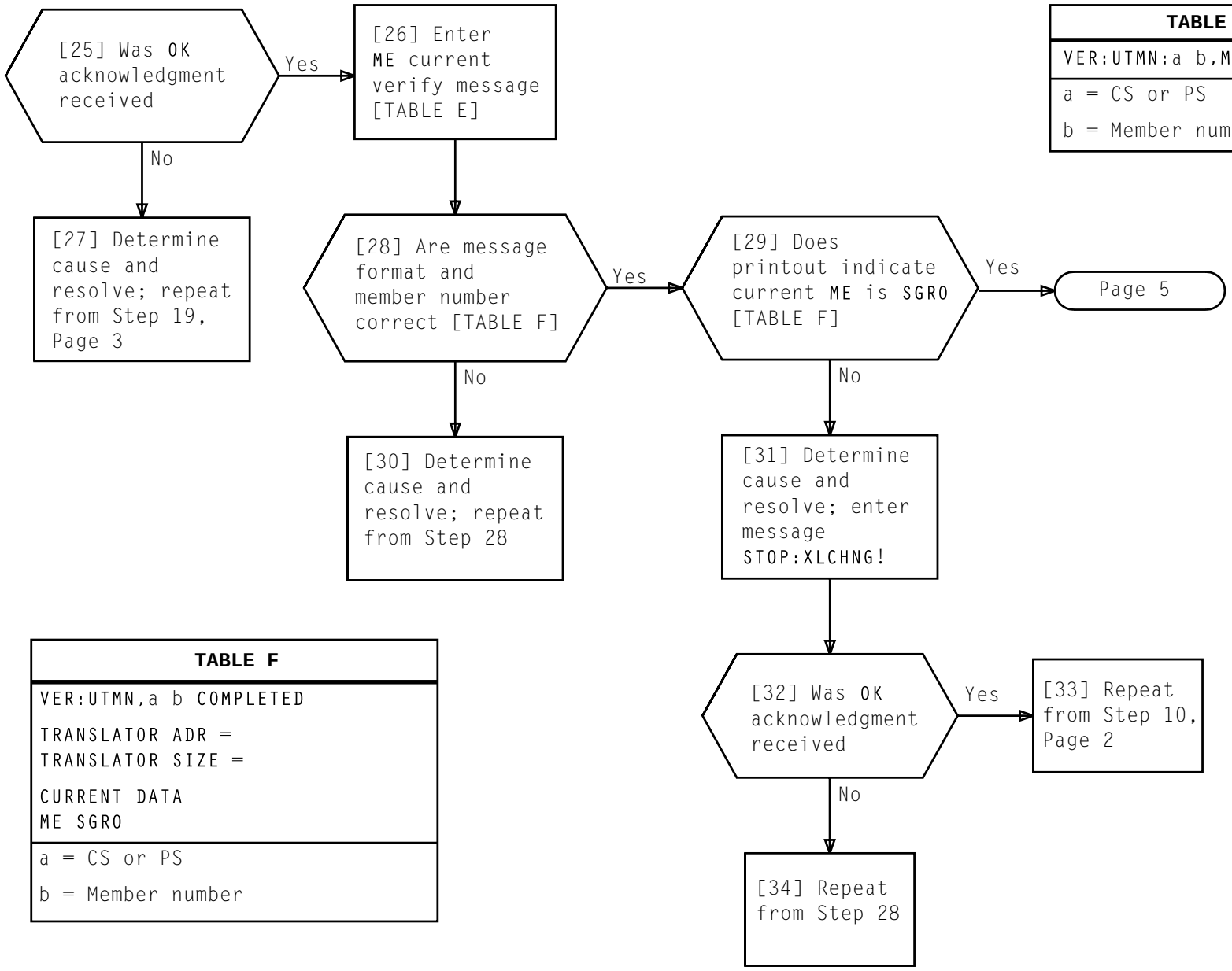
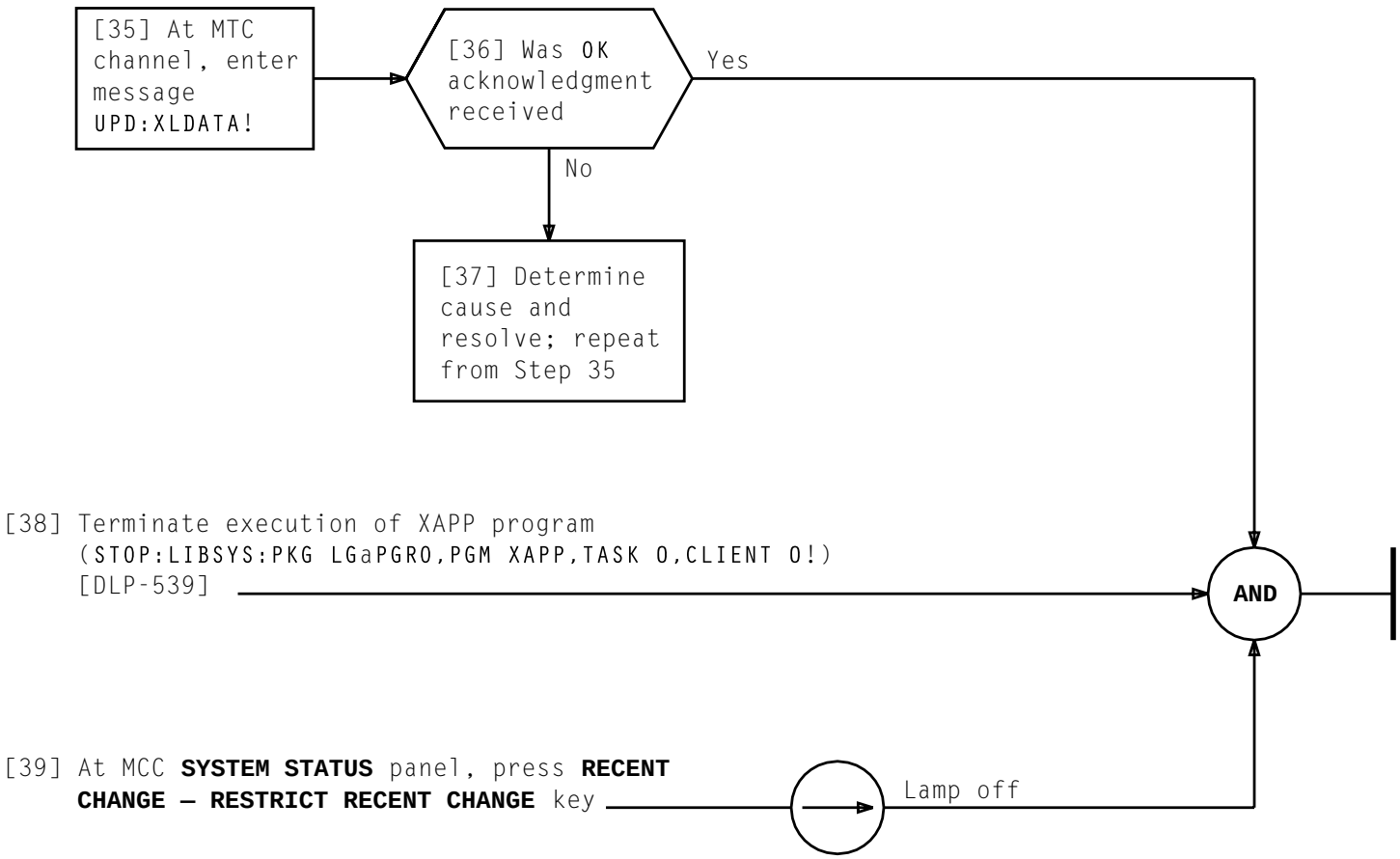


TABLE E
VER:UTMN:a b,ME!
a = CS or PS b = Member number

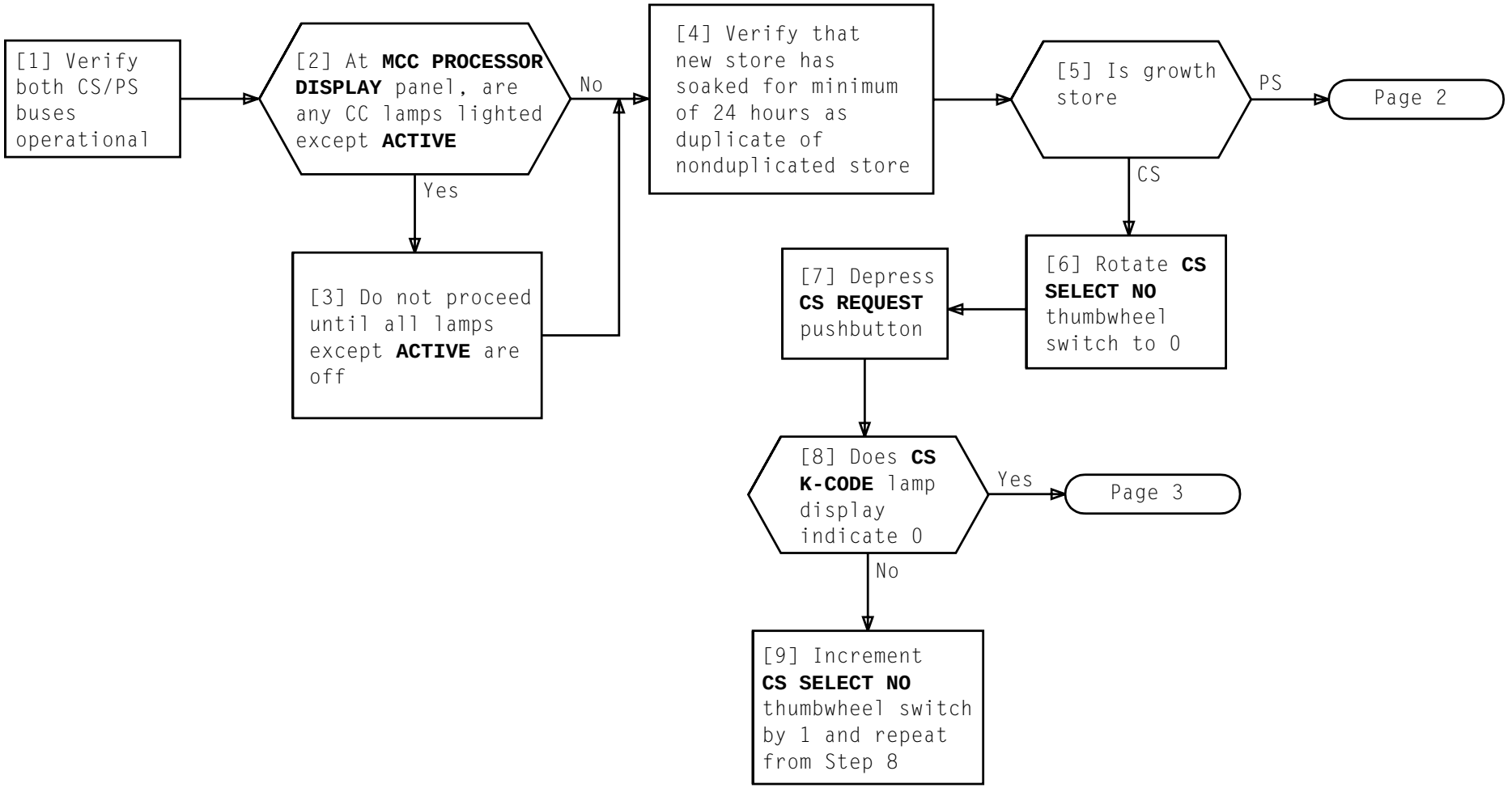
TABLE F
VER:UTMN,a b COMPLETED TRANSLATOR ADR = TRANSLATOR SIZE = CURRENT DATA ME SGRO
a = CS or PS b = Member number

DEGROW STORE TO SPECIAL GROWTH STATE

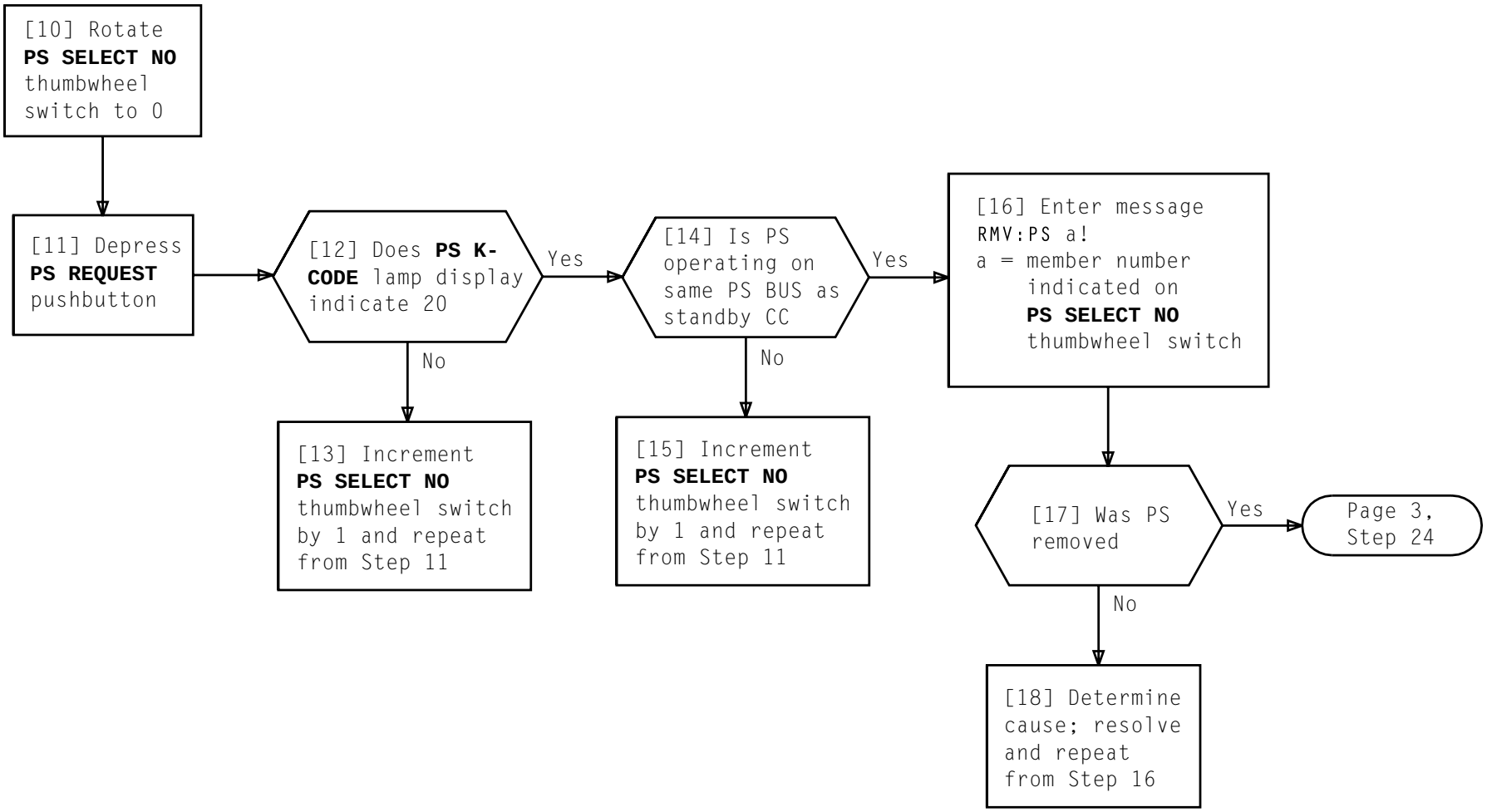


DEGROW STORE TO SPECIAL GROWTH STATE

SUMMARY	
Assure both call store/call program (CS/PS) buses are operational and new store has soaked a minimum of 24 hours.	Select proper K-code. Remove new store from service and then configure as a duplicate base store using set message. Soak minimum of 24 hours in this mode



CONFIGURE NEW STORE AS DUPLICATE BASE STORE, SEMICONDUCTOR STORE



CONFIGURE NEW STORE AS DUPLICATE BASE STORE, SEMICONDUCTOR STORE

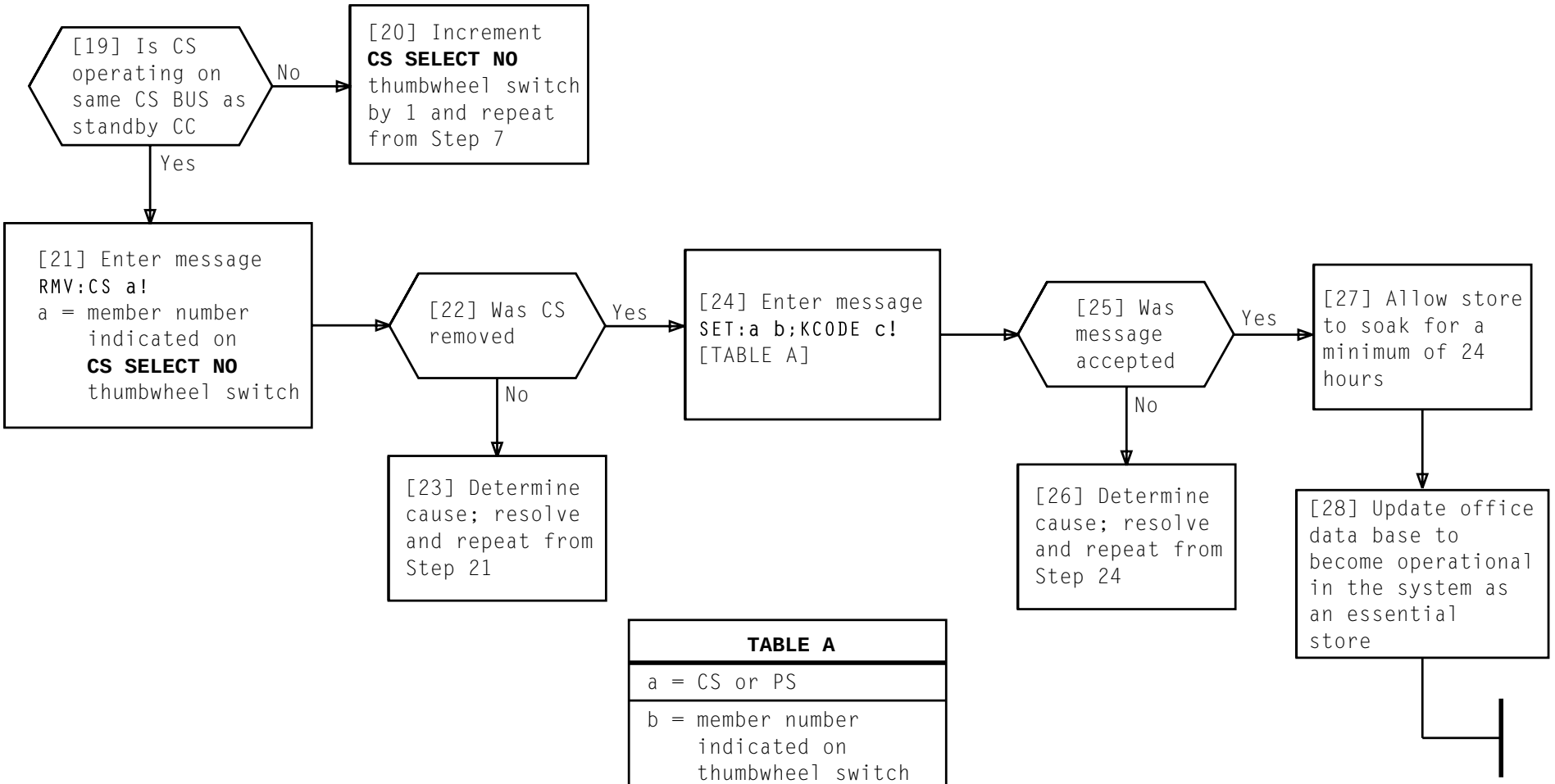
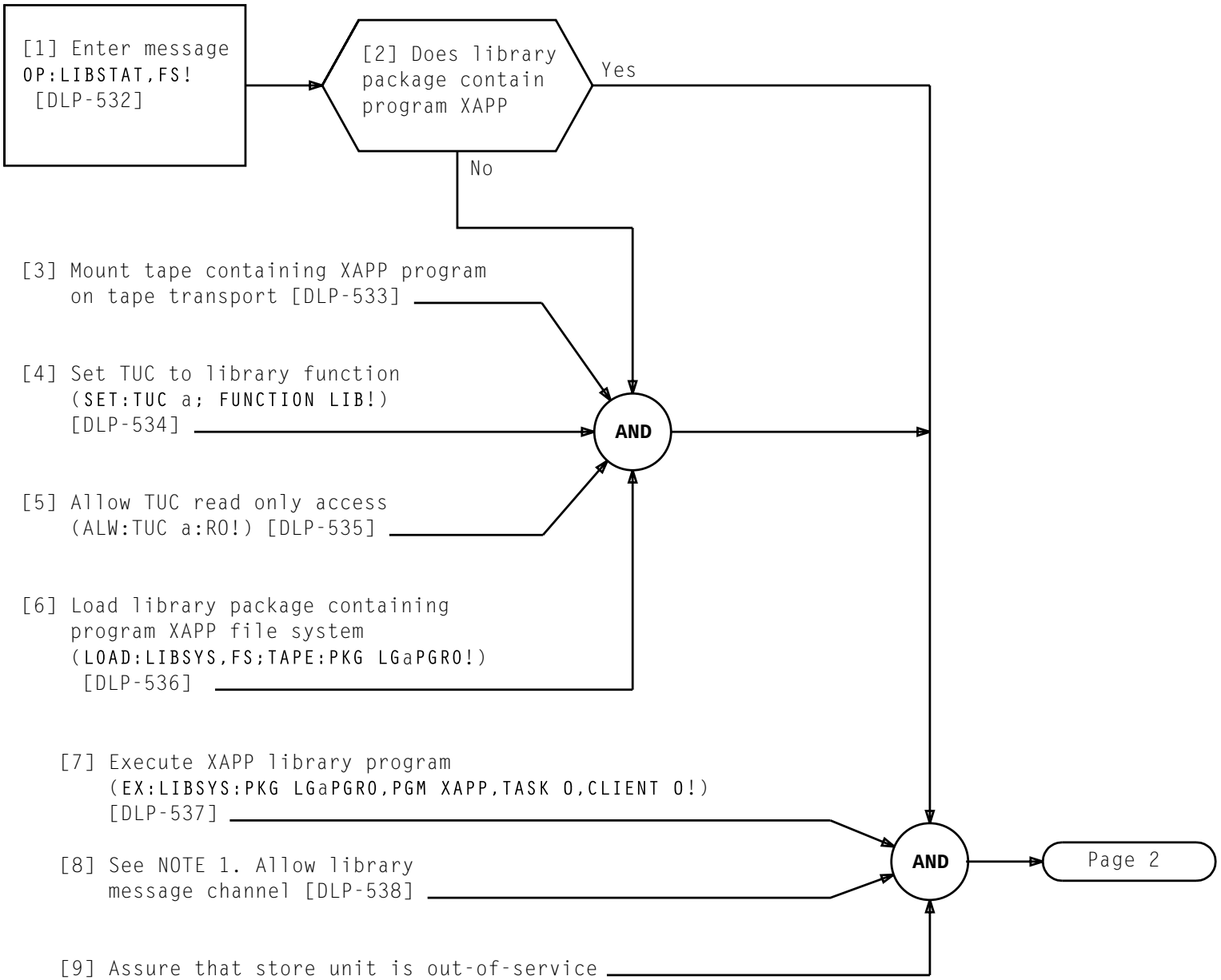


TABLE A
a = CS or PS
b = member number indicated on thumbwheel switch
c = 0 for CS, 20 for PS

CONFIGURE NEW STORE AS DUPLICATE BASE STORE, SEMICONDUCTOR STORE



NOTE 1
XAPP library program times out after 2 hours of inactivity. If XAPP does time out, items 7 and 8 must be performed before using XAPP input messages

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 1 of 5	**520**

GROW STORE FROM SPECIAL GROWTH STATE TO OPERATIONAL

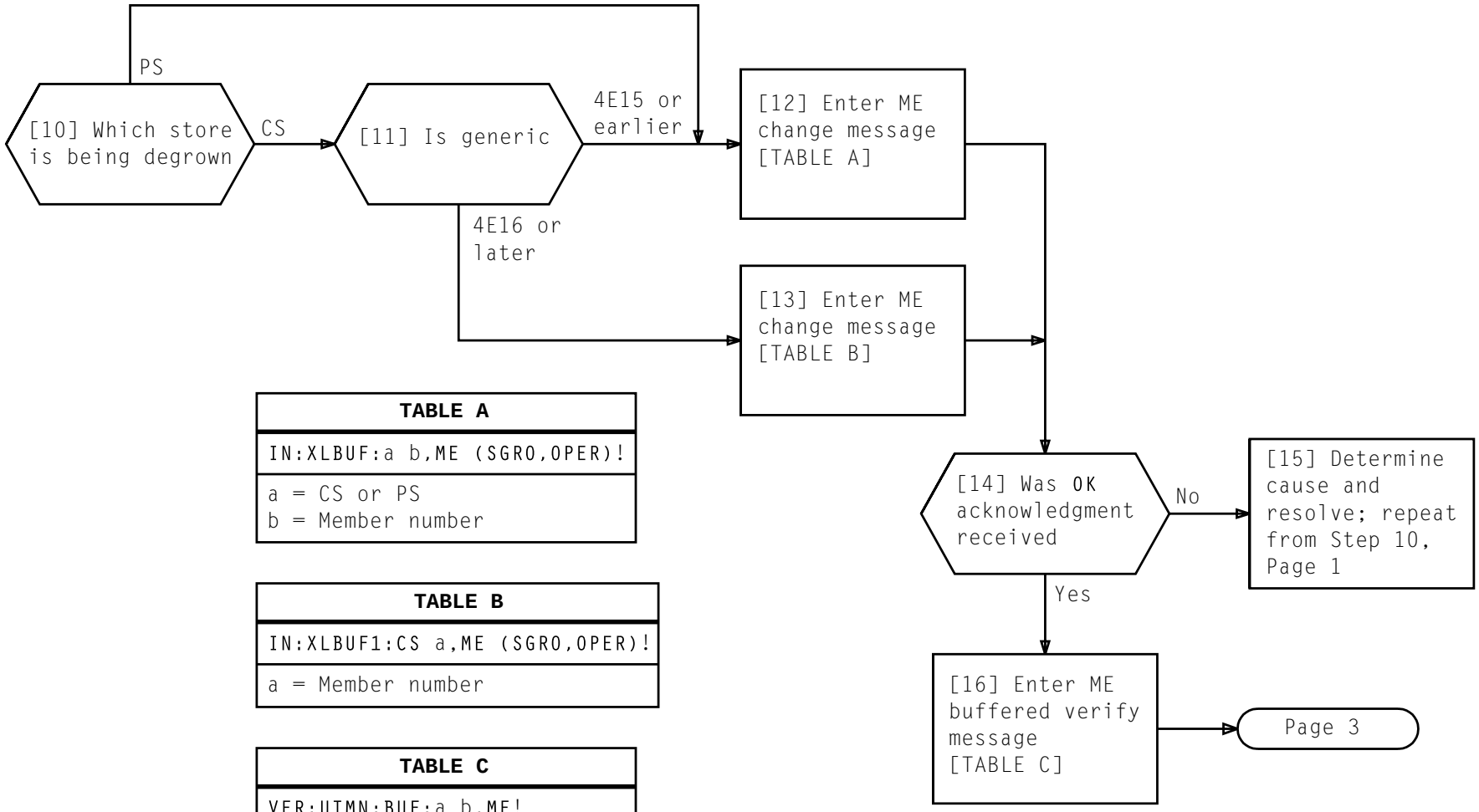


TABLE A
IN:XLBUF:a b,ME (SGRO,OPER)!
a = CS or PS b = Member number

TABLE B
IN:XLBUF1:CS a,ME (SGRO,OPER)!
a = Member number

TABLE C
VER:UTMN;BUF:a b,ME!
a = CS or PS b = Member number

GROW STORE FROM SPECIAL GROWTH STATE TO OPERATIONAL

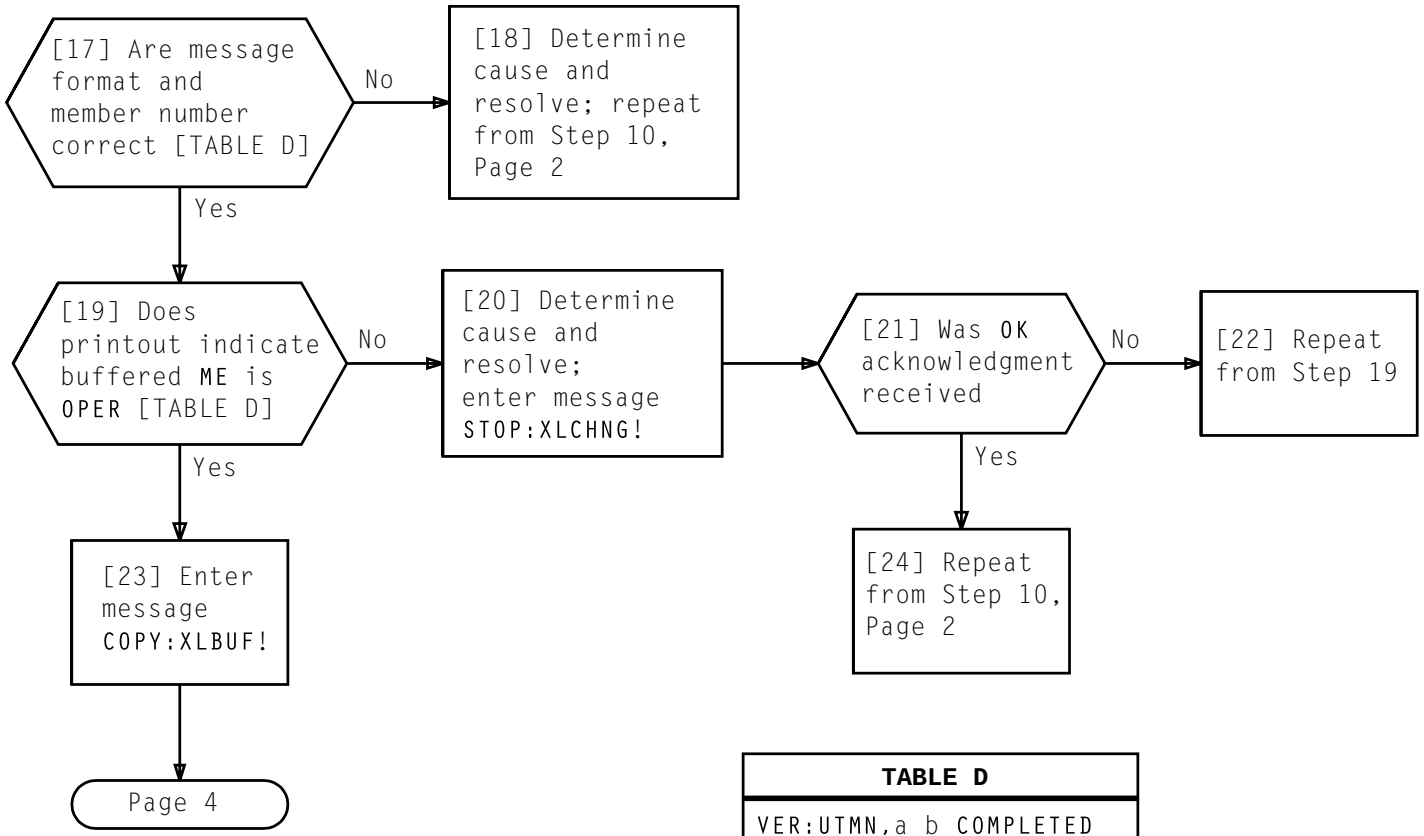


TABLE D
VER:UTMN,a b COMPLETED TRANSLATOR ADR = TRANSLATOR SIZE = BUFFERED DATA ME OPER
a = CS or PS b = Member number

GROW STORE FROM SPECIAL GROWTH STATE TO OPERATIONAL

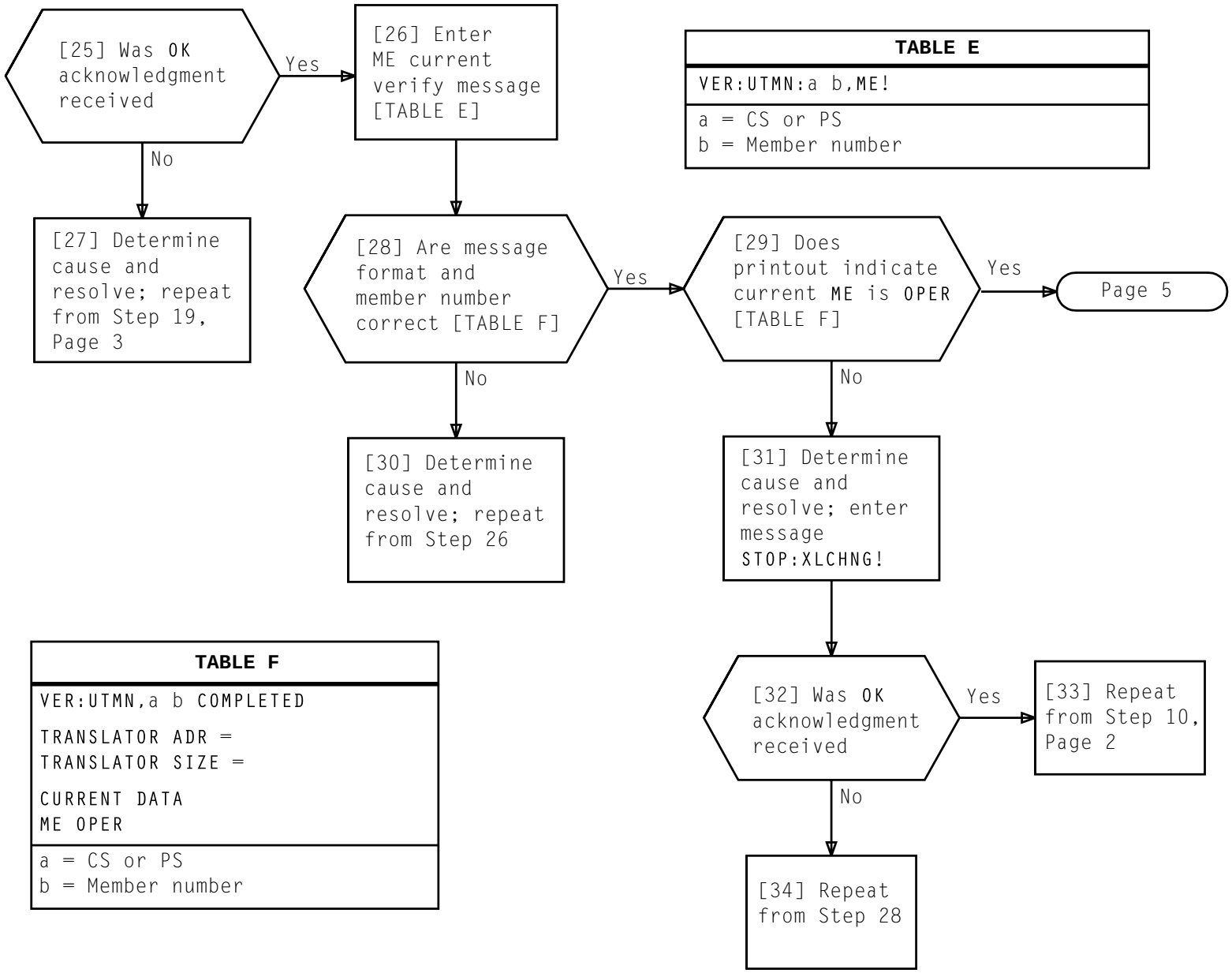


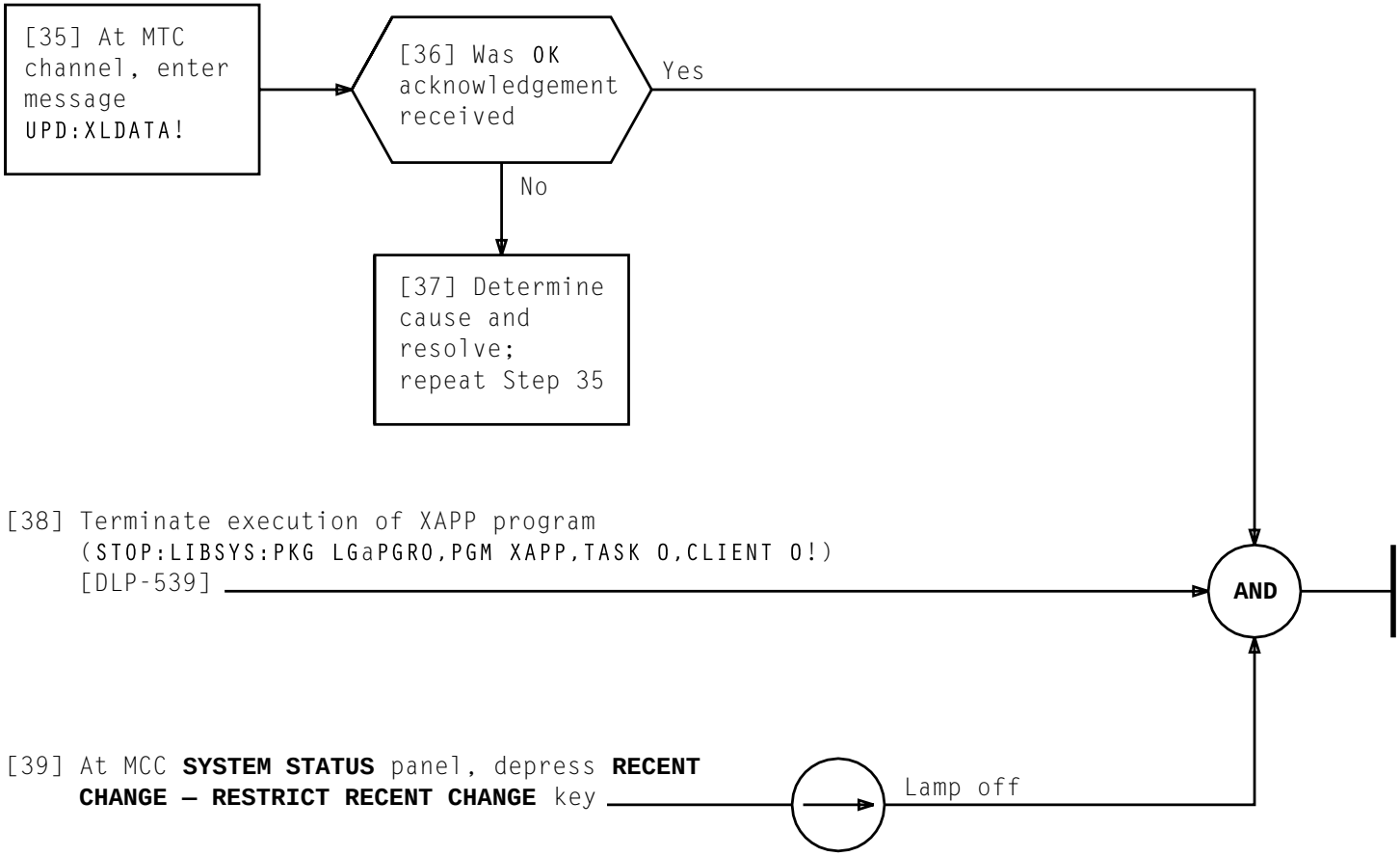
TABLE E

VER:UTMN:a b,ME!
a = CS or PS b = Member number

TABLE F

VER:UTMN,a b COMPLETED TRANSLATOR ADR = TRANSLATOR SIZE = CURRENT DATA ME OPER
a = CS or PS b = Member number

GROW STORE FROM SPECIAL GROWTH STATE TO OPERATIONAL



GROW STORE FROM SPECIAL GROWTH STATE TO OPERATIONAL

SUMMARY

Identify first failing phase, test, and address. Locate mismatch data; convert to binary and determine failing bits. Relate to SD and identify circuit pack, its input and output packs

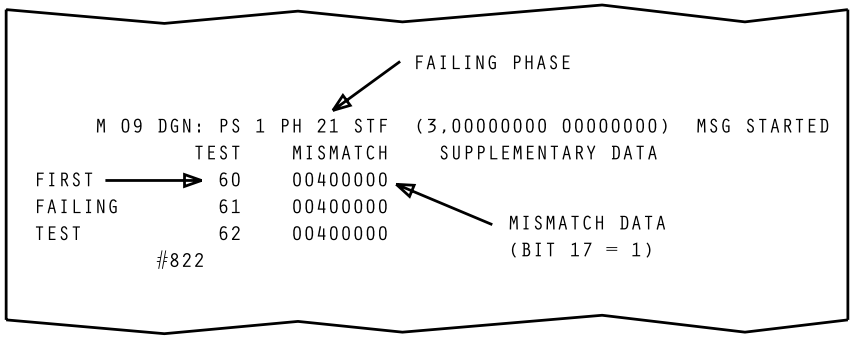


FIG. 1 – Sample of Printout

[1] See FIG. 1. Identify first failing phase on printout

[2] Using TABLE A, Page 2 identify PIDENT for first failing phase

[3] Obtain PIDENT

[4] See FIG. 1. Within PIDENT, find first failing test per printout

AND

[5] See FIG. 2, Page 4. Using PIDENT data, determine address

[6] Obtain PK TABLE B, Page 2

[7] See FIG. 3, Page 5. Within PK, locate page using address determined in Step 5 (upper left or lower left corner)

AND

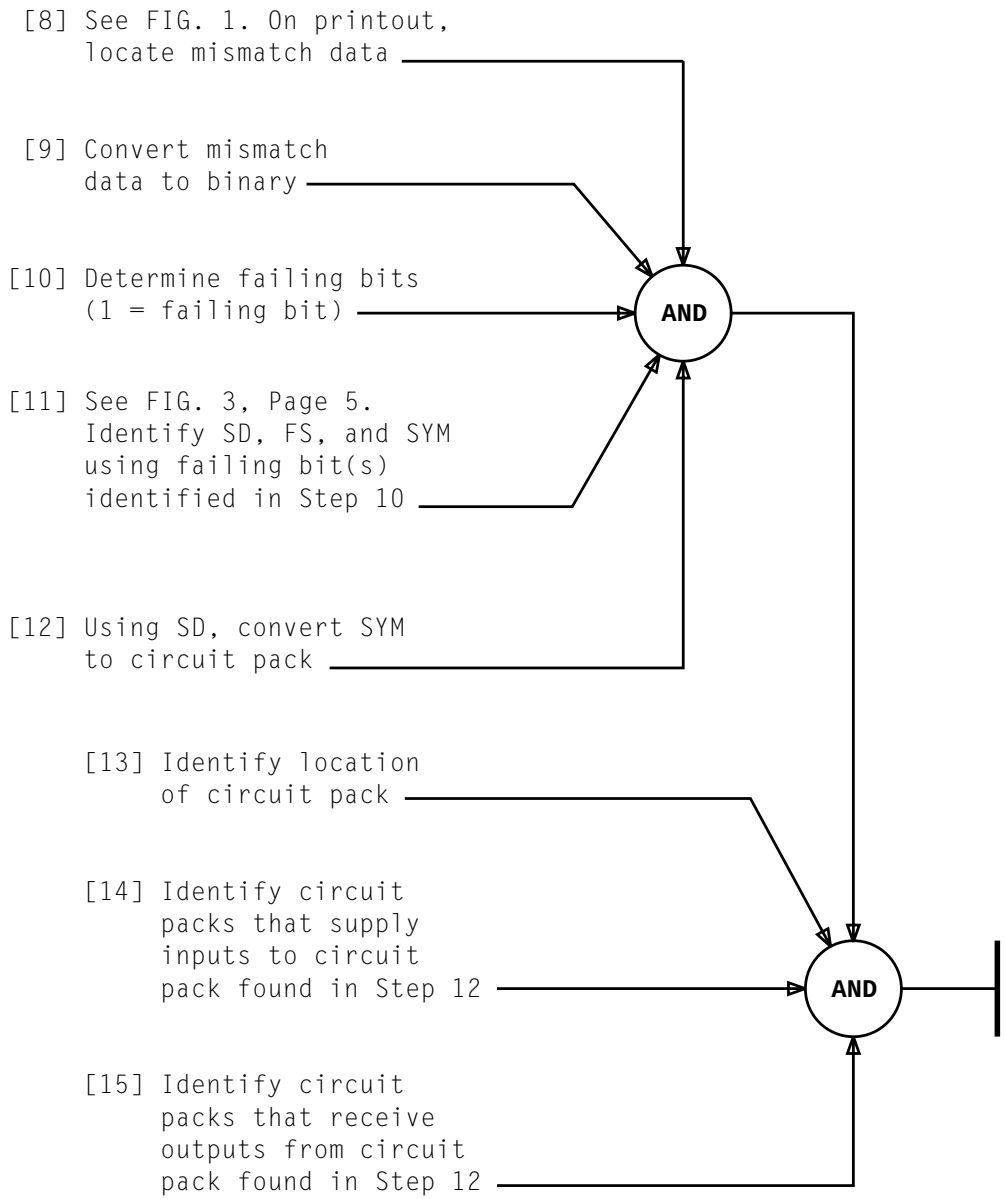
Page 3

IDENTIFY CIRCUIT PACKS AND LOCATIONS USING DIAGNOSTIC INFORMATION

TABLE A								
PHASE	SEMICONDUCTOR PIDENT		PHASE	SEMICONDUCTOR PIDENT		PHASE	SEMICONDUCTOR PIDENT	
	J5A008A	J5A010A/B		J5A008A	J5A010A/B		J5A008A	J5A010A/B
1	M2DG01	M3DG01	15	M2DG15	M3DG15	29	———	M3DG29
2	M2DG02	M3DG02	16	M2DG16	M3DG16	34	———	———
3	M2DG03	M3DG03	17	M2DG16	M3DG16	35	———	———
4	M2DG03	M3DG03	18	M2DG18	M3DG18	36	———	———
5	M2DG05	M3DG05	19	M2DG19	M3DG19	37	———	———
6	M2DG05	M3DG05	21	M2DG21	M3DG21	38	———	———
7	M2DG07	M3DG07	22	M2DG22	M3DG22	39	———	———
8	M2DG07	M3DG07	23	M2DG23	M3DG23	91	M2DG91	M3DG91
9	M2DG09	M3DG09	24	M2DG24	M3DG24	92	M2DG92	———
11	M2DG11	M3DG11	25	M2DG25	M3DG25	93	M2DG93	———
12	M2DG12	M3DG12	26	M2DG26	M3DG26	94	M2DG94	M3DG94
13	M2DG13	M3DG13	27	M2DG27	M3DG27	97	M2DG97	M3DG97
14	M2DG14	M3DG14	28	M2DG28	M3DG28			

TABLE B	
TYPE STORE	PK & SD
Semiconductor J5A008A	5A040
Semiconductor J5A010A J5A010B	5A053 5A059

IDENTIFY CIRCUIT PACKS AND LOCATIONS USING DIAGNOSTIC INFORMATION



IDENTIFY CIRCUIT PACKS AND LOCATIONS USING DIAGNOSTIC INFORMATION

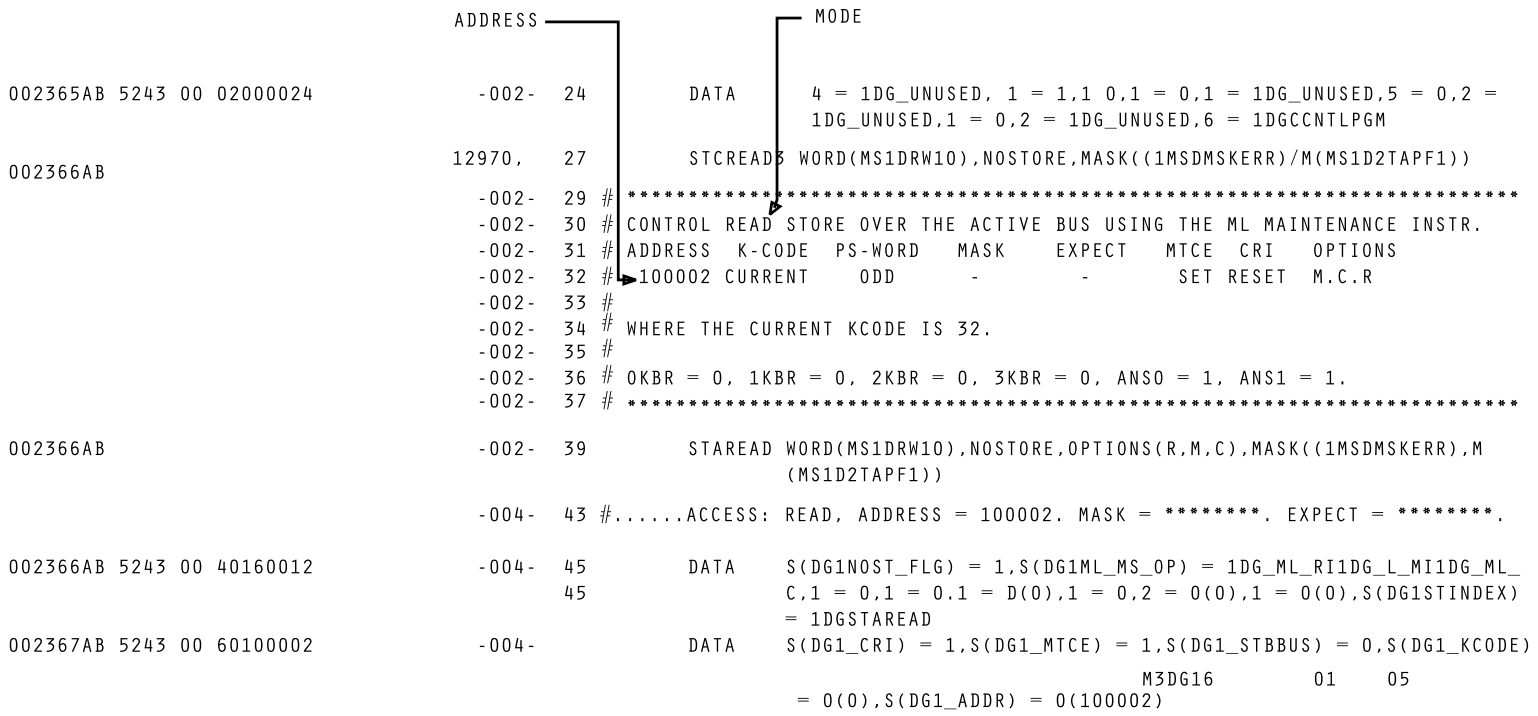


FIG. 2 – Sample Portion of Program Listing (PR)

MODE=READ CONTROL READ 10

ADDRESS ESS=6100002

COMPOOL MNEMONIC = DRW10
SD-5A053-01
GATEOUT ENABLE: CR101

SD-5A053
FS 1
SYM3

FAILING
BIT

BIT	OP	FUNCTION COMPOOL NAME	ALIAS	SD	FS/SYM	LEAD DESIG	CPS REG/GATE NAME	DESCRIPTION*
00		TRFA001		53	1/3	C000	TRFA00	TRAP REFRESH ADDRESS REGISTER BIT 00
01		TRFA011		53	1/3	C010	TRFA01	TRAP REFRESH ADDRESS REGISTER BIT 01
02		TRFA021		53	1/3	C020	TRFA02	TRAP REFRESH ADDRESS REGISTER BIT 02
03		TRFA031		53	1/3	C030	TRFA03	TRAP REFRESH ADDRESS REGISTER BIT 03
04		TRFA041		53	1/3	C040	TRFA04	TRAP REFRESH ADDRESS REGISTER BIT 04
05		TRFA051		53	1/3	C050	TRFA05	TRAP REFRESH ADDRESS REGISTER BIT 05
06		TRFA061		53	1/3	C060	TRFA06	TRAP REFRESH ADDRESS REGISTER BIT 06
07		TRFA071		53	1/3	C070	TRFA07	TRAP REFRESH ADDRESS REGISTER BIT 07
08		TRFA081		53	1/3	C080	TRFA08	TRAP REFRESH ADDRESS REGISTER BIT 08
09		TRFA091		53	1/3	C090	TRFA09	TRAP REFRESH ADDRESS REGISTER BIT 09
10		TRFA101		53	1/3	C100	TRFA10	TRAP REFRESH ADDRESS REGISTER BIT 10
11		TRFA111		53	1/3	C110	TRFA11	TRAP REFRESH ADDRESS REGISTER BIT 11
12		TRFA121		53	1/3	C120	TRFA12	TRAP REFRESH ADDRESS REGISTER BIT 12
13		TRFA131		53	1/3	C130	TRFA13	TRAP REFRESH ADDRESS REGISTER BIT 13
14		TRFA141		53	1/3	C140	TRFA14	TRAP REFRESH ADDRESS REGISTER BIT 14
15		TRFA151		53	1/3	C150	TRFA15	TRAP REFRESH ADDRESS REGISTER BIT 15
16		TRFA161		53	1/3	C160	TRFA16	TRAP REFRESH ADDRESS REGISTER BIT 16
17		TRFA171		53	1/3	C170	TRFA17	TRAP REFRESH ADDRESS REGISTER BIT 17
18		TRFDPF1		53	1/2	TRFDPF1	TRFDPF	OUTPUT OF TRFDPF FF
19								UNUSED
20								UNUSED
21		1		53	1/3	C210	VB	256K SEMICONDUCTOR STORE FLAG BIT
22		0/		53	1/3	C220		256K SEMICONDUCTOR STORE FLAG BIT (0 = SLOW ONLY, 1 = SLOW OR FAST)
23		0		53	1/3	C230		256K SEMICONDUCTOR STORE FLAG BIT

MODE = READ
ADDRESS = 100002

* NONE OF THE TRAP REFRESH ADDRESS REGISTER OUTPUTS, TRFA00 THROUGH TRFA17, ARE DIRECTLY ACCESSIBLE FROM CIRCUIT-PACK PINS. THESE OUTPUTS CAN BE READ OUT VIA CONTROL READ DATA BITS 00 THROUGH 17.

SEMICONDUCTOR CALL STORE/PROGRAM STORE TEST ACCESS ISSUE 1 PK-5A053-01-C9

FIG. 3 — Sample Portion of Datapool Listing (PK)

1. Use failing phase on printout to obtain PIDENT for first failing test [TABLE A, Page 2]

2. Locate TEST NUMBER INDEX page near end of PR [FIG. 1, Page 3]

3. Locate first failing test on TEST NUMBER INDEX page

4. After failing test, locate and record LOC

5. After failing test, locate and record looping ADR

End of procedure

DETERMINE LOOPING PARAMETERS

TABLE A								
PHASE	SEMICONDUCTOR PIDENT		PHASE	SEMICONDUCTOR PIDENT		PHASE	SEMICONDUCTOR PIDENT	
	J5A008A	J5A010A/B		J5A008A	J5A010A/B		J5A008A	J5A010A/B
1	M2DG01	M3DG01	15	M2DG15	M3DG15	29	———	M3DG29
2	M2DG02	M3DG02	16	M2DG16	M3DG16	34	———	———
3	M2DG03	M3DG03	17	M2DG16	M3DG16	35	———	———
4	M2DG03	M3DG03	18	M2DG18	M3DG18	36	———	———
5	M2DG05	M3DG05	19	M2DG19	M3DG19	37	———	———
6	M2DG05	M3DG05	21	M2DG21	M3DG21	38	———	———
7	M2DG07	M3DG07	22	M2DG22	M3DG22	39	———	———
8	M2DG07	M3DG07	23	M2DG23	M3DG23	91	M2DG91	M3DG91
9	M2DG09	M3DG09	24	M2DG24	M3DG24	92	M2DG92	———
11	M2DG11	M3DG11	25	M2DG25	M3DG25	93	M2DG93	———
12	M2DG12	M3DG12	26	M2DG26	M3DG26	94	M2DG94	M3DG94
13	M2DG13	M3DG13	27	M2DG27	M3DG27	97	M2DG97	M3DG97
14	M2DG14	M3DG14	28	M2DG28	M3DG28			

DETERMINE LOOPING PARAMETERS

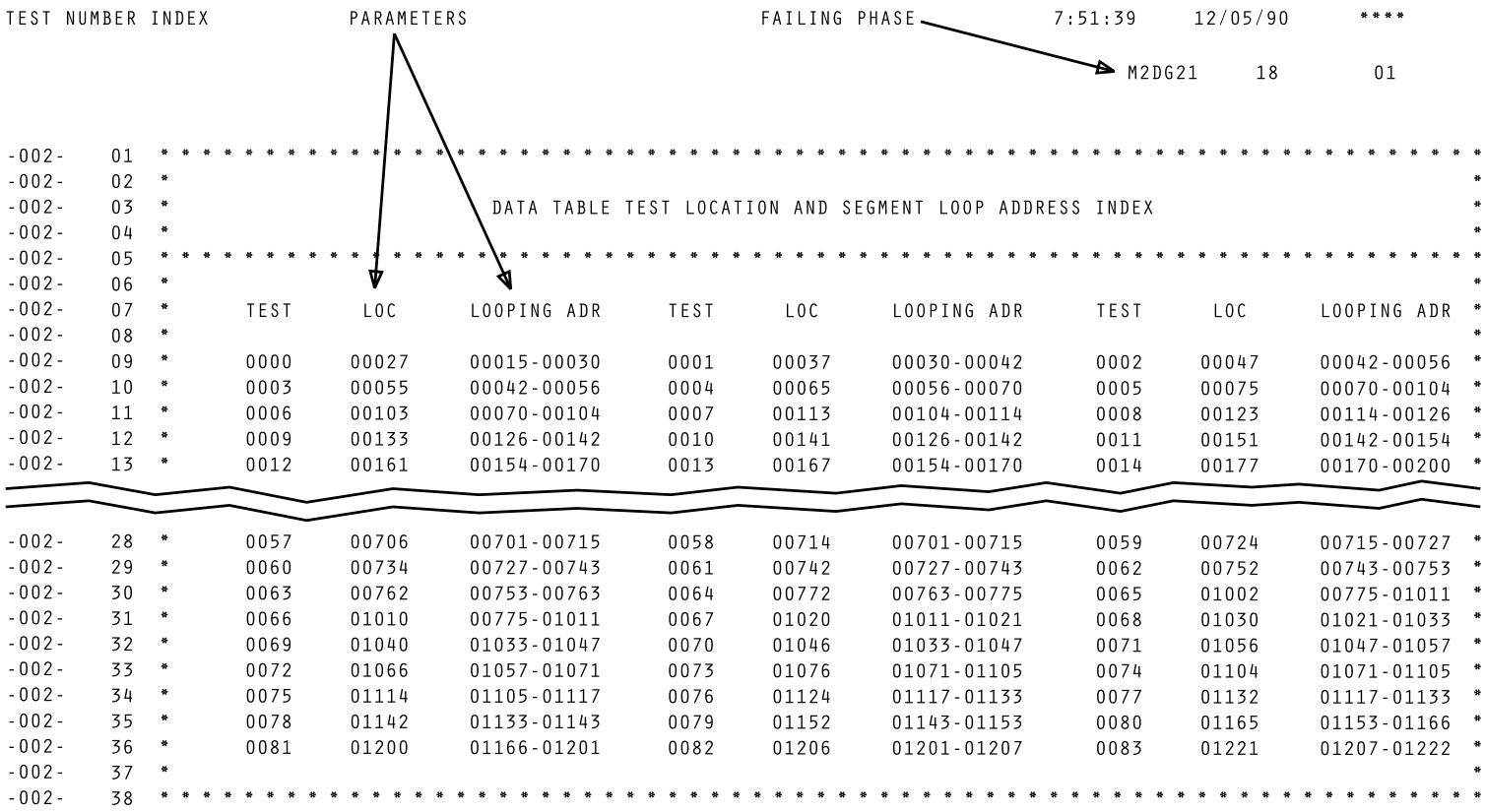


FIG. 1

DETERMINE LOOPING PARAMETERS

At front of store [FIG. 1 — J5A008A or FIG. 2 — J5A010A or FIG. 3 J5A010B]:

[1] Depress **ROS/OFF** switch

PWR OFF lamp lights

[2] Select pack to be replaced

[3] See WARNING 1. Release lock on latch and remove circuit pack

AND

[4] Clean and lubricate replacement circuit pack

[5] Insert new circuit pack; ensure it is firmly seated and latch is secured

[6] Depress **ON** pushbutton

PWR OFF lamp is off

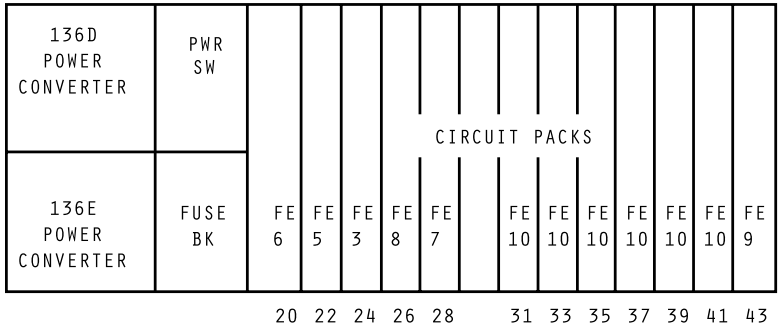


FIG. 1 — Front View — Semiconductor Store J5A008A

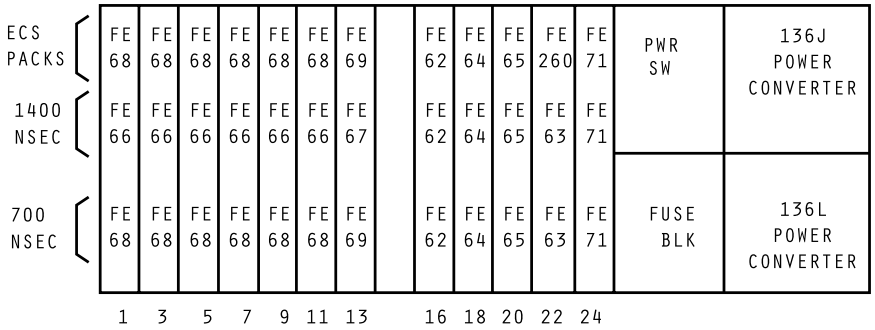


FIG. 2 — Front View — Semiconductor Store J5A010A

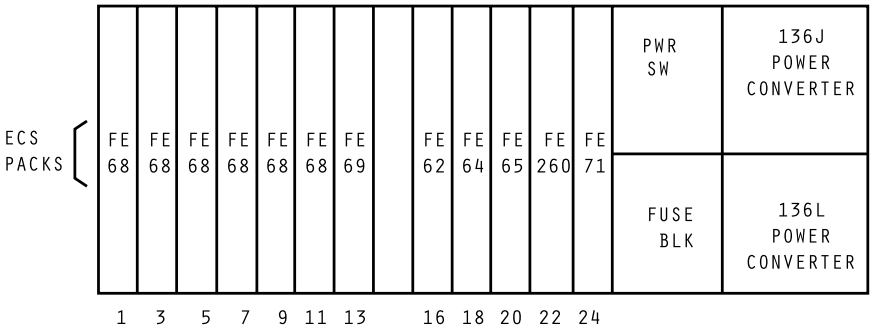
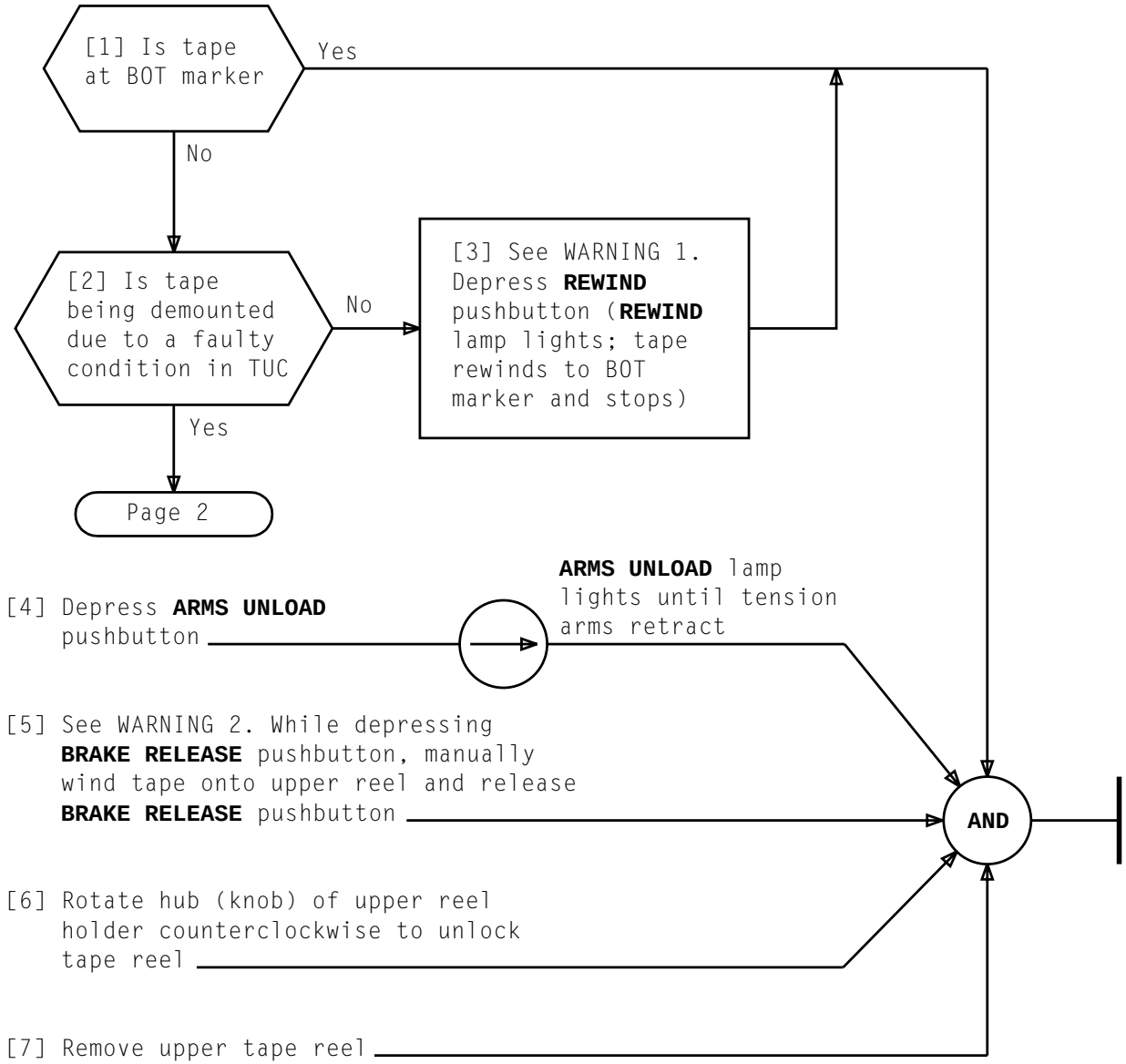


FIG 3 — Front View — Semiconductor Store J5A010B

WARNING 1
An antistatic wrist strap must be worn to prevent electrostatic discharge and possible damage to circuit pack while handling

REPLACE CIRCUIT PACK, SEMICONDUCTOR STORE J5A008A OR J5A010A or J5A010B

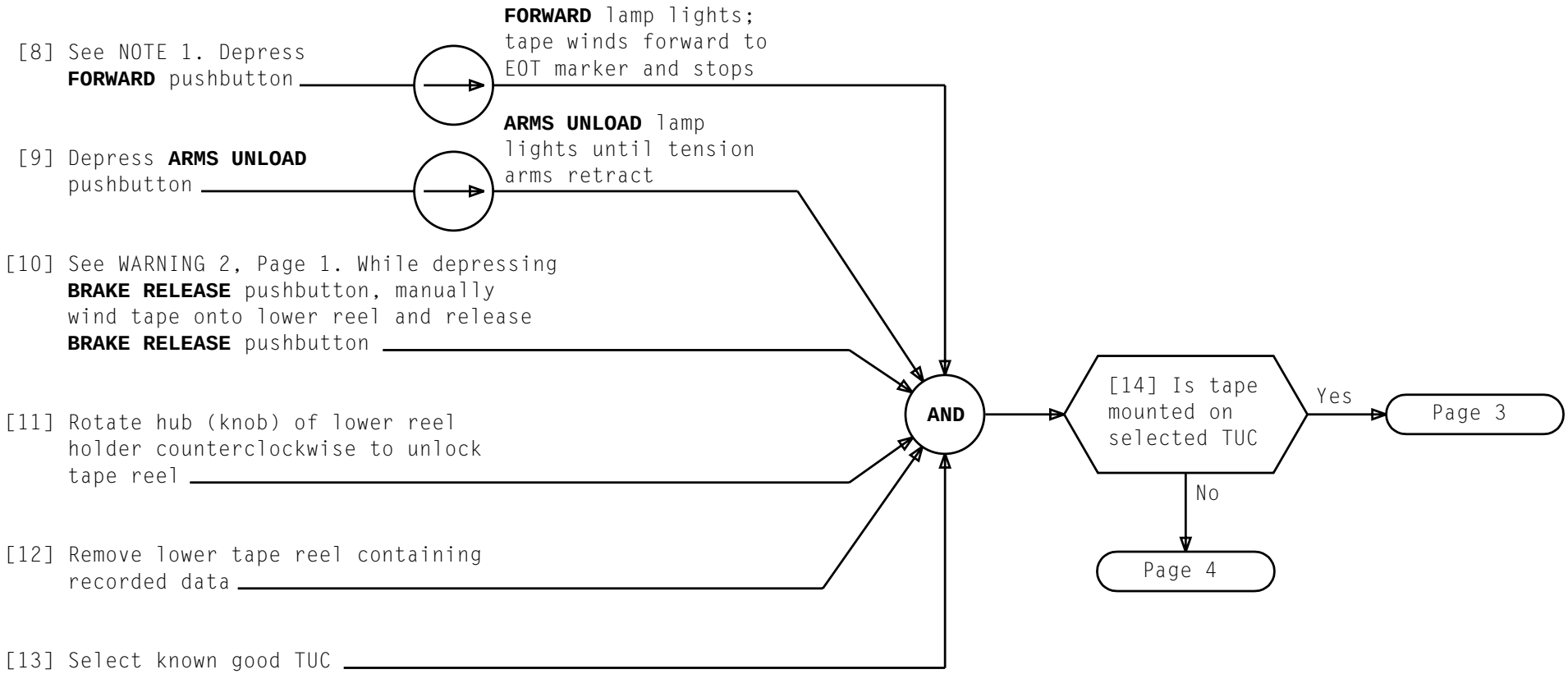
Issue 7	NOV 1993
254-251-005	DLP
PAGE 1 of 1	523



WARNINGS

1. *If alignment tape is mounted, use REVERSE pushbutton to rewind tape*
2. *Pulling or dragging last 5 feet of tape across heads may contaminate heads*

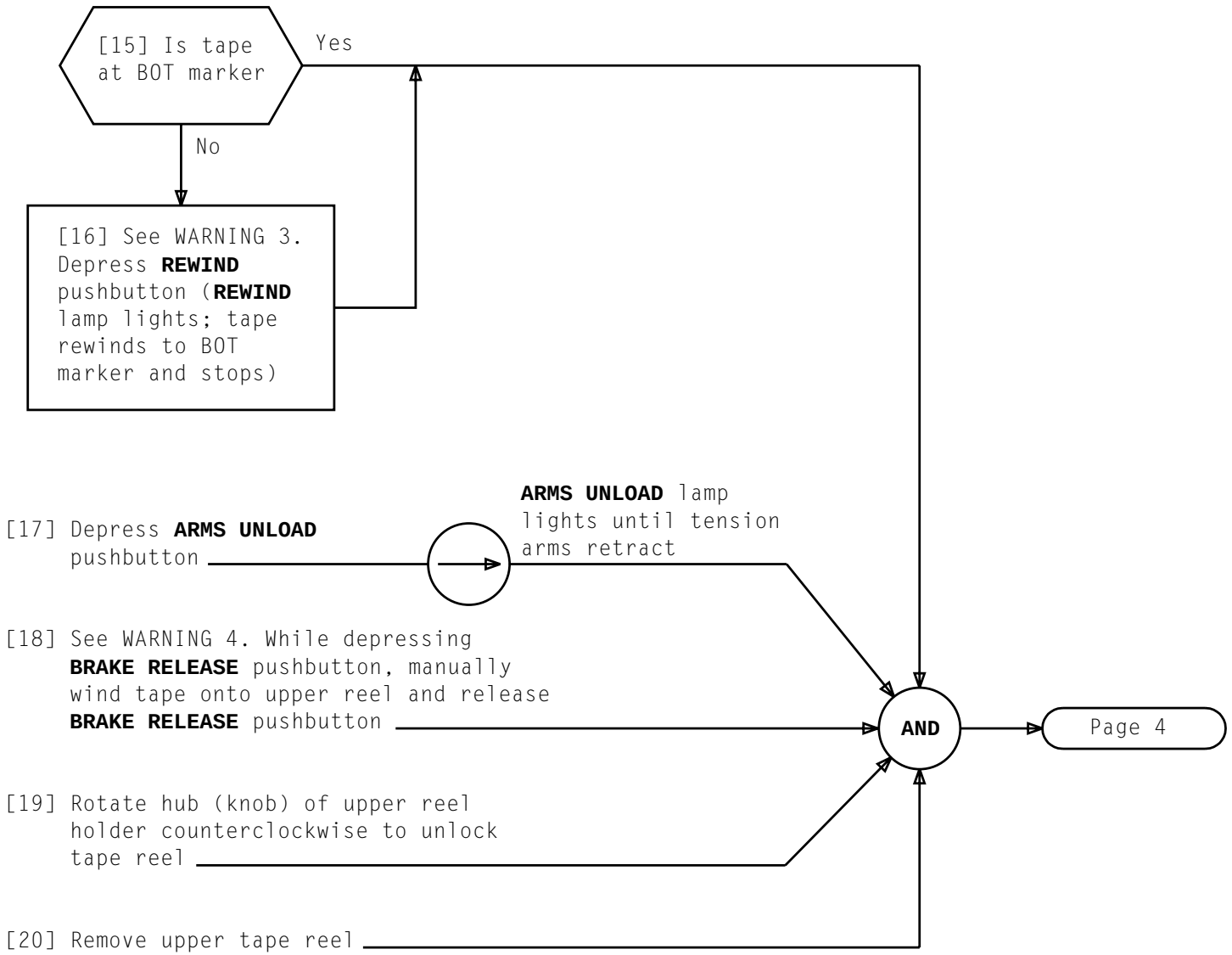
DEMOUNT TAPE ON TAPE TRANSPORT



NOTE 1

Steps 8 through 37 are being performed to prevent possible loss of recorded data

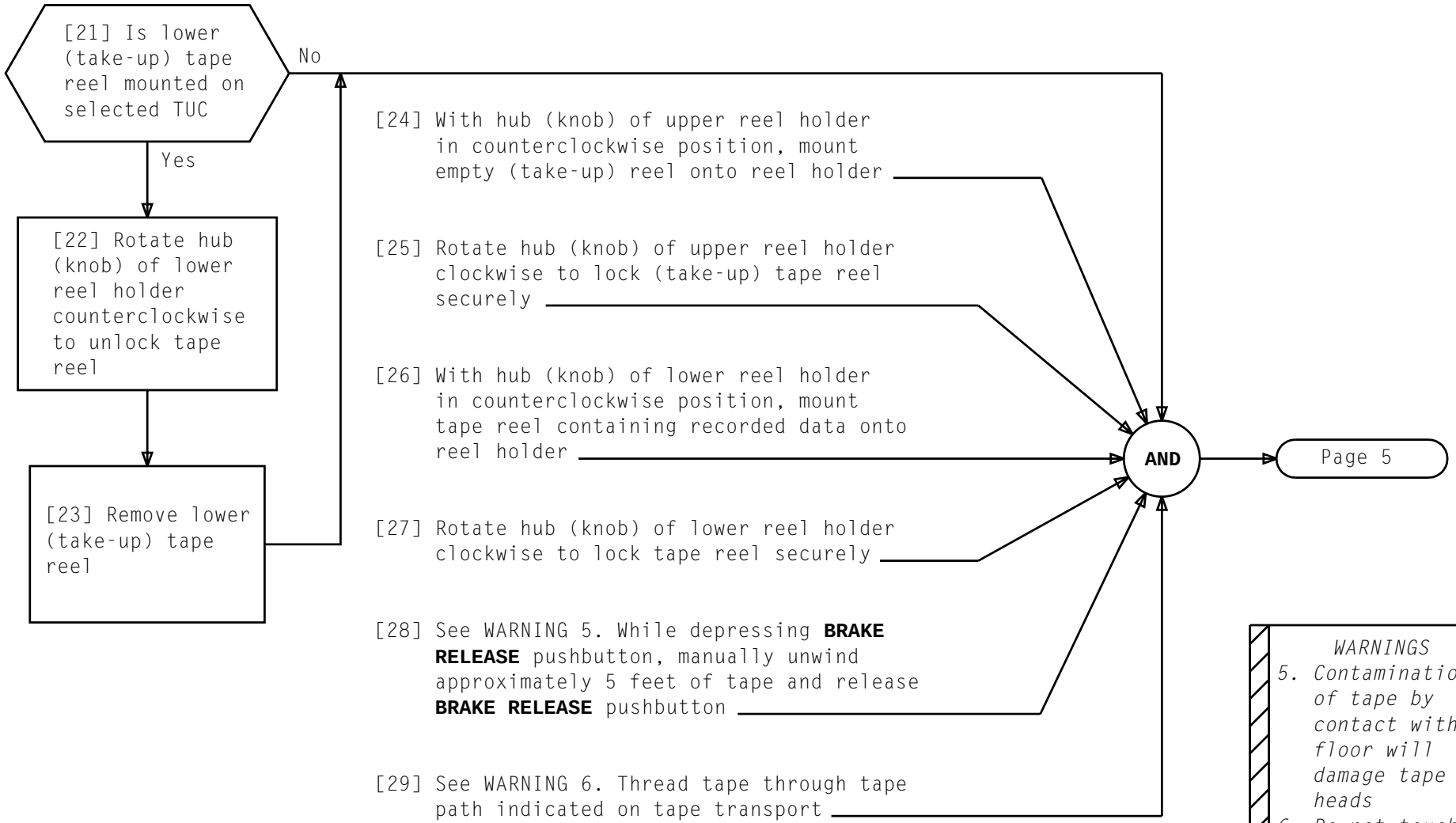
DEMOUNT TAPE ON TAPE TRANSPORT



WARNINGS

3. *If alignment tape is mounted, use REVERSE pushbutton to rewind tape*
4. *Pulling or dragging last 5 feet of tape across heads may contaminate heads*

DEMOUNT TAPE ON TAPE TRANSPORT

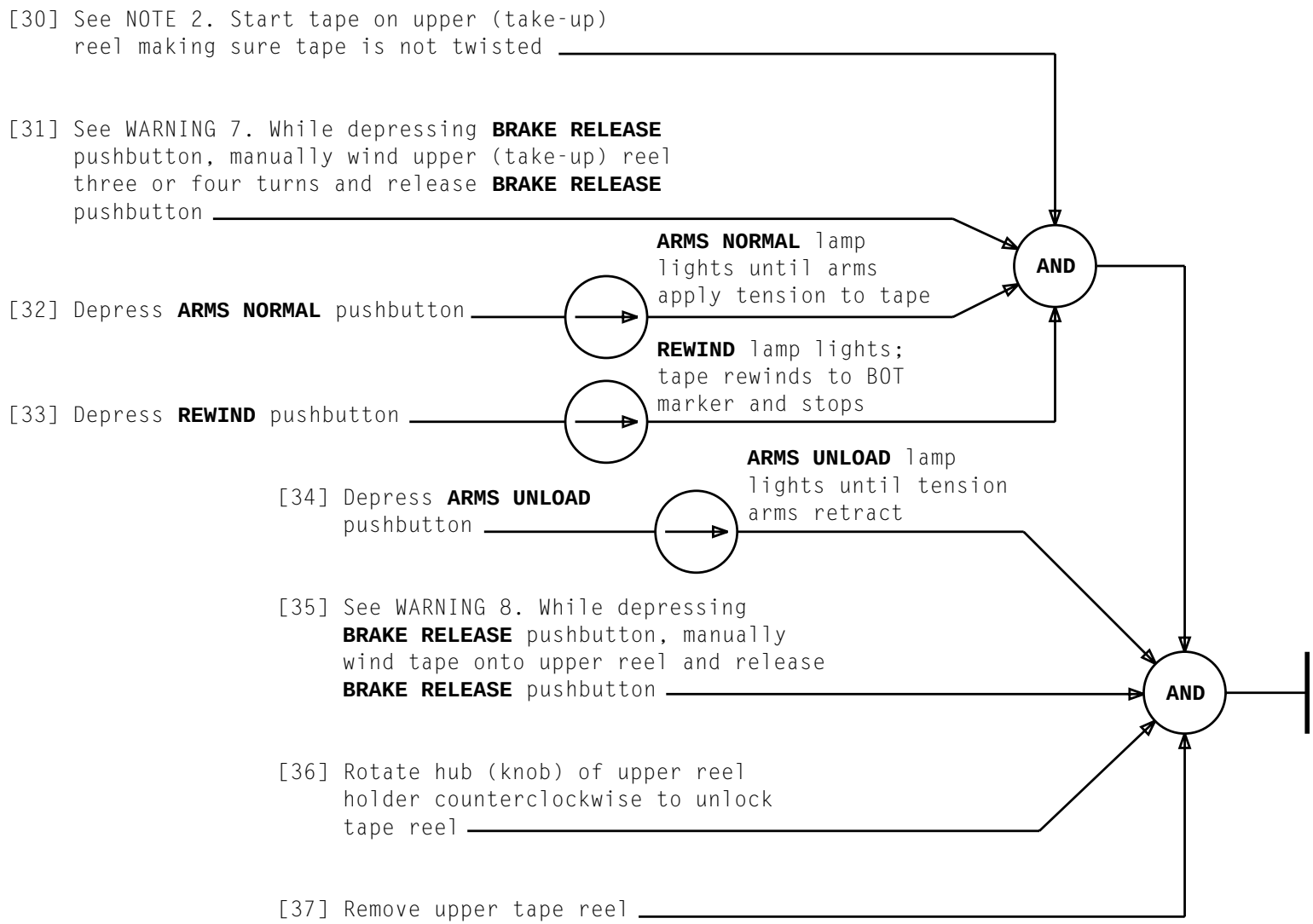


WARNINGS

5. *Contamination of tape by contact with floor will damage tape heads*
6. *Do not touch tape head surfaces; body oil will contaminate tape*

DEMOUNT TAPE ON TAPE TRANSPORT

DEMOUNT TAPE ON TAPE TRANSPORT



NOTE 2

To start tape on take-up reel, it may help to moisten tape end (moistened fingers) and stick tape to reel axle

WARNINGS

7. *If tape is not properly aligned along rollers and guides or is too loose, it may be damaged*
8. *Pulling or dragging last 5 feet of tape across heads may contaminate heads*

SUMMARY

Open cover door and operate **LOCAL/REMOTE** switch, then mount reel. Thread tape and turn take-up reel two or three turns and release break. Depress **ARMS NORMAL** pushbutton, then **FORWARD** pushbutton; obtain **25 IPS** and remote conditions and close door

At tape transport:

[1] Open interlocked cover door; at upper right of tape transport, pull interlock plunger out

[2] Operate **LOCAL/REMOTE** switch to obtain **LOCAL** lighted condition

LOCAL lamp lighted

[3] Verify that empty lower (take-up) tape reel is same size or larger than tape reel to be mounted

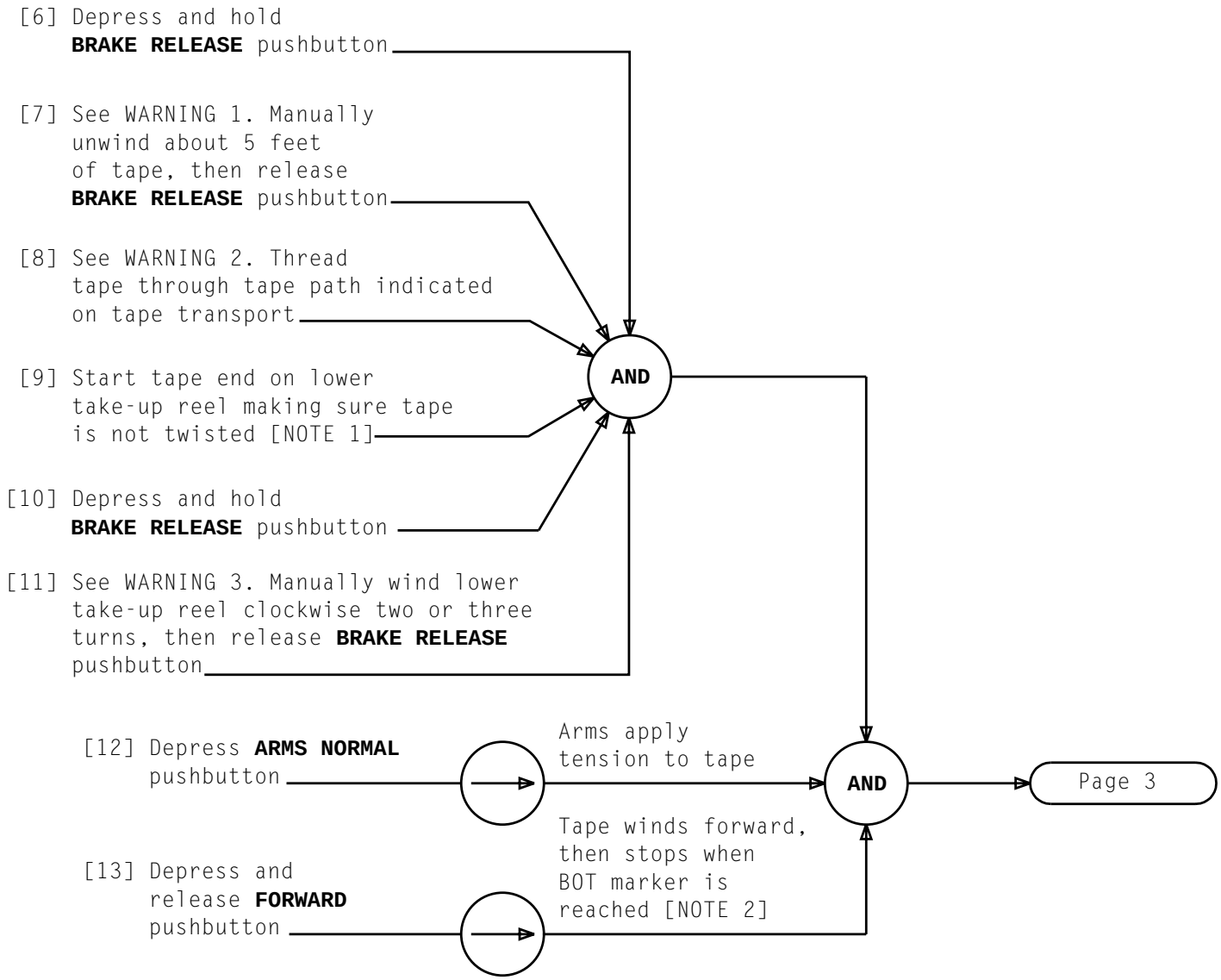
[4] With hub (knob) of upper reel in counterclockwise position, mount reel with tape on reel holder

[5] Rotate hub (knob) of upper reel clockwise to detent to lock tape reel securely

AND

Page 2

MOUNT TAPE ON TRANSPORT UNIT



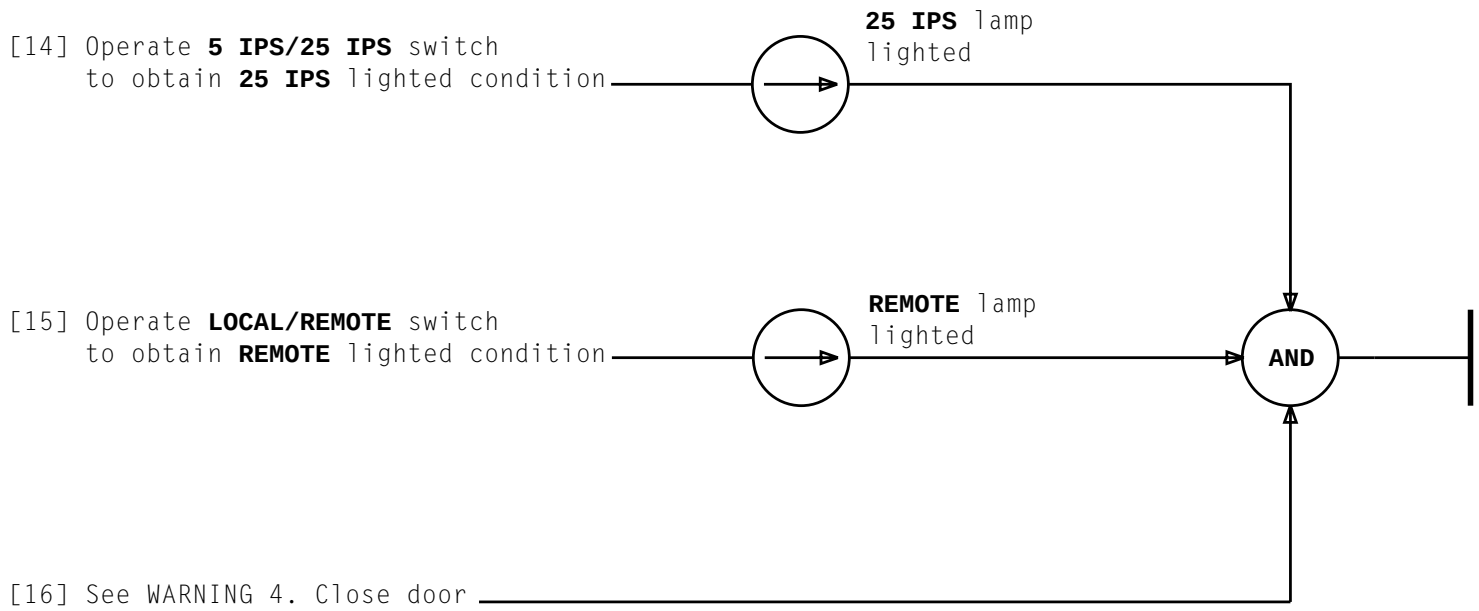
NOTES

1. To start tape on take-up reel, it may help to moisten the tape end (moistened fingers) and stick it to the reel axle
2. Tape may not stop at BOT marker if **FAST FORWARD** is depressed

WARNINGS

1. *Contamination of tape by contact with floor damages tape heads*
2. *Tape head surfaces should not be touched; body oils contaminate tape*
3. *If tape is not properly aligned along rollers and guides or is too loose, it may be damaged*

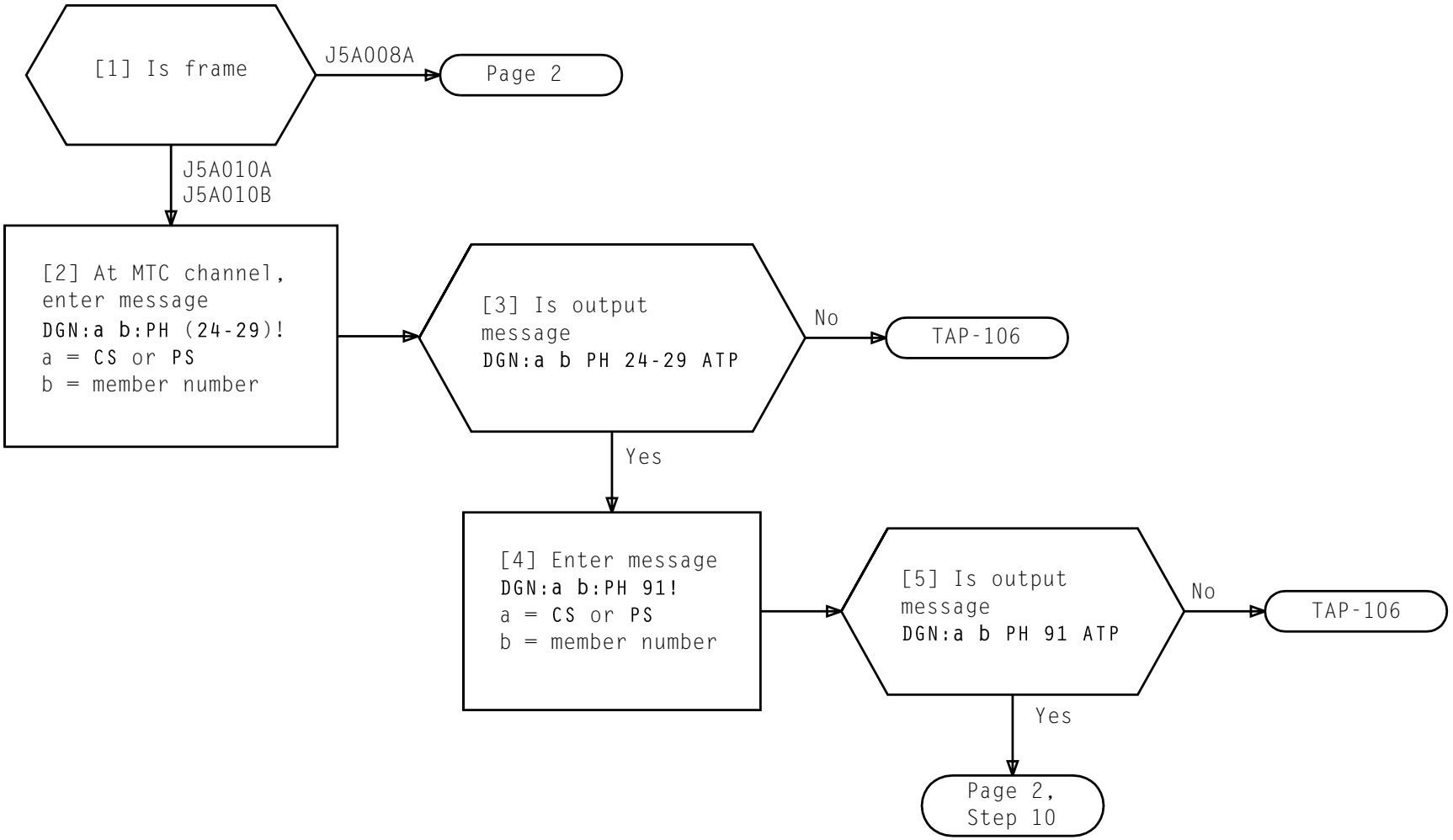
MOUNT TAPE ON TRANSPORT UNIT



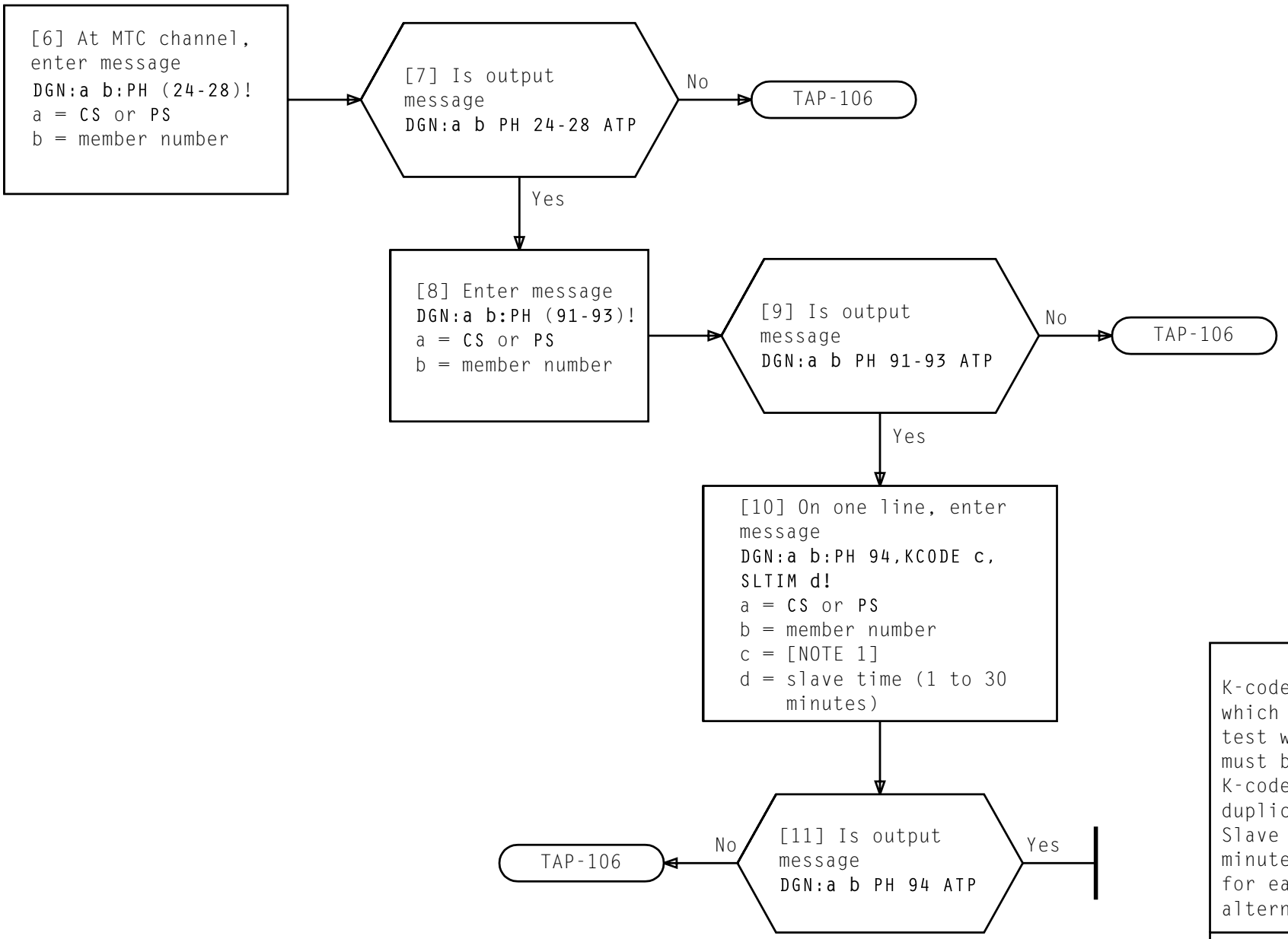
WARNING 4
Closing tape transport door in a harsh manner may upset alignment

Issue 7	**NOV 1993**
254-251-005	**DLP**
PAGE 3 of 3	**525**

MOUNT TAPE ON TRANSPORT UNIT



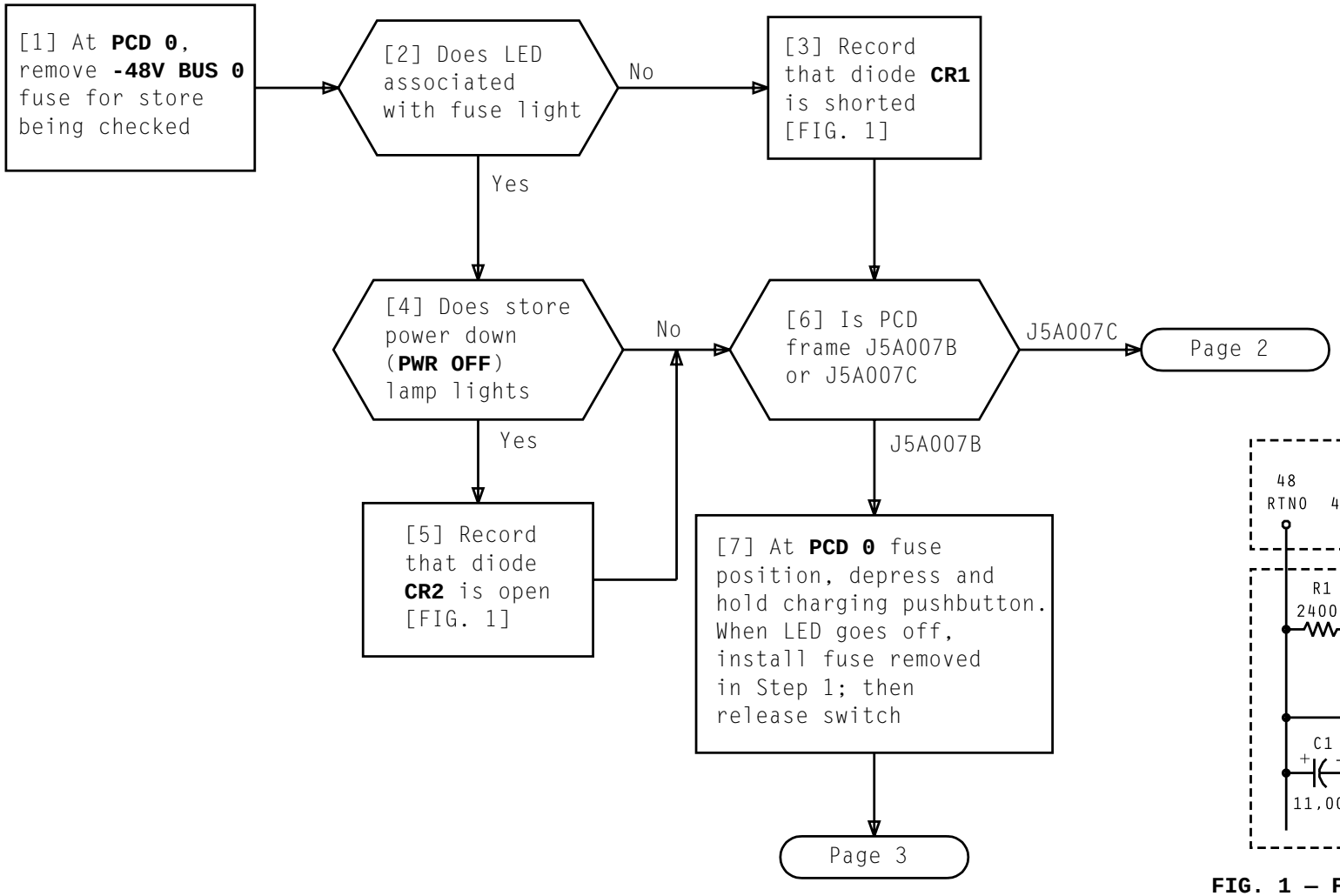
PERFORM MEMORY AND SLAVE TESTS, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



NOTE 1
K-code of unit to which unit under test will be slaved must be a valid K-code and not duplicated.
Slave time of 10 minutes is suggested for each K-code alternately

PERFORM MEMORY AND SLAVE TESTS, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

SUMMARY	
At **PCD 0,** remove **-48V BUS 0** fuse for store. LED lights and store stays up for no-fault condition. LED remains off or	LED lights and store goes down for faulty diode condition. Repeat at **PCD 1 -48V BUS 1**. Replace any diodes found to be open or shorted



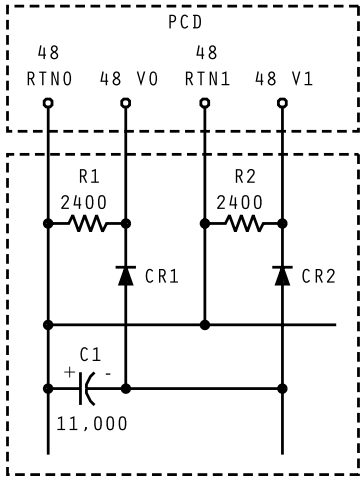


FIG. 1 — Fuse to Diode Layout

CHECK -48V ORED DIODES, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

At **PCD 0**:

[8] Remove fuse indicator associated with **-48V BUS 0** fuse removed in Step 1, Page 1

[9] See WARNING 1. Insert input of charge probe into panel charge jack

[10] Insert opposite end of charge probe into indicator holder

CHARGE MONITOR LED lights

CHARGE MONITOR LED goes off

[11] Depress and hold charge switch

AND

Page 3

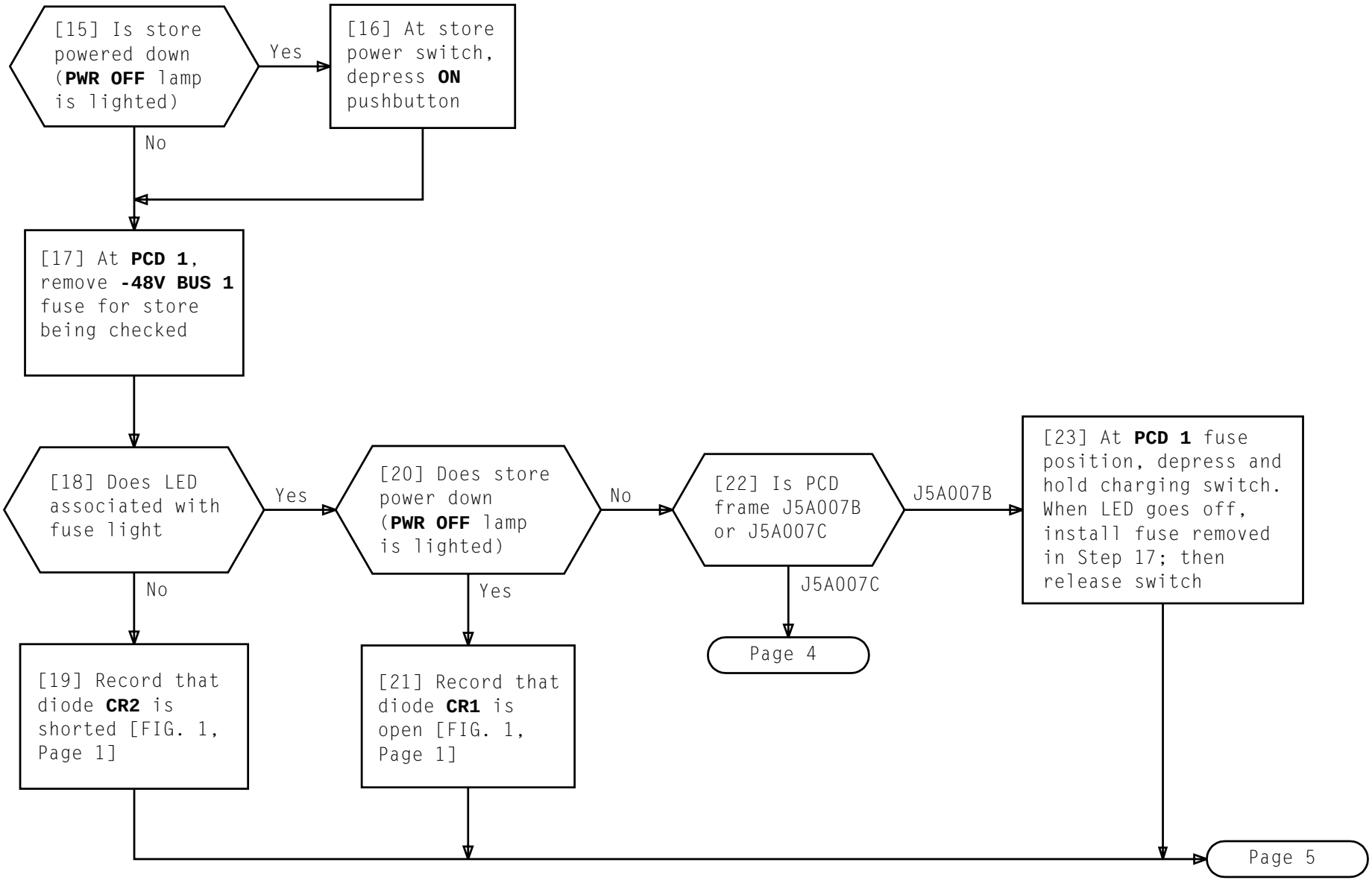
[12] Insert **-48V BUS 0** fuse removed in Step 1, Page 1 into fuse holder

[13] Release charge switch and remove charge probe from indicator holder

[14] Insert fuse indicator removed in Step 8 into indicator holder

WARNING 1
Voltage may be present on opposite end of probe; equipment damage possible if grounded

CHECK -48V ORED DIODES, SEMICONDUCTOR STORE J5A008A OR J5A010B



CHECK -48V ORED DIODES, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

At **PCD 1**:

[24] Remove fuse indicator associated with **-48V BUS 1** fuse removed in Step 17, Page 3

[25] See WARNING 2. Insert input of charge probe into panel charge jack

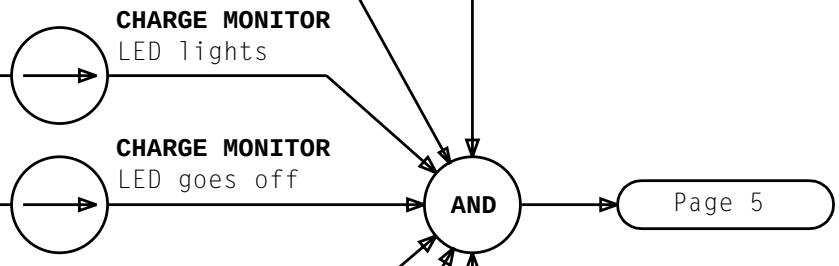
[26] Insert opposite end of charge probe into indicator holder

[27] Depress and hold charge switch

[28] Insert **-48V BUS 1** fuse removed in Step 17, Page 3 into fuse holder

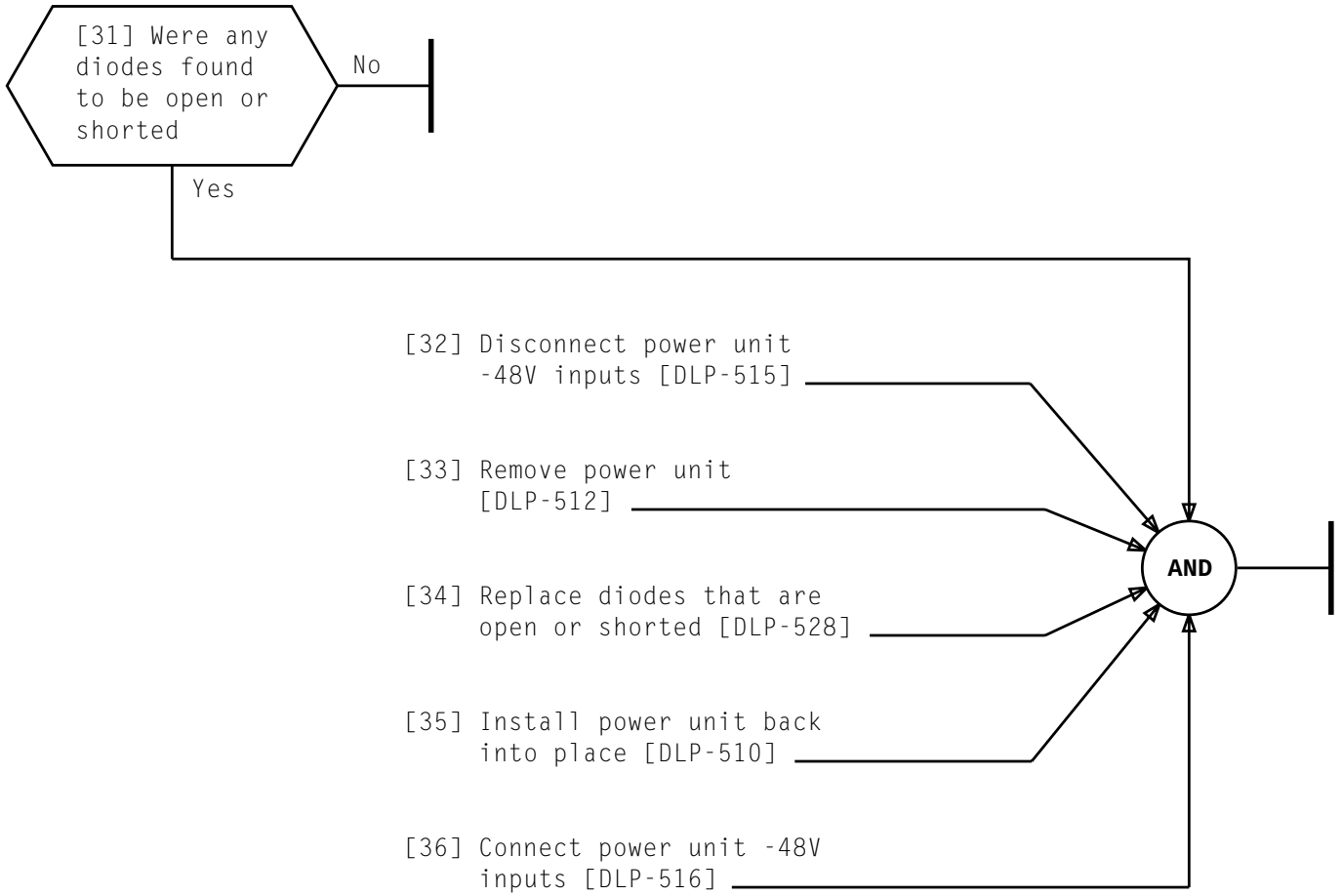
[29] Release charge switch and remove charge probe from indicator holder

[30] Insert fuse indicator removed in Step 24 into indicator holder



WARNING 2
Voltage may be present on opposite end of probe; equipment damage possible if grounded

CHECK -48V ORED DIODES, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



CHECK -48V ORED DIODES, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

SUMMARY

If diode was shorted, check resistor circuit and replace any defective resistor. Replace diode and check for values. Check all diodes in unit before replacing cover plate

[1] Remove cover plate by removing screws from side and front of unit

[2] Is suspect diode indicated as shorted or open

Open

Shorted

[3] See FIG. 1. Check diode input resistor circuit for defects

AND

[4] Replace any defective resistor found in resistor check

[5] See NOTE 1. Replace diode (**CR1** or **CR2**) checked as open or shorted

Using ohmmeter, set at **RX1**:

[6] Connect negative lead to cathode side of diode

AND

Page 2

[7] Connect positive lead to anode side of diode

Meter indicates less than 10 ohms

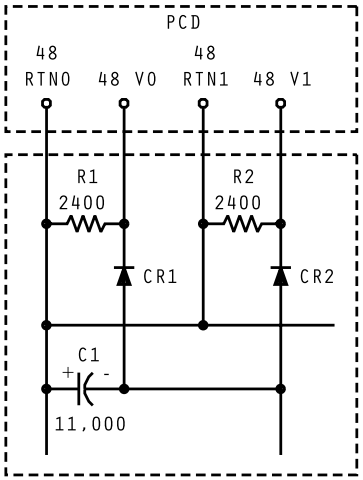
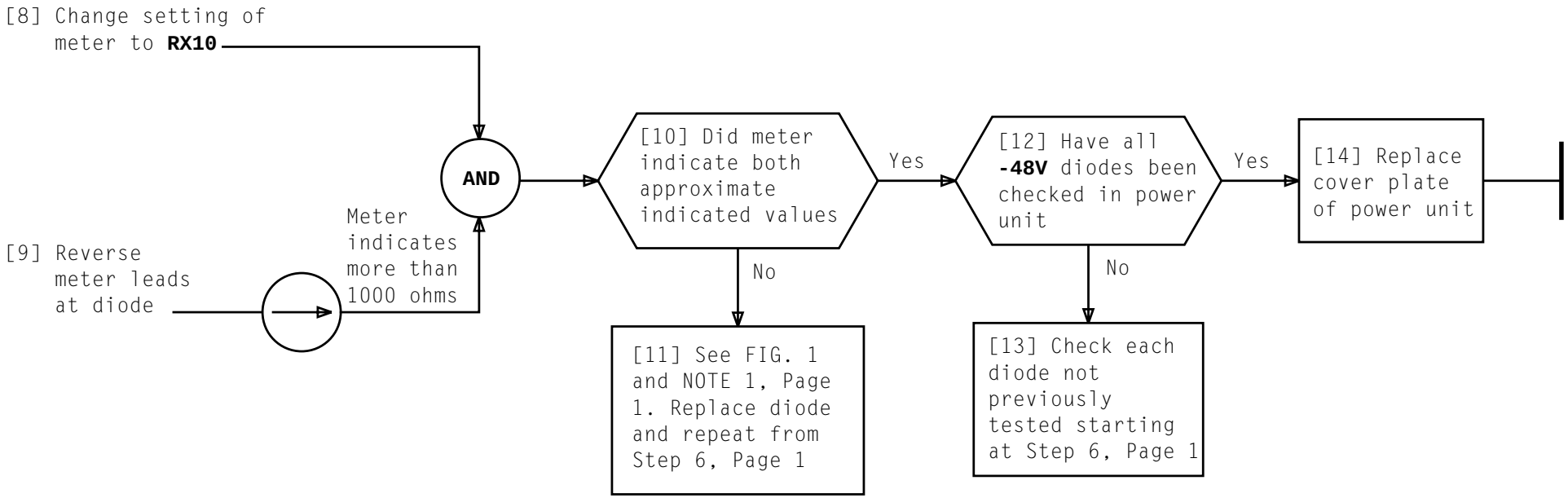


FIG. 1 — Fuse to Diode Layout

NOTE 1

Wiring is to be removed and replaced in accordance with wiring standards

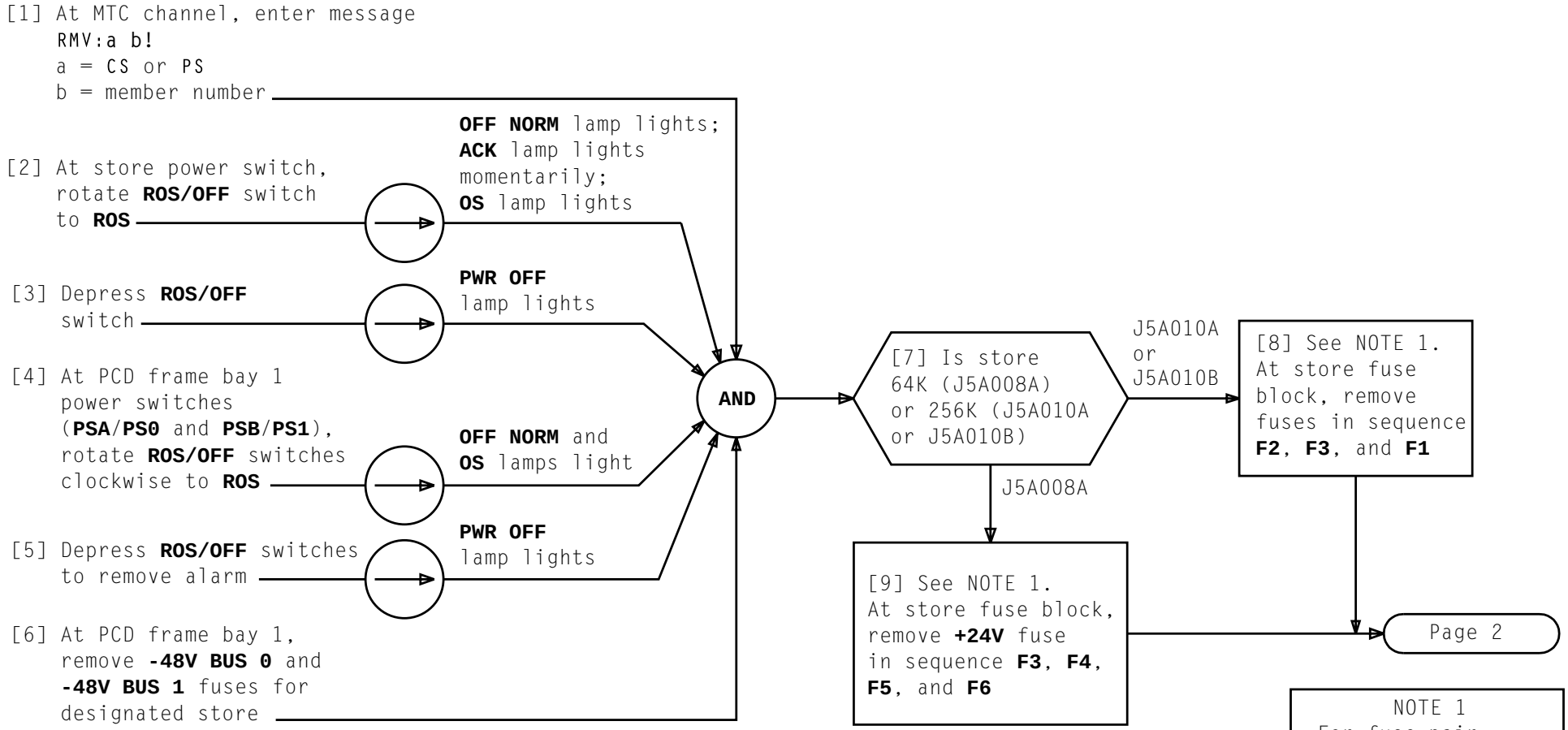
REPLACE AND CHECK ORED DIODES, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B



REPLACE AND CHECK ORED DIODES, 256K SEMICONDUCTOR STORE J5A010A OR J5A010B

SUMMARY

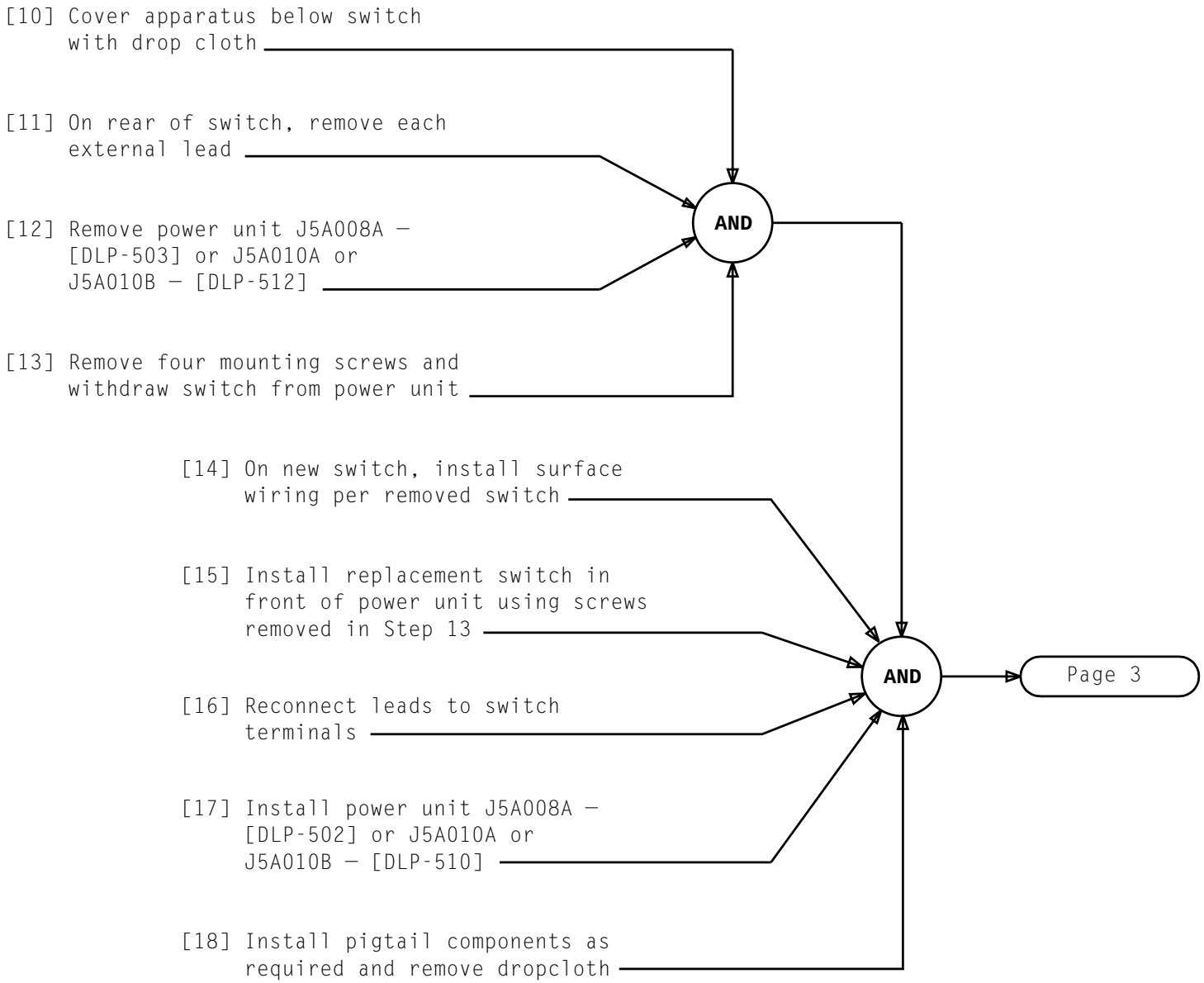
Remove store from service at MTC channel; remove power at store and **PCD** frame as required. Remove fuses associated with switch, then remove switch. Install surface wiring; replace switch, external wiring and pigtail components. Replace fuses, enable PCD frame, alarms as required; restore power to store and return to service



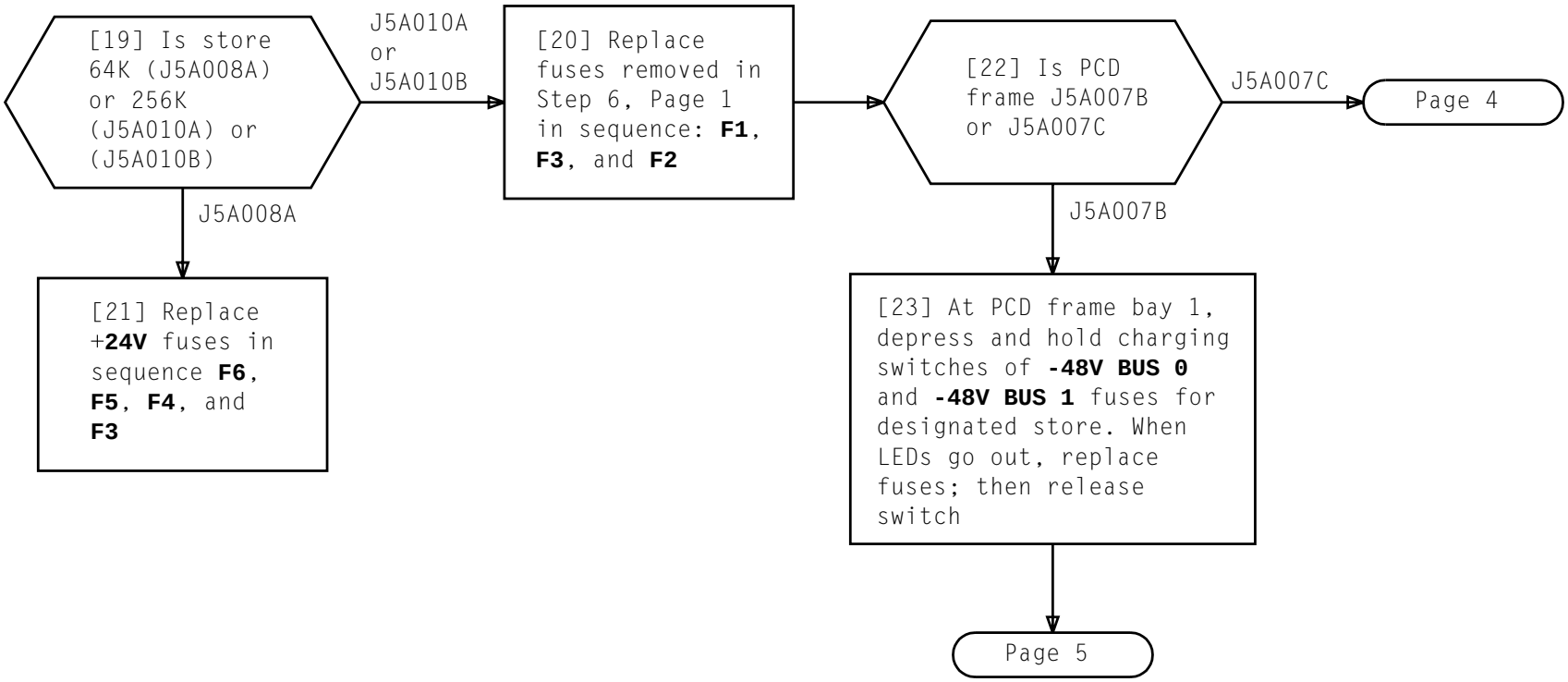
NOTE 1

For fuse pair removal, indicator fuse is removed first and replaced last

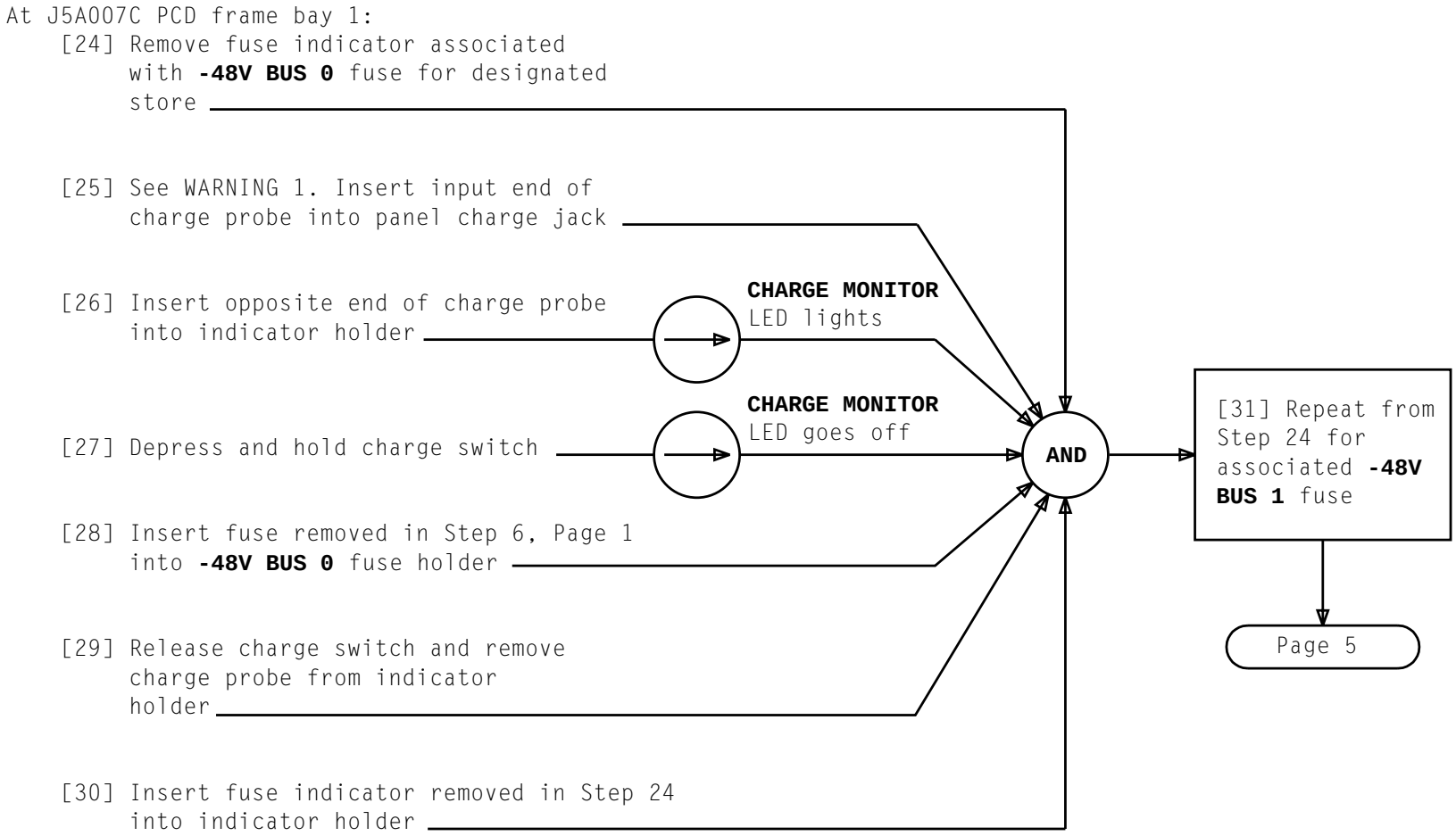
REPLACE POWER SWITCH, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



REPLACE POWER SWITCH, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

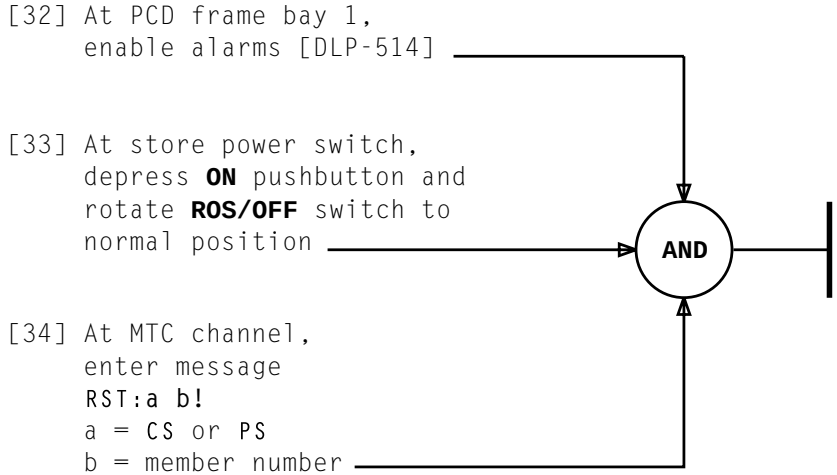


REPLACE POWER SWITCH, SEMICONDUCTOR STORES J5A008A OR J5A010A OR J5A010B



WARNING 1
Voltage may be present on opposite end of probe; equipment damage possible if grounded

REPLACE POWER SWITCH, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B



REPLACE POWER SWITCH, SEMICONDUCTOR STORE J5A008A OR J5A010A OR J5A010B

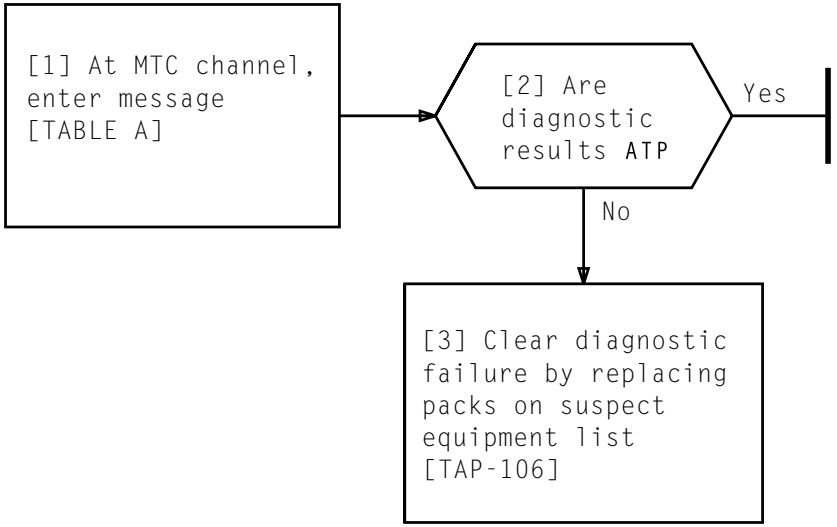


TABLE A
RST:a b:TLP!
a = CS or PS b = Member number of CS/PS

DIAGNOSE CALL STORE/PROGRAM STORE IN NORMAL MODE

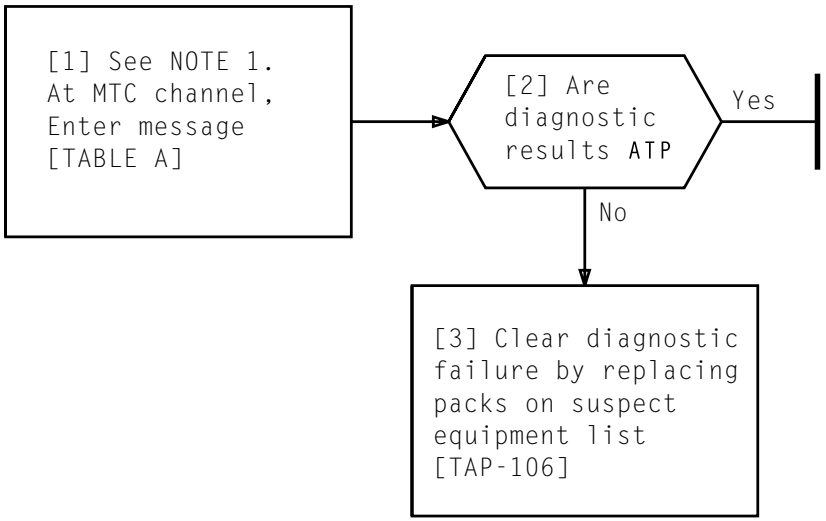


TABLE A
DGN:a b;SLOW:TLP!
a = CS or PS b = Member number

DIAGNOSE CALL STORE/PROGRAM STORE IN SLOW MODE

NOTE 1
Phase 23 (Slave tests) is not run when performing diagnostics in slow mode

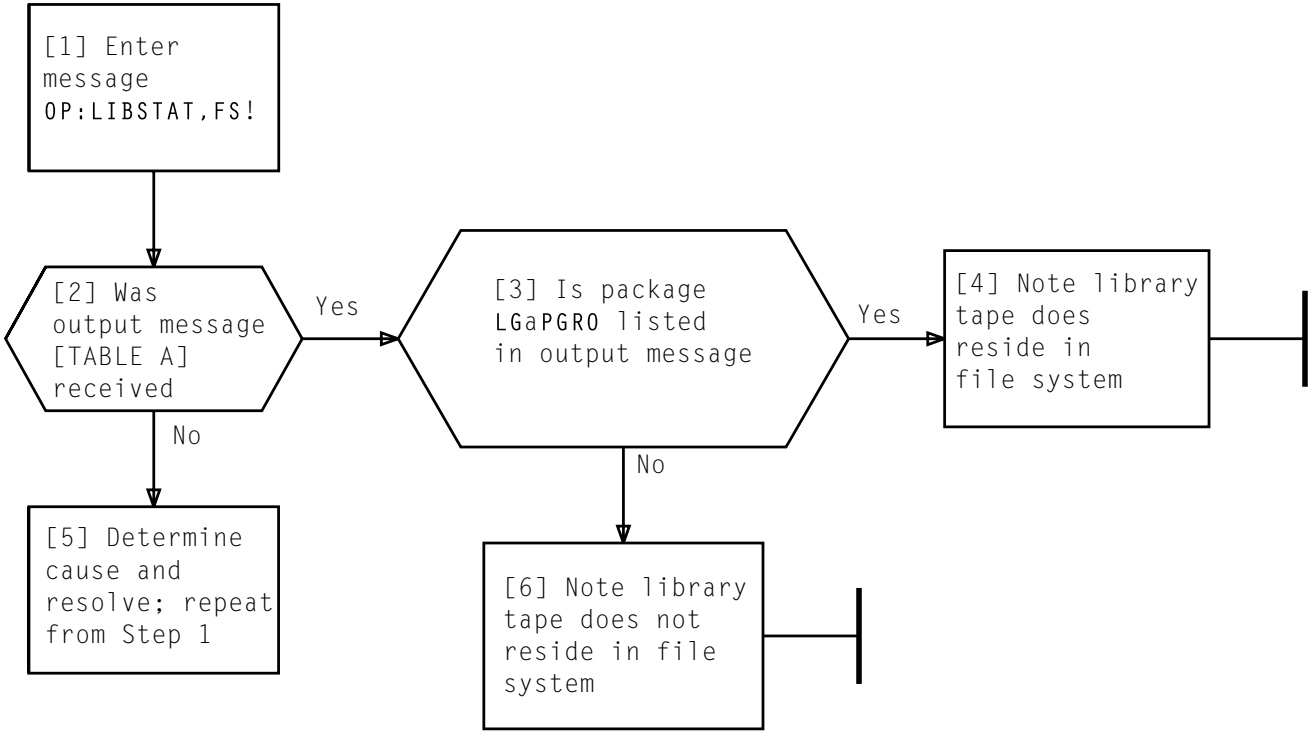


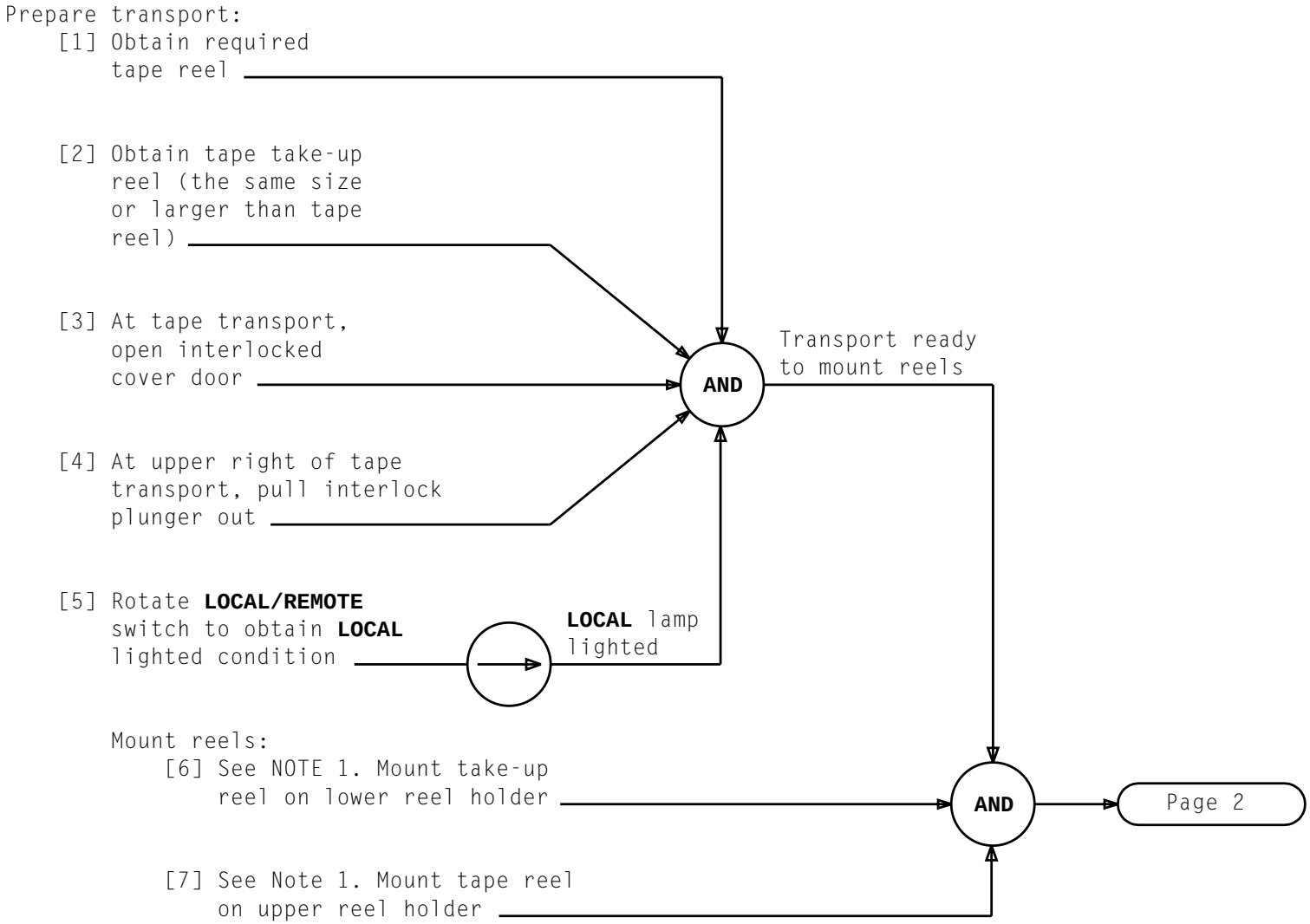
TABLE A

```
OP:LIBSTAT FS PF
OP:LIBSTAT COMPLETED
FS LIBRARY DIRECTORY

PKG NAME      ADDRESS      LENGTH
   .             .            .
   .             .            .
. . . . . . . . . .
```

DETERMINE IF LIBRARY TAPE CONTAINING PROGRAM TO BE USED RESIDES IN FILE SYSTEM

SUMMARY	
Mount tape and tape take-up reels on tape transport. Thread tape through tape transport and start on take-up reel.	Apply tension to tape and verify tape is at BOT marker. Verify that **25 IPS** and **REMOTE** lamps are lighted.



NOTE 1
With the hub (knob) of upper reel in counterclockwise position, the reel should be mounted on holder and the hub of the reel should be rotated clockwise to detent and lock reel. It should be made certain that the detent is securely locked.

MOUNT TAPE ON TAPE TRANSPORT

Thread tape:

[8] See WARNING 1. Depress/hold **BRAKE RELEASE** pushbutton; manually unwind about 5 feet of tape; then release **BRAKE RELEASE** pushbutton

[9] See WARNING 2. Thread tape through tape path indicated on tape transport

[10] See NOTE 2. Start tape end on take-up reel making sure tape is not twisted

[11] See WARNING 3. Depress/hold **BRAKE RELEASE** pushbutton; manually wind take-up reel clockwise — two or three turns; then release **BRAKE RELEASE** pushbutton

AND → Tape threaded

Apply tension:

[12] Depress **ARMS NORMAL** pushbutton → Arms apply tension to tape

[13] Depress **FORWARD** pushbutton → See NOTE 3. Tape winds forward then stops when BOT marker is reached

AND → Arms extended and tape at BOT → Page 3

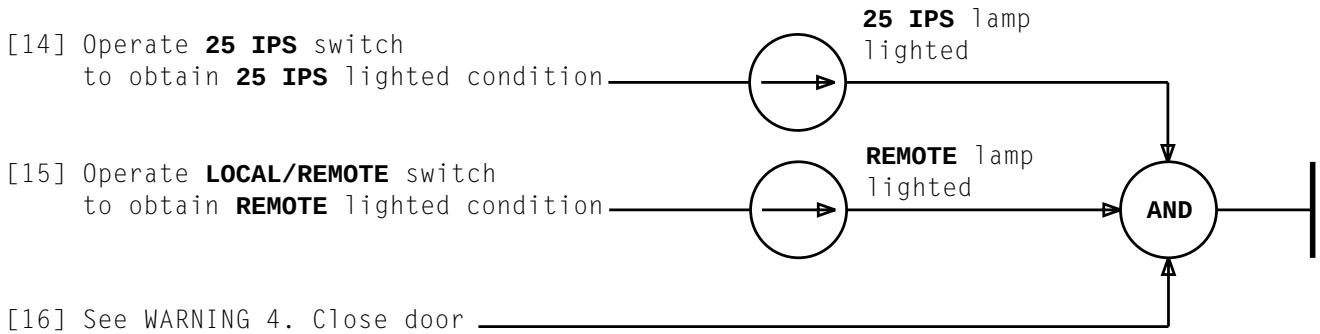
NOTES

2. To start tape on take-up reel, it may help to moisten the tape end (moistened fingers) and stick it to the reel axle
3. Tape may not stop at BOT marker if fast forward is depressed

WARNINGS

1. *Contamination of tape by contact with floor damages tape heads*
2. *Tape head surfaces should not be touched; body oils contaminate tape*
3. *The tape may be damaged if not properly aligned along rollers and guides or mounted too loose*

MOUNT TAPE ON TAPE TRANSPORT



WARNING 4
Closing tape transport door in a harsh manner may upset alignment

MOUNT TAPE ON TAPE TRANSPORT

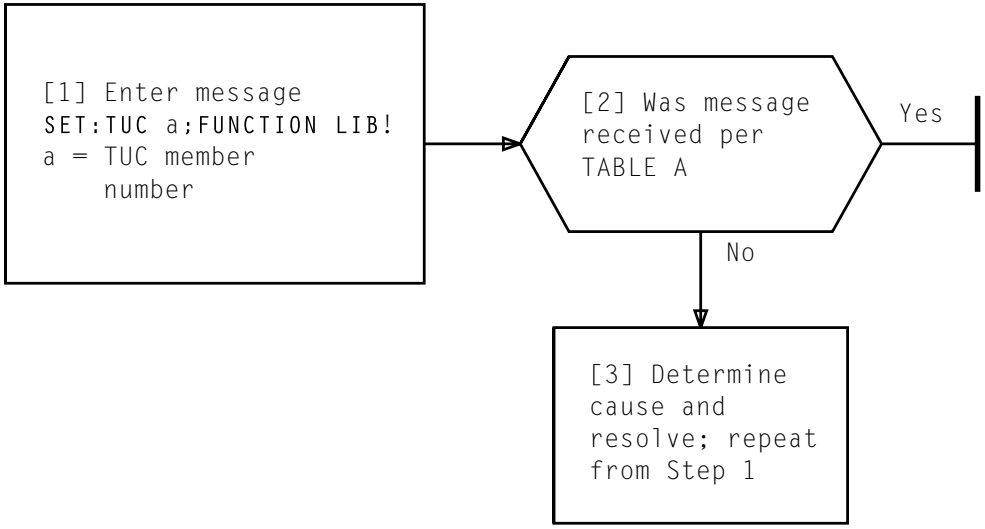
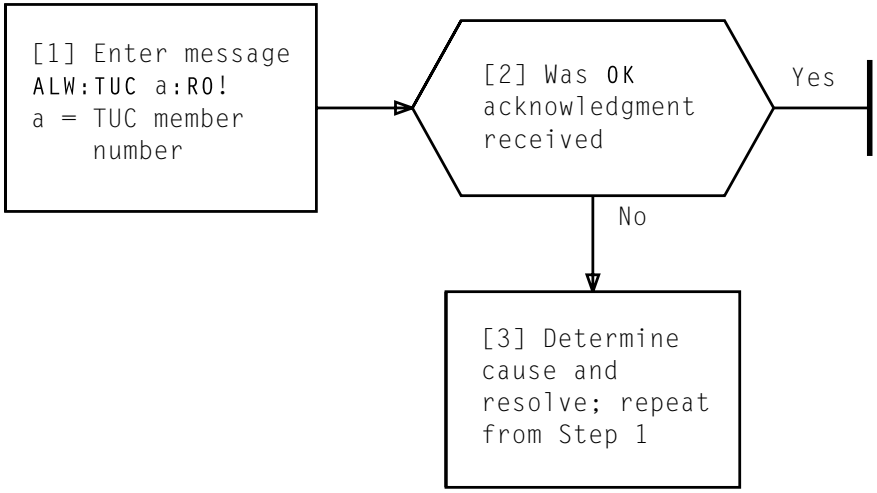


TABLE A
SET:TUC a TAPE MOUNTED ON TUC TAPE TYPE: LIB . . . . OK TO PROCESS TAPE?
a = TUC member number

SET TUC TO LIBRARY FUNCTION



ALLOW TUC READ ONLY ACCESS

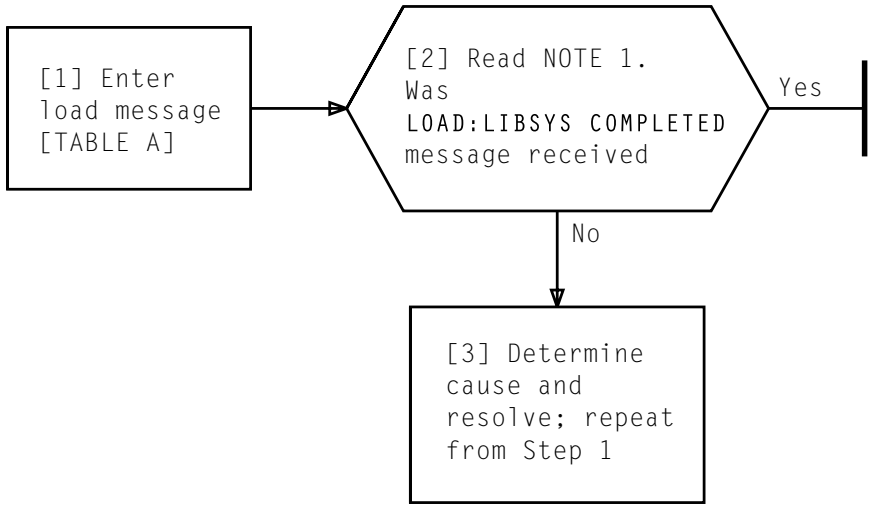


TABLE A
LOAD:LIBSYS,FS;TAPE:PKG LGaPGRO!
a = Office generic (for example, 15 for 4E15)

LOAD LIBRARY TAPE CONTAINING PROGRAM TO BE USED IN FILE SYSTEM

NOTE 1
System does not respond COMPLETED until tape loaded

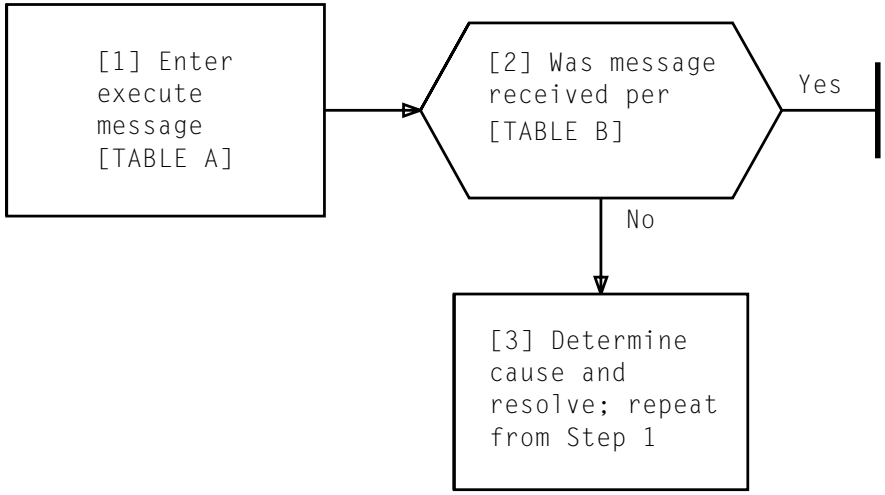


TABLE A
EX:LIBSYS:PKG LGaPGRO,PGM XAPP,TASK 0,CLIENT 0!
a = Office generic (for example, 15 for 4E15)

TABLE B
EX:LIBSYS:PKG LGaPGRO,PGM XAPP,TASK 0 ,CLIENT 0 STARTED
a = Office generic

EXECUTE LIBRARY PROGRAM

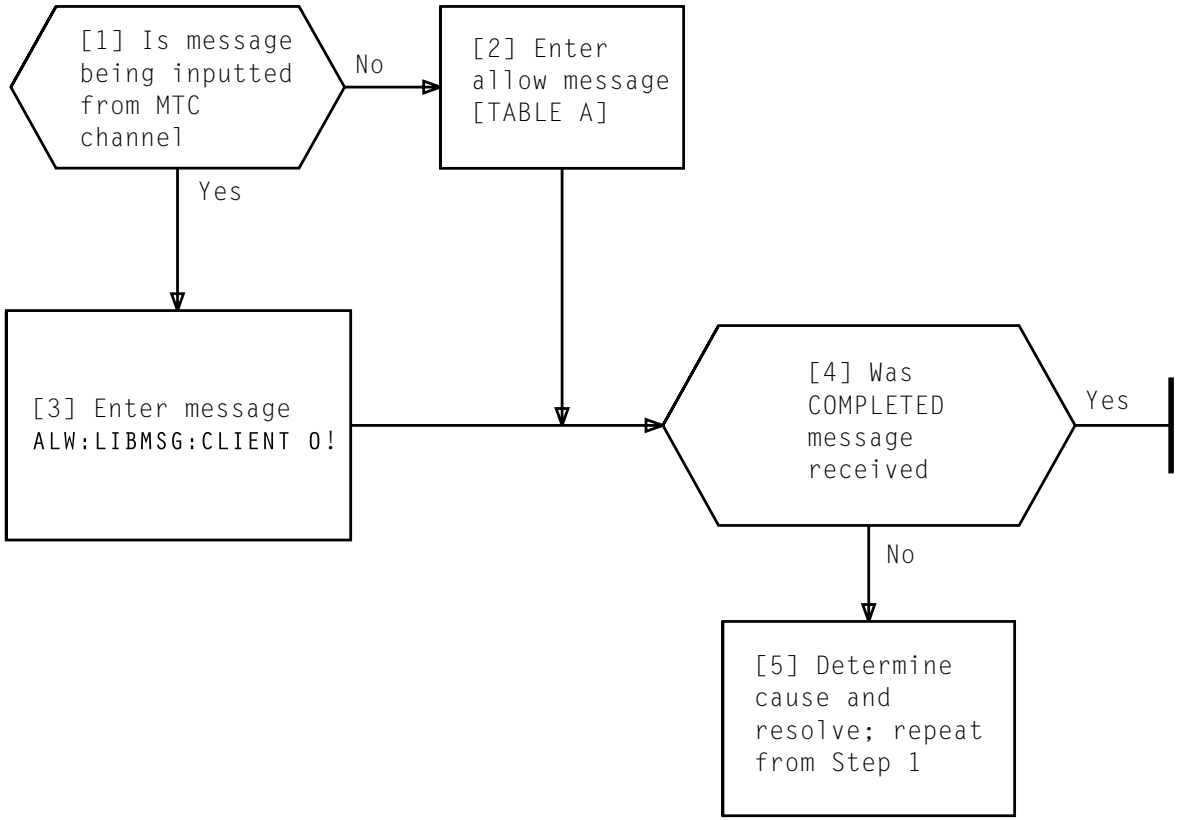


TABLE A
ALW:LIBMSG:CLIENT 0,CHAN (MTC,a)!
a = Channel name on which the message is to be inputted

ALLOW LIBRARY MESSAGE CHANNEL

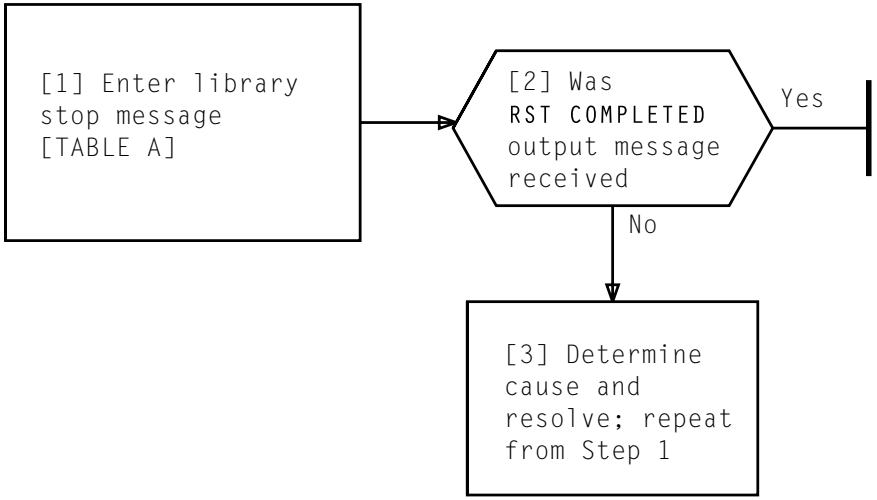


TABLE A
STOP:LIBSYS:PKG LGaPGRO,PGM XAPP,TASK 0,CLIENT 0!
a = Office generic (for example, 15 for 4E15)

TERMINATE EXECUTION OF LIBRARY PROGRAM

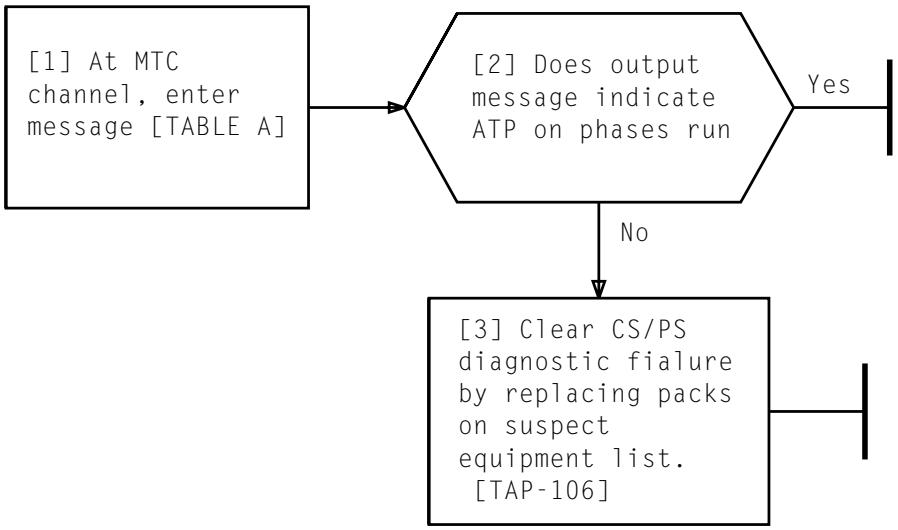


TABLE A
DGN:a b:PH (24-29,91):TLP!
a = CS or PS b = Member number

DIAGNOSE CALL STORE/PROGRAM STORE DEMAND DIAGNOSTICS IN NORMAL MODE

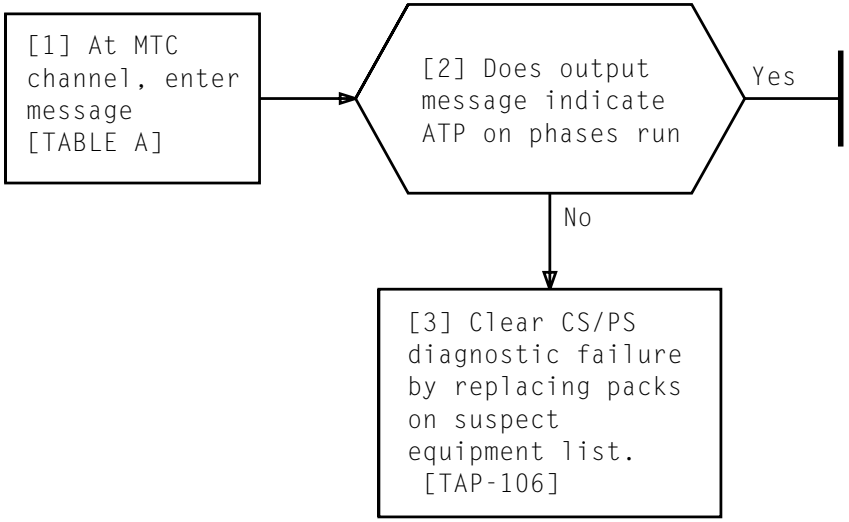


TABLE A
DGN:CS a;SLOW:PH (24-29,91):TLP!
a = CS or PS b = Member number

DIAGNOSE CALL STORE/PROGRAM STORE DEMAND DIAGNOSTICS IN SLOW MODE

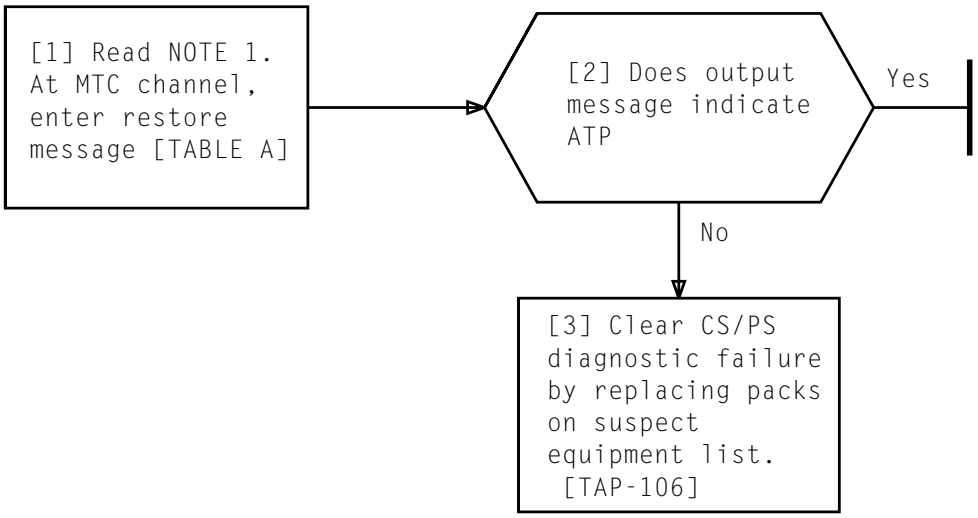


TABLE A
RST:a b!
a = CS or PS b = Member number

NOTE 1
Restore message will cause CS/PS diagnostic to be run. CS/PS will be restored, if ATP

RESTORE CALL STORE/PROGRAM STORE TO SERVICE

ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE
• IXL-001		TAP-125		DLP-532							
NTP-002		TAP-126		DLP-533							
NTP-003		TAP-127		DLP-534							
• NTP-004		DLP-500		DLP-535							
• NTP-005		• DLP-501		DLP-536							
• NTP-006		DLP-502		DLP-537							
• NTP-007		DLP-503		DLP-538							
• NTP-008		DLP-504		DLP-539							
NTP-009		DLP-505		DLP-540							
NTP-010		DLP-506		DLP-541							
TAD-100		DLP-507		DLP-542							
TAD-101		DLP-508		• CKL-891							
TAD-102		• DLP-509		• TNG-893							
TAP-103		• DLP-510		DPL-895							
ISD-104		DLP-511									
TAP-105		DLP-512									
• TAP-106		DLP-513									
TAP-107		DLP-514									
TAP-108		• DLP-515									
TAP-109		• DLP-516									
TAP-110		• DLP-517									
TAP-111		DLP-518									
TAP-112		DLP-519									
TAP-113		DLP-520									
TAP-114		• DLP-521									
TAP-115		• DLP-522									
ISD-116		• DLP-523									
ISD-117		DLP-524									
ISD-118		DLP-525									
ISD-119		• DLP-526									
TAP-120		• DLP-527									
• TAP-121		• DLP-528									
• ISD-122		• DLP-529									
• TAP-123		DLP-530									
• TAP-124		DLP-531									