Fig. 1—3A Central Control

parallel channel and DMA may be optionally connected.

The actual interface between the 3A CC and the PCH/DMA is through the collector diffusion isolation logic to transistor-transistor logic interface (CTI) unit. The 1A technology integrated circuits in the 3A CC require 3 volts for operation while the parallel channel units use transistor-transistor logic (TTL) integrated circuits which require 5 volts. The CTI unit provides logic level shifting necessary to permit the two types of circuits to function together.

The DMA channel may be installed to permit the high-speed transfer of blocks of data between MAS and a peripheral device without intervention of 3A CC except for initialization of the transfer.

- **Large Addressing Capability:** The 3A CC may theoretically access up to 1,048,576 words of storage by using a 20-bit address.

- **Sixteen General Registers:** General purpose registers in the 3A CC provide flexibility in performing logical operations.

- **Manual Control and Display Panel:** Each 3A CC has a control panel by which maintenance personnel can gain access to the unit for testing or performing manual operations.

- **Double Store Read:** When parity errors occur in a read operation of the on-line store, a double store read is performed if the system is in the update mode. The double store read is the procedure for the on-line processor to initiate a new read operation of the corresponding word at the same address in the off-line store.

- **Complement Correction:** Complement correction allows the continued use of a memory location that has a single stuck bit which causes bad parity when read. All the bits of the word, including parity, are complemented and then written back at the failed memory location with both parity bits set to an incorrect parity state. The data is, therefore, in the correct but complemented form. When the data is read, two parity errors are detected and serve as a flag to indicate a previously corrected memory location. All the bits of the word are then

recomplemented with parity corrected to obtain the correct word.

2. PHYSICAL DESCRIPTION

2.01 The 3A CC is located in the upper midsection of each bay of the processor frame (Fig. 2). All interconnections between the 3A CC and other units are accomplished by one of the following types of cabling techniques (Fig. 3). The first type of cable is a 30-gauge, 25- or 31-conductor, flat ribbon cable. The second type of cable consists of twisted pairs; the third consists of coaxial cable. The first two types of cable require 942- or 943-type connectors at each end. Coaxial cable may be connected with subminiature RF-type connectors or 942- or 943-type connectors.

2.02 The 3A CC is 23-1/2 by 12 by 12 inches in overall size. Basically, it consists of a logic unit and front control panel.

3A CENTRAL CONTROL LOGIC UNIT

2.03 A 12-inch mounting plate provides the necessary structure for mounting eight 80C apparatus housings. These housings hold the 3A CC circuit packs. Three types of 1A circuit packs used in the 3A CC are the FA, FB, and FC types. Fig. 4 shows an example of typical discrete and ceramic circuit packs. Fig. 5 shows the three types of 1A circuit packs and their arrangement in the 3A CC.

2.04 Three basic types of SIC logic gates, which are in the 1A logic family, are the low power TTL NAND gate (Fig. 6), the high-power TTL NAND gate, and the resistor-transistor logic (RTL) buffer inverter gate. The low-power gate is used in all logic circuits. The high-power gate is used in special applications such as cable driver circuits. The buffer inverter gate is used to buffer signals coming in from the backplane. Four to eight gates are packed onto an SIC chip. A maximum of 52 SIC chips may be mounted on a ceramic substrate which is 3-1/4 by 4 inches in size. The ceramic substrate is mounted on a removable FA-type circuit pack (4 by 7-3/4 inches) with an 82-pin connector. In the 3A CC, there are 55 FA-type circuit packs with an average of 43 SIC chips on each.

2.05 The FB- and FC-type circuit packs are similar to each other. Both types contain discrete devices and may contain hybrid integrated circuits (HICs). (An HIC is a small ceramic chip mounted on a board along with other discrete devices.) The major difference between the FB- and FC-type packs is their means of external connections. The FB-type circuit packs use a 42-pin connector. The FC-type circuit packs use an 82-pin connector.

3A CENTRAL CONTROL PANEL

2.06 The control panel consists of a 12 by 23-1/2 inch panel which is silk-screened with the appropriate nomenclature. The panel includes the following apparatus:

(a) Status indicator lamps and switches

(b) Light-emitting diodes (LEDs) which display register contents or status information

(c) Register select switches for loading or displaying internal registers

(d) Switches for selecting particular manual functions.

2.07 The panel is mounted to an aluminum frame and has a printed wiring board which supports the apparatus and circuitry necessary for the control panel to function. The entire assembly is hinged to the side brackets of the 3A CC logic unit to provide access to the circuit packs within the unit. Most of the interconnections between the panel and the rest of the 3A CC are accomplished by means of a connectorized flat tape cable assembly. Some interconnections are by coaxial cable.

2.08 The panel is subdivided into the following areas:

(a) LOAD AND DISPLAY

(b) REGISTER SELECT

(c) REGISTER

(d) COMPARE

(e) MEMORY

(f) MODE

(g) COMMAND

PARALLEL CHANNEL (PCH) 00 (JICI06AB-1)

DIRECT MEMORY ACCESS (DMA) 00 (JICI06AA-1)

OPTIONAL

CTI / POWER UNIT 00 (JICI06AC-1)

3A CC 0 (JICI050A-1)

MAS CONTROLLER (MASCM) MOD 0, MOD 1 (JICO52B-1)

MAIN STORE (MAS) 00

MOD 2, MOD 3 (JICO52B-1)

MOD 4, MOD 5 (JICO52B-1)

MOD 6, MOD 7 (JICO52B-1)

POWER SUPPLY (JICO57A-1)

PCH 10

DMA 10

CTI/PWR 10
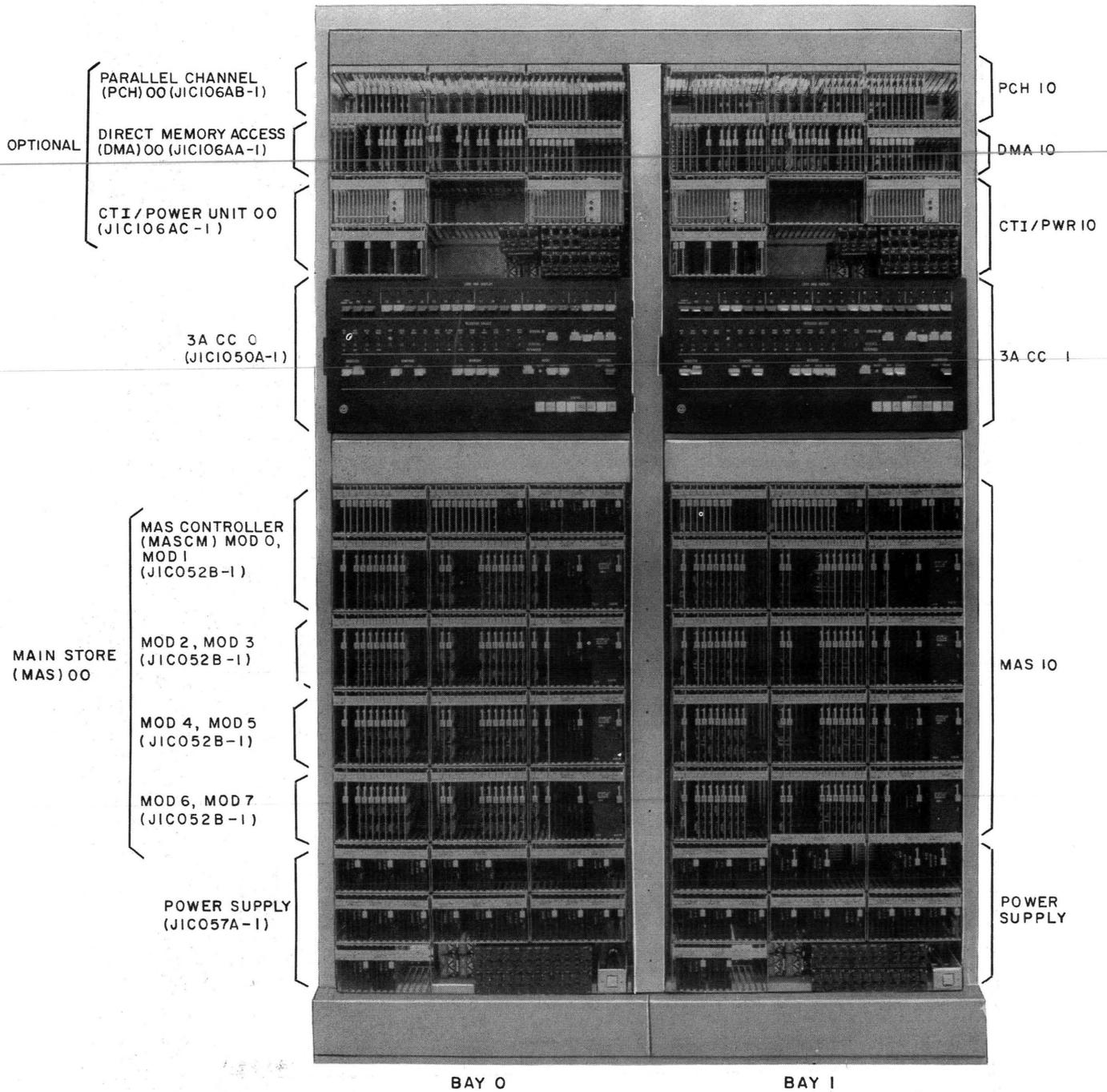
3A CC 1

MAS 10

POWER SUPPLY

BAY 0

BAY 1

Fig. 2—Typical 3A Processor Frame

(h) STATUS.

Table A lists the keys, lamps, and switches of these areas and their purposes.

3A CENTRAL CONTROL GROWTH

2.09 Growth within the 3A CC includes the microstore and the input/output areas. There are also provisions for accommodating a wider
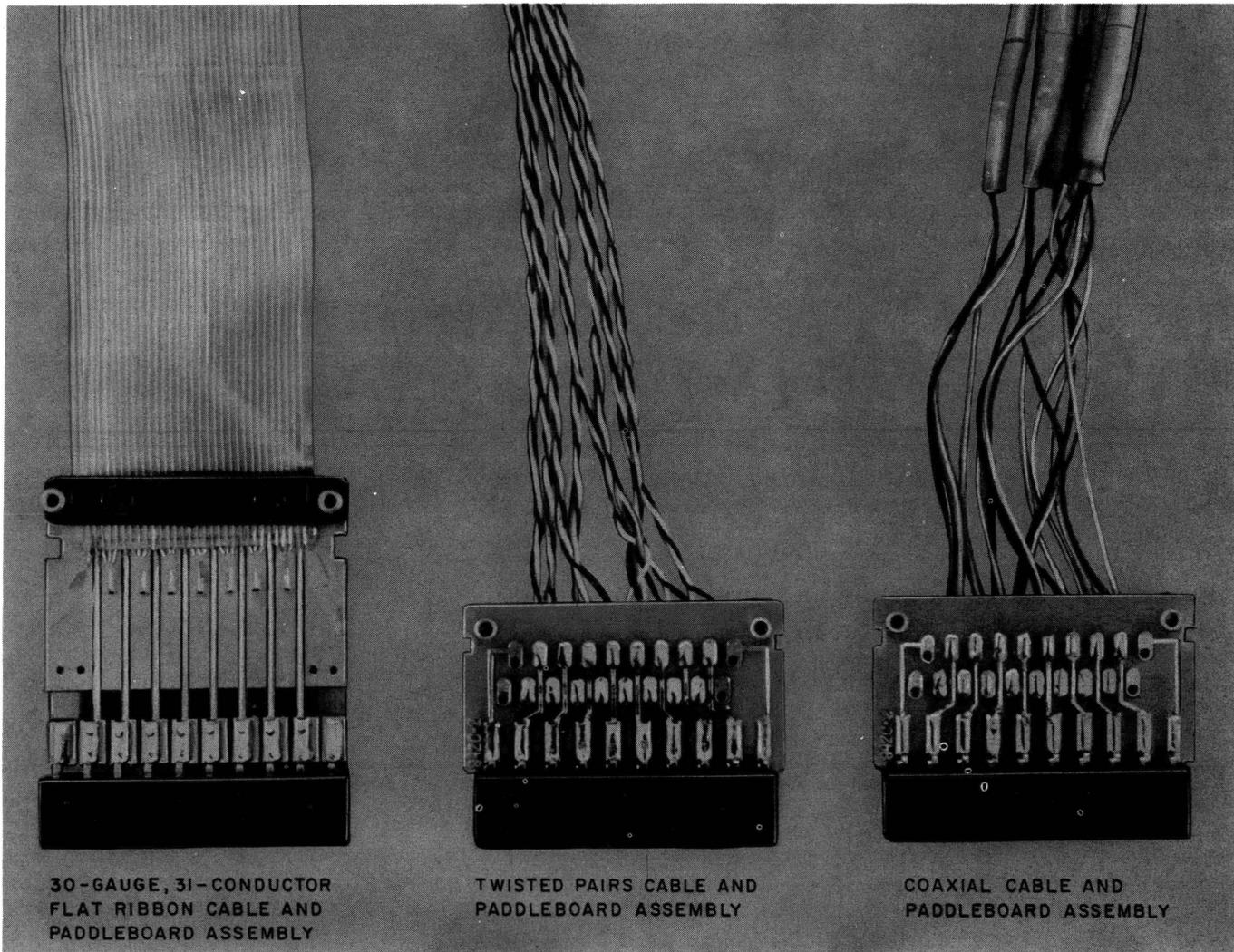
30-GAUGE, 31-CONDUCTOR FLAT RIBBON CABLE AND PADDLEBOARD ASSEMBLY

TWISTED PAIRS CABLE AND PADDLEBOARD ASSEMBLY

COAXIAL CABLE AND PADDLEBOARD ASSEMBLY

Fig. 3—Cabling and Connectors

store. Table B lists the growth provisions for the 3A CC.

3. FUNCTIONAL DESCRIPTION

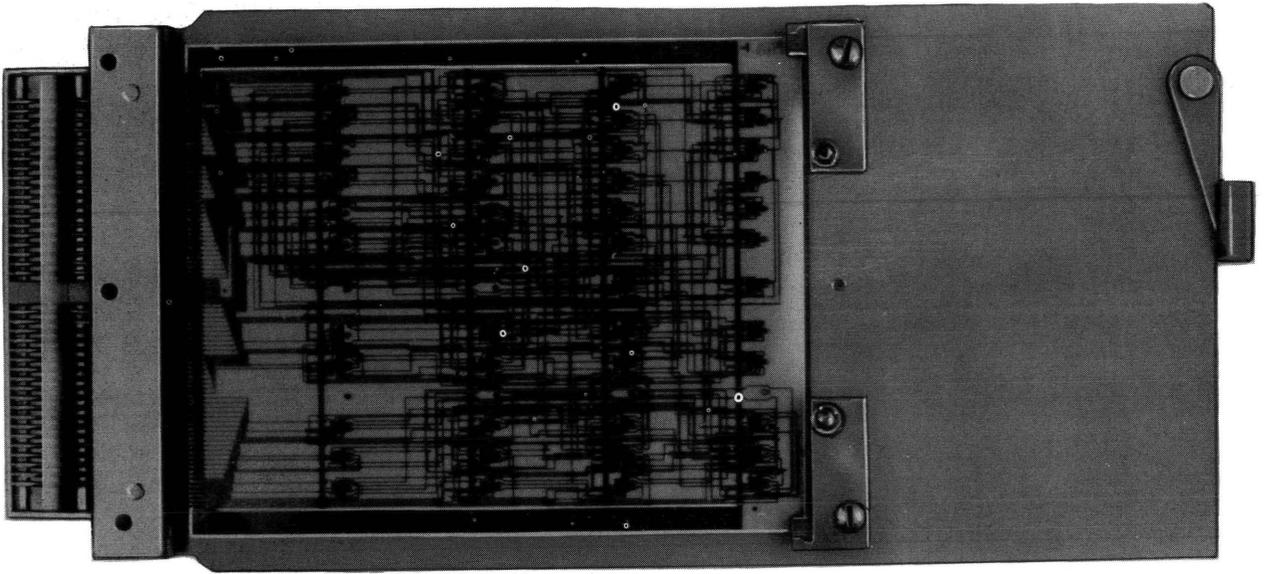### 3A CENTRAL CONTROL FUNCTIONS IN RELATIONSHIP TO OTHER SYSTEM UNITS

3.01 The 3A CC is the controlling unit of the common systems 3A Processor (Fig. 2). The 3A CC (as well as some other units of the system) is duplicated to provide continuous real-time operation with a high degree of system reliability. The 3A CC uses the instructions and data stored in the main store to direct and control normal system functions as well as to aid in detecting and analyzing improper performance of the equipment involved in this task. One 3A CC always has active control over the system while the other 3A CC is in a not active mode. Each 3A CC has its own dedicated main store. The on-line 3A CC keeps both the on-line and standby memory up-to-date so that the standby 3A CC can assume control of the system with an up-to-date storage area.

3.02 Since the 3A CC via hardware and software controls the operation of the system, it must be able to communicate with various units within the system. This communication involves the sending/receiving of information to/from other processor units and peripheral units.
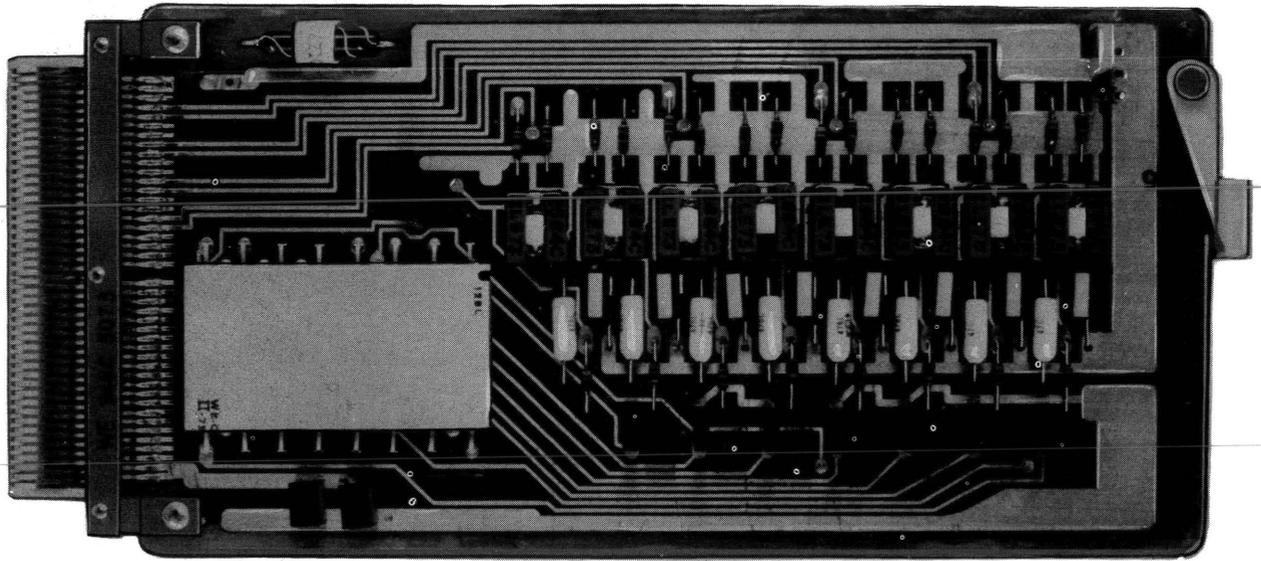
A. DISCRETE CIRCUIT PACK

B. CERAMIC CIRCUIT PACK

Fig. 4—Typical Discrete and Ceramic Circuit Packs

A. Communications Functions of 3A Central Control Within the 3A Processor

3.03 The functions performed by the 3A CC in relation to main store are the reading from or writing into a memory location. These functions are performed between the 3A CC and main store over the main store bus (MASB).

3.04 The cartridge tape system of the 3A Processor contains certain software not stored in main store and a backup for all software stored in main store. Therefore, the 3A CC must access or communicate with the tape system and perform the functions of reading the tape contents or writing information onto the tapes. These functions are performed between the 3A CC and the tape system over a serial I/O subchannel.

3.05 The teletypewriter (TTY) and system status panel (SSP) provide an interface between operating personnel and the system. The 3A CC must communicate with the TTY to perform the functions of outputting characters to the TTY and receiving input characters from the TTY. The 3A CC must also communicate with the SSP to perform functions of sending status information to the SSP and receiving requested panel operations. These functions for both the TTY and SSP are performed over serial I/O subchannels.

3.06 Since the 3A CC is duplicated, both 3A CCs must be able to communicate with each other. This communication is over the maintenance channel. The functions performed via these communications are given for the maintenance channel controller in 3.25.

B. Communications Functions of 3A Central Control in Relationship to Periphery

3.07 For the system to provide proper service, the 3A CC must communicate with and control the periphery. This communication is over serial I/O subchannels and results in such functions as scanner interrogation, switching control, and transfer of data to and from a data bus. Optional parallel I/O channels are also available to different users of the 3A CC.

FUNCTIONAL SECTIONS WITHIN THE 3A CENTRAL CONTROL

3.08 The block diagram in Fig. 7 shows the functional sections within the 3A CC. These sections are:

- 3A CC system clock

- Central control registers

- Microprogram control

- Data manipulation

- Interrupt facility

- Processor bus controller

- Serial I/O channels and controllers

- Interface to parallel I/O channels and DMA (optional)

- Maintenance channel and controller

- Control panel interface

- Gating bus and bus parity checker

- Miscellaneous registers.

A. 3A Central Control System Clock

3.09 The 3A CC system clock supplies the basic timing pulses necessary to control system actions. Each timing pulse is nominally 37.5 ns in duration. Four of these pulses make up one cycle of 150 ns. Timing pulses are used for controlling various system functions such as data timing, gate control, synchronization of events, etc.

3.10 The 3A CC system clock contains counters, timers, and a clock signal generator. The basic timing signal is generated by a standard crystal oscillator and squaring circuit. The crystal oscillator generates a sine wave which is then passed through a squaring circuit to generate a square wave with a period of 37.5 ns. By the use of a flip-flop and combinational logic, four clock phases are generated. Every cycle of 150 ns, a 10-bit counter within the clock is incremented by one. This 10-bit counter indirectly increments the timing counter (TC) and program timer (PT). The

REPRESENTS 12-INCH MOUNTING PLATE

REPRESENTS 80C APPARATUS HOUSING

I/O CHANNEL #00 | OPTIONAL I/O CHANNEL 01 | OPTIONAL I/O CHANNEL 02

Top Row

Pos	Code	Function
1	FC 21	+3V REGULATOR
2	TS 1	I/O CHANNEL 0 TERMINAL STRIP
3	FA 1038	I/O CHANNEL B#1
4	FA 1039	I/O CHANNEL B#2
5	FC 201	10 I/O SUBCHANNELS
6	FC 201	10 I/O SUBCHANNELS
7	FA 1038	
8	FA 1039	
9	FC 201	
10	FC 201	
11	FA 1038	
12	FA 1039	
13	FC 201	
14	FC 201	
16	TS 2	I/O CHANNEL 2 TERM. STRIP (IN NO. 3 ESS, NO PACK USED)
17	TS 3	SYSTEM STATUS, TTYC, TDC, I/O UNIT TERMINAL STRIP
18	TS 4	TEST SET CONN CONTROL COMPLEX
19	TS 5	TEST SET CONN CONTROL COMPLEX
20	TS 6	CONTROL PANEL TERMINAL STRIP
21	TS 7	CONTROL PANEL TERMINAL STRIP
22	FA 1028	ERROR REGISTER AND DISPLAY #2
23	FA 1027	ERROR REGISTER AND DISPLAY #1
24		
25		
26	TS 8	TEST SET CONN MICROSTORE
27	TS 9	TEST SET CONN MICROSTORE
28	FB 152	+12V REFERENCE AND CONTROL PANEL POWER TERMINAL STRIP
29	FC 21	+3V REGULATOR

Middle Row

Pos	Code	Function
1	FC 21	+3V REGULATOR
2	FC 21	+3V REGULATOR (IN NO. 3 ESS, NO PACK USED)
3		
4	FA 1031	4-OUT-OF-8 CHECKER (TO)
5	FB 6	PROTECTION CKT
6	FA 1034	CONSOLE AND 3A CC INTERFACE
7	FB 6	PROTECTION CKT
8	FB 6	PROTECTION CKT
9	FA 1010	BIT SLICE B#1 (6)
10	FA 1010	
11	FA 1010	
12	FA 1010	
13	FA 1010	
14	FA 1010	
16	FA 1010	BIT SLICE B#1 (3)
17	FA 1010	
18	FA 1010	
19	FA 1020	MICROCONTROL B#5
20	FA 1026	BUS PARITY CHECKER
21	FA 1013	DML 1 (4)
22	FA 1012	
23	FA 1015	
24	FA 1012	
25	FA 1012	DML 0 (4)
26	FA 1015	
27	FA 1012	
28	FA 1014	
29	FB 486	CRYSTAL OSCILLATOR
31	FA 1025	CLOCK (3A CC)
32	FA 1019	MICROCONTROL B#4
33	FA 1011	4-OUT-OF-8 DECODER (FROM)
34	FA 1045	4-OUT-OF-8 DECODER (TO)
35	FA 1021	MICROCONTROL B#6
36	ED4C 063	MICROSTORE (BITS 16-31)
37	ED4C 065	
38		
39	ED4C 069	
40		
41		
42		
43		
44	FC 21	+3V REGULATOR

Bottom Row

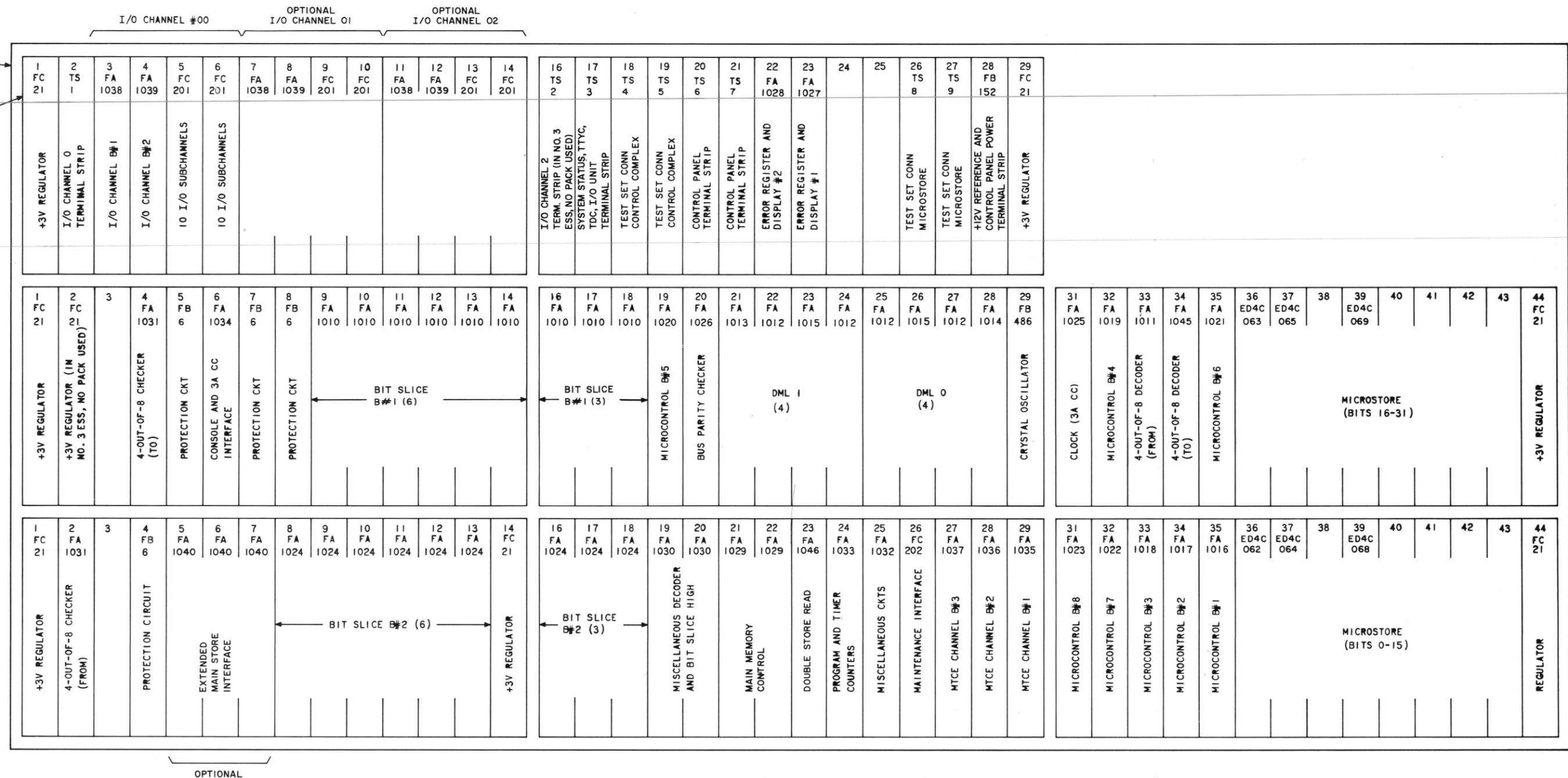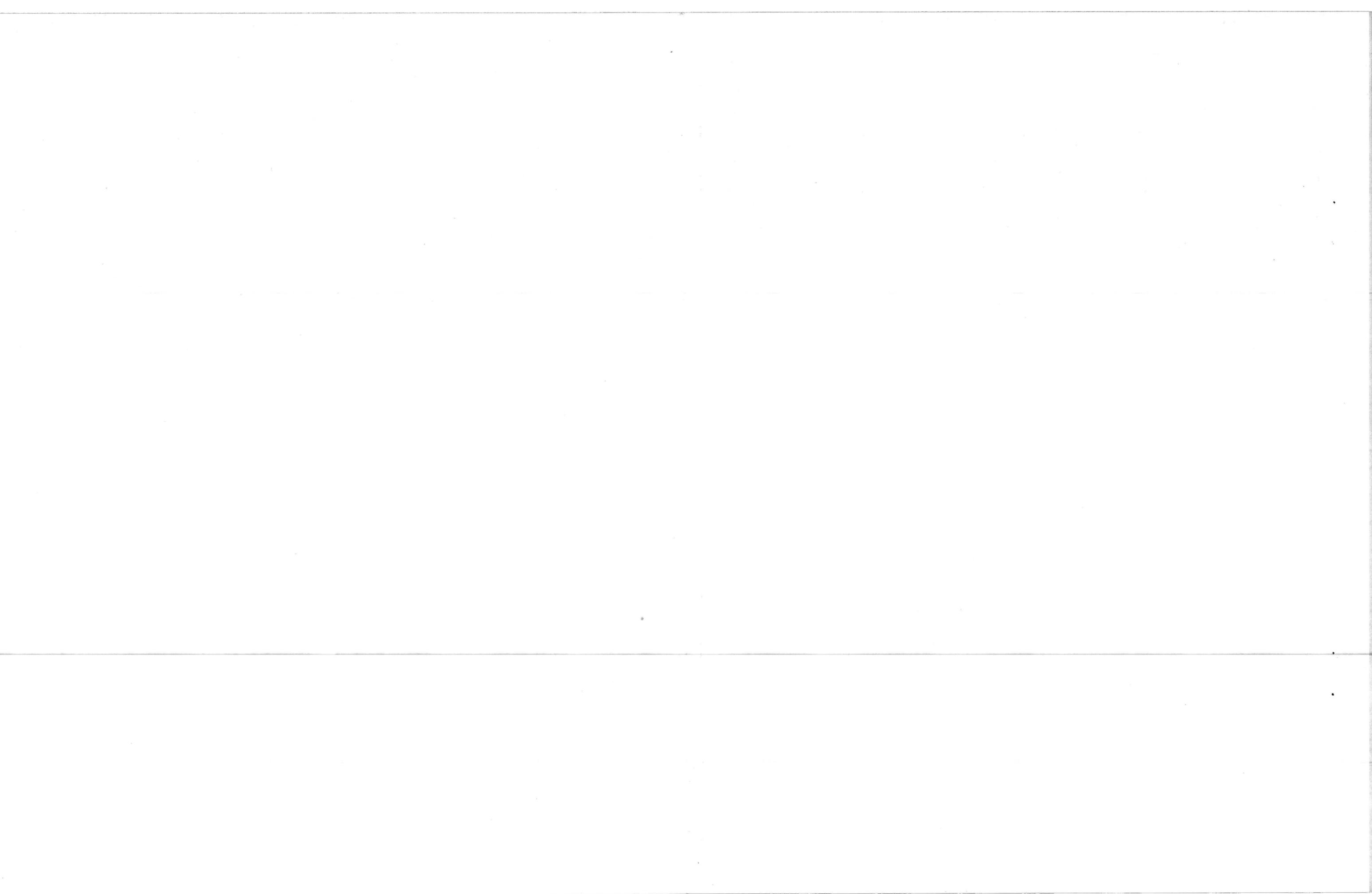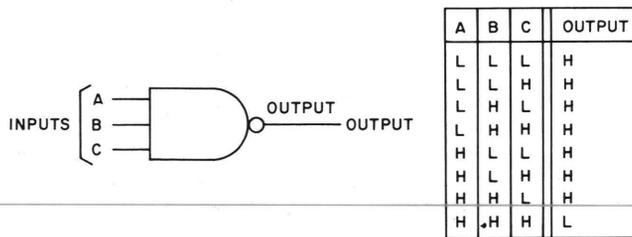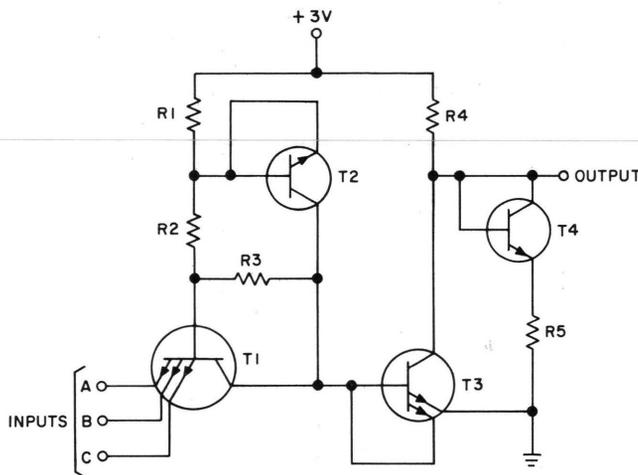| Pos	Code	Function
1	FC 21	+3V REGULATOR
2	FA 1031	4-OUT-OF-8 CHECKER (FROM)
3		
4	FB 6	PROTECTION CIRCUIT
5	FA 1040	EXTENDED MAIN STORE INTERFACE
6	FA 1040	
7	FA 1040	
8	FA 1024	BIT SLICE B#2 (6)
9	FA 1024	
10	FA 1024	
11	FA 1024	
12	FA 1024	
13	FA 1024	
14	FC 21	+3V REGULATOR
16	FA 1024	BIT SLICE B#2 (3)
17	FA 1024	
18	FA 1024	
19	FA 1030	MISCELLANEOUS DECODER AND BIT SLICE HIGH
20	FA 1030	MAIN MEMORY CONTROL
21	FA 1029	
22	FA 1029	
23	FA 1046	DOUBLE STORE READ
24	FA 1033	PROGRAM AND TIMER COUNTERS
25	FA 1032	MISCELLANEOUS CKTS
26	FC 202	MAINTENANCE INTERFACE
27	FA 1037	MTCE CHANNEL B#3
28	FA 1036	MTCE CHANNEL B#2
29	FA 1035	MTCE CHANNEL B#1
31	FA 1023	MICROCONTROL B#8
32	FA 1022	MICROCONTROL B#7
33	FA 1018	MICROCONTROL B#3
34	FA 1017	MICROCONTROL B#2
35	FA 1016	MICROCONTROL B#1
36	ED4C 062	MICROSTORE (BITS 0-15)
37	ED4C 064	
38		
39	ED4C 068	
40		
41		
42		
43		
44	FC 21	REGULATOR

OPTIONAL

Fig. 5—3A Central Control Circuit Pack Locations

A	B	C	OUTPUT
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

INPUTS: A, B, C — OUTPUT — OUTPUT

A. NAND GATE – SYMBOLIC FORM AND TRUTH TABLE

+3V

R1, R2, R3, R4, R5

T1, T2, T3, T4

INPUTS: A, B, C

OUTPUT

B. TTL NAND GATE

Fig. 6—NAND Circuit

TC is used to generate timed interrupts for software use and to increment the PT. The PT is an overall system sanity check for both hardware and software faults.

B. Central Control Registers

3.11 The central control registers provide quick access storage media for data being stored in a current logical operation. The two basic types of registers in the 3A CC are as follows:

- General registers
- Special registers.

The general register organization provides for flexibility in performing logical operations. The general registers are designated R0 through R15. Each general register stores 18 bits: 16 bits of data and 2 parity bits (parity on bits 0 through 7 and parity on bits 8 through 15).

3.12 Since an address for the 3A CC consists of 20 bits, a pair of general registers are utilized to address memory. Register pair R12 (bits 0 through 3) and R13 (bits 0 through 15) or register pair R14 (bits 0 through 3) and R15 (bits 0 through 15) are typical of register pairing for this application.

3.13 General registers R9, R10, and R11 serve particular functions concerning the I/O:

(a) R9 as a buffer for identification of the controller and for the control information to be sent to that I/O controller

(b) R10 for the data to be sent to the I/O controllers

(c) R11 for the results or data received from the external units via the I/O channels and controllers.

When these registers are not being used for their I/O functions, they may be used as general registers.

3.14 The special registers are dedicated to specific functions and, depending on those functions, may vary in length, eg, 20-bit plus 2-parity bit store address register (SAR) and 18-bit store data register (SDR). Special registers are not shown as a separate functional section but form a part of the other functional sections in which they are used. Only 16 of the special registers may be displayed, loaded, or accessed by operation of the control panel. These are shown in the REGISTER SELECT area on the front of the 3A CC panel. Other special registers are used only by the internal 3A CC operations and are not accessible by the user.

C. Microprogram Control

3.15 The microprogram control is the center of the 3A CC operation. It directs and controls the operation of all the other functional sections within the 3A CC. The microprogram control consists of a microstore, several special registers, decoders, translators, logic, and check circuits. The microstore is a read only memory (ROM) type permanent memory which contains both the discrete steps (microinstructions) necessary to carry out main store program instructions and certain special

TABLE A

3A CENTRAL CONTROL PANEL KEYS, LAMPS, AND SWITCHES

AREA	DESIGNATION	COLOR	INDICATION OR FUNCTION
LOAD AND DISPLAY	0-19, PH, PL (LEDs)	Green	Visual indication of the contents of the display buffer. The LEDs are divided into groups of three or four for easy conversion to either octal or hexadecimal. When all LEDs are lighted, it may indicate an erroneous request.
	0-19, PH, PL (Switches)	Blue, White, and Gray	Manual input to the display buffer. Switches are divided into groups of three (by blue and white colors) for easy conversion to octal. Switches are also divided into groups of four for easy conversion to hexadecimal. P_H (parity high) and P_L (parity low) are used only when the ENABLE MANUAL PAR switch is operated.
	ENABLE MANUAL PAR (Switch)	Gray	Allows the manual setting of the parity switches (P_H, P_L). Unless this switch is operated, the 3A CC automatically generates parity for the input switches 0 through 19.
REGISTER SELECT	8, 4, 2, 1 (Switches)	White	Selects one of the 16 general or 16 special (panel-addressable) registers depending upon the setting of the SPECIAL/GENERAL switch. (Only performed when EXECUTE switch is operated.)
	SPECIAL/GENERAL (Switch with LEDs) *Note:* The EXTENDED and abbreviations under the general register numbers are used only for No. 2B ESS applications.	White Switch	This switch in the normal (down) position selects the general register group. This switch in the operated (up) position selects the special register group. Either position is effective only when EXECUTE switch is operated.
		Green LEDs	The GENERAL LED indicates when this group has been selected. The SPECIAL LED indicates when this group has been selected. The special registers are: MCTL STAT — Microcontrol Status Register (read only) TIM — Timing Counter (read only) SYS STAT — System Status Register (read only) ST ADRS — Store Address Register PROG ADRS — Program Address Register MTCE STA — Maintenance State Register M.MEM STAT — Main Memory Status Register

TABLE A (Cont)

3A CENTRAL CONTROL PANEL KEYS, LAMPS, AND SWITCHES

AREA	DESIGNATION	COLOR	INDICATION OR FUNCTION
STATUS (Cont)	MANUAL (Key/Lamp)	Amber	Operation enables the manual state in the not active 3A CC only. The manual state permits panel load and display functions.
	ERROR STOPPED (Lamp)	Red	Indicates the status of the STOP flip-flop. This flip-flop is set by error detection circuits or the other 3A CC and is cleared by initialization hardware or the other 3A CC. When this lamp is lighed, the 3A CC is in the STOP state.
	RESET CIRCUITS (Key)	White	Active only in the MANUAL mode. Initializes the critical flip-flops and puts the 3A CC in the HALT state. The HALTED LED lights.
	TEST MODE (Lamp)	Red	Lights only when the test mode switch (located on the inside of the panel) is active. Test mode switch enables panel functions in an on-line 3A CC and disables the program timer operation. *CAUTION: When this lamp is lighted, use of the panel may cause interruption of service.*
	LAMP & PWR TEST (Key)	White	Utilized to ensure that all lamps within STATUS area will light and to perform a test of the power alarm circuits in the power converters and FB152 packs. The power converters are located within other units of the frame. When the key is operated, the converter LEDs will light. When the key is released, the converter LEDs extinguish.

functions, such as initialization, control panel sequences, interrupt recognition, etc. The special registers are for status, microstore address generation, and microinstruction interpretation purposes. Microcontrol status saves certain status states (I/O status, memory data ready, etc) and utilizes their value to modify addressing of microinstructions. Typically, a main store instruction is used to address, via a microstore address register, a set of microinstructions which will implement the function specified by the MAS instruction. This begins a microsequence, composed of microinstructions. Each microinstruction executes, through the instruction register and decoders, one step of the sequence. The microinstructions also contain a next instruction address field which progresses the sequence until the required function is completed. During the decode portion of a sequence, check circuitry verifies that the correct control signals to other 3A CC circuits were generated.

TABLE B

GROWTH WITHIN THE 3A CENTRAL CONTROL

SECTION	MINIMUM SIZE	GROWABLE BY UNITS OF	TO A MAXIMUM SIZE OF
Microstore	1024 words (2 circuit packs)	1024 words (2 circuit packs)	4096 words (8 circuit packs)
Serial Input/ Output Channels	One I/O serial channel (20 I/O subchannels, 4 circuit packs) (Standard equipment)	One I/O serial channel (20 I/O subchannels, 4 circuit packs)	*Note:* Only the wiring or apparatus for three I/O main channels is available for use within the 3A CC.
Store Width	16 bits	8 bits	32 bits

D. Data Manipulation

3.16 The data manipulation area provides the special registers, matchers, parity generator, and logic necessary to perform such functions as addition, rotation, logical combinations (Boolean functions), and find low zero.

3.17 The data manipulation area contains duplicated data manipulation logic (DML 0 and 1). Information is gated into both DMLs via the gating bus. After both DMLs perform the desired function, the results are compared by the matchers. If no mismatch occurs, parity is generated on all DML results by the parity generator attached to DML 1. The data manipulation output will then interface with the rest of the system.

3.18 Each DML consists of a function register, an A register, a B register, and combinational logic. The function register provides the control information used by the DML to perform the desired function. Registers A and B buffer the data to be manipulated. The combinational logic is used to perform the functions indicated by the function register on the data in A and/or B registers.

E. Interrupt Facility

3.19 The interrupt facility provides the means of breaking into the program flow so that a timed or more urgent task may be performed. The interrupt facility consists of two special registers (interrupt set and interrupt mask) and interrupt logic. This facility enables any desired input to the 3A CC to be recognized and serviced relative to its priority. Interrupts may be caused by such inputs as teletypewriter messages, control panel operations, timing counter signals, and certain error conditions.

F. Processor Bus Controller

3.20 The PBC is the means or interface by which information is transmitted to or received from the main memory. The PBC contains special registers (main memory status register, program address register, store address register, store instruction register, and store data register) which buffer:

(a) Data or status from main memory for use within the 3A CC

(b) Data to the main memory location defined by SAR for storage

(c) Address of present and last program word fetched from memory.

3.21 A normal main store bus interface width of 18 bits (16 data bits plus 2 parity bits) is provided. An extended MASB interface is used for No. 2B ESS applications to provide an interface to a 26-bit memory (24 data bits plus 2 parity bits). The interface within the 3A CC provides for an expansion of up to 18 additional bit positions (16 data bits plus 2 parity bits) for this interface. By adding an 18-bit (instead of an 8-bit) interface expansion, the implementation is made more compatible with microcode operation and provides greater flexibility for future requirements. If the
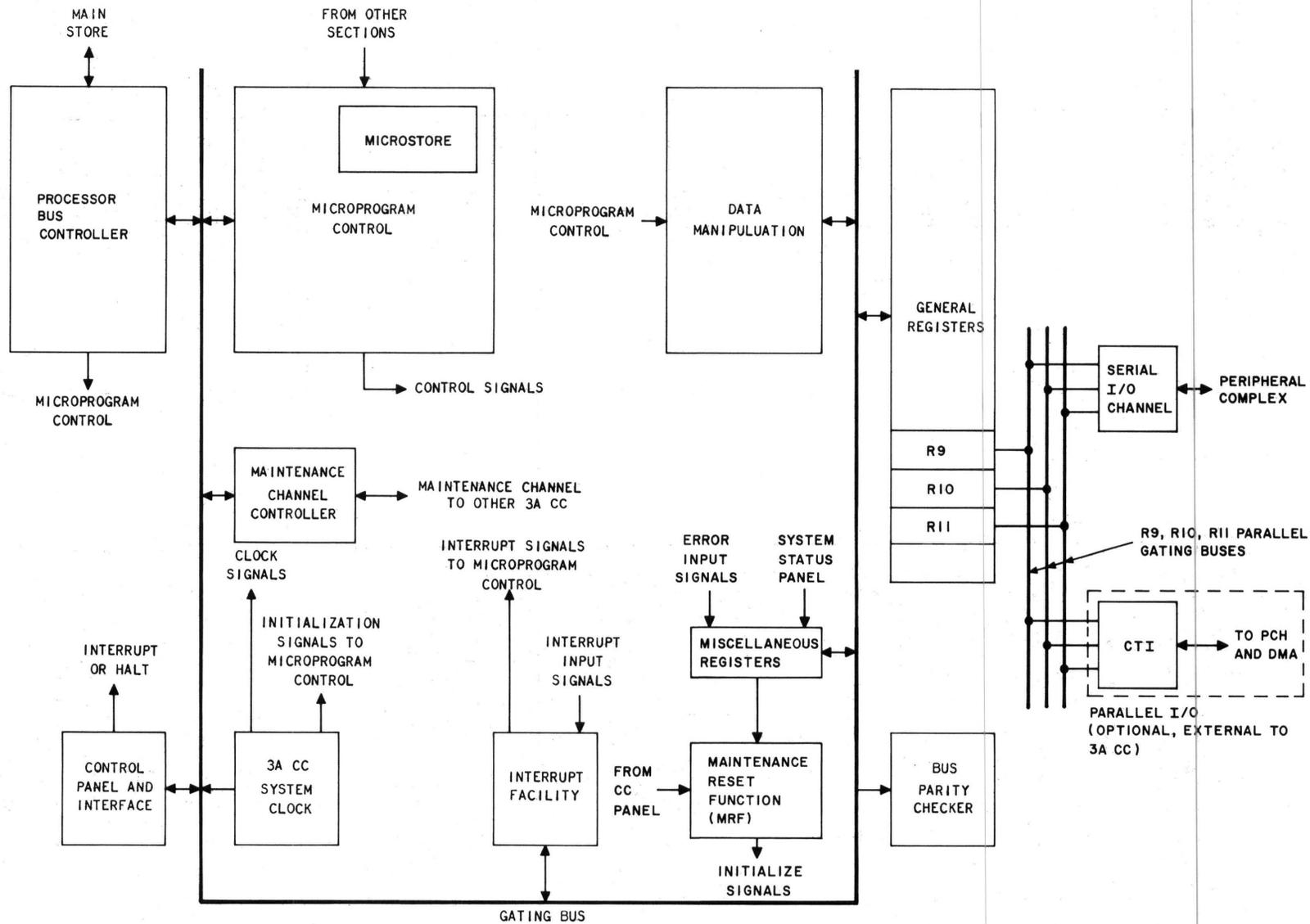
Fig. 7—Block Diagram of the 3A Central Control

extended MASB is implemented, three optionally provided circuit packs in the specified locations (Fig. 5) provide interfacing for a 36-bit memory (32 data bits plus 4 parity bits).

G. Serial Input/Output Channel and Controller

3.22 The I/O channels of the 3A CC form an asynchronous, semiautonomous data transfer system which provides the communication link between the 3A CC and the periphery. The 3A CC has the addressing capability to support a maximum of 20 I/O main channels, up to 3 of which may be optionally supplied within the unit. Each of the I/O main channels is identical to, and independent of, the other main channels, and has a capacity of 20 subchannels. These 20 subchannels, each consisting of a dedicated cable driver and a dedicated cable receiver, are controlled by a main channel controller. The I/O main channel controller consists of an I/O status register, a start code register, sequence and control logic, error check circuitry, and various intraprocessor gating paths.

H. Interface to Parallel I/O Channels and DMA (Optional)

3.23 Three special parallel gating buses accommodate all the data communication between the 3A CC and the I/O main channel registers. Special access is provided into and out of general registers R9, R10, and R11 (3.13). Individual outputs of registers R9 and R10 appear on the backplane. Inputs are provided to the individual bits of register R11 together with a miscellaneous decoder control signal that allows gating of the I/O data bus into R11. Thus, in addition to the serial I/O channels, the 3A CC has the capability of servicing high-speed peripheral devices through a parallel I/O channel. This is accomplished by interfacing optional external DMA or PCH equipment to the gating buses (Fig. 2 and 7).

I. Maintenance Channel and Controller

3.24 The maintenance channel (MCH) is an asynchronous, semiautonomous data transfer system capable of serial ac data transfers at a rate of 6.67 megabits per second. It provides a half-duplex mode of communication between the duplicated 3A CCs. This communication is necessary for one 3A CC to determine the state of the other and for the on-line 3A CC to exercise the other 3A CC as well.

3.25 The MCH controller of the on-line 3A CC is used to perform the following functions in relation to the other 3A CC:

(a) Periodic auditing of 3A CC off-line status

(b) Periodic or diagnostic exercise

(c) Stopping

(d) Starting or initializing

(e) Updating the program timer

(f) Disabling the serial I/O

(g) Controlling the clock.

3.26 The MCH controller consists of special registers (transmit/receive register, command register, and buffer register), sequence and control logic, error check circuits, bipolar drivers/receivers, and a command decoder.

J. Control Panel Interface

3.27 The control panel is one of the means for communications between maintenance personnel and the 3A CC. The control panel interface consists of special registers (three switch registers, display buffer, data input register, data mask register, address input register, address mask register), matchers, and interface logic.

K. Gating Bus and Bus Parity Checker

3.28 The gating bus is the communications path within the 3A CC. Most information is transferred between functional sections of the 3A CC via this gating bus. The bus parity checker tests the parity of the information placed on the gating bus to ensure its accuracy.

L. Miscellaneous Registers

3.29 Within the miscellaneous section, a group of special registers and cable receivers are present. The cable receivers provide a means for receiving information from the SSP. The special registers provide:

(a) A hardware-assisted subroutine facility (hold-get register)

(b) A buffer for error signals (error register)

(c) A buffer for status and control information (system status register)

(d) A buffer for testing purposes (maintenance state register)

(e) A buffer used as a scratch area by the microprogram (C register).

4. POWER

4.01 The 3A CC is not equipped with its own power supply. Power converters in the processor frame power unit must supply the following voltage inputs to the 3A CC:

(a) 3 volts (used in 1A logic)

(b) 5 volts (used in microstore, clock oscillator, panel LEDs)

(c) In addition, +24 volts is provided via the power unit for use in the control panels and as reference and sensing for 3-volt regulation.

5. MAINTENANCE

5.01 Three functions are involved in the maintenance of the system:

(a) Fault detection is the first and most important function in realizing a highly reliable system.

(b) After detection of a fault, rapid recovery of the system must occur to ensure the protection of messages in progress and the continuation of the message switching processing functions.

(c) After recovery, the fault must be diagnosed and isolated to the unit in trouble for replacement purposes.

FAULT DETECTION

5.02 Fault detection is accomplished by hardware and/or software. The 3A CC is designed to be a self-checking unit utilizing error checking techniques such as:

(a) *Bit-Slicing:* The 3A CC uses 2-bit partitioning or 2-bit slicing to aid in the detection of errors, especially in areas such as the general registers. Two-bit slicing means that two bits of each register are on a single circuit pack (Fig. 8). For example, the first circuit pack contains bits 0 and 8 of every general register. Partitioning is used so that a fault will affect at most only two bits of any register and therefore be detected by the two parity bits.
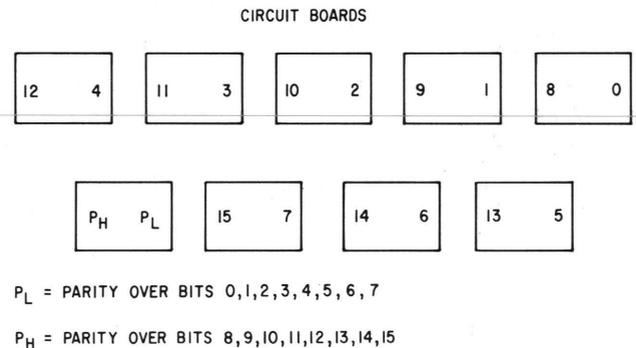
CIRCUIT BOARDS

P_L = PARITY OVER BITS 0,1,2,3,4,5,6,7

P_H = PARITY OVER BITS 8,9,10,11,12,13,14,15

Fig. 8—Bit-Slicing of General Registers

(b) *Parity Check:* Each word used in the 3A CC contains 18 bits (16 data and 2 parity bits). A parity bit is associated with 8 other bits in a 16-bit word to make the total number of 1s, including the parity bit, odd. Parity checks are used throughout the 3A CC. Each time information is transferred from one location to another via the gating bus, a parity check is performed in the gating bus parity checker. Whenever incorrect parity is found, an error is indicated.

(c) *M-Out-of-N Codes:* M-out-of-n codes are used throughout the 3A CC to provide maximum error detection capability. M-out-of-n means that "m" ones should be present in "n" bits. For example, four-out-of-eight means that exactly four ones will always be present. The associated decoder check circuits verify that the number of ones is correct. If an incorrect code is detected, an error is indicated.

(d) *Duplication:* Duplication of units, such as in the data manipulation logic, is another means used in the 3A CC to detect faults. Duplicated units are given the same inputs. Their outputs are then compared to verify their

correctness. Whenever the two outputs differ, an error is indicated.

(e) *Periodic Detection Tests:* Since the 3A CC uses self-checking circuits, its fault detection is adequate only as long as the check circuits work properly. A combination of hardware and software is used to verify that the check circuits provide an indication when a fault occurs. Hardware provides a means of simulating test conditions or circuit faults. By appropriately setting up the test conditions and applying a well-designed test sequence, the detection circuitry is checked on a periodic basis.

(f) *Program Timer:* Although the 3A CC is designed to be self-checking, an overall system sanity check for both hardware and software is provided by the program timer. The use of the hardware timer is closely related to the system program. A reset is generated for the timer only if the program proceeds through the normal program loop correctly within the prescribed period. If the program deviates from the normal course, no reset is given. The timer automatically times out, stops processing, and starts the recovery process.

RECOVERY

5.03 After detection of a fault, the system must quickly and automatically recover itself to a point or condition where it can function to process messages. The error signals that result from detected faults are buffered in the error register of the 3A CC. These signals are sorted and divided into four groups with each causing a different set of system actions.

(a) *Interrupts*—This is the least severe of the recovery actions since the on-line 3A CC maintains complete control. Error signals that cause this action are usually associated with the I/O facility, MCH, or off-line errors.

(b) *MAS read parity error*—Invokes double store read or complement correction.

(c) *Initialization*—This action is a restart of the 3A CC in a particular state. Error signals that cause this action are usually caused by software errors.

(d) *Switch to other 3A CC*—This action changes control from one 3A CC to the other due to a fault in the on-line system.

5.04 Although the system is designed to automatically recover itself under trouble conditions, certain software or hardware faults or combinations of the two may occur in which the system is unable to configure into a working mode, eg, continuously switching 3A CCs. In these cases, manual recovery must be performed via the system status panel which allows maintenance personnel the capability of forcing the system into a fixed configuration.

DIAGNOSTIC AND REPAIR

5.05 A diagnostic is a test sequence that localizes a fault to an area for repair. The diagnostics operate on a "start small" philosophy. This means that a small portion of the off-line 3A CC is first diagnosed by the on-line 3A CC. If this portion of the off-line 3A CC operates properly, it may be used for further diagnosis. For example, before the on-line 3A CC runs any diagnostics on the off-line 3A CC, the maintenance channel must first be checked to verify its proper operation. As the diagnostics continue, that portion of the off-line 3A CC that has been checked increases until correct operation of the total 3A CC is verified. If a failure occurs in the diagnostics, a TTY message is printed which gives a trouble number. This trouble number, when looked up in the trouble locating manual, should indicate the cause of the trouble. Maintenance personnel must then take appropriate repair actions, such as replacement of a circuit pack.

6. REFERENCES

6.01 The following documents are referenced for supporting information:

Section 254-300-100—Common Systems 3A Processor

Section 254-300-120—3A CC Theory of Operation

Section 254-300-130—Common Systems I/O Interfaces

Section 254-300-140—3A Processor Power System

Section 254-300-150—Common Systems Main Store and Supplemental Store

Section 254-300-160—Processor Maintenance Frame

Section 254-300-170—Tape Data Controller

Section 254-300-180—System Status Panel

7. GLOSSARY

7.01 The following terms and definitions are used in this description.

Ceramic Substrate—A type of substrate in which ceramic is the insulating material (see substrate).

Chip—A small piece (approximately 35 mils square) of silicon integrated circuit (SIC) that contains four to eight gates.

Gate—A circuit which has the ability to produce an output dependent upon specified type or the coincident nature of the input(s).

Hybrid Integrated Circuit (HIC)—Consists of an assembly of one or more semiconductor devices and a thin-film integrated circuit on a single substrate, usually of ceramic. This ceramic is small in size, eg, 1.05- by 1.9-inches, and is mounted on a circuit pack along with discrete devices.

Initialization—A program restart to a fixed location to provide an orderly return to a stable state in the data processing routines. A count of the number of restarts incurred during a given time is used to progressively clear areas until the system recovers its sanity.

Instruction—A word which directs a unit to perform a particular function such as the clearing of a register, the gating of information from one place to another, etc.

Integrated Circuit—A circuit in which many elements are fabricated and interconnected by a single process, as opposed to a "nonintegrated" circuit in which the transistors, diodes, resistors, etc, are fabricated separately and then assembled.

Interrupt—A break in the normal flow of a system or routine such that the flow can be resumed from the point at a later time.

Light Emitting Diode—LEDs are chemically grown gallium phosphide crystals that convert direct current into a visible light output.

Microinstruction—A 32-bit word stored in the microstore of the microprogram control. This word is broken down into a FROM field (bits 7 through 0), a TO field (bits 15 through 8), a NEXT ADDRESS field (bits 27 through 16), a 2-bit control field (bits 28, 29), and a 2-bit parity field (bits 30, 31). The TO and FROM fields are decoded and used to enable the gating from a source register to a destination register for data transfer. The NA field contains the address of the next microinstruction to be executed. These fields are sometimes used for other special purposes.

Parity Check—A hardware check which tests whether the number of 1s in a word is even or odd.

Parity High—A parity bit carried for bits 8 through 15 of information (in 16-bit words).

Parity Low—A parity bit carried for bits 0 through 7 of information.

Real Time—Actual time of occurrence of an event. A real time control system is one in which operations are performed by the control equipment in time with a physical process such that the outputs obtained are useful in controlling that process.

Silicon Integrated Circuit (SIC)—An integrated circuit where all the elements such as transistors, diodes, resistors, and capacitors are successively fabricated in or on the silicon and interconnected.

Substrate—The underlying material upon which a device, circuit, or epitaxial layer is fabricated.

Transistor-Transistor Logic NAND Gate (Fig. 6)—The standard logic gate used throughout the 3A CC.

8. ABBREVIATIONS

8.01 The following abbreviations are used throughout this section:

CTI—Collector diffusion isolation logic to transistor-transistor logic interface

DMA—Direct memory access

DML—Data manipulation logic

ESS—Electronic switching system

HIC—Hybrid integrated circuit

I/O—Input/output

LED—Light emitting diode

MAS—Main store

MASB—Main store bus

MASC—Main store controller

MCH—Maintenance channel

PBC—Processor bus controller

PCH—Parallel channel

P$_H$—Parity high bit

P$_L$—Parity low bit

PT—Program timer

ROM—Read only memory

RTL—Resistor-transistor logic

SAR—Store address register

SDR—Store data register

SIC—Silicon integrated circuit

SSP—System status panel

TC—Timing counter

TTL—Transistor-transistor logic

TTY—Teletypewriter

3A CC—3A Central Control