INPUT/OUTPUT INTERFACES
DESCRIPTION AND THEORY OF OPERATION
COMMON SYSTEMS

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1. GENERAL

1.01 This section provides a physical and functional description and theory of operation of the input/output (I/O) interfaces between the 3A Central Control (3A CC) and its periphery.

1.02 When this section is reissued, the reason for reissue will be listed in this paragraph.

1.03 The I/O interfaces to the 3A CC consist of the following:

- Direct memory access (DMA) unit
- Parallel channel (PCH) unit
- Duplex bus selector (DBS)
- Collector diffusion isolation to transistor-to-transistor interface/power (CTI/power) unit
- RS232C serial interface (RSI).

PURPOSE

1.04 Three channels are provided to facilitate communication between the 3A CC and its peripheral devices (Fig. 1). These channels are the serial channel (SCH), the PCH, and the DMA. The SCH provides for low- and medium-speed data

transfer to peripheral devices. The PCH provides for medium- and high-speed data transfer. The DMA provides for the direct, independent transfer of blocks of data between main store and high speed peripheral devices. Also, the DMA reduces requirements for 3A CC control of data transfer and provides control over data transfer involving high speed peripheral devices (eg, PROMATS).

1.05 The I/O interface units use the outputs of 3A CC registers R9 and R10, with inputs gated to register R11. Register R9 contains address information, register R10 contains data to be transferred to peripheral devices, and register R11 receives data from peripheral devices.

- ***The DMA channel*** provides a means of transferring blocks of data directly between high speed peripheral devices and the main store (MAS) in the 3A CC. The DMA channel is controlled by the 3A CC but is related functionally to the MAS and the peripheral

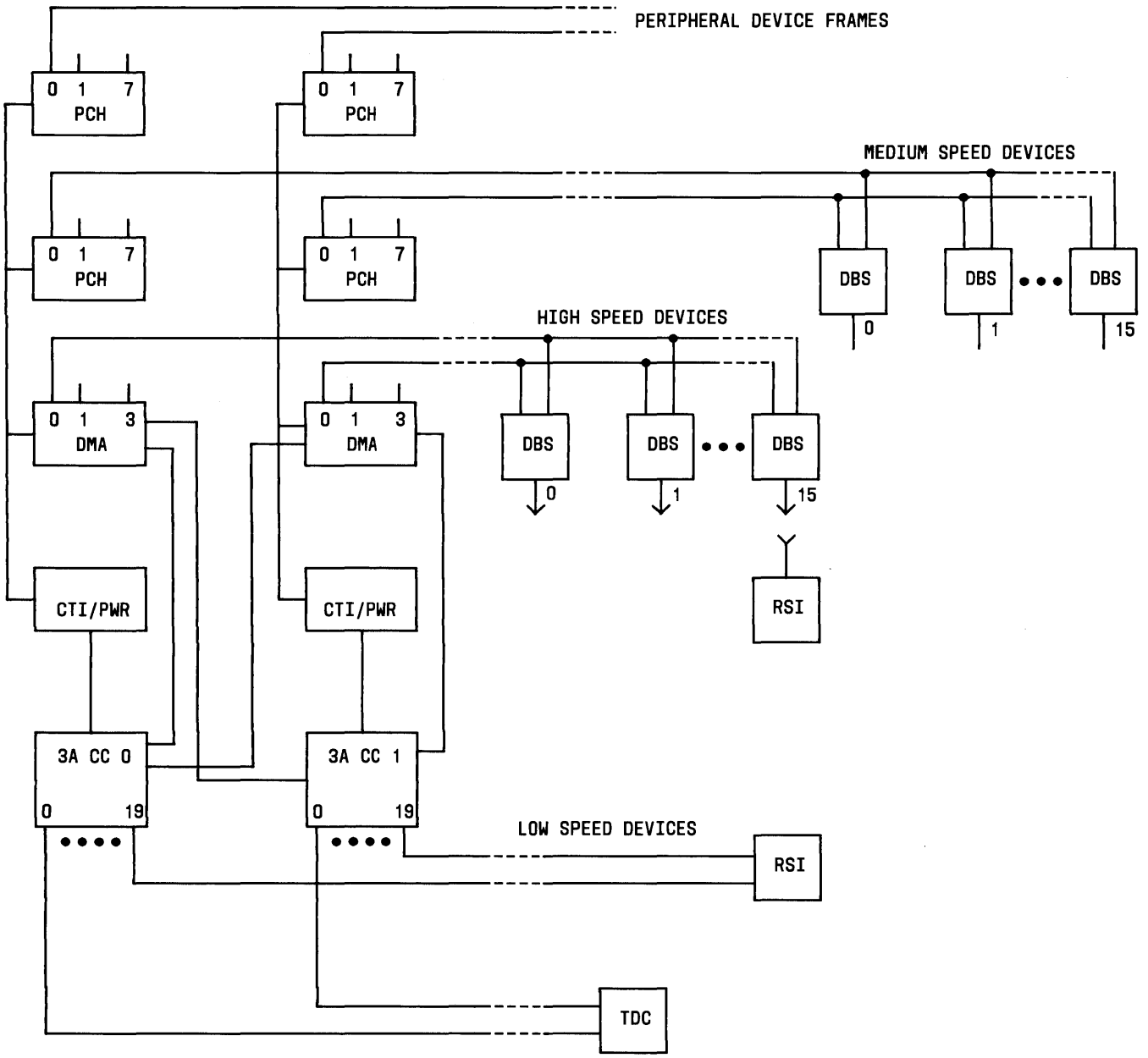


Fig. 1—3A CC Input/Output Interfaces

devices that have access to the DMA bus. The DMA unit provides the I/O interface between the 3A CC and these peripheral devices.

- ***The PCH unit*** provides a high speed data link between the 3A CC and peripheral devices that require a parallel interface for data transfer.

- ***The DBS*** is used to interface a peripheral device to a subparallel channel of the 3A CC. The subparallel channel (SPCH) is part of a PCH unit or a DMA channel unit. The DBS converts bipolar ac pulses from the channel unit to transistor-transistor logic (TTL) levels and transmits these signals to the peripheral device. Also, the DBS converts TTL signals from the peripheral device to bipolar ac pulses for transmission to the channel unit (PCH or DMA).

- ***The CTI/power unit*** converts collector diffusion isolation (CDI) logic (3 volts) level signals from the 3A CC to TTL (5 volts) levels required by the DMA and PCH units. Also, it converts TTL level signals from the DMA and PCH units to CDI level signals required by the 3A CC. The CTI/power unit also provides +5 volt power for the DMA and PCH units as well as fuses and power alarm circuits.

- ***The RSI*** is a serial line controller which interfaces the 3A CC using either the PCH or a serial peripheral interface (SPI) on a serial subchannel (SSCH), with any peripheral device having an interface that conforms to the Electronic Industries Association/RS232C (EIA/RS232C) standard for asynchronous serial data transfer.

CONFIGURATION

1.06 The 3A Processor can accommodate up to 20 SCHs, 2 PCHs, and 1 DMA unit. However, the 3A CC has only physical space to equip three SCHs within the 3A CC unit itself. All other SCHs must be mounted elsewhere. The number of I/O interface units used is determined by system requirements.

1.07 Each SCH can control up to 20 SSCH and associated serial peripheral devices and special circuits (eg, system status panel). The CTI/power unit provides the interface between the 3A CC and the PCH channel interfaces (PCH unit and DMA). The PCH unit consists of one main parallel channel that can control up to eight SPCHs. Each SPCH can service up to 16 peripheral devices via a parallel bus. The peripheral devices are interfaced to the parallel bus via the DBS. A single PCH can maintain up to 128 peripheral devices. The DMA is equipped with up to four SPCHs to communicate with the peripheral devices. Since each SPCH can service 16 peripheral devices (via DBS) the DMA can control a maximum of 64 peripheral devices. The RSI can interface between the 3A CC and the peripheral devices it serves via PCH or SCH. Each RSI unit contains up to four RSI circuits on one SPI.

1.08 The DMA unit is located in the upper part of the 3A Processor frame (Fig. 2). Three 14-card housings contain the DMA and associated main parallel channels and subparallel channels. (See Section 3 of this document.)

1.09 The PCH unit is located in the upper part of the 3A Processor frame. A 4-inch mounting plate and three 14-card apparatus housings are used. (See Section 4 of this document.)

1.10 The DBS is located in the peripheral device that requires its functions. Each DBS unit is housed in a type 80C 12-card front removable housing. (See Section 5 of this document.)

1.11 The SCH is located in and is considered an integral part of the 3A CC. Additional information is provided in Section 254-300-120.

1.12 The CTI/power unit is mounted in the upper part of the 3A Processor frame. The unit is installed on a mounting plate. There are three positions in the upper part of the mounting plate for three 132M-type power supplies. The lower portion of the mounting plate is dedicated to the CTI unit and fuses and power alarm circuits. (See Section 6 of this document.)

1.13 The RSI unit is mounted in a front-removable 80C 14-card apparatus housing, and is installed in the peripheral device that requires its functions or on equipment frames designated by the operating company. (See Section 7 of this document.)

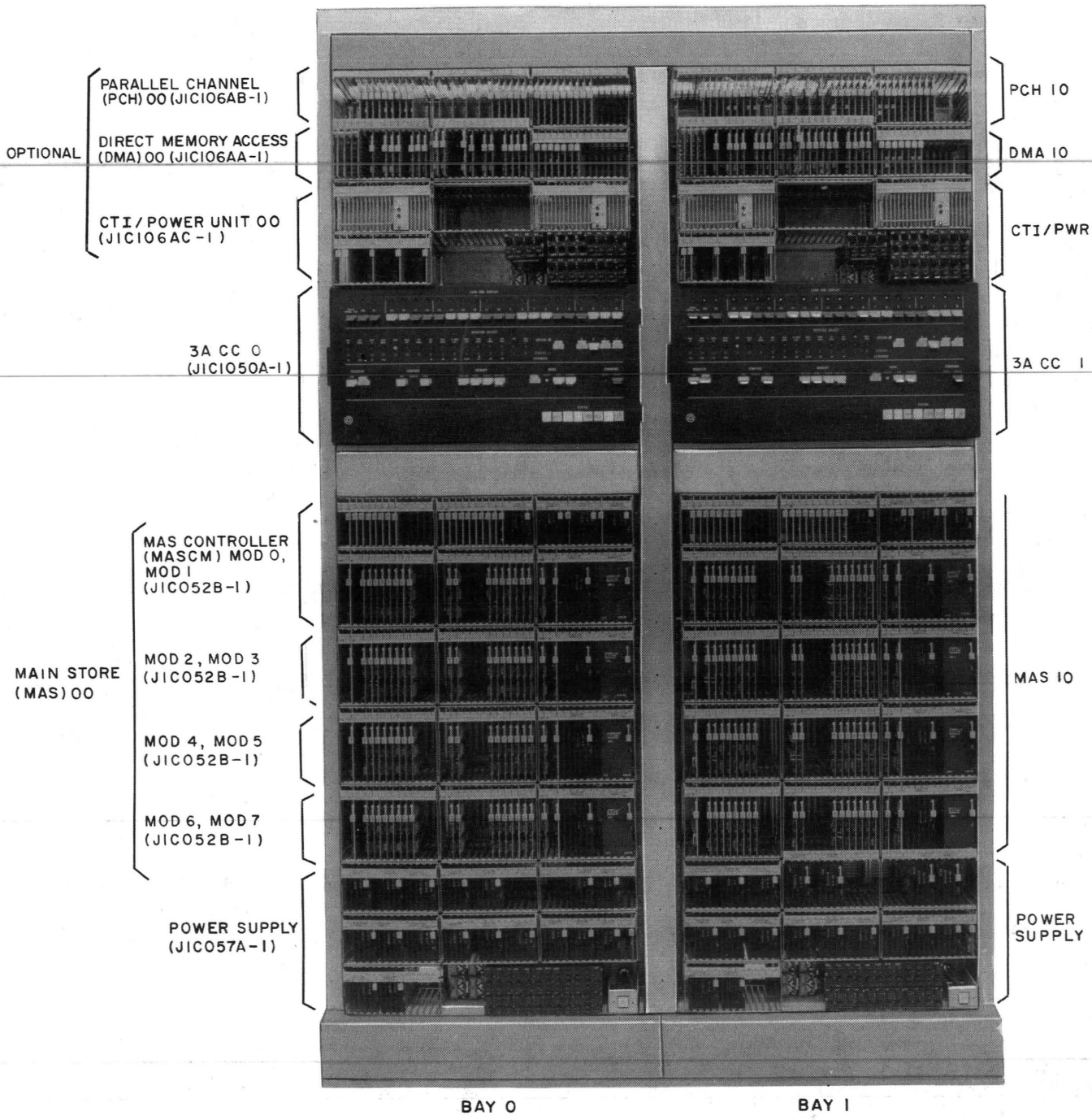


Fig. 2—Processor Frame

2. INTERFACES

2.01 The DMA interfaces with the 3A CC through the CTI/power unit which converts CDI logic (3 volts) level signals to TTL logic (5 volts) level signals (3A CC to PCH/DMA unit) and TTL logic level signals to CDI logic level signals (PCH/DMA unit to 3A CC). Also, the DMA interfaces with the MAS via the 3A CC and the MAS bus system. The DMA interfaces to its peripheral devices via an ac bus to the DBSs and then via TTL dc bus from the DBS to the peripheral device.

2.02 The PCH unit interfaces with the 3A CC via the CTI/power unit and with the peripheral devices via the DBS. The PCH unit interfaces the CTI/power unit via a parallel bus and with the DBS via an ac parallel bus.

2.03 The CTI/power unit interfaces the 3A CC via a parallel bus and the PCH unit or DMA via a parallel bus. Inputs to the CTI/power unit from the 3A CC are provided by general registers R9 and R10 in the 3A CC. Outputs to the 3A CC from the PCH unit or DMA via the CTI/power unit are received by 3A CC general register R11. The power supplies in the CTI/power unit receive -48 volts from the 3A Processor frame power. Output voltages (5 volts) and SENSE leads are provided to the DMA/PCH unit as required.

2.04 The RSI interfaces peripheral devices (eg, 202 series data set) via an RS232C serial link to the 3A CC via an SPI or DBS. The SPI is connected to each 3A CC by three coaxial cables. The DBS is connected to the 3A CC via an SPCH/PCH. The RSI is interfaced to the peripheral devices it serves via remote lines.

3. DIRECT MEMORY ACCESS UNIT

INTRODUCTION

3.01 The DMA channel provides a means of transferring blocks of data directly between a high-speed peripheral device (eg, a disk unit) and the MAS. Hereinafter, the high-speed peripheral device will be referred to as a device.

3.02 The DMA channel is controlled by the 3A CC but is related functionally to the MAS and the devices that have access to the DMA bus. In a duplex system configuration, the DMA channels transfer data into both MASs.

A. Physical Description

3.03 The DMA is located in the upper portion of the 3A Processor frame shown in Fig. 2. Three 14-card housings contain the DMA and associated main parallel channel (MPCH) and SPCH. Space is allotted in the housings for four SPCHs, but only one is normally equipped. The combined associated MPCH and SPCH will be referred to as the PCH.

3.04 The DMA (Fig. 3) requires 20 circuit packs (CPs) (including the four FB6 protection CPs). The MPCH consists of four CPs and each SPCH uses three CPs. The types and locations of these CPs are shown in Fig. 4. The DMA uses standard 1A multilayer etched CPs (Fig. 5). The CPs plug into standard (942) connectors mounted on the multilayer printed wiring board (MLPWB), which is located at the rear of each CP housing. Connections on the MLPWB backplane are made by solid 30-gauge wires wrapped onto terminal pins. Flat tape and shielded twisted pair cables are also used.

B. DMA Interfaces and Interconnections

3.05 The interfaces of the DMA to other units are shown in Fig. 6 and Fig. 7. Interconnections for the duplex system configuration are shown in Fig. 8. The DMA interfaces with the 3A CC through the CTI/power unit. Also, the DMA interfaces with the MASs through the 3A CC via the standard MAS bus system. The MAS bus

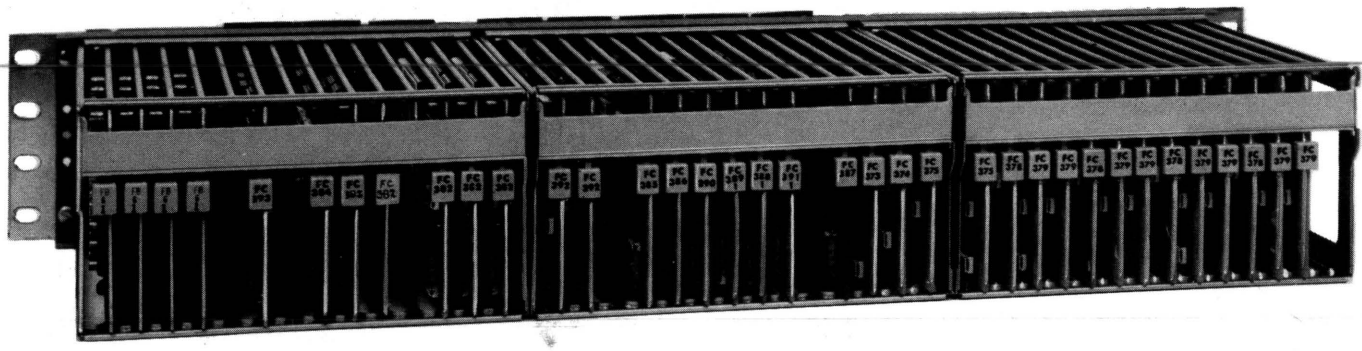


Fig. 3—DMA Unit

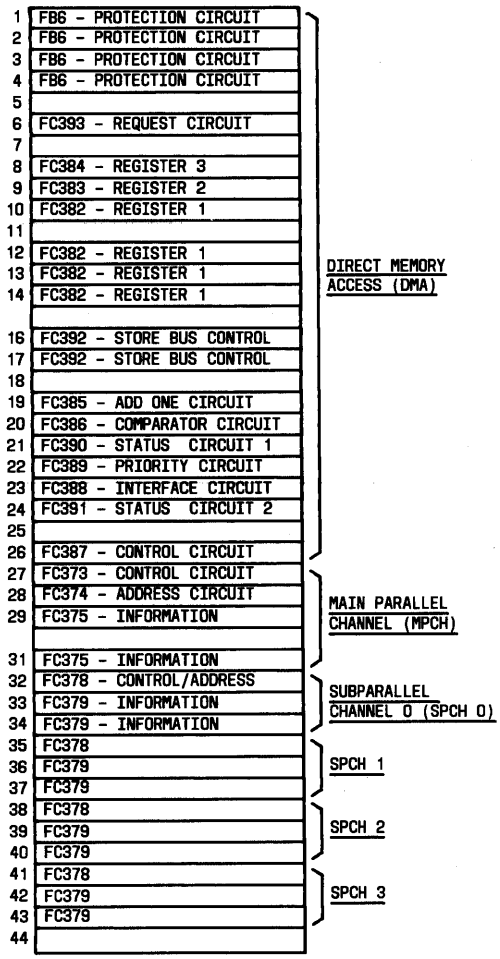


Fig. 4—DMA Circuit Pack Locations

(sometimes referred to as the memory bus) provides the necessary parallel commands, address, and data to access the MASs. The DMA interfaces with the devices via an ac bus (SPCH) to the DBSs and via a TTL bus between the DBSs and the devices.

3.06 Three MAS bus ports are provided by the DMA and are used as follows:

(a) One accesses the MAS of the mate side of the duplex configuration via the mate 3A CC (eg, DMA 0 to 3A CC 0 to MAS 0).

(b) One accesses the other MAS via the mate 3A CC (eg, DAM 0 to 3A CC 0 to DMA 1 to 3A CC 1 to MAS 1).

(c) One is used by the other 3A CC to access the mate MAS (see example in b).

3.07 An MPCH using SPCHs interfaces with the devices via DBSs. The MPCH is equipped with a maximum of four SPCHs. Each SPCH has the capacity of addressing the devices via 16 DBSs; therefore, the capability of supporting 64 devices is provided. A maximum of 16 devices can transfer data through the DMA simultaneously, provided the combined effective transfer rate does not exceed the maximum transfer rate of the DMA. The 16 active devices can be distributed among the SPCHs. However, devices with the same address but on different SPCHs are not permitted to be active at the same time. All active devices must have unique addresses.

3.08 The 5-volt power for the DMA is supplied by converters in the CTI/power unit located below the DMA. The 3-volt power is supplied by a power converter located at the bottom of the processor frame.

3.09 Control of the DMA is implemented by software. Manual controls to directly operate the DMA are not provided.

C. Functional Description

Introduction

3.10 The state of the DMA and the information pertinent to data transfer of the devices are stored in various registers internal to the DMA (Fig. 9). The state, mask, control, status, error data, and memory data registers are single-word registers used by all the devices attached to the MPCH. The data buffer, flag, parameter, present address low (PAL), present address high (PAH), final address low (FAL), and final address high (FAH) are 16-word registers that contain one word for each active device.

DMA Registers

3.11 The ***data buffer register*** provides intermediate storage between the device and the MAS. When the device sends a word to memory, the word is first stored in the data buffer register. The first word is transmitted to the memory when the next request from the same device is being serviced and the second word is received in the data buffer. Therefore, the time required to access the memory and the time required to fetch the next word from the device can be overlapped. The data buffer register is

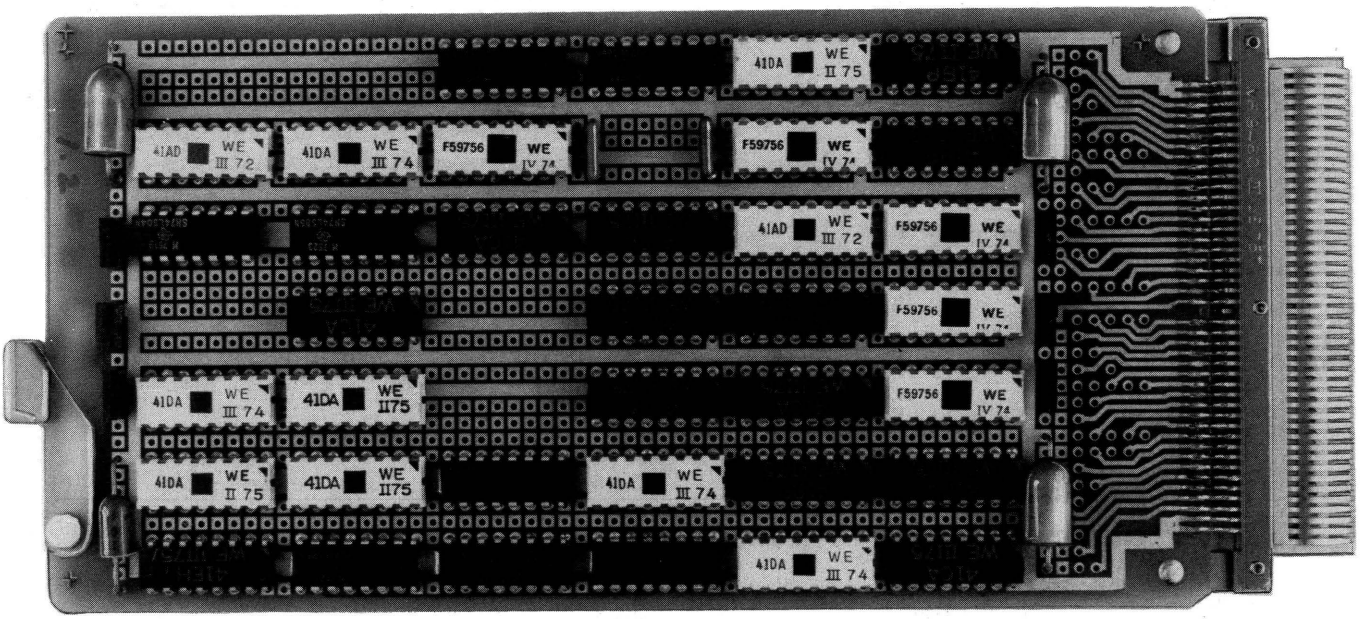


Fig. 5—Typical Circuit Pack

used in the same manner when a transfer from memory to the device is made.

3.12 The ***parameter register*** is used to establish the conditions relevant to a data transfer. Bit assignments and functions are shown in Table A. Conditions are stable until the data transfer is complete. The ***flag register*** monitors progress of the data transfer and principally maintains the error status (Table B).

3.13 The ***control register*** contains information pertinent to data transfers of all active devices. When bit 15 of the control register is set, the mate 3A CC is prevented from accessing the memory. The remaining bits are used primarily for maintenance purposes. Refer to Table C for the bit assignments.

3.14 Error conditions detected by the DMA are flagged by setting bits in the ***status register*** (Table D). Bit 5 (DMA error) is a summary status bit that reports the existence of an error. Any error condition detected locks the DMA in the state which the error was found.

3.15 The ***memory data register*** is used as a buffer for interfacing with the memory bus. It operates in conjunction with the ***error data register,*** which is loaded with data from the memory when the memory controller signals a parity error on a read command. With a parity error indication, the DMA will abort the data transfer for the device. Later, the 3A CC can read the error data register and analyze the data. It can then redirect the DMA to read data from the other memory or invoke complement correction and restart the data transfer from the same memory.

3.16 Different states of the DMA are generated by the ***state register.*** It is implemented by a parallel-in/parallel-out rotating shift register.

3.17 The ***mask register*** inhibits the DMA request (DMAR) signal from devices which are out of service. When a bit corresponding to a device is set to zero, the DMA will not respond to the request. This enables the DMA to continue functioning if a DMAR lead is stuck.

3.18 The ***PAL register*** is used to service the low 16 bits of the MAS address for the ***next*** MAS access. The ***PAH register*** is used to service the high 4 bits of the ***present*** MAS address plus 4 parity bits used across the 20-bit present address. Similarly, the FAL and FAH registers, including parity bits, service the MAS address for the ***final*** MAS access.

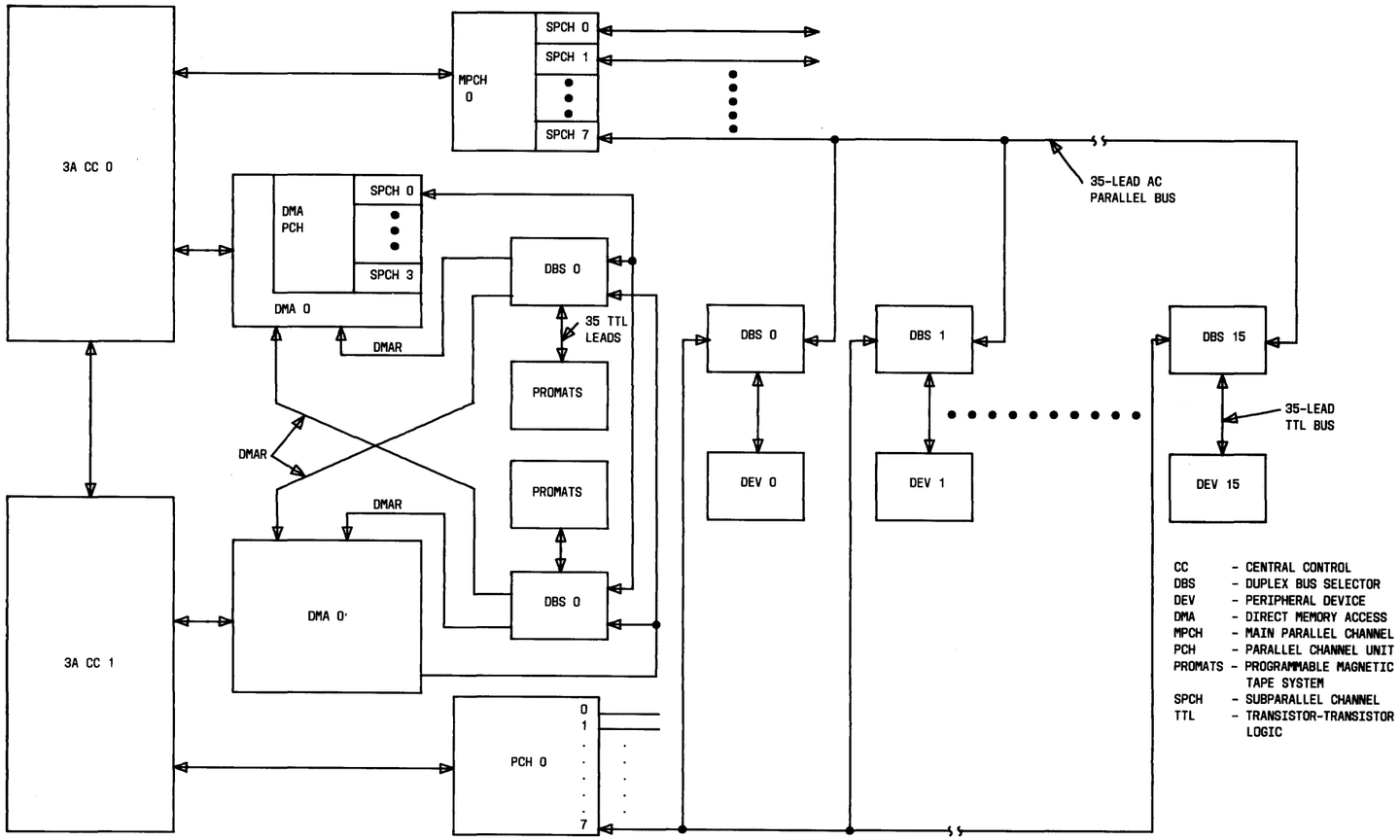


Fig. 6—DMA System interface

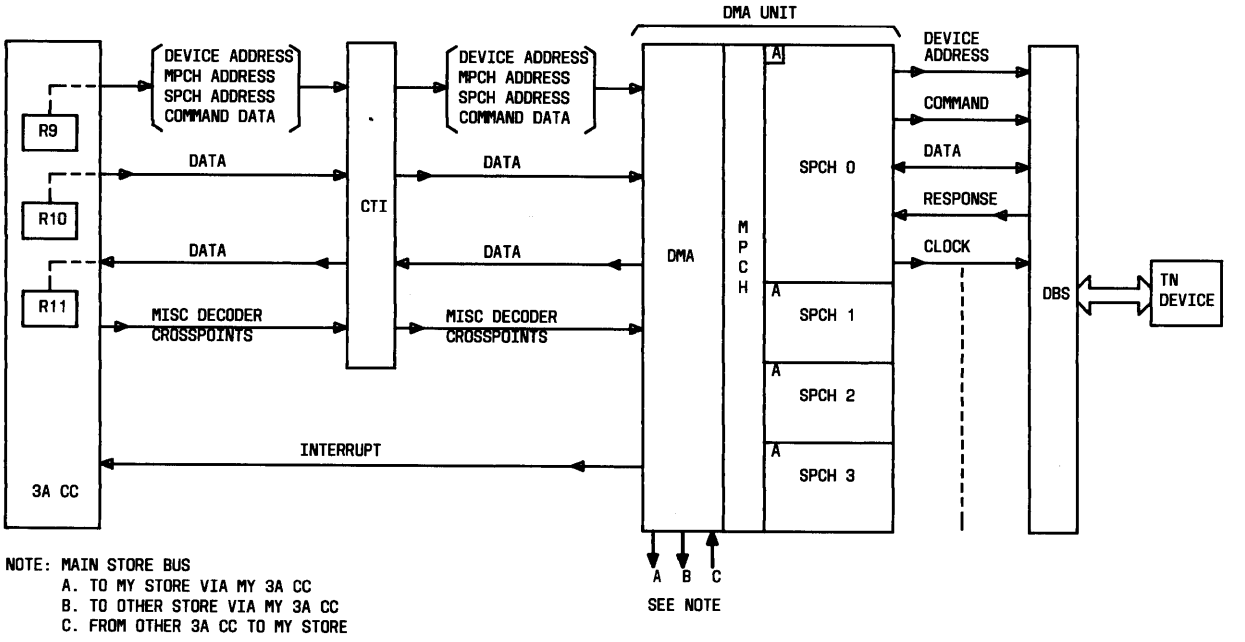


Fig. 7—DMA Interfaces

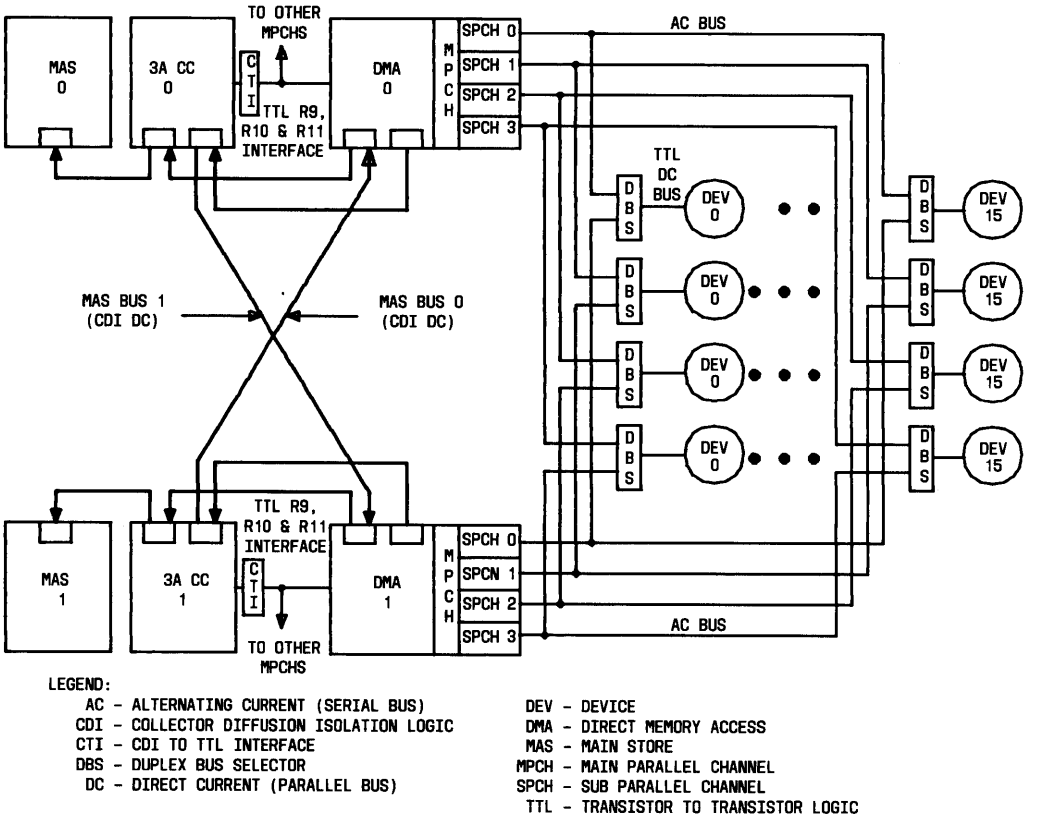


Fig. 8—3A Processor Duplex Configuration

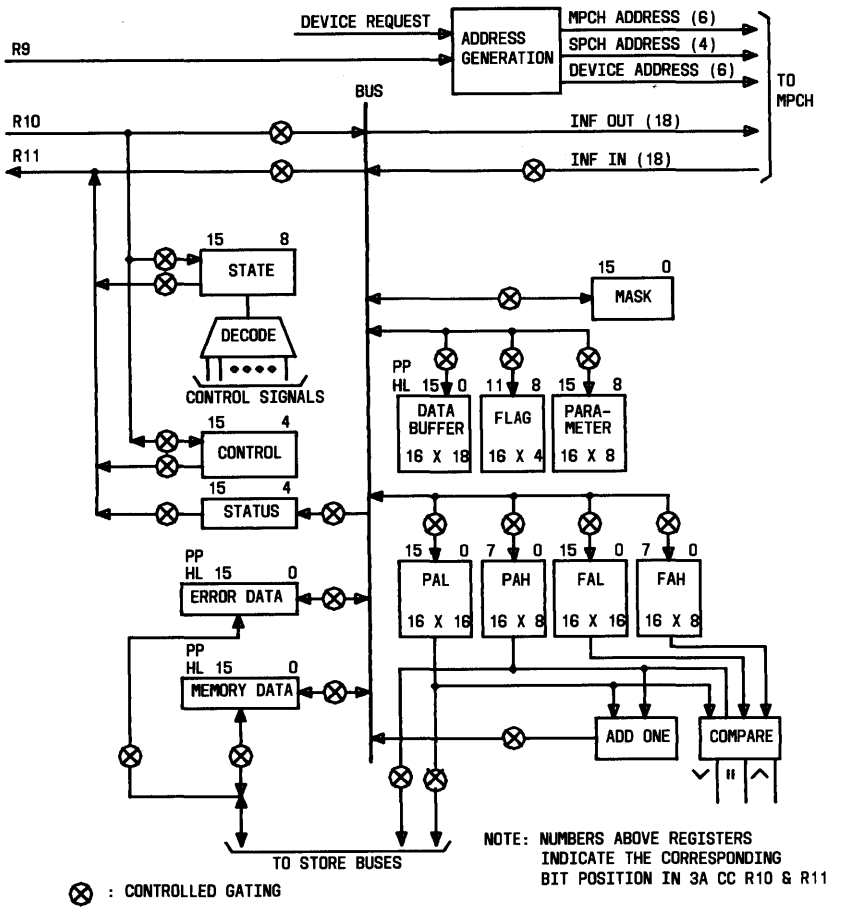


Fig. 9—Register and Data Paths Inside the DMA

3.19 For the 3A CC to start a device for data transfer, the PAL and PAH registers of the device must be loaded with the address of the first memory location to be read or written. The FAL and FAH registers must be loaded with the address of the last memory location for writing the memory or with one plus the address of the last location for reading the memory.

DMA Related Instructions

3.20 The PCH and DMA instructions are required to set up the direct memory data transfer for a device. The PCH instructions are used to set the device to a proper state, and the DMA instructions are used to prepare the DMA for processing the data transfer for the device. The DMA instructions are described in Table E. The address of the PCH associated with the DMA (010101) should be used for all PCH instructions, and the address of the DMA (010110) should be used for all DMA instructions.

DMA Operation

3.21 When the system is first placed in service, the initialization DMA instruction should be executed to place the DMA in a known inactive state. The DMA can be placed in an active state by writing 01010101 into the state register. Then the mask register is loaded with 1s in the bit positions corresponding to the addresses of devices allowed to make DMA requests. In an active state, the DMA repeatedly senses whether there is a request from the 3A CC or from the 3A CC devices according to assigned priorities. After the DMA has been properly set up for the data transfer from a device, the 3A CC commands the device to start the data transfer by using PCH instructions. The 3A CC is now available for other work while the

TABLE A

PARAMETER REGISTER BIT ASSIGNMENTS

BITS								ASSIGNMENT
7	6	5	4	3	2	1	0	
0	0							SPCH address of device
0	1							
1	0							
1	1							
		0	1					Access MY MAS
		1	0					Access OTHER MAS
		1	1					Access both MASs
				0	0	1	1	Read
				0	1	0	1	Spare
				1	0	0	1	Read the write protect register
				1	1	0	0	Write with write protect
				1	0	1	0	Write without write protect
				0	1	1	0	Write the write protect register

TABLE B

FLAG REGISTER BIT ASSIGNMENTS

BITS				ASSIGNMENT
3	2	1	0	
1	1			Normal
0	1			MAS read parity error
1	0			MAS write protect error
0	0			All other MAS errors
		1		Normal
		0		Device error
			1	Internal flag to DMA
			0	

DMA processes the data transfer between the device and the MAS. An interrupt will be generated from the device after the data transfer is completed or when abnormal conditions are detected. Functions of the PCH (MPCH and SPCH) associated with the DMA are the same as the PCHs used for medium-speed devices and are covered in Section 4 of this document.

Data Transfer Setup Procedure

3.22 In order to start direct memory data transfer from a device, the DMA registers corresponding to the device must be properly set up. A flowchart of the setup sequence is shown in Fig. 10. The PAL and PAH registers are loaded with the address of the first memory location to be read or written. The FAL and FAH are loaded with either the address of the last memory location to be written or one plus the address of the last memory location to be read. After loading the registers, an instruction (TDMA) is executed to ensure that the decoder for loading the registers is free of faults. While reading, the TDMA instruction can be executed to fetch the first word into the data buffer register for the device.

TABLE C

CONTROL REGISTER BIT ASSIGNMENTS

	BIT	MNEMONIC	ASSIGNMENT
Not Equipped	0		
	1		
	2		
	3		
FC391 Status 2	4	SYNC	SYNC signal from MPCH
	5	STCOMP	Store complete signal
	6	STEP	DMA in single-step mode
	7	CCFF	DMA access to MAS when 3A CC flip-flop in system status register is not set
FC390 Status 1	8	PMODE	DMA in parallel channel (PCH) mode
	9	MTN	DMA in maintenance mode (all DMA signals forced active)
	10	TESTA	Disable one path of comparator logic which detects PA=FA
	11	TESTB	Disable other path of comparator logic which detects PA=FA
	12	SAC	Request MAS to complement a data word if both parities of the word are incorrect
	13	OLCK	Disable OTHER MAS bus control circuit
	14	MLCK	Disable MY MAS bus control circuit
	15	MISO	Isolate MY MAS bus from OTHER 3A CC
	9&13	FDVER	Force device error
	9&14	FDGTER	Force data gating error

Data Transfer Termination Procedure

3.23 When the 3A CC recognizes the interrupt from the device, a termination sequence is performed to ensure that the transfer was successfully completed. Refer to Fig. 11 for a flowchart showing this termination sequence. The contents of the PAL and PAH registers must match the expected final address. Any discrepancy indicates the number of words transferred is incorrect. Any error condition in the status register sets a bit in the error register of the 3A CC and initiates a separate interrupt.

D. Theory of Operation

Introduction

3.24 The DMA is designed to operate in a duplex system consisting of two DMAs and two 3A CCs (Fig. 8). Each DMA can communicate with both MASs. Each device on the DMA channel can be accessed by either DMA via the DBS. The DMA and the 3A CC use the same bus to access the MAS; therefore, the 3A CC and the DMA cannot access the memory at the same time.

TABLE D

STATUS REGISTER BIT ASSIGNMENTS

	BIT	MNEMONIC	ASSIGNMENT
Not Equipped	0		
	1		
	2		
	3		
FC391 Status 2	4	VFREQ	Device request verification
	5	DMAER	DMA error
	6	DGTER	Data gating error
	7	STERR	State error
FC390 Status 1	8	SPARE	Spare
	9	CNTER	Counter error
	10	DAER	Device address parity error
	11	PAGFA	Present address greater than final address
	12	FAER	Final address parity error
	13	PAER	Present address parity error
	14	DRER	Data ready mismatch error
	15	CHER	Parallel channel error

3.25 The DMA services all its active devices on a request basis. When a device is ready to send or receive data, the device sets its DMAR lead. Each group of devices with the same address is assigned a priority level. The higher the address, the higher the priority. The DMA periodically senses the DMAR leads which are seeking a request. Requests when detected are transmitted into a priority receiving circuit, which sets the DMAR lead and generates the address of the device with the highest priority. If no 3A CC request is present (the 3A CC has first priority), the DMA goes into a sequence to transfer a data word to or from the device with the address that has just been generated. When the transfer is complete, the DMA returns to the request-seeking mode.

3.26 ***MY*** refers to the unit under consideration. It is interconnected to a duplicate unit that provides an alternate unit function to assure performance. ***OTHER*** refers to a duplicate unit that is interconnected with the currently active unit to provide an alternate unit function to assure performance. In a duplex configuration, duplicate units are usually designated 0 and 1. ***MY*** can be either the 0 or 1 unit depending upon which unit is considered currently active. ***OTHER*** always refers to the support unit.

Communication With MAS

3.27 The DMA communicates with the MAS via the 3A CC using the standard parallel MAS bus. The MAS bus consists of 53 leads that support 6 major functions: ***control, error, response, command, data,*** and ***address.*** These leads and associated functions are identified in Fig. 12. Two buses are used for accessing the two MASs in a duplex system. A third bus is connected to the OTHER 3A CC and can provide access to MY MAS from the OTHER 3A CC. All leads of the third MAS bus enter the DMA through four FB6 fuse packs (Fig. 13) to protect against overvoltage

TABLE E

DMA INSTRUCTIONS

INSTRUCTION	MNEMONIC	DESCRIPTION
Initialize DMA	IDMA	DMA is placed in inactive state. Control, status, and mask registers are cleared. All internal control flip-flops are cleared.
Lock DMA	LDMA	DMA is placed in inactive state. This is used for maintenance purposes only.
Step DMA	SDMA	Single-step mode bit of control register must be set. DMA is advanced to the next state. This is for maintenance purposes only.
Write DMA	WDMA REG NAME	Load the specified DMA register from R10 of 3A CC. The DMA register is read back and matched with R10. A mismatch causes a DML mismatch interrupt. CF will be cleared if it takes too long for the DMA to respond.
Read DMA	RDMA REG NAME	Read the specified DMA register into R11 of 3A CC. Parity error causes a data bus parity error interrupt. CF will be cleared if it takes too long for the DMA to respond.
Read/write memory	MDMA	If bits 0 through 3 of parameter register are loaded with a read command, the contents of the memory location specified by PAL and PAH registers are read into the data buffer register. If bits 0 through 3 of the parameter register are loaded with a write command, the contents of the data buffer register are written into the memory location specified by PAL and PAH registers. CF will be cleared if it takes too long for the DMA to respond.
Test DMA decoder	TDMA	The decoder for reading and writing the DMA register is tested. CF will be cleared if the test failed or if it takes too long for the DMA to respond.

propagating from one side to the other in a duplex system.

3.28 After being fused, the control, error, and response leads are applied to MAS bus control circuit packs (FC392). There is one each for communicating with MY MAS and the OTHER MAS in a duplex system. The store bus control (SBC) circuits are used for processing communications with the MASs. The SBC runs asynchronously with the DMA sequencer. The SBC responds to the DMA sequencer requests (eg, requests access to either MAS or both simultaneously). Each MAS bus is released by the DMA as soon as access is complete. However, when both MASs are being accessed, completion is not reported to the sequencer until access to both is complete.

3.29 The DMA and 3A CC units share the MAS bus. Signals on the MAS bus from a unit are blocked by the unit which is physically closer to the store. When the bus is freed by the unit closer to the MAS, the signals from the other unit can be transmitted to the MAS and the closer one is blocked from using the MAS until the bus is freed. Under normal conditions, both the 3A CC and the DMA release the MAS bus after each store access.

3.30 The MAS errors during DMA access will cause internal flags to be set. Communication

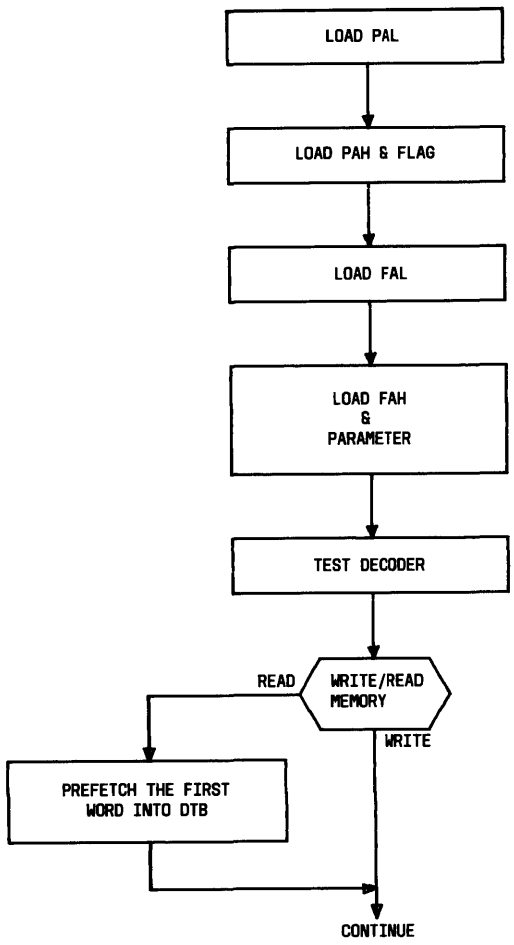


Fig. 10—Data Transfer Setup Procedure

with the device is aborted. When parity indicates a faulty read from the MAS, the faulty word is buffered in the error data register (EDR) for later analysis. To prevent faults in the off-line DMA from gating erroneous signals onto the MAS bus, the 3A CC inhibits DMA MAS bus access by clearing bit 12 of the system status register (3A CC flip-flop) in the off-line 3A CC.

3.31 For communicating with the MAS via the 3A CC, several key flip-flops are included in the FC392 circuitry. The data ready (DR) flip-flop indicates that MAS access is complete. The SEIZE flip-flop implements DMA seizure of the MAS bus. The GO flip-flop provides the store go (SGO) signal to the MAS. The enable data ready (ENBDR) flip-flop enables the DR flip-flop being set when MAS access is completed. The enable release (ENREL) flip-flop prevents the DMA from making another MAS access before the MAS is ready.

3.32 Access to the MAS is triggered by a signal (TGMRY1) that clears the DR flip-flop. When the store bus becomes idle [ie, SGO, store complete (SCMP) and store error C (SERC) are no longer active], the SEIZE flip-flop is set. The seize signal sets the GO flip-flop that sends the SGO signal to the MAS. When SCMP is active, the ENBDR flip-flop is set, which enables the DR and ENREL flip-flops to be set. Output of the DR flip-flop causes the ENBDR flip-flop to be cleared. Output of the ENREL flip-flop clears the GO flip-flop. Finally, the seize and ENREL flip-flops are cleared when the SCMP becomes inactive.

3.33 After being fused, command, data, and address leads/signals are applied to register CPs (Fig. 13). Command, data, and address information is communicated between the register CPs (four FC382s, one FC383, and one FC384) to MY/OTHER MAS via MY 3A CC utilizing the MAS bus. All registers on these CPs are loaded and read from and to the 3A CC via the DMA internal bidirectional bus. Each device (to a maximum of 16) has its own set of certain registers. These registers are implemented with a 4-bit by 16-word random access memory (RAM) integrated circuit providing 16 copies of each register. The device address is used as the address of the RAM for accessing registers for the device.

3.34 Register CP FC382 is used four times in the DMA to accomplish bit partitioning for improved reliability and to implement the following 16-bit registers:

- DTB—Data buffer
- PAL—Present address low
- FAL—Final address low
- MDT—Memory data
- EDT—Error data
- MSK—Mask.

Register bits are distributed in the four FC382 CPs so that one CP provides bits 0, 4, 8, and 12; one CP, bits 1, 5, 9, 13; one CP, bits 2, 6, 10, and 14; and one CP, bits 3, 7, 11, and 15. The DTB,

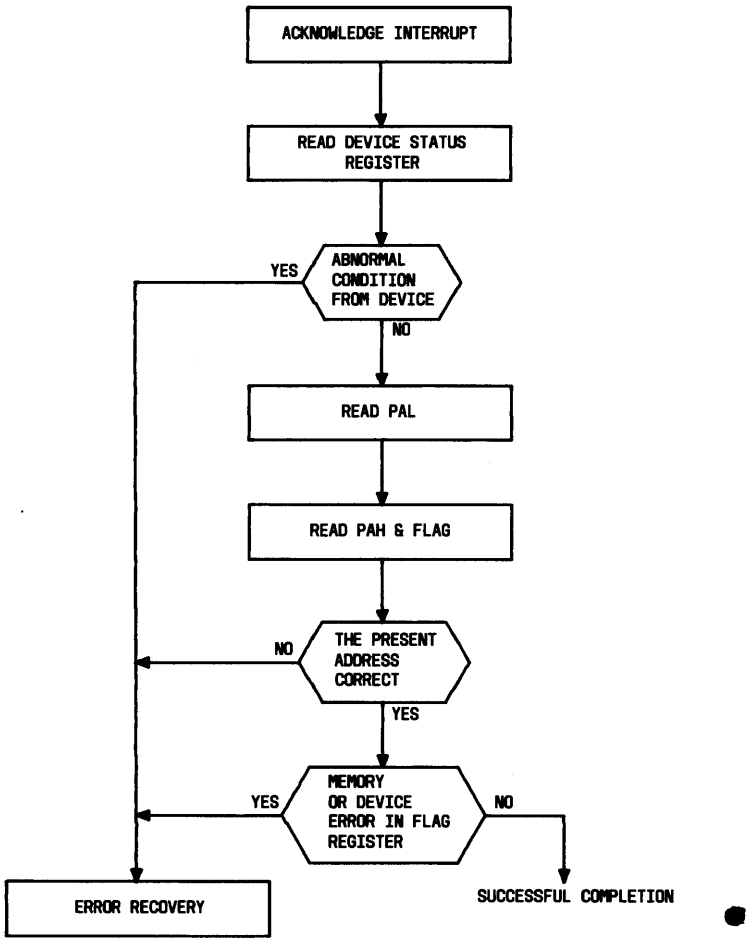


Fig. 11—Data Transfer Termination Procedure

PAL, and FAL registers are implemented by a 4-bit by 16-word RAM providing 16 registers one for each of the active devices. The MDT, EDT, and MSK registers are implemented by 4-bit single-word registers. These are ***shared*** by all devices.

3.35 Repeaters for interfacing with the MAS bus are implemented by hybrid integrated circuits (145T and 143AD for unidirectional and bidirectional repeaters, respectively). Communication with the MAS including MAS address is unidirectional. The MAS data is an exception and is bidirectional. Repeaters for MY MAS bus are controlled by MY GO (MGO1) and MY WRITE signals. Repeaters for the OTHER MAS bus are by the OTHER GO (OGO1) and OTHER WRITE (OWT1) signals. When the MGO1 or OGO1 signal is zero, MY or the OTHER MAS bus repeaters are enabled. When these signals are logic one, the associated repeaters are isolated and the PAL register is gated onto the MAS bus. The MDT register is loaded from MAS bus by load memory data register signal (LDT0), and the bus is loaded from MDT register by gate memory data register signal (GDT0). A bad parity word read from the MAS is loaded into the EDT register. Bits 8 to 15 of 3A CC register R10 can be gated onto the DMA internal bus via FC382s, and the corresponding bits on the internal bus can be gated to 3A CC register R11.

3.36 Register CP FC383 (register 2) provides four bits for each of the following registers:

- PAH—Present address high
- FAH—Final address high

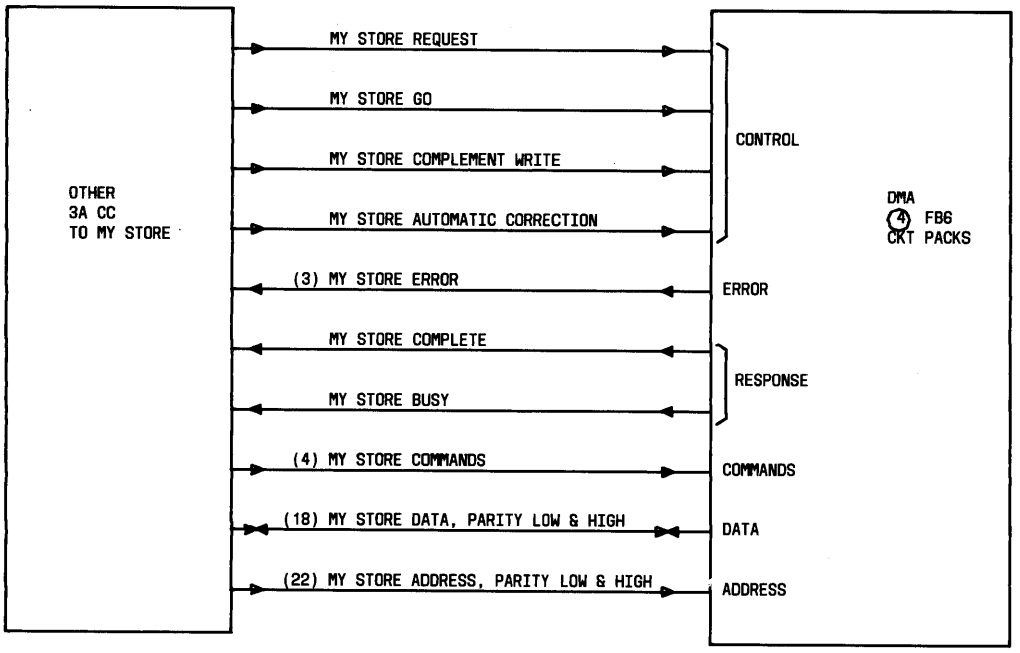


Fig. 12—Main Store Bus Leads

- FLAG—Flag
- PARM—Parameter.

The four bits contained in PAH and FAH registers are 16 through 19. The PARM register contains 2-out-of-4 commands to the MAS.

3.37 Repeaters for interfacing with the MAS bus are implemented as in FC382 and are also controlled by GO except that the PAH and PARM registers are gated onto MY or OTHER MAS bus. Another function performed in FC383 is a parity check of the DTB register.

3.38 Register CP FC384 (register 3) contains another four bits of the PARM register. Parity bits are supplied for the PA, FA, DTB, MDT, and EDT registers. The PA and FA have four odd parity bits. Each parity bit covers four bits of its associated register. The DTB and MDT registers use two odd parity bits each, one to check bits 0 through 7 and the other to check bits 8 through 15. The DTB, PAH, and FAH registers are implemented as in FC382 with 16 copies. The MDT and EDT registers are implemented by 4-bit single-word registers and are shared by all devices.

3.39 Repeaters for the MAS bus are controlled by the go and write signals. Two parity bits of the PA, one over bits 0 through 7 and one over bits 8 through 19, are generated and gated onto the MAS bus. The MDT register is gated onto the MAS bus or loaded from the MAS bus depending on the write signal 0 or 1, respectively. Bad parity words from the MAS are also loaded into the EDT register. Parity high (P_H) and parity low (P_L) bits of 3A CC register R10 can be gated to the DMA internal bus, and the corresponding bits on the bus can be gated to 3A CC register R11.

DMA Address Monitoring Circuits

3.40 The add-one CP FC385 and the comparator CP FC386 monitor the present MAS address (Fig. 13). The main function of FC385 is to increment the 20-bit present address via a 20-bit binary counter, which is directly loaded from the PA register. Output of the counter is gated to the internal bus and loaded back into the PA register as the next address. A parity generator provides four odd parity bits used to cover the next address. After the counter is incremented by adding one, its output is compared with its input to assure that the next address is not less

than the PA. If the next address is greater than the PA, a counter error is reported. Parities of the PA are checked. Also, parity bits are generated for use while the 3A CC is loading the PAH register. For interfacing with the 3A CC, bits 4 through 7 of R10 can be gated onto the internal bus, and the corresponding bits on the DMA internal bus can be gated back to R11 of the 3A CC.

3.41 The comparator CP FC386 compares PA with FA. When PA equals FA, the end of the data transfer is signaled. If PA is greater than FA, an error will be reported. Parities of the FA are checked. Also, parity bits are generated for use while the 3A CC is loading FAH register. For interfacing with the 3A CC, bits 0 to 3 of R10 can be gated onto the DMA internal bus, and corresponding bits on the internal bus can be gated back to R11 of the 3A CC.

DMA Interface Control With 3A CC and Devices

3.42 Communication between the 3A CC and the devices via the DMA are controlled essentially by CP FC387, control; CP FC388, CC interface; CP FC389, priority; and CP FC393, DMA request (Fig. 13). The state register contained in FC387 is an 8-bit shift register that is rotated to generate different states of DMA control. It can be parallel loaded with bits 8 through 15 of the 3A CC general register R10. The DMA is in the ***inactive*** state when the state register is loaded with all zeros. To initialize the DMA to the ***active*** state, the state register is loaded with the value 01010101. During the active state, the DMA state register alternates between the 01010101 and 10101010 states. When a request is received by the DMA, the state register is loaded with the value 00001111.

3.43 Normally, the 3A CC clock phase 1 (P10) is used in FC387 to advance the state register to the next state. During certain functions, the clock is inhibited; eg, when an internal error is detected by the DMA, while the DMA is waiting for a valid response (SYNC signal) from devices, and when the DMA is in the single-step maintenance mode. Activating 3A CC crosspoint MD5 (single-step DMA) with the DMA address in R9 enables the clock for one cycle, which advances the state register to the next state. Output of the state register can be gated back to bits 8 through 15 of 3A CC register R11.

3.44 Circuitry in FC388 decodes the contents of 3A CC register 9 and generates appropriate control signals for processing 3A CC requests. The types of 3A CC requests are as follows:

(a) Load or read DMA registers (register sequence).

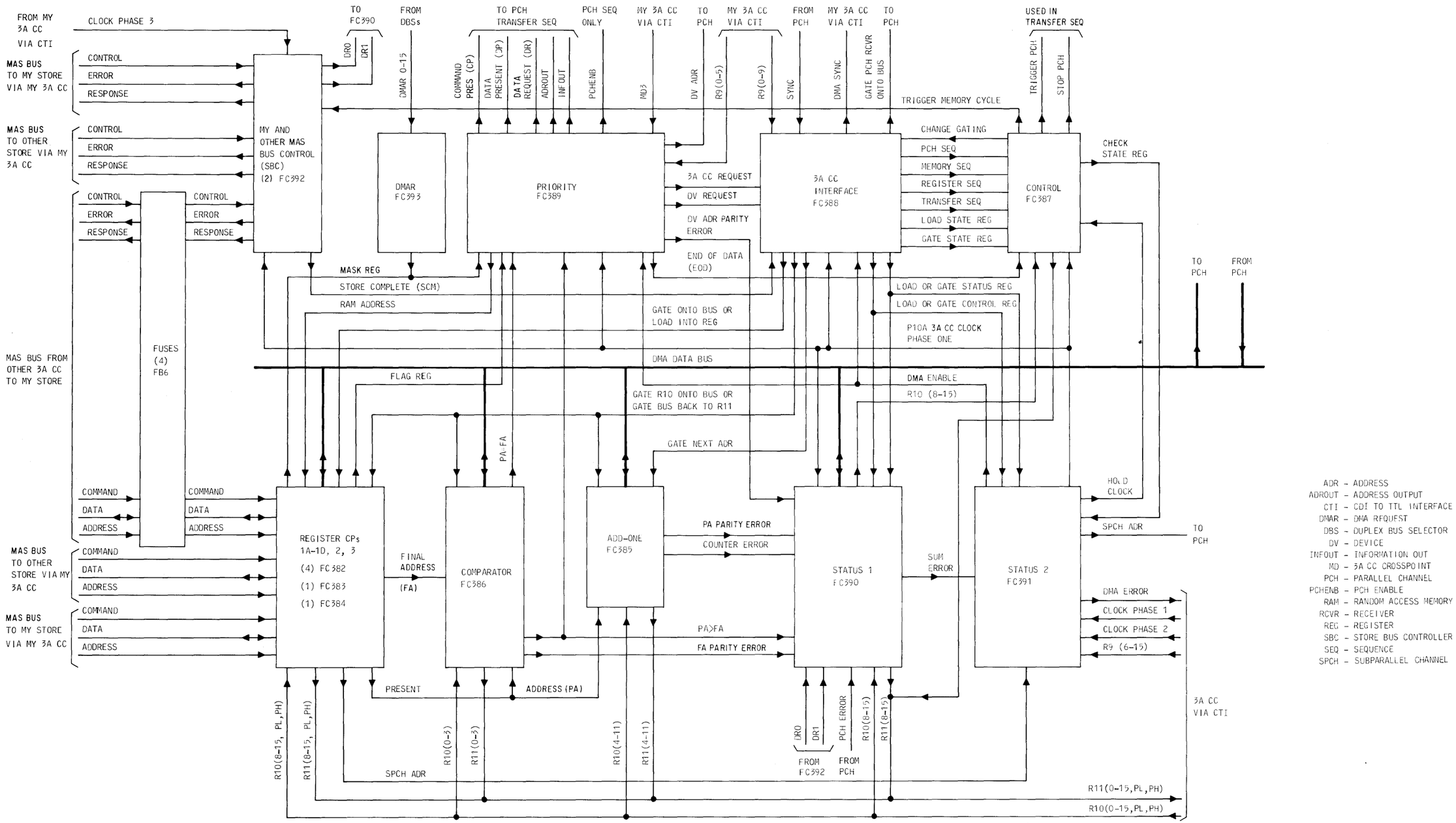
(b) Fetch a word from the MAS to the DTB register or write the contents of the DTB register into the MAS (memory sequence).

(c) Use the parallel channel (PCH) for communicating with the devices (PCH sequence).

For each of these requests, a different DMA sequence is used. The DMA distinguishes 3A CC requests through the contents of register R9. The PCH address in bits 10 through 15 of register R9 indicates that the 3A CC wants to communicate with a device. Also, bits 6 through 9 contain the SPCH address, and bits 0 through 5 contain the device address. Bits 10 through 15 in the DMA address indicate that the 3A CC request to read/load a DMA register or to store/fetch a word to/from the MAS. Bits 0 through 9 are used to specify the exact request.

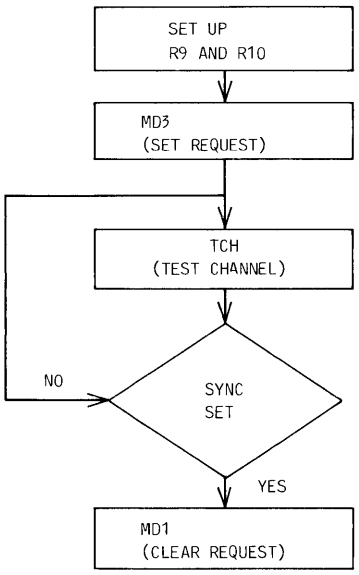
Register Sequence

3.45 In the register sequence, 3A CC register R10 is used for storing data to be loaded into the DMA registers. Register 11 of the 3A CC is used for receiving data from the DMA registers. The 3A CC can access the DMA registers via either one of two gating paths. One path provides direct register access through registers R10 and R11. The DMA registers can be read or loaded without a 3A CC request to the DMA through this path. The 3A CC sets up registers R9 and R10 and executes an input/output (I/O) crosspoint signal to load or read the register. The second path allows DMA registers to be accessed only through the internal data bus. This access requires a 3A CC request to the DMA in order to load DMA registers. Upon acknowledgment of the request, DMA starts the sequence. A flowchart of 3A CC microcontrol of DMA register sequence and an associated state diagram are shown in Fig. 14.

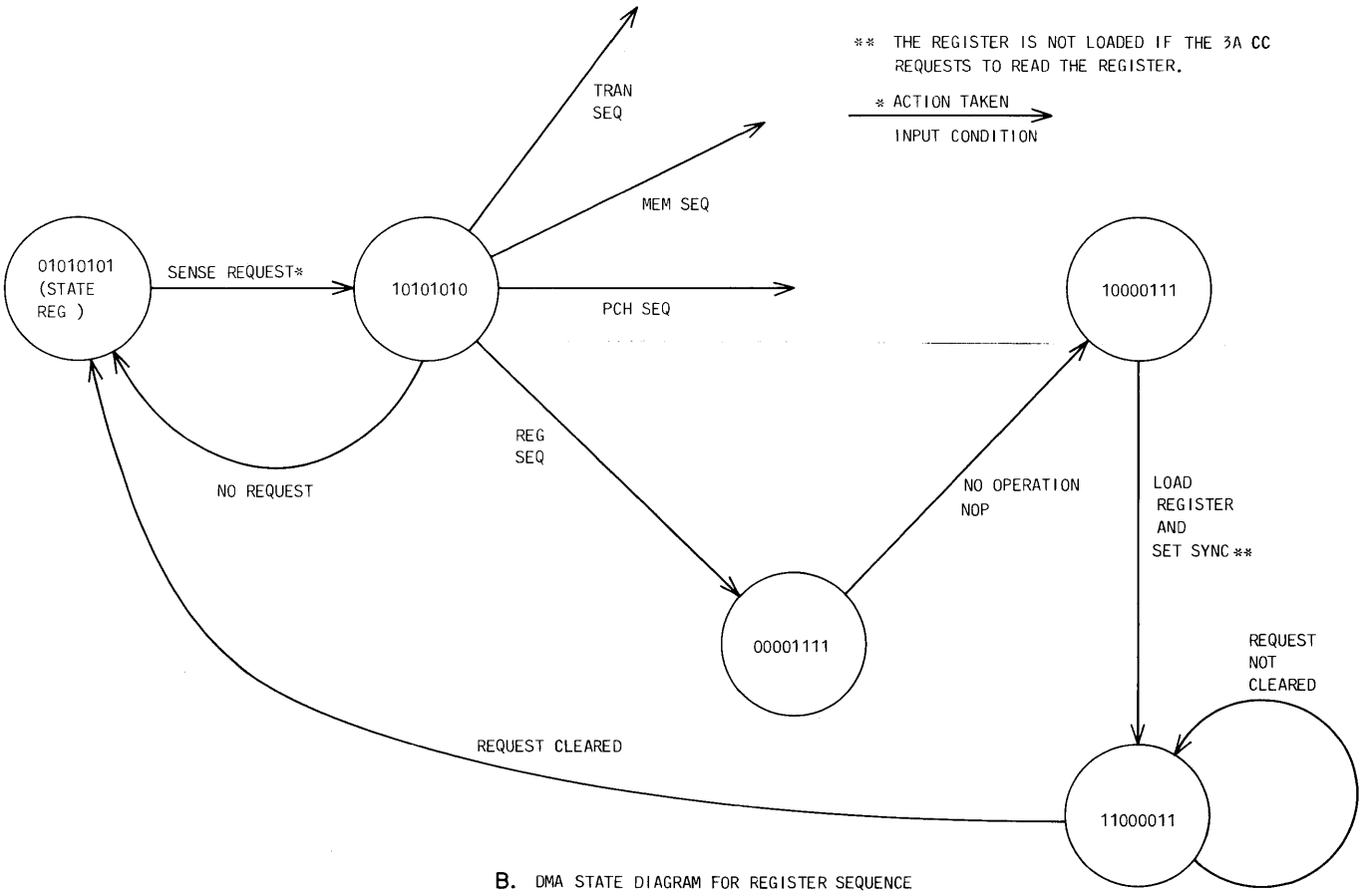


ADR - ADDRESS
ADROUT - ADDRESS OUTPUT
CTI - CDI TO TTL INTERFACE
DMAR - DMA REQUEST
DBS - DUPLEX BUS SELECTOR
DV - DEVICE
INFOUT - INFORMATION OUT
MD - 3A CC CROSSPOINT
PCH - PARALLEL CHANNEL
PCHENB - PCH ENABLE
RAM - RANDOM ACCESS MEMORY
RCVR - RECEIVER
REG - REGISTER
SBC - STORE BUS CONTROLLER
SEQ - SEQUENCE
SPCH - SUBPARALLEL CHANNEL

Fig. 13—DMA Functional Block Diagram



A. CC = MICROCONTROL STEPS FOR REGISTER SEQUENCE



B. DMA STATE DIAGRAM FOR REGISTER SEQUENCE

Fig. 14—DMA Register Sequences

Memory Sequence

3.46 The memory sequence either fetches a word from MAS to DTB register or stores DTB register contents in the MAS. The 3A CC register R9 bits 0 through 5 specify the device with the DTB register to be loaded. The DMA PAL and PAH registers point to the associated MAS location. The 3A CC microsequence is the same as the register seqence (Fig. 14). The DMA memory sequence for fetching a word from MAS is shown in Fig. 15. At the end of the memory cycle, the store bus controller circuit automatically loads data into the MDT register. Then the DMA sequencer moves data from MDT to DTB. To store DTB register contents in MAS, DTB register data is moved to the MDT register before starting the memory cycle. Data in MDT is not moved back to DTB after the memory cycle is complete.

PCH Sequence

3.47 The 3A CC must send a request to DMA to communicate with devices. When DMA recognizes the request, the PCH sequence is started. The 3A CC microsequence for accessing a device via PCH is shown in Fig. 16. First, the 3A CC generates a crosspoint signal (MD0,...,MD7). The crosspoint functions specify the control signal [DR, data present (DP), command present (CP), etc] that the 3A CC wants to send to the device. This information is latched into the PCH. The DMA maintains complete control of PCH after execution of this crosspoint signal. Then the 3A CC generates crosspoint signal MD3 (set 3A CC request), which sets the REQUEST flip-flop. After the DMA starts the PCH sequence, it sets the ENABLE flip-flop. The enable signal causes the PCH to send data and an address to the device; and 150 ns later, the control signal specified by the first crosspoint signal is sent. At this time, the PCH is controlled by the 3A CC (issues MD2 which clears the control signal). The last crosspoint signal, MD1 (clear 3A CC request), clears the REQUEST flip-flop, which signals the DMA to terminate the PCH sequence. The response signal (SNYC0) from the devices and the store complete (SCMP0) signal from FC392 are strobed into flip-flops by clock pulse, phase 1 (P10), on FC388 (Table F).

Priority Circuit

3.48 Circuit functions on the priority CP FC389 enforce priorities among requests from the 3A CC and various devices. Circuit design is such that 3A CC requests have priority over those of devices. When a 3A CC request and a device request are received simultaneously by the DMA, a signal (CCREQ0) is activated to cause the DMA to serve the 3A CC request first. Device requests received by the DMA in the absence of a 3A CC request cause a signal (DVREQ0) to be activated. The greater the address of a device, the higher its priority. Two priority encoding devices are used to generate the device address with the highest priority. The address for accessing the RAM and the device address are generated in FC389. If the CCREQ0 signal is not active, ie, the 3A CC is not making a request, the output of the priority encoders are used as the device address. If the CCREQ0 signal is active, bits 0 through 5 of 3A CC register R9 are used as the address. When the DMA is in the maintenance mode, the device address is forced to the DBS maintenance address 111100. Additional functions provided on FC389 include parity checking of RAM addresses and generation of PCH control signals. When the condition for inhibiting MAS access is detected, IHBMRY1 signal is activated. As the end of data (EOD) transfer is detected, TERMN0 signal is activated, or TRNSF0 signal is activated to indicate a normal data transfer.

Data Transfer

3.49 To start a data transfer, the 3A CC must properly set up DMA registers and initialize the device for the transfer. Then the device can request DMA to transfer one word via usage of the DMAR lead. This request causes the DMA priority circuit to generate the address of the requesting device. The address of the highest priority device will be generated and this device will be served first for simultaneous device requests. The DMA data transfer sequence is shown in Fig. 17. The sequence assumes that a word is present in DTB. Sending the present word to the device overlaps with fetching the next word from the MAS. The next word is transferred from MDT to DTB before the sequence is completed in preparation for the next transfer.

3.50 The transfer of data from the device to MAS is similar to the transfer of data from MAS to the device (Fig. 17) except that data movement is reversed. The DMA overlaps storing the present word in the MAS with fetching the next word from the device.

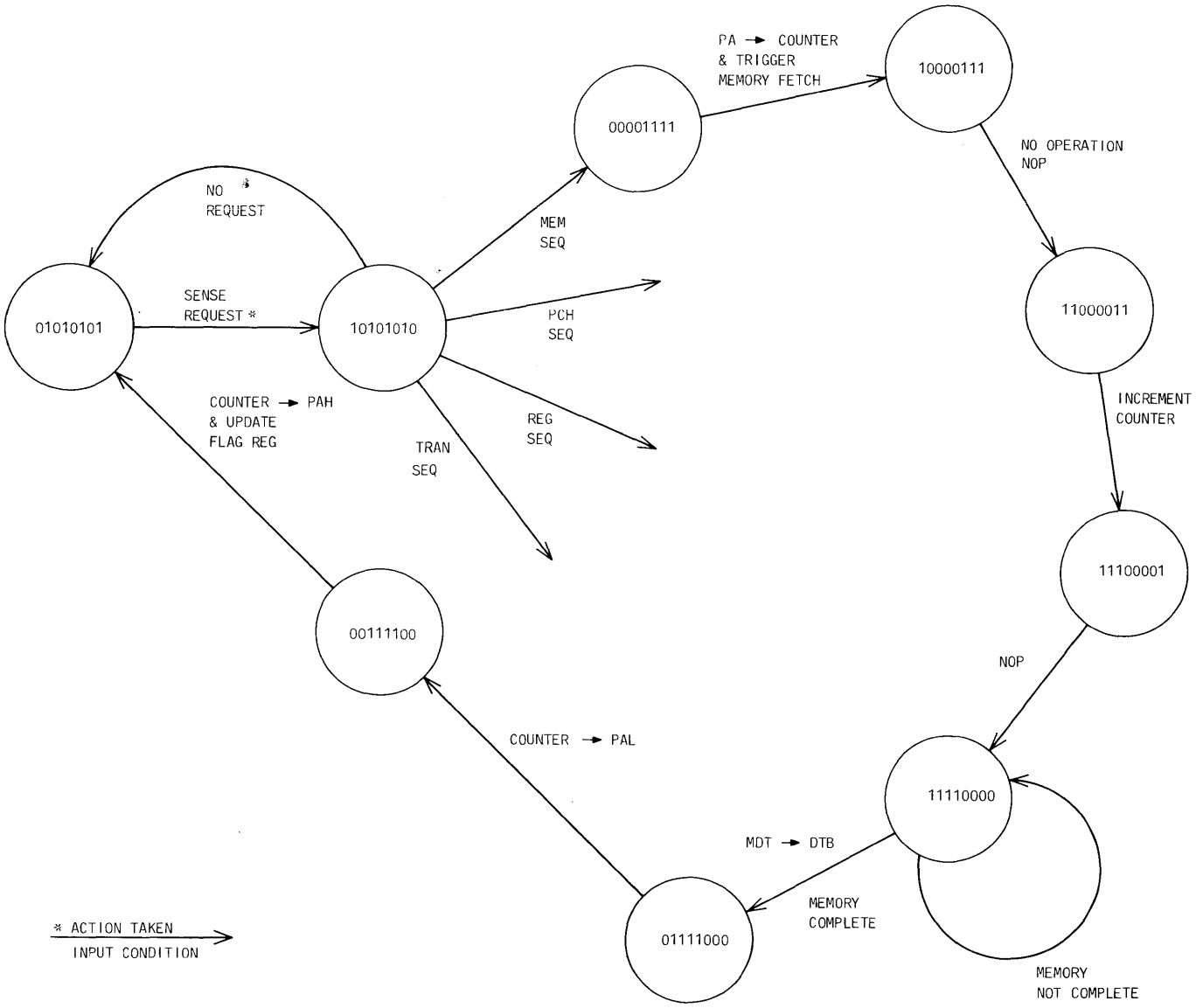


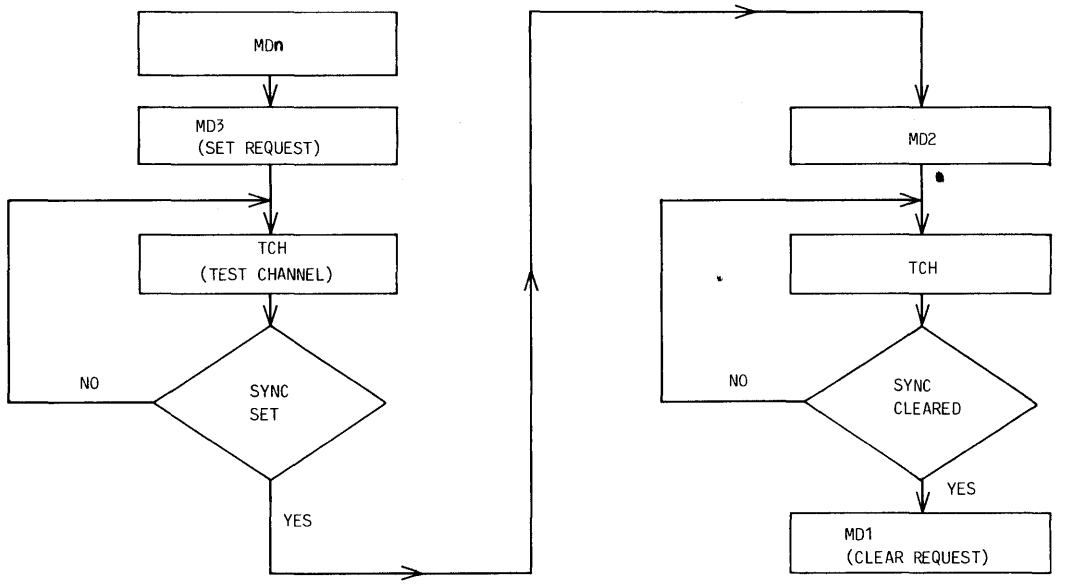
Fig. 15—DMA (State Register) Memory Sequence

3.51 When PA equals FA, the DMA will generate the EOD command. Also, an EOD command is sent to abort the current data transfer if errors are detected by the devices or MAS. When the device recognizes the EOD command, the 3A CC is interrupted to indicate termination of the data transfer.

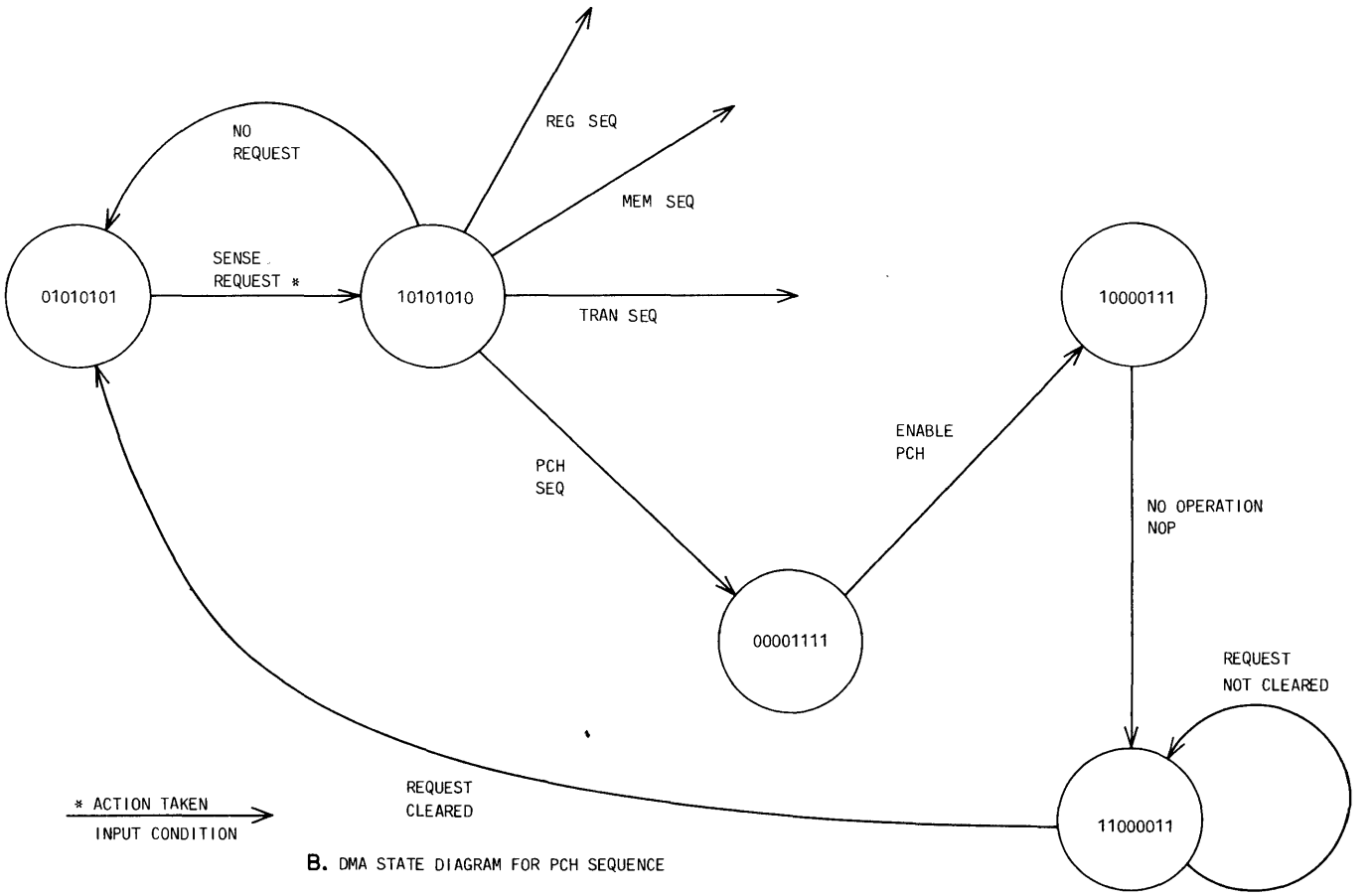
DMA Error Detection

3.52 Normally, the state register contains a 4-out-of-8 code. In each state of each sequence, a critical signal is identified. A 1-out-of-20 check ensures that only one of the critical signals is active during each cycle and the DMA is in a valid state.

3.53 To implement PA and FA, 16-word by 4-bit RAMs are used. The PA and FA registers are designed for 4 bits per circuit pack. Four parity bits cover multiple faults of a single device. Parities are checked during each word transfer. At the beginning of each word transfer, PA is compared with FA. If PA is greater than FA, an error bit in the DMA status register is set. Under normal conditions, after PA is incremented, the



A. 3A CC MICROCONTROL STEPS FOR PCH SEQUENCE



B. DMA STATE DIAGRAM FOR PCH SEQUENCE

Fig. 16—DMA PCH Sequences

TABLE F

3A CC/DMA MICROCONTROL CROSSPOINTS

MISC DECODER CROSSPOINT	CROSSPOINT FUNCTION (NOTE)
MD0	Reset DMA
MD1	Clear 3A CC request
MD2	Clear DMA state register
MD3	Set 3A CC request
MD4	Load DMA registers
MD5	Single-step DMA
MD6	Not used
MD7	Not used

Note: 3A CC general register R9, bits 10 through 15, must have correct DMA address before crosspoint functions can be activated.

new address is compared with the old address to ensure that PA is in the valid range.

3.54 Two parity bits are implemented to cover 16-bit data words. Signals to load MDT and DTB registers are checked to ensure these function once during each word transfer. Also, outputs of the two SBC circuits are compared and matched.

3.55 Validity of the DMAR signal from the device is checked by the address generated in the priority circuit. In addition, circuit redundancies are provided to detect whether PA equals FA. This ensures DMA detection of the end of transfer conditions.

3.56 The DMA request (DMAR) circuit pack, FC393, consists of 16 sets of transformers and receivers for receiving 16 DMA request signals. Input is received from DBSs via individual twisted pair leads (Fig. 18). Receivers are cleared by the RESET0 signal. Signal MTNDMAR1 forces the outputs of all receivers active (Table C).

Status

3.57 Status of DMA is provided by FC390 (status 1) and FC391 (status 2) circuit packs. These CPs receive desired inputs from the 3A CC devices and internal DMA circuits to generate status. Bits of the control registers are also on these CPs. Functions of each bit of status and control registers contained in FC390 and FC391 are given in Table D.

3.58 Circuit pack FC390 (status 1) contains bits 8 through 15 of status and control registers (Tables C and D). All bits of these registers, with the exception of bit 9 of the status register, can be loaded from 3A CC register R10 and gated back to 3A CC register R11. Bit 9 of the status register can be gated back to R11 but not loaded from R10. Functionally, when MTN1 and OLCK1 of the control register are both set, device error is forced for diagnostic purposes. When MTN1 and MLCK1 of the control register are both set, data gating error is forced for diagnostic purposes. Device errors and MAS errors are checked and latched into flip-flop on this CP.

3.59 Circuit pack FC391, status 2, contains bits 4 through 7 of status and control registers. All bits of these registers, except bits 6 and 7 of the control register, can be gated back to 3A CC register R11 but not loaded by the 3A CC. Bits 6 and 7 of the control register can be loaded from 3A CC register R10. To check control signals from FC387, a 1-out-of-20 checker is used to ensure integrity of the state register. When an error is detected, the checker is forced to an error state independent of the inputs to the checker. This checker error is reported as state error. The checker circuit is reset by signal RESET0. Bit 5 of the status register (DMA error) is the sum of all other error bits in the status register.

3.60 When DMA detects an error, a hold clock (HLDCLK1) signal inhibits the clock causing the state register to cease rotation. Signal HLDCLK1 also is used when DMA is in the single-step mode. For this mode, the check is enabled for one cycle each time that crosspoint MD5 is executed. Signals to load the memory data register (LMDT0) and the data buffer registers (LDTB0) are checked in this CP to assure that each of these registers is activated once during each word transfer. An error detected by this checker is reported as a data gating error.

3.61 When 3A CC register R9 contains the DMA address 010101 in bits 10 through 15, DMA enable (DMAEN0) signal is activated, which enables

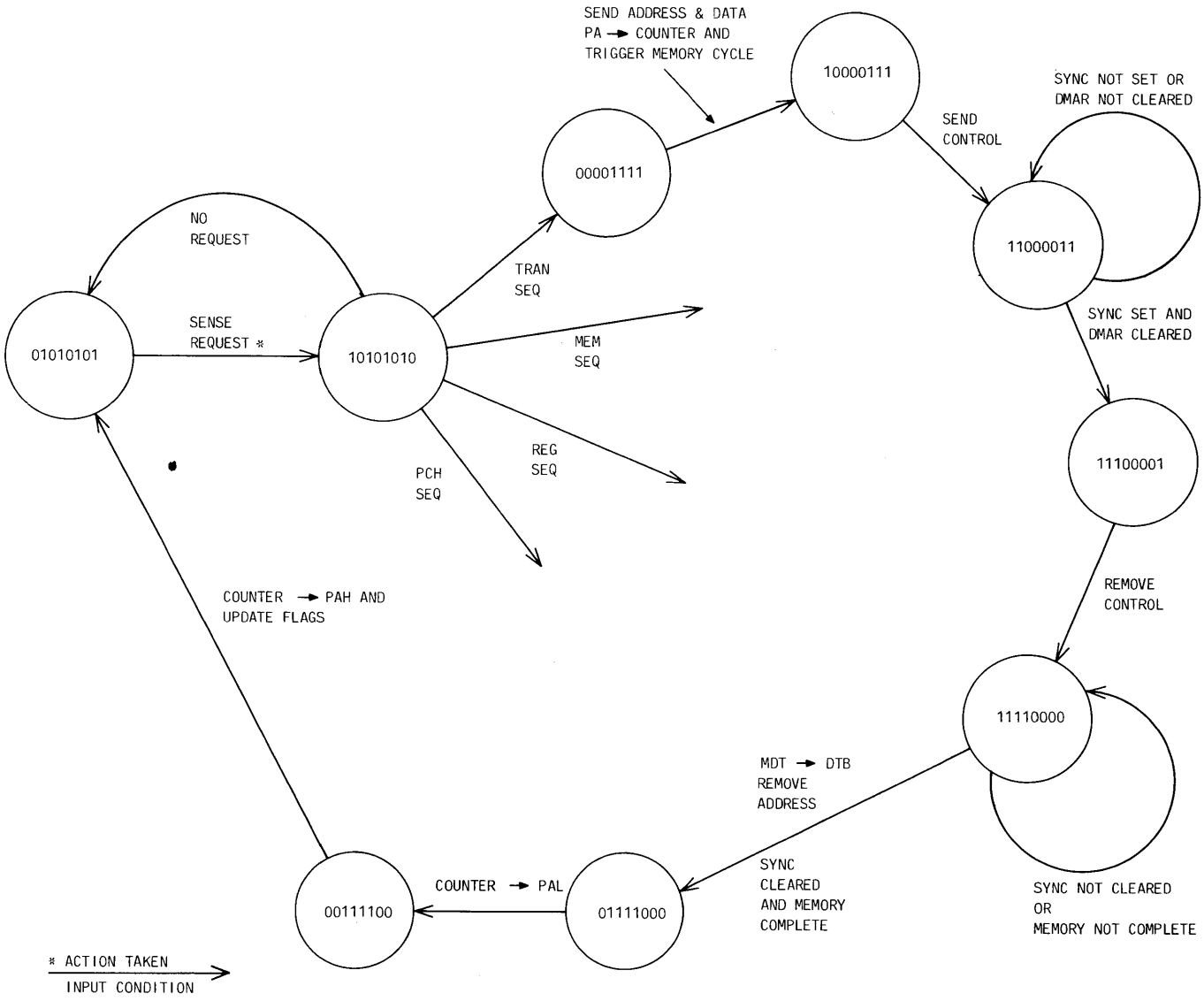


Fig. 17—DMA Data Transfer Sequence

the DMA to respond to crosspoint signals (Table F). The SPCH address is also generated on this CP. Bits 6 through 9 of 3A CC register R9 are used as the SPCH address when signal CCREQ0 is a logic zero. Outputs of the parameter register are used as SPCH address when CCREQ0 is a logic one.

E. Maintenance

3.62 Various maintenance states of the DMA are made available by setting different bits in the control register (Table C). The SYNC0 signal from the PCH and the store complete (STCOMP0) signal from the store bus control circuits can be read back to 3A CC register R11 for verification as bits 4 and 5 of the control register.

3.63 The DMA is put into the single-step mode; ie, the DMA state register is not advanced when bit 6 of the control register is set. In this mode, the DMA state register is advanced one step each time SDMA instruction is executed. This

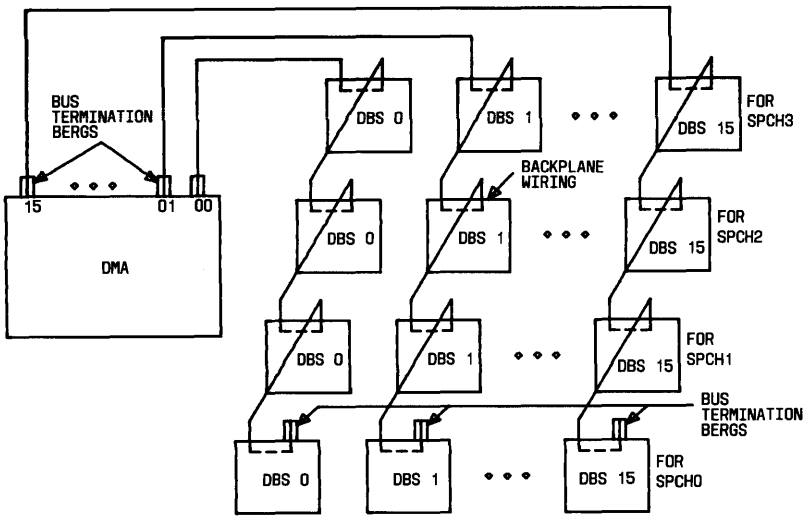


Fig. 18—DMAR Lead Interconnections

mode provides the capability of examining internal circuitry of the DMA while it is in different states.

3.64 In order to prevent the off-line DMA from interfering with the on-line 3A CC, the DMA is inhibited from using the store buses if the 3A CC flip-flop in the system status register is not set (ie, 3A CC is off-line). However, this inhibit function can be overridden by bit 7 of the control register while the off-line DMA is being diagnosed.

3.65 The DMA is in the PCH mode when bit 8 of the control register is set. In this mode, DMA state register is not cycling, and PCH is constantly under 3A CC control. This mode allows PCH diagnostics to diagnose the PCH in the DMA without interference from DMA sequence.

3.66 The DMA can be placed in the maintenance mode by setting bit 9 of the control register. All DMAR receivers are forced active in this mode. The mask register can be used then to simulate requests from various devices for diagnostic purposes.

3.67 Bits 10 and 11 of the control register are used to individually inhibit the two paths of the comparator logic, which detects that PA equals FA, in order to diagnose each path separately.

3.68 The store will complement-correct a word with double parity errors when bit 12 of the control register is set. Complement correction is controlled by 3A CC.

3.69 Bits 13 and 14 are used to force various error conditions as described in Table C.

3.70 To prevent the off-line 3A CC or DMA from altering the on-line store, bit 15 of the control register can be set to block all store bus signals from the off-line 3A CC.

3.71 When a stop and switch or maintenance reset function (MRF) occurs, DMA should be reset to ensure that it is not in a state which prevents system recovery. Therefore, DMA monitors the STOP flip-flop of the 3A CC and generates an internal reset pulse when the flip-flop is set. In case of an MRF, CC initialization microcode will reset all I/O channels including DMA.

3.72 Maintenance features for PCH (MPCH and SPCH) associated with the DMA are discussed in Section 4 of this document.

4. PARALLEL CHANNEL UNIT

INTRODUCTION

4.01 The PCH unit provides a high-speed data link between the 3A CC and peripheral devices that require a parallel channel interface for data transfer. The association between the parallel channel and other equipment is shown in Fig. 19. A more detailed interface between the PCH unit, 3A CC, and device is shown in Fig. 20. The interface to the 3A CC is via the collector diffusion isolation (CDI) logic to transistor-transistor logic (TTL) interface unit (CTI/power unit). The primary purpose of the CTI/power unit is to convert 3A CC CDI logic level voltages (+3 volts and 0 volt) to TTL logic level voltages (+5 volts and 0 volt). Additionally, the CTI/power unit provides operational power to the DMA and PCH units, fuses all such power, sequences power to the bus drivers, and provides an alarm interface to frame power units. All devices interface with the parallel bus via a duplex bus selector (DBS). The input/output of the duplex bus selector is switched so that a device may be operated by either of the duplicated 3A CCs. The DBS is analogous to a multipole double throw switch, thereby allowing only one 3A CC at a time to communicate with the device. The DBS also provides several maintenance and reliability features to protect the 3A CC against devices that fail to operate properly. The PCH unit incorporates interrupt lines and provides a hardware interrupt vectoring arrangement. These interrupt lines are connected directly to the 3A CC.

4.02 Data communication between peripheral devices and the PCH unit via DBSs is accomplished via a 35-lead parallel bus that utilizes:

- An 18-bit data field
- A 6-bit peripheral device address field
- A 6-bit command field
- A 4-bit response field
- A 1.67-MHz clock signal.

4.03 The PCH unit is composed of two functional modules: main parallel channel (MPCH) and subparallel channels (SPCH).

4.04 The MPCH provides the interface between the 3A CC and a maximum of eight SPCH circuits (Fig. 21). It interfaces directly to the CTI/power unit via an 82-lead parallel bus (tape cable).

4.05 The SPCH functions as a transmitter/receiver between the MPCH and a transformer-coupled ac parallel bus. Each SPCH controls a dedicated parallel bus that can service up to 16 peripheral devices per bus via DBS units. Thus, a single MPCH can service a maximum of eight SPCHs, providing a capacity of 128 peripheral devices per MPCH. The ac parallel bus from the SPCH to the DBS is used to transmit bipolar pulses (Fig. 22). Pulses generated by the SPCH are 150 nanoseconds wide. Positive voltage is used to indicate a logic one, and negative voltage is used to indicate a logic zero. The transmission medium consists of 35 balanced twisted-pair lines bundled together in a common sheath.

A. Physical Description

4.06 The PCH unit consists of circuit packs located in the upper part of the processor frame. A front-removable 4-inch mounting plate and three 14-card apparatus housings (type 80C) are used. A basic PCH unit is equipped with one set (four) of MPCH circuit packs and one set (three) of SPCH circuit packs (Fig. 23). Additional SPCHs (each SPCH consists of three circuit packs) are added, as required, to provide additional capacity for each application. A fully loaded PCH unit contains circuit packs for one MPCH and eight SPCHs. When more than one MPCH is required, a second PCH unit can be mounted directly above the first unit in the processor frame. Interconnection between the two PCH units and the CTI/power unit is accomplished via tape cable and 942-type connectors. This provides a maximum parallel channel capability for controlling a total of 256 peripheral devices (128 per PCH).

4.07 The circuit packs are all FC type packs [two power and four signal layers (Fig. 5)]. Table B provides a summary of circuit pack types and functions in the PCH unit. Each circuit pack uses an 80-pin 946C connector and has power and ground distributed on the outer two layers with signal interconnections distributed on internal layers (maximum of four signal layers).

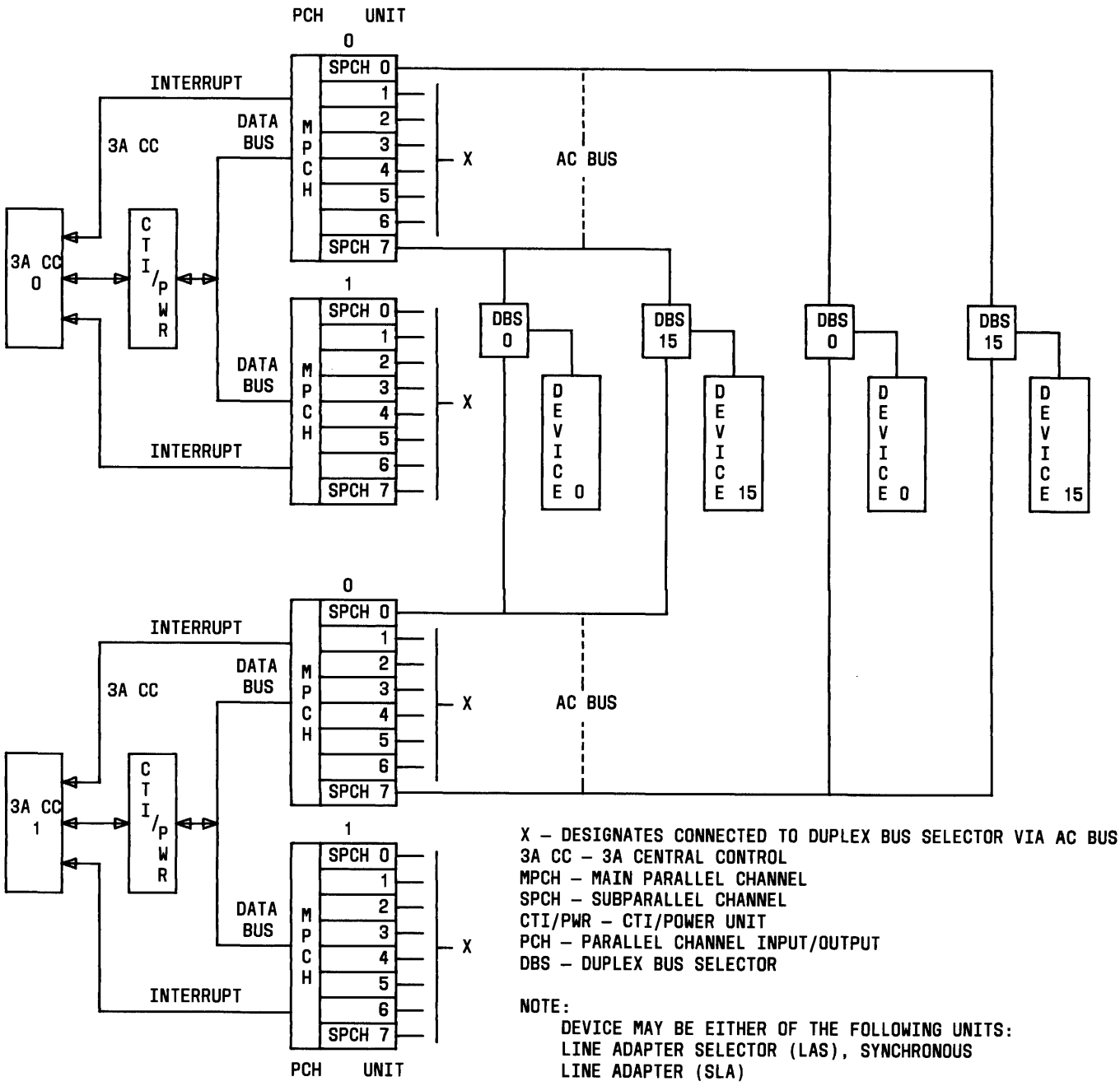


Fig. 19—Parallel Channel Unit Interfaces

B. Interfaces

4.08 The PCH unit interfaces with the 3A CC via the CTI/power unit and with peripheral devices via DBS (Fig. 20). The PCH unit interfaces with the CTI/power unit via an 82-lead parallel bus and with the duplex bus selector via a 35-lead ac parallel bus.

4.09 The 35-lead ac bus contains pairs of leads that are bidirectional (the 18 INF and associated parity leads are bidirectional; all other leads are unidirectional). This is accomplished by the use of transformer coupling between the SPCH and the bus, also between the bus and the periphery. One set of windings is used to transmit signals, and another set of windings is used for receiving signals.

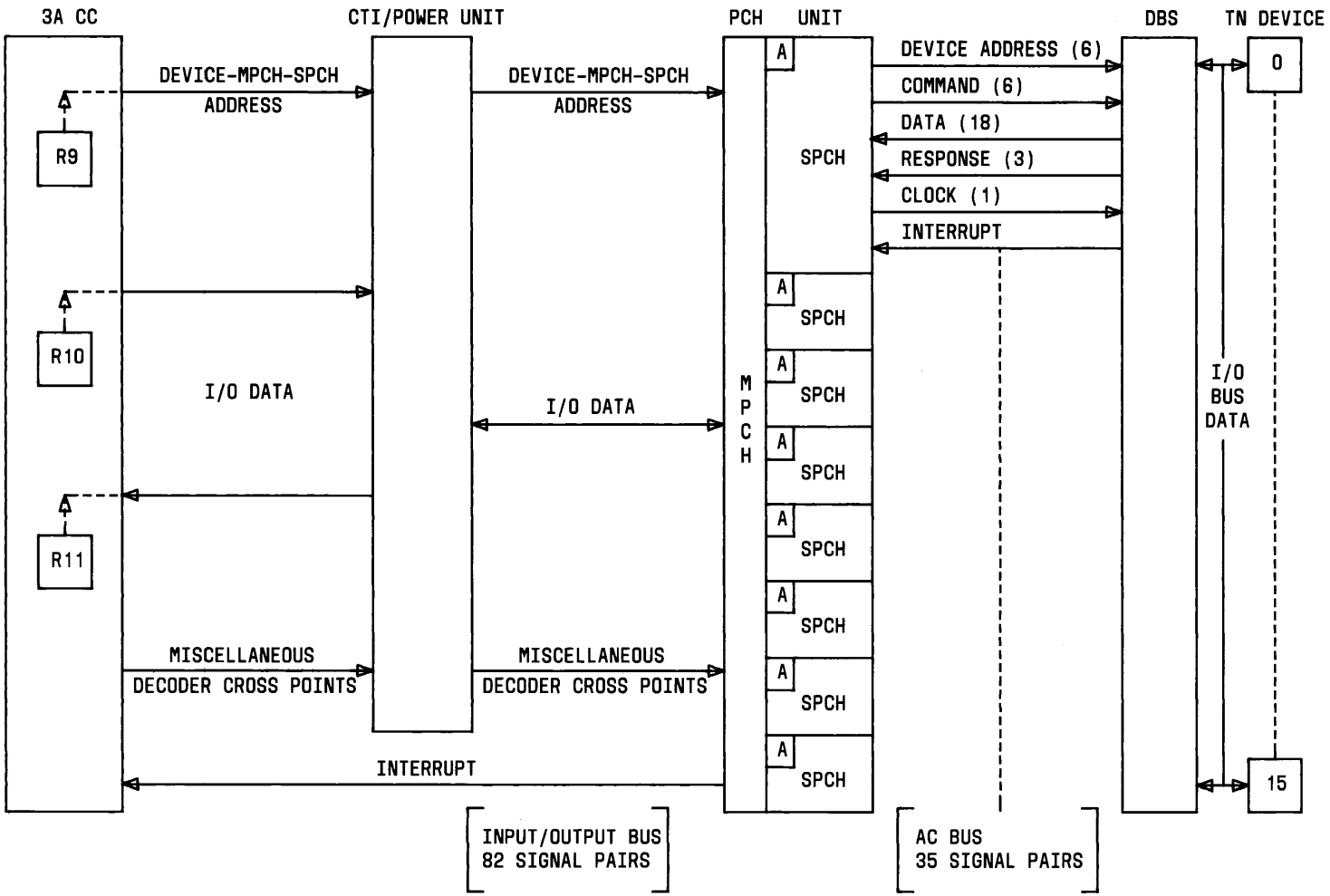


Fig. 20—Detailed PCH Unit Interface

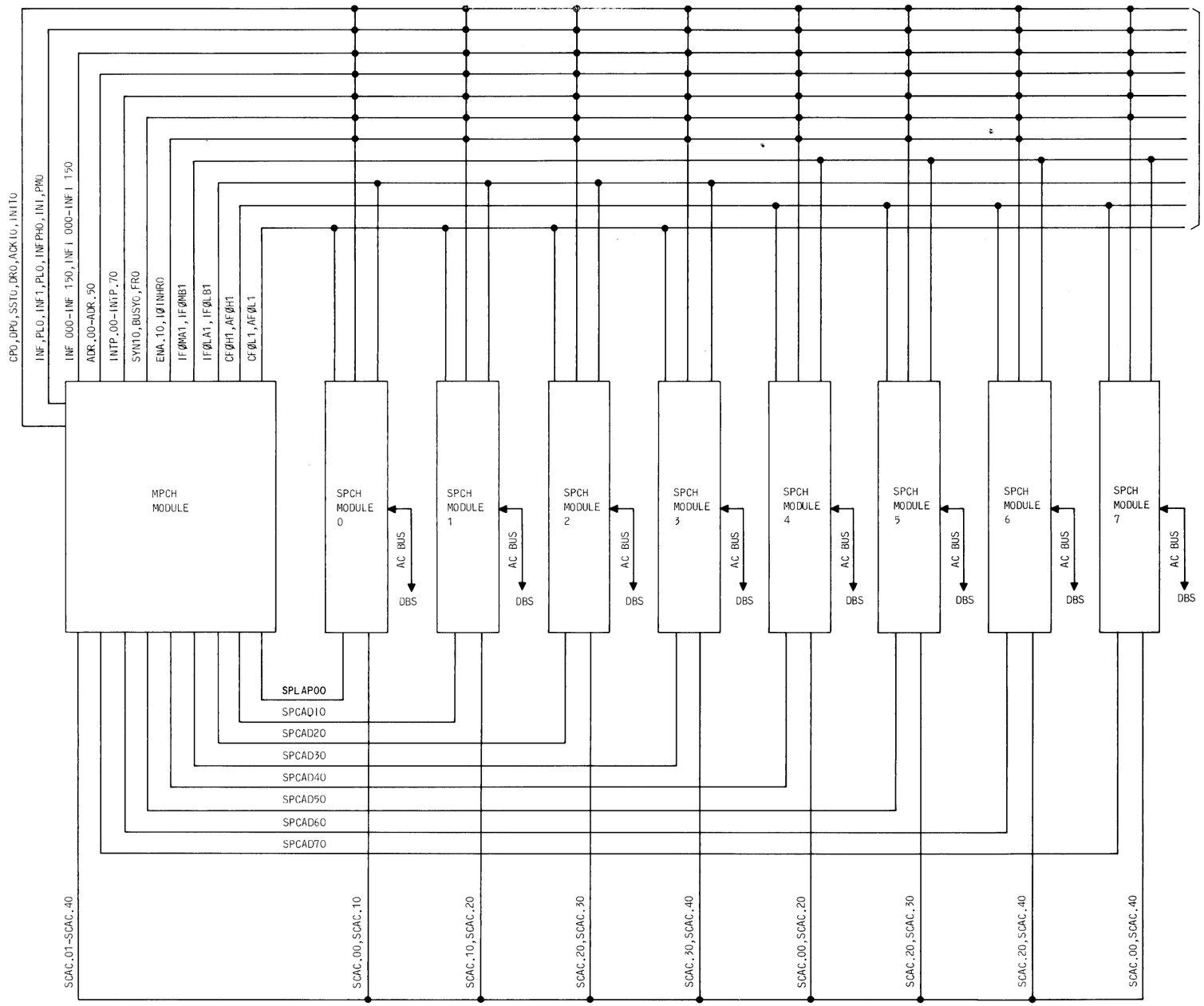


Fig. 21—MPCH-SPCH Interface

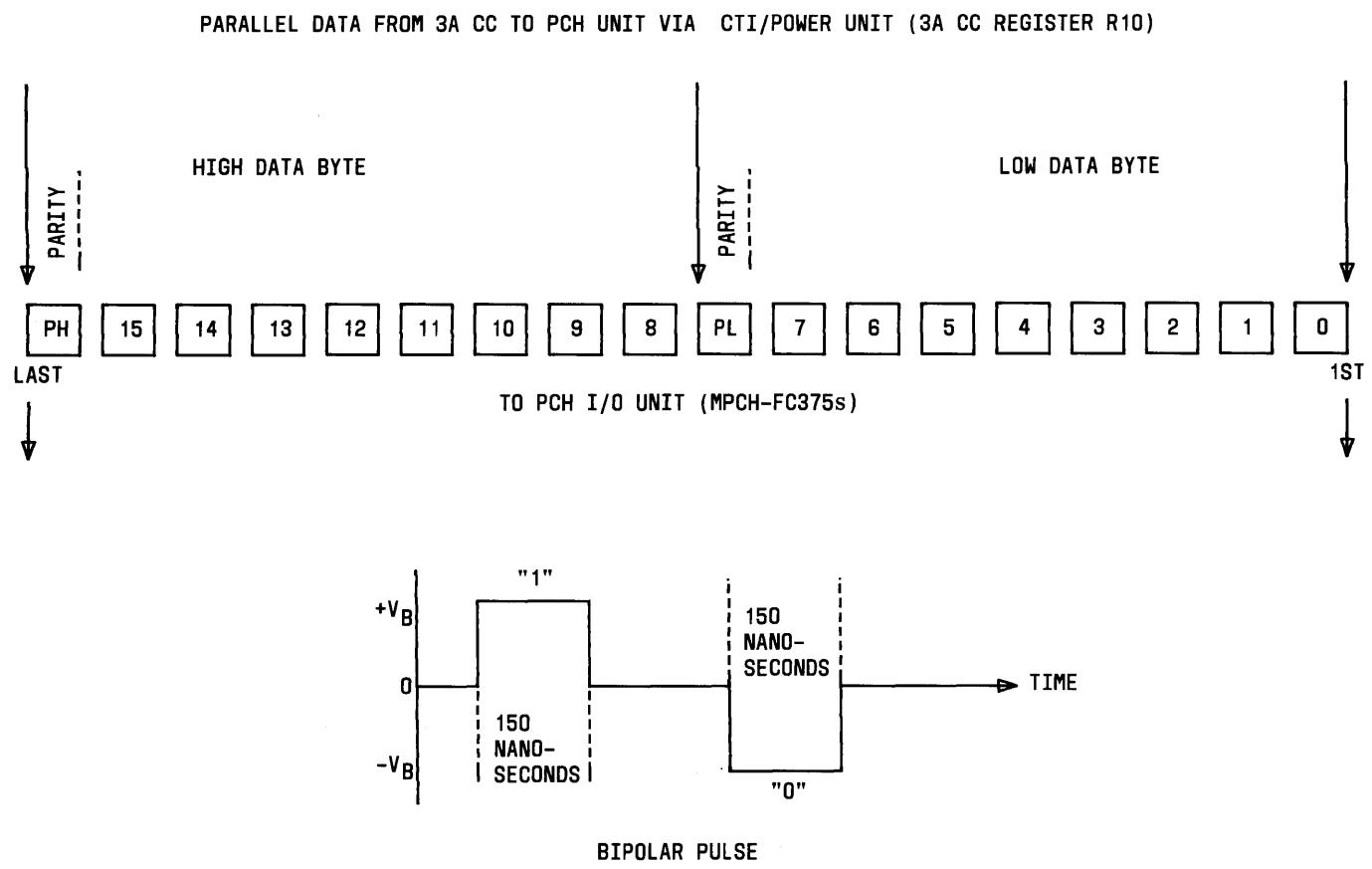


Fig. 22—Bipolar Pulses (Data Bytes)

C. Functional Description

Introduction

4.10 The PCH unit is composed of two functional modules: MPCH (one per PCH unit) and SPCH (maximum of eight per PCH unit).

Main Parallel Channel

4.11 The MPCH (Fig. 24) consists of the following functional subunits:

- Address circuit—FC374 (one)
- Information circuit—FC375 (two)
- Control circuit—FC373 (one).

Address Circuit

4.12 The address circuit (FC374) decodes main channel select (MCS) and subchannel select (SCS) codes on the parallel bus from 3A CC register R9. If the MCS code matches the address of the MPCH, this circuit returns a 3-out-of-6 code to the 3A CC indicating that the FC374 has been selected, generates an internal activation signal to be used in other MPCH circuits, and decodes the subchannel select code. The circuit also sends an enable command to the selected subchannel. If the main channel select code does not match the address of the MPCH, no action is taken.

Information Circuit

4.13 The information circuit (FC375) is composed of two identical FC375 circuit packs. Each pack interfaces a data byte (8 bits plus parity) between the 3A CC and the particular subchannel selected. Each circuit pack incorporates a mode

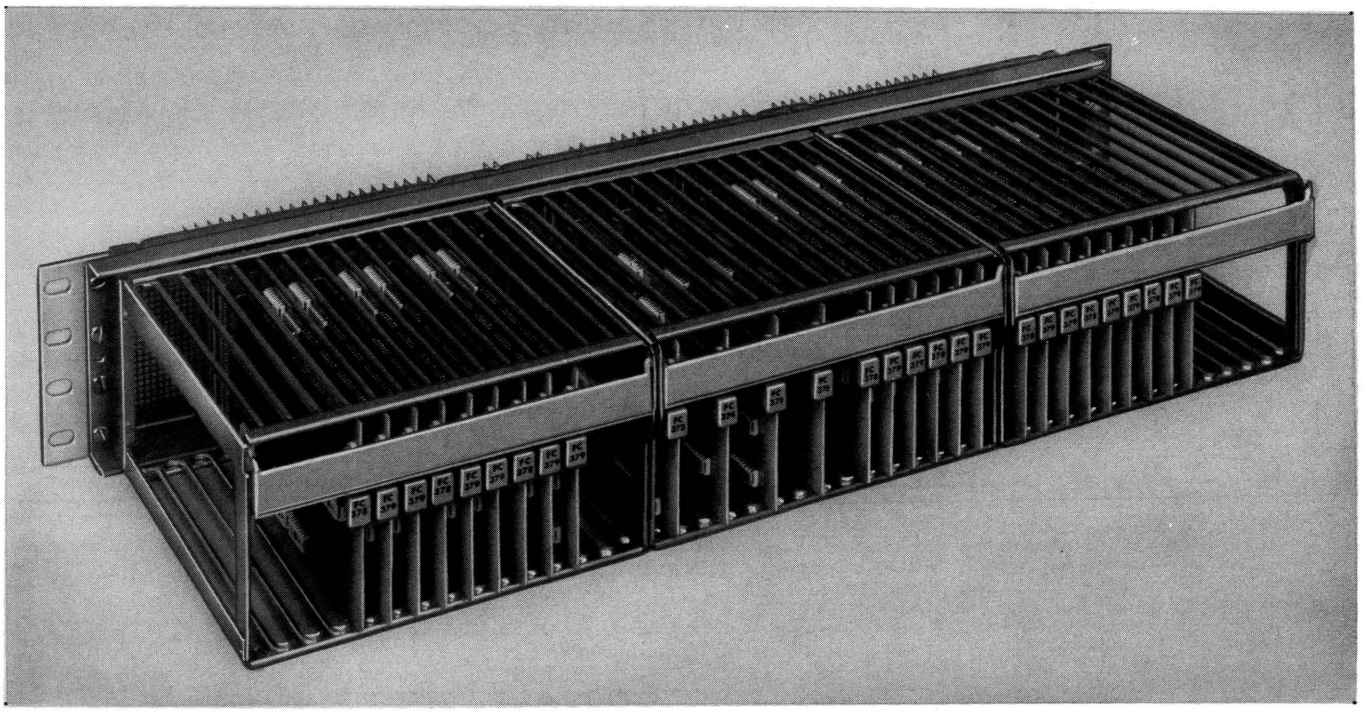


Fig. 23—Parallel Channel Unit

control circuit which may be stimulated to effect a report of the MPCH internal state to the 3A CC via general register R11. Control information is received from the MPCH control circuit pack defining the direction for data to proceed (ie, to the device on a write command or to the 3A CC on a read command) and whether the circuits should pass data or return status information.

Control Circuit

4.14 The control circuit (FC373) provides necessary control signals to other MPCH circuits and sends the proper device command code (via SPCH circuits) to identify the type of operation desired. This circuit contains a 7-bit state register with bits that are set under microprogram control via activation of prescribed miscellaneous decoder crosspoints in the 3A CC. Control information to this circuit originates from the 3A CC (miscellaneous decoder crosspoint) or from the direct memory access (DMA) unit.

Subparallel Channel

4.15 The SPCH (Fig. 25) serves as a transmitter/receiver and interfaces the MPCH unit with a transformer-coupled ac parallel bus. This ac parallel bus provides signal paths between the PCH unit with the dedicated peripheral devices via the duplex bus selector. The SPCH is composed of the following functional modules:

- Control/address circuit—FC378 (one)
- Information circuit—FC379 (two).

Control/Address Circuit

4.16 The control/address circuit (FC378) provides the interface for the parallel bus device address, control, clock, and response leads. This circuit returns a 2-out-of-5 check code to the MPCH when it is selected.

Information Circuit

4.17 The information circuit, consisting of two FC379 circuit packs, interfaces information data (16 data bits and 2 parity bits) between the MPCH and the ac parallel bus. It also provides an internal loop-around register for checking the integrity of the data path as desired.

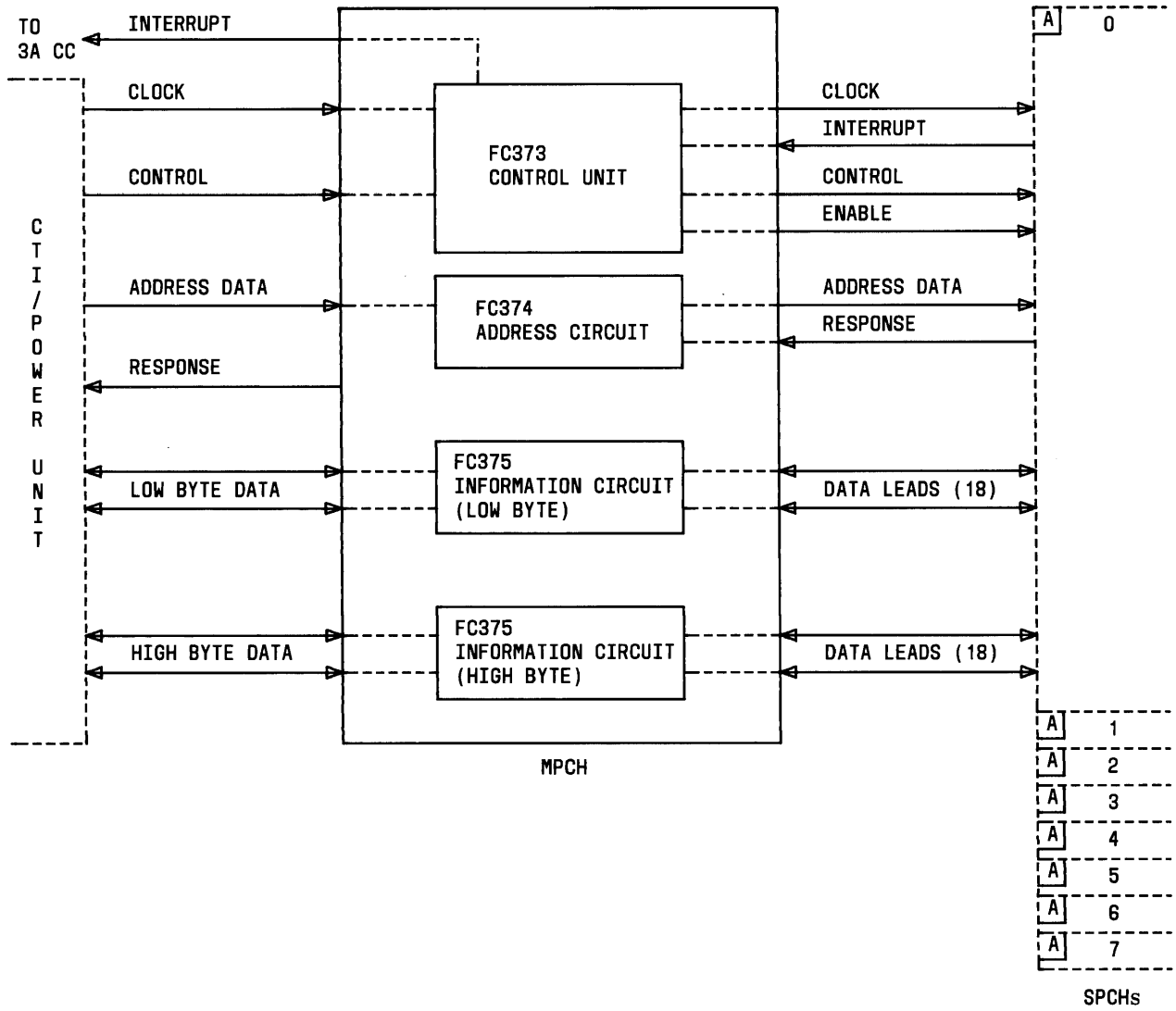


Fig. 24—Main Parallel Channel

D. Theory of Operation

Introduction

4.18 The PCH unit supplies a high-speed data link between the 3A CC and peripheral devices that need parallel inputs and outputs for operation. Communication between the 3A CC (via CTI/power unit and PCH unit) and the duplex bus selector is fast enough so that once a message is sent to the peripheral device the 3A CC waits for a reply before proceeding to other functions.

Communication Between the 3A CC and the PCH Unit

4.19 Communication between the 3A CC and PCH units is performed by three 16-bit general registers (3A CC registers R9, R10, and R11) and eight miscellaneous decoder (MD) crosspoints generated by the 3A CC. Register R9 contains the MPCH, SPCH, and device addresses. Register R10 is the data register and supplies data needed by the addressed peripheral device. Register R11 is used as a data storage register for incoming data from the peripheral device or status information from the MPCH. Miscellaneous crosspoints provide

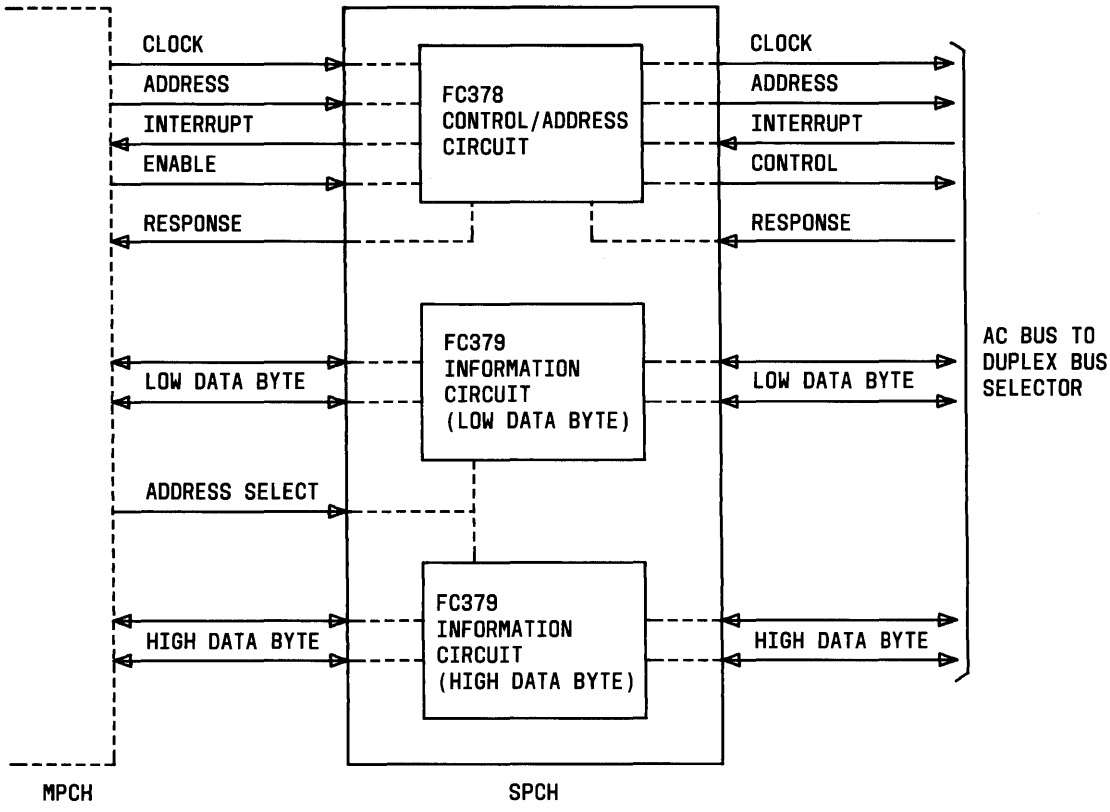


Fig. 25—Subparallel Channel

the PCH unit MPCH with control sequencing information.

4.20 The MPCH receives information from 3A CC register R9 as follows:

- ***R9 Bits 15 Through 10:*** This is the main input/output select field and must match the designated code of the MPCH (6 bits) to enable the MPCH (3-out-of-6 code).
- ***R9 Bits 9 Through 6:*** This is the SPCH field which is used to select the desired SPCH (3-bit binary plus odd parity bit).
- ***R9 Bits 5 Through 0:*** This is the peripheral device field. These bits are sent to peripheral devices (via MPCH and SPCH) and are used to select the desired peripheral device.

4.21 Register R10 bits 15 through 0 contain the data necessary for the peripheral device operation. This data is transmitted to the peripheral device via the MPCH, SPCH, and duplex bus selector.

4.22 Register R11 is used by the 3A CC to contain and store the data from the peripheral device (via SPCH and MPCH) or the status report (internal state) of the MPCH.

4.23 The control sequence of the MPCH is developed from the input signals from the 3A CC over eight miscellaneous decoder crosspoints, which are listed below. The input/output instructions activate a fixed sequence of crosspoints, or special maintenance sequences may be applied to the MPCH for diagnostics.

MISCELLANEOUS DECODER (MD) CROSSPOINT	CROSSPOINT FUNCTION
MD7	Command present (CP)
MD6	Data present (DP)

MD5	Data request (DR)
MD4	Sense status (SST)
MD3	Acknowledge interrupt (ACKI) if first crosspoint in a normal sequence; transmit command otherwise
MD2	Initialize periphery (IP) if first crosspoint in a normal sequence; clear command otherwise
MD1	Clear address—data lines go to idle state
MD0	Set MPCH in maintenance state.

Note: After the first MD_ is sent, it is normally followed by MD3, then MD2, and then MD1.

4.24 When the PCH unit is activated by the 3A CC, the MPCH checks message integrity, returns a response code to the 3A CC, and waits for crosspoint information used to instruct desired action. One of six possible crosspoints (MD2 through MD7) is then issued to MPCH. A 1-out-of-6 code is stored in the 7-bit state register (MPCH FC373) indicating the function to be performed (read data, write data, send device command, sense device status, identify interrupting device, or initialize duplex bus selectors). At the same time, the MPCH determines when data is to be transmitted to the devices, transmits data when required, and transmits device address. (Transmission to the device is via the selected SPCH.)

4.25 Miscellaneous decoder crosspoint MD3 is then issued by the 3A CC, causing the MPCH to interrogate the 7-bit state register (FC373) and transmit proper command signals to the device via the selected SPCH. Response signals from the selected peripheral device are relayed to the 3A CC via the SPCH and the MPCH.

4.26 After processing the peripheral device response, the 3A CC issues miscellaneous decoder crosspoint MD2. This crosspoint instructs to clear all command line signals via the selected SPCH. Peripheral device responses are evaluated by the 3A CC. When the transaction is complete, miscellaneous decoder crosspoint MD1 is issued to the MPCH. Crosspoint MD1 instructs to clear all parallel channel bus address and data lines. (These lines receive zeros from the PCH unit to place them in the clear state.) The MPCH then goes into an idle state.

4.27 Special crosspoint sequences may be issued for maintenance control. Miscellaneous crosspoint MD0 is used to set the maintenance state. In this state, selected circuits may be exercised without causing improper transmission on SPCHs. Also, in the maintenance state, certain improper data may be sent to the duplex bus selector and peripheral devices for diagnostic purposes.

AC Parallel Bus Interface

4.28 The ac parallel bus interface is used to connect the duplex bus selector (connected to the peripheral device) to the PCH unit. The parallel bus interface consists of 35 leads: 6 address leads, 18 information leads, 6 control leads, 4 response leads, and a clock lead.

4.29 Six address leads are used to select the desired peripheral device. Five address leads (ADR0 through ADR4) select the desired peripheral device; the sixth lead (ADR5) provides for odd parity over the five address leads.

4.30 Eighteen bidirectional information leads are used to transmit data and commands to peripheral devices and receive data and status from peripheral devices. The leads are broken down into two groups of nine each: leads INF 0 through INF 7 with INF P_L as the parity low lead and INF 8 through INF 15 with INF P_H as the parity high lead. Each group corresponds to a data byte (8 bits plus parity): INF 0 through INF 7 plus INF P_L are the low data byte, and INF 8 through INF 15 plus INF P_H are the high parity byte.

4.31 Five of the six command leads send control signals to peripheral devices to indicate that address and information data signals are valid. Control leads are: command present, data present, data request, sense status, and acknowledge interrupt.

(a) ***Command Present (CP):*** The peripheral device selected by the address is signaled that a command is present on the information leads when CP is set to logic one. The information leads contain a coded command, and

only the selected peripheral device should respond to this command.

(b) ***Data Present (DP):*** When set to logic one, the peripheral device selected by the address is instructed that data is present on the information leads.

(c) ***Data Request (DR):*** When set to logic one, the peripheral device selected by the address is requested to gate data onto the information leads.

(d) ***Sense Status (SST):*** When set to logic one, the peripheral device selected by the address is requested to gate the contents of its status register onto the high ten information leads (INF 15 through INF 6) and its address onto the low six information leads (INF 0 through INF 5). Proper parity (INF PL and PH) is normally generated by the peripheral device. The sense status command must be accepted and responded to by the addressed peripheral device even when it is busy.

(e) ***Acknowledge Interrupt (ACKI):*** This lead is used to identify the peripheral devices requesting interrupts. When ACKI is set to logic one, each peripheral device requesting an interrupt sets a predefined bit on the information bus to logic one and all other peripheral devices set their assigned bits to logic zero. The 3A CC can then identify the devices requesting interrupts by testing the INF leads for logic ones. All peripheral devices respond to the acknowledge interrupt without regard to the address leads.

A sixth control lead, INIT, is connected between each SPCH and associated DBSs. When this lead is set to one, registers within the DBSs are set to a predefined state. This signal is not transmitted to the device by the DBS.

4.32 Four response leads carry peripheral device responses to the 3A CC. The response leads are: synchronization, not busy, error, and interrupt. While the interrupt lead may be set by the peripheral device at any time, the not busy synchronization, and error leads are set only when a peripheral device has been selected by the address leads.

(a) ***Synchronization (SYNC):*** After a control signal has been issued by the 3A CC and received by the peripheral device, the peripheral device sets SYNC to logic one. This indicates that the control signal has been understood, that all peripheral device check circuits have settled, and that information has been gated to/from the information leads. If the peripheral device is not ready, SYNC will be held to zero until the peripheral device has properly responded. Control and information signals are held steady until the peripheral device has properly responded to the control signal by setting SYNC to one. SYNC is released by the peripheral device setting it to zero when all the control signals are set to zero.

(b) ***Not Busy (NOTBSY):*** This lead is used by the peripheral device to inform the 3A CC of its readness to read or write data.

(c) ***Error (ER):*** This lead is set to one (at or before the time that SYNC is set) when the peripheral device selected by the address leads has discovered an abnormal condition.

(d) ***Interrupt (INT):*** This lead is set to one when any peripheral device serviced by the parallel bus desires to interrupt the 3A CC. Interrupt should be reset to zero by a special command present command, not by the acknowledge interrupt command.

4.33 An interrupt initiated by the peripheral device is transmitted from the device via the PCH unit (FC378 SPCH) to the 3A CC. At the 3A CC, the interrupt signal is gated into the interrupt status (IS) register. The 3A CC then issues an acknowledge interrupt signal (to identify the device requesting the interrupt) to the SPCH (assigned to the device requesting interrupt) via the MPCH. The device is then identified via inputs on the information leads. Appropriate 3A CC operations service the peripheral device requests.

4.34 The clock lead supplies a 1.67-MHz square wave to the peripheral devices via the PCH unit. This 1.67-MHz clock is always present and can be used by peripheral devices for internal timing.

Parallel Bus Interface Timing

4.35 Signals transmitted on the parallel bus interface are bipolar pulses. These pulses are 150 nanoseconds wide and use positive voltage to indicate a one and negative voltage to indicate a zero. Address and data information signals (if provided) are sent at the same time, with command signals sent following a 200-nanosecond delay. After peripheral device response plus a delay of up to 750 nanoseconds, all command signals are cleared to zero. Peripheral device acknowledgment is checked with a possible delay (maximum of 750 nanoseconds), and all address and data information signals are cleared to zero. The minimum input/output transaction execution time is 2.7 microseconds, as shown in the following timing table.

TIMING TABLE

150 ns	Decoding
150 ns	Set Up ADDRESS/DATA Information
150 ns	Nonoperation (NOP) (Provides Needed Delay)
150 ns	Transmit Command
1050 ns	Wait for SYNC
150 ns	Clear Command
1200 ns	Test for Error/Wait for Clear
150 ns	Test for Error
150 ns	Clear Address.

Execution time may be greater depending on peripheral device response delay up to a 10-microsecond time-out implemented by 3A CC microcode. Parallel bus timing intervals are shown in Fig. 25.

Main Parallel Channel

4.36 An MPCH contains four circuit packs: one FC373 control pack, one FC374 address pack, and two FC375 information packs (Fig. 26).

4.37 These circuit packs perform the following functions:

(a) ***FC373 Control Circuit:*** This circuit provides for command, interrupt, two response, and transmit control signals and provides main control over the SPCH (ie, controls when to transmit).

(b) ***FC374 Address Circuit:*** The address circuit processes address information, selects one of the eight SPCH units, processes three responses, monitors the 2-out-of-5 response code from the units, monitors the input bus for MPCH selection, informs of selection, and sends a 3-out-of-6 response to the 3A CC after selection.

(c) ***FC375 Information Circuits:*** Each circuit provides for processing a data byte (8 data bits plus 1 parity bit) and contains a mode control circuit to report the MPCH internal state to the 3A CC.

4.38 Upon reception of the first crosspoint from the 3A CC, FC373 loads the 7-bit register with a 1-out-of-6 code from 3A CC register R9. An enable set signal is sent to the FC374 address circuit to transmit the device address. The FC373 then responds with a data signal (via the receiver/transmitter in the SPCH). The enable flag is set to indicate that crosspoint information was received and that status data is a valid input/output instruction. The crosspoint signal condition is now in the 7-bit register and ready for reuse, if needed. A 300-nanosecond waiting period is then observed.

4.39 When the second crosspoint (MD3) is received from the 3A CC, the FC373 interrogates the 7-bit register and transmits the appropriate command code to SPCH (FC378 control/address circuit). The SPCH sends a data message to the peripheral device via the duplex bus selector. Another 150-nanosecond wait is exercised. The peripheral device responds to the data message with SYNC or BUSY, or no response at all. If no response is received within 19.2 milliseconds, the 3A CC transmits the next crosspoint.

4.40 The third crosspoint (MD2) is then transmitted by the 3A CC. This instructs the FC373 control circuit to send all zeros out on the command leads to which the device responds by clearing SYNC.

4.41 The 3A CC then transmits the fourth crosspoint (MD1). This crosspoint results in all address and data lines being cleared (all zeros), and the FC373 control circuit clears its internal state.

Control Circuit

4.42 The FC373 control circuit provides control over the operation of the PCH unit. Sequence logic of the FC373 provides the coordination of bus pulse circuits as well as all MPCH functions. FC373 sequence logic is under control of 3A CC microcode, sent via eight miscellaneous crosspoints. FC373 divides the 1.67-MHz clock pulse and provides this clock pulse to the bus. Also, FC373 supplies a 1-out-of-6 bus command corresponding to one of the following basic input/output commands:

- Read data
- Write data
- Output command
- Receive status
- Acknowledge interrupt
- Initialize.

4.43 FC373 controls the MPCH operation by the following circuits:

- The 7-bit command register
- Command pulse flag flip-flop
- Address sent flag flip-flop
- Command sent flag flip-flop
- Enable flag flip-flop
- Input/output inhibit override flag flip-flop.

4.44 At the start of each input/output instruction (first crosspoint), the enable flag is set and the 7-bit command state register is set to a 1-out-of-7 code that indicates the sequence (type of input/output command) to be performed. The seven states give the following bus commands:

- Data receive (DR)
- Sense status (SST)
- Data present (DP)
- Command present (CP)
- Initialization (INIT)
- Acknowledge interrupt (ACKI)
- Parallel channel maintenance state.

4.45 The second instruction (second crosspoint MD3) prepares the command pulse flag to be set on the next clock phase. The next clock phase resets the command pulse flag, which in turn sets the command sent flag. The third instruction (crosspoint MD2) prepares the command pulse flag to be set on the next clock phase. The next clock phase resets the command pulse flag, which in turn sets the command sent flag. This ends the command sequence.

4.46 The input signal address pulse (AF0) is set to logic one during bus transmission of the device address information. This signal is gated into the address pulse flag flip-flop. The command pulse flag is not allowed to operate if the address sent flag is not set. The DMA release flag is set during DMA operations when the 3A CC requests the parallel channel. The DMA then gives up control of the parallel channel. When the DMA release flag is set, the MPCH issues the device address and data stored in the 3A CC registers R9 and R10, respectively. Also, the MPCH issues the bus command stored in the 7-bit command state register. The DMA release flag is then reset as this command is transmitted.

4.47 During normal DMA operation, the DMA requests transmission of its requested command by setting the DMA set request flag. This flag toggles the command pulse flag and the command sent flag as described in paragraph 4.45. The DMA requests that the command be removed by setting the command pulse clear (CFCLR) flag, which toggles the command pulse flag and resets the command sent flag.

4.48 The enable flag is reset at the end of each 3A CC-to-parallel channel sequence by the 3A CC (crosspoint MD1).

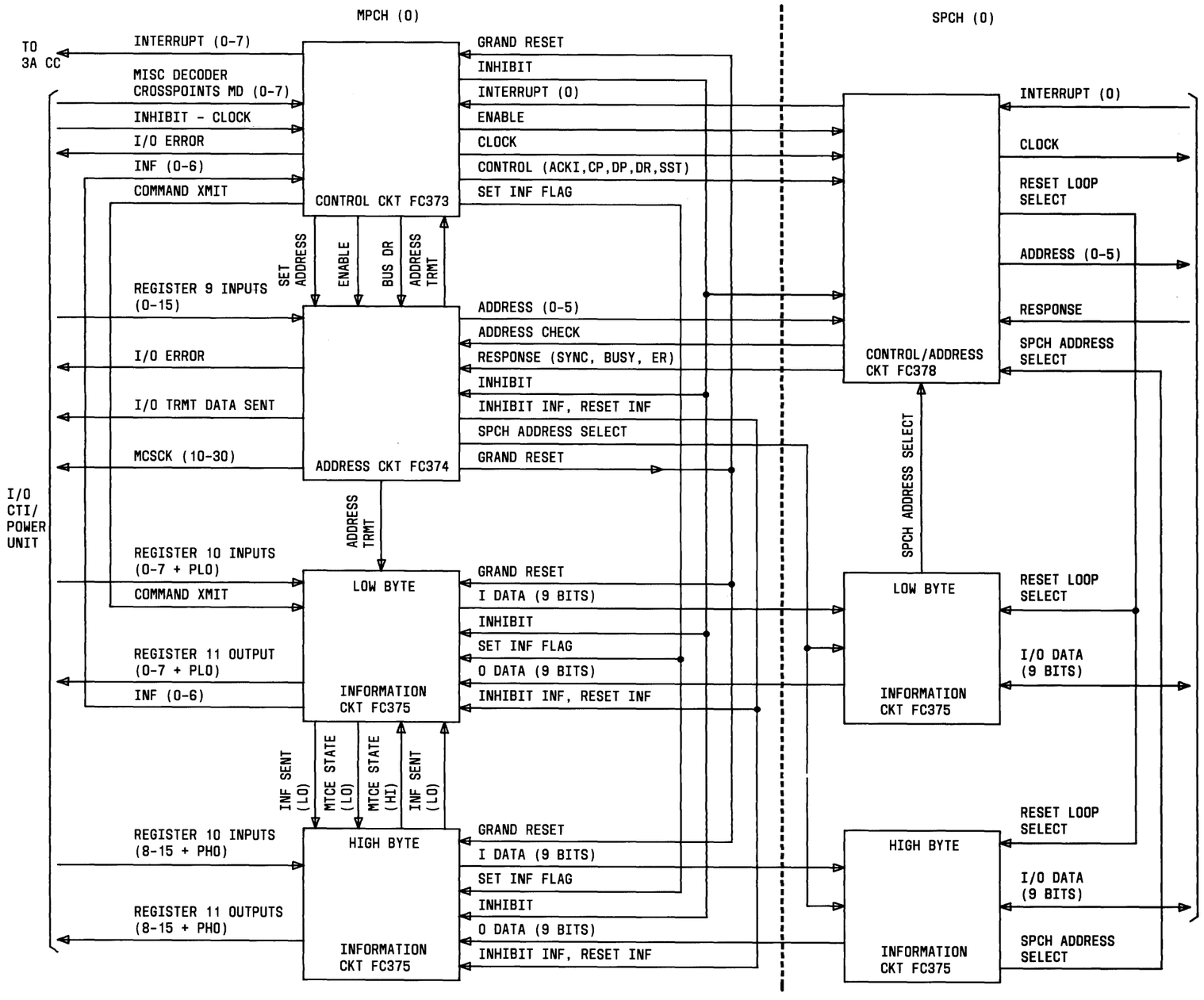


Fig. 26—MPCH-SPCH

4.49 The FC373 provides the following outputs to the SPCH for control functions:

- CLOCK0—1.67-MHz square-wave clock signal (for timing)
- ENA.10—Used to reset the SPCH bus receivers
- CF0—Provides a 150-nanosecond STROBE signal to initiate command lead transmission
- CF—When set, inhibits set pulses on bus command leads
- INIT0, ACKI0, SST0, DR0, DP0, RD0, or CP0—Indicates present instruction.

4.50 When more than one command signal is present, check circuits generate an input/output error (IOER0) signal, which is enabled by the command pulse flag.

4.51 The input/output inhibit override flag is set by the coincidence of the main channel select (MCS1) signal from the 3A CC and the zero-to-one transition crosspoint MD7. This allows the channel to function in a maintenance mode under control of the off-line 3A CC.

Address Circuit

4.52 The FC374 address circuit monitors the 3A CC register R9. Upon command from the MPCH control circuit, FC373 generates proper SPCH select and device address output signals. Also, all device responses received via the bus are received by FC374 and are conditioned before being sent to the 3A CC. All check circuit signals are resolved on FC374 and combined to make a single channel error signal to be monitored by the 3A CC.

4.53 Control for FC374 is received from FC373. This control state consists of combined contents of the address pulse flag flip-flop, address sent flag flip-flop, and MPCH error flag flip-flop. The high six bits of 3A CC register R9 (bits 15 through 10) are input as channel select inputs (CS_) and are decoded to generate main channel select signal (MCS). The next four bits of 3A CC register R9 (bits 9 through 6) appear as inputs and are decoded into a 1-out-of-8 SPCH address select signal (SPCAD_). The low six bits of 3A CC register R9 (bits 5 through 0) are gated via the FC374 to SPCHs to be transmitted as the device address bus signal (ADR00 through ADR50).

4.54 Action due to the first instruction from the 3A CC (first crosspoint) causes FC373 to pulse the set address line. The address pulse flag is set on the next clock phase and then reset on the following clock phase. The address sent flag, similar to the address pulse flag, is set to record generation of the address lead gating pulse. The ERROR flip-flop is strobed by the trailing edge of the address pulse flag signal to determine whether an error condition exists.

4.55 Upon receiving an XPTB1 input (a regenerated MD1 crosspoint signal), the address pulse flag will be toggled, thereby causing the address sent flag to be reset to zero. Three flip-flops are provided in FC374 to enforce SYNC, BUSY, and ER lead transitions on the trailing edge of the 3A CC clock pulse.

4.56 A grand reset (GRNDRST) signal is generated whenever a main channel address of a binary 011111 is present and a crosspoint MD0 instruction is given. Additionally, a grand set (GRNDSET) is pulsed when power (+5 volts) is applied to the unit during power-on sequencing. The grand set and grand reset are used to place the FC374 circuit into known states.

4.57 A subchannel address check (SCAC) circuit monitors SCAC lead inputs and operates if more than one SPCH is active while the address sent flag is set. This is detected by the occurrence of an invalid 2-out-of-5 code on these leads.

Information Circuit

4.58 The MPCH contains two FC375 information circuit packs. Low data byte (8 data bits plus 1 parity bit) is received by one FC375, and high data byte plus parity is received by the remaining FC375.

4.59 The FC375 interfaces a data byte (8 data bits plus 1 parity bit) between the 3A CC and the eight SPCHs. The FC375 uses a mode control circuit which may be examined to give a report of the MPCH internal states to 3A CC register R11. This status report is used during diagnostic checks and periodic channel integrity checks to provide access to test points.

4.60 The FC375 receives control data from the FC373 board. Control of the FC375 circuit is derived from the following flip-flops:

- Information pulse flag
- Information sent flag
- Maintenance state flag.

One byte of data (8 bits plus 1 parity bit) is gated from the 3A CC to the SPCH bus. This gating is controlled by the information inhibit (INFINH) signal generated by the FC374 so that data inputs (INF._) are enabled only until the address lines have been pulsed and are disabled during the remaining portion of each instruction.

4.61 When the first instruction (crosspoint) from the 3A CC is an MD6 or MD7, the set information flag input is pulsed by FC373. The information pulse flag will be set on the next 3A CC clock phase and then reset on the second clock phase. The information sent flag is set on the leading edge of the information pulse flag signal to indicate that the information lines have been pulsed. The information pulse flag is again set and reset along with the second operation of the address pulse flag from FC374 as commanded by the reset information (RINF) input. The information sent flag is reset by the cycle end (CYCEND) pulse generated by FC374 at the end of every instruction sequence.

4.62 The maintenance state of FC375 is entered by operation of an instruction from the 3A CC (crosspoint MD0) which sets the maintenance state flag. The maintenance state flag controls the 3A CC register R11 output multiplexer. When the maintenance state flag is set, a parallel channel status word is made available to the 3A CC. The parallel channel internal state appears as ST— inputs to the FC375. The maintenance state flag is reset by either the end of sequence crosspoint (MD1) or MD7 crosspoint from the 3A CC.

Subparallel Channel

4.63 The SPCH is functionally composed of three circuit packs: one FC378 control/address circuit and two FC379 information circuits (one per data byte). The SPCH operates under control of MPCH. Basically, the SPCH does not perform any signal processing but mainly provides transmitter/receiver facilities to drive the ac parallel bus that is interfaced to the peripheral devices. The SPCH is used to convert dc signals to bipolar pulses.

Control/Address Circuit

4.64 The SPCH control/address circuit, FC378, interfaces with the parallel bus address, control, clock, and response leads. Two basic circuits of the FC378 are the ac driver and ac receiver circuits. Inputs to the drivers are on the ADR._ leads, and driver outputs are on output leads SADR._/RADR_. Output pulses generated by the drivers are 150 nanoseconds wide. A logic one is indicated by positive voltage, and a logic zero by negative voltage. Driver outputs are enabled by signal AF01 or CF01 and the coincidence of signal SPCAD.B1 or SPCAD.A1, respectively.

4.65 Inputs (SSYNC1 and RSYNC1) are gated to the receiver and the receiver generates an output signal (SYNC0). SSYNC1 and RSYNC1 are balanced inputs, and the input to the receiver is a one when there is a positive signal on SSYNC1 with respect to RSYNC1 and a zero when a negative signal is on each. A compensating circuit is used that acts like a flip-flop and latches the last pulse detected.

4.66 Enable input (ENA1.0) is monitored for a high-to-low (one-to-zero) transition. When this happens, a 40-nanosecond pulse is generated on the reset output (RESET0). A negative-going transition on either the initialize (INIT0) or acknowledge (ACKI0) inputs cause a pulse to reset the interrupt receiver. Special inputs SPCAD.A1 and SPCAD.B1 are used to generate SPCH address check response signals SCAC.A0 and SCAC.B0. These are open collector tied to the backplane leads to form a 2-out-of-5 code which is checked by the MPCH.

SPCH Information Circuit

4.67 Two FC379 information circuits are used in the SPCH, each interfacing a byte of data (8 data bits plus 1 parity bit) between the duplex bus selector and MPCH. Also, an internal loop-around register is provided that supplies checking of the transmitted data.

4.68 The FC379 contains nine ac driver/receiver circuits. These circuits receive an information

signal [INF.(A through I)0] and generate a 150-nanosecond output signal [INFI.(A through I)0] on the AC bus. Positive voltage indicates a logic one and negative voltage indicates a logic zero. The AC bus receivers catch the positive-going pulse using a flip-flop arrangement. Each receiver is reset at the beginning of an input/output sequence by a pulse on the RESET0 circuit input. The loop-around register is strobed by a strobe signal (LDL.RG0). Also, the loop-around register may be selected over the bus receivers by a loop select signal (LOOPSEL0). SPCH select signal (SPCAD0) is received and sent to FC378 as a select signal (SPCHAD1).

E. Maintenance

Introduction

4.69 The PCH unit incorporates check circuits, the integrity of which are verified by the 3A CC (via a mode-control circuit on the MPCH control circuit FC373) or which may be stimulated to effect a report via the MPCH internal state through 3A CC register R11. This status report is used during diagnostic anlaysis to provide periodic channel-integrity audits to access test points. Failures detected by PCH unit self-check circuits or by input/output microcode sequences will cause an error interrupt by the 3A CC.

4.70 Special hardware features are used in the PCH unit to prevent conflict/interaction between the SPCHs. This ensures that only one SPCH serviced by an MPCH may be actively transferring data at any instant of time.

4.71 Errors within the PCH unit must be detected within one I/O instruction. (The data bytes are checked in the peripheral devices for correct parity.) FC374 uses a checking circuit to ensure that only one SPCH is active at a time. When an I/O instruction fails, the processor control flag (CF) is set to zero signifying that the instruction failed. The 3A CC does not initiate a retry automatically. Periodic audits and certain maintenance functions are performed by 3A CC instructions and checks. These are performed only in the maintenance mode. Miscellaneous decoder crosspoint MD0 loads the FC373 7-bit state register with data from register R10, thereby enabling microcode to audit PCH check hardware.

Note: PCH status checks are only performed in the maintenance mode while check circuits perform checks (integrity of data handling sequence) during normal signal processing.

Parallel Bus Interface Error Detection

4.72 To ensure that only the proper peripheral device responds to control signals, a sense status control signal must be issued periodically. The peripheral device, upon receiving this command, should gate its address code onto leads INF 0 through INF 5 plus 10 status bits onto leads INF 6 through INF 15 and the proper generated parity onto INF leads P_L and P_H. This is checked by the peripheral device software driver.

4.73 Normally, only one control lead should be set (to one) at a time. The fault of one control lead stuck at zero will be detected when that particular lead is used to send control data to the peripheral devices and there is no response. The fault of one control lead stuck at one might be indicated in one of two ways, either by improper response and/or no response. Two control leads being set and reset together can only occur due to a major fault in the MPCH. The MPCH is equipped with a special check circuit to detect this type of fault.

4.74 A control lead stuck at one and always present at the peripheral device interface will cause the SYNC signal to become stuck, ensuring detection. (SYNC may only be set to zero if all the control leads are in the zero state.) The two information parity bits (INF P_L and INF P_H) are used to detect faults on the information leads employing odd parity. An address lead fault is detected when the desired peripheral device fails to respond to a given instruction.

4.75 Synchronization (SYNC) lead faults are detected when the SYNC lead fails to change its state (zero-to-one and then one-to-zero) in response to a control signal. NOTBSY failures are detected in an analogous manner. An error (ER) lead stuck at zero is checked by having the peripheral device set error to one while the peripheral device sets SYNC to one in response to a CP signal. An ER lead stuck at one is an indication of an error to the 3A CC. The interrupt lead is checked by periodic audits. Clock signal errors can be diagnosed by periodic audits and/or device failure modes.

5. DUPLEX BUS SELECTOR

INTRODUCTION

5.01 The DBS (Fig. 27) is used to interface a peripheral device (DEV) to a subparallel channel (SPCH) of the 3A CC. The SPCH may be a part of either a parallel channel (PCH) unit or a direct memory access (DMA) channel unit. The DBS converts bipolar ac pulses from the channel unit in the active central control to transistor-transistor logic (TTL) levels and passes these signals to the peripheral device. Conversely, the DBS converts TTL level signals from its peripheral device to bipolar ac pulses for transmission to the PCH.

A. Physical Description

5.02 The DBSs are located in the peripheral devices that require its functions. The DBS-to-DEV bus is composed of four flat flexible cables. The ac parallel bus between the subparallel channel and its associated DBS units consist of 35 twisted pair conductors making up a single cable. An additional signal pair (physically independent of the main bus) is implemented for a DMA channel. Up to 16 DBSs may be connected to one ac parallel bus. Connections to each unit are made through type 942-943 multipin connectors. Power and ground are applied through multilayer printed wiring board (MLPWB) backplane.

5.03 Each DBS unit usually consists of six or seven FC-type circuit packs housed in a type 88A 12-card front-removable housing. A designation strip on the front of the housing identifies each circuit pack and its physical location. Six of the FC-type circuit packs provide the logic for interfacing and control functions of the DBS. The seventh circuit pack, type FC402, provides power sequencing and monitoring of power-on and mode control for the DBS. The FC402 power sequencer circuit pack

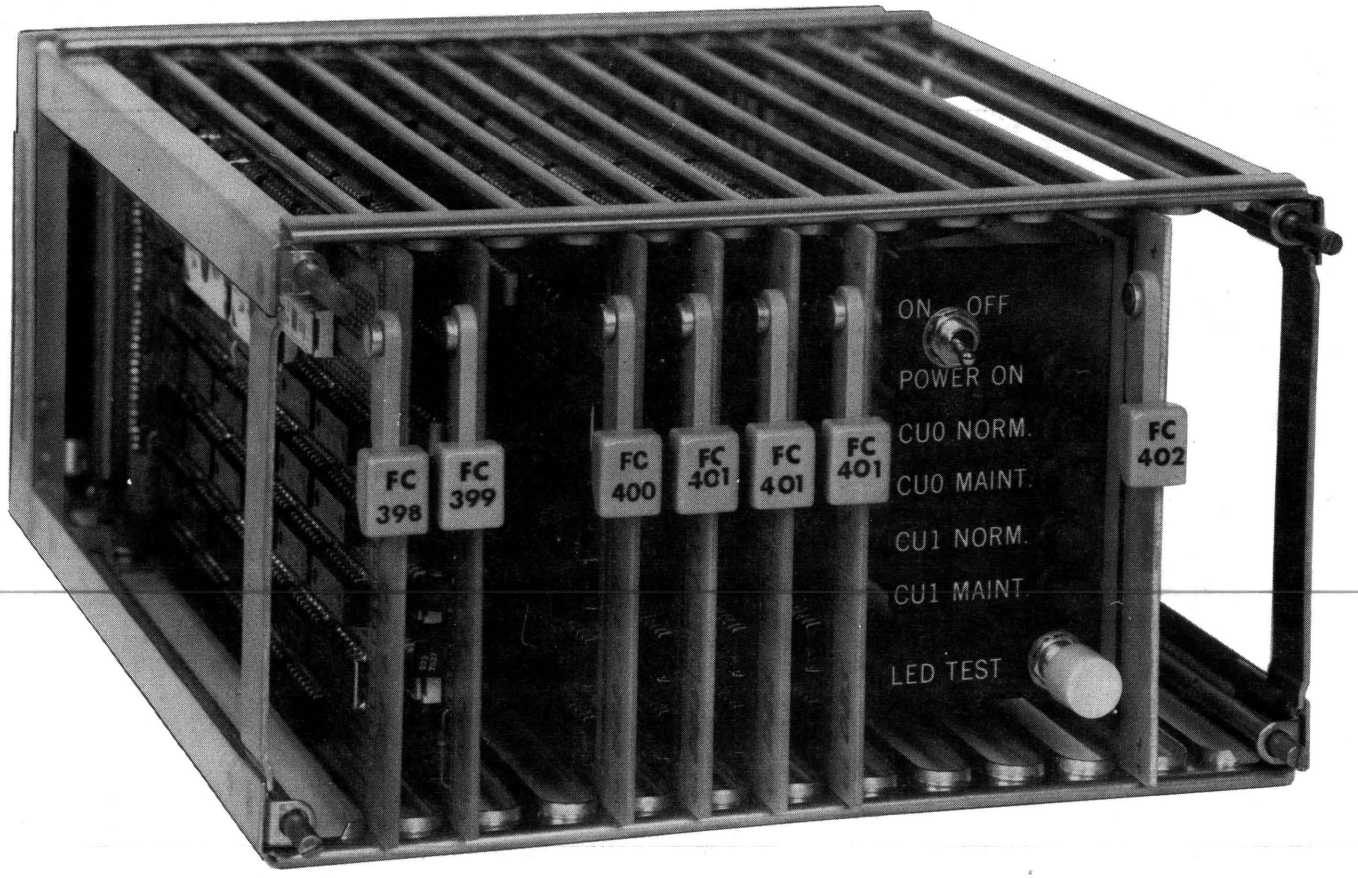


Fig. 27—DBS Front Panel and Circuit Locations

is optional in some applications of the DBS. Adjustments are not provided on the DBS circuit packs.

B. Interfacing and Control Circuit Packs

5.04 Interfacing and control logic for the DBS consists of the following circuit packs:

- One FC398 control and timing (CONT)
- One FC399 command (CMND)
- One FC400 address (ADR)
- Three FC401 information (INF).

These packs contain the transformer-coupled bus receivers and drivers, and integrated circuit components required for all logic functions of the DBS.

Power Sequencer

5.05 The FC402 power sequencer resides in position 11 of the DBS housing unit (Fig. 27). A front panel on the FC402 contains the following switches and light-emitting diode (LED) indications:

- Power on-off switch (PWR)
- Light-emitting diode test switch (LED TEST)
- Power on indicator
- Control unit one maintenance mode indicator (CU1 MAINT.)
- Control unit one normal mode indicator (CU1 NORM.)
- Control unit zero maintenance mode indicator (CU0 MAINT.)
- Control unit zero normal mode indicator (CU0 NORM.).

The FC402 power sequencer circuit pack contains integrated circuit packages which drive LED indicators, in addition to discrete components and relay circuitry for performing proper sequencing of power to the DBS.

C. Functional Description

5.06 Each peripheral device requires a DBS for interfacing to the bus. The parallel bus is a transformer-coupled 35-lead ac bus and utilizes bipolar pulses. It is the communication link which provides for peripheral device addressing, transfer of information (data) between the subparallel channel and peripheral devices, control signals to peripheral devices, and response signals from peripheral devices. One other lead, separate from the 35-lead bus, provides an additional response signal from each DBS to the direct memory access channel. Peripheral devices interface to duplicate parallel buses via a DBS, thus providing access to peripheral devices from either 3A CC in a duplex processor configuration. Details of the parallel bus configuration are shown in Fig. 28 and 29. The DBS is a 2-port device and functions as a multipole, double-throw switch connecting peripheral devices to the active 3A CC (Fig. 30). Duplicate halves of the DBS (side 0 and side 1) interface with the corresponding duplicate processor channels. Common circuitry in the DBS interfaces the selected side of the DBS with the peripheral device. Under normal conditions, the DBS is functionally invisible to both the active processor and the peripheral devices. However, during diagnostics and system reconfiguration, the DBS can be instructed to intercept and execute input/output (I/O) commands. The DBS converts ac bus signals to TTL levels and passes these signals from the active 3A CC to the peripheral device. Conversely, the DBS converts TTL level signals from its peripheral device to bipolar ac pulses for transmission to the 3A CC.

Functional Sections Within the DBS

5.07 The DBS consists of three major functional blocks:

- Bus drivers and receivers
- Control and timing information
- Power sequencing.

Bus Drivers and Receivers

5.08 Five of the seven circuit packs used in the DBS contain bus drivers and receivers. Three FC401 INF circuit packs interface the 18 information leads. One FC400 ADR circuit pack interfaces six address leads, the 1.67-MHz clock

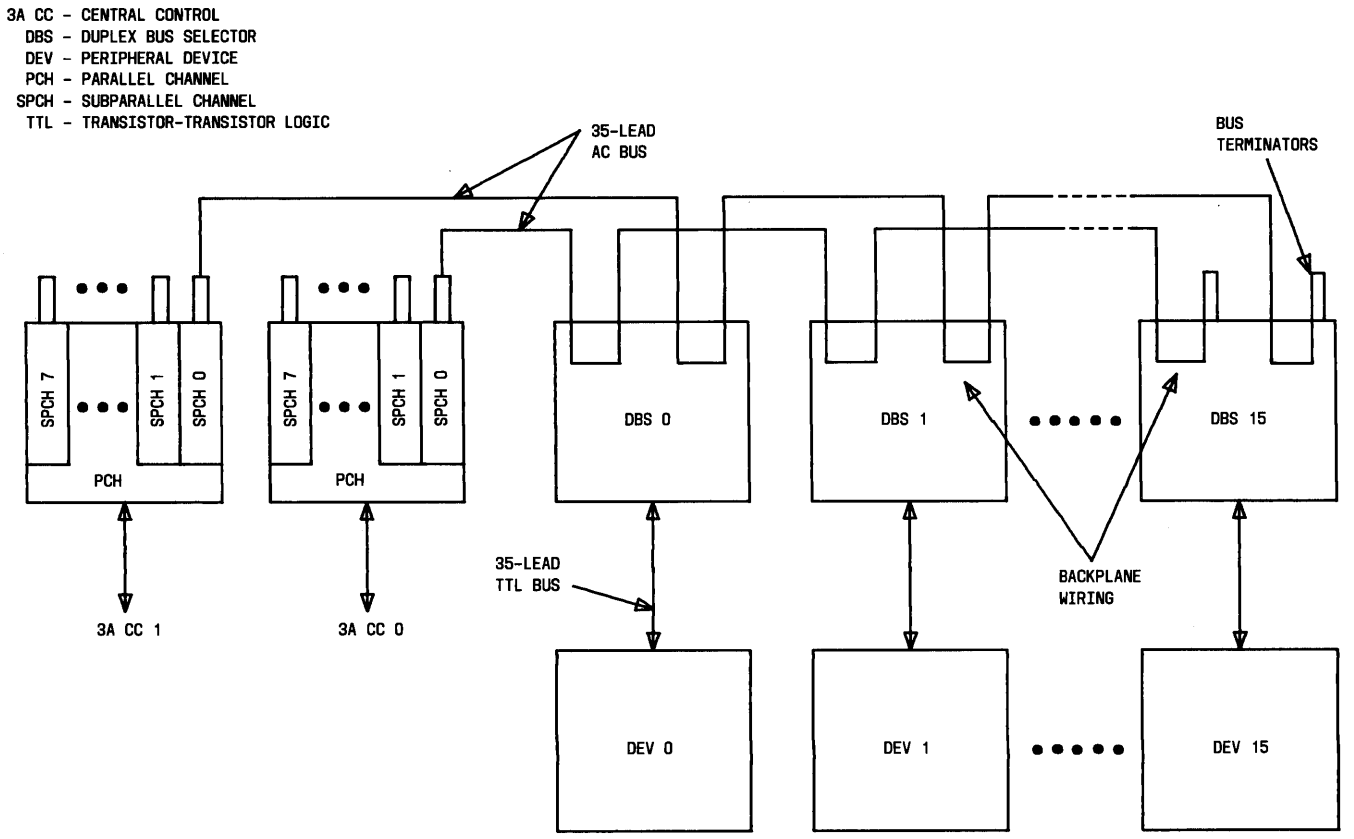


Fig. 28—Parallel Bus Configuration

lead, and the direct memory access request (DMAR) and error (ER) response leads. One FC399 CMND circuit pack interfaces six control leads and the synchronization (SYNC), NOTBSY, and interrupt (INTP) response leads.

Control and Timing Information

5.09 Control and timing information for the DBS is derived from FC398 CONT circuit pack. This circuit pack contains mode control flip-flops, DBS command decoding circuits, and decoding circuits for DBS address and maintenance address 111100. Control circuits for DBS readout to the ac bus are also contained in this circuit pack.

Power Sequencing

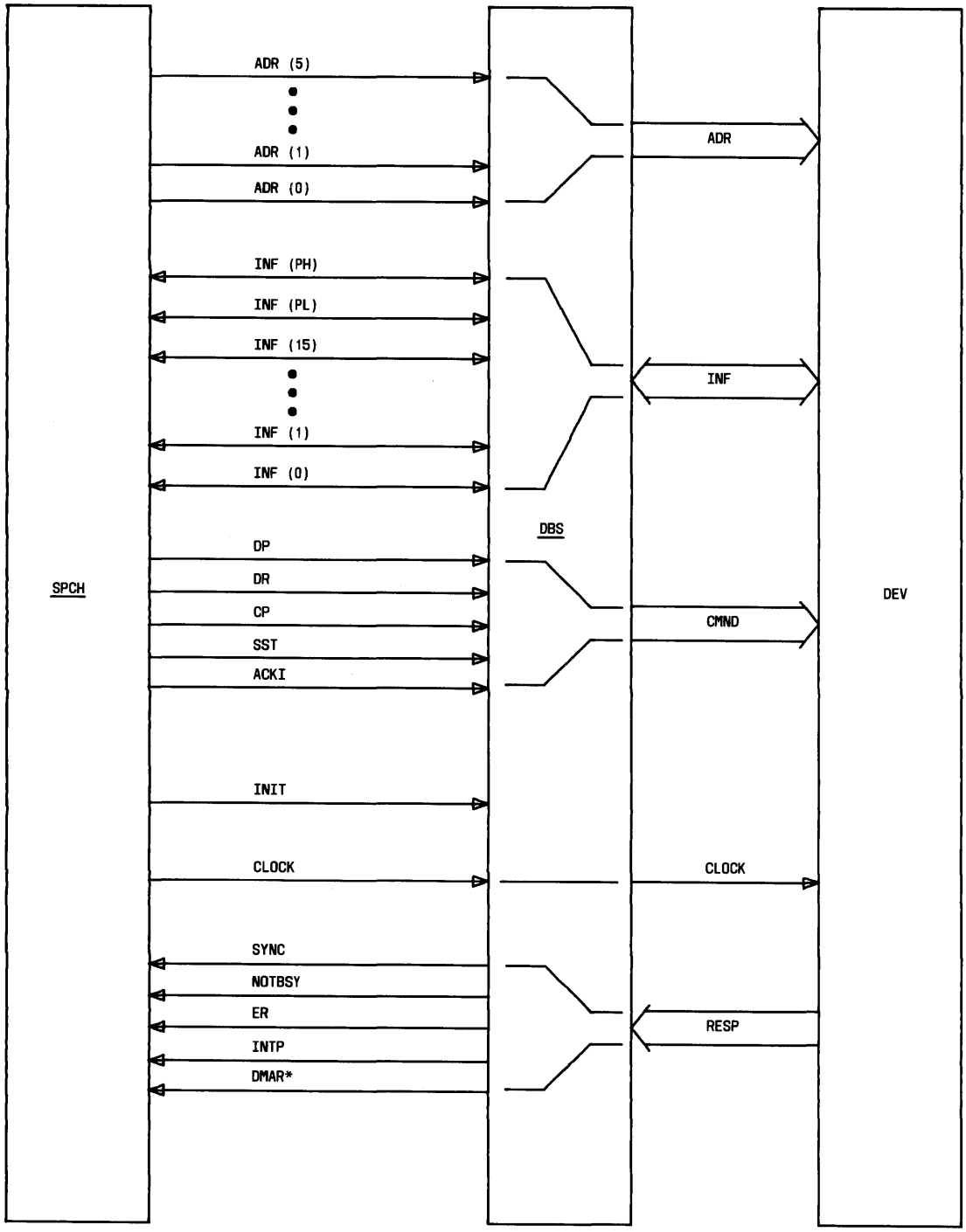
5.10 Power sequencing to the DBS is required to prevent outpulsing onto the parallel bus during power-up or power-down of the DBS. Power is applied (or removed) in two phases. Phase one of a power-up sequence applies +5 volt logic power to the DBS prior to application of bus power. Both central control 0 and 1 sides of the DBS are initialized to an out-of-service mode. Phase two of a power-up sequence provides power to the bus driver circuits after a short delay. On power-down of the DBS, power sequence phase two precedes phase one. Bus driver power is removed prior to removal of logic power.

D. Theory of Operation

Parallel Bus Lead Description

5.11 A transformer-coupled ac parallel bus connects each subparallel channel with up to 16 DBSs, and up to 16 peripheral devices as shown in Fig. 28. The parallel bus consists of the following twisted pair signal leads:

- Eighteen information leads



* FOR DMA CHANNEL ONLY.

Fig. 29—DBS Bus Lead Structure

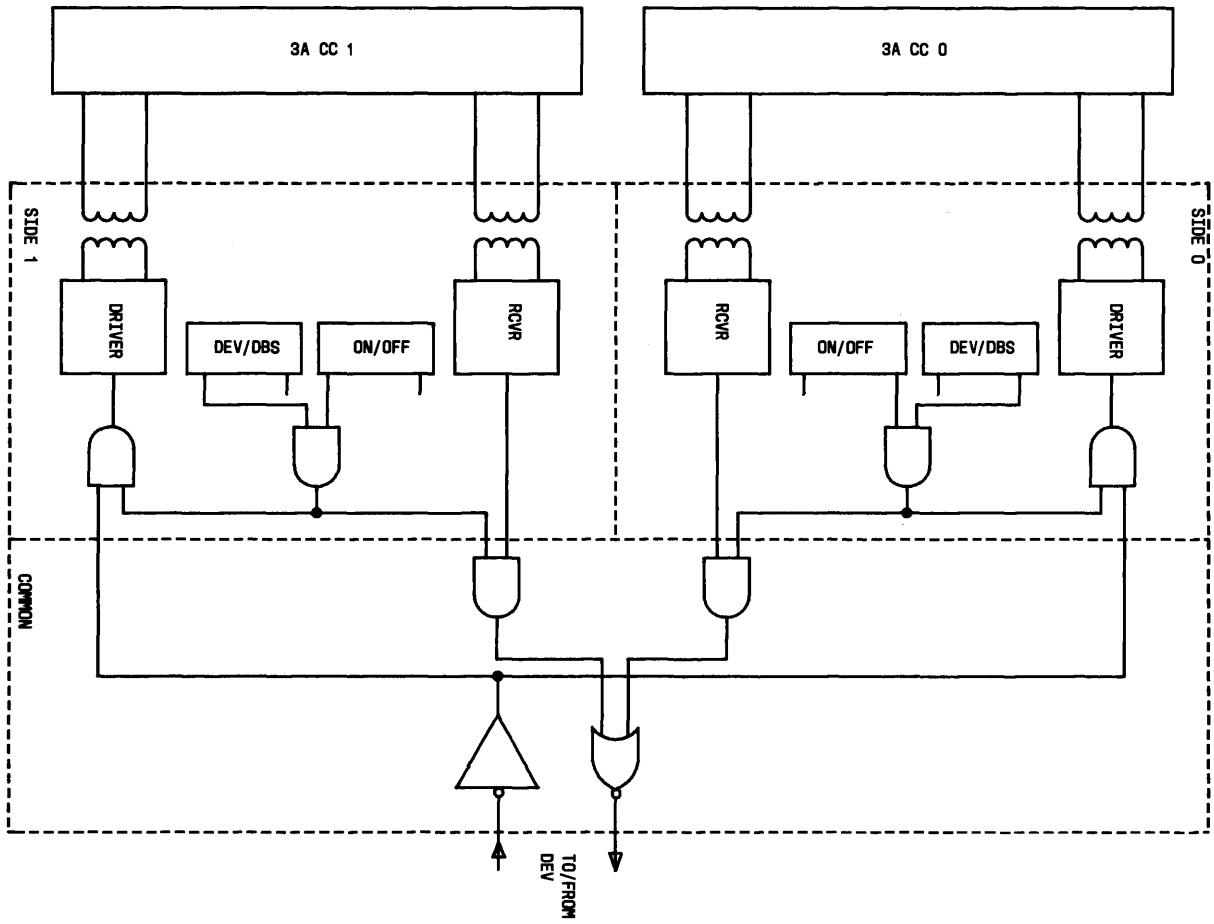


Fig. 30—DBS Functional Diagram

- Six address leads
- Six control leads
- Four response leads to a parallel channel, or five response leads to a direct memory access channel
- One clock lead.

Pulses generated by the subparallel channel are approximately 150 nanoseconds wide and signals generated by the DBS on the ac bus are approximately 200 nanoseconds wide. Information transmission on the ac bus is accomplished with balanced differential bipolar pulses. A positive voltage differential on the two leads of a twisted pair represents a logic one, while a negative voltage differential corresponds to a logic zero.

5.12 Exceptions to the bipolar convention are the interrupt (INTP) and information (INF) leads. An interrupt signal from any peripheral device may occur at any time. Since the INTP

signal lead on the ac bus is paralleled from all DBSs on the bus, a means is required for the 3A CC to determine which peripheral devices sent an interrupt. On signal from the 3A CC, each interrupting peripheral device sets a predefined information data bit to one while all other peripheral devices set their assigned bit to zero. This ***wired-OR*** arrangement for the interrupt function requires unipolar pulsing (logic ones only) on the INTP signal lead, and on the INF leads when transmitting from the DBS to the subparallel channel. Since the parallel bus contains 16 INF leads, this is the factor which limits each bus to a maximum of 16 devices connected to it.

5.13 Duplicate ac buses, one from each 3A CC channel, are connected to each DBS. The ac signals from the active subparallel channel are converted by bus receivers to TTL levels and passed on to the peripheral devices. Similarly, TTL level signals from the peripheral devices are converted to ac by an ac bus driver and put on the ac bus for transmission to the active 3A CC. All signals passed to and from the peripheral device by the DBS are at TTL levels and are active low. That is, a logic one is presented as a low voltage, while a logic zero is presented as a high voltage level.

Information Leads

5.14 The 18 information leads are bidirectional and are used by the subparallel channel both to send data and commands to a peripheral device and to receive data and status from a peripheral device. These leads provide for 16 data bits, INF(0) through INF(15), and two parity bits, INF(P_L) and INF(P_H). INF(P_L) provides odd parity over data bits INF(0) through INF(7), and INF(P_H) provides odd parity over data bits INF(8) through INF(15). In conjunction with the command present (CP) signal, commands are transmitted to a properly addressed peripheral device on leads INF(1) through INF(15). INF(0) is reserved for a channel maintenance function when command present signal is set. When INF(0) is set to a one, CP is inhibited from reaching the peripheral device.

Address Leads

5.15 Six address leads are used to select a particular peripheral device location. These leads are unidirectional and use bipolar pulsing. Five of the address leads, ADR(0) through ADR(4), select 1 of 32 possible binary addresses. The sixth lead provides odd parity over the five address bits. Although 32 possible locations are uniquely addressable, only 16 peripheral devices may be attached to a single ac bus. The limit of 16 peripheral devices on a parallel bus is set by the maximum of 16 INF leads available for unique identification of an interrupting device. Each DBS is assigned a unique 3-out-of-6 code address and a unique 5-bit plus odd parity binary address, both of which are specified by backplane wiring straps. (A 3-out-of-6 code is defined as a group of 6 bits having three, and only 3 bits set to ones.) The 3-out-of-6 code address is returned to the 3A CC as part of the DBS maintenance status word. The use of 3-out-of-6 codes provides the capability to verify that only one DBS unit is responding to the 3A CC. If more than one DBS transmits its status word, the resulting status address field will not be a 3-out-of-6 code. The 5-bit binary address is employed to select a particular DBS during diagnostics and system reconfiguration. In addition, all DBSs share a single maintenance address, 111100. This address is reserved for diagnostics only and is otherwise an illegal address since it contains even parity.

Control Leads

5.16 The six control leads are unidirectional and use bipolar pulsing. These are used by the subparallel channel to send control signals to a peripheral device (or its DBS) to transfer data and commands. The six control leads are identified as:

- Command present (CP)
- Data present (DP)
- Data request (DR)
- Sense status (SST)
- Acknowledge interrupt (ACKI)
- Initialization (INIT).

Command Present (CP)

5.17 The peripheral device selected by address leads ADR(0) through ADR(5) is requested to receive a command on information leads INF(0) through INF(15) when CP is set to one. INF(0) is reserved for a channel maintenance function. The CP is inhibited from the DBS-to-DEV bus if

the DBS port is not in the NORMAL (DEV,ON) condition or if INF(0) is not a zero.

Data Present (DP)

5.18 The peripheral device selected by address leads ADR(0) through ADR(5) is requested to accept data from the INF leads when DP is set to one. The DP is inhibited from the DBS-to-DEV bus when the DBS port is not in the NORMAL mode.

Data Request (DR)

5.19 The peripheral device selected by address ADR(0) through ADR(5) is requested to gate data onto the INF leads of the bus when data request is set to one. The DR is inhibited from the DBS-to-DEV bus if the DBS port is not in the NORMAL mode. The DR also inhibits the ac INF receivers from the DBS-to-DEV bus thus allowing the peripheral device to gate data onto the bus.

Sense Status (SST)

5.20 When SST is set to one, the peripheral device selected by address leads ADR(0) through ADR(5) is requested to gate the contents of its status register onto information leads INF(6) through INF(15), and its address code onto information leads INF(0) through INF(5). An SST command must be accepted and properly responded to by the device addressed, regardless of its busy status. The SST is inhibited from the DBS-to-DEV bus if the DBS port is not in NORMAL mode. The SST also inhibits the ac INF receivers from the DBS-to-DEV bus thus allowing the peripheral device to gate status onto the bus.

Acknowledge Interrupt (ACKI)

5.21 A peripheral device may issue an interrupt request at any time. When one or more peripheral devices on a parallel bus issue an INTP, the active 3A CC must determine which peripheral device(s) issued the request. In response to one or more interrupt requests, the active 3A CC issues an ACKI to all peripheral devices on the parallel bus. All peripheral devices on the bus are selected simultaneously. The ACKI is inhibited from the DBS-to-DEV bus if the DBS port is not in the NORMAL mode or if the maintenance address is present on address leads ADR(0) through ADR(5). This condition is employed during diagnostics to effect a test of the ACKI lead. The ACKI instructs each peripheral device sending an interrupt request to set a single predefined INF bit to one, while all other peripheral devices set their assigned bit to zero. The 3A CC then identifies the interrupting peripheral devices by the INF bits containing ones. The ACKI also inhibits the ac INF receivers from the DBS-to-DEV bus while allowing the peripheral device to gate its one INF bit onto the bus.

Initialization (INIT)

5.22 During a processor switch, the INIT lead is used to simultaneously switch all DBSs on a single subparallel channel toward the 3A CC which issues the control signal. The INIT, in conjunction with the DBS maintenance address on address leads ADR(0) through ADR(5), switches the on-line port of the DBS to the NORMAL mode and the other DBS port to an out-of-service state. With any address other than 111100, INIT does not change the control state of the DBS, but does clear the maintenance DMAR flip-flop. The INIT signal receiver output is converted to a pulse by a monostable multivibrator to prevent failures in one 3A CC from locking out the other 3A CCs access to the peripheral device. The INIT is not passed on to the peripheral device. The peripheral device must be initialized by a send device command (SDC) instruction (CP control signal).

Response Leads

5.23 The peripheral devices send responses back to the 3A CC over the response leads of the ac parallel bus. These leads are identified as follows:

- Synchronization (SYNC)
- NOTBSY
- Error (ER)
- Interrupt (INTP)
- DMA request (DMAR).

These leads are all unidirectional and bipolar, except INTP, which is unipolar. The INTP may be set by the peripheral device at any time. The NOTBSY, SYNC, and ER are set only while a peripheral device is currently selected by address leads ADR(0) through ADR(5). The DMAR lead is required for

direct memory access operations. Peripheral devices not served by a direct memory access channel do not use this lead.

Synchronization (SYNC)

5.24 A SYNC signal is generated by a peripheral device in response to any control signal that has been properly received and acted upon by the peripheral device. The SYNC is set to one to indicate that a control signal has been understood and data has been gated onto or from the information leads.

NOTBSY

5.25 The device selected by address leads ADR(0) through ADR(5) gates the contents of its READY flip-flop onto the NOTBSY lead in response to a control signal.

Error (ER)

5.26 In the NORMAL mode, the ER lead is set to one when the peripheral device selected by the ADR leads detects any abnormal condition. To check the operation of the ER lead, its meaning is reversed in response to the CP control signal.

Interrupt (INTP)

5.27 The interrupt lead is set to one at any time a peripheral device, whether addressed or not, wishes to interrupt the processor.

DMA Request (DMAR)

5.28 A peripheral device serviced by the DMA employs the DMAR to initiate a 16-bit word transfer directly into memory during an autonomous DMA block transfer. The peripheral device sets the DMAR lead to one when it is ready to transmit or receive another word of data. The DMAR is then cleared in response to the DP or DR subsequently sent by the DMA. Peripheral devices not served by a DMA channel do not use this lead.

Clock Lead

5.29 The clock lead carries a 1.67-MHz clock signal from the 3A CC via the subparallel channel and associated DBS to the peripheral device. During diagnostics, an internal clock check circuit is employed to guarantee the integrity of the clock receivers. The check circuit outputs are reported as part of the DBS status word.

Bus Drivers and Receivers

5.30 Bus drivers and receivers within the DBS connect to the ac parallel bus from the subparallel channel and to the DBS-to-DEV bus. Each bus receiver converts ac pulses from the parallel bus to TTL levels for processing by the DBS or peripheral device. Each bus driver converts TTL level information from the peripheral device or DBS to ac pulses and outpulses the information onto the parallel bus. The six ADR leads, six CONT leads, and the clock lead all terminate into receivers in the DBS. The five response leads are connected to drivers within the DBS. The 18 INF leads are bidirectional and therefore connect to both receivers and drivers in the DBS.

5.31 The basic element of the ac bus drivers and receivers is a 3-winding transformer (Fig. 31). One winding is connected to the twisted pair signal leads on the ac bus in parallel with up to 15 other DBSs. A second winding functions as a receiver winding and a third winding functions as a driver winding. Each parallel bus signal lead utilizes only that part of the circuit shown in Fig. 31 which is required to perform its function as stated in paragraph 5.30. Each DBS receiver consists of a differential voltage comparator with positive feedback to form a Schmitt trigger. The line input of the comparator is biased by the feedback network to a voltage slightly above or below the comparator reference voltage, depending upon whether the receiver is in the one or zero state. Incoming pulses must be of an amplitude great enough to raise or lower the line input voltage to within 100 mV of the reference voltage. When this occurs, the comparator output state will change. This state change is fed back through the resistor divider into the line input, thus reinforcing that change and latching up the receiver. To provide a symmetric set-and-reset trigger threshold, the comparator reference voltage is set halfway between the receiver output zero and one voltage levels. Thus, a receiver is set or reset depending on whether a one or zero, respectively, was transmitted on the ac bus to the DBS. Output of the receiver is then passed to the peripheral device under control of the FC398 CONT circuit pack. The signals on the DBS-to-DEV bus are active low. The bidirectional INF leads employ open collector TTL gates pulled up to +5 volts

through a 680-ohm resistor in the DBS. The address, control signal, and clock leads utilize medium power TTL gates.

5.32 Each DBS driver circuit consists of a differential line driver with complementary outputs connected to the driver winding of the transformer (Fig. 31). These outputs serve as a source and sink for current flow through the transformer winding when the driver is enabled by an active high pulse input. If the data input to the driver is a one (active high) when the driver is pulsed, current flows from the noninverting output gate (A) through the transformer and into the current sinking stage of inverting output gate (B). This generates a voltage across the transformer winding which is induced onto the ac bus as a positive pulse. If the data input is a zero when the driver is pulsed, current flows in the opposite direction through the transformer. The current flow is from the inverting output gate (B) and into the current sinking stage of noninverting output gate (A). This induces a negative pulse onto the ac bus. Positive 200-nanosecond wide driver pulses are derived from a monostable multivibrator which is triggered on both rising and falling edges of the incoming data signal. Thus, a transition of the signal from zero to one (rising) will induce a positive pulse onto the ac bus, while a transition from one to zero (falling) will induce a negative pulse onto the ac bus. These pulses of opposite polarity represent the bipolar one and zeros transmitted to the SPCH on the response leads.

5.33 Unipolar bus drivers for the 18 INF leads and the INTP lead utilize the same type of driver circuit with the exception that the data input to the line driver is tied to a positive voltage so that only ones can be transmitted. Similarly, only rising edges cause outpulsing. All INF drivers whose input INF signal is a one are simultaneously enabled on the rising edge of SYNC. This is accomplished by ANDing the incoming data signal with the pulse generated by the rising edge of SYNC. Data for the INF bus drivers is multiplexed from one of four separate sources by the FC398

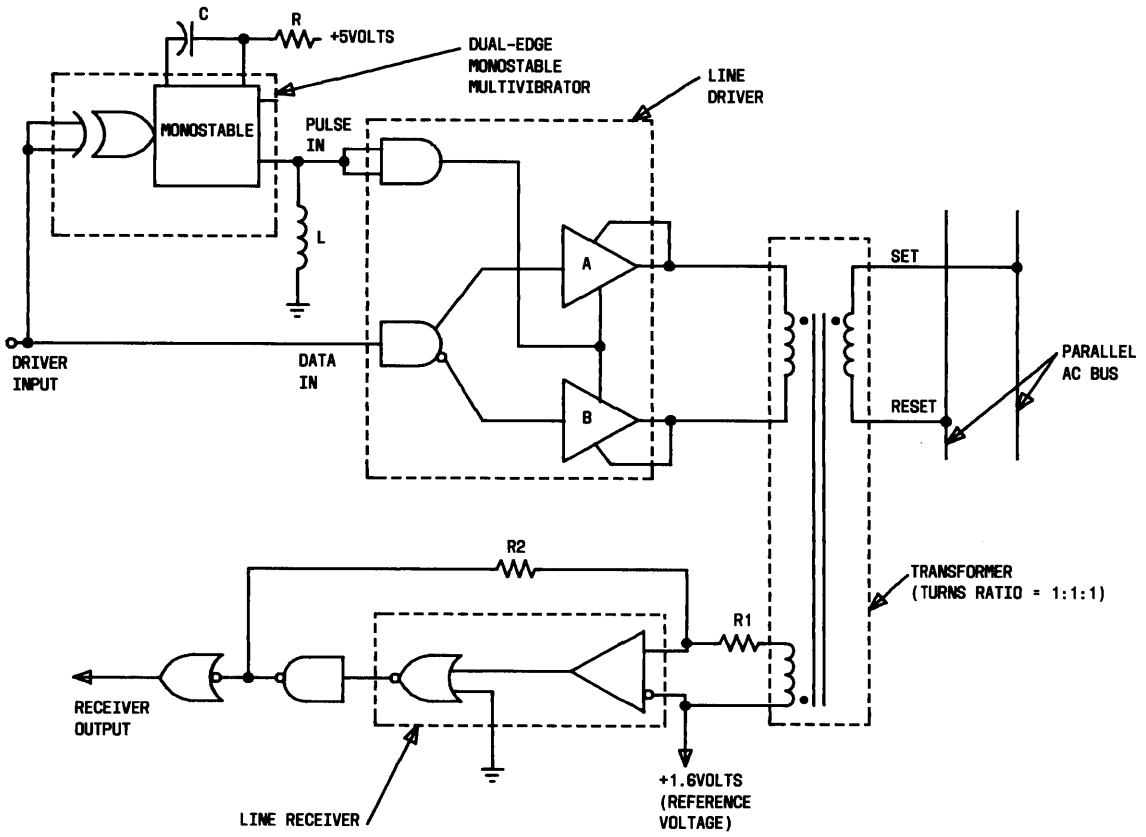


Fig. 31—DBS Bipolar Driver and Receiver Circuits

CONT circuit pack. When the DBS is in the NORMAL mode, data to the INF bus drivers is gated from the peripheral device interface. When the DBS is in a MAINTENANCE mode, data to INF bus driver circuits is multiplexed from:

(a) A register which allows data from the INF bus receivers to be stored and looped back onto the INF bus drivers

(b) DBS status information

(c) A positive voltage source which supplies an all ones response to a maintenance ACKI instruction.

Control and Timing

5.34 As shown in Fig. 30, the DBS is partitioned into two duplicate sides to allow a single TTL peripheral device interface to be switched to either of two ac parallel bus interfaces. Each port of the DBS is connected to the 3A CC via an ac bus; however, only one 3A CC at a time is connected to a peripheral device. Accordingly, one 3A CC can execute channel diagnostics while the other 3A CC simultaneously executes normal I/O functions. Each side of the DBS has two control state flip-flops which determine its mode of operation. One, an ON/OFF flip-flop, enables or disables its side of the DBS from communicating on the ac bus. The second, a DEV/DBS flip-flop, functions as a seventh address bit. Since the peripheral device and DBS addresses overlap, a method is required to distinguish between peripheral device instructions and DBS instructions. The DEV/DBS flip-flop performs this function. In the DEV (set) state, this flip-flop directs instructions and addressing from the 3A CC through the DBS to the peripheral device. The DBS (clear) state of the flip-flop causes control signals to be blocked from the peripheral device. Each port of the DBS may then be in one of four possible control states:

- DBS, OFF (Out of service)
- DBS, ON (MAINTENANCE mode)
- DEV, ON (NORMAL mode)
- DEV, OFF (Out of service).

In the NORMAL mode, the DBS side connected to the on-line 3A CC (MY side) is set to a DEV, ON state. This mode enables the DBS-to-DEV interface and connects the ac bus through the DBS to the peripheral device. The DBS side connected to the off-line 3A CC is always set either to an out-of-service mode (OFF) or to a MAINTENANCE mode (DBS, ON). The MAINTENANCE mode inhibits the DBS-to-DEV interface and enables the DBS to respond to all control signals from the 3A CC when properly addressed. A third flip-flop in each side of the DBS provides a maintenance DMAR signal on command from the 3A CC.

5.35 During power-up or power-down of the DBS, all control and DMAR flip-flops are locked to a reset state by the power sequencing of +5 volts BUSPWR. Both sides of the DBS are initially set to a DBS, OFF mode. After initial power-up, each 3A CC determines the state of the two control flip-flops associated with the DBS port by issuing an appropriate command. An INIT command, in conjunction with maintenance address 111100 issued by either 3A CC, initializes the control flip-flops for both sides of all DBSs on a single subparallel channel. The 3A CC issuing the command switches its side of the DBSs to DEV, ON and the OTHER side to DBS, OFF. The INIT command with any other address will not change the DBS control state, but will clear the DMAR flip-flop. At any other time, two control flip-flops for a particular side of the DBS can be altered only by the 3A CC with which they are associated. The contents of all four control flip-flops and the DMAR can be interrogated by either 3A CC.

5.36 The address present in the MY address receivers of the DBS is continuously compared to the binary DBS address (specified by backplane wiring) and to the shared maintenance address (111100). Presence of either address when in the DBS, ON (MAINTENANCE) state enables the DBS to respond to DP, DR, and SST control signals. In the MAINTENANCE mode, the DBS responds to ACKI in conjunction with a maintenance address only. In either MAINTENANCE or NORMAL mode, the DBS responds to a CP control signal in conjunction with the binary DBS address when INF(0) is set to one. In all cases of DBS instructions, the DBS generates the SYNC and NOTBSY responses to indicate proper receipt of the control signals.

5.37 Each 3A CC alters the state of the two control flip-flops associated with its DBS port by issuing a CP control signal to the DBS with INF(0) set to one. The CP control is inhibited

from the DBS-to-DEV bus when INF(0) is set to one. Actual response of the DBS to this command is determined by a 2-out-of-4 code on leads INF(1) through INF(4) as shown in Table G. In addition to set and reset commands to the control flip-flops, commands are provided which cause the DBS to respond with a DMAR or interrupt request for maintenance purposes. When the CP and INF(0) commands are active, the meaning of the error signal is reversed. The seven decoded DBS commands shown in Table G are ORed together to cause an active ER signal when a valid command is recognized.

TABLE G

TABLE OF DBS OPERATIONS IN RESPONSE TO CP WITH INF (0) SET

INF (4–0)	DBS OPERATION
00001	NO STATE CHANGE
00111	DEV/DBS → DBS (CLEAR)
01011	DEV/DBS → DEV (SET)
01101	ON/OFF → OFF (CLEAR)
10011	ON/OFF → ON (SET)
10101	DMAR → SET
11001	INTERRUPT REQUEST

5.38 Either 3A CC may interrogate the state of the DBS when its DBS port is in MAINTENANCE mode (DBS, ON). In response to an SST control signal, the DBS selected by the address leads returns a status word to the 3A CC on the INF leads. Format of the status word is shown in Fig. 32. The status address returned is the 3-out-of-6 code equivalent of the binary DBS address. This address, like the DBS binary address, is specified by backplane wiring. A logic one transmitted on the ac bus represents a ***false*** condition for status and a ***true*** condition for address in the status word. If more than one DBS responds to the status request, an invalid address (non 3-out-of-6 code) will appear on the bus.

5.39 The 3A CC can loop a 16-bit data word through the DBS and read it back. In response to a DP control signal, the DBS selected by the address leads reads a 16 plus 2 parity bit word from the INF leads of the ac bus and stores it in a loop-around register. A subsequent DR control signal addressed to the same DBS causes the DBS to output the data word onto the INF leads to the 3A CC. In this mode, the DP or DR control signals also apply a reset to the DMAR flip-flop. In response to an ACKI control signal and the maintenance address, 111100, the DBS sends an all ones data word on the INF leads. Other interface functions are verified with INTP and DMAR commands. An INTP command causes the DBS to return a pulse on the INTP signal pair. A DMAR command, however, causes the DBS to hold its DMAR signal set until it is subsequently cleared by either a DP or DR control signal or by an INIT.

Power Sequencing

5.40 Each DBS is powered by a converter furnished by the peripheral device interfacing the DBS. All DBSs connected to one subparallel channel share a common ac-coupled bus. Maintenance procedures may sometimes require removal of a DBS from service. If the DBS accidentally outpulses on the ac bus during power-down for removal from service, or during power-up for restoral to service, bus faults may result. To avoid this problem, power to the DBS logic and to the bus drivers is applied and removed in sequence. This sequencing of power to the DBS is provided by an FC402 power sequencer (PS) circuit pack in the DBS housing. A front panel on the circuit pack provides a 4-pole, double-throw, toggle switch for power ON/OFF. Also provided are five LED indicators (for indicating mode of operation and power) and a switch for testing the LEDs.

5.41 Power output of the converters supplying the DBSs may be turned on and off via a remote shutdown feature. Some converters require a normally open switch contact, and others require

PH	15	14	13	12	11	10	9	8	PL	7	6	5 4 3 2 1 0
-	OTHER DMAR	MY DMAR	DEV INTP	DEV DMAR	OTHER ON/OFF	MY ON/OFF	OTHER DEV/DBS	MY DEV/DBS	-	OTHER CLOCK CHECK	MY CLOCK CHECK	MY ADDRESS (3-OUT-OF-6 CODE)

Fig. 32—DBS Status Word Format Description

a normally closed switch contact across the shutdown (R) and shutdown return (S) leads to the converter. The PS directly controls either type of converter through its remote shutdown feature, and a single 26-gauge twisted pair lead connecting the shutdown terminals to the backplane of the DBS. The PS terminals R0 and S0 provide control to a normally closed shutdown pair while terminals R1 and S1 provide control to a normally open pair.

5.42 Operation of the ON/OFF switch on the PS panel applies a closure across R1 and S1 terminals and open circuit across R0 and S0 terminals. This action enables the converter, whether its remote shutdown is normally open or normally closed, and applies +5 volts to the DBS. The +5 volts is applied to an RC network which begins charging toward the applied voltage. Upon reaching an appropriate level, the charge on the network operates a relay. Time constant of the network is such that approximately 2 seconds of delay is provided from initial application of +5 volts to operation of the relay. The bus driver power is switched on and off by a pair of normally open contracts on the relay and is, therefore, applied to the DBS approximately 2 seconds after application of +5 volts logic power.

5.43 Initial +5 volts power is also applied to a second RC network which, after a short delay, operates two additional relays. Normally open contacts on one of these relays apply a parallel closure across the R1 and S1 remote shutdown leads, while normally closed contacts on the second relay reinforce the open circuit across the R0 and S0 leads. Operation of the ON/OFF switch to the OFF position immediately removes +5 volts from the BUSPWR leads and simultaneously applies a discharge path for the second RC network. Time constant of the network discharge path is such that the two relays providing remote shutdown action are held operated for approximately 2 seconds and thereby prevent an immediate change in state of the remote shutdown leads. When the network voltage decays to a sufficiently low level, the relays are released. Release of the relays returns the remote shutdown leads to a normal state, thereby turning off the +5 volt power to the DBS. The bus driver power is, therefore, removed approximately 2 seconds to removal of +5 volt logic power during power-down of the DBS.

E. Maintenance

5.44 Maintenance procedures for the DBS reply on built-in fault detection techniques and software diagnostic routines. The DBS contains no adjustments and no test points for local monitoring. The DBS has no audible or visual alarms. Visual indicators on the power sequencer panel indicate mode of operation and power on. A power converter alarm indicates when the DBS unit is not powered. All circuit packs in the DBS are plug-in units and are replaceable.

5.45 In a DBS, ON (MAINTENANCE) mode, the DBS to peripheral device interface is blocked, and the DBS becomes a terminating device on the ac bus. The DBS responds to all properly addressed instructions from the 3A CC in this mode. All signal leads on the subparallel channel to DBS interface are checked, and the DBS receivers, drivers, and control circuits are verified through exercising the DBS by the 3A CC. Under maintenance program control, the 3A CC can perform the following maintenance functions on the DBS:

(a) Initialize and switch control states of the DBS

(b) Monitor status of the DBS

(c) Loop around a 16 plus 2 parity bit data word from the ac bus, through the DBS receivers and drivers, and back onto the ac bus

(d) Cause the DBS to transmit an all ones data word in response to ACKI and the maintenance address

(e) Command the DBS to transmit an interrupt signal

(f) Activate the DMAR signal with a command, and deactivate the signal with a subsequent DP, DR, or INIT

(g) Cause the DBS to generate ERROR, NOTBSY, and SYNC signals.

When switched to a DEV, ON (NORMAL) mode, the DBS becomes functionally transparent to the communications path between the 3A CC and the peripheral device. The DBS-to-DEV interface is

then verified through maintenance tests on the peripheral device.

6. CTI/POWER UNIT

INTRODUCTION

6.01 The collector diffusion isolation to transistor-to-transistor interface/power unit (CTI/power) provides the logic level shifting between 3-volt CDI integrated circuits used in the 3A CC and 5-volt TTL integrated circuits used in the DMA and PCH units. In addition the CTI/power unit contains three type 132M power supplies which provide 5-volt power to the DMA, PCH 0, and PCH 1, as well as fuses and power alarm circuits (Fig. 33 and Fig. 34).

6.02 Inputs to the CTI/power unit are gated from registers R9 and R10 in the 3A CC by miscellaneous decoder crosspoints (see Section 3 of this document). Logic levels of these inputs are shifted to the higher level required by the DMA and PCH and placed on the DMA and PCH input bus.

6.03 Information being returned from the DMA and PCH to register R11 in the 3A CC is shifted to lower voltage levels (required by the 3A CC) in the CTI/power unit and gated onto the 3A CC register R11 gating bus.

6.04 The CTI/power unit requires +3 volt power which is supplied by a 3-volt dc-to-dc converter located in the 3A Processor frame power unit. When a DMA unit is installed, the 132M power supply which provides +5 volts for the DMA also supplies the required +5 volts for the CTI/power unit. In installations that do not require the DMA, the +5 volts required by the CTI/power unit is furnished by the PCH 0 +5 volt power supply.

A. Physical Description

6.05 The CTI/power unit is positioned above the 3A CC on the 3A Processor frame and installed via an 8 inch by 23-1/2 inch mounting plate. The mounting plate (upper portion) has three positions dedicated to 132M type power supplies used not only by PCH 0, but also by PCH 1 and the DMA (if equipped). These power supplies are plug-in types with connectors mounted on the rear of the mounting plate. The mounting plate lower right corner holds the five fuse blocks providing power fusing. Adjacent to the fuse blocks (on the left) are two type AK-44 relays used in the alarm circuit. A contactor (high current relay) is provided for bus power. The CTI/power unit is mounted in the lower right corner of the mounting plate using an 80C apparatus housing. The 1A connectors are mounted on the 80C housing to accommodate the circuit packs that comprise the CTI/power unit. These connectors are inserted into an MLPWB which is mounted on the rear of the apparatus housing.

6.06 The CTI/power unit contains the following types of circuit packs:

- FC403 3-volt reference and filter circuit equipped with fuse alarm relays
- FA1211 CDI-TTL interface circuit
- FA1212 CDI-TTL interface circuit
- FA1213 CDI-TTL interface circuit.

B. Interfaces

Power Supplies

6.07 The power supplies receive -48 volts from the 3A Processor frame power. Each power supply output voltage (+5 volts) and SENSE leads are connected to the unit which it serves. The +5 volt outputs to the designated units are fuse protected.

Circuit Packs

6.08 The FC403 circuit pack receives power (+3 volts) from the +3 volt converter mounted in the power unit at the bottom of the processor frame via the MLPWB and associated cabling. All other inputs to the FC403 are from the CTI/power unit.

6.09 Circuit packs FA1211, FA1212, and FA1213 are connected to the 3A CC via tape cable (bus) and connected to the input/output unit (PCH or DMA) it is assigned via tape cable (bus). These tape cables are attached to the CTI/power unit (MLPWB) using 942-type connectors. Inputs from the 3A CC to CTI/power unit are gated out of the 3A CC registers R9 and R10 via the bus. Outputs from the CTI/power unit to the 3A CC

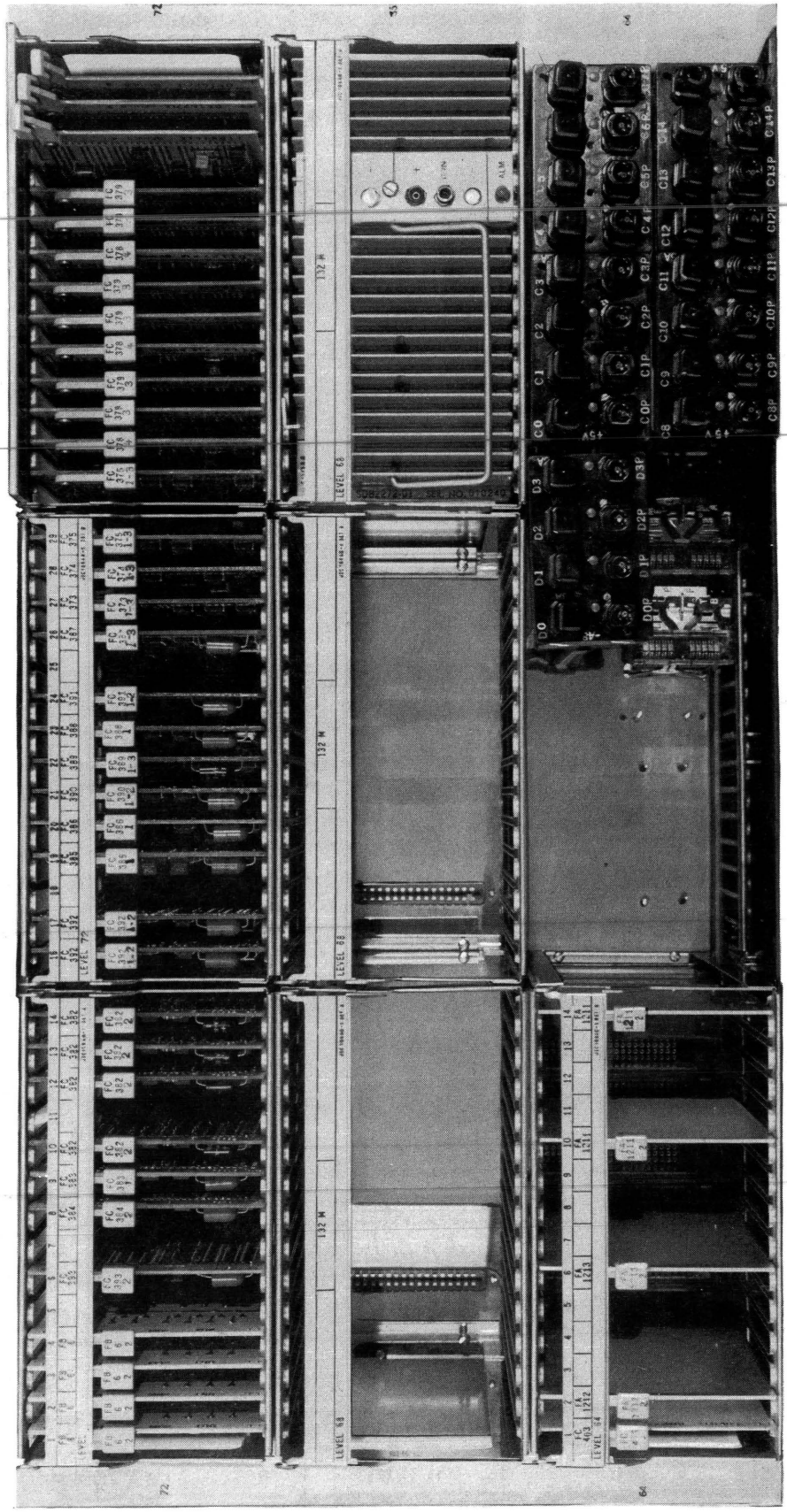


Fig. 33—CTI/Power Unit

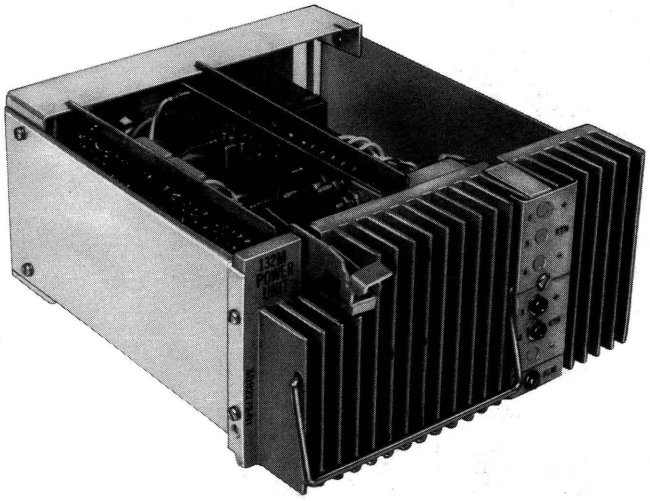


Fig. 34—132M Power Supply

are transmitted via bus to the 3A CC register R11.

C. Functional Description

6.10 The CTI/power unit consist of the following circuit packs:

- One FC403 3-volt reference and filter circuit equipped with fuse alarm relays
- One FA1213 CDI-TTL and TTL-CDI interface circuit
- One FA1212 CDI-TTL and TTL-CDI interface circuit
- Two FA1211 TTL-CDI interface circuit.

FA1213, FA1212, and FA1211

6.11 The FA1213, FA1212, and FA1211 CTI circuits are used to convert CDI signals from 3A CC to TTL signals required by the PCH unit or the DMA. Also, FA1213 and FA1212 circuit packs convert TTL signals from the PCH unit or the DMA to CDI signals required by the 3A CC. (See Table H.) This logic level conversion is accomplished using two different types of logic gates in series. The TTL gate operates on +5 volts while the CDI gate operates on +3 volts.

FC403

6.12 The FC403 3-volt reference and filter circuit equipped with fuse alarm relays provides reference and sense inputs for the 3-volt dc-to-dc converter in the processor frame power unit. Also, FC403 provides filter capacitance at the load for one power converter (up to 4 amperes). Filters made up of ten capacitors connected in parallel reduce the series resistance. The fuse alarm relays mounted on FC403 are used by the CTI/power unit fuse alarm system.

TABLE H

CTI/POWER CIRCUIT PACKS INPUT/OUTPUT

CIRCUIT PACK	INPUTS	INPUT LOGIC LEVEL	OUTPUTS	OUTPUT LOGIC LEVEL
FA1213	3A CC (6)	CDI (3V)	PCH or DMA	TTL (5V)
	PCH or DMA (18)	TTL (5V)	3A CC	CDI (3V)
FA1212	3A CC (12)	CDI (3V)	PCH or DMA	TTL (5V)
	PCH or DMA (10)	TTL (5V)	3A CC	CDI (3V)
FA1211 (2)	3A CC (16)	CDI (3V)	PCH or DMA	TTL (5V)

D. Theory of Operation

6.13 The FA1213, FA1212, and FA1211 use two series gate circuits to convert CDI signals to TTL signals. Also, FA1213 and FA1212 use two series gate circuits to convert TTL signals to CDI signals. The basic difference between the circuit packs is the number of signals it can handle, plus the fact that FA1211 only converts CDI logic to TTL logic.

CDI Logic Level to TTL Logic Level Conversion

6.14 The CDI signal from the 3A CC is buffered and inverted by a 137N integrated circuit pack (ICP) (Fig. 35). A 470-ohm resistor connected to the output of the 137N inverter is used to pull up the open collector output. This output is applied to the input of a 227A ICP (chip version of WECo 41BS) which inverts the input signal (from the 137N) and transmits the signal at TTL level to the PCH unit or DMA.

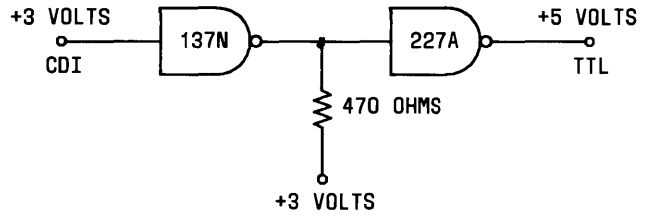


Fig. 35—CDI to TTL Logic Conversion

TTL Logic Level to CDI Logic Level Conversion

6.15 The TTL signals from the PCH unit or DMA are buffered and inverted by ICP 227A inverter. The output of the 227A inverter is applied to the input of ICP 137J (the internal input pull up of the 137J pulls up the output of the 227A) (Fig. 36). The 137J inverter inverts the signal and transmits it to the 3A CC as a CDI level signal.

Fig. 36—TTL to CDI Logic Conversion

FC403

6.16 The functions and theory of operations of FC403 circuit pack are covered in detail by Section 254-300-140.

E. Maintenance

6.17 The CTI/power unit is treated as part of the input/output channel and does not incorporate internal maintenance functions. When the CTI/power unit malfunctions, it is reported as an input/output channel failure and the appropriate action is initiated.

6.18 Maintenance of the power and alarms circuits is described in Section 254-300-140.

7. RSI UNIT

INTRODUCTION

7.01 The RSI unit is a serial line controller which interfaces the 3A CCs using a DBS on a PCH or an SPI on an SSCH, with any peripheral device having an interface that conforms to the EIA/RS232C standard for asynchronous serial data transfer. Examples of peripheral devices that can be interfaced to the 3A CC via the RSI unit are:

- 202 Series data sets
- Local TTY terminals (including those that have higher performance capability than the Model 33 and Model 35 TTY)
- Remote TTY terminals over voice grade lines interfaced by modems (modulator-demodulators)
- Remote TTY terminals that share voice grade lines into the 3A CC on a dial-up basis. The RSI unit provides auto-answer capabilities for the 3A CC to respond to the incoming call
- Other processors via dedicated or dial-up lines
- Variety of low speed peripheral devices such as line printers and card readers.

The RSI has 16 programmable baud rates provided (all under software control). These rates are: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000,

2400, 3600, 4800, 7200, 9600, and 19,200. This rate is selected by the 3A CC software, using four command bits.

7.02 The RSI unit can be program driven in either half-duplex or full-duplex (simultaneous send and receive) mode.

7.03 The RSI unit consists of a serial parallel interface unit (SPI4), a bus terminator (BT4), a regulator circuit, and up to four RSI channel circuits.

7.04 When the RSI unit is interfaced to the 3A CC via the serial channel, the SPI4 circuit is used. However, when the RSI unit is interfaced to the 3A CC via the parallel channel, the SPI4 and BT4 circuits are not required. This is because the interface to the parallel channel is via a DBS which provides the parallel channel needed for the RSI circuits.

7.05 The RSI has two interrupt capabilities which can be enabled or disabled independently under 3A CC (program) control. Both interrupts activate the same interrupt lead on the DBS/SPI. One is the character interrupt, which occurs (if enabled) when a character has been received or when the transmit side is ready to accept another outgoing character. The other interrupt (status) signals any change in any of the six incoming RSI status lines. Separate enable control allows for use of no interrupts, both interrupts, or polling for characters.

7.06 When receiving, the RSI gives status information to the 3A CC with each received character byte. Most of this status refers to the quality of the character it accompanies, but one status bit signals RSI status changes.

7.07 The transmit and receive sides each have a 64-character queue buffer. These buffers permit longer polling intervals.

7.08 When several RSI circuits share one DBS or SPI4, the RSIs are enabled by the 3A CC one at a time to transfer data.

A. Physical Description

7.09 The basic RSI unit (one RSI channel circuit only) utilizes plug-in circuit packs as follows:

- SPI4 circuit—FC381, FC394, and FC395
- BT4 circuit—FC396 and FC397
- Voltage regular circuit—FC380
- RSI channel circuit—FC376 and FC377.

7.10 The circuit packs that compose the RSI unit are mounted in a front-removable 80C 14-card apparatus housing (Fig. 37).

7.11 The RSI unit is mounted on office equipment frames designated by the operating company, based primarily on space availability and proximity.

B. Interfaces

Serial Channel

7.12 Three coaxial leads connect the RSI unit (SPI4) to the 3A CC serial channel. These leads are designated send (S), receive (R), and interrupt (I). The RSI unit is interfaced to the peripheral device via remote lines.

Parallel Channel

7.13 The RSI unit is interfaced to the 3A CC via an SPI4, the parallel bus provides the signal path between the RSI unit (RSI channel circuit) and the SPI4. The RSI unit is interfaced to the peripheral device as described in paragraph 7.08.

Parallel Bus Structure

7.14 The parallel bus structure extending from the SPI4 to the BT4 and the RSI channel circuits is a master-slave arrangement. The 3A CC via the SPI4 is the master. Peripheral devices must gate data onto the information leads only during sense status or send-data cycles. WAIT and SYNC are response leads and must be activated only in response to a command state from the SPI4.

7.15 The parallel bus consists of 6 address leads, 18 information leads, 8 command leads, and 5 reply leads (Fig. 38).

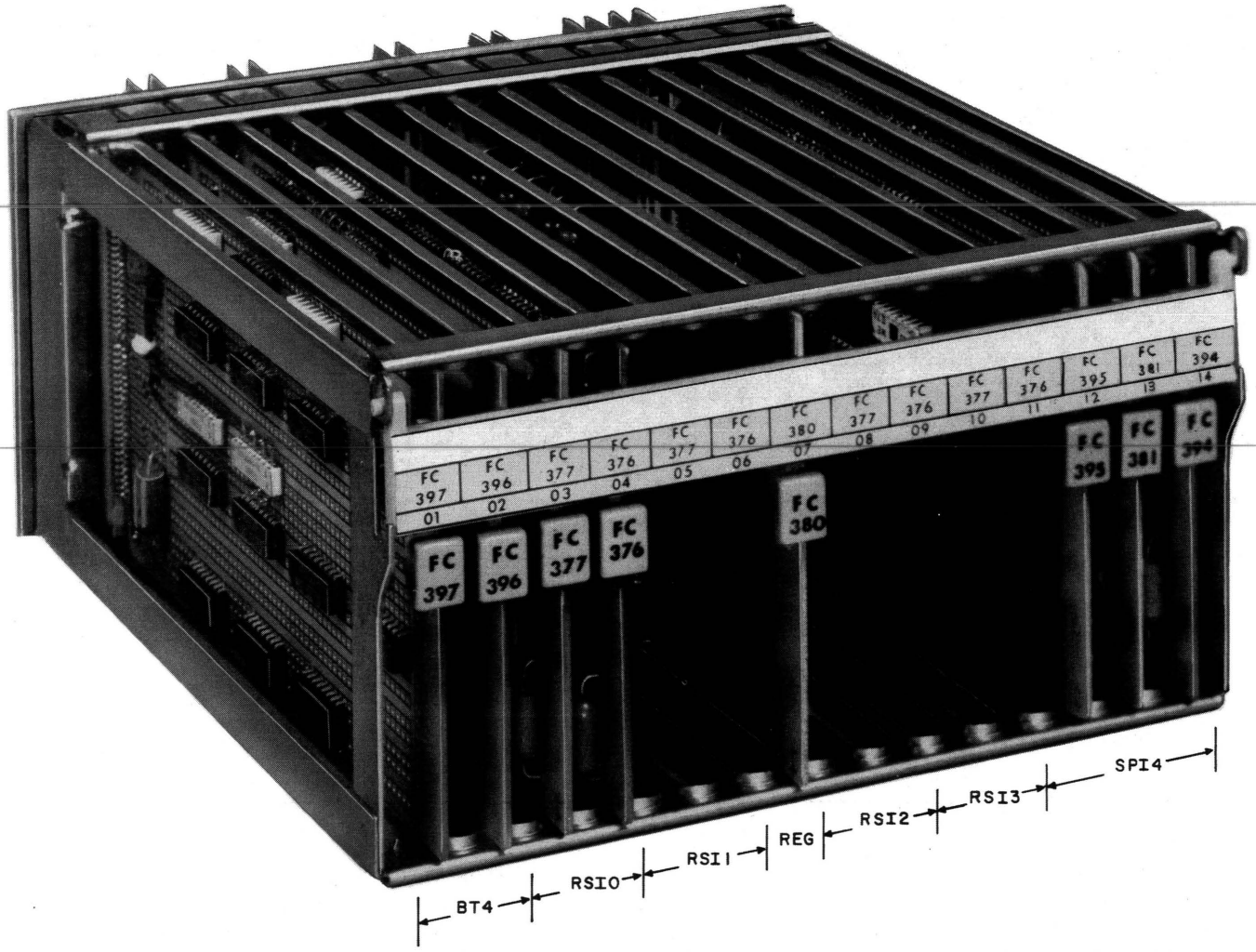


Fig. 37—RSI Unit Equipped With RSI0 and Regulator Board

7.16 Intra-unit wiring within the RSI unit is via 30 AWG wire and power is distributed via the multilayer back plane wiring board.

C. Functional Description

7.17 The RSI unit is comprised of four circuits:

- Serial peripheral interface (SPI4)
- Bus terminator (BT4)
- RSI channel circuit (RSI Ch 0 through 3)
- Voltage regulator (REG).

Communication Time States

7.18 The basic communications between the 3A CC and a peripheral device can be separated into five time states:

- Serial receive
- Parallel send order
- Parallel get reply
- Serial send
- Idle.

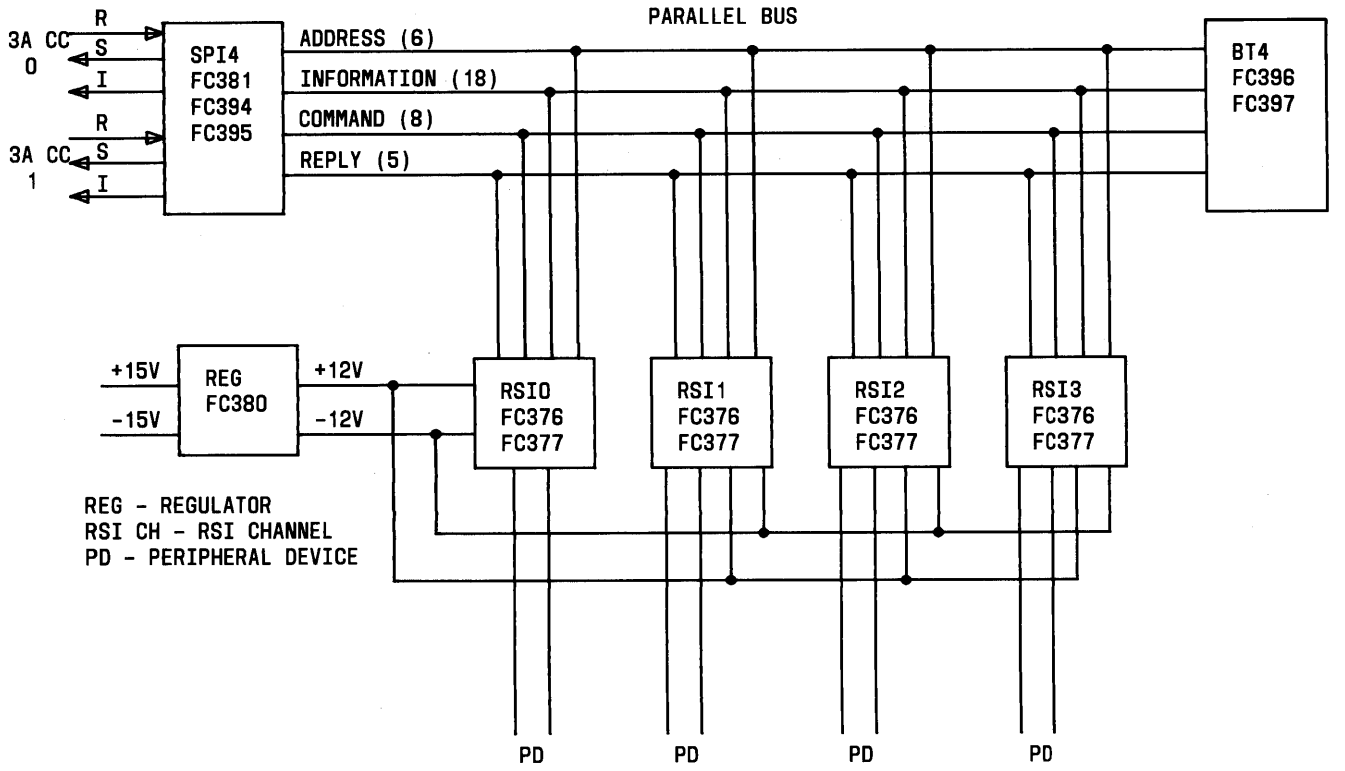


Fig. 38—RSI Interface

Serial Receive

7.19 The 3A CC sends a 21-bit bipolar message (3-bit start code, 8-bit low data byte, low data parity bit, 8-bit high data byte, and high data parity bit) over the serial channel at a rate of 6.67 MHz. The first bit of this message (start code) is always a one. This bit is used to indicate that the message has been fully shifted into the SPI4 21-bit shift register. When the first bit (1) is in the least significant bit position of the shift register, the serial receive time state is complete. The 3A CC continues to send a zero bit stream to the SPI4 until a reply is sent to the 3A CC.

Parallel Send Order

7.20 Eighteen data bits of the 21-bit message in the shift register (SPI4) are gated onto the parallel bus. The 3-bit start code is decoded to determine whether the information in the 18-bit message is a command or data for a peripheral device. (A 101 start code signifies the message is a command, a 011 start code signifies the message is data.) Some of the commands are sent to the SPI4 to create control signals. Others are sent to the peripheral devices. The SPI4 determines (from address information within the 18-bit data message) which commands are to be directed to the peripheral devices. For these messages, the SPI4 creates a receive command control signal (RC0) and gates the command information onto the information leads during this time state. Each RSI circuit uses the RC0 signal to examine the message on the parallel bus to determine if it is addressed. The addressed device responds to the SPI4 over a response lead (SYNC0) to indicate that it has received the message. When the start code indicates data is present, the SPI4 creates a receive data control signal (RD0) during this time state. A peripheral device that had been previously directed via command signal to receive data uses the RD0 signal to gate the data from the information leads. The peripheral device signals the SPI4 using the SYNC0 lead that the data has been received. The SYNC0 signal is used by the SPI4 to terminate the parallel send order time state.

Parallel Get Reply

7.21 During this time state, a peripheral device uses the parallel bus to reply to the SPI4.

The SPI4 sends a command directing the peripheral device to return a send status (SST0) or send data (SD0) reply. The addressed peripheral gates the 18-bit reply onto the information leads and responds by activating SYNC0. The SPI4 uses SYNC0 to gate the reply message on the information leads into the 21-bit shift register, and the timing state is terminated.

Serial Send

7.22 The SPI4 takes the 18-bit data message from the 21-bit shift register with appropriate generated start code and returns this message to the 3A CC. The zero bit stream from the 3A CC is used to create the timing sequence to return this message to the 3A CC. When the 3A CC receives the message, the zero bit stream will stop and serial send timing state will be terminated.

Idle

7.23 No communication between the 3A CC and the SPI4 is occurring during this state. The idle time between successive orders and replies is at least 1 microsecond long. The SPI4 control states are reset during this time.

Signal Lead Description

7.24 Negative logic is used on all parallel bus leads. On the data leads, a high level designates a logic 0 and a low level designates a logic 1. On the control and response leads, a low level indicates active and a high level indicates removal of the signal on a given lead. The bidirectional data leads are designated INF000 through INF150. These leads are used to transfer 16-bit words from the SPI4 to a device or the BT4. Sixteen-bit words can also be transferred from the BT4 or a device to the SPI4. Two leads are used to transmit parity bits along with the data word. The INFPL0 is the low parity bit associated with the low byte. The INFPH0 is the high parity bit associated with the high byte. Parity is odd over each half-word.

7.25 The INF000 corresponds to bit 0 in a register in the 3A CC. The INF150 corresponds to bit 15 in a register in the 3A CC. On a message received from the 3A CC, INF000 corresponds to the first bit received after the 3-bit start code. On a message returned to the 3A CC, INF000 corresponds to the first bit being sent after the 3-bit start code. In the serial message INFPL0 and INFPH0 follow bit 7 and bit 15 of the data, respectively.

7.26 The following signals generated by the SPI4 are used to control and time commands, data, or status appearing on the information leads:

(a) ***RC0—Receive Command:*** The SPI4 received a message with a start code of 101. The RC0 is generated during a parallel send order time state to request a device to receive a command from the SPI4. The information leads should contain a 3-out-of-6 device address code on INF000 through INF050, and a 10-bit command on leads INF060 through INF150. Some particular command codes contain a 3-out-of-6 device address defined to be that of the SPI4. These particular commands, used to activate control signals, do not result in the generation of the RC0 signal.

(b) ***RD0—Receive Data:*** [Functionally equivalent to DP in the DBS.] The SPI4 receives a message with a start code of 011. The RD0 is generated during a parallel send order time state to request a device to receive a data word from the SPI4. The bit configuration on leads INF000 through INF150 is recognized by the SPI4.

(c) ***SST0—Send Status:*** [Functionally equivalent to sense status in the DBS.] The SPI4 requests the addressed device to place a status word onto the information leads during the parallel get reply time state. The status word should contain the 3-out-of-6 device code representing the addressed device on INF000 through INF050, and other device status information on leads INF060 through INF150. The 2 parity bits INFPL0 and INFPH0 must also be supplied by the device. The configuration of the 18-bit reply is recognized by the SPI4.

(d) ***SD0—Send Data:*** [Functionally equivalent to DR in the DBS.] The SPI4 requests the addressed device to place a 16-bit data word with proper parity onto the information leads. The format of the 18-bit reply is decoded by the SPI4 and appropriate action taken. The SD0 is sent during a parallel get reply time state.

(e) ***ACKI0—Acknowledge Interrupt:*** This lead is used to identify the devices which are requesting interrupts. When ACKI0 is activated, each of the devices which are requesting interrupts sets a predefined information lead to 1. When the 3A CC receives the reply from SPI4, the devices which are requesting interrupts can be identified by the set bits of the reply. The ACKI0 results during a parallel get reply time state as a result of a command which uses the special SPI4 3-out-of-6 device address.

(f) ***INIT0—Initialize:*** The SPI4 commands all devices connected to the bus to assume a known state. All device address flip-flops then reset. The INIT0 results during a parallel get reply time state as a result of a command which uses the special SPI4 3-out-of-6 device address.

(g) ***CLK—Clock:*** The SPI4 provides a free-running clock to peripheral devices. This clock is derived out of the serial channel bitstream and therefore will only be present when the 3A CC is communicating with the SPI4. The clock frequency is one-fourth the serial channel repetition rate, or a nominal 1.67 MHz pulse train with 300 nanoseconds per level. There is no guaranteed relationship between the clock phases and command state timing.

7.27 The following signals are generated by the devices to indicate to the SPI4 or BT the operation to be performed with timing or information:

(a) ***SYNC0—Synchronization:*** SYNC0 is a response to command states set up by the SPI4. A device asserts SYNC0 only in response to an RC0 command if the device has decoded its identity from the information leads. A device activates SYNC0 only in response to RD0 or SD0 command states if the device is designed to accept and supply data words. Also in order to allow multiple devices to coexist, a device must respond to RD0, SD0, or SST0 only if previously addressed by a proper RC command. Devices shall not respond with SYNC0 to ACKI0 or INIT0 commands. The bus terminator responds to these two commands to complete the handshaking with the SPI4.

(b) ***WAIT0—Wait:*** WAIT0 is a response from a device during any command state set up by the SPI4. WAIT0 is activated by a device if this device is activating SYNC0 but more than 300 nanoseconds is needed to accept a command.

(c) ***ER0—Error:*** The addressed device activates the ER0 lead to inform the 3A CC that an error condition exists. The SPI4 returns a start code (101) to the 3A CC when ER0 is activated.

(d) ***INTP0—Interrupt Pulse:*** A device activates the INTP0 lead to interrupt the 3A CC. A monopulser in the SPI4 senses the high-to-low transition lead INTP0 and sends a nominal 350-nanosecond wide pulse to each 3A CC.

(e) ***GP0—Generate Parity:*** A device signals the bus terminator to generate parity over the 16-bit reply placed on the information leads by the device. A device may activate GP0 only during SST0 or SD0 command states. The BT clocks the state of the information leads into its 16-bit holding register at the trailing or low-to-high transitions of GP0. This is not used by the RSI circuit.

(f) ***GPR0—Generate Parity Reply:*** The bus terminator responds to the GP0 signal by activating GPR0. The device must remove the signals from the information leads and remove the WAIT0 control signal input. This is not used by the RSI circuit.

SPI4

7.28 The SPI4 consist of three circuit packs:

- FC381
- FC394
- FC395.

7.29 The SPI4 unit is a serial-to-parallel and parallel-to-serial converter. Two serial ports are used to receive 21-bit (bipolar pulses) messages from either 3A CC (0 or 1). Two serial output ports are provided to send the 21-bit reply message to either 3A CC. The transmission path between the 3A CC and SPI4 unit is via coaxial cables (R, S, and I) with transformer coupled drivers and receivers within the SPI4 unit to convert bipolar pulses to TTL logic levels and TTL logic levels to bipolar pulses. Input signals from either of the

3A CCs are received by the SPI4 and ORed into the clock and data recovery circuit. The SPI4 unit handles the serial communication with the 3A CCs and establishes the timing, control, and data signals over the parallel bus to the bus terminator and the RSI channel circuits.

7.30 The SPI4 removes the data from the serial input from the 3A CC as well as two phase clock signals. An additional timing pulse is created to shift the data bits into a 21-bit shift register (input/output shift register-IOB). Reply data to the 3A CC uses the same shift register (IOB) and the output data is gated to the 3A CC via the dedicated output port.

Communication Between the 3A CC and the SPI4 Unit

7.31 The 3A CC sends a 21-bit message to the SPI4 unit via the serial channel. The first bit of this message is always a one (1). This bit sets a latch after it has been shifted into the least-significant bit position of the 21-bit shift register. When the latch becomes set, the received message is locked in the shift register. The 3A CC keeps sending a stream of zeros which provides clock pulses to drive the SPI4 control logic.

7.32 The contents of the shift register determines the action to be performed. A start code (first 3 bits of 21-bit message) of 011 indicates that the 16 data bits in the shift register are to be treated as data. A start code of 101 indicates that the 16 data bits are to be treated as a control order. Bits 0 through 5 of this data identify the device code.

7.33 A timing sequence is started to transfer the 18 bits (low data byte, low parity bit, high data byte, and high parity bit) stored in the shift register to the RSI channel circuit over the parallel bus. The information bits stored in the shift register are gated onto the information (INF) leads. Approximately 150 nanoseconds later the receive command (RC0) lead is activated by the SPI4 circuit. The timing sequence keeps the RC0 lead and the information leads stable in this state. The RSI channel circuit decodes the identity message from the information leads and recognizes the command signal. The RSI channel circuit addressed responds by activating the synchronization (SYNC0) response lead.

7.34 Activation of the SYNC0 lead restarts the SPI4 circuit timing. At the trailing edge of the RC0 command, the 4-bit control register is loaded with send status-SST0 (0001) data. Approximately 150 nanoseconds after RC0 goes high, the SPI4 circuit gates itself off the information leads. (Note: The information leads are stable over the entire duration of the RC0 command state, permitting the RSI channel circuit to clock information from the parallel bus into a register on either edge of the RC0 command.) The SPI4 circuit timing sequence is stopped and waits for a response from the address peripheral device via the RSI channel circuit. The proper reply must be for the addressed device to release the SYNC0 lead. When the SYNC0 lead goes high, the timing sequence will activate the send status (SST0) command lead. The addressed device must again respond by activating the SYNC0 lead and gating a 16-bit reply with correct parity onto the information leads as long as SST0 is activated.

7.35 The reply data from the peripheral device should contain the device code and status information. Approximately 300 nanoseconds after the SPI4 has recognized the high-to-low transition on the SYNC lead, the data on the information leads is gated into the shift register and control signal SST0 is removed. The RSI channel circuit must respond with the releasing of the SYNC0 signal and gating itself off the information leads. The SPI4 will test the error (ER0) lead after the low-to-high transition of the SYNC0 signal following the trailing edge of the get-reply command. If the ER0 lead is not activated, SPI4 sends the start code (011) and the peripheral device reply now stored in the shift register to the 3A CC.

7.36 The ER0 signal is activated during the error check time the SPI4 goes through an additional timing cycle to change the start code (from 011 to 101). Twenty bits of the 21-bit shift register are contained in five dual in-line package ICs. To perform a parallel-load operation, all 20 bits must be clocked at the same time. To change the two start code bits without losing the peripheral device reply already stored in the shift register (18 bits), the information is gated back onto the information leads so that the information appears on the input (parallel) of the shift register. After the parallel bus stabilizes, all 20 bits are clocked into the shift register. The SPI4 now gates itself off the information leads and sends peripheral device reply and start (101) to the 3A CC.

7.37 The same sequence is used to send a control order and status reply to the 3A CC. The difference being the start code (011) results in the receive data command lead being activated by the SPI4.

Acknowledge Interrupt, Initialize, Send Data, and Send Status Command States

7.38 The SPI4 decodes the 000111 device code as its own address code when the message received from the 3A CC is preceded by start code 101. The timing sequence in the SPI4 always follows the same sequence. Two time states within SPI4 (designated T1 and T3) are used as send order and get reply timing sequences when the SPI4 recognizes its own address code, it generates SYNC for the T1 cycle and transfers the upper 4 bits in the shift register into the 4-bit command register. The contents of the shift register are not gated onto the information leads nor is the receive command lead activated.

7.39 After the SPI4 has replied with the SYNC signal to move the timing sequence through the T1 cycle, the 4-bit command register data is gated onto the command leads. (All 16 combinations can be generated by software control.) During T3 cycle, one or more of the command leads becomes activated. For sense status or send data, the addressed device must reply with a SYNC signal and must gate valid status or data onto the information leads. For acknowledge interrupt and initialize, only the BT4 responds with SYNC and WAIT signals.

7.40 When the SPI4 issues a control signal to peripheral devices, the control signal will remain on the leads as long as there is no reply from the peripheral device. If a wrong device address code is issued by the 3A CC there will be no serial reply to the 3A CC. If this error condition occurs due to software error, the 3A CC responds by stopping data to SPI4, which causes SPI4 to reset the command control leads.

WAIT

7.41 The WAIT control lead provides for asynchronous communication between SPI4 and peripheral devices. The SYNC0 lead must be activated by the addressed peripheral device in response to any control state set by SPI4. If the device responds to the leading edge of a command state within a few gate delays, the minimum width of the command state is two 3A CC clock cycles (approximately 300 nanoseconds). However, if the device is not ready to accept the command or more time is required to accept the command, the device can activate WAIT0 response lead. The WAIT0 lead being activated overrides SYNC reply and SPI4 holds the command state as long as WAIT0 is activated. For WAIT function to operate properly for slow responding devices, the leading edge of WAIT signal must occur 15 nanoseconds before the leading edge of SYNC signal.

7.42 The WAIT function can be used during the send order and get-reply timing cycles. A peripheral device can thereby get additional time to process a command, but WAIT is not to be used for long time response.

Parity

7.43 The SPI4 checks the 21-bit serial message for serial parity errors as the message is shifted into the shift register. A toggle flip-flop checks for an even number of ones over the first 21 bits of the message. If the message has correct parity, the normal command timing is started. However, if a parity error exists, the normal command timing is inhibited and an error reply message is returned to the 3A CC. The reply message for parity error consist of the 101 start code and data bits 0, 1, 2, and 8 set to ones and the SPI4 device address.

Bus Terminator (BT4)

7.44 The BT4 is comprised of two circuit packs:

- FC396
- FC397.

7.45 The BT4 is located at the end of the parallel bus and contains a 16-bit register. The BT4 can be addressed with proper start code (101) and data bits 0 through 5 being all zeros or ones. Bits 6 through 15 may be any configuration. The 16 bits of the data (order) are stored in the register and the BT4 address flip-flop is set. The SPI4 automatically sends send status (SST) command following the control order used to address BT4. The BT4 responds to SST signal with contents of the 16-bit register. As long as BT4 address flip-flop is set, BT4 also accepts receive data orders from

the 3A CC and stores the 16-bit data word in the holding register. The automatic SST command following the receive data order also returns to the 3A CC the 16-bit data word stored in the holding register. Data stored in the holding register may also be retrieved by SST command while BT4 address flip-flop is set. Since BT4 is used in this manner for maintenance type operations, it activates the error lead (ER0) whenever it is addressed. This causes SPI4 to issue a start code (101) with all BT4 replies to the 3A CC. The BT4 does not respond to the send data command. The addressing feature of the BT4 permits the 3A CC to verify SPI4 operation and information leads of the parallel bus.

Parity Generation by BT4

7.46 A peripheral device which does not have a parity generator for information to be sent to the 3A CC during the send status and send data control states can have parity generated by parity circuits within BT4. The 16-bit register in the BT4 is used as a temporary storage register. Outputs of the register are gated into two 8-bit parity circuits. Resulting parity bits (P_L and P_H) and outputs of the register can then be gated onto the information leads.

7.47 Generate parity (GP0) lead and generate parity reply (GPR0) lead are used as handshaking (for synchronization) leads between peripheral devices and BT4. Both leads are connected between SPI4 and BT4. A device requiring parity to be generated during the send status or send data commands follows this sequence: SPI4 activates send status or send data command leads. The addressed device activates SYNC0 and WAIT0 control leads. The device activates GP0 for approximately 200 through 300 nanoseconds. While GP0 is activated, the device gates 16 bits of data onto the information leads. The BT4 recognizes GP0 and activates WAIT0 lead in response to the leading edge of GP0. At this time, both BT4 and the device are activating the WAIT0 signal. At the trailing edge of GP0, BT4 clocks the data on the 16 information leads into BT4 holding register and after several gate delays activates GRP0. The device must respond by gating the data off the 16 information leads and removing WAIT0 control output signal. Now only BT4 activates the WAIT0 command. The BT4 gates the register and parity data onto the information leads and parity leads. The BT4 then removes the WAIT0 command. The SPI4 recognizes the removal of WAIT0 command and clocks the data on the information leads into the 21-bit shift register and then removes SST or send data control signal. The device responds by removing SYNC0 signal; BT4 responds by removing GPR0 and gating itself off the information leads.

Acknowledge Interrupt

7.48 Only BT4 responds to the acknowledge interrupt (ACKI) command with SYNC and WAIT signals. A device which sends a pulse on the demand interrupt lead (INTP0) gates its acknowledge interrupt reply bit onto the assigned information lead. The device must remove its reply data when the BT4 generates GPR0. The BT4 gates the data on the information leads into its holding register and activates GPR0 lead. Data from the holding register (16 bits) and parity circuits (P_L and P_H) is gated onto the information leads, and WAIT is removed. The SPI4 gates data on the information leads into the 21-bit shift register and removes ACKI. The BT4 then removes SYNC and the output of the holding register from the information leads.

Initialize

7.49 Only BT4 responds to initialize (INIT) command with SYNC and WAIT signals activated. All devices go to a predefined state and reset their address flip-flops. (The INIT pulse is a minimum of 300-nanosecond duration.) The BT4 generates GPR0 during INIT command. (GPR0 inhibits outputs from devices onto the information leads.) The BT4 gates data on the information leads into the holding register, then outputs of the register and parity circuits are gated onto the information leads. The BT4 then removes WAIT; this notifies the SPI4 that a reply is ready. The SPI4 gates data on information leads into the 21-bit shift register and removes INIT. The BT4 removes SYNC and gates itself off the information leads. The SPI4 checks the ER0 lead and if ER0 is not set, sends a start code (011) and the all zeros reply with correct parity to the 3A CC.

7.50 The BT4 also provides the termination for the information leads and command leads.

RSI Channel Circuit

7.51 Each RSI channel is comprised of two circuit packs:

- FC376 (Low data byte)
- FC377 (High data byte).

7.52 The RSI channel circuit is the interface between the parallel bus and the peripheral device; it is also somewhat of a peripheral controller. Parallel information is gated into the RSI channel from the parallel bus, TTL logic levels are changed to EIA logic levels, and information is outputted to the peripheral device as serial data.

7.53 The RSI channel receives serial EIA logic level signals from the peripheral device, converts these signals to TTL logic levels, and outputs the data in parallel onto the parallel bus. The RSI channel operates under control of the SPI4 and BT circuits (directed by the 3A CC).

7.54 Low-byte data from the parallel bus is gated into FC376 (bits 0 through 7) and the high-byte data is gated into FC377 (bits 8 through 15). The FC376 contains an oscillator that provides timing of the serial output via software control. The RSI channel also provides a parity check on the input data.

Voltage Regulator (REG)

7.55 Voltage regulator circuit (FC380) is an optional circuit pack to convert unregulated positive and negative 15-volt supply to a regulated positive and negative 12-volt supply used by the EIA drivers. The voltage regulator also provides filtering and no load protection for the regulated 12-volt output.

D. Theory of Operation

7.56 The following list contains the circuits that comprise the RSI unit, the circuit packs that comprise the circuit, and the necessary drawings to follow the theory of the circuit pack.

- SPI4
  FC381 CPS-FC381
  FC394 CPS-FC394
  FC395 CPS-FC395
- BT4
  FC396 CPS-FC396
  FC397 CPS-FC397
- RSI Channel
  FC376 CPS-FC376
  FC377 CPS-FC377
- Voltage Regulator (REG)
  FC380 CPS-FC380

SPI4 Circuit

FC381

7.57 The FC381 contains a 6-bit latch circuit which stores the address of the last device on the parallel bus which the 3A CC communicated. Mainly, the FC381 SPI4-A circuit pack provides buffer receivers (18) and open collector bus drivers (18) for the information (18) leads. The information (INF) leads are used for the transmission of the low data byte (0 through 7) and the low parity bit (P_L) also the high data byte (8 through 15) and the high parity bit (P_H). The FC381 also provides termination (resistive voltage divider) for each of the information leads. Gate information lead (GINF0) when low gates the bus drivers to the ON state.

7.58 When a parity error is detected, information leads (bits) 0, 2, and 8 are placed at ground level by lead SPER1 going to the high (1) state. This signal format is returned to the 3A CC as the parity error message.

7.59 The pulse train signals on the RSHPOA lead has a 50 percent duty cycle which drives a retriggerable monopulser (MP1). The leading edge on the first pulse of this signal sets the 1 output of the monopulser (MP1) to the high state (1). If the incoming pulse signal train is interrupted by an interval of approximately 350 nanoseconds, the 1 output of the monopulser is set to the low state (0). This signal transition (1 to 0) triggers monopulser (MP2) to generate a 350-nanosecond wide RESET pulse on the BSD1 and RSETD1 leads used to reset the RSI unit to its original state.

7.60 A low-to-high (0 to 1) transition on the INTERRUPT (INTP0) lead causes demand interrupt signals (2) to be generated (one for each 3A CC). These demand interrupt signals are transmitted to the 3A CC via bus drivers.

7.61 A special power on circuit is used by the FC381. A resistor-capacitor network connected to a Schmitt trigger circuit generates an exponential voltage rise as the logic voltage (+5 volts) is applied to the FC381. As long as input voltage is below the input level to the Schmitt trigger, the output of the Schmitt trigger remains in the high state. This high state output keeps the RESET (RSETD1) line active (1). The serial parallel interface control logic is initialized by this active (1) level.

FC394

7.62 The FC394 serial peripheral interface-B circuit contains a 21-bit shift register [input/output buffer (IOB)] that receives the serial message from either 3A CC via input ports A or B. The input signals received from the 3A CC are bipolar pulses which are converted to transistor-transistor logic (TTL) level. A clock pulse (RSHP1) of approximately 75 nanoseconds is recovered from the incoming bit stream. The recovered data signal (DTAIN1) is held in the stable condition over the trailing edge of the clock pulse (RSHP1).

7.63 The 21-bit input message is checked for parity (odd) errors. A stop latch is set when the first 1 bit is clocked into the least significant bit of the shift register. The shift register contents are locked-in because the register is set into the parallel load mode of operation. The remaining 20 bits of data in the register are available for decoding. The states (low-high) of the 18 information leads and a start code determined by the state of lead 101ST0 are loaded into the shift register on the trailing edge of the pulse signal on the PLIOB0 lead to return the 21-bit message to the 3A CC. The ENR flip-flop enables the reply message modulator (RMM) and places the shift register into the serial shift mode of operation. The data present at the output of the IOB as DTAOT0 modulates the two clock pulses to generate the bipolar pulses (derived from TTL logic) at the A or B output ports.

7.64 A high on the RESET lead (RSETD1) initializes the FC394 circuit. An internal voltage regulating circuit is provided by resistor R13 and diode CR1 which converts +5 volts to +3 volts. This +3 volts is used to convert the bipolar pulses to TTL levels.

FC395

7.65 The FC395 circuit pack provides most of the control functions of the SPI4 unit. These functions include the supervision of the 21-bit shift register (FC394) which receives or transmits the 21-bit message to the 3A CC via serial channel. The FC395 also controls handshaking with RSI channel circuits using the parallel bus (derived from the 21-bit shift register outputs).

7.66 Command information from the 3A CC is fed into the FC395 in parallel on three groups of output leads from the IOB: the start code group (SCB10, SCB20), the device address code group (B000 through B050), and the command group (B120 through B150). A start code of 011 in the 21-bit shift register (FC394) activates the parallel bus command lead RD0 during the T1 timing sequence of FC395. If the SPI4 is not addressed, a start code 101 activates command lead RD0 during the T1 timing sequence. The SPI4 is addressed when an 000111 device address code accompanies the 101 start code during the T1 timing sequence. The 000111 device address code is decoded inhibiting the RC0 signal. An addressed SPI4 activates SYNC0 during T1 timing sequence and clocks the command group information into the command register (COMR) on the trailing edge of T1 sequence. A set bit in the command register activates the corresponding command lead (SD0, INIT0, ACKI0, or SST0) during the T3 timing sequence. The command register SST bit is normally in the set state when the SPI4 is not addressed.

7.67 The sequence arrangement on FC395 can be separated into three timing sequences: send order (T1), get reply (T3), and error sequences. T1 and T3 are controlled by timing generator (TGEN) while the ERTCH circuit controls the error sequence. The TGEN is clocked by the pulse train on the RSHPOA lead. The RSHPOA signals are divided by two to clock the ERTCH circuit and by four to produce bus clock signals on the CLK lead. The TGEN and ERTCH circuits are normally idle in the cleared state also flip-flops ERSA and ERSB. The TEO1 and TEO2 flip-flops are idle in the set state.

7.68 Presence of a 21-bit message (from the 3A CC) in the IOB activates the STOPB0 lead. If SPE1 signal is false (0) at this time, with no serial parity errors indicated, STTG0 signal drives

TGEN serial input high to begin the send order sequence. With TGEN state (Q_C Q_B Q_A = 001) set, this activates GINF0 signal which gates the 21-bit shift register data onto the parallel bus, depending on the received start code. Start code 101 along with the SPI4 address code inhibits RC0 and GINF0 signals, activates SYNC0 signal via SPIY0 gate, and enables command group inputs to the command register. The TGEN state 111 causes the sequencer circuit to stop further action until SYNC0 signal is returned in response to the command signal and WAIT0 signal is inactive. The BANC0 gate ensures that TGEN reaches the 111 state even if SYNC and WAIT signal condition is quickly satisfied in T1 timing sequence. When SYNC and WAIT signals are satisfied, SSTG0 signal is false (0) and TGEN serial input goes low. The TGEN state 111 to 110 transition cuts off T11 (IC6) gate and loads the command register. The next clock pulse clears TGEN circuit, clears TE01 flip-flop and inhibits the GING0 signal. The TGEN circuit marks time in the 000 state until SYNC0 signal is removed.

7.69 The SYNC0 signal goes negative which drives TGEN serial input high and starts the get reply sequence. The TGEN state 011 activates PLIOB0 signal and T31 circuit, gating the command register output onto the parallel bus. The TGEN stays in the 111 state until SYNC and WAIT signal condition is satisfied. The TGEN transition from 111 to 110 state cuts off T31 gate and drives PLIOB0 signal negative, thereby clocking data on the parallel bus into the IOB. The next clock pulse clears TGEN and TEO2 circuits. The sequence circuit waits until SYNC0 is removed. The SYNC0 signal goes negative causing ERSA circuit to become set on the next negative transition of RSHPOA signal. The bus device error lead is checked at this time and ERROR flip-flop latches if ER0 signal is true (1). The next negative transition of the RSHPOA signal sets ERSB circuit. Absence of device errors results in activation of STRTR1 signal which starts return of a serial message to the 3A CC.

7.70 The error sequence is initiated when either a serial parity error or device error occurs. Device errors latch ERL flip-flop following the get ready sequence. The STRTR1 is temporarily inhibited while EERT1 circuit activates 101ST0 signal and forces ERTCH circuit serial input high. The ERTCH first activates the PLIOB0 and GINF0 signals which gates the IOB output onto the parallel bus. The 101ST0 signal forces a 101 start code as the trailing edge of PLIOB0 signal loads the parallel bus data into the IOB. The ERTCH circuit then activates STRTR1 signal to complete the sequence. Serial parity errors occurs when the serial message from the 3A CC is registered in the IOB. A serial parity error activates SPER1 101ST0 signals, starting the error sequence. The ERTCH circuit pulses PLIOB0 lead which loads the 21-bit shift register with the parity error reply message and a start code of 101. The ERTCH circuit then activates STRTR1 signal to complete the sequence. The RSETD1 and RSET1 leads are pulsed to return the sequencing circuit to the idle state once the 3A CC receives the reply message.

Bus Terminator (BT4)

FC396

7.71 This circuit provides handshaking and control logic for the parallel holding register on FC397. Also, it provides far-end terminating resistors for the parallel bus command leads and the serial bus leads.

7.72 The BT4 address flip-flop becomes set at the leading edge of RC0 signal if IB001 through IB051 leads are all ones or zeros. This activates the SYNC0 and CLKR0 signals. The SYNC0 and CLKR0 signals remain low until RC0 signal returns to the high level at the trailing edge of RC0 signal, data on the information leads is clocked into the register on FC397.

7.73 A low level signal on RD0 lead and flip-flop IC18 being set activates SYNC0 and CLKR0 signals. The SYNC0 signal remains low until RD0 signal returns to a high level. At the trailing edge of the RD0 signal, data on the information leads is gated into the register on FC397.

7.74 A low level signal on SST0 lead and the BT4 being addressed activates SYNC0 and GOB1 signals. The GOB1 signal gates the output of register onto the information leads.

7.75 Command inputs INIT0 or ACKI0 also activates SYNC0 signal. The WAIT0 signal is activated by ETCH1 circuit, flip-flop AIDA and gate AICLK0 generate the clock pulse on CLKR0 lead. The trailing edge of this clock pulse gates data on the information leads into the register on FC397. The trailing edge of CLKR1 signal enables

the timing sequence, flip-flops DA and DB are enabled to activate GPR0 and GOB1 signals. When flip-flop DB becomes set, WAIT0 signal goes negative. The GRP0, GOB1, and SYNC0 signals remain true (1) until INIT0 or ACKI0 signals return to the high state.

7.76 A pulse on GP0 lead with signal SST0 or SD0 being low enables the parity generation sequence. The leading edge of GP0 signal activates WAIT0 signal. At the trailing edge of GP0 signal, the parallel register (FC397) is clocked via CLKR0 signal and flip-flop STD is toggled. The next transition of the clock activates GPR0 signal and enables the output on the register on FC397 via GOB1 signal. The next transition of the inverted clock toggles the DA flip-flop and activates WAIT0. The GOB1 and GRP0 signals remain true (1) until SST0 or SG0 signal is returned to the high level.

FC397

7.77 The FC937 contains a 16-bit holding register. The 16 outputs of the register feed into two 8-bit parity circuits. The output of each of the parity circuits is a one (1) whenever there is an odd number of ones present on the register inputs. Data on the 16 information leads are gated into the 16-bit register at the trailing edge of the pulse on CLKR0 lead. Contents of the register and associated parity bits are gated onto the information leads by setting GOB1 signal to a one (1).

7.78 Transmission line terminations are provided by resistive voltage dividers for each of the 18 information leads. The six least significant bits (0 through 5) of information leads are inverted and gated to FC396 for device addressing.

RSI Channel Circuit

FC376

7.79 The FC376 RSI low bits circuit (Fig. 39):

- Drives and receives the low byte (bits 0 through 7) of the parallel bus interface information leads
- Drives SYNC
- Receives command present (CP or RC0), data present (DP or RD)
- Receives and recognizes device address
- Converts character bytes on information (INF) leads for serial transmission and reception
- Provides independent buffers up to 65 bytes of data in both directions.

7.80 Parallel bus interface commands SDG1 or data ready (DR) and SSTG1 or sense status (SST) causes the RSI to gate INF bits to the parallel bus interface. The SDG1/DR and SSTG1/SST are ORed to generate output strobes SNDG1 and ASOUT0 for the information multiplexers. Signals RDG1/DP and RCG1/CP are ORed to generate signal RCUG0. Signals acknowledge interrupt (ACKI1) and initialize (INIT) are ORed to generate signal AKINIT0. Signals SNDG1, ASOUT0, RCUG0, and AKINIT0 are ORed to generate SYNC signal after a 120-nanosecond delay. Signals RCUG1 and SYNC0 are also used to strobe the received-information parity on FC377.

7.81 Low byte information (INF) is received from the parallel bus interface by FC376. Also parity (odd) is checked and outputs a parity check signal (PLOK1) to FC377.

7.82 Outputs from FC376 (low byte) to the low byte of the parallel bus interface information leads are selected by the 4 to 1 multiplexers under control of SLA1 signal as follows:

SLA1	SSTG1	SELECTS
0	0	Receive data character from the universal asynchronous receiver/ transmitter
0	1	Normal status, including address
1	0	All zeros (0) or ones (1) equal signal ALAD1
1	1	Diagnostic loop-back of mode for maintenance

When the multiplexers are strobed by signal ASOUT0, information low byte is gated back on the parallel bus and P_L is generated.

7.83 Signal RCB0/CP0 (command present) is received from the parallel bus interface as signal RC1. The six address leads (ADR0IN through ADR5IN) from the parallel bus interface is received by FC376. Information on the address leads is compared with address select signals. When the set of incoming address signals is equal to the complement of the address select signals, MYADDR1 goes high (1) and signal RC1 can now activate RCG1 and BRCG1 signals.

7.84 For serial parallel interface (SPI) operation, each RS1 signal also strobes the state of MYADDR1 signal and creates the latched addressed test signal ASPI1. The RSI addressed state is backplane wired to ADRD1 which controls each individual RSI circuit communicating with the parallel bus. Address select is gated to information leads INF 0 through INF 5 on a normal SST signal.

7.85 A crystal oscillator generates 5068.8 KHz clock signals. A programmable frequency divider converts the clock signals to 1 of 16 possible serial bit rates (baud). This rate is selected by the state of signals INF6R1 through INF9R1 on the last CS2M1 strobe signal and drives a universal asynchronous receiver/transmitter (UART), which independently converts the parallel data byte to serial data output to the EIA line drivers on FC377. The FC376 controls SEND BREAK mode signal SBRK, which when set forces the serial output to become low (SPACE) regardless of the signal from the UART. For testing purposes, the output of the UART may be internally looped back to the input by the program.

7.86 Two 4 × 64 bit first in-first out (FIFO) buffers store the incoming data word from the 3A CC. When both FIFOs can accept a new byte of data from the parallel bus interface, their input ready (IR) leads are raised to logic 1 level activating signal CKS1. Signal CKS1 goes out as status bit 7 and can perform the interrupt function when enabled on FC377. When the 3A CC sends another data word, RDG1/CP signal strobes data into the FIFOs. The UART takes a data byte from the FIFO buffers when both FIFO output ready (OR) signal leads and UART signal UTBMT1 are high. This combination activates UDS0 signal to strobe the new data byte into UART and a trigger delay circuit. After approximately 300 nanoseconds, the delay outputs signal inhibits signal UDS0 and sets a latch circuit. Signal QSSO1 from this latch circuit removes the strobe byte from FIFO buffers resulting in removing of output ready (OR) signals thereby resetting the delay circuit. After approximately 100 nanoseconds, the trailing edge of UDS0 signal causes the UART to remove its UTBMT1 signal, which resets the latch circuit and clears signal QSSO1. The circuit is now in its original state and ready for the next data byte transfer to the UART.

After a power up, data reset signal UXR0 can force the RSI circuit to a known state and ready for a data transfer to the UART. However, on power up the FIFOs do not contain data.

7.87 When the send buffer and the UART internal registers become empty, send in progress (SIP1) signal goes low. Received data bits from the UART are outputted to the parallel bus interface via two more 4 × 64 bit FIFOs in parallel. A third FIFO is used to store the UART status associated with each word as it is shifted. When these three 4-bit FIFO buffers have input space available [the input ready (IR) signals are active] and the output of the UART has data available (UDAV1) the data is strobed into two of the FIFOs in parallel. The third FIFO gets status information strobed into it concurrently with the data in the other two FIFOs, UPER1 (UART parity error), UOVR1 (UART overrun), and UFER (UART framing error). After the data is transferred, the UART is reset for the next transfer.

7.88 When a character is available at the receive FIFO buffers outputs, the combined output ready (OR) signal leads activate the data available (QDAV1) signal, which is read as status on information bit 6 and causing an interrupt on FC377 (if enabled). The next SDGI/DR signal to the 3ACC sets CBCRR1. The CBCRR1 signal is read out along with data on information (INF) bit 11 and indicates a new character. When the SDG1/DR signal ends, the character just read from the receive FIFO buffers is removed resetting QDAV1 and OR. The circuit is now ready for the next character.

> ***Note:*** If signal QDAV1 goes active during an SDG1/DR signal pulse but was inactive at the leading edge of signal SDG1, nothing happens until the next SDG1 signal cycle. This prevents bad characters (races and glitches) from being sent out.

Signal CEX1 outputted as information (INF) data bit 12 indicates something is wrong with the character.

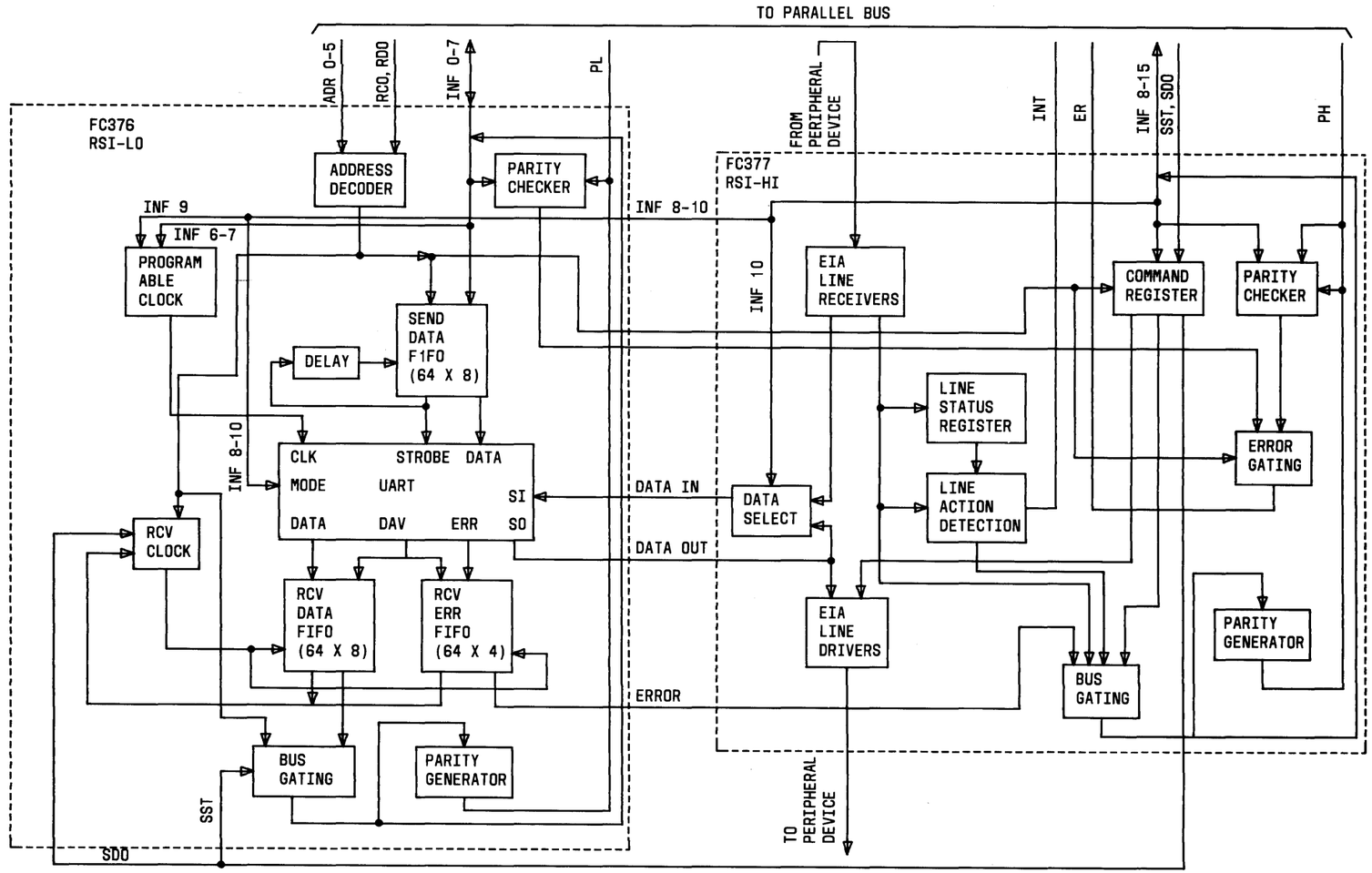


Fig. 39—RSI Channel Circuit

7.89 Data reset signal UXR is generated by either a master clear INIT1 signal or a UINIT0 signal command. The UXR signal clears all five FIFO buffers and the UART (both directions). Because the UART requires a 500-nanosecond time to clear, UXR signal is lengthened by a latch circuit. The UXR signal stays active until the RSI circuit is de-addressed or an SST signal is received.

FC377

7.90 The FC377 RSI high bits circuit:

- Drives and receives the high byte (8 through 15) of the parallel bus interface information leads
- Receives acknowledge interrupt (ACKI1), send data (SD), sense status (SST), and initialize (INIT) signals
- Drives busy, interrupt, direct memory access request, and error leads (where used)
- Interfaces all EIA RS-232 signals with transistor-transistor logic (TTL) signals
- Holds CONTROL modes and states.

7.91 Active low (0) parallel bus interface information signals (high byte) INF8B0 through INF15B0 and parity high signal PHB0 are received by FC377. These signals are converted to active high (1) signals INF8R1 through INF15R1 and distributed. Parity of data bits is checked by and correct parity check signal PHOK1 is generated [PHOK1 is high (1) with odd parity]. When the RCVG1 signal indicates the RSI is receiving data from the information (INF) leads and BSYNC1 signal delay has permitted parity checker outputs to stabilize, a low on either the parity high check signal (PHOK1) or the parity low check signal (PLOK1) from FC376 will set CPERF1 signal latch circuit. Also, the parallel bus interface ERRB0/ER lead will be driven active low (0) to signal bad parity. This latch circuit is cleared when the RSI is de-addressed or initialized. A false error (ER) signal is generated upon activation of RC/CP signal.

> ***Note:*** Parallel bus interface information parity is the only error which can activate ER lead.

7.92 Parallel bus interface command signals SDB0/DR and SSTB0/SST are received and gated by ADDRESS signal ADRD1. These signals are ORed on FC376 to provide output strobe signal SNDG1. The outputs to the information leads bit 8 through 15 are selected by 4 to 1 multiplexers under control of signals SSTG1 and SLAB1 as follows:

SSTG1	SLAB1	SELECTS
0	0	Normal data and character status
1	0	Normal status, including EIA inputs
0	1	All zeros (0) or ones (1) equal signal BLAD1
1	1	Diagnostic mode-audit status for testing

When signal SNDG1 is given by FC376, BSOUT0 signal strobes the selected 8 bits of data to bus drivers and to a parity generator which drives parity signal PHB0.

7.93 Information bits 8 through 15 are interpreted as command information upon activation of the RC/CP signal. Bits 14 and 15 encode four classes of commands, the other eight bits (6 through 13) are interpreted according to the class decoded from bits 14 and 15. Bits 14 and 15 are decoded into signals CS0D1, CS1P1, CS2M1, and CS3F0.

7.94 Signal CS1P1 is used to control ***send*** mode and the four EIA outputs data terminal ready, request to send, reverse channel transmit, and carrier fail reset. The CS2M1 signal strobes operating modes into a latch. Signal CS3F0 is used only by FC376 for the UART. The CS0D1 signal gates information (INF) bits into the diagnostic mode latch. Signal SLAB1/SLA0 (STATUS LOOP AROUND mode) when activated causes the information multiplexers to read out various mode settings on an SST signal, and all zeros (0) or ones (1) on the SDG1/DR signal lead, depending on the state of the BLAD1/LAD0 (loop around data) signal. Character-loop-around enable (CLAE) signal prevents EIA received serial data signal ERD1 from going to FC376 as signal ECHARI, and instead loops back FC376 serial send data signal ESD1 into FC376. This verifies the wiring between FC376 and FC377. Two consecutive commands with CLA set causes the loop around mode to start on FC377. Disable

send data (DSD) signal locks EIA serial output signal ESDE0 to the MARK (1) state to isolate the peripheral device during internal loop-around tests. Two consecutive commands with DSD set forces the RSI circuit into disabling all EIA outputs (DEIA).

7.95 Six EIA RS-232 STATUS lines from the interfaced device are received on FC377. The EIA status is sent to the information (INF) multiplexers and to EIA status-change detector. Current EIA status is constantly compared with the previous STATUS state. Any change in STATUS is read as bit 8 and causes an INTERRUPT (if enabled). Decoding a command signal or an initialization signal clears the latch and updates the EIA STATUS to reset and reenable the detector.

7.96 The BUSY1 signal, gated to the parallel bus interface as BUSYB0 on being addressed, is activated when no character transfer is ready in the direction currently defined by SEND1 and FULL DUPLEX (FDX). When SEND1 is low, QDAV1 from the RECEIVE buffer on FC376 controls BUSY; when SEND1 is high, control of BUSY is switched to CRS1 from the SEND buffer. If the FDX signal is ON and SEND1 is high, both QDAV1 and CRS1 can deactivate BUSY upon going high.

Note: BUSY is also given whenever SYNC is given.

7.97 An interrupt signal is activated as INTB0 signal whenever:

- BUSY1 is low indicating a CHARACTER TRANSFER READY and CHARACTER INTERRUPT ENABLE (CIE) mode is set; or
- EIA INTERRUPT ENABLE (EIE) mode is ON, and an EIA STATUS CHANGE sets EICF signal or the transmit buffer empties its contents with SEND mode OFF; or
- An EODC command signal clears DMATIP1 after a DMA data block transfer.

7.98 The FC376 holds SIP1 signal high as long as any data remain in the transmit buffers. When SIP1 goes low after SEND1 is turned OFF, the trailing edge of SIP1 sets the SIPCF0 latch, which causes INTERRUPT (if enabled). This signals the 3A CC that a data transmission has been completed.

7.99 The normal configuration of an RSI unit uses an SPI4 to access the 3A CC via an SCH, however, it may alternatively use a DBS and access via a PCH. Since several RSI circuits may access a DBS but only one RSI port at a time may perform a DMA data block transfer, the DMA ENABLE mode is provided to select the active port. Initially DMA ENABLE (DMAE) mode signal is OFF. When DMAE0 is high DMAR1 signal is inhibited, but DMA TRANSFER IN PROGRESS (DMATIP1) is active (1) and END OF DATA COMMAND (EODC0) is OFF (high). When DMAE is set, the RSI will respond to each low on BUSY1 lead by activating DMARB0 to the parallel bus interface. This signal continues until the DMA channel sends an END OF DATA COMMAND (EODC) signal which drives EODC0 low to clear the DMATIP latch circuit. This action locks out DMARB0 and an INTERRUPT is sent out. To set up another DMA data block transfer, the 3A CC must clear and then reenable DMAE to set DMATIP1 for proper operation.

Voltage Regulator

FC380

7.100 The voltage regulator FC380 contains two three terminal voltage regulators which FC380 converts the unregulated (±)15 volts to regulated (±)12 volts for use by the RSI channel circuit EIA drivers.

7.101 Positive 12 volts is regulated by the Q1 circuit with resistor R1 used to protect Q1 circuit under no load conditions (Fig. 40). Capacitors provide: stabilization under surge, high frequency decoupling, and input filtering.

7.102 The negative 12 volts is regulated in the same manner as the positive 12 volts.

E. Maintenance

7.103 The RSI unit is provided with loop-around diagnostic modes. The circuit can be sent all zeros or ones to find stuck-at faults, or to verify control states, including command lines. Diagnostics can isolate the fault to one of two circuit packs. During normal half-duplex send

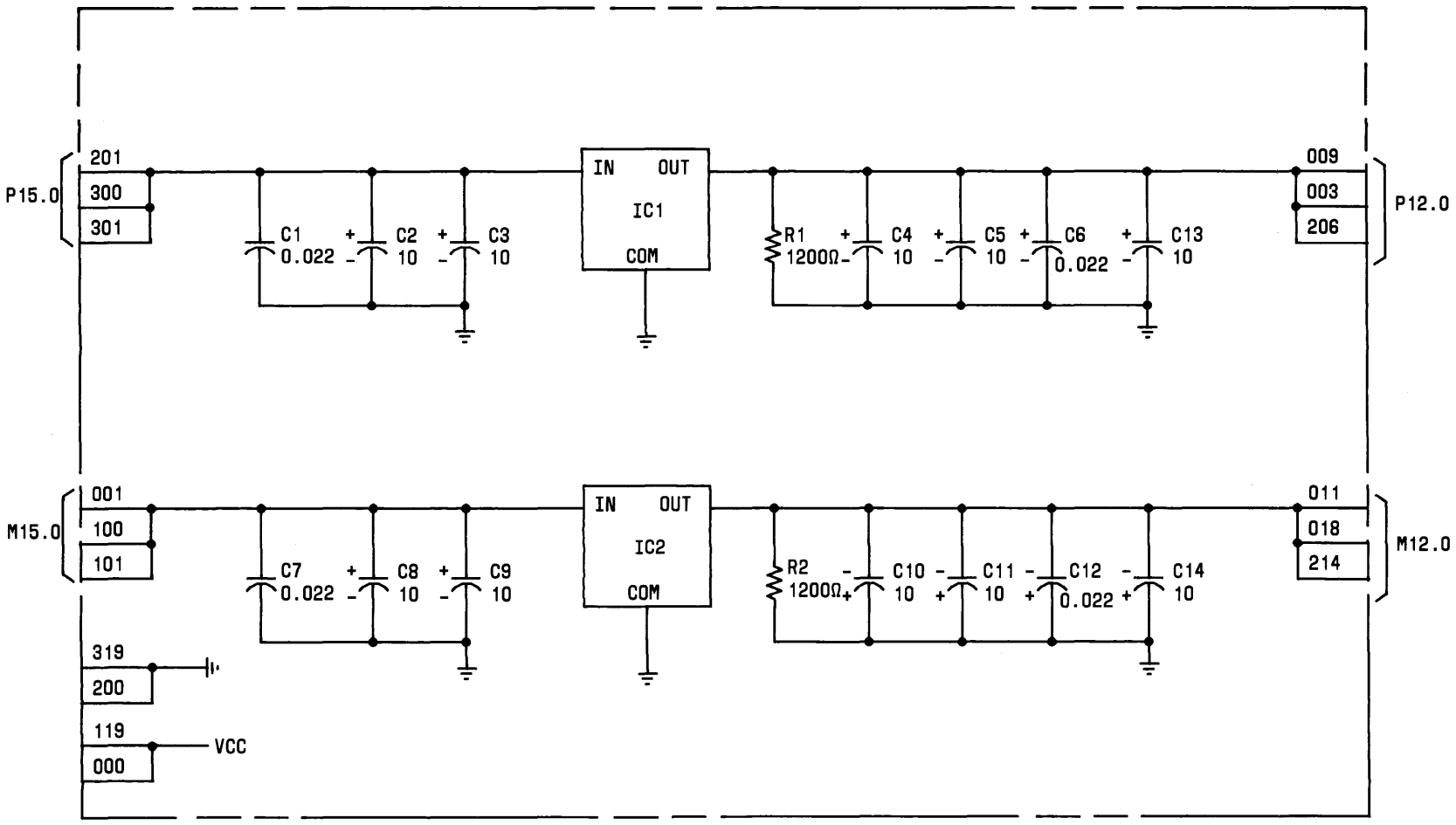


Fig. 40—FC380 Voltage Regulator

operation each character sent can be looped around the RSI circuit and verified. The 3A CC can disable RSI outputs to peripheral devices served by the RSI during the loop-around test.

7.104 Additionally, in process maintenance is provided by the parity check circuits in the RSI.

7.105 Software programs are also provided to diagnose the RSI, resolving the fault to one of two circuit packs.

8. POWER

INTRODUCTION

8.01 The +5 volt power required for the DMA unit and PCH unit is obtained from the power supplies in the CTI/power unit (located directly above the 3A CC in the processor frame). Three 132M power supplies (+5.2 volts ±5 percent, 17.5 amp) are used in the CTI/power unit, one for each of the two PCH units and one for the optional direct memory access unit. Several versions are available to allow for I/O equipment variations.

8.02 Fusing for the DMA unit and PCH unit consists of a set of fuses, each individually controlling up to 5 amps of current generated by the +5 volt supply from the CTI/power unit. The CTI/power unit is additionally fused with the main -48 volt supply. Power system alarm circuitry monitors power alarms (PAs) and fuse alarms (FAs) that indicate CTI/Power unit power failure. All CTI/power unit fuses are ***ORed*** into the frame major alarm signal. All converter alarms are ORed into the frame minor alarm signal. Power alarm test (PAT) signal to the system status panel is used as a continuity check on the power system.

CTI/POWER UNIT

8.03 The CTI/power unit serves to house, fuse, and provide alarms for the +5 volt (132M) converters. Also, it provides a power sequencing circuit that prevents the DMA and PCH units from outpulsing erratically during power-up or power-down operations. A special relay logic power sequencing subunit provides this power sequencing. The power-up sequencing provides for bringing the logic power up first and then the ac parallel bus drivers for the SPCH. The power-down sequence is the opposite of the power-up sequence; that is, power is removed from the ac parallel bus drivers, and then the logic power is removed.

8.04 The DBS is not equipped with its own power supply. Each DBS is powered by a converter furnished by the peripheral device interfacing the DBS. The DBS requires two separate +5 volt power inputs. These are ***+5V,*** which supplies power to logic circuits, and ***BUSPWR,*** which supplies power to the bus driver circuits.

8.05 A means of sequencing application of power during power-up and power-down of the DBS is required. During power-up, application of BUSPWR is delayed by approximately 2 seconds following application of +5 volts. During power-down of the DBS, removal of +5 volts is delayed by approximately 2 seconds following removal of BUSPWR.

8.06 Where proper sequencing is provided by the peripheral device, the +5 volts and BUSPWR are wired to the DBS on separate lugs in the backplane. Where power is not sequenced by the peripheral device supplying DBS power, such as in transation network (TN) application, the converter output is wired directly to the DBS +5 volt lug and an FC402 power sequencer is required in position 11 of the DBS housing.

8.07 The RSI unit requires +5 volts for TTL logic and 15 volts for the voltage regulator (FC380). The voltage regulator converts the 15 volts to 12 volts (regulated) for RSI channel circuits. Power supply and alarms circuits for the RSI unit are provided for by the operating company.

ALARMS

8.08 The 132M power converters in the CTI/power unit receive input power of -48 volts from the processor frame. Fusing and alarms for the -48 volts are provided by the processor frame. These alarms are also available as relay closure points in the CTI/power unit. Converter outputs are partitioned into 5-amp (or less) branches via a fuse subunit to prevent backplane wire burnout due to shorts. Alarms for fusing of +5 volt outputs of the 132M converters are tied into the processor frame major alarm (these alarms are also available as relay closure points in the CTI/power unit). The alarms share the relay closure scan points and are available for user scanning.

8.09 The 132M converters are equipped with their own out-of-voltage limits alarm (over and under), an overvoltage shutdown, and an overcurrent shutdown, each of which also produces a visual alarm on the converter.

8.10 The minor alarm is set by a converter in the 3A CC or CTI/power unit being out of specified voltage range; usually no action is taken. The major alarm is the result of an open fuse or a converter being out of service. (Major alarm means power is physically interrupted.) When a major alarm is given, the units are shut down and an appropriate alarm signal (visual and audible) is given.

8.11 More detailed information on power may be obtained from Section 254-300-140.

9. REFERENCES

9.01 The following documents contain information relevant to this section.

Section 254-300-110—3A CC Description, Common Systems

Section 254-300-120—3A CC Theory, Common Systems

Section 254-300-140—Processor Power System, Common Systems

10. GLOSSARY

10.01 A glossary of terms is provided to aid in the understanding of this section.

Asynchronous—Functional units operate or interface without a fixed time relationship.

Autonomous—The device can perform its primary function without external assistance.

Bit Partitioning—Functional grouping of bits of a register on two or more circuit packs.

Buffer—A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another. Normally a register.

Bus—One or more conductors over which information is transmitted from any of several sources to any of several destinations.

CDI—Collector diffusion isolation. (Technique for fabricating integrated circuits.)

Channel—A communication path providing 1-way or 2-way transmission between two terminations.

Common Control System—A switching system that makes use of common equipment, which is not part of a switching connection but is used to establish a connection and then becomes available to establish other connections.

Cross Point—A control signal generated by coincidence of two other signals.

CTI—Collector diffusion isolation (CDI) logic to transistor-transistor logic (TTL) interface.

Data Link—Electronic equipment that permits automatic transmission of information in digital form.

Diagnostic—A program which functions to isolate a fault within the unit under test.

Final Address—The address of the last (highest) memory location assigned for use by the 3A CC/DMA for addressing a device.

Flip-Flop—A device capable of assuming two stable states (set or clear), thereby storing a bit of information. It remains in either state until a signal changes it to the other state.

Interrupt—A signal generated by a device to notify the 3A CC that the device requires attention.

Interrupt Vectoring—A method whereby the identity (ie, address) of an interrupting device is provided automatically to the processor along with the device interrupt signal.

MY—Refers to the unit under consideration. It is interconnected to a duplicate unit that provides an alternate unit function to assure performance.

OTHER—Refers to a duplicate unit that is interconnected with the current unit under consideration to provide an alternate unit function to assure performance.

Present Address—The address of the device currently being serviced.

Time Shared Circuit—A common circuit with services that are used by a number of circuits during separate time intervals.

10.02 The following abbreviations are used throughout this document:

ACKI—Acknowledge interrupt

ADR—Address

BUSPWR—Bus power

CDI—Collector diffusion isolation

CLAE—Character loop-around enable

CMND—Command

CONT—Control

CP—Command present

DBS—Duplex bus selector

DTB—Data buffer

DEV—Device (peripheral device)

DMA—Direct memory access

DMAR—Direct memory access request

DP—Data present

DR—Data request or data ready

EDR—Error data register

EDT—Error data

EIA—Electronic Industries Association

ENBDR—Enable data ready

ENREL—Enable release

EOD—End of data

ER—Error

FAL—Final address low

FAH—Final address high

FIFO—First in-first out

IC—Integrated circuit

INF—Information

INIT—Initialize

INTP—Interrupt

I/O—Input/output

IOB—Input output buffer

IP—Initialize periphery

IS—Interrupt status

LED—Light emitting diode

MAS—Main store

MCS—Main channel select

MDT—Memory data

MLPWB—Multilayer printed wiring board

MPCH—Main parallel channel

MRF—Maintenance reset function

PAL—Present address low

PAH—Present address high

PBI—Parallel bus interface

PCH—Parallel channel

P_H—Parity high

P_L—Parity low

PROMATS—Programmable magnetic tape system

PWR—Power

RAM—Random access memory

SBC—Store bus control

SCH—Serial channel

SCAR—Subchannel address check

SCMP—Store complete

SCS—Subchannel select

SERC—Store error C

SGO—Store go

SLA—Synchronous line adapter

SPCH—Subparallel channel

SPI—Serial peripheral interface

SSCH—Subserial channel

SST—Sense status

SYNC—Synchronize

TN—Transaction network

TTL—Transistor-transistor logic

UART—Universal asynchronous receiver/transmitter