SYSTEM STATUS PANEL, SYSTEM STATUS PANEL CONTROLLER, AND SYSTEM STATUS PANEL RELAY UNIT DESCRIPTION AND THEORY OF OPERATION COMMON SYSTEMS 3A PROCESSOR

CONTENTS PAGE

CONTENTS PAGE

CONTENTS PAGE

Figures

Tables PAGE

1. GENERAL

1.01 This section describes, in physical and functional terms, the characteristics and theory of operation of the system status panel (SSP), the system status panel controller (SSPC), and the system status panel relay unit (SSPR) used in conjunction with the Common Systems 3A Processor.

1.02 This section is being reissued to include the system operations controlled by keys on the SSP and to clarify other areas involving system functions. Since this reissue is a general revision, no revision arrows have been used. Equipment test lists are not affected by these changes.

1.03 The SSP, SSPC, and SSPR are nonduplicated units within the processor complex. The SSP provides maintenance personnel with the means to monitor and control the status of the system. The SSPC provides the interlocks, control logic, and display buffers necessary for the operation of the SSP. The SSPR provides a relay interface between the SSPC and various system peripheral frames as well as a power sequencing function for the SSPC.

2. PHYSICAL DESCRIPTION

2.01 The SSP, SSPC, and SSPR are housed in the maintenance frame (Fig. 1). The SSPC is not shown since it is mounted behind the SSP. The SSP is hinged to the side bracket of the SSPC, and a magnetic latch on the panel keeps it securely closed. The circuit packs of the SSPC are easily accessed by opening the SSP (Fig. 2).

2.02 All interconnections between the SSPC and other units are accomplished by one of three types of cabling techniques. The first type of cable is a 30-gauge, 31-conductor, flat ribbon cable. It is used in conjunction with the second and third types to connect the SSP to the SSPC. The second type of cable consists of twisted pairs and is used

to connect the SSPC to the E2A telemetry unit. The third type of cable consists of coaxial cable and is used to connect the SSPC to the 3A central controls (3A CCs). The first two types of cable require a connector and paddleboard assembly at each end. The coaxial cables may require the paddleboard and assembly connector or the coaxial-type connector at one or both ends. The SSPR combines coaxial cable as well as twisted pairs into a "laced cable" to interconnect with the maintenance frame power unit and the SSPC.

SYSTEM STATUS PANEL

2.03 Critical, major, and minor trouble conditions in the system are indicated by visual indicators accompanied by audible alarms and/or teletypewriter (TTY) output messages. All visual alarm indicators are located on the SSP. There are visual indicators in other areas of the office, but these are used to supplement the indications on the SSP (ie, if a power alarm is displayed on the SSP, a lamp on the associated power unit is also lighted to identify the specific power unit).

2.04 The SSP for No. 3 Electronic Switching System (ESS) applications is shown in Fig. 3. Panel stamping for some of the keys and indicators may vary, depending on the system application. Otherwise, physical appearance of the SSP is as shown. The SSP consists of a plastic panel and a printed wiring board mounted to an aluminum frame. Panel devices include the following:

(a) Lamp and light emitting diode (LED) displays which indicate alarm conditions, system control unit (CU) status, and the status of the peripheral equipment

(b) LEDs 0 through 23

(c) Key/lamps for controlling the CUs

(d) Key/lamps for manually selecting and initiating system recovery.

In some applications, the system control unit will be designated SYC. For purposes of this document, the system control unit will be referred to as CU (SYC).

2.05 Four colors are used for the SSP display with each color identifying a different level of operation. Red indicates a trouble which requires immediate attention. Amber generally indicates a special condition. Green is used to indicate normal status and whether certain tests have passed. White indicates an active condition or the selection of a particular key.

2.06 In general, all logic function keys are push-push (nonmechanical locking) action (push to set; push to release). The notable exceptions to the push-push keys are as follows:

(a) DISABLE REMOTE ACCESS (mechanical locking)

(b) CKT POWER (mechanical locking)

(c) LAMP POWER (mechanical locking)

(d) ALT BUS (press to test)

(e) LAMP & POWER TEST (press to test).

2.07 The SSP consists of two major areas: SYSTEM STATUS AND CONTROL, which reflects the general condition of the system, and SYSTEM EMERGENCY MANUAL CONTROL, which is used to manually initialize or transfer a system during an emergency situation.

2.08 The SYSTEM STATUS AND CONTROL is a display of system health. Each display indicates the state of the corresponding flip-flop in the SSPC. These flip-flops are in most cases controlled by, and in all cases are readable via, input/output (I/O) messages for the 3A CCs. The only lamps or key/lamps not associated with a flip-flop are CIRCUIT POWER, LAMP TEST, and LAMP POWER. Table A lists the keys, lamps, and LEDs of the SYSTEM STATUS AND CONTROL section of the SSP.

2.09 The SYSTEM EMERGENCY MANUAL CONTROL provides a means for manually restoring the system to an operational state when various combinations of trouble conditions in CU 0 (SYC 0) and CU 1 (SYC 1) have blocked software control. The operation of the SYSTEM EMERGENCY MANUAL CONTROL is relatively complex since operator judgment is required to determine the severity of the problem and to determine the combination of keys necessary to correct the situation. Table B lists the keys and lamps of the SYSTEM EMERGENCY MANUAL CONTROL section of the SSP.

SYSTEM STATUS PANEL CONTROLLER

2.10 A 4-inch mounting plate provides the necessary structure for mounting two 80A apparatus housings required for packaging the discrete and ceramic circuit packs. The circuit pack arrangement of the SSPC is shown in Fig. 4. The SSPC contains the controller to 3A CC I/O interface (FA1101, FA1102, and FC208), E2A telemetry interface (three FA1103s), SSP interface (four FA1100s), relay driver circuits (FC209), +3 volt regulator (FC21), and +12 volt reference (FB152).

2.11 Signal distribution between the packs of the SSPC is accomplished via wire-wrap connections on the terminals of the backplane.

SYSTEM STATUS PANEL RELAY UNIT

2.12 A 4-inch mounting plate provides the structure to support five terminal strips, one AK30 relay, and fourteen AF10 relays (Fig. 5). The relays require +24 volt power. They are used in the SSP 3-volt power sequencing circuits and as buffer circuits to office alarm and monitor circuits.

3. FUNCTIONAL DESCRIPTION

3.01 The SSP and SSPC provide information and control which may be of assistance to maintenance personnel during trouble conditions. The SSP provides the following to both local and remote maintenance personnel:

(a) A visual display of system health via panel indicators

(b) A means of entering a manual request or a system initialization simultaneously to both 3A CCs

(c) A means of forcing a 3A CC on- or off-line.

3.02 The SSPC is the interface between the SSP and the 3A CC and provides the following to the SSP:

(a) Flip-flop memory elements for control of the SSP light indicators

(b) Key memory flip-flops that reflect the status of the SSP key operations and that control the corresponding SSP indicators

(c) The I/O circuits to the 3A CC

(d) The interlocks necessary to protect the system in the event that manual intervention from the SSP is accidentally or incorrectly performed

(e) The pulse drivers for the SSP force active and lock functions and the 3A CC maintenance reset function (MRF).

(f) The relay drivers for the SSPR

(g) A timing generator that gives an SSP alarm (PANEL TIME OUT) if a system message is not received within approximately 3.3 seconds.

3.03 The SSPR provides a relay interface between the SSPC and office alarm circuits as well as between the SSPC and various peripheral frames. In addition, the SSPR is used as an access point for all alarms and alarm test leads entering or leaving the maintenance frame and sequences the power to the +3 volt A8 conveters in the SSPC.

3.04 The system may be unattended, hence, the SSP functions must be available to maintenance personnel at a remote office. This remote maintenance capability is provided by an E2A telemetry unit. The E2A interface (Fig. 6) within the SSPC provides buffering between the panel interface and the E2A telemetry unit. Both the E2A telemetry unit and interface are optional and are not equipped unless ordered. If equipped, the E2A units are located on the maintenance frame above the SSP and tape data controllers.

3.05 Table A summarizes the designations and functions for keys, lamps, and LEDs in the SYSTEM STATUS AND CONTROL section of the SSP; and Table B summarizes the designations and functions for SYSTEM EMERGENCY MANUAL CONTROL keys and lamps. Where panel designations and functions vary with system application, items are listed by component designation (SD-1C906-01). Appropriate applications documents should be consulted for functional and panel stamping information.

3.06 The alarm system is based on multiple indications to locate a single unit of faulty equipment. The TTY messages, the audible alarm, and the SSP indicators combine to indicate the severity of alarm and the equipment area. Refer

to appropriate system applications documents for information on indicators that make up each level of alarms.

4. THEORY OF OPERATION

INTRODUCTION

4.01 The SSP, SSPC, and SSPR combine functions to form a visual reporting system to display system status at both the local office via the SSP and the switching control center (SCC), a control and interface unit, and a relay power sequencing and buffer unit. They provide a man-machine interface, whereby software control can be overridden. Also provided are access points for monitoring all alarm and alarm test leads entering or leaving the test frame.

SYSTEM STATUS PANEL

4.02 The SSP is comprised of switches, lamps, lamp drivers, and LEDs. The lamp and LED circuits are generally identical as are the switches. The minor differences that do exist are primarily to compensate for lamp intensity and/or switch function.

A. Switches

4.03 Switches S3 through S15, S17 through S20, and S26 are nonmechanical locking, while switches S1, S2, and S16 are mechanical locking (Tables A and B). Each switch is associated with a lamp to indicate that the function is being performed.

4.04 The switch is constructed so that one set of contacts open (break) before the other set of contacts close (make); ie, break before make. When the switch is released, it still operates as a break before make.

B. Lamp and Lamp Drivers

4.05 All lamp driver circuits are identical (Fig. 7), each consisting of three resistors and one transistor. When input (A) is open, transistor Q1 conducts, drawing approximately 35 mA through lamp DS1 to light the lamp. Resistors R1 and R2 combine to form the base-bias for Q1. R4 is used as a "keep-warm" resistor (eg, R4 maintains an 8 mA current flow through the lamp to prevent a current surge when the lamp is lighted). To prevent overloading the lamp power supply when large numbers of lamps are lighted or during a lamp test, a current limiting resistor, R11, is used in all except the green lamp circuits. The green lamp circuits are excluded because green is a better light filter than the other colors, thus the green lamps would be too dim.

C. LED Circuits

4.06 All LEDs use basically the same circuit (Fig. 8) except that the amber LEDs use a lower value for the resistor then do the red and green LEDs. Nominal operating voltage of 1.8 volts across the LED (essentially an open at (A)) produces light. The LED extinguishes when a ground is applied at (A) or when the voltage across the LED is below 1.4 volts.

D. Filter Circuits

4.07 There are capacitors in the SSP for filters. They are placed strategically throughout the lamp and LED circuits to reduce noise coupling from the current surges during lamp test.

SYSTEM STATUS PANEL CONTROLLER (SD-1C907-01)

4.08 The SSPC consists of flip-flop memory elements, shifting and decoding circuits, relay drivers, timing generators, parity checkers, and interface circuits controlled by:

(a) Serial data messages to and from the 3A CCs

(b) Pulses or levels generated by the SSP switches

(c) E2A telemetry switch operation initiated at the switching control center.

Electronic interlocks are provided that require certain emergency manual control key functions on the SSP to be operated sequentially. Electronic "debounce" functions are incorporated in the circuits connected to switches to compensate for multiple pulses which mechanical switches tend to generate upon closure.

A. Key Memory

4.09 The memory circuit pack (FA1100) contains 24 flip-flops which are used as memory

devices to reflect the state of an SSP key or to control an SSP status LED or lamp. The 24 flip-flops are subdivided into three groups of eight data bits each (DG0, DG1, and DG2). A write-read 8-bit data bus is common to all three data groups. Data group DG0 is in most cases writable and in all cases readable via the data bus. Data groups DG1 and DG2 are in all cases writable and readable via the data bus.

4.10 Data group DG0 is not only accessible by the data bus but also from external sources. Data groups DG1 and DG2 are not accessible externally because they do not have the same attributes as DG0 which enable it to respond as toggle flip-flops to the first input pulse or to repetitive pulses.

B. Shift Register and Control Logic

4.11 The SSPC is accessed via a serial 21-bit data message from the 3A CC which is transmitted in bipolar form (Fig. 9). Each bipolar pulse is decoded into a data zero or one with the total bipolar pulse period being used to form a shift pulse for the shift register. Figure 10 shows the I/O message format. The expected start code is 011. Any other code or bad parity causes a maintenance start code (101), with the data bits all set to zeros, to be transmitted back to the sending 3A CC. The op-code decoder recognizes a write-read operation when bit 4 is 0 and bit 3 is 1. Any other op-code is decoded as a read only. The 3/6 address bits are decoded, and the outputs determine the key memory data group that is selected. Data bits 12 through 19 correspond to the data group bits 0 through 7. PL is parity for bits 3 through 10, and PH is parity for bits 12 through 19.

4.12 The control logic receives messages in control state S0 (Fig. 11) until the shift register advances a data one into shift register bit STA00 signaling that a complete message is received. The 3A CC continues to transmit data zeros following the message until it receives an acknowledge or until a software time-out occurs (approximately 25 microseconds). At the end of the next CLK0 pulse (150 ns), the control state advances to S1. During the 150-ns interval before the advance to S1, parity was checked, and the start code was checked and ANDed with the parity. If the message is correct, output STPK0 (FA1101) will be zero before the advance to the S1 state. S1 then becomes a dummy state; and at the next CLK0 pulse (150 ns), the control state advances to S2. The selected op-code output lead remains active through control state S3, and the address select remains active through S5. The data outputs (DB00 through DB07) from the shift register are active during S2 and S3. If a write-read op-code is present, the selected FA1100 data group outputs to the data bus are blocked until S4, by which time the data group has been updated to the shift register data contents. When the first output shift occurs, a dummy data 1 is shifted into the PH bit to guard against a premature all-zeros output of shift register data which would reset the control state to S0, thereby inhibiting the sending of the 21-bit message to the 3A CC. This process is also explained in flowchart form in Fig. 12.

4.13 The shift register control logic looks for all zeros in the shift register as an indication to change from the send state to the receive state. When this occurs, several bipolar pulses may still be received; but since they are zeros, the shift register remains cleared. The 3A CC I/O is capable of blocking further pulses after it has received the full 21-bit message. Approximately 250 ns after the last bipolar pulse is received by the SSPC, the I/O sequence reset monopulser becomes active causing the control state to be forced to S0 and the PH bit to be cleared. Although resetting by the monopulser may seem unnecessary, it is useful in reducing the number of useless messages due to transients on the receive line.

C. Miscellaneous Circuits

4.14 The miscellaneous circuits (FA1102) are split into four functional elements (A, B, C, and D), each of which is related directly to an SSPC function. Element A contains the logic for transmitting and receiving messages and a parity tree for checking and/or generating parity for the I/O messages. Element B provides the panel time-out circuit and clock pulses for element C. Element C is comprised of interconnecting logic and transformer driver circuits for the SSP ***force*** and ***lock*** functions. Element D is comprised of the interconnecting logic and drivers for the SSP initialization functions.

Element A

4.15 Element A is comprised of two basic parts, the transmit-receive circuits and a parity

circuit. The receive circuit decodes the data from a bipolar pulse stream and originates the shift pulse for the shift registers. The initialization section of the receive circuits is used to minimize the receiving of bad messages. The transmit section transmits the output messages back only to the originating source. The SELCC flip-flop determines which transmit port is enabled and which one is to be blocked. The I/O messages interrogated by the parity tree are expected to be of odd parity for both PH and PL. The parity section checks itself by doing a parity compare with the actual data bits of the I/O message and the parity determined by the parity tree. The results of the compare either generate a start code or reject the message with a parity error.

Element B

4.16 Element B contains the panel time-out circuit which consists of a 7-bit binary counter configured to produce an output only when the count reaches 120. A pulse shaping circuit is used to control the pulse widths of the transformer driver gates. The counter is reset each time a system message is received; and since system messages should be received before a 120 count, the output of the counter is an indicator of abnormal system operation.

Element C

4.17 Element C logically combines all the conditions necessary for the ***lock*** function and the ***force CU*** function. When all conditions are valid, the output gates begin outpulsing a zero active signal to the selected 3A CC at a 27-ms rate.

Element D

4.18 Element D contains the miscellaneous interconnecting logic for the system initialization function (MRF) provided by the SSP. For each attempt at system initialization from the SSP, one MRF pulse is generated. The length of the MRF pulse is determined by a gate delay chain and is generally between 80 and 150 ns.

Maintenance Telemetry Interface

4.19 Three maintenance telemetry interface circuits (FA1103) make up the telemetry interface that is used to buffer the E2A telemetry inputs from the SSPC flip-flop outputs. Each buffer circuit is an "OR" output of two double-inverted inputs. Inputs from the E2A telemetry are zero active to the SSPC, and the SSPC provides one-active signals to the E2A telemetry.

I/O Shift Control Monopulser, Transformer, and Clock

4.20 The I/O shift control-reset monopulser, I/O transformers, and emergency action clock circuit provide three separate functions to the SSPC. There are eight transformer interface circuits for isolating and busing signals such as the force and MRF pulses. An I/O sequence monopulser responds to input pulses of greater than 70-ns duration and provides output pulses of greater than 30-ns duration to the input buffer. A timing circuit provides a continuous asymmetrical square wave with a 27-ms period to the timing counter on FA1102.

Lamp and Relay Circuit

4.21 The lamp and relay circuits (FC209) are controlled by 3.5 mA of current at +0.4 volt as provided by an open collector logic gate and +3 volt power. The driver in turn provides 50-mA drive current at +26 volts to the lamps and relays. Grounding the inputs sinks the 3.5 mA and turns the driver off.

SYSTEM STATUS PANEL RELAY UNIT

4.22 The system status panel relay unit is comprised of power sequencing relay logic and alternate bus switching relays for the SSP and SSPC as well as relay buffers connected between the SSPC and the office alarm circuits and other peripheral frames as needed. Under normal (SYSTEM NORMAL) operating conditions the relays maintain the following states:

- A relay—Released
- INB relay—Operated
- CRT relay—Operated
- ELT relay—Operated
- PAS relay—Released
- BAT ALM relay—Operated
- MIN PWR relay—Operated

- PF relay—Operated
- AB 2/AB 4 (AB24) relay—Operated
- B relay—Released
- ALM TRFR relay—Operated
- MAS ALM relay—Operated
- FAL relay—Operated
- MIN ALM relay—Operated
- MAJ PWR relay—Operated.

A. Relay Logic

4.23 The power-sequencing relay logic (SD-1C908-01) consists of two relays, A and B, and their related components. A power sequence occurs when either the SSP CIRCUIT POWER key is operated or an alternate bus switch has occurred. Relay A (Fig. 13) is supplied with a -48 volt source and is made to operate (or release) by providing (or removing) its ground path via a set of contacts. Relay B is supplied with a +24 volt source and is made to operate (or release) by controlling its ground path via a transistor switch in the SSPC circuit. The transistor switch turns on to operate relay B when an RC circuit connected to its input has been sufficiently charged by +3 volts dc, and turns off to release the relay when +3 volt power is removed.

4.24 A power sequence begins with relays A and B nonoperated. When the CIRCUIT POWER key on the SSP is operated, a ground path for the -48 volt supply is provided via the switch contacts to operate relay A. Operation of relay A applies +24 volts to the start terminal of the +3 volt dc A8 converters located in the maintenance frame power unit, thus enabling the +3 volt converter output. Since a finite time interval is required for the +3 volt output to stabilize, operation of relay B is delayed to ensure a known initial state of the SSPC circuits when the +3 volts is stable. An open-circuit signal via contact 6 on relay A and contact 8 on relay B blocks all SSPC I/O operations, resets I/O control states, and clears all key memory flip-flops. Similarly, a ground signal, via the same contacts on relays A and B blocks the SSPC force-active function and MRF. These two signals remain active until relays A and B have both operated.

4.25 When the RC circuit connected to the B relay driver has been sufficiently charged by +3 volts dc, the transistor switch turns on to operate relay B. Operation of relay B switches the ground operate path for relay A such that it bypasses the CIRCUIT POWER key contacts and grounds via B relay contacts 6 and 10. This enables the power-sequencing process to be reversed for removing +3 volts dc to the SSPC.

4.26 Depressing the CIRCUIT POWER key on the SSP while the equipment is operating applies a ground path to the relay B driver circuit, causing the transistor switch to turn off. This releases relay B, thus initializing all SSPC key memory circuits, blocking all I/O functions in the SSPC and removing the ground operate path from relay A. Release of relay A turns off the A8 converter and removes +3 volts dc from the SSPC circuit.

B. Alternate Bus Switching

4.27 The alternate bus switching arrangement automatically attempts to switch from primary A power buses to alternate B power buses when loss of bus power occurs. The +24 volt dc A bus is monitored by relay AB24 and the -48 volt dc A bus is monitored by relay AB48 (SD-1C908-01). Both relays are held normally operated.

4.28 Relay AB24 is powered by the +24 volt A power source via fuse AA0A in the maintenance frame power unit. Ground return is provided via contact 9 on relay AB48. With this configuration, +24 volt dc power is distributed from the A bus via AB24 relay contacts. Loss of either +24 volt A bus power or the ground return will release relay AB24, thus transferring +24 volts dc to the B power source.

4.29 Relay AB48 is powered by the -48 volt A power source via fuse AOA in the maintenance frame power unit. Ground return for operation of the relay is provided via normally closed contact 1 of ALT BUS key on the SSP. Release of relay AB48 transfers -48 volt power to the B power source. It also releases relay AB24 to transfer +24 volt power to the alternate bus. Switching of relay AB24 from one bus to the other reverses the voltage polarity across power-sequencing relay

A, causing it to release for several milliseconds and then reoperate. This provides the required sequencing and initialization made necessary by momentary shutdown of the A8 converters during a bus switch. A test of the alternate bus switching function may be made by depressing the ALT BUS key on the SSP to release AB48 (Fig. 14).

C. Relay Buffer

4.30 The relay buffer (SD-1C908-01) provides isolation between the key memory flip-flops in the SSPC and the office alarm circuits and, if required, between the memory and other peripheral units. Setting a flip-flop in the memory operates a relay driver which in turn operates the related relay in the buffer. The exception is the PF relay which acts as a buffer from the peripheral switches to the test control bit in the SSPC. Operating the PF relay sets or clears the corresponding flip-flop in the memory.

SYSTEM FUNCTIONS

A. Lamp Power

4.31 Lamp power (+24 volts) (Fig. 15) is supplied to the lamps via fuse AA3 in the maintenance frame power and contacts 3 and 2 of the LAMP POWER (S2) switch on the SSP. LED power (+24 volts) is through fuse AA2 and contacts 6 and 5 of the LAMP POWER switch. A marginal amount of current, insufficient to light the lamps and LEDs, is available to the lamps and LEDs through R18 and R17 when S2 is not operated to prevent power surges when S2 is operated. The "marginal" current level is sufficient when S2 is off to provide control to other logic in the E2A telemetry and SSPC.

B. Lamp and Power Test

4.32 The LAMP & POWER TEST switch (S4) (Fig. 15) is used to initiate a lamp test for the SSP and a power alarm test for all converters and reference circuits in the maintenance frame. Operating S4 supplies +24 volts via contacts 2 and 3 to enable the LAMP & POWER TEST indicator and to enable transistors Q2 and Q3. Transistor Q2 inhibits all lamp control circuits in the SSPC, thereby removing the control signals and causing the lamps and LEDs to light. Transistor Q3 operates the ALM-XEFR relay in the maintenance frame power circuit which controls the sequencing for the power section of the test and lights the power and alarm indicators. When S4 is released, all indicators return to their former status and indicate system operation.

C. Lock

4.33 The LOCK flip-flop, when set, enables software access to the SELECT 0, 1, FORCE, and LOCKP flip-flops. To set the LOCK flip-flop from the SSP, the LOCK key (S20) is operated and KR01I00 becomes a one while KR01I10 and INHKR011 are grounded, thereby setting the LOCK flip-flop. When software interrogates the LOCK flip-flop and finds it set, a message is sent to the SSPC to set the LOCKP flip-flop which holds KMR0110 at a zero. Releasing the LOCK key enables the LOCKP flip-flop to be cleared by software or by operating the SELECT or FORCE keys. Software then sets the selected SELECT flip-flop and then the FORCE flip-flop.

D. Force SYC Active

4.34 The force CU (SYC) function may be initiated at the SSP by operating first a select key and then the FORCE key for manual selection or by operating the LOCK key which enables software selection of system control. Operating the SSP SELECT 0/1 key sets lead KR02(3)I00 to one and lead KR02(3)I10 to zero. The SELECT 0/1 flip/flop being set sets lead INSEL1 and clears lead KR01INH1. INSEL1 is connected to the inhibit inputs of the SELECT 0/1 flip-flops and prohibits the selection of both flip-flops during a force operation. Since KR11INH1 is a zero (LOCK key is released) on a one inhibit, the FORCE flip-flop is set by operating the FORCE key. With the SELECT and FORCE flip-flops set, the "AND" function of the transformer driver gates is satisified with the next 27-ms timing input. The transformer coupled pulses are positive to the active 3A CC and negative to the unavailable 3A CC. Each pulse enters a rectifier circuit in the 3A CCs and sets the system status register, LON bit 8, on the active 3A CC and LOF bit 9 on the unavailable 3A CC. When the force active signal is removed, the rectifier circuit times out, automatically clearing bits 8 and 9, and returns to system control.

E. SCC Lock/Force SYC Active

4.35 The SCC functions the same as the SSP; however, because of the interface telemetry,

the SSPC circuits operate with only a few significant differences. The KR101I10 inputs to the flip-flops remain grounded, and the gate delay chains internal to the telemetry interface are used in their place. The delay chains employed by the SSPC enable the SSPC to respond functionally the same as to an SCC or the SSP. The E2A telemetry uses nonbouncing, mercury-wetted relay contacts that give only one contact closure for each operation of the switch. This enables the SSPC flip-flops to be left in the repetitive toggle mode. The SCC functions are cleared the same as those set at the SSP with the only differences again being the type of switch used and the delay circuits replacing certain internal SSPC circuits.

F. Alternate Bus Test

4.36 The ALT BUS key (S3) provides the ground operate path for the +24 volt alternate power bus relay (PAB24) in the maintenance frame power unit. It also provides a ground path for the alternate power bus relay (AB48) in the SSPR which controls the alternate bus switching relay logic. Depressing S3 releases the ground to AB48 which initiates a bus transfer and causes the release of relays AB24, AB48, and PAB24. Software constantly monitors the relays in an attempt to set the ALT BUS flip-flop which can only be done when one or more of the relays is released. The ALT BUS indicator, driven from the ALT BUS flip-flop, indicates a change in the power supplied to the SSP, SSPC, and SSPR. Releasing the ALT BUS key results in switching back to the primary buses.

G. Test Control Execute

4.37 Depressing the ~~INIT~~ EXECUTE key (S5) operates the PF relay in the SSPR which enables the TESTEXEC flip-flop in the SSPC. This allows other switches in the office to operate the flip-flop through the buffering action of the PF relay.

H. System Initialization

4.38 The system initialization function provides a single transformer coupled pulse to each 3A CC for each initialization sequence executed at the SSP. The following procedure should be followed.

(a) Depress the ENABLE key.

(b) DEPRESS one, none, or all of the following keys depending on the function desired:

(1) S10 (See Note)

(2) S11 (See Note)

(3) S12 (See Note)

(4) BACKDT OFFICE DATA.

(c) Depress the INIT EXECUTE key.

The ENABLE flip-flop, when set, enables the setting of the STBLCALL, MEMRLOAD, RECNTCHG, BACKDT, and INITEXEC flip-flops. Enabling the STBLCALL, MEMRLOAD, RECNTCHG, and BACKDT flip-flops dictates to the system the type of change, if any, that is to be made. The INITEXEC flip-flop, when set, generates the MRF (maintenance reset function) pulse to the 3A CCs. The duration of the MRF pulse is determined by the gate delays on FA1102 and the reset time of the ENABLE flip-flop which is automatically reset by hardware as part of the MRF pulse generation design. Once software acknowledges an MRF, it scans the SSPC to determine if any of the initialization level flip-flops are set and what action is to be performed. Software performs the functions and clears the INITEXEC flip-flop and may or may not clear the initialization level flip-flops, depending on system requirements.

> ***Note:*** Refer to applications documents for the applicable system for information on functions and designations of these keys.

I. Alarm Control

4.39 FS 4 (SD-1C907) consists of a 27-ms timing generator that provides clock pulses for the SSPC time-out counter and the FORCE CU transformer pulsing circuit. It also contains the panel time-out flip-flop (PNTIMOUT) as well as flip-flops for alarm control. All the alarm control flip-flops have a corresponding relay in the SSPR which controls an indicator on the SSP except for the ALARM REL flip-flop. The ALARM REL flip-flop is set when a system alarm occurs that requires the ALARM RELEASE indicator on the SSP to light. The ALARM RELEASE switch/indicator on the SSP is used to clear the ALARMREL flip-flop but cannot be used to set it. ALARM TRFR and INHIBIT BUILDING ALARM keys on the SSP are

capable of setting their respective flip-flops in the SSPC.

J. Panel Time-Out and Timing Generator

4.40 The 27-ms timing generator is comprised of discrete components on FC208 whose output after reshaping in FA1102 is used to control the FORCE CU transformer driver gates. A binary counter using seven GDFFs as toggle flip-flops also uses the 27 ms to generate a time-out condition. When the counter reaches a 120 count (3.24 seconds), the counter sets the PNTIMOUNT flip-flop which sets the CRIT relay in the SSPR that trips the critical alarm and lights associated indicators on the SSP. Under normal system operating conditions, messages are sent from the 3A CC, resetting the counter, frequently enough to prevent the counter from reaching the 120 count. If the PNTIMOUT flip-flop is set, normally, a software-generated message must be used to clear it; however, the system could be configured to clear it with the ALARM RELEASE key.

K. TTY Initiate

4.41 The TTYINIT flip-flop is set by depressing the TTYINIT key. When software detects that the flip-flop is set, it resets the flip-flop, initializes the TTY controllers, and clears all TTY message memory buffers.

L. Circuit Power

4.42 Operating the CIRCUIT POWER key operates relays AB24, A, B, and ALM-XEFR which removes the A Bus supply to the +3V converters for the SSPC logic. All panel indicators are lighted while CIRCUIT POWER is operated as a result of the switch to B Bus and all I/O functions from the SSP are blocked.

M. Disable Remote Access

4.43 Operating the DISABLE REMOTE ACCESS key blocks the E2A functions to the SSP, but not the ability to monitor the SSP, and operates the DISREMAC flip-flop. DISREMAC is not a controlling flip-flop; hence, it serves only to light the DISABLE REMOTE ACCESS indicator and keeps software informaed as to the status of the key.

5. POWER

5.01 Power for the SSP, SSPC, and SSPR is supplied by the maintenance frame power unit. The SSP requires +24 volt input for the lamp and LED circuits. The SSPC requires +3 volts to operate the logic circuitry and +24 volts for alarms and the 12-volt reference circuit. The SSPR requires +24 volts for the relay buffer and +24 volts and -48 volts to operate the relay logic.

5.02 The SSPR monitors the -48 volt and +24 volt source. Loss of either the -48 volt or +24 volt A-bus operates the relay logic to switch the SSP and SSPC to B-bus power and sequences the +3 volt logic supply to the new bus. When power is supplied by the B-bus, the ALT BUS indicator is lighted.

6. MAINTENANCE

6.01 The SSP, SSPC, and SSPR are not involved with the message processing services for customers; therefore, they are nonduplicated units. Should a failure occur, any one or all three of the units can be removed from service without affecting normal operating service. However, if the SSP and/or the SSPC is out of service, maintenance personnel lose the emergency action capabilities provided and some knowledge of system status reported via the SSPC flip-flops. Although the TTY is available as a maintenance tool, the SSP, SSPC, and SSPR should be repaired as soon as possible since the following services are lost:

(a) Part of the remote maintenance capabilty

(b) Visual display of system status and trouble conditions

(c) Capability of manual system control.

6.02 In order to detect errors in the SSP, SSPC, and SSPR, the 3A CC checks all messages received from the SSPC for correct parity and start code. If the message contains incorrect parity or start code, a bit is set in the 3A CC error register. The SSPC control flip-flops are also monitored by software, and any abnormal condition causes an error register to be set, followed by an error message printout.

7. REFERENCES

7.01 The following Bell System Practices contain information which is relevant to this section.

Section 254-200-001—No. 1A Technology Description

Section 254-300-110—3A Central Control, Description, Common Systeems, 3A Processor

Section 254-300-160—Maintenance Frame, Description and Theory of Operation, Common Systems, 3A Processor

SD-1C906-01—System Status Panel

SD-1C907-01—System Status Panel Controller

SD-1C908-01—System Status Panel Relay Circuit

8. GLOSSARY

8.01 The following terms and definitions may aid in understanding this section.

Initialization [Also referred to as maintenance reset function (MRF)]—Restart of the 3A CC at a known location and condition. Two basic types are: system generated and manually generated.

Light Emitting Diodes—LEDs are chemically grown gallium phosphide crystals that convert direct current into a visible light output without benefit of energy-consuming filaments.

MRF—See ***Initialization.***

Network—Equipment that provides the interconnections which enable subscribers who are connected to the same or different offices to communicate with each other.

Off-Line—Equipment which is not actively performing a part of normal system functions may be either out of service for maintenance or operating in a standby mode.

On-Line—Equipment in actual use and performing normal system operational functions.

Parity—A bit attached to a word to make the total number of ones including the parity bit either odd or even.

Start Code (I/O)—A 3-bit code used to notify a device of an I/O message and the type of I/O message, normal or maintenance.

Temporary Store—The part of main store used for transitory data such as the information collected, used, and deposited during each call.

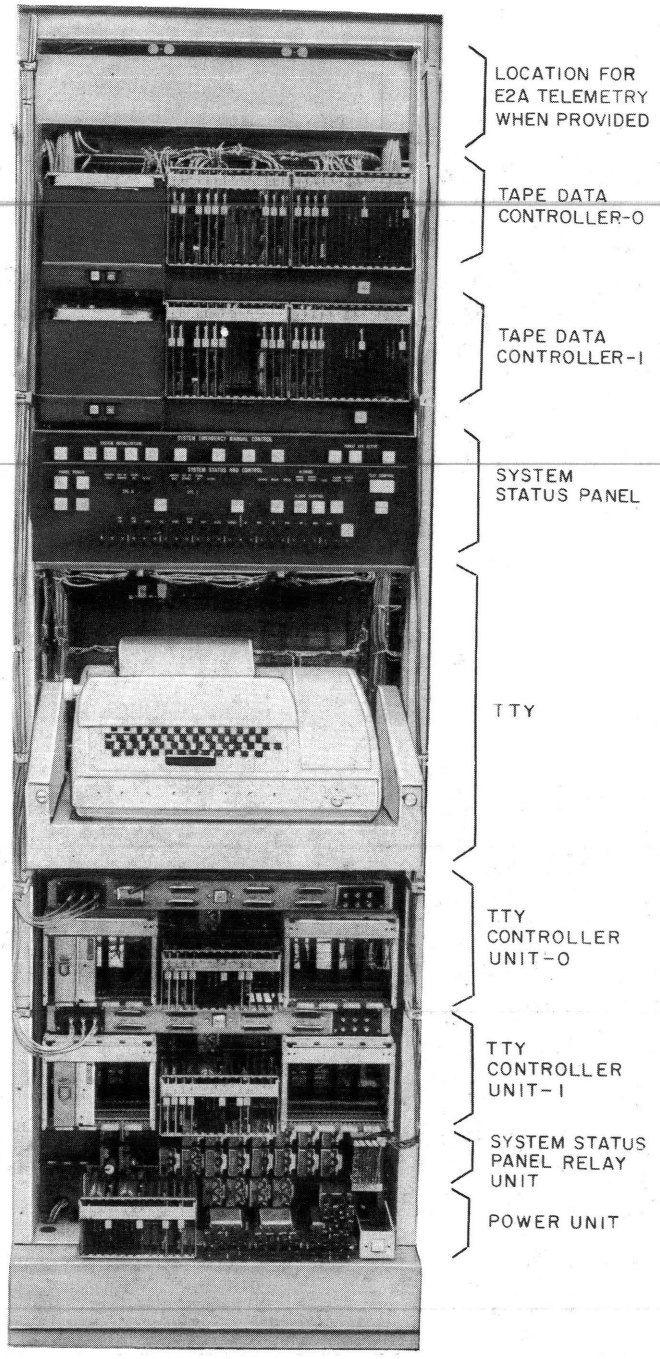

Fig. 1—Common Systems Processor Maintenance Frame

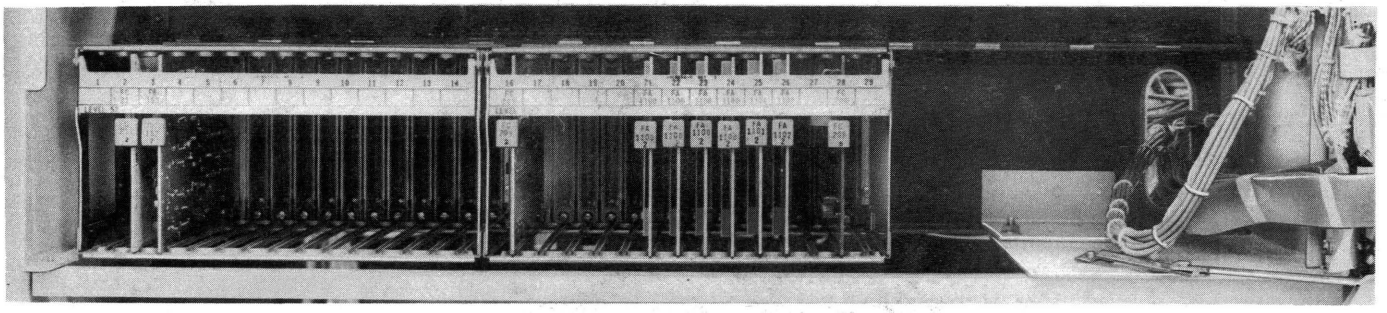

Fig. 2—System Status Panel Controller

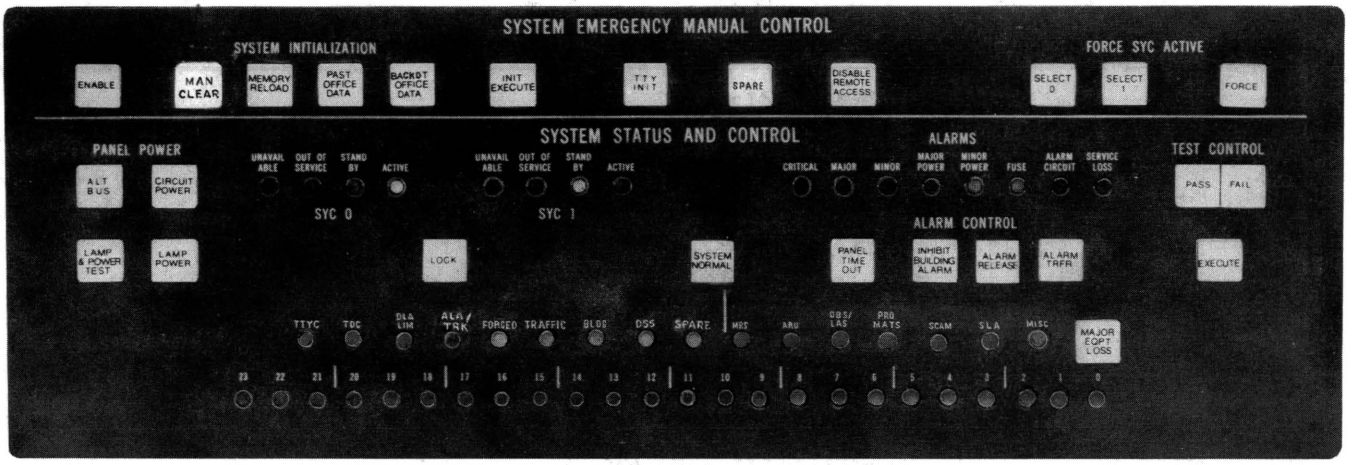

Fig. 3—System Status Panel for No. 3 ESS Applications

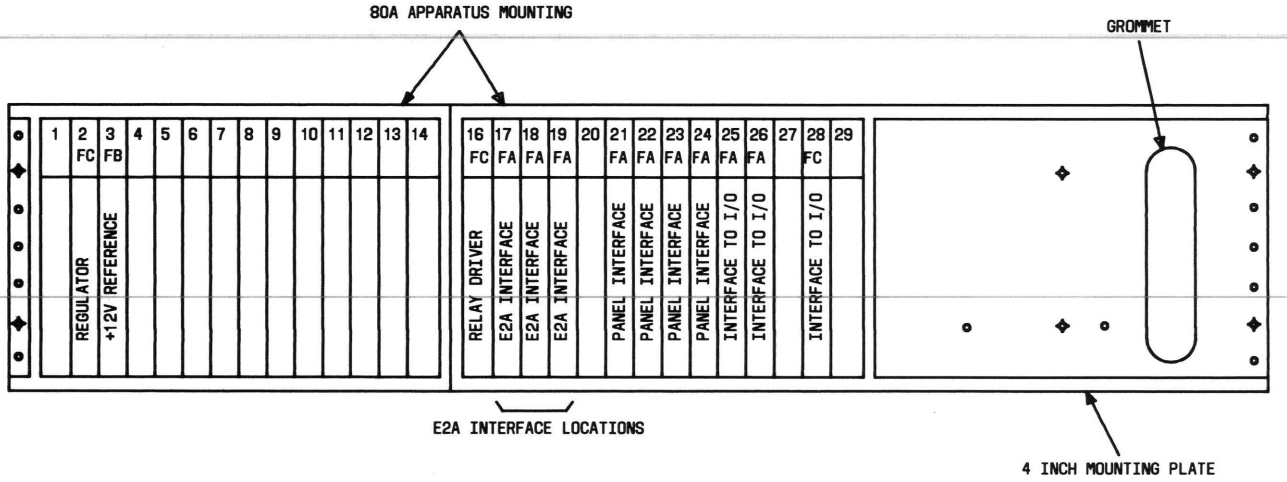

Fig. 4—System Status Panel Controller

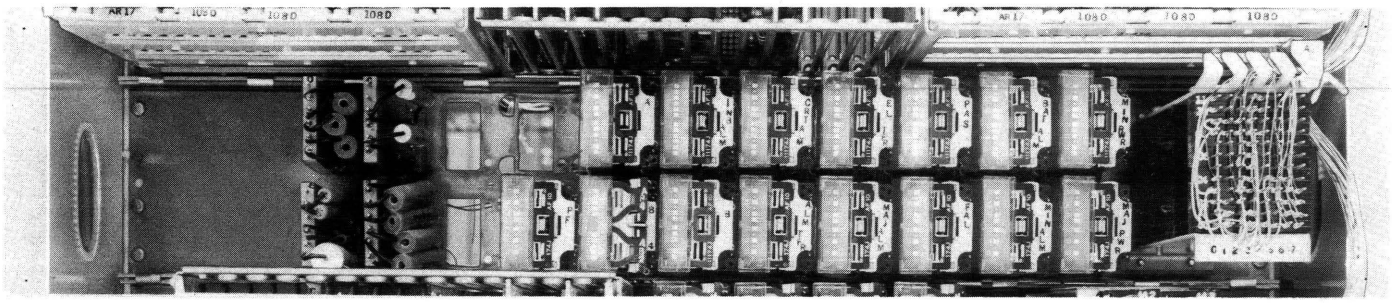

Fig. 5—System Status Panel Relay Unit

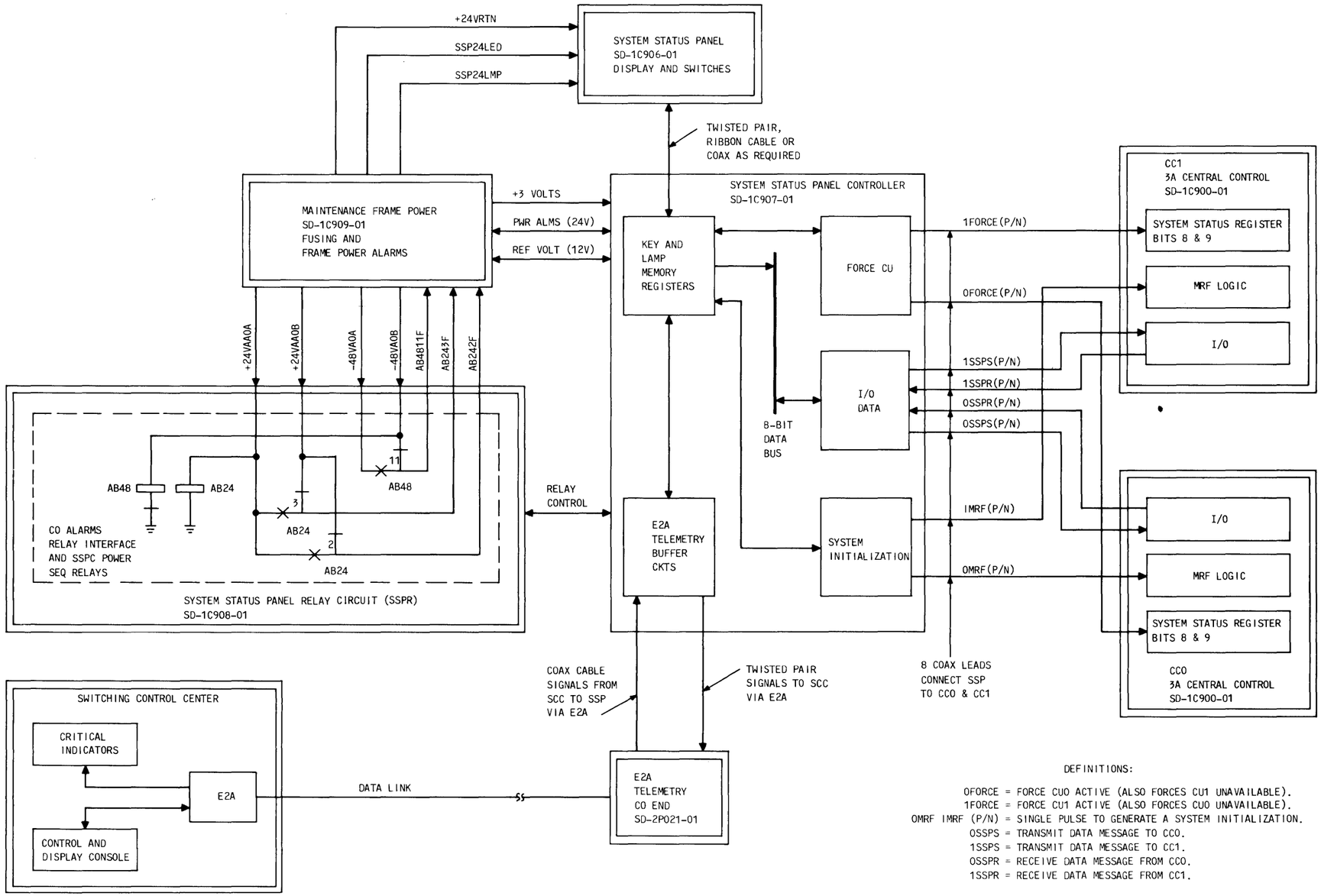

Fig. 6—System Status Units

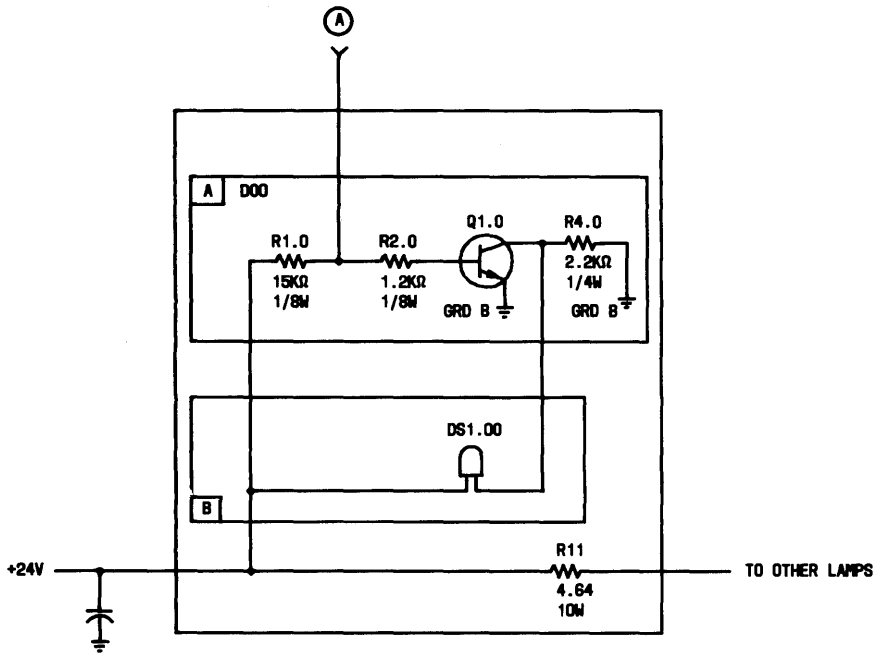

Fig. 7—Lamp and Driver Circuit

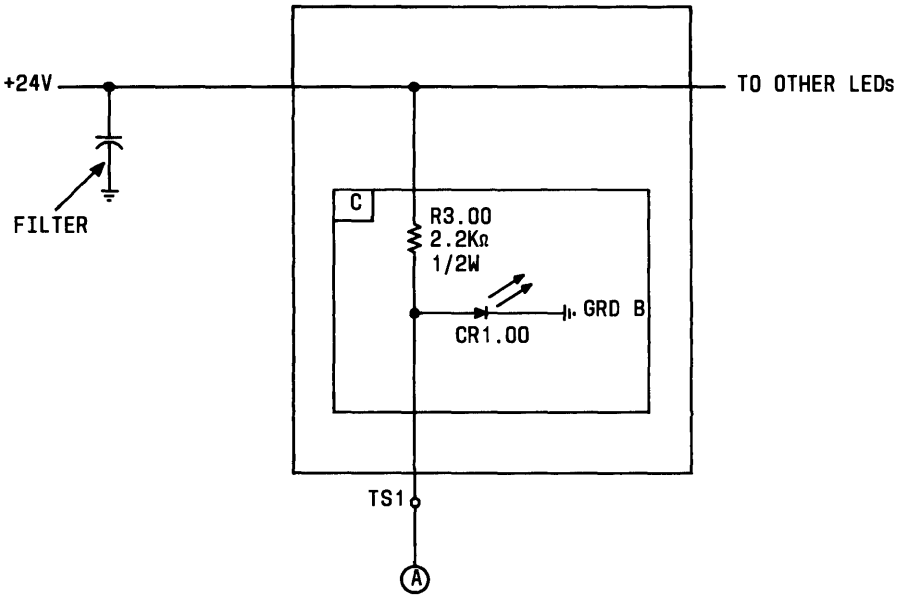

Fig. 8—LED Circuit and Filter

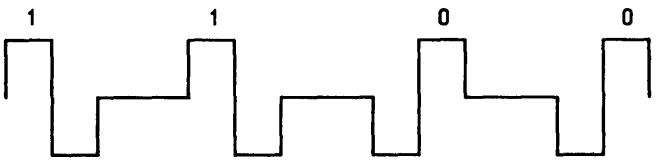

Fig. 9—Bipolar Pulse Pattern

PH	DATA BITS								PL	3/6 ADDRESS CODE						OP CODE		START CODE		
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Fig. 10—I/O Message Format

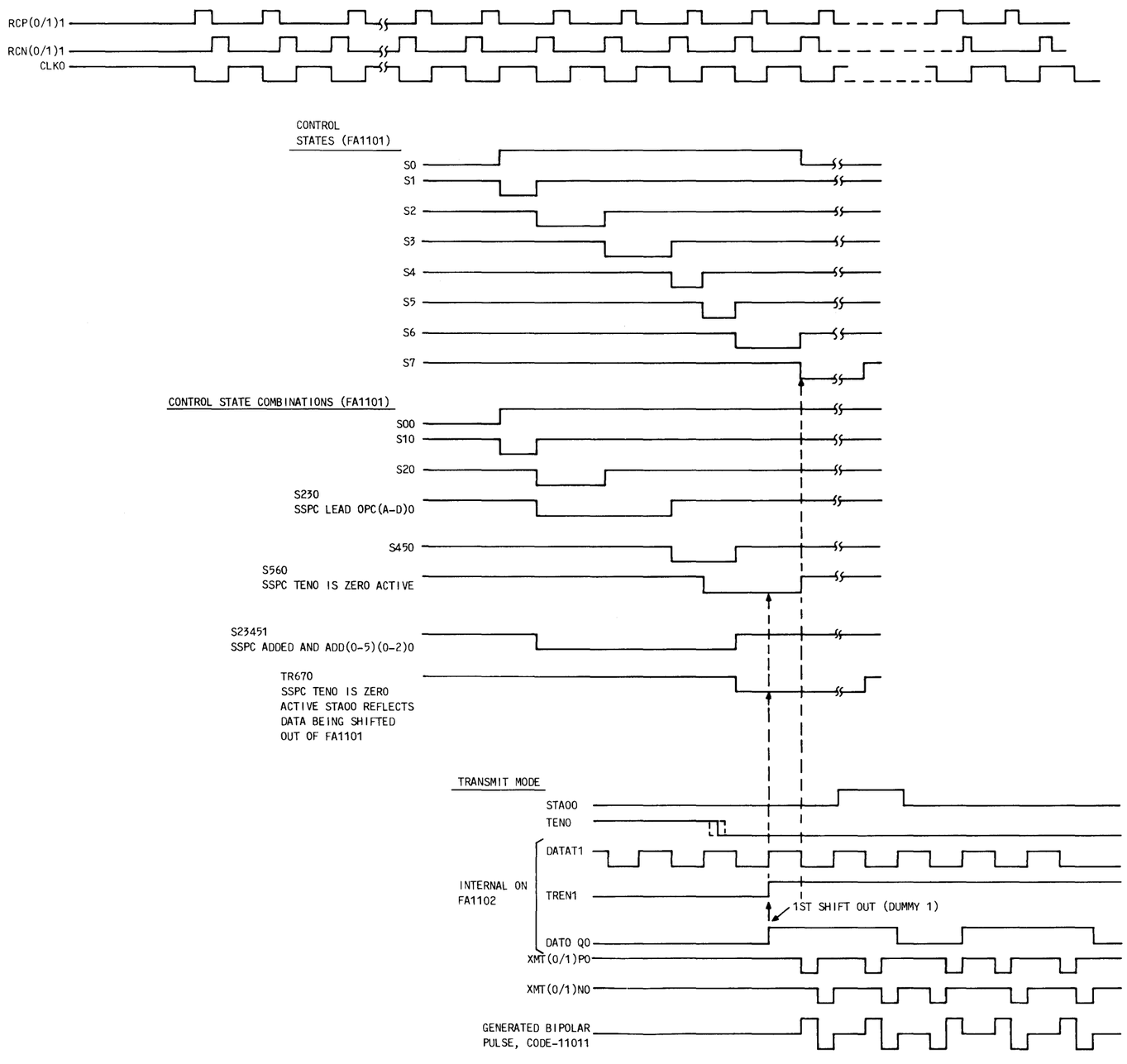

Fig. 11—I/O Control Timing

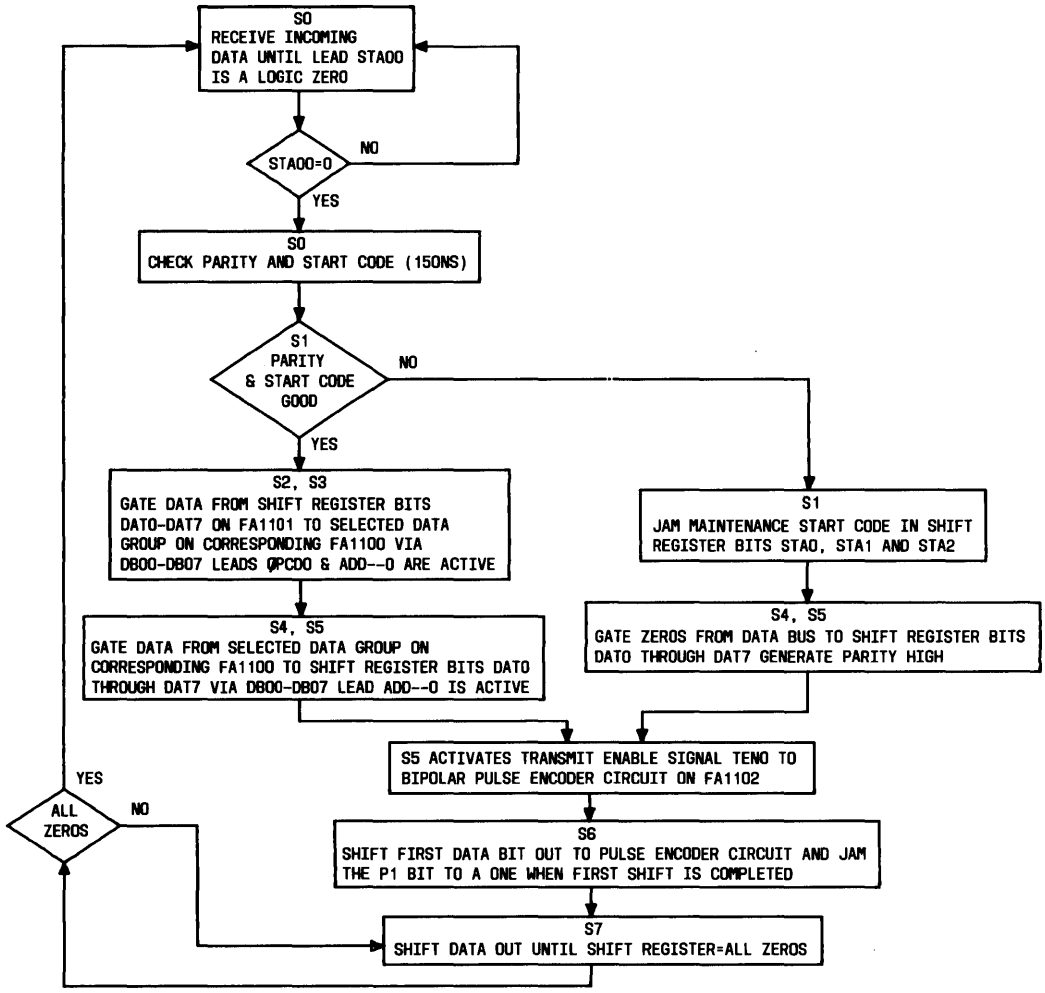

Fig. 12—I/O Control Flow Diagram

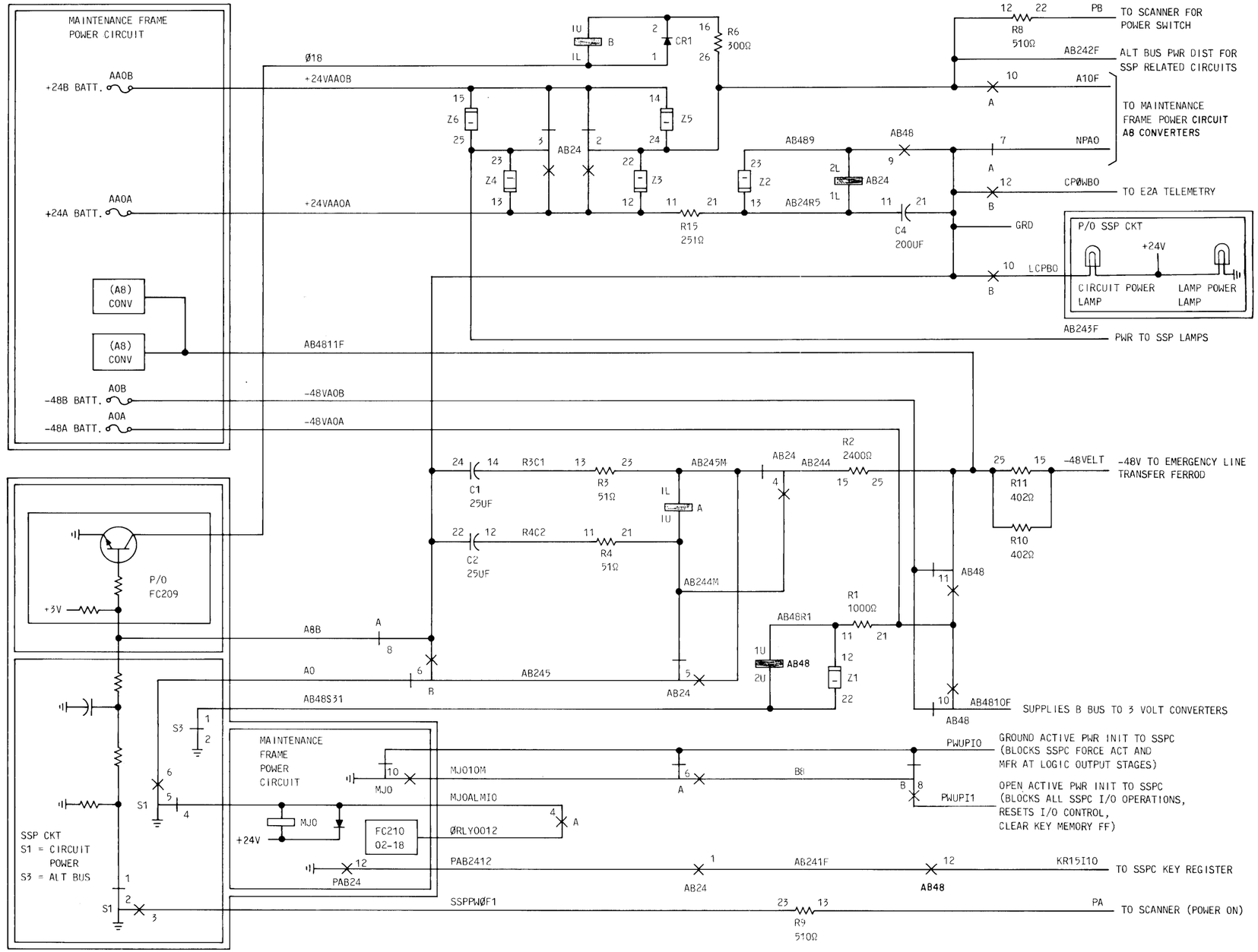

Fig. 13—SSPR Relay Logic

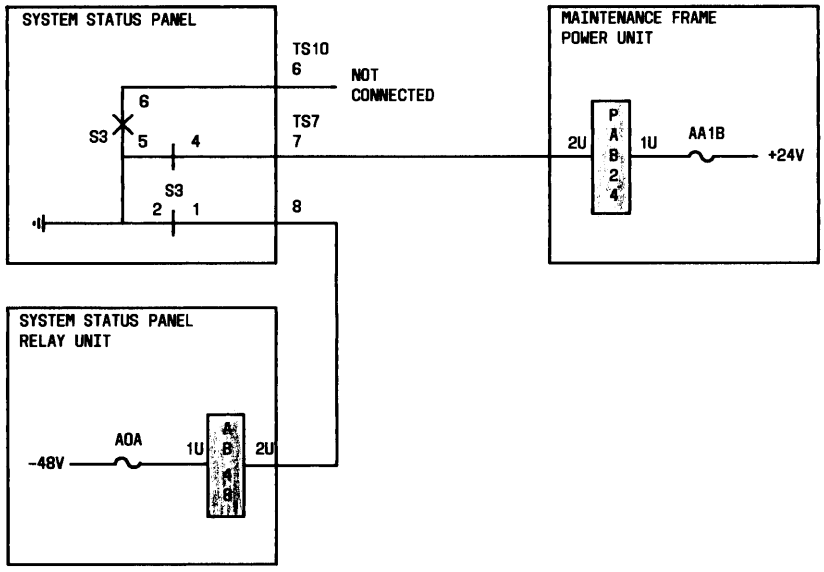

Fig. 14—ALT BUS Switch

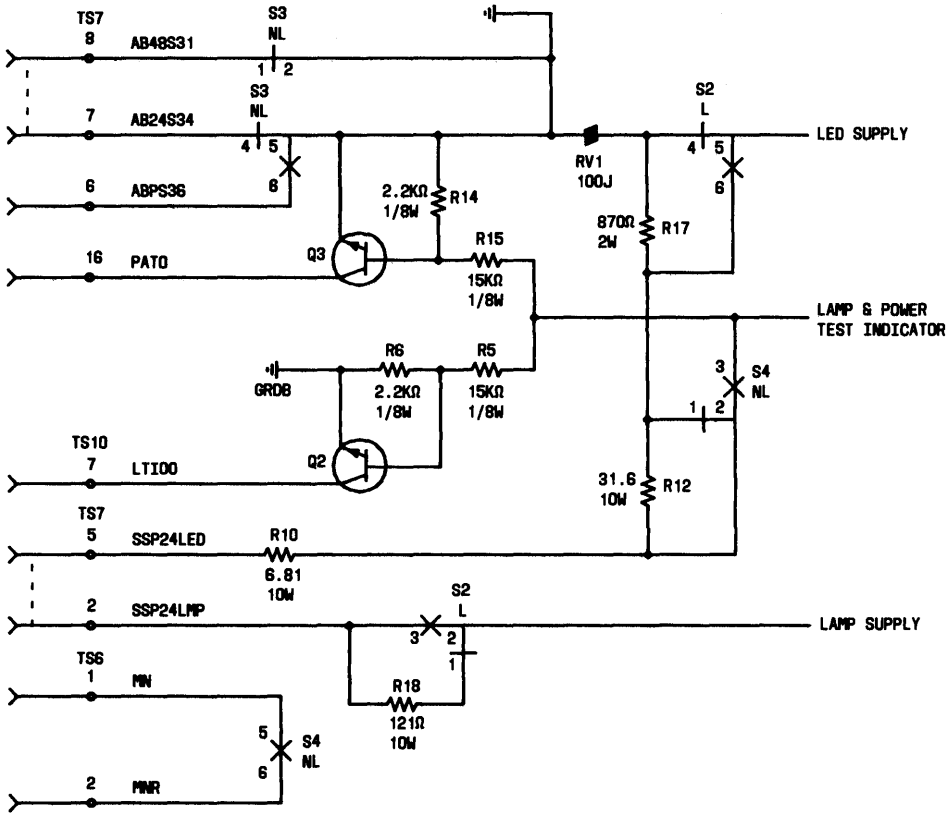

Fig. 15—Lamp and Power Test Circuits

TABLE A

SYSTEM STATUS AND CONTROL KEYS, LAMPS, AND LIGHT EMITTING DIODES

SUBAREA GROUPING	KEY/LAMP DESIGNATION	LAMP COLOR	INDICATION OR FUNCTION
PANEL POWER	ALT BUS (Key/Lamp) (S3)	Red	When depressed, initiates a switch from primary A power buses (+24V and −48V) to alternate B power buses. Lamp indicates a change in power supplied to SSP, SSPC, and SSPR. When released, restores operation to primary A power buses.
	CIRCUIT POWER (Key/ Lamp) (S1)	Green	When operated, switches SSP to B bus which lights SSP indicators and removes +3V from SSPC.
	LAMP POWER (Key/ Lamp) (S2)	Green	On-off switch used to supply 24 volts to the panel power lamp/ LED circuitry. When operated, power is reduced to a level that lamps/LEDs will not operate.
	LAMP & POWER TEST (Key) (S4)		When operated, causes all lamps/ LEDs to light.
CU0 (SYC0) or CU1 (SYC1) Status	LOCK (Key/Lamp) (S20)	Red	Prevents the off-line CU (SYC) from placing itself on-line or the on-line CU (SYC) from placing itself off-line.
	ACTIVE (LED)	Green	Gives visual indication of which CU (SYC) is on-line and processing.
	STANDBY (LED)	Green	Gives visual indication of which CU (SYC) is off-line and that the CU (SYC) is capable of being switched on-line (circuits working and temporary store is up to date).
	OUT OF SERVICE (LED)	Red	Gives visual indication that CU (SYC) is off-line for some maintenance or diagnostic purpose. Can be switched on-line but only under emergency conditions. (Temporary store is not up to date.)
	UNAVAILABLE (LED)	Red	Gives visual indication that CU (SYC) is off-line and cannot be switched on-line without manual effort from SSP or SCC.

TABLE A (Contd)

SYSTEM STATUS AND CONTROL KEYS, LAMPS, AND LIGHT EMITTING DIODES

SUBAREA GROUPING	KEY/LAMP DESIGNATION	LAMP COLOR	INDICATION OR FUNCTION
ALARMS	CRITICAL (LED)	Red	A visual indication of a total system loss or that a major portion or feature of the system is lost. Emergency response or craft action is required.
	MAJOR (LED)	Red	A visual indication of a partial loss of the system capability or a failure of the type that a similar failure could result in a critical condition. Immediate response or craft action is required.
	MINOR (LED)	Red	A visual indication of a minor loss of system capability or some condition requiring the attention of maintenance personnel but not immediately.
	MAJOR POWER (LED)	Red	A visual indication of a major failure in the power equipment. Immediate response or craft action is required.
	MINOR POWER (LED)	Red	A visual indication of a minor failure in the power equipment. Attention required but not immediately.
	FUSE (LED)	Red	A visual indication that a fuse has operated.
	ALARM CIRCUIT (LED)	Red	A visual indication of a failure within the office alarm circuit or its battery supply.
	SERVICE LOSS (LED)	Red	Indicates a manual initialization occurrence. Flashes during initialization.
ALARM CONTROL	(Key/Lamp) (S6)	Red	See Note.
	ALARM RELEASE (Key/Lamp) (S7)	Red	Requests restoration of critical, major, and minor alarms.
	(Key/Lamp) (S8)	White	See Note.
TEST CONTROL	EXECUTE (Key/Lamp) (S5)	White	Used to control the execution of repetitive or step functions entered via a TTY input message.
	PASS (Lamp) (S21)	Green	Indicates a test pass condition.
	FAIL (Lamp) (S22)	Red	Indicates a test failure condition.

Note: Refer to applications documents for the applicable system for information on the functions and panel designations of these indicators.

TABLE A (Contd)

SYSTEM STATUS AND CONTROL KEYS, LAMPS, AND LIGHT EMITTING DIODES

SUBAREA GROUPING	KEY/LAMP DESIGNATION	LAMP COLOR	INDICATION OR FUNCTION
MISCELLANEOUS LEDs and Lamps	SYSTEM NORMAL (Lamp) (S24)	Green	Indicates that all critical functions are normal.
	PANEL TIME OUT (Lamp) (S25)	Red	Indicates that the panel timer has timed out. A time-out (approximately 3 seconds) results in a critical alarm. Timer is usually reset by message from 3A CC every 100 ms.
	MAJOR EQPT LOSS (Lamp) (S23)	Red	Visual indication of equipment trouble or failure associated with one of the following seven LEDs.
	16 LED indicators to left of MAJOR EQPT LOSS lamp (Designations vary with system application.)	Red/ Amber	See Note.
	0 through 23 (LEDs)	Green	Visual means for display for memory words and scanner rows.

Note: Refer to applications documents for the applicable system for information on the functions and panel designations of these indicators.

TABLE B

SYSTEM EMERGENCY MANUAL CONTROL KEYS AND LAMPS

KEY/LAMP DESIGNATION	LAMP COLOR	INDICATION OR FUNCTION
ENABLE (Key/Lamp) (S9)	Red	When operated, allows initialization to be made by operation of any, none, or all of the SYSTEM INITIALIZATION keys and the INIT EXECUTE key.
(Key/Lamp) (S10)	Red	(See Note).
(Key/Lamp) (S11)	Red	(See Note).
(Key/Lamp) (S12)	Red	(See Note).
BACKDT OFFICE DATA (Key/Lamp) (S26)	Red	When operated, and INIT EXECUTE key is pressed, causes the older copy of office data to be loaded from tape into main memory during a bootstrap operation.
INIT EXECUTE (Key/Lamp) (S13)	Red	When operated, will generate a single MRF pulse to both CCs. ENABLE key must be activated before this key.
TTY INIT (Key/Lamp) (S14)	Red	When operated, causes the clearing of the TTY memory area via programmed routine.
(Key/Lamp) (S15)	Red	(See Note).
DISABLE REMOTE ACCESS (Key/Lamp) (S16)	Red	When operated, prevents control from remote SCC. The remote SCC still gets visual display of system status but does not exercise control.
SELECT 0 (Key/Lamp) (S17)	Red	When operated, CU 0 (SYC 0) may be forced on-line.
SELECT 1 (Key/Lamp) (S18)	Red	When operated, CU 1 (SYS 1) may be forced on-line.
FORCE (Key/Lamp) (S19)	Red	When operated, will force the selected CU (SYC) on-line. When released, restores system to software.

Note: Refer to applications documents for the applicable system for information on the functions and designations of these keys.