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1. GENERAL

INTRODUCTION

1.01 This section describes the Programmed Magnetic Tape Transport System (PROMATS) and contains the following information:

- (a) Physical description of the PROMATS including subassemblies, controls, and indicators
- (b) Functional theory of operation
- (c) Power requirements.

1.02 Whenever this section is reissued, the reasons for reissue will be listed in this paragraph.

EQUIPMENT CHARACTERISTICS

1.03 The PROMATS (Fig. 1) is designed to be an independent data storage unit requiring minimum control from its parent system. It is designed around two microprocessors (programmable controller or PROCON); one which controls the read operation of the PROMATS and one which controls the write and format operation. The operation of the two PROCONS is controlled by firmware programs stored in nonvolatile, static read only memories (ROMs). All control formatting and diagnostic functions performed by the PROMATS are controlled by the programs stored in the ROMs. The parent system provides macro-type commands that direct the PROMATS to execute a specified task. These commands are translated by the PROCONS into signals that control all the subsequent operations necessary to write or read data on the magnetic tape.

2. PHYSICAL DESCRIPTION

PROGRAMMED MAGNETIC TAPE TRANSPORT SYSTEM (PROMATS)

2.01 The PROMATS (Fig. 1) is installed in a standard 2-foot, 2-inch wide by 7-foot high single bay frame and consists of the following units:

- (a) J99384AA PROCON unit located at levels 71 through 75 of the frame.
- (b) J99384AB logic unit located at levels 63 through 67 of the frame.
- (c) J99384AC input/output (I/O) unit located at levels 59 through 63 of the frame.
- (d) KS-20571 tape transport located at levels 30 through 59 of the frame.
- (e) KS-21104 power supply (dc-to-dc converter) located at levels 18 through 30 of the frame.

PROGRAMMABLE CONTROLLER (PROCON)

2.02 The PROCON unit J99384AA (Fig. 1) consists of a J1C082B read PROCON, a J1C082A L20 controller PROCON, and an associated type 132 AB power supply located in a 4-inch high mounting plate assembly. The PROCON unit occupies levels 71 through 75 in the PROMATS frame. The PROCONS are 16-bit microprocessors whose functioning

is controlled by a series of instructions read from program store (a fixed, nonvolatile read only memory) which is an integral part of the PROCON. The read and controller PROCONs are essentially identical, differing principally in the amount of self-checking ability provided, the quantity of program store furnished, and the instructions encoded in the store. High-level instructions [from the 3A Central Control (CC) or direct memory access channels] are translated into detailed instructions by PROCONs and used by PROMATS to execute each task.

2.03 The PROCONs consist of integrated circuit packages mounted on multilayer etched circuit boards. The circuit boards, usually referred to as "circuit packs," are connected to the multilayer printed wiring backplane via 80-pin connectors. The circuit packs are contained in a 12-card housing similar to the ESS type 80-card housing. Power and ground connections to the packs in the housing are made through the various layers in the backplane. System interconnects are made by multipin connectors and tape cable.

2.04 The read PROCON is equipped with the fast clock (500 ns) and 1K of program store memory. It uses two data manipulation cards, one 16-bit control unit card, and one program storage unit card.

2.05 The controller PROCON is equipped with the fast clock and 2K of program store memory. Its card complement consists of four data manipulation cards, one 16-bit control unit card, and two program storage unit cards.

LOGIC UNIT

2.06 The J99384AB logic unit (Fig. 1) consists of 16 circuit cards and an ED97810 control and status display panel assembly mounted in three 14-card housings located at levels 63 through 67 in the PROMATS frame. The logic unit provides the internal interfaces from the tape transport unit to the read and write PROCONs, the duplex bus selector (DBS), and the local control panel. The logic unit:

- Receives and decodes commands from the external system

- Provides switches for manually inputting commands and lights for displaying data and status
- Receives and formats data to be recorded by the tape transport
- Provides error detection capability
- Provides status report capability
- Processes analog signals (read from magnetic tape) into digital format for use by the parent system.

INPUT/OUTPUT (I/O) UNIT

2.07 The J99384AC I/O unit (Fig. 1) consists of a J1C107A DBS unit located in the center third of a standard 4-inch high mounting plate. The DBS includes one FC398 circuit pack, one FC399 circuit pack, one FC400 circuit pack, three FC401 circuit packs, and one FC402 circuit pack. These packs are located in equipment locations 18, 19, 21 through 24, and 29 respectively. The DBS is used to provide the interface between the PROMATS and the data buses from the duplicated 3A CCs.

TAPE TRANSPORT

2.08 The KS-20571 tape transport (Fig. 1) occupies levels 30 through 59 of the PROMATS. It serves as the recording and reproducing medium for digital data supplied to and from the peripheral devices. The tape transport uses standard 1/2-inch wide magnetic tape and accommodates reels up to 10-1/2 inches in diameter. Data is recorded as phase-encoded signals at 25 inches per second and 1600 bits per inch (BPI). A 9-track format is used.

2.09 The tape transport contains only the electronic circuits that control the mechanical operation such as drive motors, solenoids, and relays. The circuitry for the read, write, and erase heads is contained in the logic unit.

2.10 A control panel (Fig. 1) is provided on the tape transport so that local control of the tape motion can be exercised for maintenance purposes or for loading or unloading tapes.

POWER SUPPLY

2.11 The KS-21104 power supply (Fig. 1) for the tape transport is located in levels 18 to 30 of the PROMATS frame. It is a dc-to-dc converter that converts the standard -48V primary power into +5V at 3.5A, +15V at 4.5A and -15V at 1.5A for the tape transport electronics and +15V at 4.5A, -15V at 4.5A and -24.5V at 14.0A for the mechanical operations. Over- and under-voltage and over- and under-current sensors and protective circuits are included in the power supply.

3. INTERFACES

3.01 The interface (Fig. 2) between PROMATS and the parent system is through the I/O unit (Fig. 3). A standard duplex bus selector (DBS) mounted in the I/O unit provides the means of connecting PROMATS to the two parallel channels of the duplicated 3A processor.

3.02 The DBS has a peripheral bus interface (PBI) to connect devices to the 3A CC. The PBI utilizes 36 leads including 6 address leads, 18 bidirectional information leads, 6 control leads, 5 response leads, and a clock lead. Each 3A CC (in a duplicated system) provides a parallel bus that connects to the DBS. The DBS, under 3A CC control, selects the parallel bus that will provide control and information then transfers that information from the bus to the logic unit.

3.03 The six address leads, labeled ADR (0) through ADR (4) and ADR (P), are used to select the peripheral device. The 18 bidirectional information leads are designated INF (0) through INF (15), INF (P_L), and INF (P_H). The parity bit for INF bits 0 through 7 is P_L, and P_H is the parity bit for INF bits 8 through 15.

4. THEORY OF OPERATION

4.01 The PROMATS consists of the following functional groups:

- (a) Bus interface unit (BIU)
- (b) Controller formatter (CONFORM)
- (c) Read system
- (d) Magnetic tape transport

(e) Power supply.

The boundaries of these functional groups do not coincide in all cases with the physical units which make up the PROMATS.

4.02 The bus interface unit consists of the following circuit packs mounted in the logic unit (Fig. 3):

- (a) FC 423
- (b) FC 427 (shared with the controller formatter)
- (c) FC 428.

4.03 The controller formatter (CONFORM) consists of the following units:

- (a) Controller PROCON mounted in the PROCON unit (Fig. 3)
- (b) FC 421, FC 422, FC 426, and part of an FC 427 circuit pack which are mounted in the logic unit
- (c) ED 97824 and 97825 circuit packs, which are mounted behind the display/control panel (Fig. 4).

4.04 The read system consists of the following units:

- (a) Three FC 429 circuit packs, three FC 431 circuit packs, two FC 432 circuit packs, one FC 430 circuit pack, and one FC 433 circuit pack, which are mounted in the logic unit
- (b) Read PROCON, which is mounted in the PROCON unit.

4.05 Refer to Fig. 5 for a diagram which depicts the signal flow within PROMATS and to Fig. 6 for a block diagram.

A. Bus Interface Unit

4.06 The bus interface unit (BIU) provides the interface between the duplex bus selector (DBS) and the 16-bit CONFORM bus. The BIU interprets 3A CC signals, generates return signals to the 3A CC, and detects bus-related errors. It also controls the transfer of commands, data, and status between the duplex bus selector and the

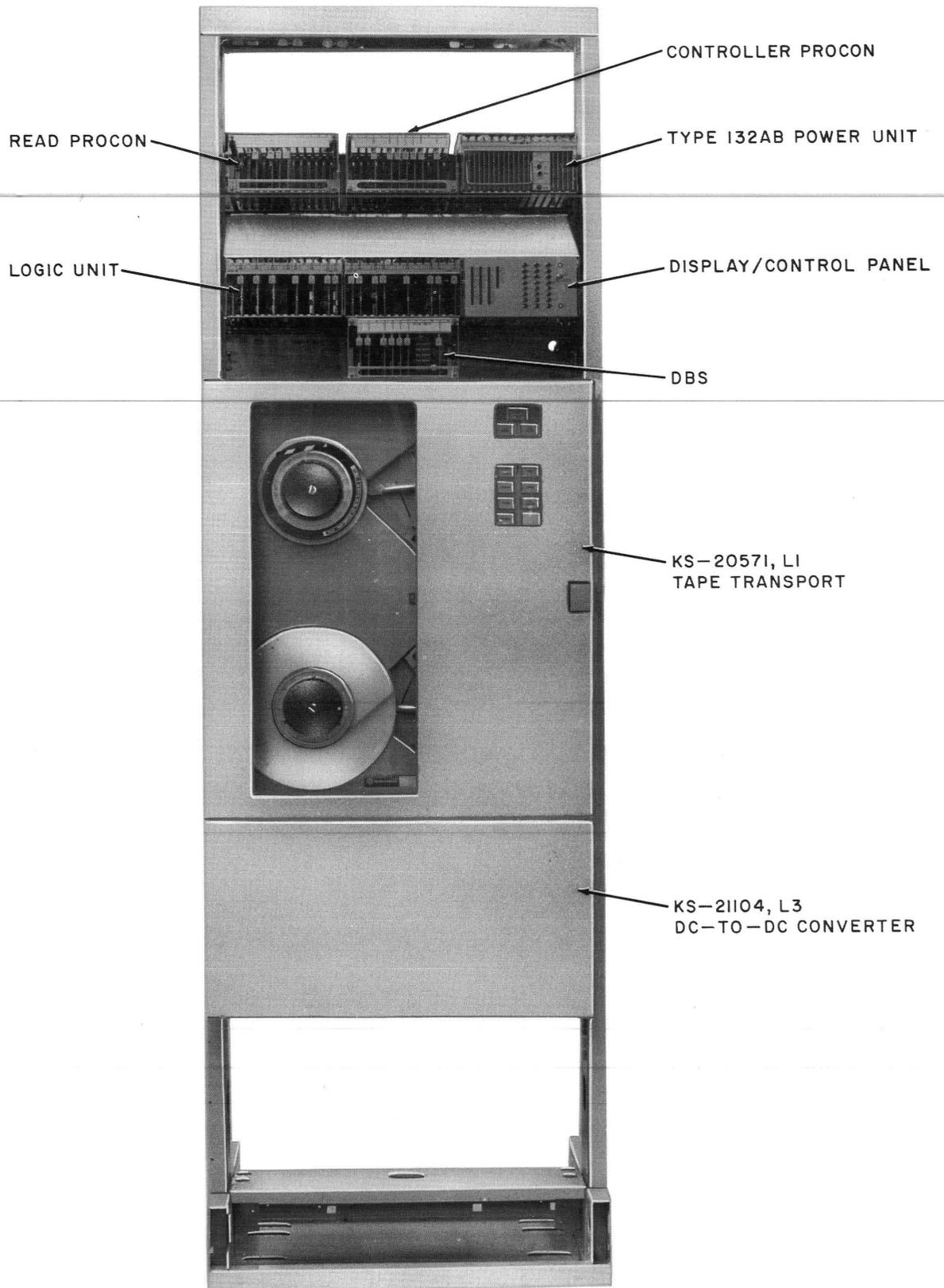


Fig. 1—PROMATS Frame, Front View

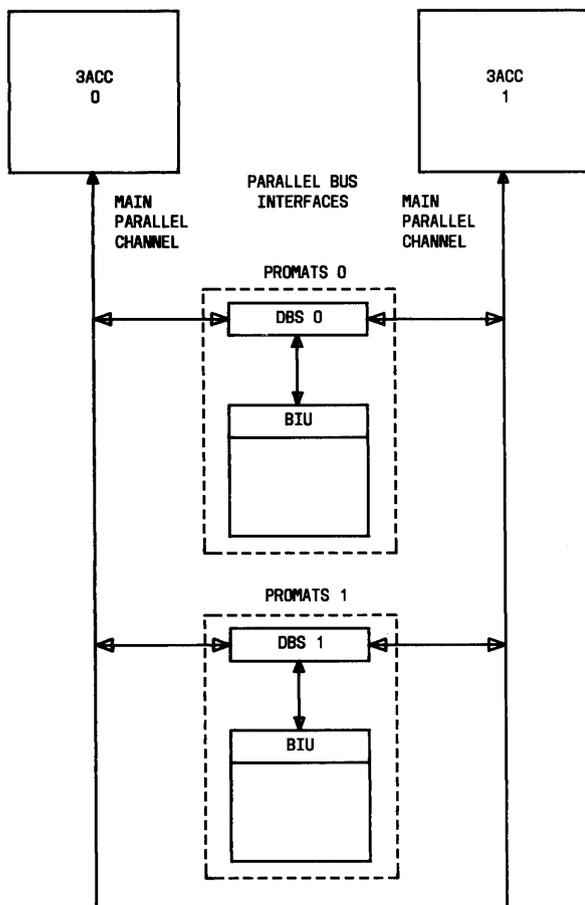


Fig. 2—PROMATS Interfaces

CONFORM. Strap options are provided for peripheral bus interface (PBI) or serial peripheral interface (SPI) operation, 6-bit device address selection, and DBS/SPI bus bit selection for interrupt response. The SPI option is not used in the TN.

4.07 Interface leads which connect BIU with DBS and CONFORM are shown in Fig. 7. A block diagram of BIU is shown in Fig. 8, and the equipment boundaries of BIU are defined in Fig. 9. The eleven control and response leads which provide the signaling path for transfer of data, commands, and status between the BIU and 3A CC (via the DBS) are listed in Table A.

4.08 All operations are initiated by the 3A CC setting the command present (CP) lead, setting the device address on the address leads, and placing the command word on the information (INF) leads. Refer to Fig. 7. The address decoder checks the address to ensure that the proper device

is being addressed. When the address is correct, the information-to-register (INFTRG) signal is produced to gate the command word present on the INF leads into the input-output register. The synchronization (SYNC) signal is returned to the 3A CC, and the command word in the input-output register is partially decoded to determine whether the command is for the CONFORM or the BIU. (Refer to Table B for the CONFORM command list.) A CONFORM command causes the command flag (CMDFLG) and BUSY signals to be set. The CONFORM responds within 2 microseconds by setting the command-to-information bus (CMDTIB0) signal which gates the command onto the controller input bus (CIB 0 through CIB 9). CMDFLG is reset by CMDTIB0. Decoding of a BIU command causes the flip-flop specified in the command to be set.

4.09 A write operation is initiated by inputting a CONFORM write command (WRITE ID, RECORD, or WRITE TAPE MARK) to the BIU. The command is processed as previously described. After CONFORM has decoded the command, write head power is turned on and the tape started forward. A 12-millisecond delay is inserted to allow the tape to get up to speed. The BIURDY signal is set, informing the 3A CC that the command is being processed. Approximately 1 millisecond after BIURDY is set, the first data word to be written is placed on the PBI. Succeeding words are transferred until the end of data (EOD) signal is received by the BIU. The time relationships in which these events occur is shown in Fig. 10

4.10 The CONFORM gates the high order data byte from the input-output register (INF 8 through 15 and INF P_H) onto CIB 0 through 8 with the data-high-to-information bus signal (DHTIB0). After 2 microseconds, the CONFORM gates the low order data byte from the input-output register (INF 0 through 7) and INF P_L onto CIB 0 through 8 with the data-low-to-information-bus signal (DLTIB0). This signal also clears the DATA FLG, BUSY and BIU ready (BIURDY) signals and sets the direct memory access request (DMAR) signal. This completes the transfer of a data word from the PBI to the CONFORM. The BIU can now accept another 18-bit word from the PBI.

4.11 When a data word is to be transferred to the PROMATS, the word is available to the BIU as an 18-bit word on information leads (INF 0 through 15, P_L , P_H). The word is accompanied

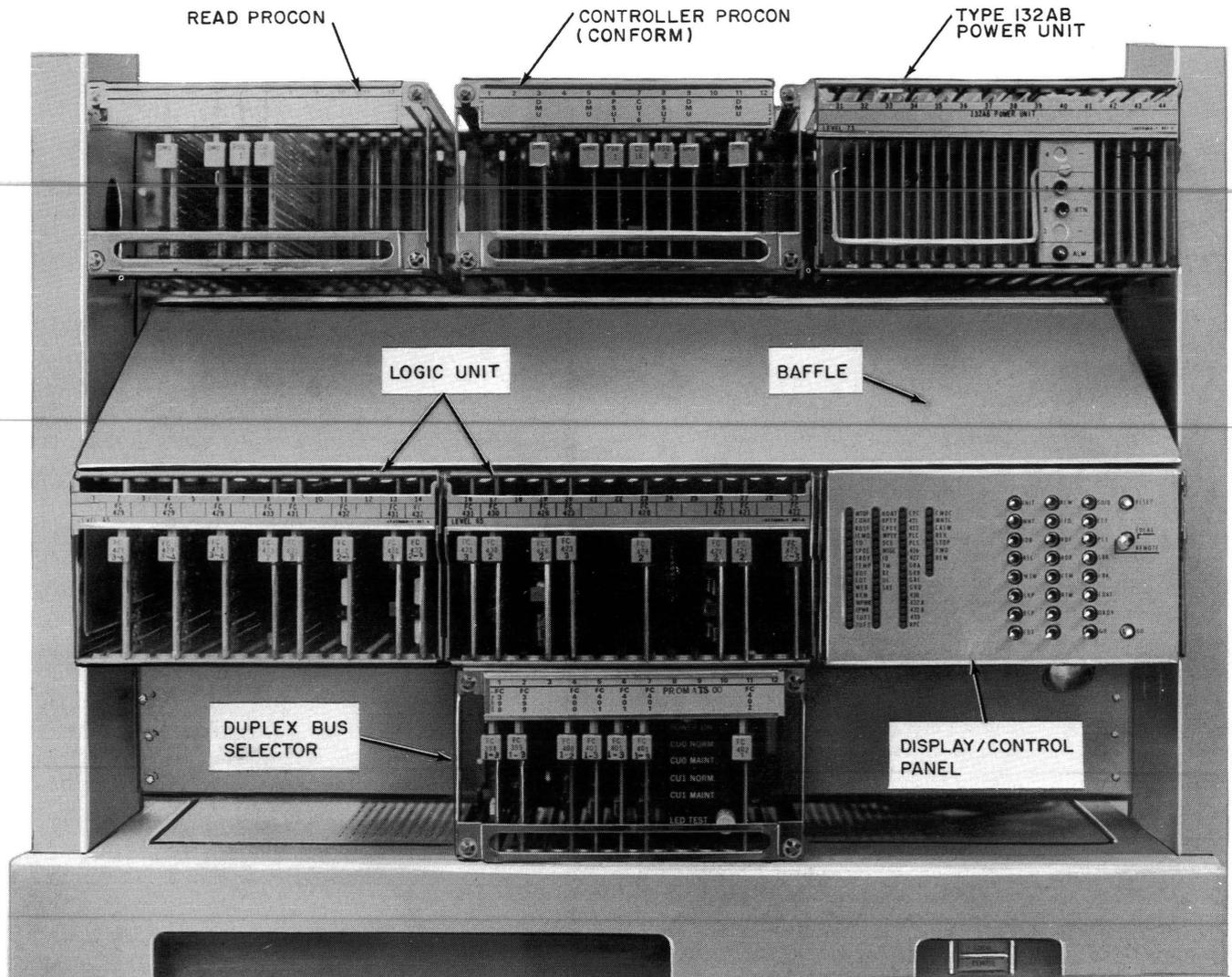


Fig. 3—PROMATS Frame, Upper Section

by the data present (DP) signal on the DP lead and the devices address on address leads (ADR 0 through 5). When the BIU accepts the word, the INFTRG signal gates the word into the input-output register. The data flag (DATA FLG) is set to inform the CONFORM that the word is in the register. The SYNC signal is generated at this time and returned to the 3A CC. The BUSY flip-flop is also set to indicate that the BIU is processing a word.

4.12 A read operation begins with the inputting of a READ command. The ADDR and DR signals set the DATA flip-flop to generate the register-to-information (RGTINF) signal. This gates

the contents of the I/O register onto the INF-0 through INF-P_H bus.

4.13 Data is transferred one byte at a time from CONFORM to the BIU I/O register. The data-high-to-register (DHTRG) signal gates the high-order byte first. The data-low-to-register (DLTRG) follows the DHTRG signal by 1.5 microseconds, gating the low-order byte into the I/O register. DLTRG also sets the word ready (WRDRD) flip-flop, clears the BUSY signal, and sets the BIURDY and DMAR signals.

4.14 Status word 0 (SW0) is composed of 10 status bits and 6 device address bits. Bits

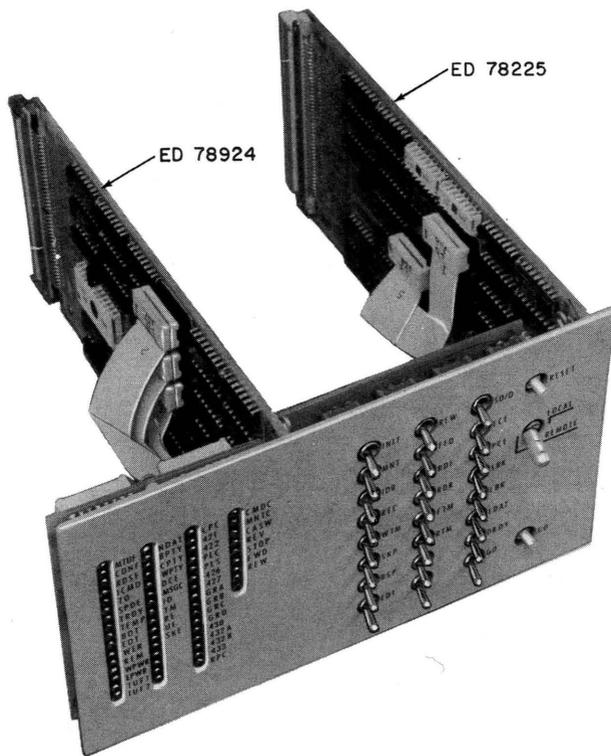


Fig. 4—Display Control Panel, Front View

0-5 represent the device address generated by BIU. Bits 6-11 are status bits generated by CONFORM and bits 12-15 are status bits generated by BIU. SW0 is available by inputting a send status (SST) command and ADDR. (Refer to Tables C, D, E, and F for the word formats for status words 0, 1, 2, and 3.) This combination sets SYNC; and if the BIU STATUS signal is clear, status word 0 is placed on the PBI bus by the status word 0-to-information (SW0INF) signal. When BIU STATUS is set, the status word stored in the I/O register is placed on the PBI bus by the status word-to-information (SWTINF) signal. No commands are sent to CONFORM during a SW0 request.

4.15 Status words other than SW0 may be obtained by inputting a status words (SWS) command to PROMATS. Approximately 22 microseconds after the command is accepted by the CONFORM, the requested status word is transferred to the I/O register by the status word-to-register (SWTRG) signal. SWTRG also sets the SWRG flip-flop to indicate that the I/O register contains the requested status word. The command complete (CMNDC) signal is generated 3 microseconds after SWTRG.

4.16 In order to obtain a status word other than SW0, it is necessary to input a status word select (SWS) command followed by a minimum of three send status (SST) commands. The first SST provides SW0 with the CMNDC bit cleared. The second SST provides SW0 with CMNDC set. The third SST provides the requested status word. Additional SSTs provide status word 0 with CMNDC set. Refer to Fig. 11 for the status word select timing diagram.

4.17 An interrupt operation is initiated when the BIU sets the interrupt (INTP) signal. The 3A CC (via the PBI) responds with an acknowledge interrupt (ACKI) signal which sets SYNC and the INF lead designated to identify the particular device. The trailing edge of the ACKI pulse clears the SYNC and INF lead. The INF lead that is set is predetermined by strapping in the FC 428 circuit pack in the BIU. The interrupt operation will function only if an interrupt enable (INTE) command was previously inputted to the BIU.

4.18 The PROMATS can be cleared by any of three commands. The initialize (INIT) signal is the simplest from a circuit standpoint. The leading edge of INIT generates a SYNC signal and a clear pulse which clears BIU and CONFORM. INIT is not used by the DBS, but may be used by the SPI. The BIU emergency stop (ESTP) command performs the same function except that it does not clear the SPI address flip-flop, and is the only clear function which resets the INTE flip-flop to disable the interrupt operation mode. The CONFORM INIT also clears the BIU and CONFORM by generating a POWER RESET signal.

4.19 A number of options for control and addressing are available by changing the connections on strap blocks on the FC 428 circuit pack. An 8-position block (STP 24) is used for establishing the PBI or SPI option. A 6-position block (STP22) is used for wiring the device address. Both STP 36 and STP 48 are 8-position blocks used to select the INF bit which identifies the device for interrupt acknowledge.

4.20 The end of a CONFORM command is denoted by the command complete (CMDC) signal. During maintenance, the end of each step is indicated by the maintenance complete (MNTC) signal. Either of these signals clears the BUSY flip-flop and sets interrupt (INTP) if interrupt enable (INTE) is set.

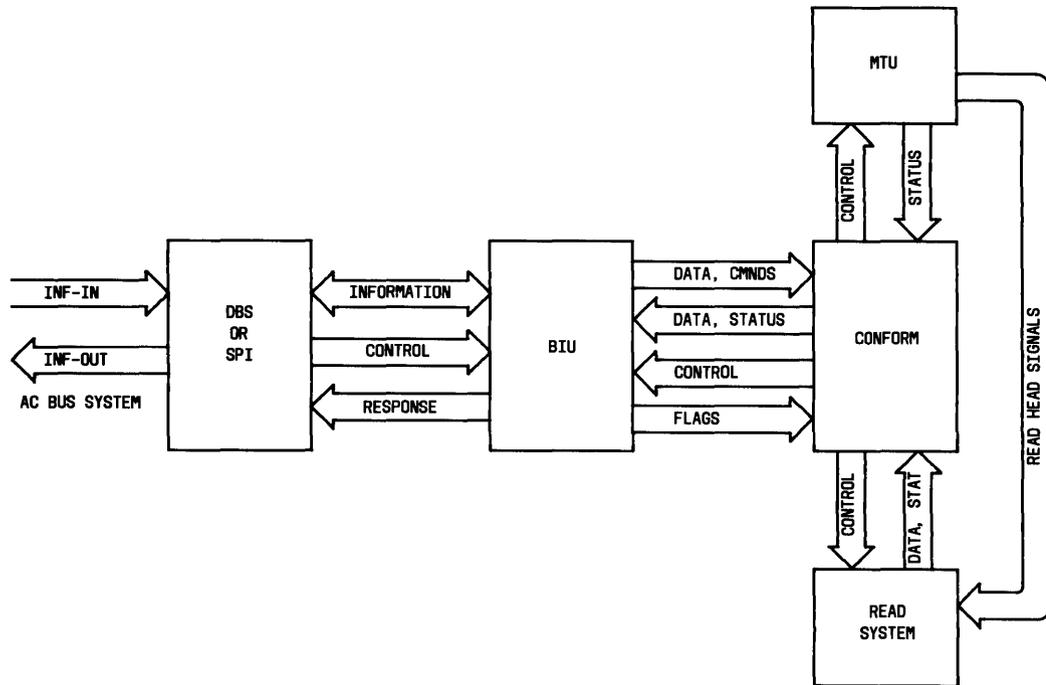


Fig. 5—PROMATS Internal Interface Diagram

B. Controller Formatter

4.21 The CONFORM used in the PROMATS consists of a 16-bit programmable controller (PROCON) and six related circuit packs. The CONFORM accepts and processes commands from the parent system, controls the motion of the magnetic tape, formats and records input data, formats output data, reports status, and performs maintenance and diagnostic tests.

4.22 A block diagram of CONFORM is shown in Fig. 12. The CONFORM communicates with BIU, the read system, and the tape transport via registers that access the PROCON input and output buses. The local control and display panel is also

shown in Fig. 6. When the PROMATS is in LOCAL mode, all the operational commands can be exercised from this panel. Contents of the four status registers and the last data character read can be displayed by the panel lamps. Switches are provided to change the data pattern and block length, provide an external clock, and reset both PROCONs.

4.23 The operation of the magnetic tape unit is controlled by a 4-bit register located on circuit pack FC 422. The commands to which the tape transport responds are STOP/START, FORWARD/REVERSE, HIGH/LOW, and 5/25 inches per second. The tape transport is controlled by these commands when the LOCAL/REMOTE

pushbutton indicator on the tape transport control panel is activated to the REMOTE position. Data is read or recorded at the speed of 25 inches per second. The high speed of 100 inches per second is used for rewind or fast forward. Four status bits (stop, forward, reverse, rewind) are returned from the tape transport to indicate tape motion. These bits are placed in status register 0 and are available to the parent system on request.

4.24 The I/O register in the BIU provides the interface between CONFORM and the parent system. When data is being written on tape, the contents of the 18-bit I/O register are gated onto the PROCON input bus in two 9-bit bytes. Data characters are gated into the data register on circuit pack FC 422 at 25-microsecond intervals. This register feeds the write head current driver on circuit pack FC 426. Data parity is checked in the BIU I/O register, at the inputs to the write-head current drivers, and at the output of the drivers.

4.25 CONFORM obtains data and status from the read system via a 16-bit read output register. This register contains data, read system status reports, or maintenance results.

4.26 Four status registers are provided to store information concerning system condition and results of command processing. The contents of these registers are not only available to the external system via BIU but also are displayed on the local control and display panel. Status register 0 is always available to the external system. Registers 1 and 2 are updated at the end of each command, and their contents are transferred to the BIU output register when a command requesting one of them is received. Register 3 is used only in the maintenance routine and is also available on command.

4.27 All CONFORM registers that send control signals to other system units can be read back into the PROCON to be compared with the original signals or will have status bits indicating that the command was executed properly. Figure 11 shows how these registers are connected to the PROCON bus. An error encountered during the execution of an operational command sets the CONFORM MALFUNCTION bit. An error during a maintenance routine sets a bit in status register 3, indicating where the error occurred. A PROCON all-seems-well (ASW) error will set the CASW bit in status register 0 and a flip-flop on circuit pack

FC 422. This flip-flop can be cleared with a reset or initialize command. When it is not cleared, the next attempt to execute an operational command sets the CONFORM FAILURE status bit.

C. Conform Commands

4.28 When idle, CONFORM PROCON is in a loop reading tape transport status. While in this loop, it writes into status registers 0, 1, and 2 and checks to determine whether a command is present. When a command is found, it is gated into CONFORM and decoded.

4.29 The INITIALIZE command resets the controller and read PROCONs and places the tape transport in the not-ready condition (reel motor brakes are on, and reel motor power is off). The status registers are cleared, the read system is checked, and the updated status is placed in the status registers. The initialize routine is executed when power is applied to the system, an initialize or emergency stop command (ESTP) is received, or the RESET pushbutton on the local control panel is depressed.

4.30 The WRITE ID command records a string of zeros that is 3.5 inches in length (ID burst) on track 4 of the tape. When the command is received, the tape transport is checked to see if the tape is positioned at the beginning of tape (BOT) marker. At the same time, a check is made to verify that the write and erase head power is off and that the tape transport is ready and in the remote mode. The head power is applied, and the start forward command is given to the tape transport. After a 12 millisecond delay, the tape transport status is checked to verify that head power is applied and that the tape is moving at the proper speed. The READ ENABLE signal to the read system is set and recording of the ID burst is begun. When the proper number of characters to fill 3.5 inches of tape has been written, recording is stopped. After a further delay of 2.5 inches of tape, a STOP command is given to the tape transport. Final status is checked, the results are placed in status registers 0, 1, and 2, and the command complete bit is set.

4.31 The RECORD command writes one block of data on the tape. When the command is received, tape transport status is checked, a START command is given to the tape transport, and the 12 millisecond delay is inserted to allow the tape

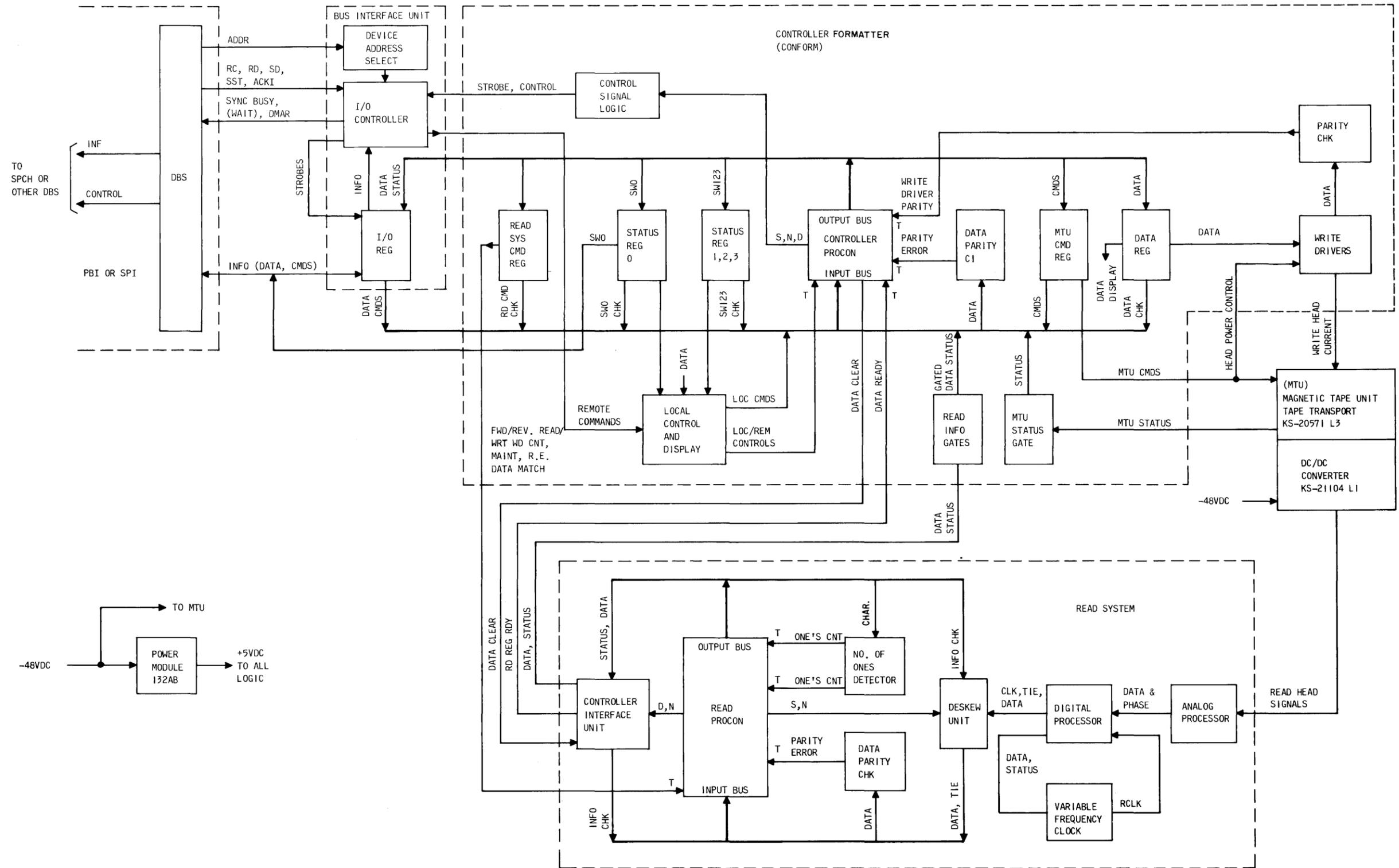


Fig. 6—PROMATS Block Diagram

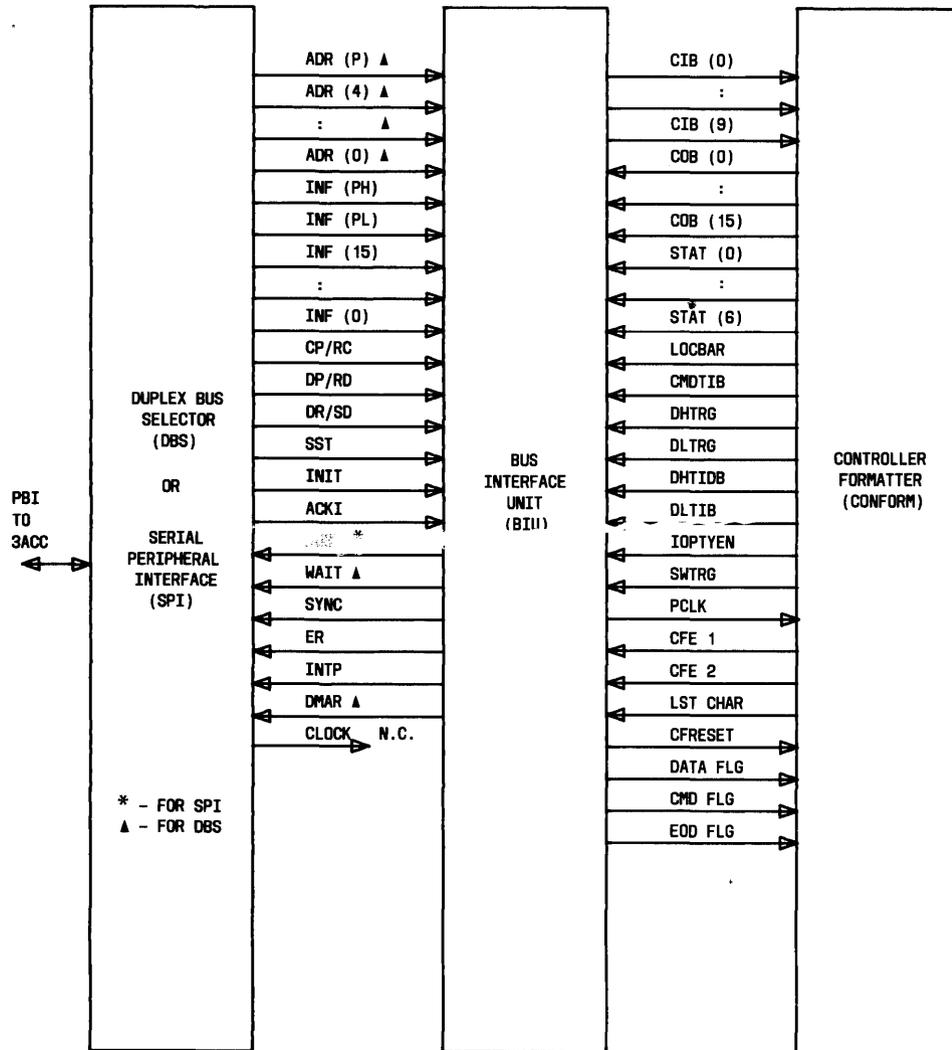


Fig. 7—PROMATS Interface Signals

to get up to speed. The tape transport status is rechecked; and if no errors are found, the preamble is written. The preamble consists of 40 all-zeros characters, followed by an all-ones character. Parity is checked on the data register and write drivers. If an error is found, that information is stored in the PROCON to be outputted as part of status at the end of the command. The data ready (DRDY) lead (PROCON test lead T0) is checked to see whether it is set, which indicates that data is available in the BIU I/O register. If DRDY is not set (ie, there is no data present) the postamble (an all-ones character followed by 40 all-zeros characters) is written on tape, and a NO DATA indication is set in status register 2. Data, when ready, is read from the BIU I/O register and stored

in PROCON general register G1 for the first character and G2 for the second character. After the preamble is written, the next character to be written on the tape is the first phase character associated with input data. The phase encoded format involves generation of "phase characters" associated with data characters. If two successive data bits on a tape track are alike (that is, both are ones or both are zeros), a phase bit must be written in between so that the second data bit transition will have the proper polarity to identify it as a one or a zero. When successive data bits are not alike, a phase bit is not required between them. The set of phase bits written before a data character constitutes the phase character associated with that data character. After the first data

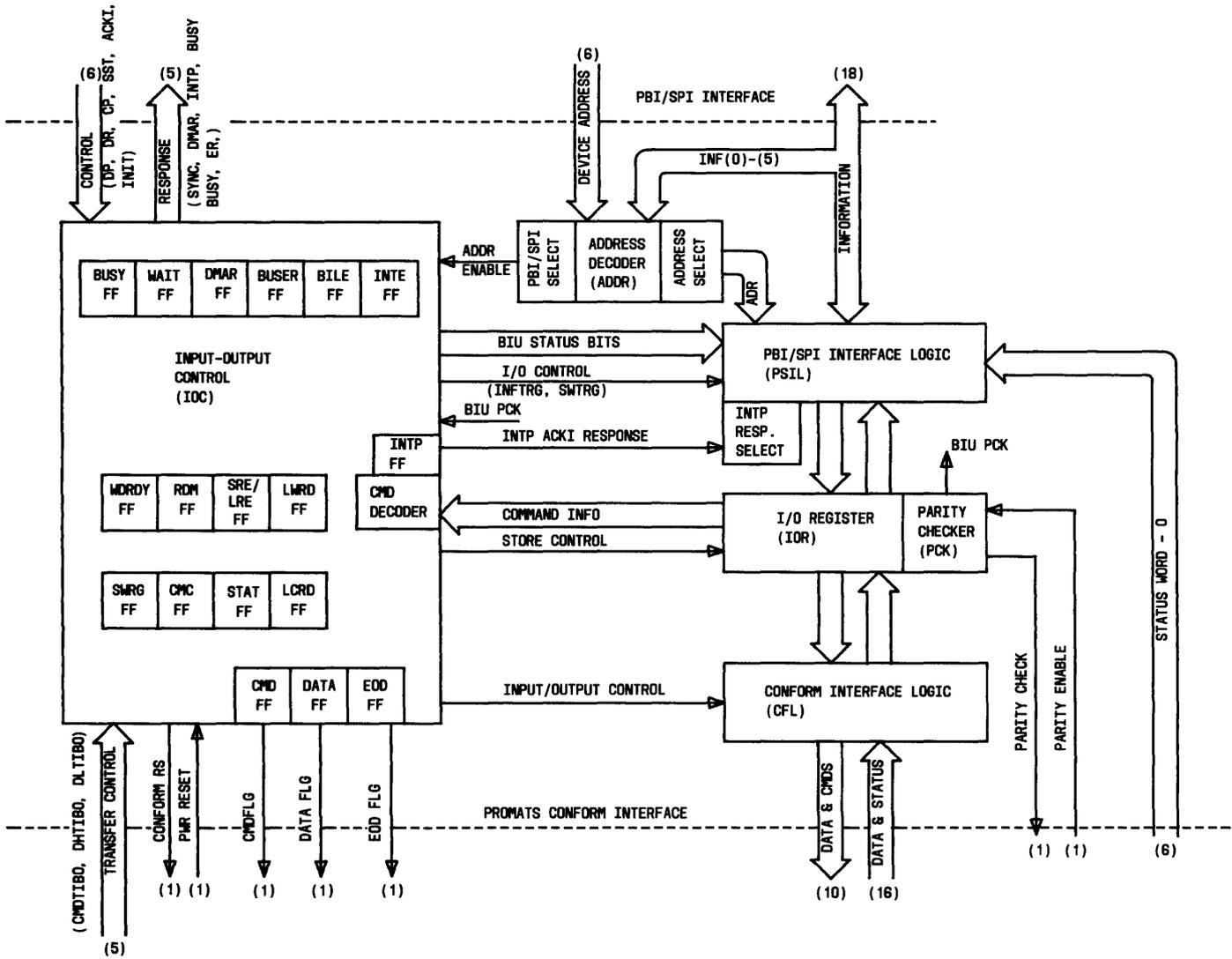


Fig. 8—BIU Functional Block Diagram

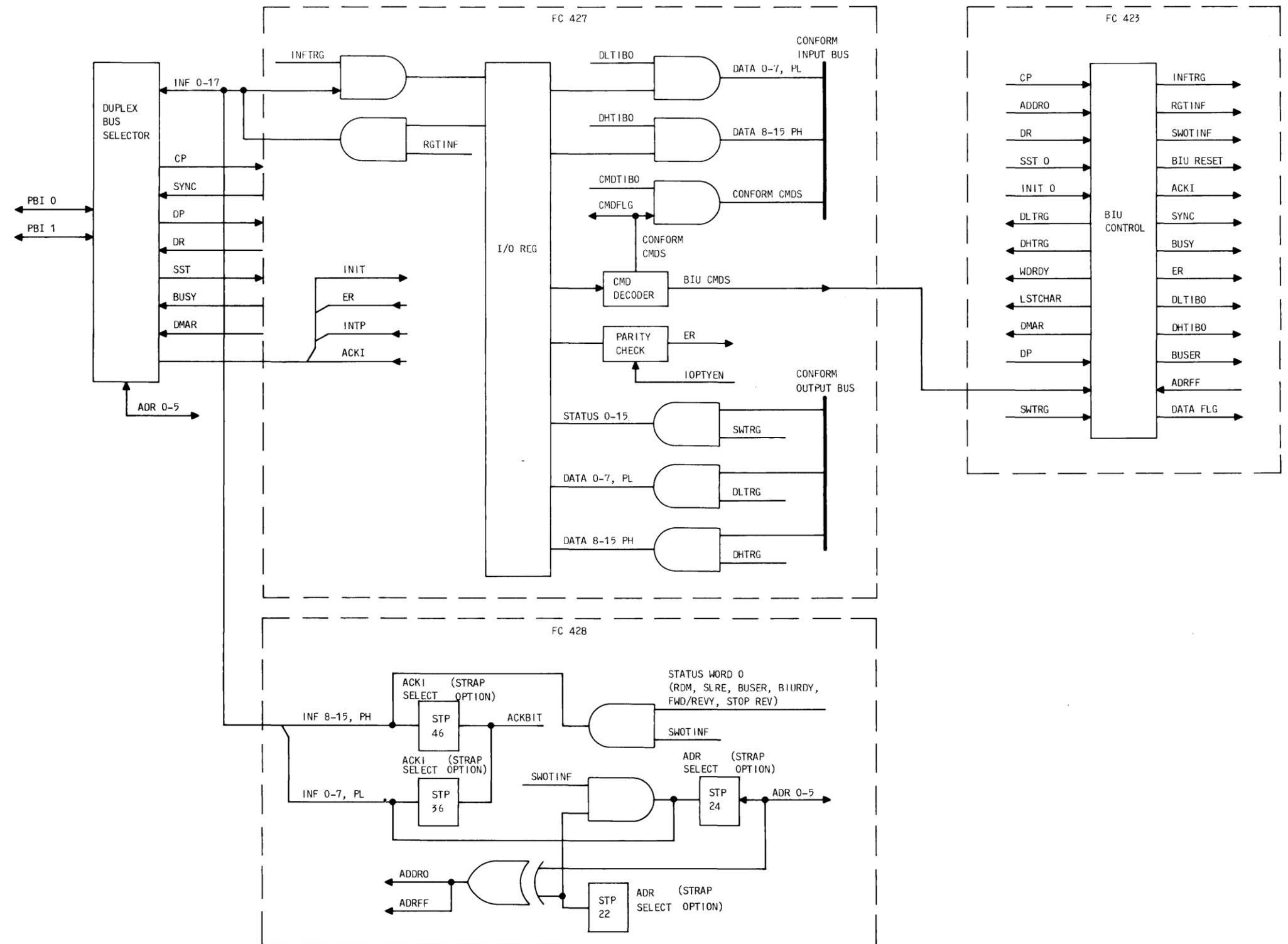


Fig. 9—BIU Block Diagram

TABLE A

INTERFACE SIGNALS BETWEEN BIU AND PBI

MNEMONIC	DESCRIPTION
CP (Command Present)	Informs the BIU that a command is present on the INF leads.
DP (Data Present)	Informs the BIU that a data word is present on the INF leads.
DR (Data Request)	Informs the BIU that the PBI is ready to accept a data word.
SST (Send Status)	Informs the BIU that one of the four PROMATS status words is being requested.
ACKI (Acknowledge Interrupt)	Requests the BIU to set an INF lead to identify itself as the interrupting device.
INIT (Initialize)	One of the signals that causes the PROMATS to be initialized. Used on SPI only.
BUSY	Informs the PBI that the BIU is not ready to send or accept information.
ER (Error)	Informs the PBI that an error has been detected by the PROMATS.
INTP (Interrupt)	Informs the PBI of a command-complete or maintenance-complete status.
DMAR (Direct Memory Access Request)	Informs the PBI that data can be transferred during DMA mode of operation.
SYNC	Informs the PBI that the BIU is responding to a control signal.

character is written, parity is checked on the data register and the write drivers. The second phase and data characters are written in the same manner as the first. A timing diagram for the record sequence is shown in Fig. 10.

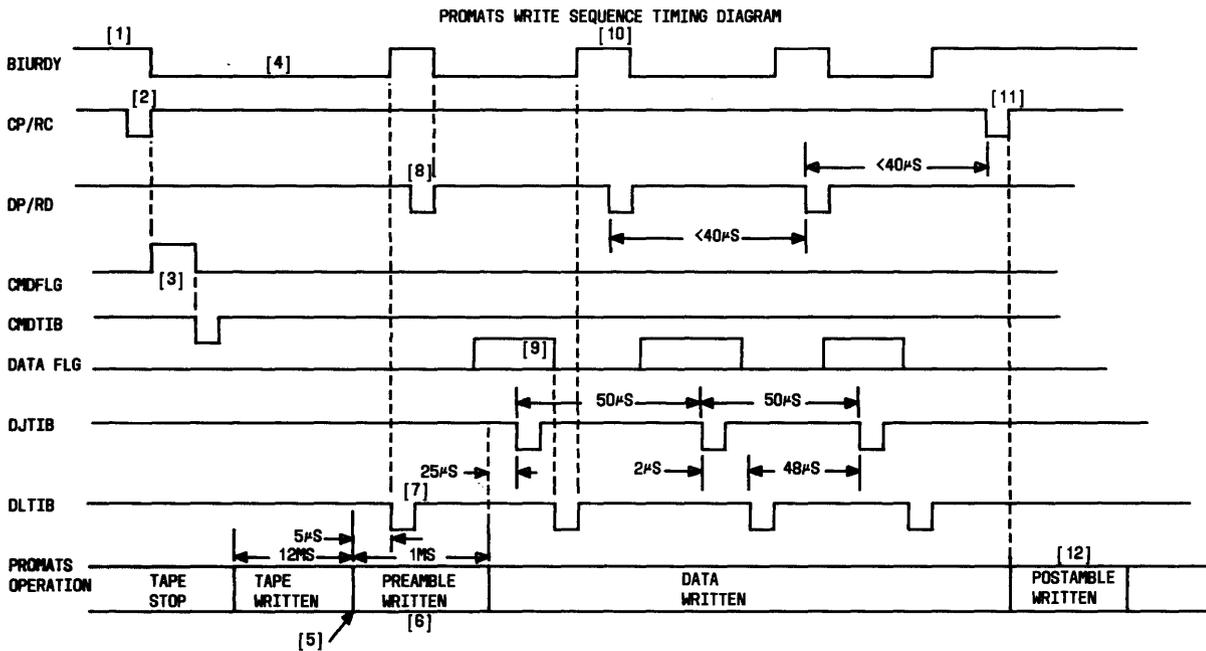
4.32 Once the second data character is written, the data end (DEND) signal (PROCON test lead T2) is checked to determine whether additional data is ready. If there is, the recording process is repeated until the end-of-data flag is received (DEND is set). The recognition of DEND initiates the writing of the postamble, which consists of an all-ones character and 40 all-zeros characters. The tape speed is now checked by measuring the time

interval between the writing and reading of the last character. If the time is not correct, the SPEED ERROR bit in status register 1 is set.

4.33 During the recording process, a count of the number of bytes (9-bit characters) obtained from the BIU is kept in PROCON register G4. The read system counts the number of characters it reads. The two counts are compared, and the DATA COUNT ERROR bit in status register 2 is set if they are not the same. The stop subroutine is then executed, and the final read system status is placed in bits 6 through 10 of status register 2.

TABLE B
CONFORM COMMAND REGISTER WORD FORMATS

BIT	COMMAND	COMMAND	COMMAND
0	Initialize	Rewind	Status Register 1 Request
1	Maintenance	Fast Forward	Status Register 2 Request
2	Write ID	Read Forward	Status Register 3 Request
3	Record	Read Reverse	
4	Write TM	Forward to TM	
5	Skip	Reverse to TM	
6	Backspace		
7	Edit		
8	1	0	1
9	0	1	1



- [1] PROMATS READY FOR COMMAND
- [2] WRITE COMMAND
- [3] COMMAND TRANSFERED TO CONFORM
- [4] PROMATS NOT READY FOR COMMAND OR DATA
- [5] TAPE UP TO SPEED
- [6] PREAMBLE WRITTEN (41 CHAR.)
- [7] SET BIURDY
- [8] DATA INPUTED TO BIU
- [9] DATA TRANSFERED TO CONFORM, DATA FLG → DGTIB, DLTIB
- [10] PROMATS READY FOR MORE DATA
- [11] END OF DATA COMMAND, EOD FLG SET
- [12] POSTAMBLE WRITTEN

Fig. 10—PROMATS Record Sequence Timing Diagram

TABLE C
STATUS REGISTER 0 WORD FORMAT

BIT	DEFINITION
0	Device Address Bit 0
1	Device Address Bit 1
2	Device Address Bit 2
3	Device Address Bit 3
4	Device Address Bit 4
5	Device Address Bit 5
6	Command Complete
7	Maintenance Step Complete
8	Controller ASW
9	Reverse
10	Stop
11	Forward/Rewind
12	BIU Ready
13	Bus Error
14	Short/Long Record Error
15	Read Data Missing
PL	0
PH	0

4.34 The WRITE TAPE MARK command is used to write an identification symbol on tape. This mark is 128 flux reversals at 3200 reversals per inch on tracks 2, 5, and 8, while a constant bias current is maintained in all other tracks.

4.35 When the WRITE TAPE MARK command is received and decoded, the CONFORM and tape transport status is checked and the tape started forward. Status is rechecked to ensure that after 12 milliseconds the tape has reached a speed of 25 inches per second. PROCON general registers G1, G2, and G4 are loaded with the tape mark character, phase character, and character count, respectively. Special 3-bit characters are written on tape until the character count has been decremented to zero. The tape is then stopped, system status is obtained from the read system and added to the status report.

4.36 The SKIP command is used to ERASE 6 inches of tape. PROCON checks status of the tape transport and CONFORM. Write and erase head power is turned on, then the tape is started forward. The time necessary to write 6 inches of tape is measured by a delay counter composed of PROCON registers G1 and G6. At the end of the delay period, the tape transport is stopped. The read system is not enabled during the SKIP routine.

4.37 The BACKSPACE command is used to reverse the tape over a block of data, a tape mark, or an ID burst. When the command is decoded, tape transport status is checked. Status is checked to ensure that the BOT marker has not been reached. The tape transport overtemperature, EOT, and write enable ring bits in the status register are not checked. A reverse command is issued and after 12 milliseconds delay, the tape transport status is checked to make sure the tape is up to speed. The tape is read in the reverse direction until the read system determines that an ID burst, tape mark, unrecoverable error, or preamble has been found. At that time, PROCON issues a command to stop the tape, place the final status into the status registers, and terminate the command. If no data are found after approximately 10 inches of tape has been read, the time-out status bit is set and the command is terminated.

4.38 The EDIT command erases a block of data and inserts a new block in its place. [The new data block cannot be longer than the old block to avoid shortening the interblock gap (IBG) or overwriting the next data block.] The block to be edited should be found by a normal READ FORWARD operation which properly positions the block for the editing process. After the command is received and decoded, PROCON checks tape transport and CONFORM status, then gives a start reverse command to move the tape in reverse with write head power on to erase the block that is to be edited. During this time the read system is looking for the end of the block. If the BOT marker, an ID burst, or a tape mark is found, the illegal command status bit is set and the tape is stopped. An unrecoverable error (two or more tracks with no data written) detected by the read system indicates that the end of a bad block of data has been reached. Either an end of data or an unrecoverable error report indicates that the data block has just been read. (The read head is at the front end of the block to be edited.) Reverse

TABLE D
STATUS REGISTER 1 WORD FORMAT

BIT	DEFINITION
0	MTUF—MTU Malfunction
1	CONF—Controller/Formatter Malfunction
2	RDSF—Read System Malfunction
3	ICMD—Illegal Command
4	TO—Time-Out
5	SPDE—Speed Error
6	TRDY—MTU Ready
7	TEMP—MTU Temperature High
8	BOT—Beginning of Tape
9	EOT—End of Tape
10	WER—Write Enable Ring In
11	REM—MTU in Remote
12	WPWR—Write Head Power On
13	EPWR—Erase Head Power On
14	TUF1—MTU Failure 1—AC Power, Arms Off Normal, Servo Lamp
15	TUF2—MTU Failure 2—DC Power, Door Open, Tape Absent

TABLE E
STATUS REGISTER 2 WORD FORMAT

BIT	DEFINITION
0	NDAT—No Input Data
1	BPTY—Bus Controller Parity Error
2	CPTY—Controller Output Parity Error
3	WPTY—Write Driver Parity Error
4	DCE—Data Count Error
5	MSGC—Missing Tape Character
6	ID—ID Read
7	TM—TM Read
8	RE—Recoverable Error
9	URE—Unrecoverable Error
10	SKE—Skew Error

tape motion continues. Now the size of the interblock gap between the block that has just been read and the block preceding it is measured. Two PROCON general registers (G3 and G4) are initialized. Register G3 is loaded with a value which corresponds to a maximum wait time of 6 inches of tape. Register G4 is used to measure the time required to traverse the interblock gap. When the read system starts reading information again or when the maximum distance is covered, write-head power is removed while reverse motion continues. A count which corresponds to the read-to-write head distance (0.3 inches) is subtracted from the count in G4. G4 now contains the width of the interblock gap that must be reproduced when new data is to be recorded. The tape continues in the reverse direction until read system indicates that it has identified what it has been reading. If the BOT marker, ID burst, tape mark, or unrecoverable error is found, a command is given to stop the tape. If another preamble is found, tape motion continues until the end of this block of data is

TABLE F
STATUS REGISTER 3 WORD FORMAT

BIT	DEFINITION
0	CPC—Controller PROCON Error
1	421
2	422
3	PLC—Panel Local Control, ED 97824
4	PLS—Panel Local Status, ED 97825
5	426
6	426
7	GRA—Group A Error
8	GRB—Group B Error
9	GRC—Group C Error
10	GRD—Group D Error
11	430 Error
12	432A Error
13	432B Error
14	433 Error
15	RPC—Read System PROCON Error

reached. The tape is now started forward, the read system is enabled, and an ID burst tape mark or block of data is read through. At this time, regardless of the type of information previously read, the tape is at the beginning of the interblock gap preceding the location where the new block of data is to be written. Register G4 is now decremented. When it reaches zero, the write-head power is applied, and a jump is made to the record routine to write the new block of data.

4.39 The REWIND command is used to rewind the tape to the BOT marker. When the command is decoded, the tape transport status is checked to ensure that the tape is not already at the BOT marker. After the rest of the tape transport status and the CONFORM status is checked, the start, reverse, and high speed bits are set in the transport command register. PROCON enters a wait loop to read status and to monitor tape speed until the BOT marker is reached. A counter is also initialized to verify that the tape

is up to maximum speed within 200 milliseconds. As soon as the marker is reached, another loop is established to determine when the marker is passed. Detection of the no-marker condition causes the tape to be moved forward at 5 inches per second until the marker is reached again. The tape is then stopped on the BOT marker and the status registers are loaded with system status.

4.40 The FAST FORWARD command is identical to the REWIND command except that the tape is moved forward to the end-of-tape marker.

4.41 The READ FORWARD command is used to read one block of data and output it to the BIU. When the command is decoded, tape transport status is checked and tape motion started. When the transport speed check indicates that the tape is up to speed, the read system is enabled. If the BOT is found, tape motion continues until the marker is passed. If an ID burst, tape mark, or unrecoverable error is found, the tape is stopped and status is recorded in the status registers. Detection of a preamble causes a wait counter (register G5) to be loaded and the data-count register (G4) to be zeroed. The wait-count register is loaded with a number large enough to wait for the end of the preamble. Test lead T1 is tested periodically to determine whether the register-ready flag is set by the read system indicating that it has data ready to be taken. Each test causes the wait count in register G5 to be decremented. The unrecoverable error bit is set and the subroutine exited if the count goes to zero.

4.42 Data is received from the read system in 9-bit bytes. Two bytes are assembled into an 18-bit word in the BIU I/O register. Bit 15 of the read-interface register is checked to determine whether a malfunction exists in the read system, and bit 14 is checked to verify the presence of data in the register. The byte is stored and the last-character flag from the read system is checked. An even number of characters should always be present when the last-character flag is received. Detection of the presence of an odd number of characters and the last-character flag simultaneously will set the missing character flag in status register 2 and load all ones into the second byte of the word. When the last character is not present, the data count in register G4 is incremented by one, and more data is requested from the read system. The second data byte is stored before the word is transferred to the BIU I/O register.

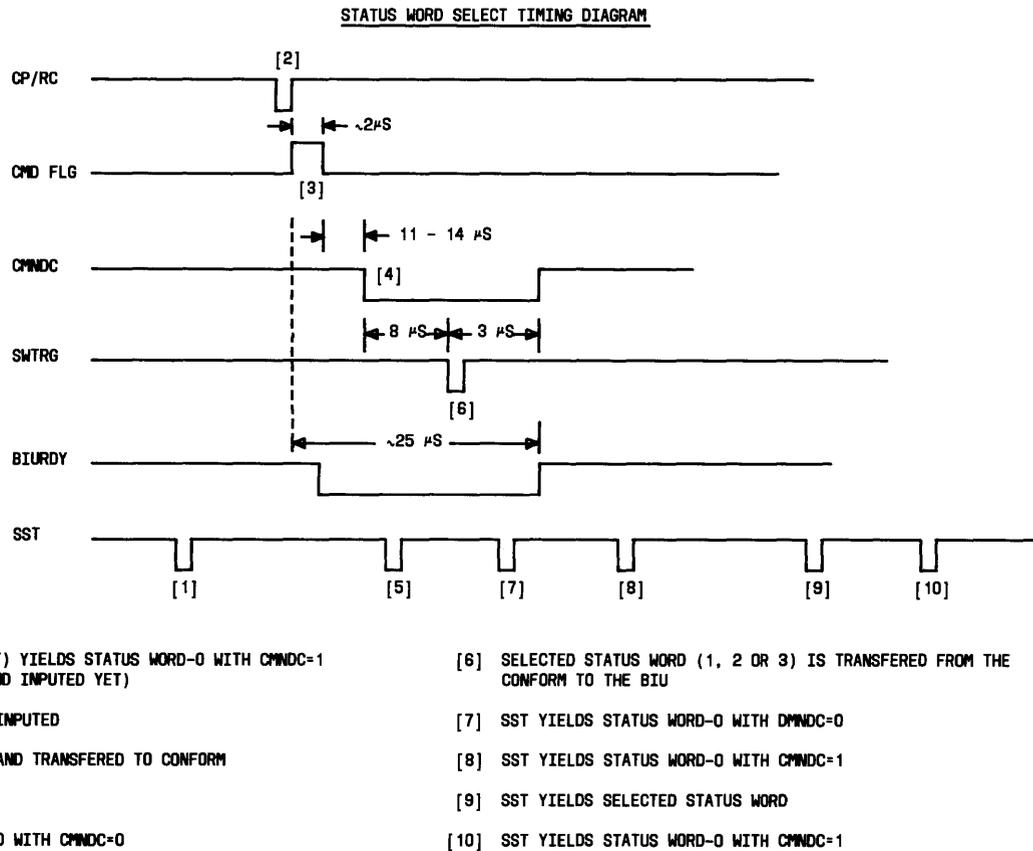


Fig. 11—Status Word Select Timing Diagram

Parity is checked after the word is in the I/O register and the word count is incremented. The read system is checked to determine whether all data has been received. When all data has been received and transferred to BIU, the last-character flag to BIU is set. The tape is then stopped and read system status is obtained and added to the status registers.

4.43 The READ REVERSE command is used to read the tape when it is moving in the reverse direction. It is similar to the read forward and uses many of the same subroutines. Only read operations can be performed in the reverse direction; write head power is not applied at any time during READ REVERSE.

4.44 A flux reversal that would be read as a one in the forward direction becomes a zero when read in reverse, so the signals that are read from tape must be inverted in order to recover

the data. In addition, the data is output in the reverse order from that in which it was written.

4.45 A different stop procedure is used in the reverse direction because a longer delay is needed before the stop command is given in order to center the heads in the interblock gap.

4.46 The FORWARD TO TAPE MARK command is used to scan the tape until a tape mark is found. Tape transport status is checked and the tape motion is started. A delay counter is established to count the number of times that the read system detects data rather than a tape mark. The counter decrements each time a preamble is detected. If the counter decrements to zero, the command is terminated and the time-out bit is set in status register 1. PROCON continues to loop until the tape mark is identified or an unrecoverable error (no identifiable signals) is found. At that time the tape is stopped and a read system status report is obtained.

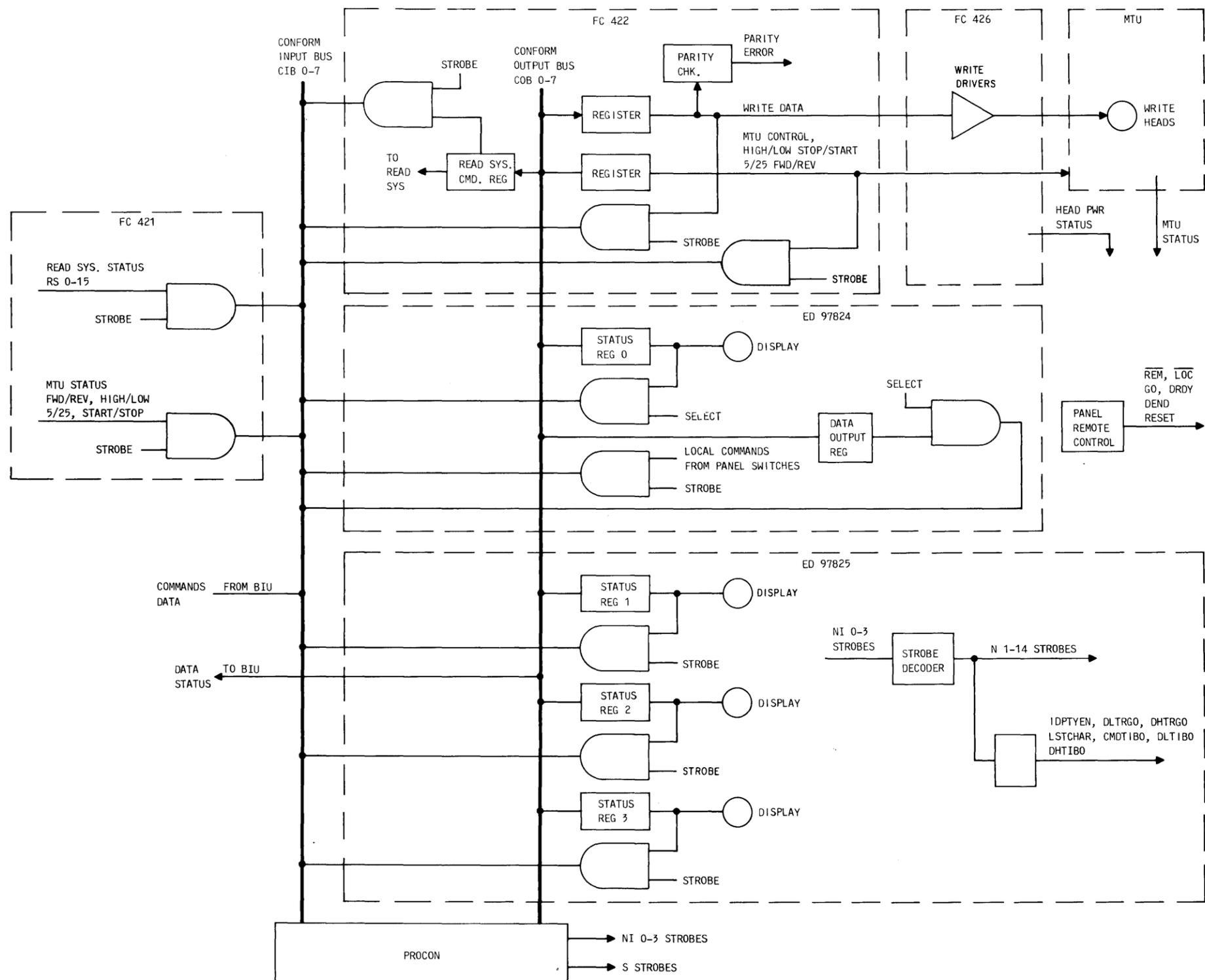


Fig. 12—Controller-Formatter Block Diagram

4.47 The REVERSE TO TAPE MARK command is almost identical to the forward command. A different subroutine is used to check status and start the tape moving in the reverse direction.

4.48 The MAINTENANCE command is used to check the operational status of PROMATS, exercise the error detection circuits, and locate faults. The complete maintenance routine consists of 11 steps. Each step is initiated by the receipt of a maintenance command. The maintenance step complete bit in status register 0 is set at the end of each step, and the command complete bit is set after the last step. These steps are described in Part 6.

D. Read System

4.49 The PROMATS read system recovers data recorded on standard 1/2-inch-wide computer tape in a 9-track, 1600-bit-per-inch, phase-encoded format. The read system amplifies the analog signals read from tape and processes them into a digital form. The read system also identifies special control characters written on tape, separates data from preambles and postambles, and provides data output, system status, and word count to CONFORM. It also has error detection and recovery capability.

4.50 The read system is controlled by a 16-bit programmable controller (read PROCON). The PROCON is a general-purpose microprocessor which contains a fixed operating program in a read-only memory (ROM). The read PROCON accepts the input commands from CONFORM and, by means of the programs in the ROM, executes a series of program steps to process data read from tape. Table G includes the read system command register word format and Table H shows the read PROCON test lead assignments. Table I lists the word formats for the read system output register. A block diagram of the read system is shown in Fig. 13, and the time relationships of significant signals in the read system are shown in Fig. 14.

4.51 The signals read from tape must be amplified to a level that will provide reliable peak detection in order to convert the signal to a digital format. Each of the nine tracks on the tape has a corresponding read channel. Circuit pack FC 429 contains three identical amplifier channels, each of which receives its input signals from one of the read heads. PROMATS contains three FC 429

TABLE G

COMMAND REGISTERS

BIT	TAPE TRANSPORT
	DEFINITION
0	Stop
1	Forward/Reverse
2	Low Speed/High Speed
3	5 IPS/25 IPS
BIT	READ SYSTEM
	DEFINITION
0	Read Enable
1	Read/Write
2	Forward/Reverse
3	Maintenance
4	Word Count
5	Data Match
6	Read Interface Check

circuit packs on which the 9 read channels are located.

4.52 A read head signal is amplified in the first stage of the amplifier and then differentiated to provide a signal with zero crossings that correspond to the peaks of the head signal waveforms. The signals then are applied to a zero crossing detector whose output is a digital waveform (labeled DAT) with transitions that correspond to the occurrence and polarity of the peaks in the read head signal (Fig. 15). The direction of the transitions corresponding to data indicates whether the bit position contains a 1 or a 0.

4.53 The gain of the amplifier is set at approximately 690 in the read-only mode. This permits operation with head signals that range from 1 millivolt to 22 millivolts in peak-to-peak amplitude. The nominal head signal is 10 millivolts peak-to-peak. In the read-after-write mode, the amplifier gain is reduced to half the read only gain to ensure that the recorded signal amplitude will be well within

TABLE H
READ SYSTEM CONTROL COMMANDS

TEST LEAD ASSIGNMENT	FUNCTION
T2	Read Enable (RE)—RE high indicates that read system is enabled and should expect data.
T3	Read-After-Write—High indicates read-after-write mode. Low indicates read-only mode. Used for gain switching and error report determination.
T4	Maintenance—Provides an indication of maintenance mode (when high).
T5	Word Count Request— When high, indicates request for read system word count to be transferred to CONFORM.
T6	Data Match Request—When high, indicates data match activity to be performed by read system.
T7	Read Interface Check—Request to perform transfer of all zeros followed by all ones data between read system and CONFORM.

the tolerance required for reliable signal detection during subsequent reading.

4.54 Each DAT signal is inputted to a dedicated channel of digital processing circuits on an FC 431 circuit pack. Transitions in the DAT signal are converted to pulses and synchronized with the decoding clock (RCLK) signal. Negative transitions of DAT are converted to pulses in IC42 on an FC 431 circuit pack and positive transitions are converted in IC41. At the beginning of each block of data, a minimum of eight negative transitions is required in less than 200 microseconds (the period of 8 bit cells). This verifies that there is at least one transition in each bit cell insuring that the signal passes a preliminary check prior to being processed as a valid data signal. The interval is established by a monostable multivibrator which enables a counter. After the counter counts eight transitions during the period, the output gating is enabled. If this condition is not satisfied, the track in error (TIEN) signal is prevented from going high, thereby indicating an error on the track.

4.55 The DAT signal contains transitions which correspond to phase character transitions as

well as data character transitions. A gating window referenced to the previous data transition is used to inhibit the phase transition and pass the next data transition to the data flip-flop. Window timing is provided by two presettable counters that count cycles of RCLK. The sequence begins with the first negative transition of the preamble (a zero). A data pulse loads the first counter which is then clocked by RCLK. After 12 RCLK pulses, the counter counts to carry and enables the window. At this time, the phase character transition has passed. The window remains enabled until the occurrence of the RCLK pulse after the arrival of the next data transition. The second counter is loaded by the carry from the first and begins to count. If it counts to carry, the bit cell has passed without a data transition. This means that a data bit has been lost (or the end of the data block has been reached). This causes the channel to be disabled for the remainder of the block. The TIEN signal goes low to signal an error. During normal decoding, pulses corresponding to the transitions in the DAT signal set or clear the DATAN flip-flop. DATAN is then available on the output as a high for a data zero and low for a data one, and is valid on the positive going edge of the DCLK signal.

TABLE I

READ SYSTEM OUTPUT REGISTER WORD FORMATS

BIT	DATA	WORD COUNT	STATUS	MAINTENANCE RESULTS
0	0	2^0	Reading Information	0
1	1	2^1	ID Read	0
2	2	2^2	TM Read	0
3	3	2^3	Recoverable Error	Group A
4	4	2^4	Unrecoverable Error	Group B
5	5	2^5	Skew Error	Group C
6	6	2^6	Beginning Preamble	Group D
7	7	2^7	—	FC 430
8	Parity	2^8	—	FC 432A
9	Last Data Flag	2^9	—	FC 432B
10	—	2^{10}	—	FC 433
11	—	2^{11}	—	Read System PROCON
12 (Note)	0	0	0	1
13 (Note)	0	1	0	1
14 (Note)	0	0	1	1
15	Ready	Ready	Ready	Ready

Note: Bits 12, 13, and 14 define the contents of the register.

4.56 Part of the digital processing circuit is a variable frequency clock derived from the data read from tape. To insure correct reading of tapes recorded on other tape transports whose speeds may vary considerably, variations in average bit cell spacing of as much as ± 25 percent must be tolerated. The variable frequency clock concept, in conjunction with the counter windowing previously described, is used to ensure accurate data decoding.

4.57 Signal channels 2 and 5 are used as references to determine the data rate of the tape transport. The decoding clock (RCLK) is derived from two phase-locked loops (PLL) consisting of a phase detector, a voltage-controlled oscillator, and a low-pass filter and frequency divider. When no data is input to the loops, they are driven by a fixed frequency clock at a frequency that is close (within 4 percent) to the nominal data frequency. As soon as signals from tape are available for

processing, the loops begin tracking data transition pulses from their respective channels.

4.58 The PLLs provide an output signal that is phase-locked to the input and is 17 times the input frequency. This is established by the divide-by-17 counter in the feedback path of each PLL.

4.59 Each of the two tape reference channels supplies the input to its dedicated PLL; however, the channel that first begins processing valid data, thus raising its TIEN signal, is selected as the master reference for decoding the data block. If the selected master channel loses its signal, the other PLL is selected as the master until the end of the data block. If both reference tracks are in error, the fixed frequency clock is used for the remainder of the block.

4.60 The self-clocking feature on each of the nine data channels permits electronic compensation of any mechanical misalignment (skew) between the read and write heads, as well as uneven tape motion (snaking) which produces dynamic skew. Any skew that is present will be evidenced by time (phase) differences among the 9 bits of a character read from tape.

4.61 Skew compensation is accomplished in the elastic stores (one for each tape track) located on the FC 432 circuit packs. The elastic stores are operated similarly to 8-bit shift registers in which data bits can be independently loaded or read out. This deskewing technique functions by effectively inserting delay into the leading channels as each elastic store detects the first one (at the end of a preamble) loaded into it. When data begins to be clocked into the store, each new bit is stored in the next sequential location designated by a write pointer within the store which is incremented with each clocking.

4.62 PROCON waits six character periods waiting for the all ones character (at the end of the preamble) to accumulate in the elastic stores. Contents of the stores are examined by gating the DATA OUT signal onto the input bus. The location whose contents appear on the DATA OUT lead is designated by a read pointer within each store. As long as the zeros of the preamble are being clocked into a store, the read and write pointers point to the same location so that the DATA OUT information is the most recent bit loaded into each store. When the first one bit enters the store, the read pointer is halted at that location while the write pointer continues to advance, storing the following data bits at sequential locations. When PROCON detects the initial one in every store, then all nine read pointers are simultaneously advanced by a read strobe from PROCON. This relationship among the read pointers is maintained until the end of the data block. Once a full character has accumulated, all stores are read simultaneously.

4.63 All data needed by the PROCON must be buffered and gated onto the input bus at the proper time, and all outputs to the CONFORM must be loaded into the interface register. Under program control PROCON generates control lead signals which can be combined to select a set of gates to place data on the input bus or to select a register destination to receive data placed on

the output bus. The following types of strobes are generated to control gating to and from the read system:

- (a) **Source Select—S0, S1, and S2:** These strobes are used to gate data onto the input bus.
- (b) **Destination Select—D0, D1, D2, and D3:** These are used to strobe data from the output bus to a destination.
- (c) **Device Select—N0, N1, N2, and N3:** These are used to expand the number of destinations that can be addressed. These leads are used directly in the read system without any further decoding.

4.64 A source strobe may be generated by combining an S-lead and an N-lead to form a gate enable during which PROCON can read information present on the inputs to the gate. A destination strobe may be generated by combining a D-lead and an N-lead to gate information on the PROCON output bus to a destination. The gating arrays selected by a combination of strobes are found on the circuit cards where they are used. Table I lists the contents of the read system output register. The register may contain any one of four types of information. The meaning of the information is specified by output register bits RS12, RS13, and RS14. All data and read system communications to CONFORM are transmitted through the read output register.

E. Magnetic Tape Transport

4.65 Theory coverage of the tape transport is not provided in this section. The documents listed in Part 6 provide adequate information for trouble-shooting and repair. The tape transport status word formats are given in Table J. The tape transport and associated power supply are shown in Fig. 16.

5. POWER SUPPLY CIRCUITS

5.01 The tape transport power supply (Fig. 17) is a dc-to-dc converter composed of two converter circuits operating from a -48 volt dc input source. The first converter supplies highly regulated +5 volts and ± 15 volts for electronic loads and ± 15 volts (less regulated) for pulse loads.

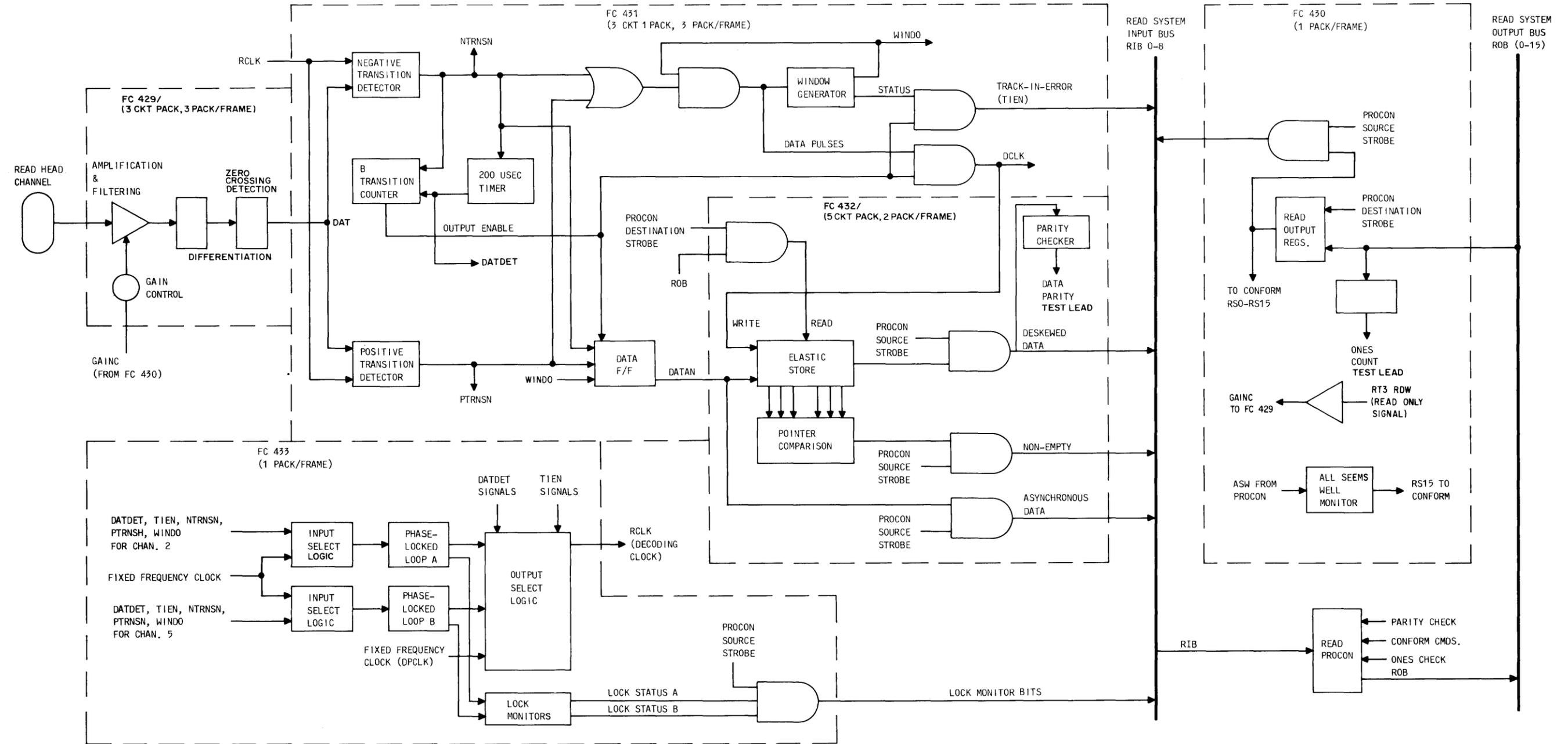


Fig. 13—Read System Block Diagram

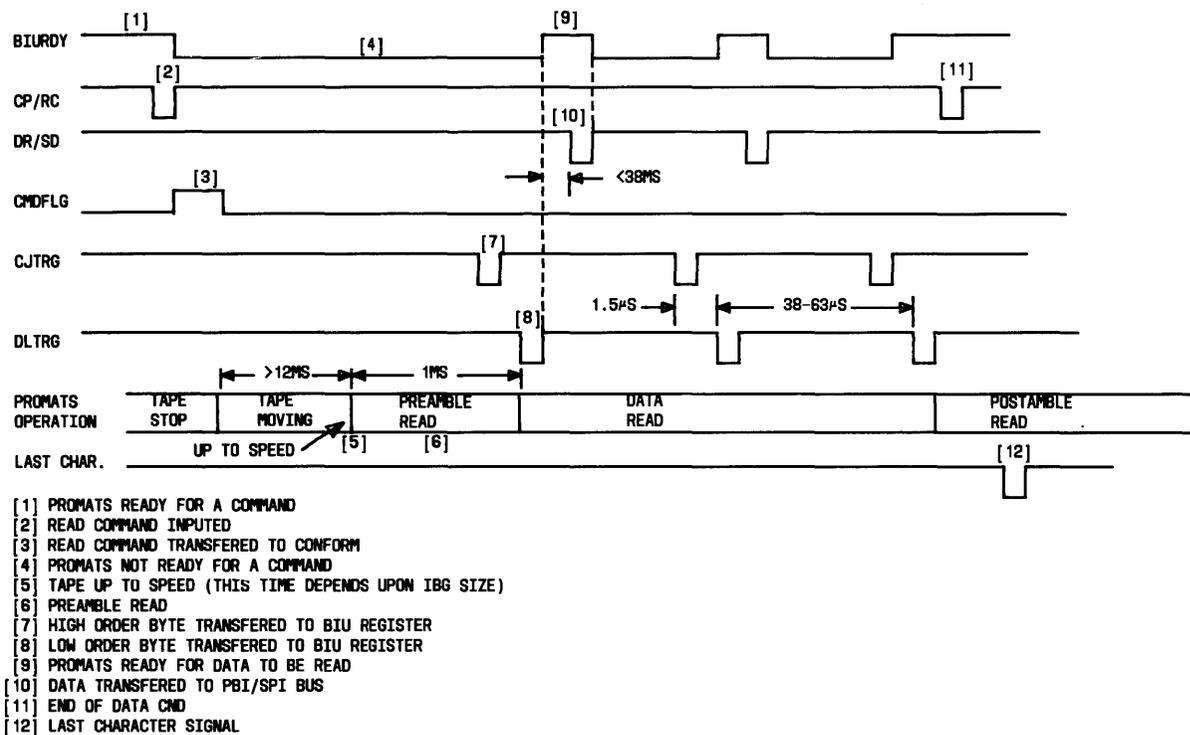


Fig. 14—Read Sequence Timing Diagram

The second converter supplies -24.5 volts for a pulse load.

5.02 The first converter consists of a driven inverter, a power transformer, rectifier and filters, an oscillator which determines the operating frequency of the driven inverter, an error detector to determine output voltage errors, and a pulse-width modulator to accomplish the voltage regulation.

5.03 The second converter has a power transformer, T2, with a center-tapped primary. The two halves of the primary winding together with a choke and a common capacitor form two L-C resonant networks. Diode switches in series with each network alternately turn on each half of the primary.

5.04 The outputs of both converters are checked by overvoltage monitors. Should the voltages exceed predetermined limits, power will be removed from the converters. A visual indicator, CR104, provides an indication of overvoltage shutdown.

5.05 A 132AB power unit provides +5 volt direct current for the PROMATS logic circuits.

The power unit is a dc-to-dc converter similar in operation to the first converter section of the tape transport power supply. The unit receives -48 volt direct current from the frame input fuse block. A transistorized inverter provides square wave alternating current to the power transformer. The pulse width of the square wave is varied to accomplish the regulation of the output voltage.

5.06 The load for the power unit is protected from excessive voltage by a protective circuit which causes the unit to shut down when the output exceeds a predetermined level. A visual alarm is provided (a light emitting diode) which illuminates if the output voltage increases beyond its limits. A relay closure provides an undervoltage indication to the external system.

6. MAINTENANCE TESTING

6.01 The maintenance command is used to check that PROMATS is operational, exercise error detection capabilities, and locate suspected faults. It primarily checks CONFORM and the read system, but a partial check of the BIU is also performed. The entire routine consists of 11 steps, each of

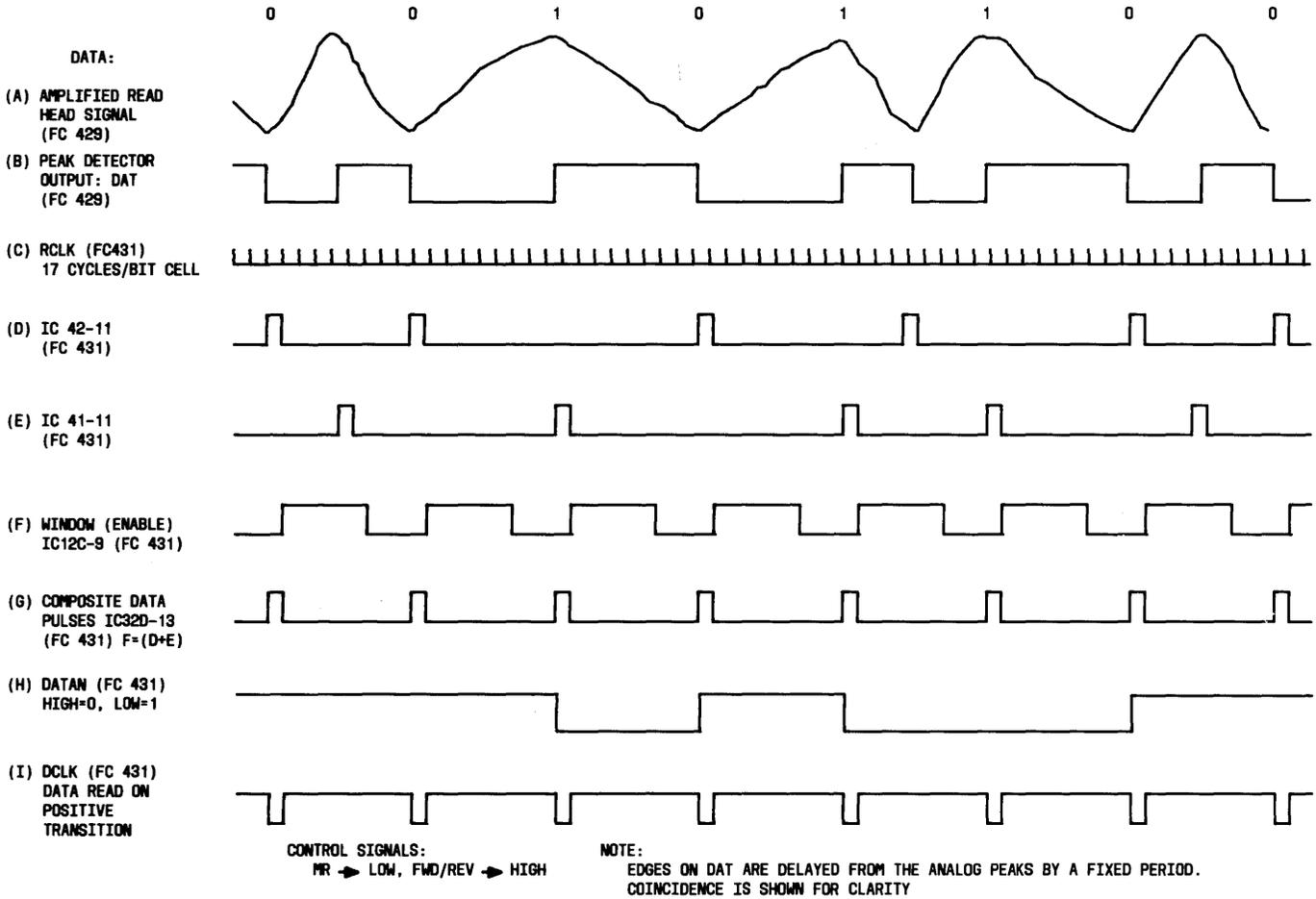


Fig. 15—Read System Waveforms

TABLE J
TAPE TRANSPORT STATUS WORD FORMATS

WORD 1		WORD 2	
BIT	DEFINITION	BIT	DEFINITION
0	—	0	
1	—	1	
2	—	2	
3	—	3	Reverse
4	—	4	Stop
5	—	5	Forward
6	Ready	6	Rewinding
7	Temp		
8	BOT		
9	EOT		
10	Write Enable		
11	Remote		
12	Write Head Power		
13	Erase Head Power		
14	MTU Failure 1		
15	MTU Failure 2		

which is started by receipt of the maintenance command. (Refer to Table K). The first three steps are static tests which do not include tape motion. The remaining steps are dynamic tests in which the tape is moving. The maintenance step complete (MNTC) bit in status register is set after each step is executed. The command complete (CMDC) bit is set after the last step. If any faults are detected, the corresponding bit is set in status register 3. The BIU status bits are listed in Table L.

6.02 When the first maintenance command is successfully decoded, the first step is executed. The status registers and data display register are loaded with all ones. This checks the ability of the registers to be set and of the display panel to show the contents of the registers.

6.03 The second time the miscellaneous command is given, all the status registers are cleared. The only bit set at the end of this step is MNTC.

6.04 Step 3 checks as much of PROMATS circuitry as possible, providing gating array checks, register loading, initialization, parity checks, and other circuit functions that do not require tape motion. Most of the static tests done by the Controller/Formatter make use of the wraparound feature; ie, registers which hold status send commands can be written and read back into PROCON to check that they were correctly written.

6.05 A test on the ASW error-catching ability of the CONFORM is also made. An instruction containing bad parity is in the program. When this instruction is executed, the ASW flip-flop on FC 422 is tested to see if the error was caught. If it was not caught, or if there was an ASW error present before the bad parity test, a PROCON error is flagged and the static tests terminated. The assumption is made that if the PROCON is not functioning correctly, the other status indications may not be valid.

6.06 The I/O register and the parity checker on FC 427 are also checked by writing and reading back the "all ones" and "all zeroes" words. When PROMATS is in the local mode, commands and data are inputted from the local panel; therefore, the strobes which gate information into the PROCON from the I/O register have to be inhibited. This causes FC 427 to fail its test when PROMATS is in *local*. As a result, the LED indicating an FC 427 failure will normally be turned on in this step.

6.07 Static diagnostic testing is performed by the read system when the maintenance mode request lead is set by CONFORM and no other read system request is waiting. Static maintenance procedures include checks on the gating paths onto the input bus, register loading and initialize checks, parity checks, and other circuit functions that do not involve tape motion.

6.08 Correct operation of the number-of-ones circuit is checked at the beginning of static maintenance testing. PROCON sends various 9-bit patterns to the number-of-ones circuit on the FC 430 circuit pack. The possible outputs of the circuit are indications on PROCON test leads that the 9-bit input group contains none, one, or more

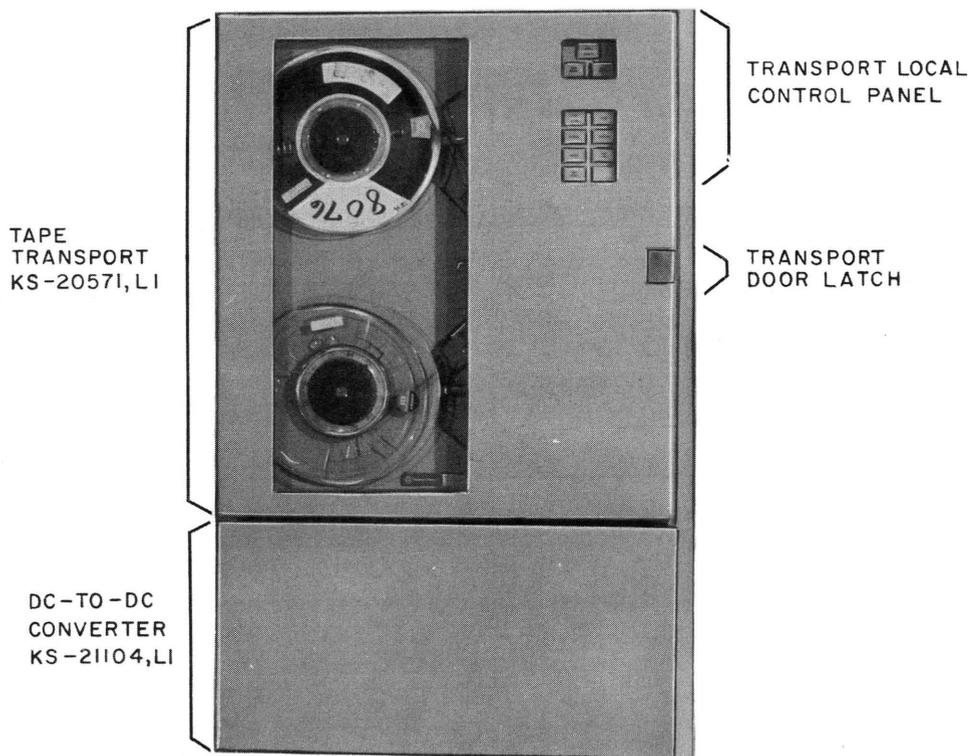


Fig. 16—Tape Transport and Power Supply

than one bit at a logic 1 level. An error results in an FC 430 failure report.

6.09 The read PROCON all-seems-well (ASW) circuit is tested in static maintenance. An instruction containing bad parity is contained in the read PROCON program. When this instruction is read, an ASW failure indication should result. If it does not, a read PROCON (RPC) error bit is set in the diagnostic summary word.

6.10 The next test is a check of the ability of the read PROCON-generated strobes to load predetermined bit patterns into the output register on FC 430. Correct input bus, output bus, and register functioning is verified by examination of the register contents by PROCON. Any pattern discrepancy causes the FC 430 error bit to be set in the diagnostic summary word.

6.11 The parity check circuitry on the FC 432 circuit pack is checked by inputting predetermined bit patterns of both good and bad parity and examining the parity check output. A parity check failure sets the FC 432A bit in the

diagnostic summary word. Both FC 432 circuit packs contain identical parity check circuits, but only the circuit pack designated FC 432A has its parity check circuits connected in the backplane wiring.

6.12 The elastic stores on FC 432 are verified by clearing the stores with a PROCON-generated initializing strobe. This sets the read and write pointers to the same store address (0) and should result in an address match or empty indication. The read pointers are then incremented, and a pointer mismatch or nonempty indication should result. When an error results, the bit in the diagnostic summary word that corresponds to the appropriate FC 432 circuit pack is set.

6.13 The two phase-locked loop circuits on FC 433 are verified by determining that they are locked onto the fixed frequency clock. The lock monitors are cleared, and the circuit then waits a fixed length of time to permit any out-of-lock condition to be detected by the lock monitors. If lock is not detected, the FC 433 error bit in the summary word is set.

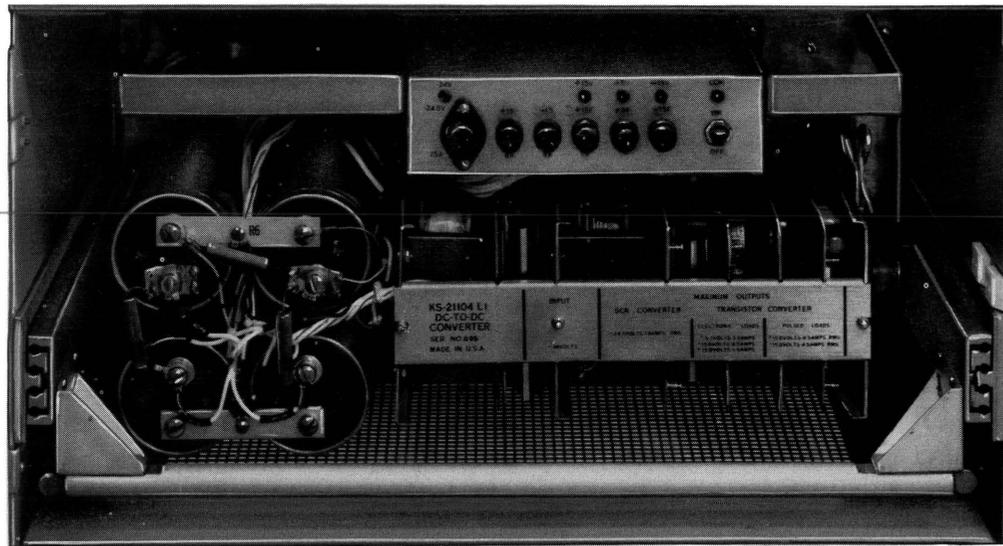


Fig. 17—Power Supply

6.14 At the end of the static maintenance steps, CONFORM requests the results of the read system static checks by generating strobes that gate the results to CONFORM.

6.15 Dynamic testing involves tape motion. Table K lists the steps and a discussion of each step follows.

(a) In step 4 the ID burst is written providing the BOT marker is at the sensor. If not, the command complete bit is set and the maintenance routine is ended. The regular routine for writing an ID burst is used and the status reported is the same as that for a write ID command except that the maintenance step complete bit will be set instead of the command complete bit.

(b) In step 5 a tape mark is written. If this is not the first time the maintenance routine has been executed and a reset or initialize has not been given, a skip will be done before the tape mark is written. This is done to move

past a possible bad spot on the tape which may cause failures in the remaining tests. At the end of this step the status which normally follows a tape mark command, along with the maintenance step complete bit, will be reported.

(c) In step 6 the first test block of data is written. This is a block of 512 even parity bytes of data. In addition, an error in the data count is forced. The data pattern, 010011100, is stored in the program. The parity checkers on the controller output data register, the write driver circuit, and the Bus Interface Unit I/O register are tested when the last character is written and flags set if they indicate even parity. After the postamble is written the routine which does the speed check and data count check is entered. Prior to this, the data count register was set up with a count one higher than the number of characters on tape. Therefore, when the error flags are checked and the read system status obtained, the final status should indicate a data count error, the three parity errors, and an unrecoverable error.

TABLE K
MAINTENANCE STEPS

STEP	ACTION
1	Load status register with all ones
2	Load status register with all zeros
3	Static board tests—local CP7 error
4	Write ID
5	Write TM
6	Test block No. 1—parity error bits set Data count error Unrecoverable error—due to bad parity
7	Test block No. 2 Recoverable error—sequences through nine tracks and nine blocks with simulated dropout
8	Test block No. 3 Data count error Skew error
9	Test block No. 4 Data match—known pattern written
10	Read reverse Data match
11	Read system board report <ul style="list-style-type: none"> • Rewind erase • Maintenance step complete at the end of each step • Command complete at the end of the maintenance command

(d) In step 7 nine data blocks of 512 characters each are written. Each block has a dropout simulated in a different track. These single track errors should be flagged as recoverable errors by the read system. The data pattern is 010010111. The dropout is simulated by not writing a data transition in one of the tracks when the last data character is written. All of the subroutines used in the record operation are used here. The tape is stopped after each block

is written but is immediately restarted. Status is obtained from the read system after each block to see that a recoverable error was indicated. If not, the unrecoverable error bit is set. Had the read system reported an unrecoverable error for any of the blocks, that fact would be saved and outputted in the status at the end of this maintenance step.

(e) In step 8 the third test block is written.

This 1024-character block has a forced data count error and a "skew error." The skew error is generated by writing the preamble, data, and postamble so that track nine is offset by four characters. The information on this track will be detected by the read head after four characters have been seen on the other tracks and will continue four characters beyond the other tracks. Since special characters were required for this, the normal preamble and postamble routines could not be used. After the block is written, the usual routines for stopping the tape and gathering status are executed. The data count and skew error bits should be set at the end of this step.

(f) In step 9 a block without any forced errors is written. The purpose of this block is to write a data pattern known to the read system so that it can do a character-by-character match with what it reads off tape. The block consists of 128 characters of pattern 10111000, followed by 128 characters of 011001011, followed by 128 characters of 10111000 pattern. When the command register to the read system is written to tell it to look for data, the data match bit is also set. For the normal condition there should be no error bit set.

(g) In step 10 a data match is done by reading in reverse the block written in step 9. No data is passed out of the system during this step. Since a symmetric pattern was written, the read system only needs to be told that the tape is moving in reverse and to do the data match. The same status as in step 9 is expected from the read system. After the block has been read, the read system is asked for any additional status on possible board failures. These would be the group errors which are added to the information in status register 3 at this time. Each of the groups identifies a signal processing path consisting of an FC 429, FC 431, and FC 432 circuit pack.

TABLE L
BIU STATUS BITS

STATUS BIT	DEFINITION
BIU Ready (BIURDY)	This status bit is generated by the BIU and, when set, indicates the BIU is ready to accept or output information. The bit is reset when a command is input, a data word is input, or a data word is output. The BIURDY bit is set when the CONFORM command or maintenance step is complete; when the low order data word is transferred from the BIU to the CONFORM; or when the low order data word is transferred from the CONFORM to the BIU.
Bus Error (BUSER)	This status bit is generated by the BIU and, when set, indicates the BIU has detected a parity error associated with the last command or data word. Once set, an initialize command is required to reset it.
Short/Long Record Error (SLRE)	This status is generated by the BIU and, when set, indicates the BIU has detected an improper sequence of PBI signals during a read operation. The Short Record Error results when, during a read operation, a shorter block of data exists on tape than is requested by the PBI bus. The Long Record Error results when, during a read operation, a longer block of data exists on tape than is requested by the PBI bus. This bit is reset by an initialize signal.
Read Data Missing (RDM)	This status bit is generated by the BIU and, when set, indicates the CONFORM has transferred a data word to the BIU I/O register before the previous word was transferred to the PBI bus causing an over-write. This bit is reset by an initialize signal.

(h) The final maintenance step 11 is used to erase what was earlier written on the tape. The erase and write head power are turned on and the rewind command is executed. After the tape is stopped at the BOT marker, head power is turned off and the command complete bit is set.

6.16 As each step is performed, read system error reports are collected to form an error summary. When all steps are completed, the error pattern (if any errors are detected) is analyzed to determine which of four circuit pack groups contains the error. Each of the groups is a signal processing path using parts of three circuit packs: FC 429, FC 431, and FC 432. When the group is identified, the group A, group B, group C, or group D (GRA, GRB, GRC, GRD) error bit is set in the diagnostic summary word. The completion of each maintenance

step sets the MAINTENANCE STEP COMPLETE flag, and the COMMAND COMPLETE signal is set. The CONFORM combines results of static and dynamic maintenance and makes the report available for output and display in status register 3.

6.17 In most types of potential system malfunctions, the maintenance routine described can be used for a meaningful indication of the problem. Some PROMATS failures may occur which prevent the system from executing the normal maintenance command. PROMATS frame maintenance procedures will involve the use of two special PROCON test programs. The programs are available in two separate program storage unit (PSU) circuit packs; one each for CONFORM and the read system. The test PSU boards are inserted in the PROCON card cage in place of the normal operating program

(memory) card. The test programs are used in conjunction with a program address display board which plugs into the PROCON unit. (See Fig. 18).

6.18 The special test routines exercise the PROCON operations used in normal PROMATS functions and verify that the PROCON unit functions properly. In addition, each test program verifies logic operation of other circuit packs, where possible, by executing static tests identical to those described in paragraph 5.01. The test programs are structured so that when a fault is found, the PROCON will execute an instruction that loops on itself. The program address for the instruction can be read from the address display board and the corresponding recommended pack replacement can be obtained from the program listing comments. Normal operation of the test program causes the PROCON to continually loop through the program. This normal situation would be evident on the address display circuit pack. Either CONFORM or read system can be tested in this manner without the

interaction between the two required in the normal maintenance command sequence.

7. REFERENCES

7.01 The following Bell System Practices contain information applicable to the PROMATS.

- Section 034-369-301—Recorder, KS20571 L1, Trouble Locating Procedures, Issue 1, March 1975
- Section 034-369-701—Recorder, KS-20571, Requirements and Adjustment Procedures, Issue 1, December 1975
- Section 034-369-801—Recorder, KS-20571, Piece Part Data and Replacement Procedures, Issue 1, February 1974
- Section 254-300-130—Input/Output Interfaces, Description and Theory of Operation, Common Systems

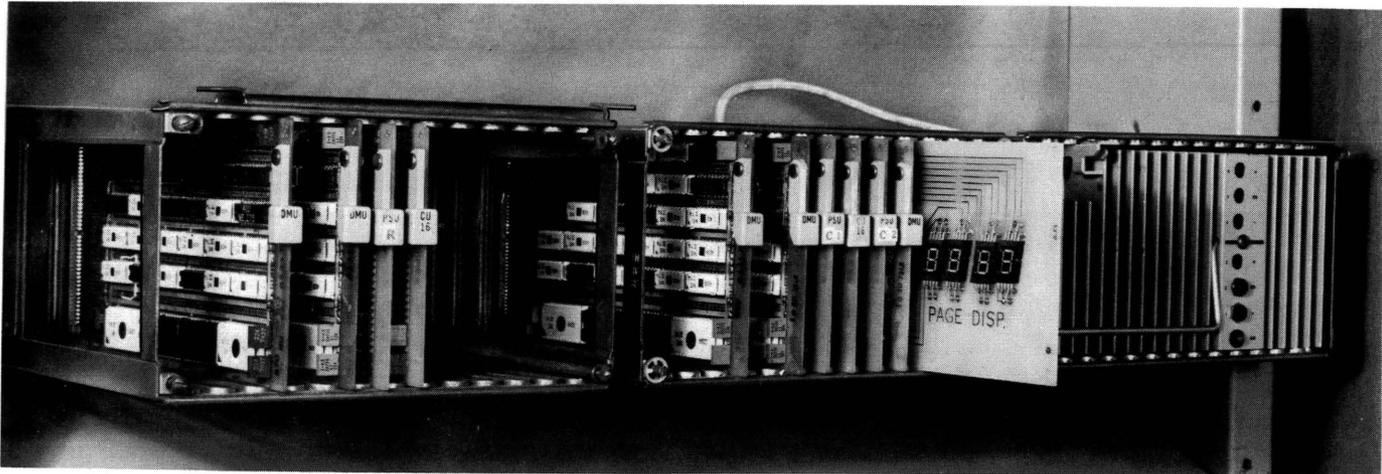


Fig. 18—PROCON Unit with Address Display Board