Task Oriented Practice
(TOP)

TROUBLE CLEARING

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254-302-812	TPG
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−48V Fuse (Processor Control Frame); Blown − Clear	TAP-101
300-MB Moving Head Disk Demand Diagnostic Failure − Clear Using Trouble Locating Program	TAP-126
300-MB Moving Head Disk Diagnostic Failures − Clear Using Trouble Locating Program	TAP-107
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Blown −48V Fuse − Clear	TAP-101
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CAP CHG Circuit Failure − Clear	TAP-102
Channel Demand Diagnostic Failure − Clear Using Trouble Locating Program	TAP-123
Control Unit (CU) Diagnostic Failure − Localize Using Demand Exercise (DEX) Option	TAP-128
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FIND YOUR JOB IN THE LIST BELOW	THEN GO TO
Diagnostic Failure; Peripheral Controller — Clear Using Trouble Locating Program	TAP-105
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Disk File Controller Demand Diagnostic Failure — Clear Using Trouble Locating Program	TAP-125
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Input/Output Processor Demand Diagnostic Failure — Clear Using Trouble Locating Program	TAP-127
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Unit — Remove From Service Via Command Code	DLP-510
Unit — Restore To Service Via Command Code	DLP-511
Unit Power Fault — Clear	TAP-108

Faults that occur within the computer are software/ hardware detected in response to automatic, manual, or routine operation failures. These faults result in terminal (cathode ray tube, TTY, and/or printer) displayed messages as well as visual and/or audible indications depending upon the application. The task index list (IXL-001) should be utilized to access fault clearing procedures. The IXL-001 is organized to direct the user to the trouble analysis procedure (TAP) necessary to correct the fault according to the given stimulus (terminal display, indicators, etc). At an appropriate point in the fault-clearing process (isolation of fault), a diagnostic test may be performed to obtain definite fault identification data. This data is available from the software routine called the trouble locating procedure (TLP) which lists the causes of the fault in order of probability (ie, the most likely cause first, the least likely cause last). Fault identification data may also be obtained from the table within each diagnostic trouble clearing TAP.

Circuit packs are replaced one at a time in the order listed in the TLP and/or table provided in the appropriate TAP unless otherwise indicated using proper power-up/ power-down procedures. The diagnostic is repeated after each circuit pack replacement. If the TLP indicates the same fault, the last circuit pack removed should be reinstalled and the next listed circuit pack is replaced. If the TLP indicates a different fault, the circuit pack replacement procedure is repeated starting with the first listed pack of the new TLP and/or table. Faults not cleared by circuit pack or fuse replacement should be cleared by referring to appropriate trouble analysis data (TAD), office documents, or finally by referring to the proper service support organization per local procedures.

CAUTION 1: Circuit pack should be handled by the edges or face plates to avoid scratching the gold-plated contacts or deforming components or leads.

(a) Office location

(b) Frame and mounting location

(c) Diagnostic fault (unit and phase)

(d) Date removed

Stored in the office are the following documents which will be useful in the maintenance of the computer:

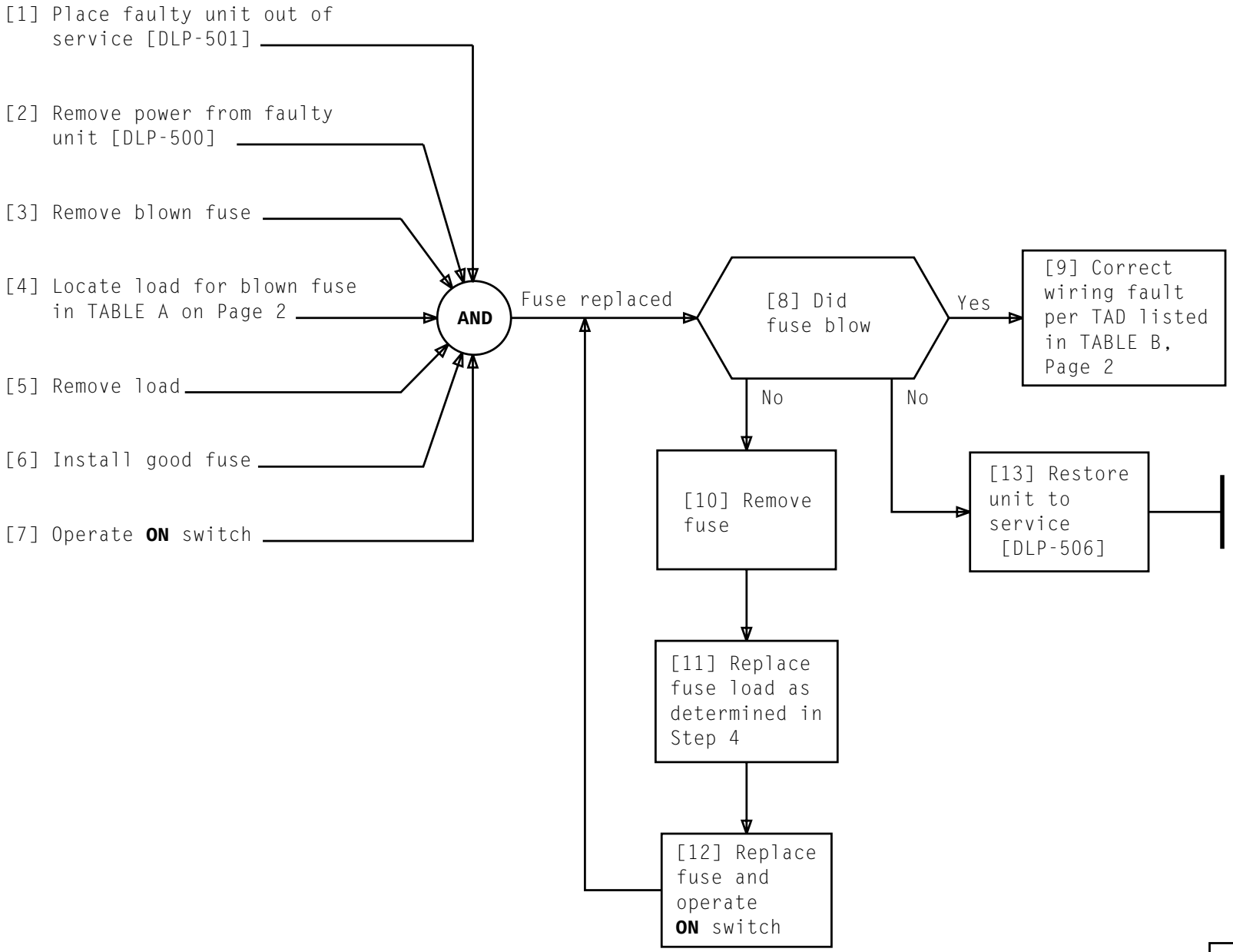
- Input/Output Manuals
- Schematic Drawings
- Program Applications
- Program Listings
- AT&T Practices
- Software Subsystem Descriptions
- Peripheral Equipment Manuals

Craft people should be familiar with the following:

- System equipment abbreviations
- Equipment locations
- Use of Task Oriented Practices
- Switching video terminal and printer between input/output processor via portswitch selector
- Use of test equipment
- Troubleshooting and signal tracing techniques

MAINTENANCE PHILOSOPHY

- Knowledge of replaceable circuit packs in moving head disk drive and tape transport
- Terminal usage
- Power-up/power-down procedures
- System/frame power, fuse assignments, etc
- Classification of faults requiring use of remote host diagnostics
- Understanding of input/output messages
- Perform complete diagnostics and phase diagnostics
- System configuration and interconnections
- Retiring system alarms
- Notifying special craft people of moving head disk drive and tape transport equipment failures.

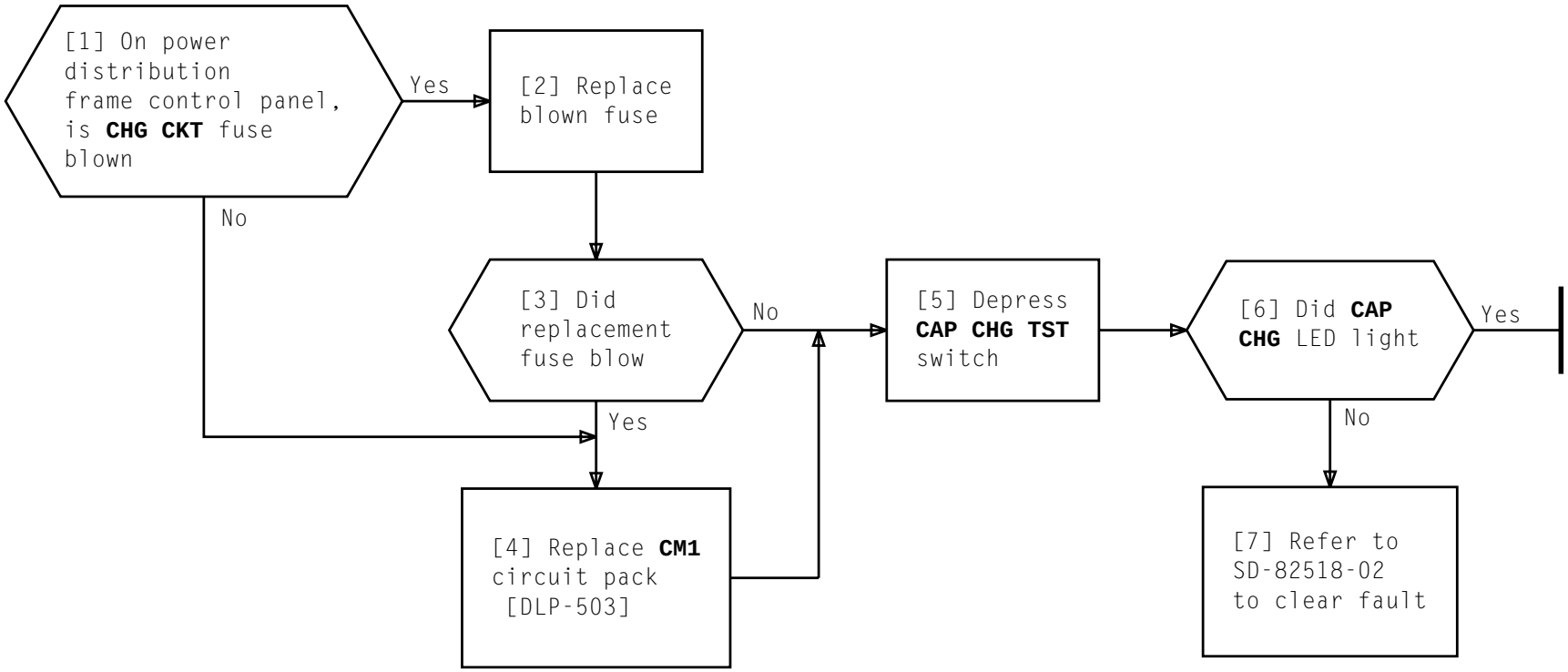


CLEAR BLOWN FUSE — PROCESSOR CONTROL AND POWER DISTRIBUTION FRAMES

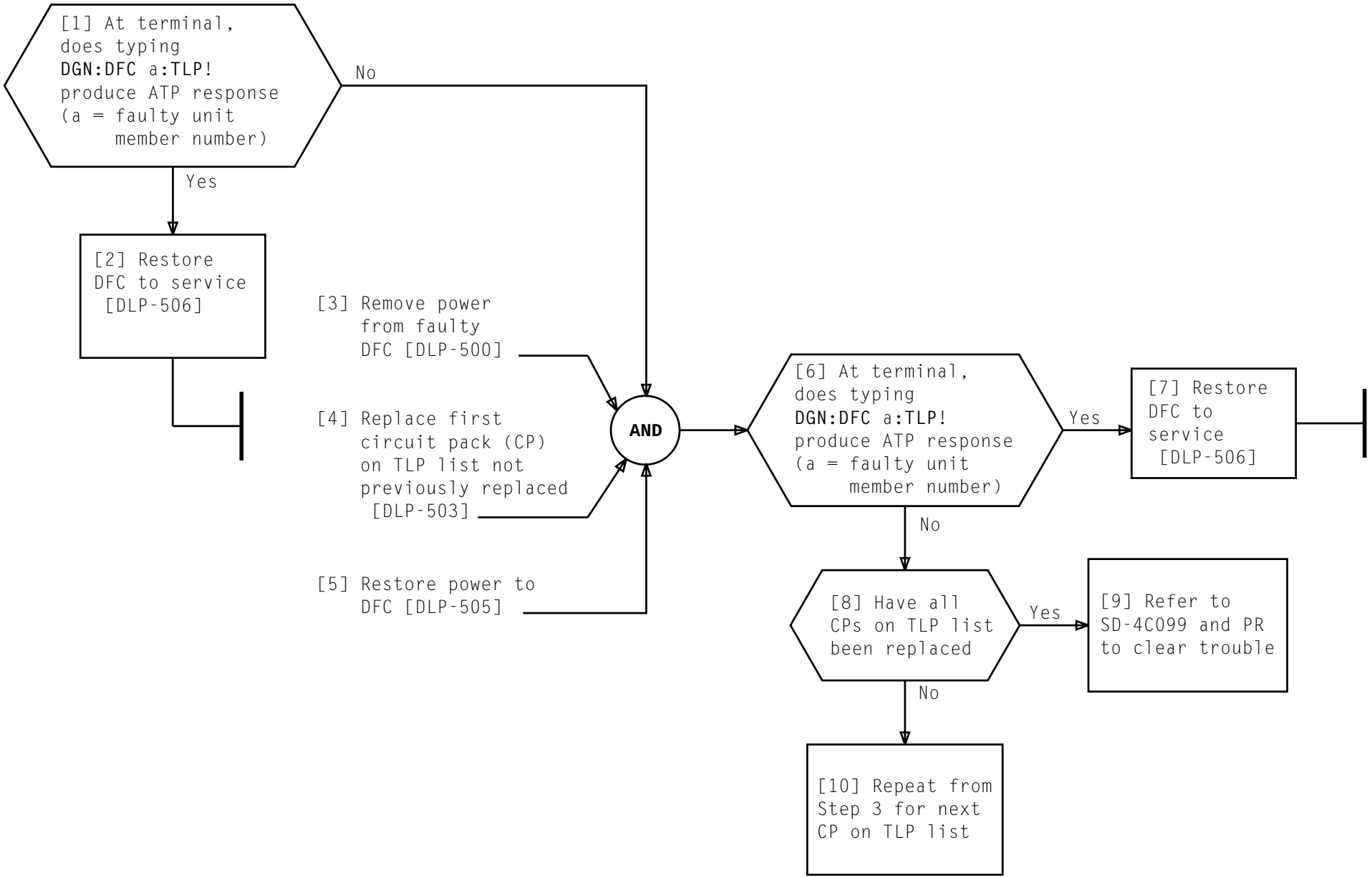
TABLE A									
FUSE	AMP	TYPE	LOAD	LOAD LOCATION	FUSE	AMP	TYPE	LOAD	LOAD LOCATION
F1A	2A	**70B**	Fan 4	20/29-*	**F16**	10A	**74D**	Power unit F	38-178
F2A	2A	**70B**	Fan 3	20/29-*	**F16A**	.25A	**70F**	Power unit F	38-178
F3A	2A	**70B**	Fan 2	20/29-*	**F17**	3A	**74B**	PC 1 TN9	29/38-032*
F4A	2A	**70B**	Fan 1	20/29-*	**F17A**	.25A	**70F**	PC 1 TN9	29/38-032*
F5A	3A	**70C**	DFC TN3	47-074	**F18**	3A	**74B**	PC 2 TN9	38-052
F6	10A	**74D**	Power unit C	47-016	**F18A**	.25A	**70F**	PC 2 TN9	38-052
F6A	.25A	**70F**	Power unit C	47-016	**F19**	3A	**74B**	PC 3 TN9	38-022
F9	10A	**74D**	Power unit D	47-178	**F19A**	.25A	**70F**	PC 3 TN9	38-022
F9A	.25A	**70F**	Power unit D	47-178	**F20**	10A	**74D**	Power unit E	38-016
F10A	3A	**70C**	CPU TN5	56-162	**F20A**	.25A	**70F**	Power unit E	38-016
F11	10A	**74D**	Power unit B	56-178	**F21**	3A	**74B**	PC 0 TN9	29/38-072*
F11A	.25A	**70F**	Power unit B	56-178	**F21A**	.25A	**70F**	PC 0 TN9	29/38-072*
F12	10A	**74D**	Power unit A	56-016	**F22A**	3A	**74B**	IOP TN6	29/38-162*
F12A	.25A	**70F**	Power unit A	56-016	**F23**	10A	**74D**	Power unit H	29/38-178*
F15	10A	**74D**	Power unit G	29/38-016*	**F23A**	.25A	**70F**	Power unit H	29/38-178*
F15A	.25A	**70F**	Power unit G	29/38-016*	**F24**	3A	**74B**	494GA power unit	29/38-024*
					F24A	.25A	**70F**	494GA power unit	29/38-024*
* If optional main store and IOP growth unit is not installed, these units move up one level									

CLEAR BLOWN FUSE — PROCESSOR CONTROL AND POWER DISTRIBUTION FRAMES

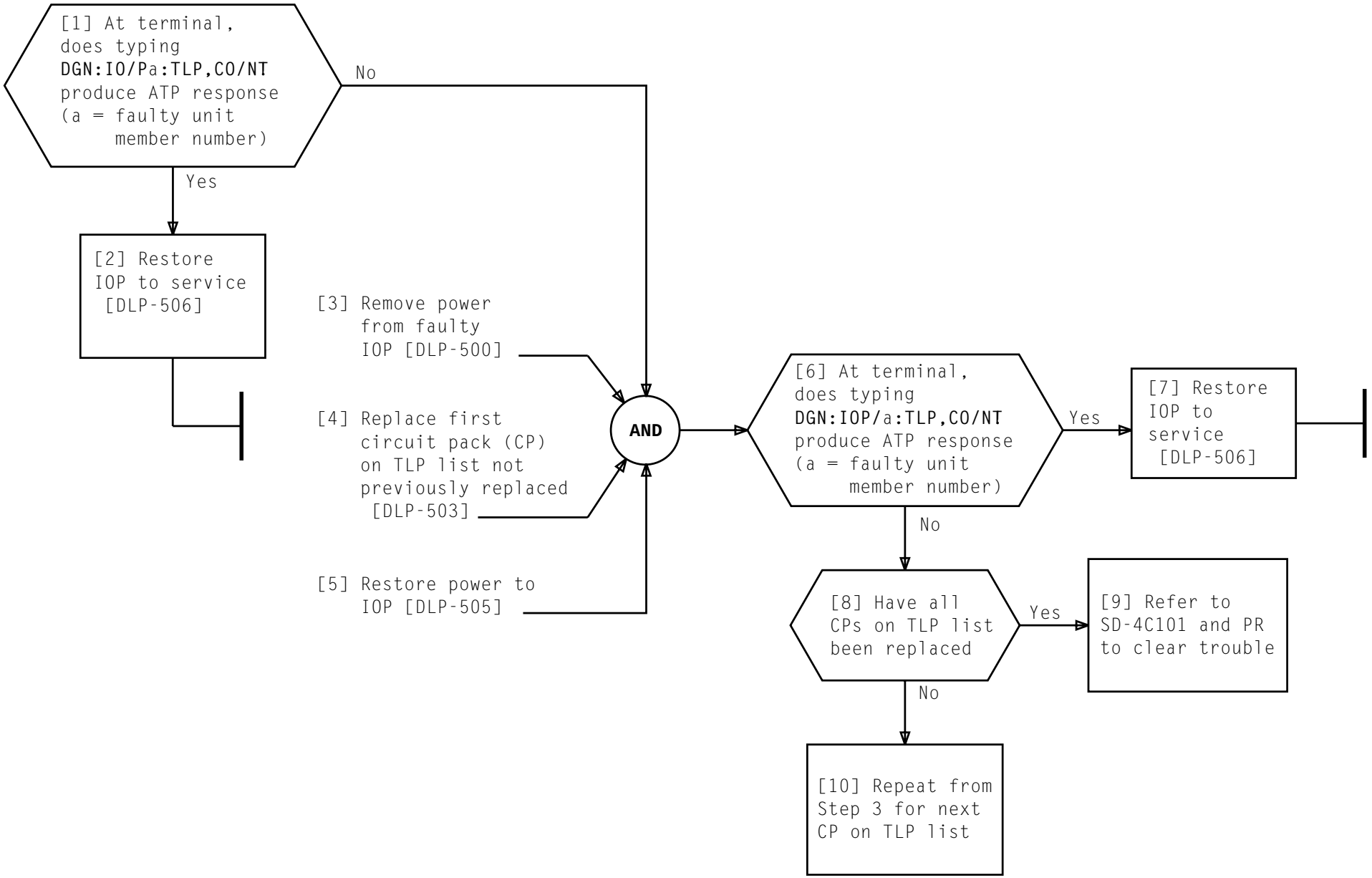
TABLE B		
SUSPECTED FAULTY LOCATION	**CIRCUIT AFFECTED**	**TAD**
Power distribution frame filter	Alarm circuit (74 and KS-type filter)	TAD-109
Power distribution frame filter	Alarm circuit (70-type filter fuse panel)	TAD-110
Power distribution frame filter	Alarm circuit (High current fuse panel)	TAD-111
Power distribution frame	Frame alarm circuit	TAD-112
Power distribution frame panel	Alarm circuits (74 and KS-type filter)	TAD-113
Power distribution frame panel	Alarm circuits (70-type filter fuse panel)	TAD-114
Power distribution frame panel	Alarm circuits (High-current — Converter Plant)	TAD-115
Power distribution frame panel	Alarm circuits (High-current — Battery Plant)	TAD-116
Power distribution frame panel	Alarm circuits (Capacitor panel)	TAD-117
Power distribution frame panel	Alarm circuits (KS-22012 Circuit Breaker Panel)	TAD-118
Processor control frame	—48V fuse failures	TAD-119



CLEAR CAP CHG CIRCUIT FAILURE



CLEAR DISK FILE CONTROLLER (DFC) DIAGNOSTIC FAILURE USING TROUBLE–LOCATING PROGRAM (TLP)



CLEAR INPUT/OUTPUT PROCESSOR (IOP) DIAGNOSTIC FAILURE USING TROUBLE-LOCATING PROGRAM (TLP)

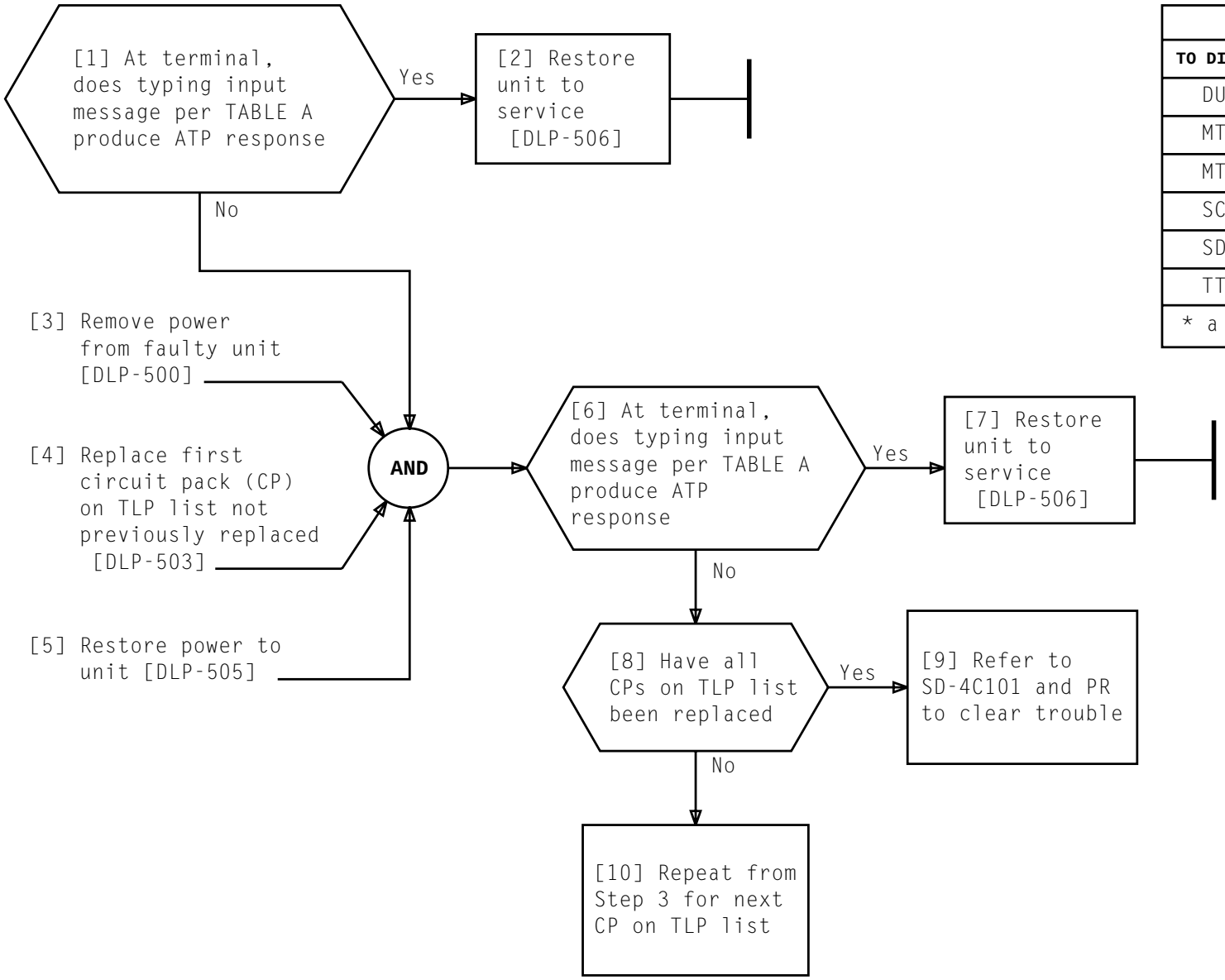


TABLE A

TO DIAGNOSE	INPUT MESSAGE*
DUIC	DGN:DUIC a:TLP!
MTC	DGN:MTC a:TLP!
MTTYC	DGN:MTTYC a:TLP!
SCSDC	DGN:SCSDC a:TLP!
SDLC	DGN:SDLC a:TLP!
TTYC	DGN:TTYC a:TLP!

* a = faulty unit member number

CLEAR PERIPHERAL CONTROLLER (PC) DIAGNOSTIC FAILURE USING TROUBLE-LOCATING PROGRAM (TLP)

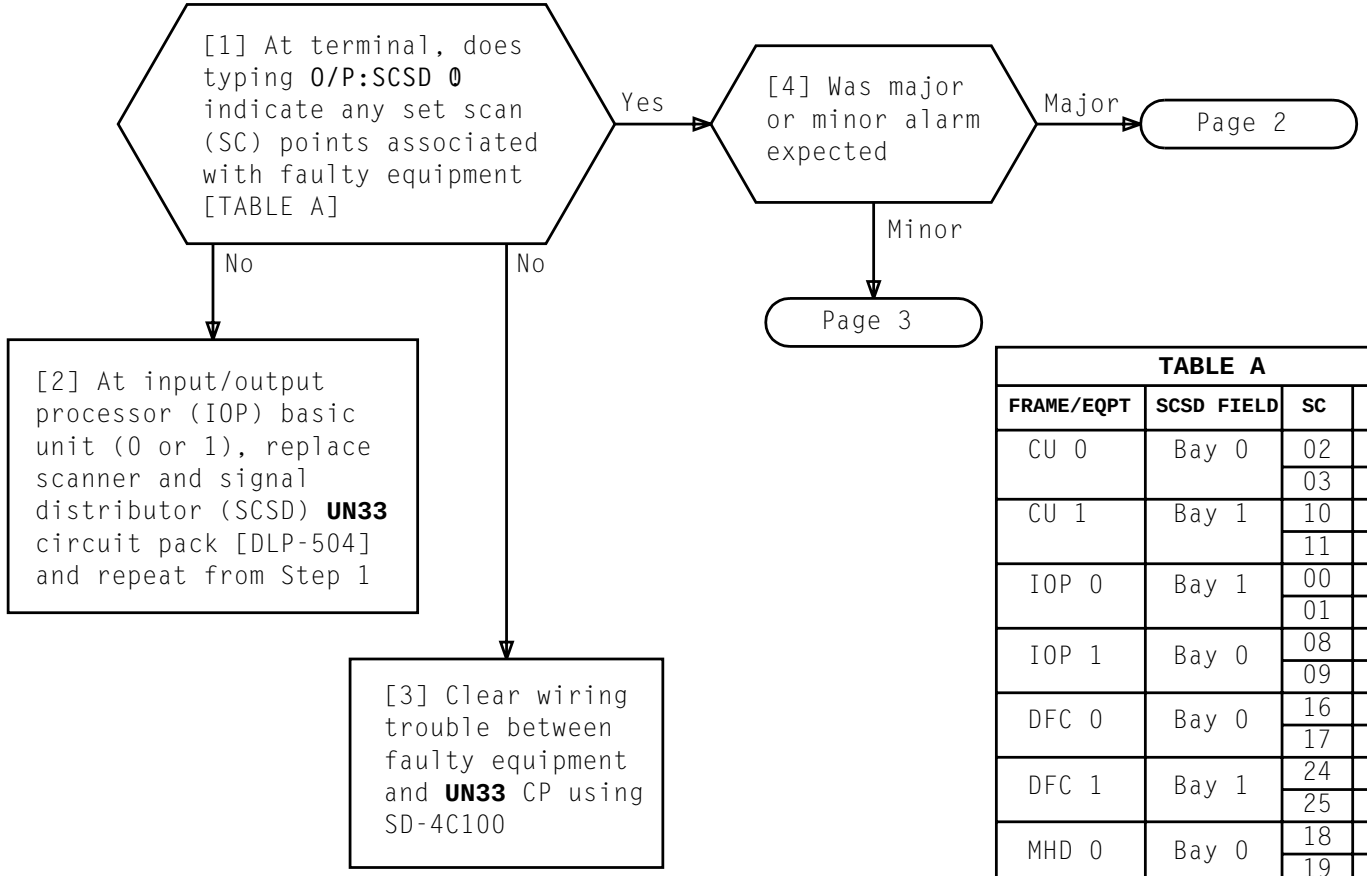
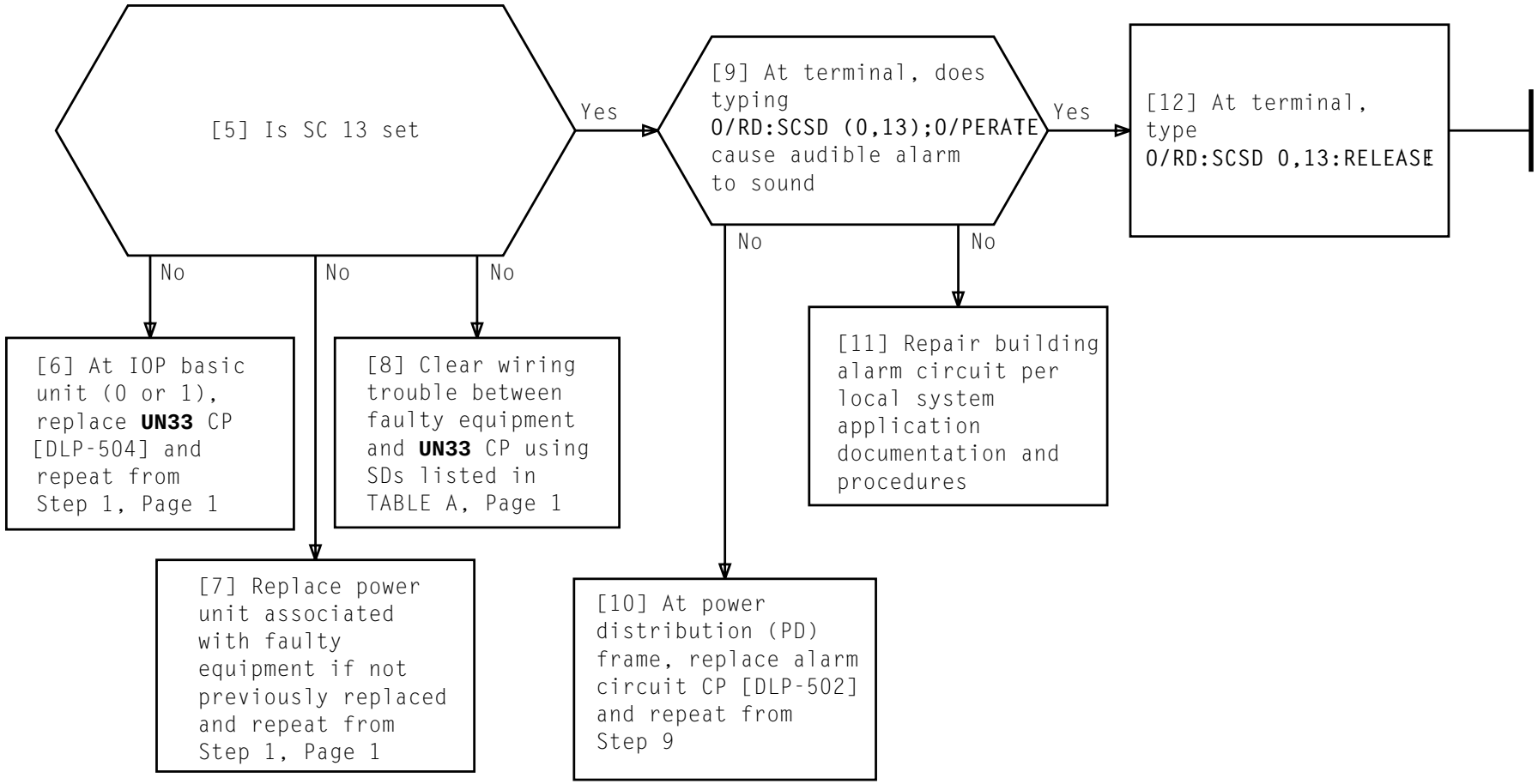


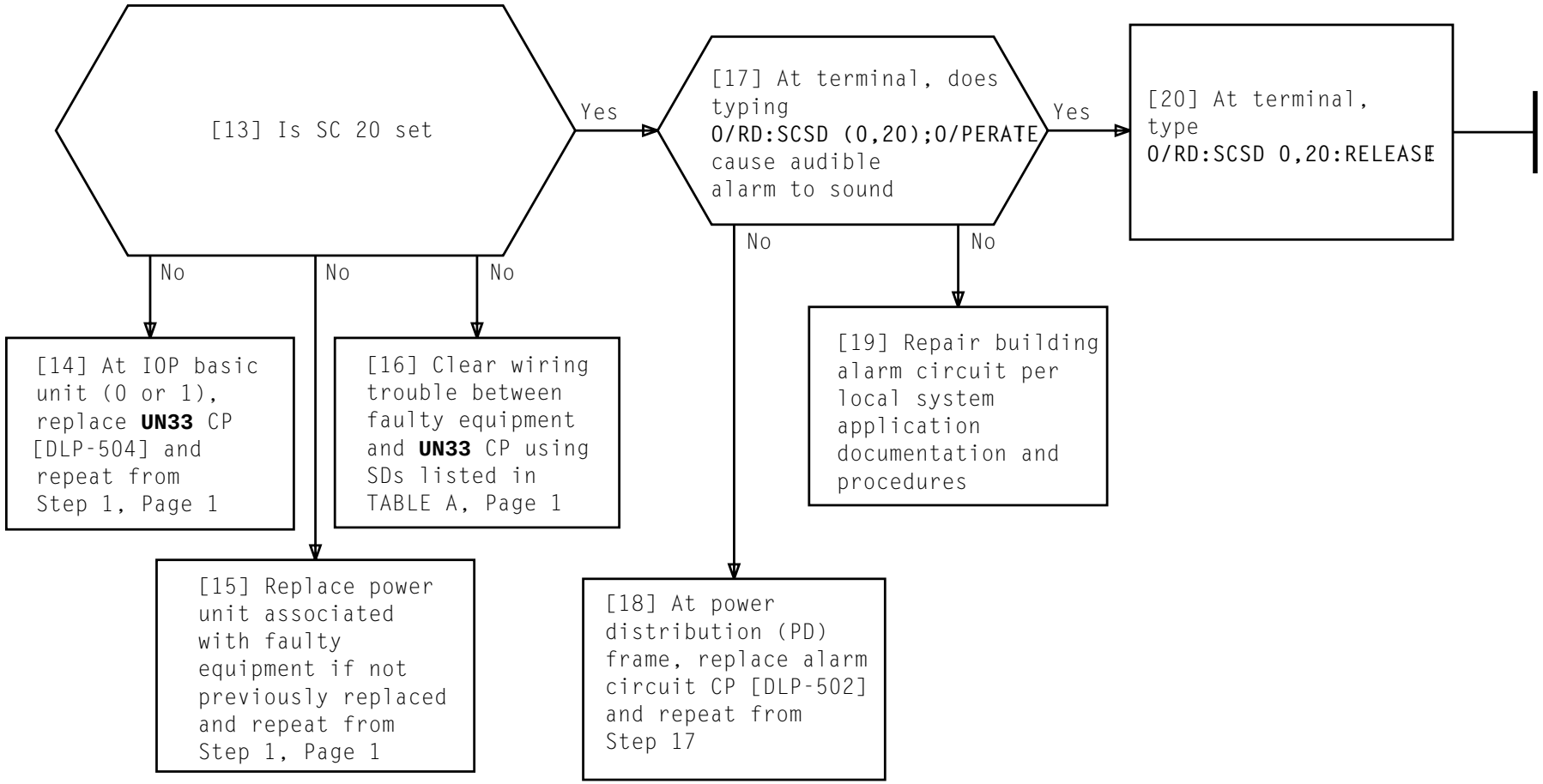
TABLE A

FRAME/EQPT	SCSD FIELD	SC	SD
CU 0	Bay 0	02	02
		03	03
CU 1	Bay 1	10	10
		11	11
IOP 0	Bay 1	00	00
		01	01
IOP 1	Bay 0	08	08
		09	09
DFC 0	Bay 0	16	16
		17	17
DFC 1	Bay 1	24	24
		25	25
MHD 0	Bay 0	18	18
		19	19
MHD 1	Bay 1	26	26
		27	27
PD 0	Bay 0	44	—
		45	—
ROP	Bay 0	15	—
		38	—
		39	—
MTTY	Bay 0	11	—
		36	—
		37	—

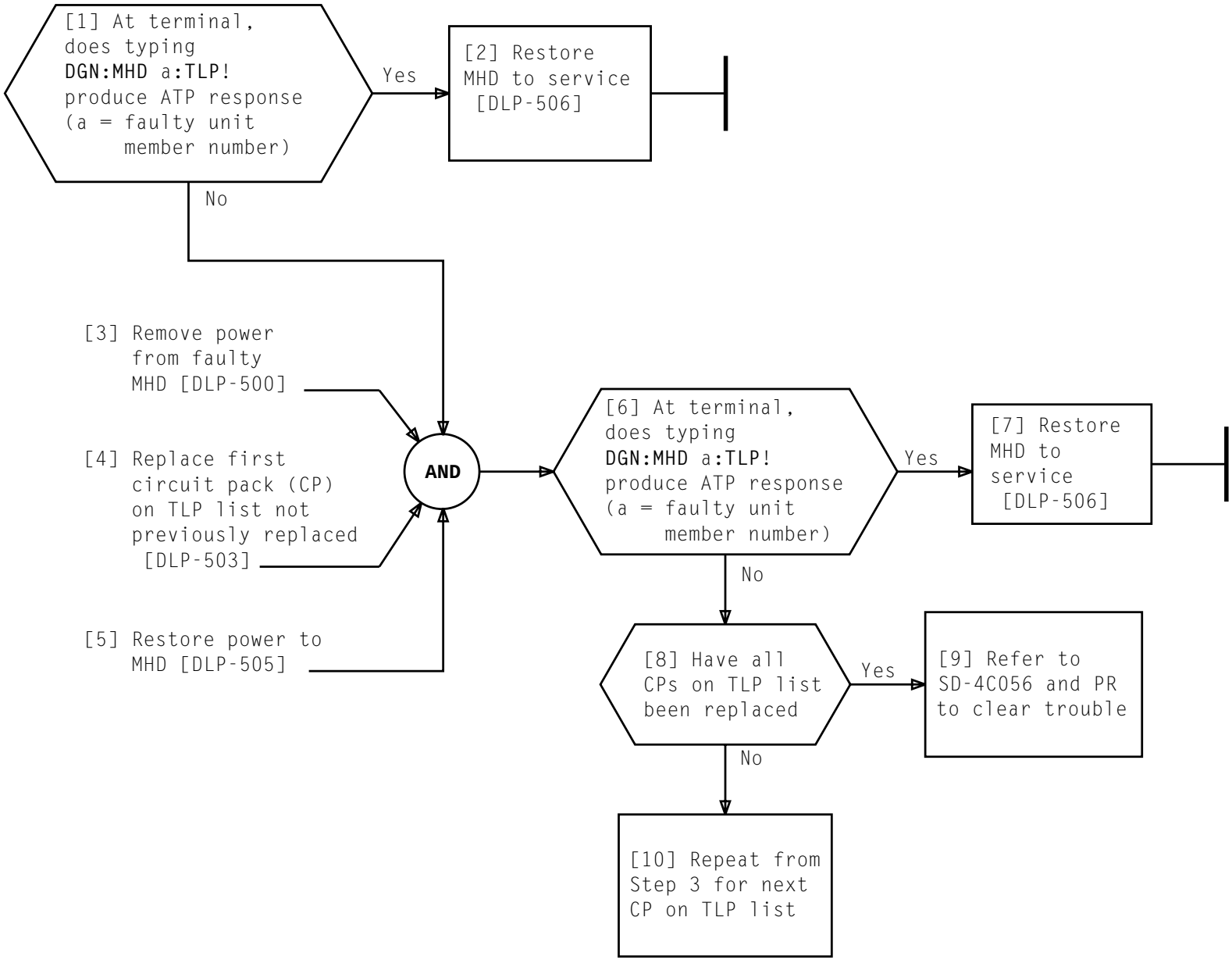
CLEAR POWER ALARM FAILURES



CLEAR POWER ALARM FAILURES



CLEAR POWER ALARM FAILURES



CLEAR 300-MB MOVING HEAD DISK (MHD) DIAGNOSTIC FAILURE USING TROUBLE-LOCATING PROGRAM (TLP)

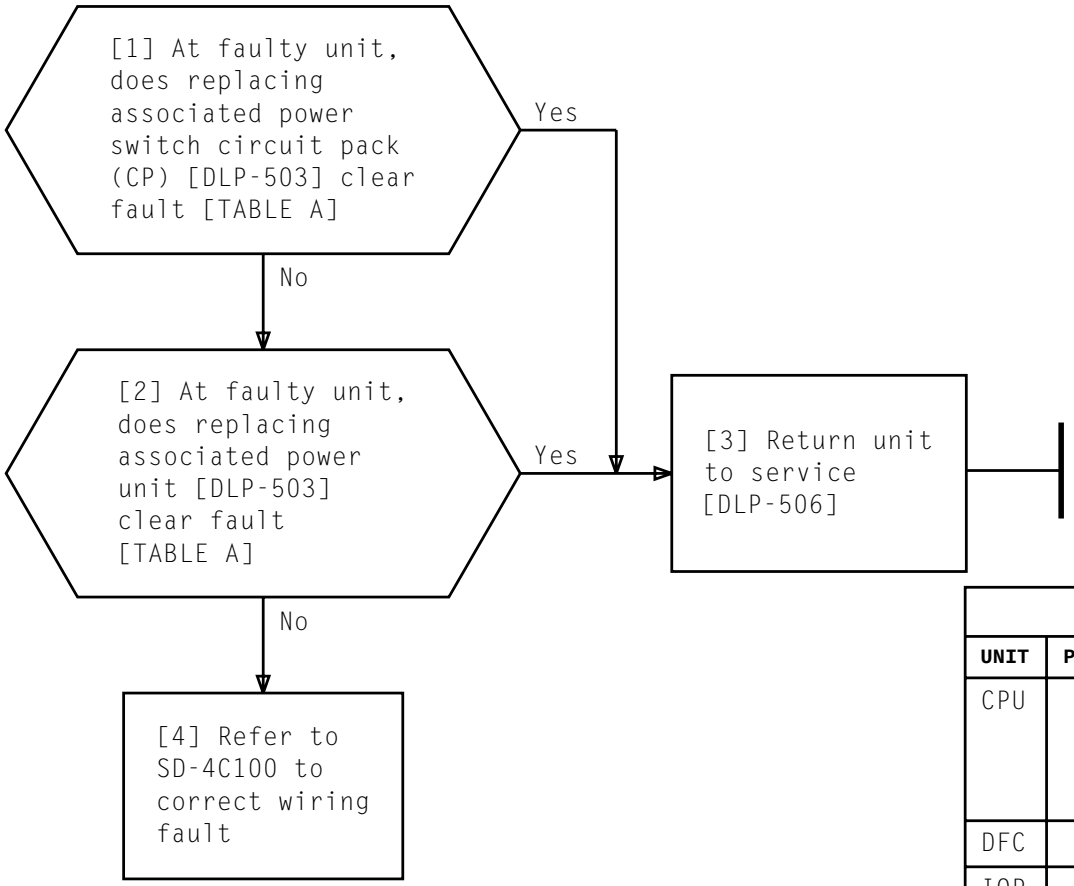
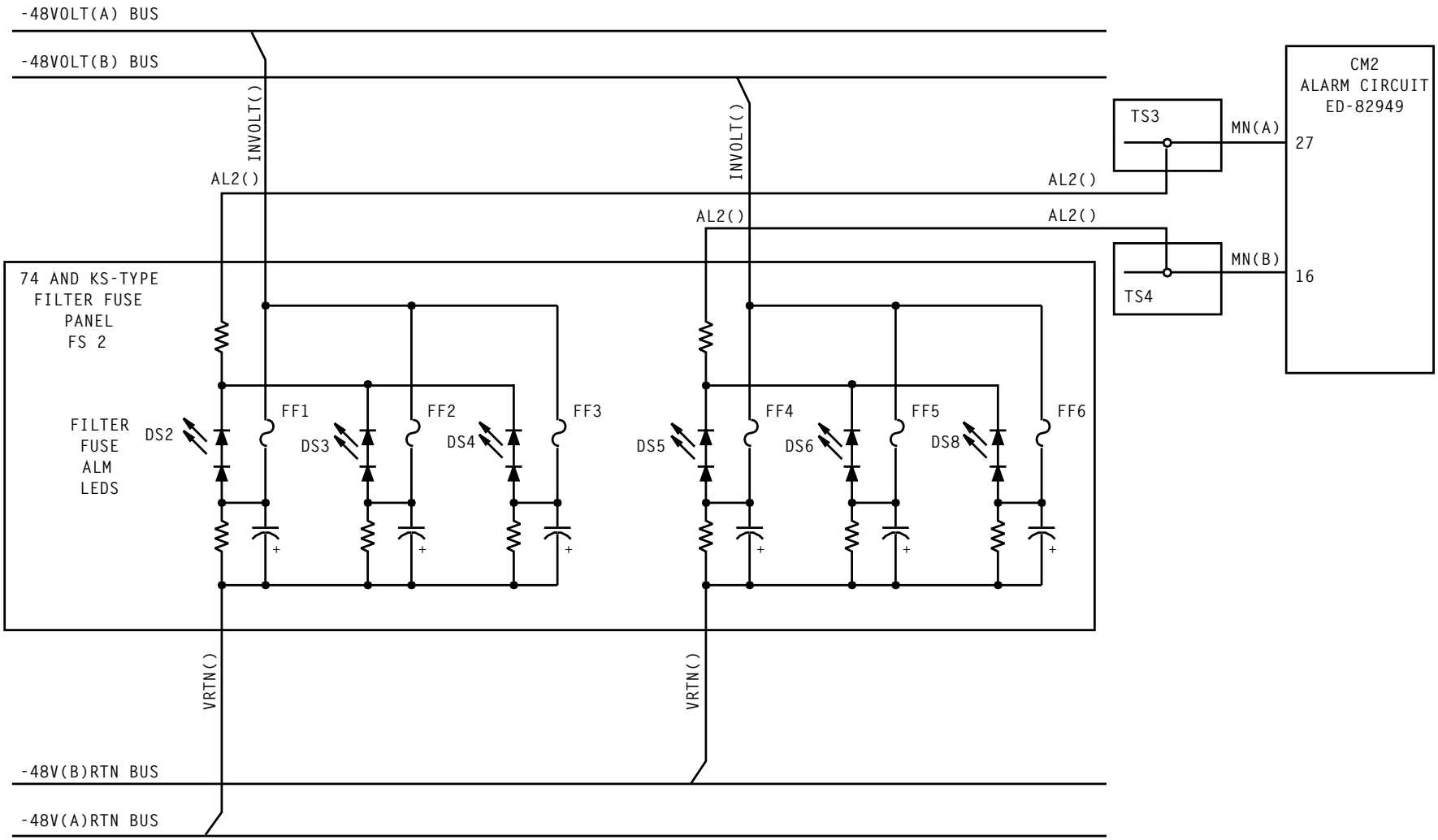


TABLE A

UNIT	POWER SWITCH	LOCATION	POWER UNIT	TYPE	LOCATION
CPU	TN5	56-162	**A**	**495FA**	56-016
			B	**495FA**	56-178
			D	**495FA**	47-178
			F	**495FA**	38-178
DFC	TN3	47-074	**C**	**495FA**	47-016
IOP	TN6	29/38-162*	**E**	**495FA**	38-016
			J	**494GA**	29/38-024*
			H	**495FA**	29/38-178*

* If optional growth unit is not installed, these units move up one level

CLEAR UNIT POWER FAULT



POWER DISTRIBUTION FRAME FILTER ALARM CIRCUIT FOR 74 AND KS-TYPE FILTER FUSE PANEL

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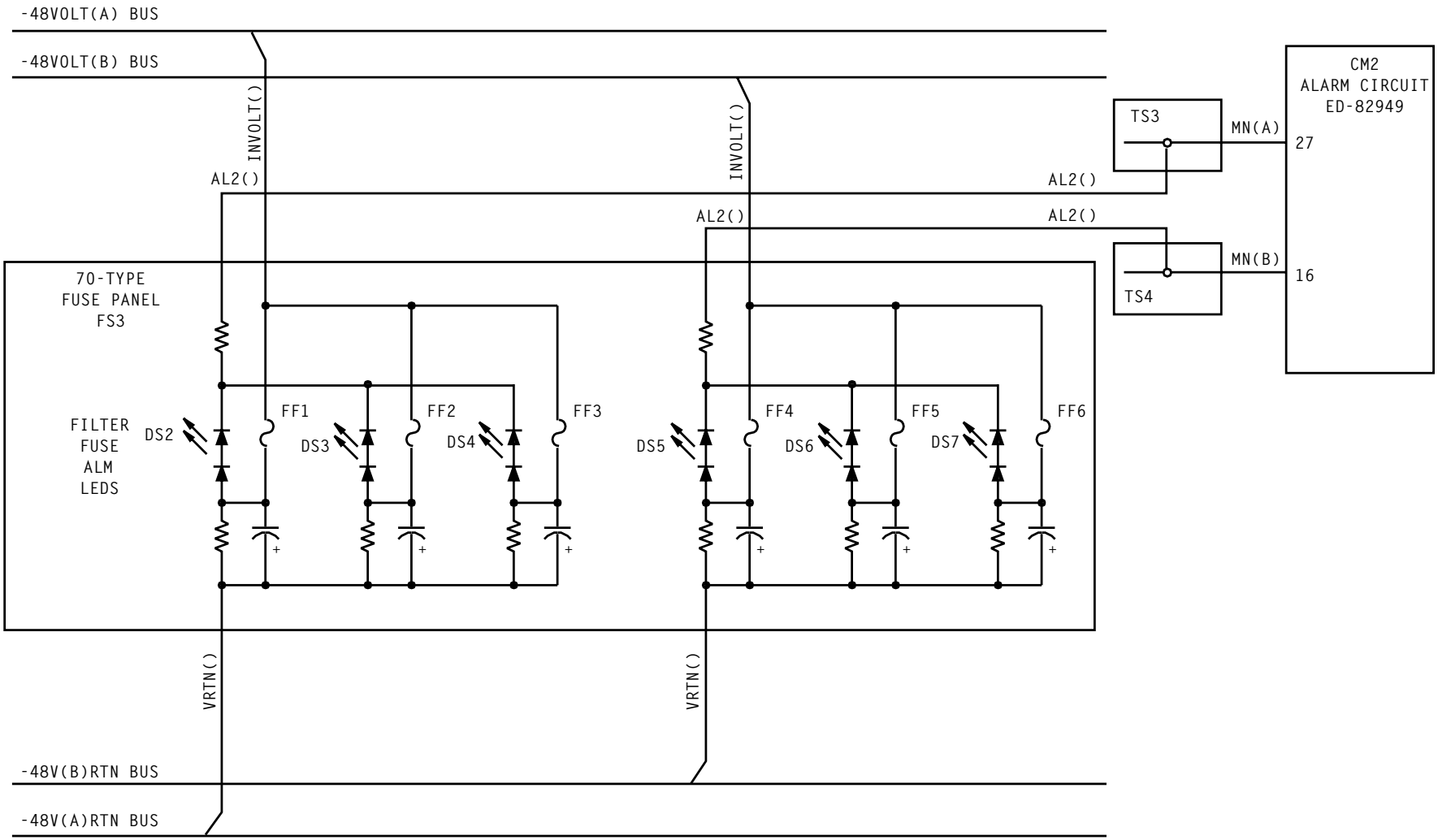

POWER DISTRIBUTION FRAME FILTER ALARM CIRCUIT FOR 70-TYPE FILTER FUSE PANEL

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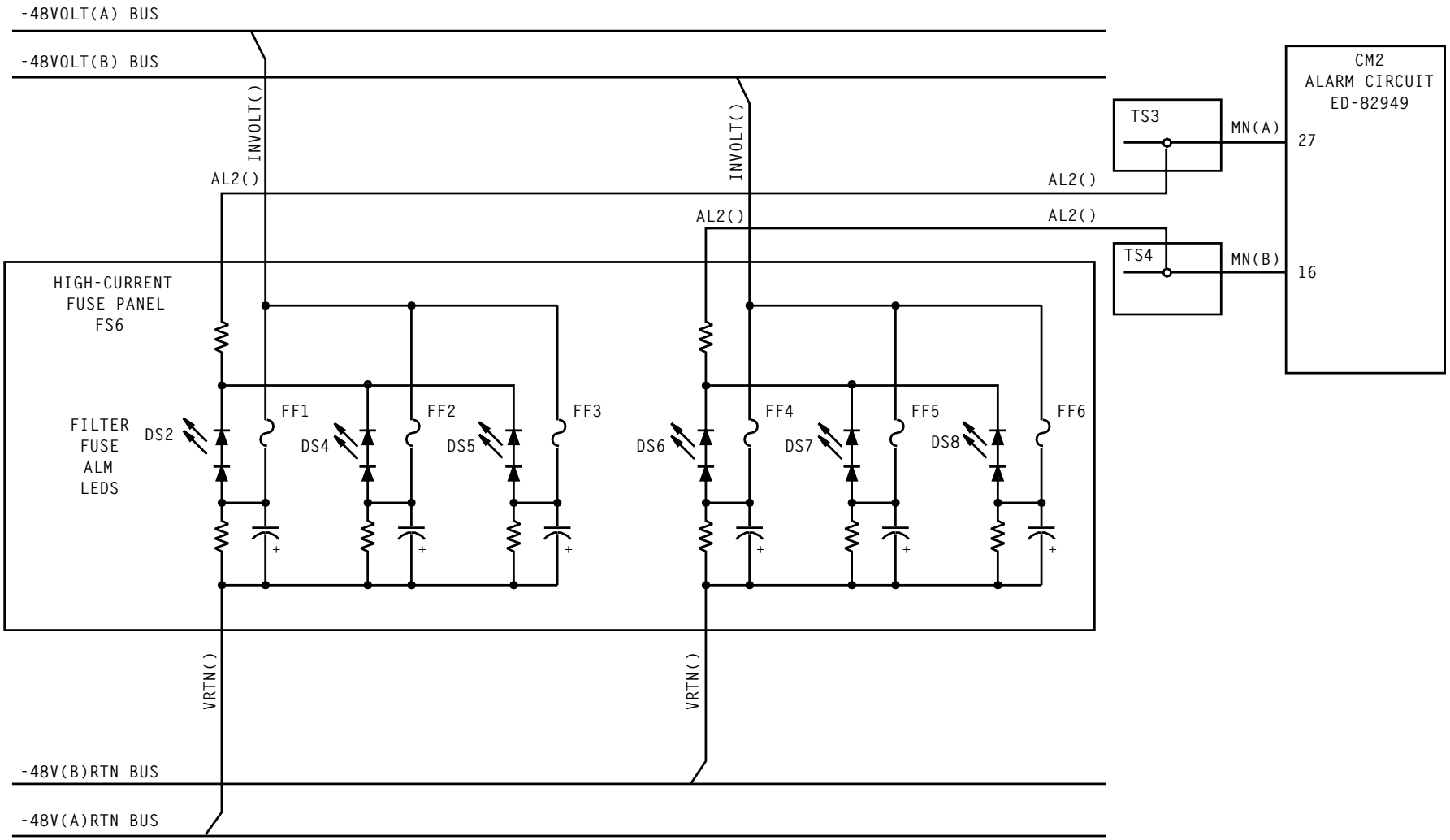

POWER DISTRIBUTION FRAME FILTER ALARM CIRCUIT FOR HIGH-CURRENT FUSE PANEL

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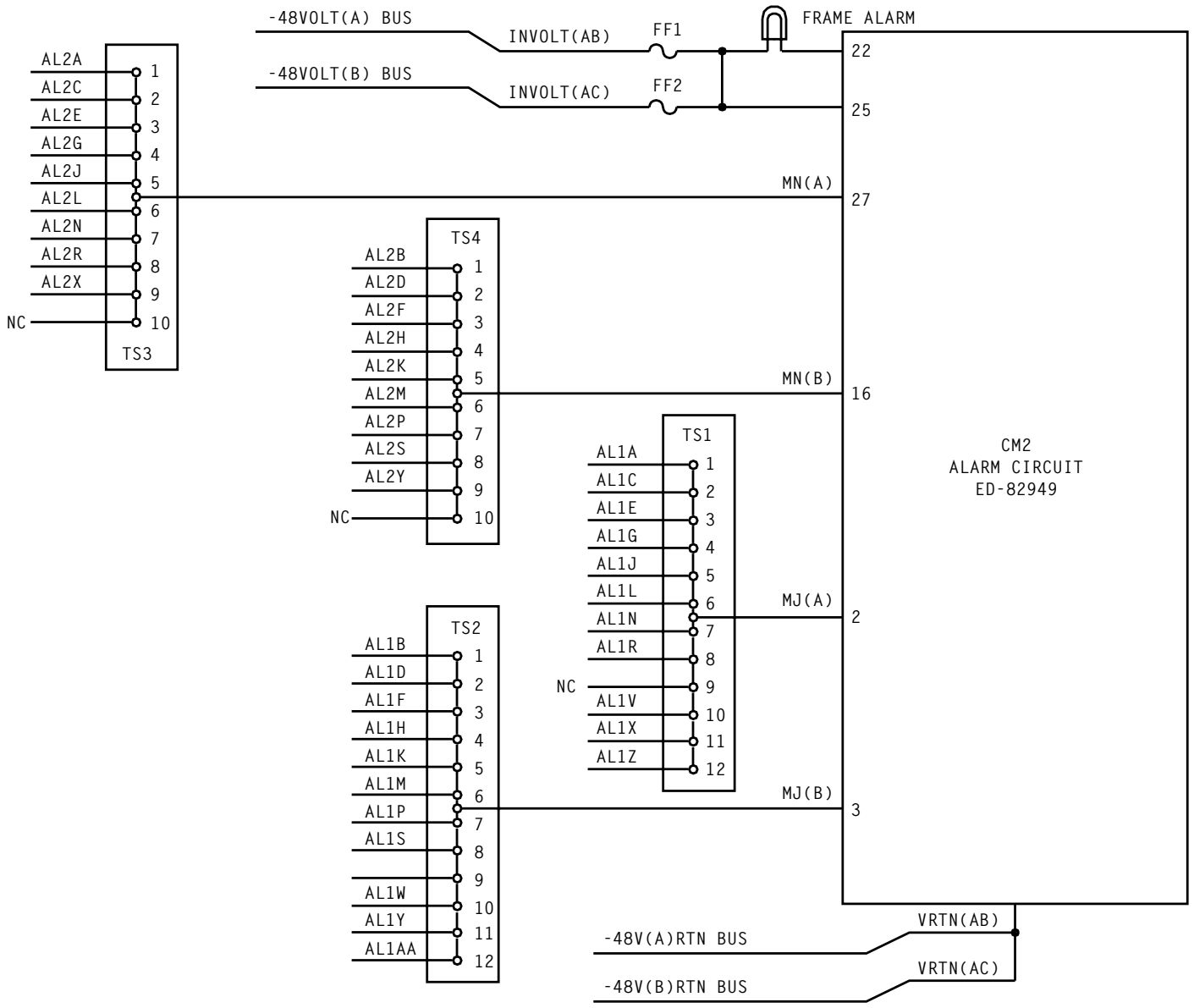

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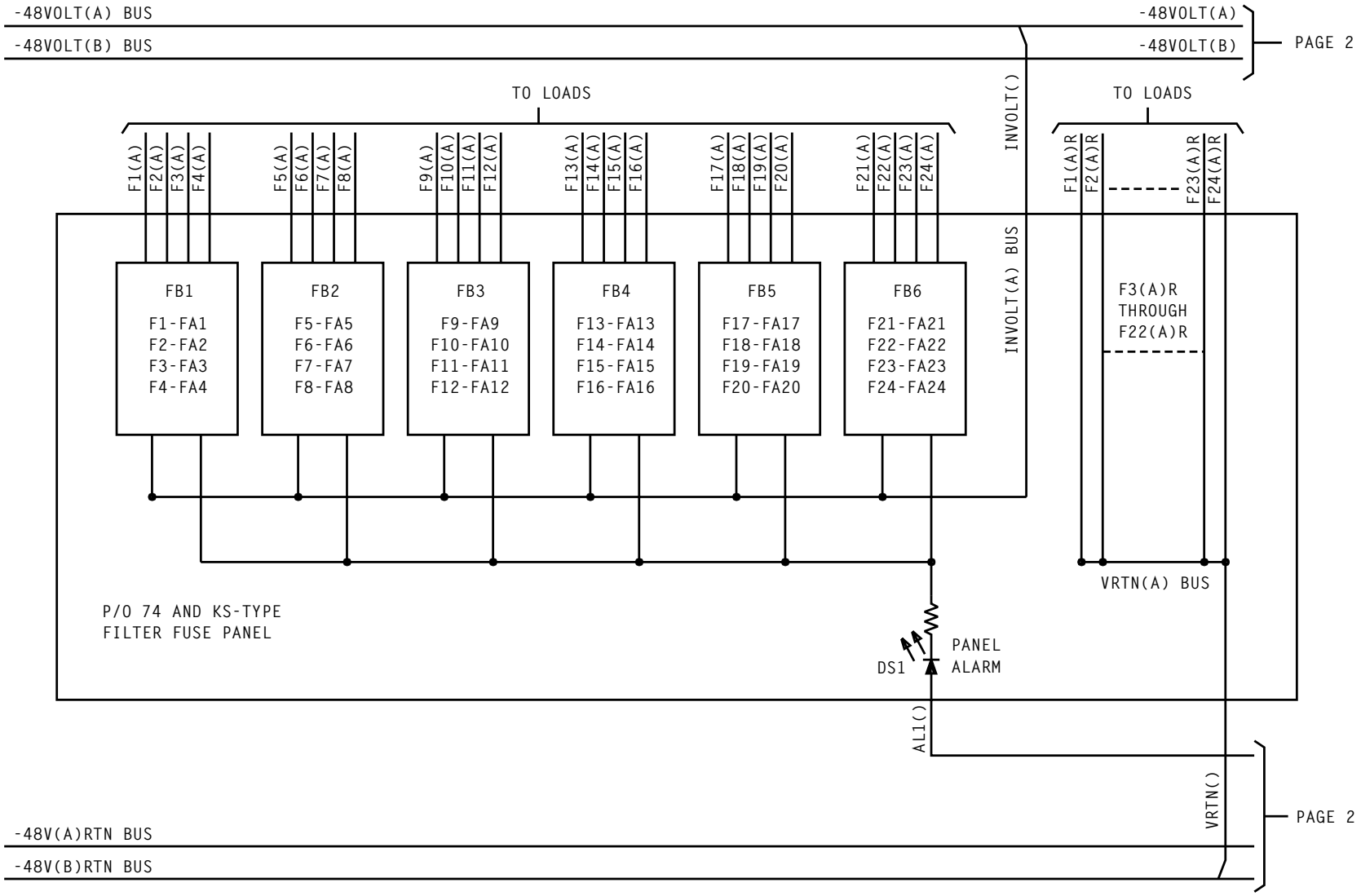
POWER DISTRIBUTION FRAME FRAME ALARM CIRCUIT



POWER DISTRIBUTION FRAME PANEL ALARM CIRCUITS FOR 74 AND KS-TYPE FILTER FUSE PANEL

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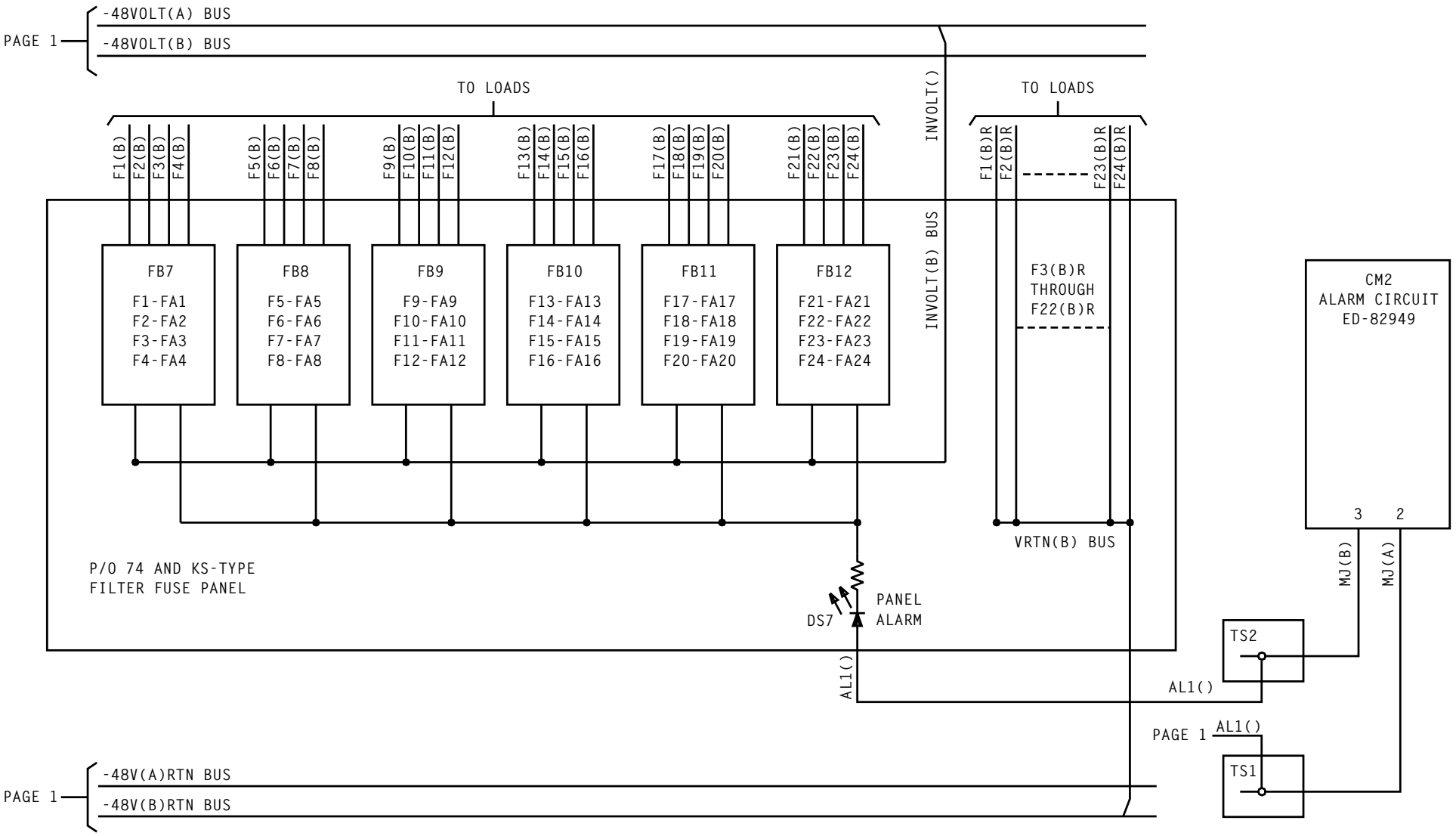

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUITS FOR 74 AND KS-TYPE FILTER FUSE PANEL

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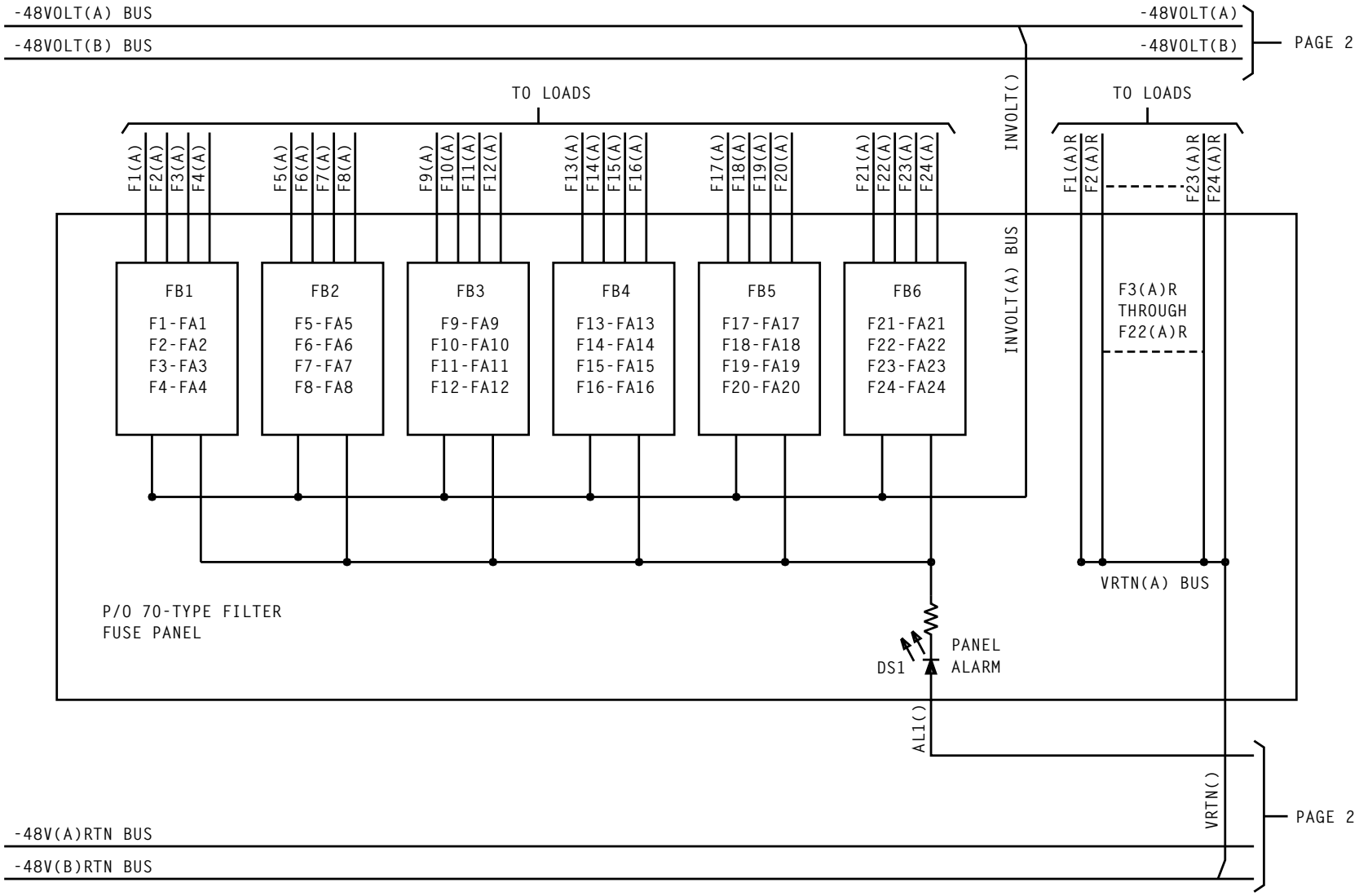

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUITS FOR 70-TYPE FILTER FUSE PANEL

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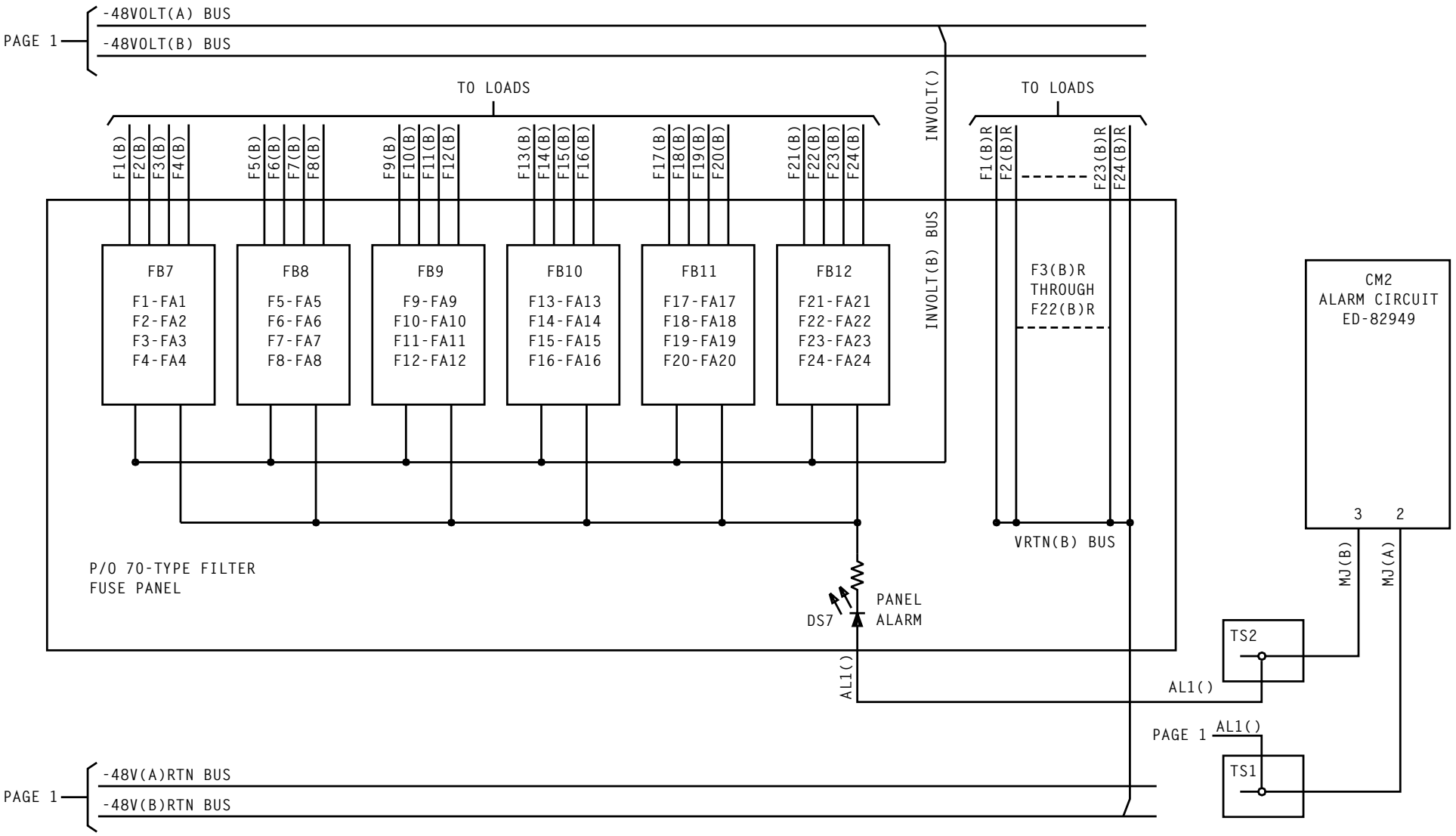

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUITS FOR 70-TYPE FILTER FUSE PANEL

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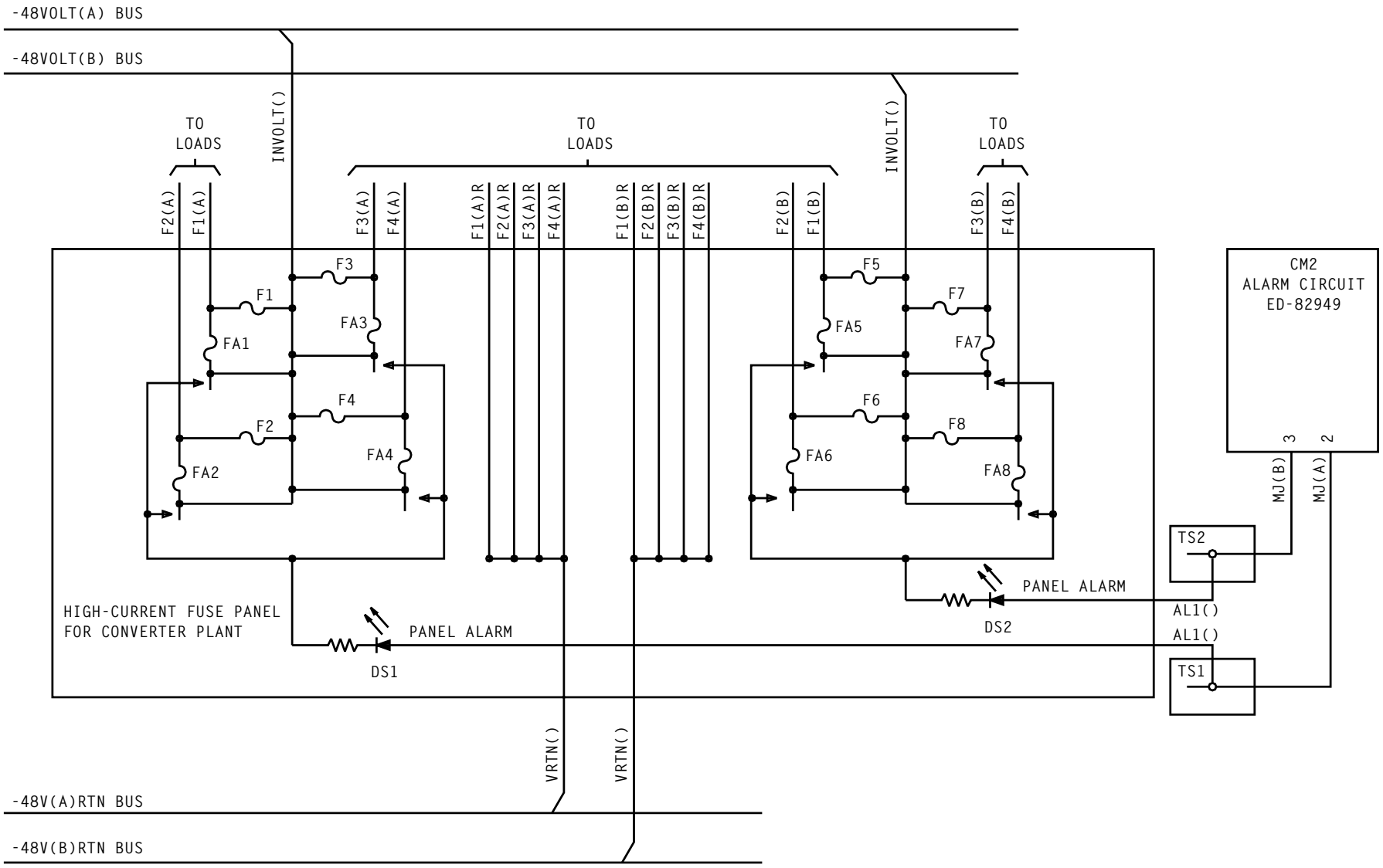

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUIT FOR HIGH-CURRENT FUSE PANEL (CONVERTER PLANT)

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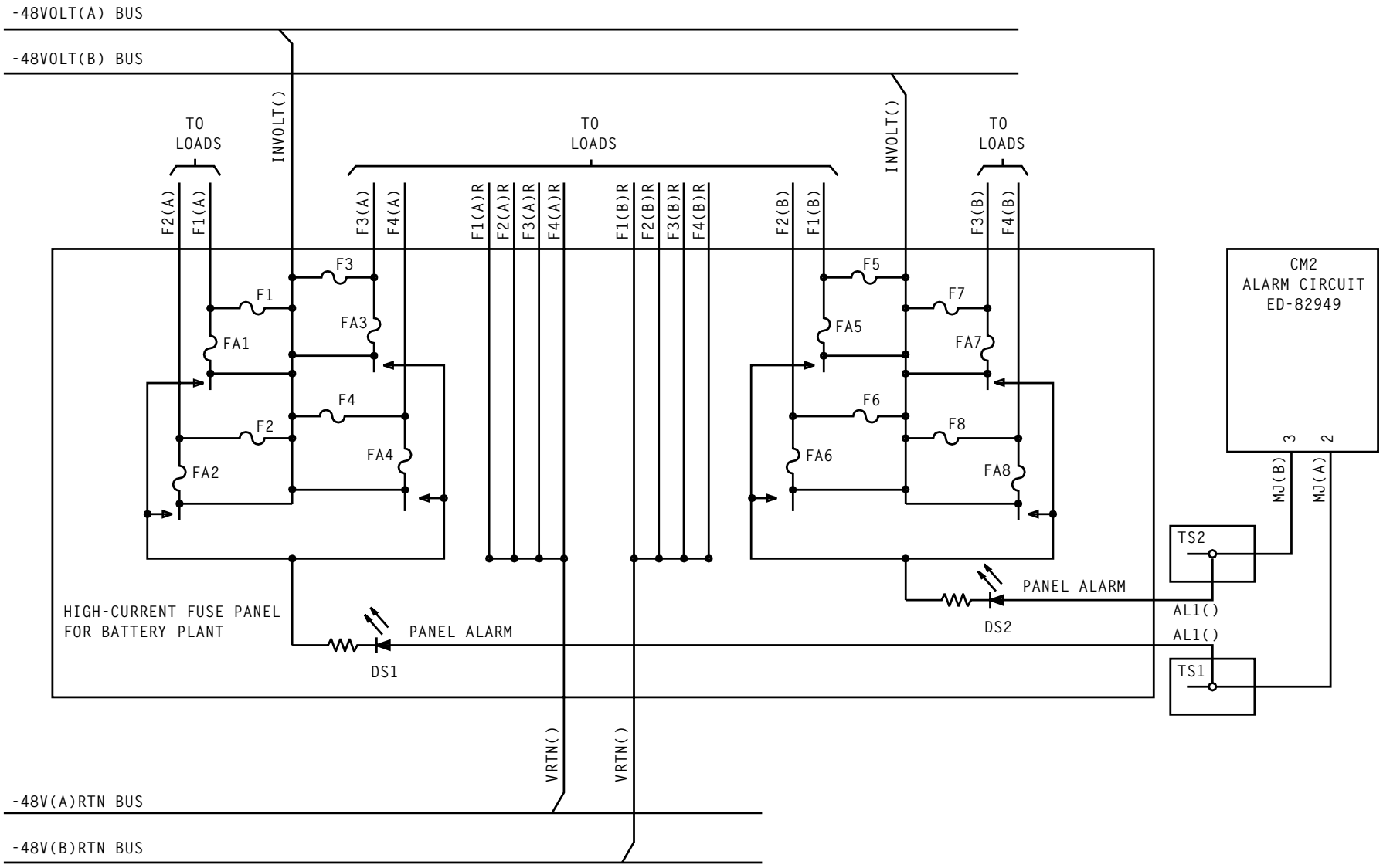

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUIT FOR HIGH-CURRENT FUSE PANEL (BATTERY PLANT)

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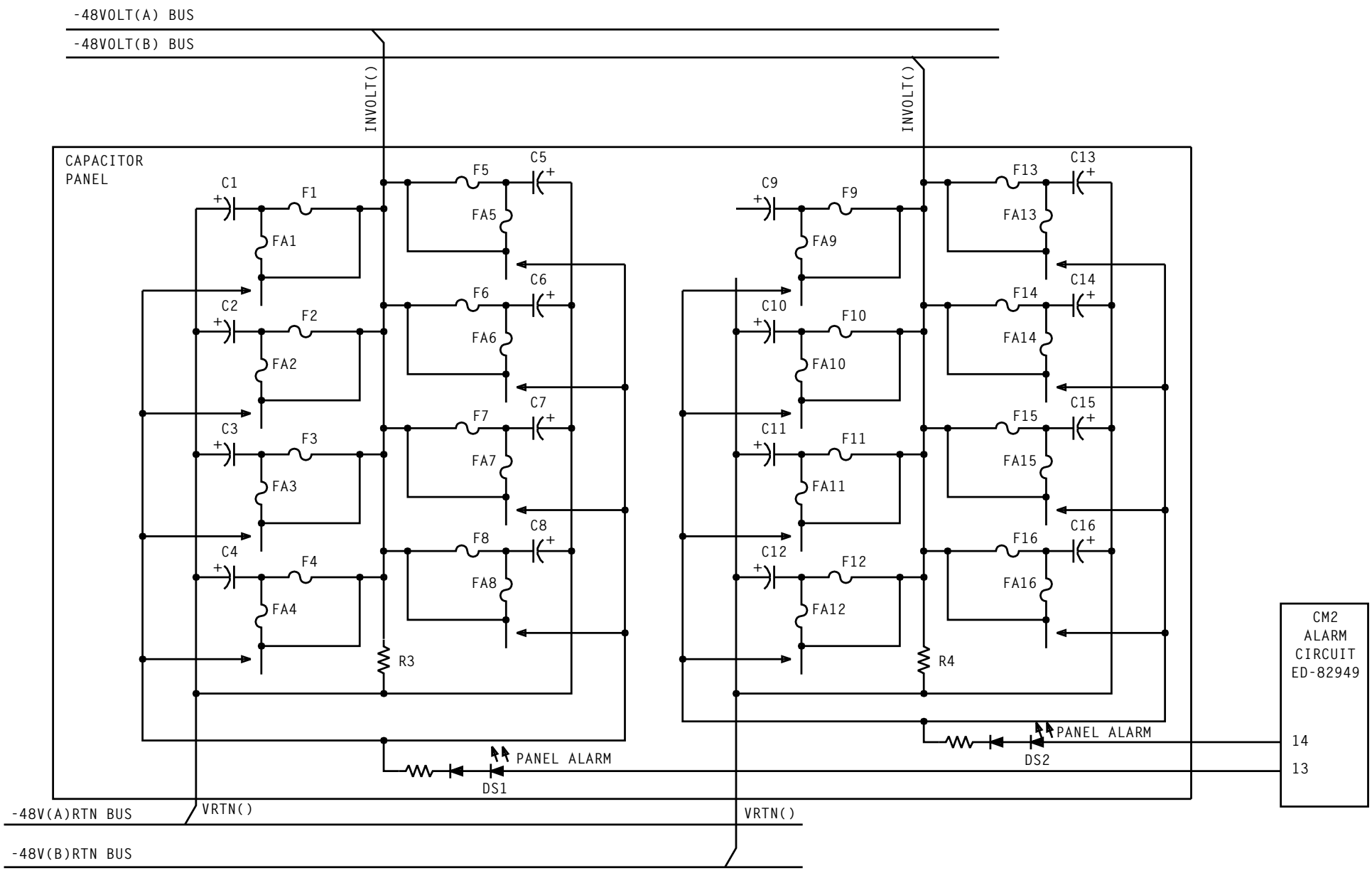

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUIT FOR CAPACITOR PANEL

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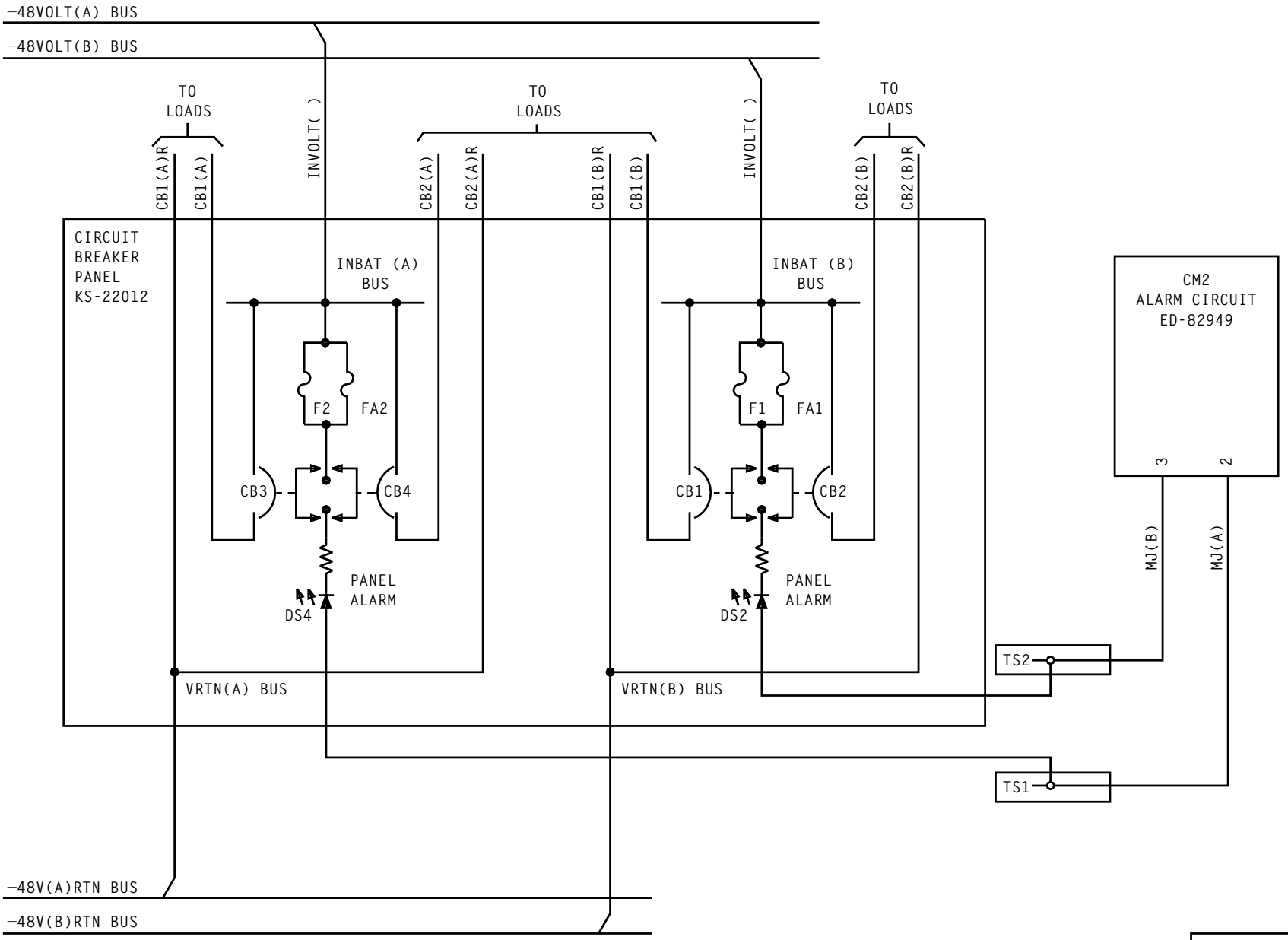

POWER DISTRIBUTION FRAME PANEL ALARM CIRCUIT FOR KS-22012 CIRCUIT BREAKER PANEL

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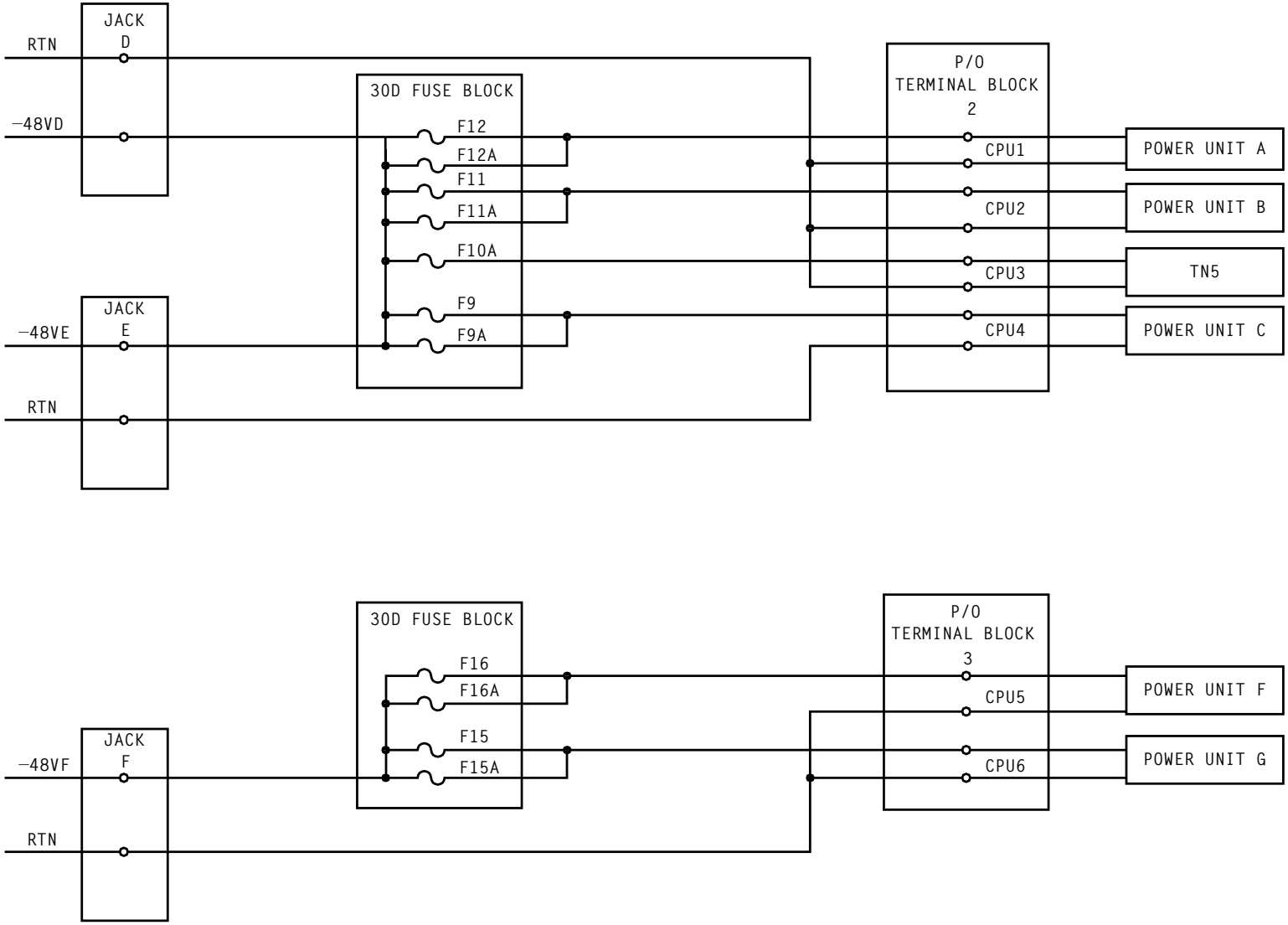


FIG. 1 — Fuse Connection (CPU)

-48V FUSE FAILURES (PROCESSOR CONTROL FRAME ONLY)

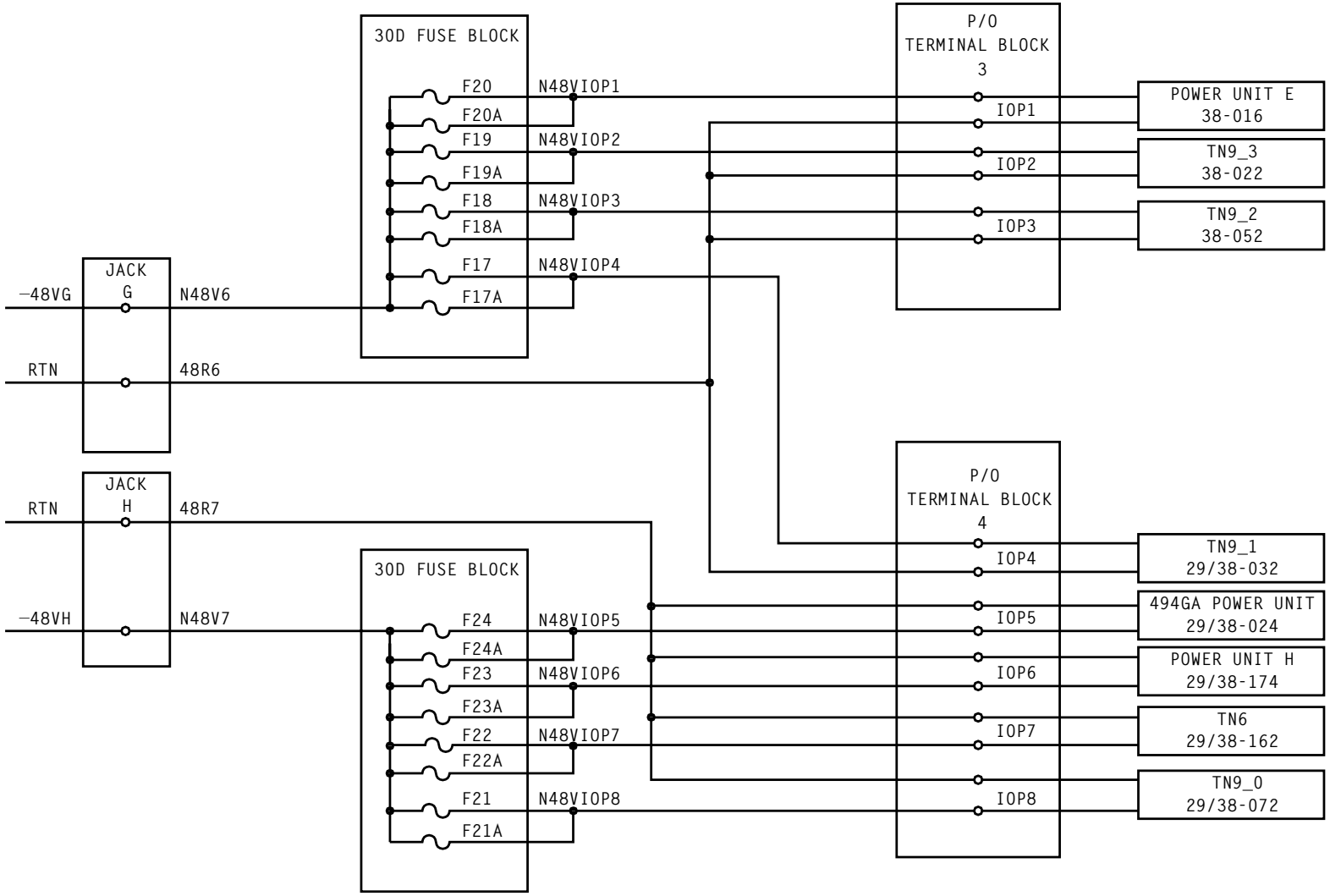


FIG. 2 — Fuse Connection (IOP)

-48V FUSE FAILURES (PROCESSOR CONTROL FRAME ONLY)

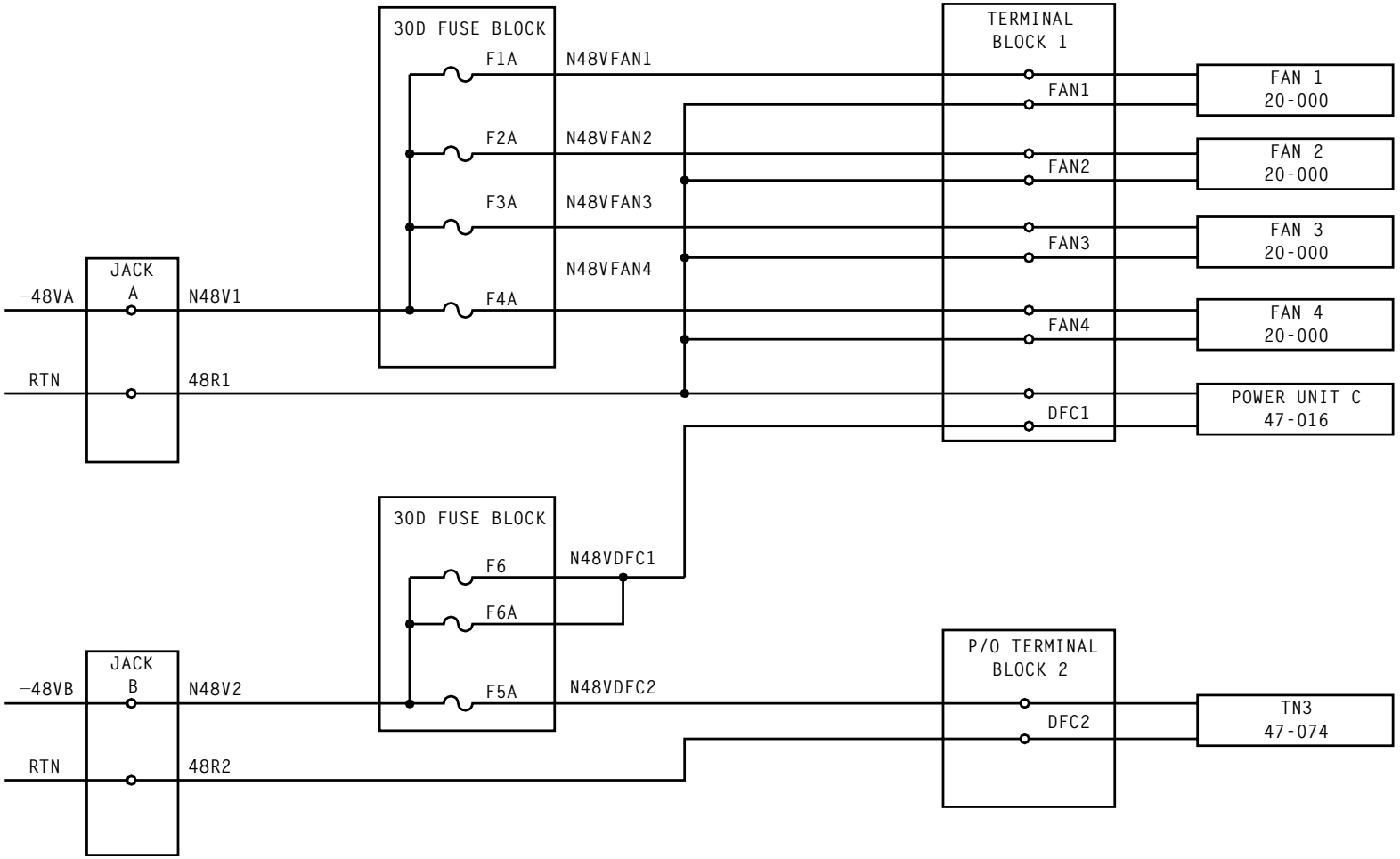
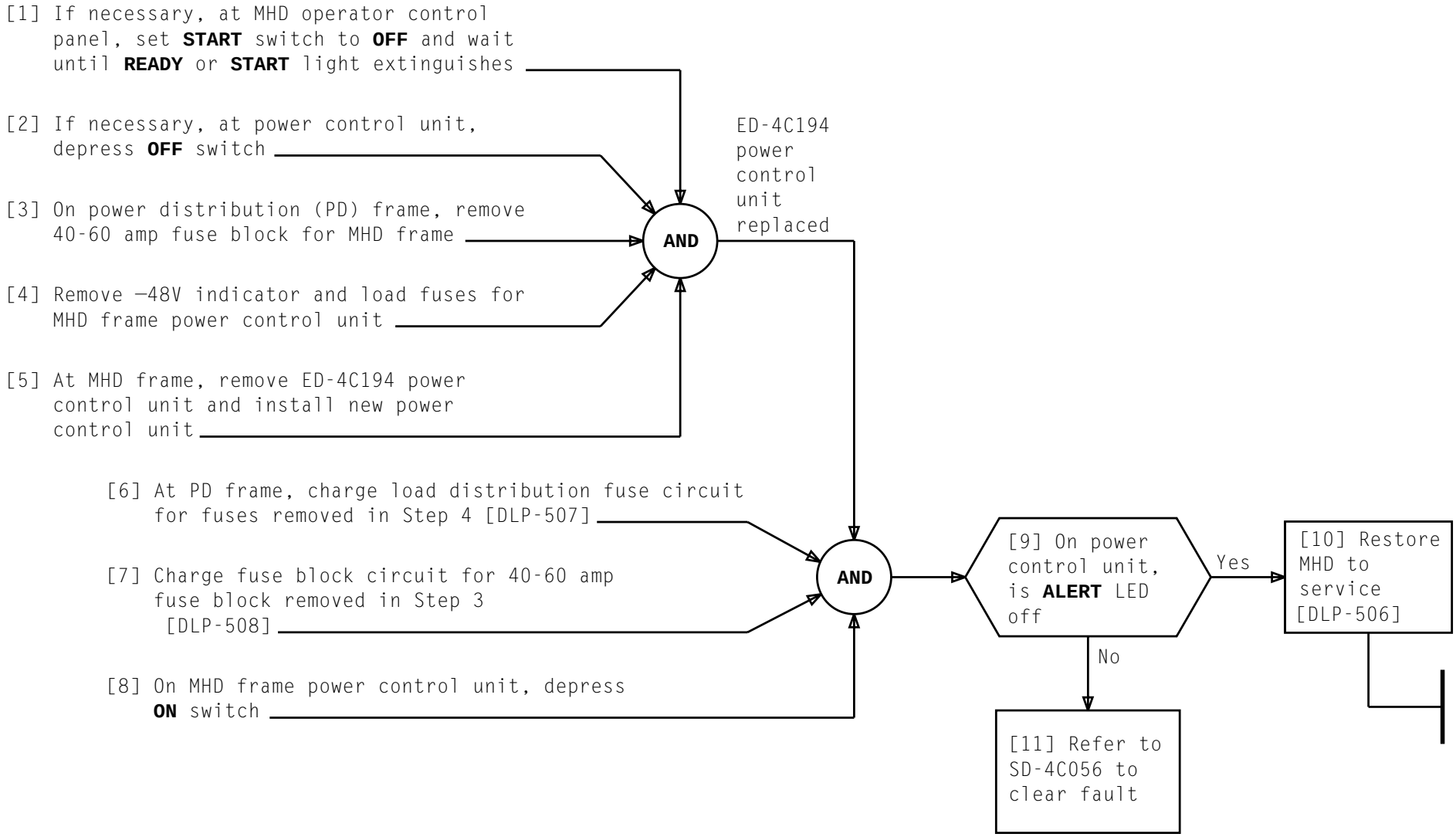
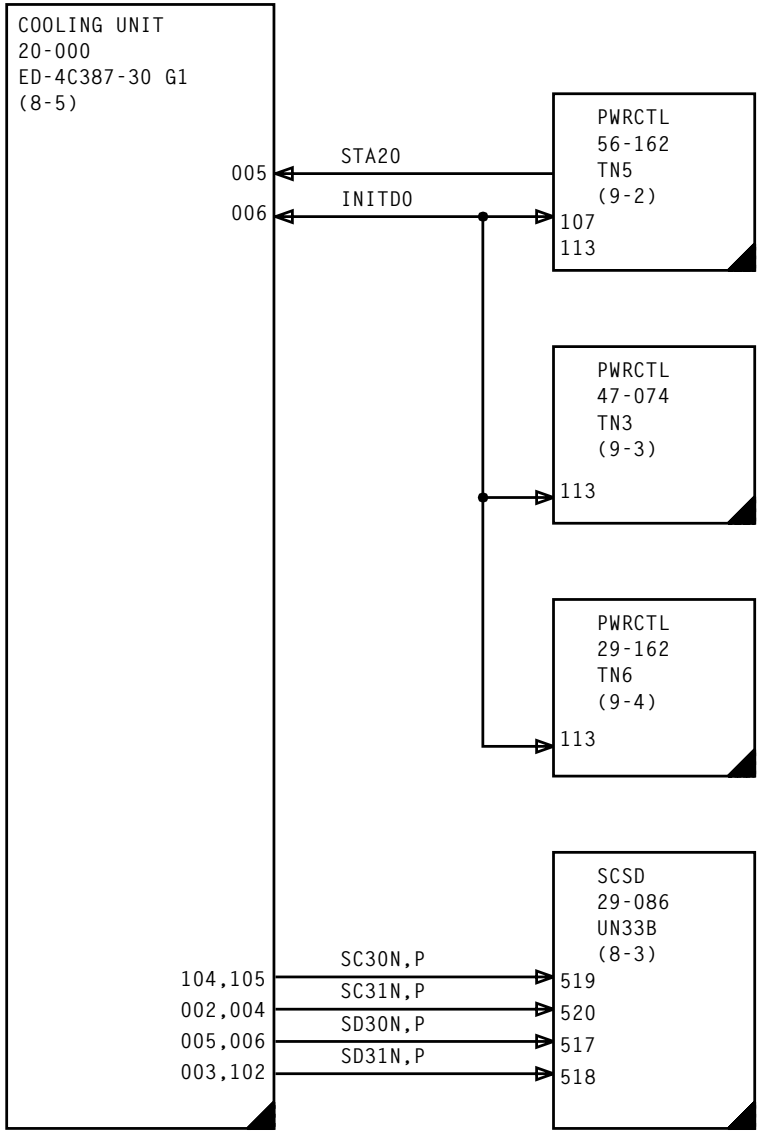


FIG. 3 — Fuse Connection (Fans and DFC)

-48V FUSE FAILURES (PROCESSOR CONTROL FRAME ONLY)



CLEAR 300-MB MOVING HEAD DISK (MHD) POWER CONTROL UNIT FAILURE



COOLING UNIT FAILURE

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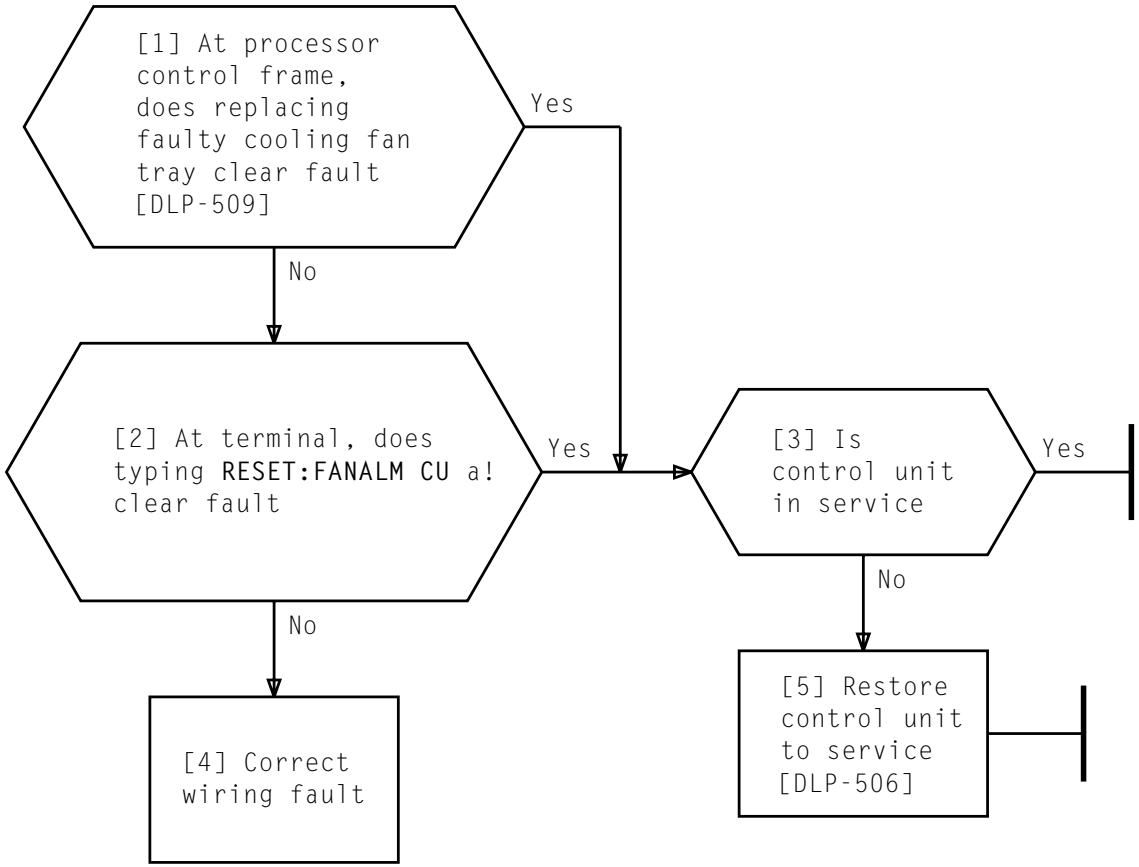
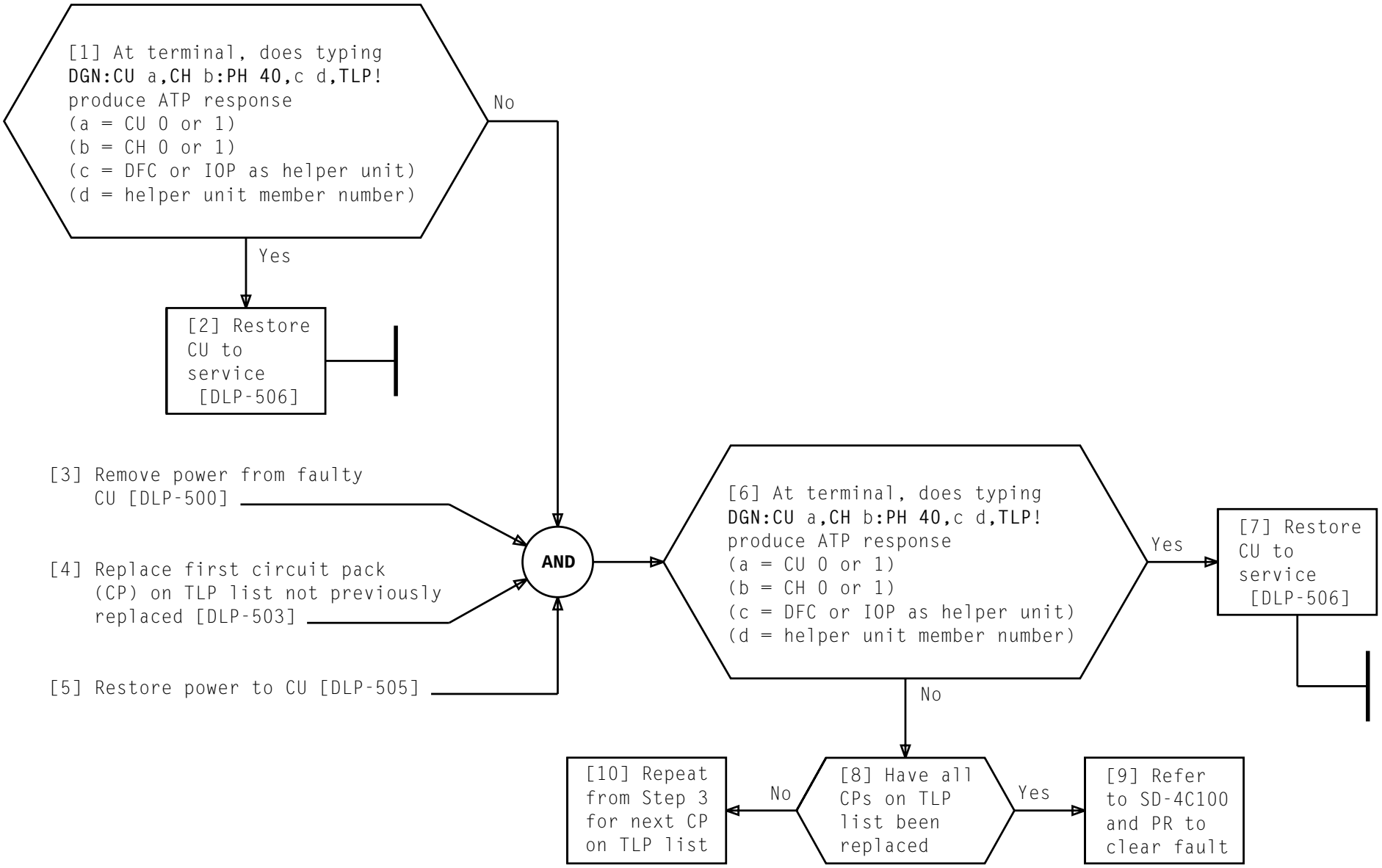
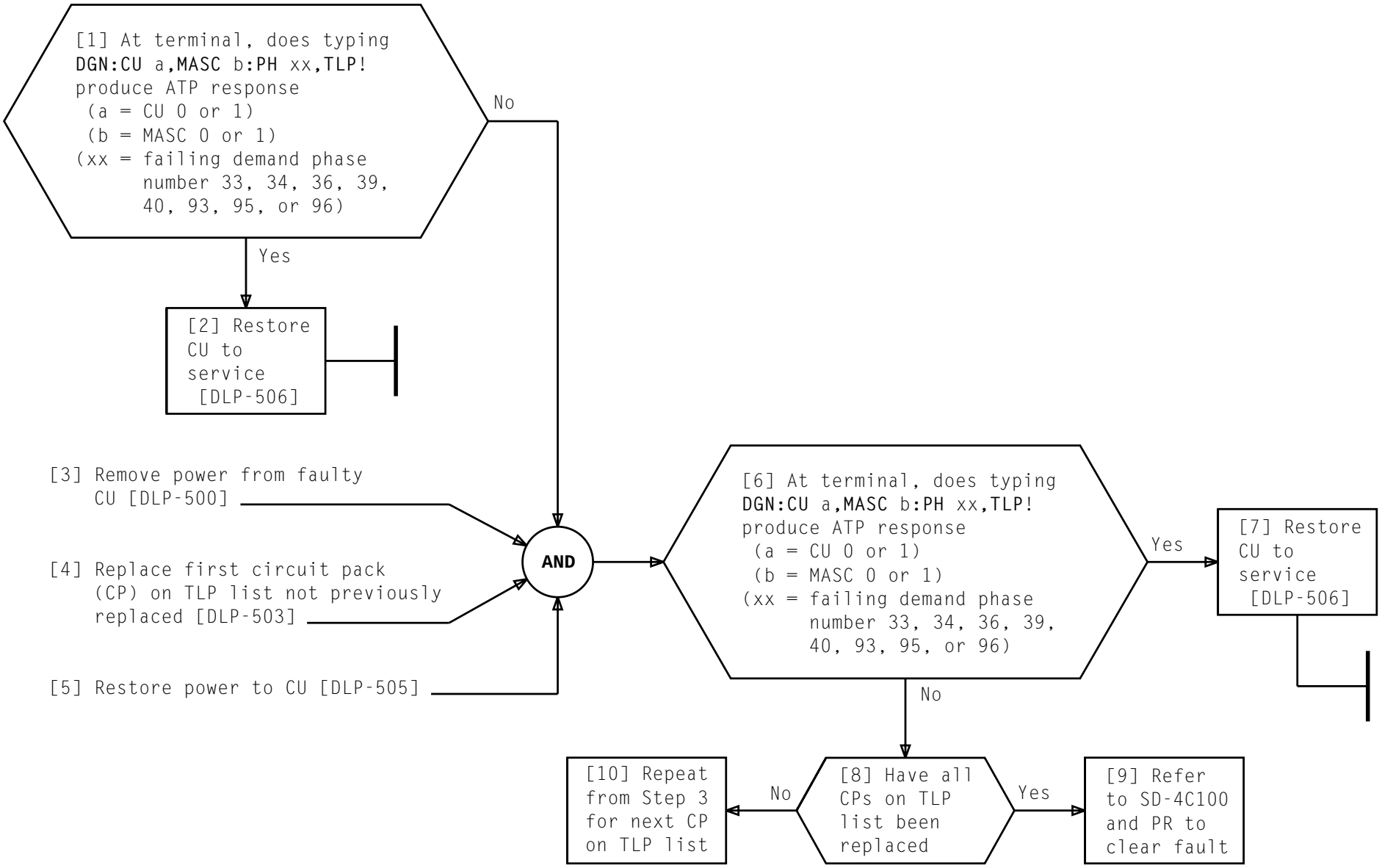


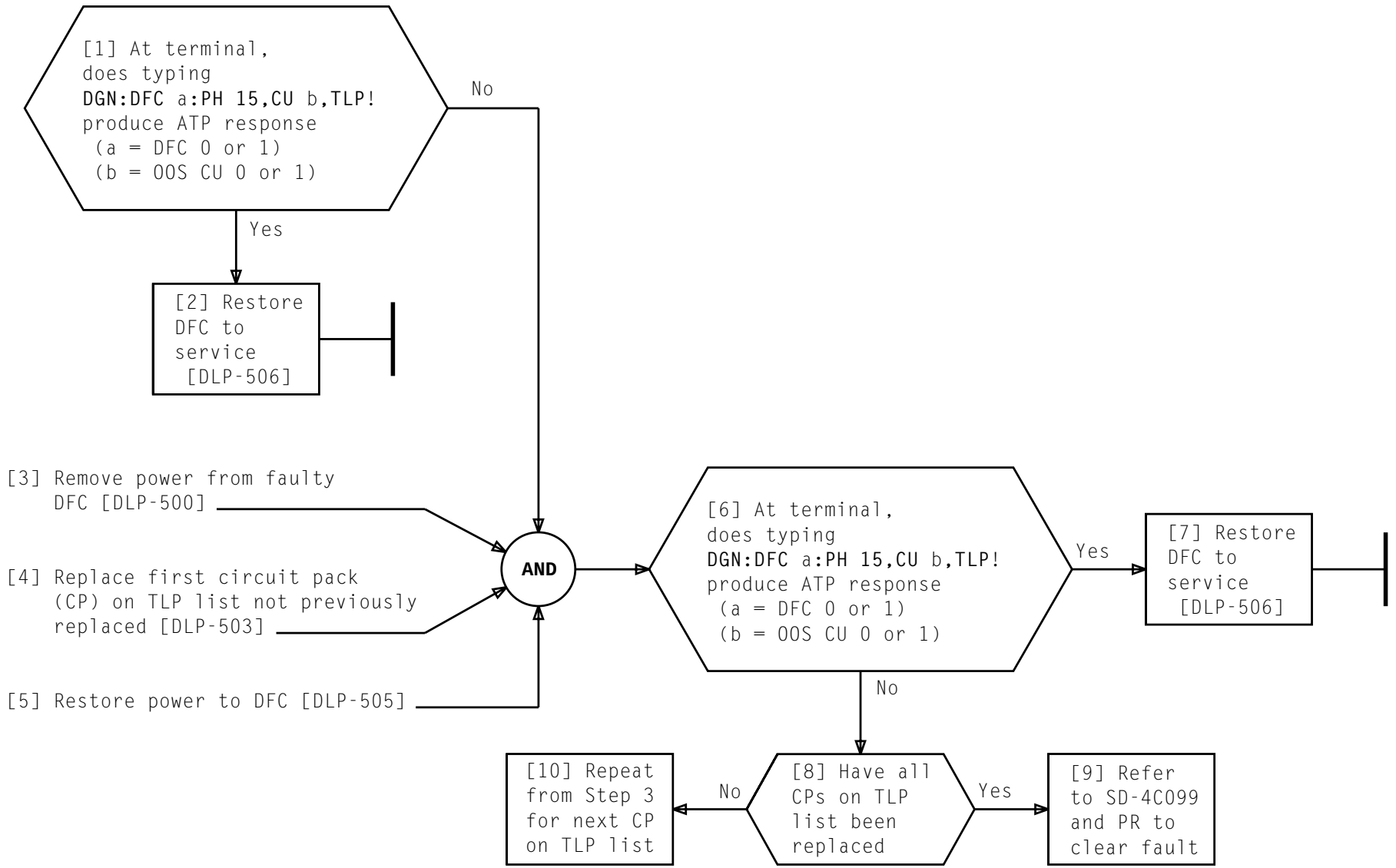
CLEAR COOLING UNIT FAILURE



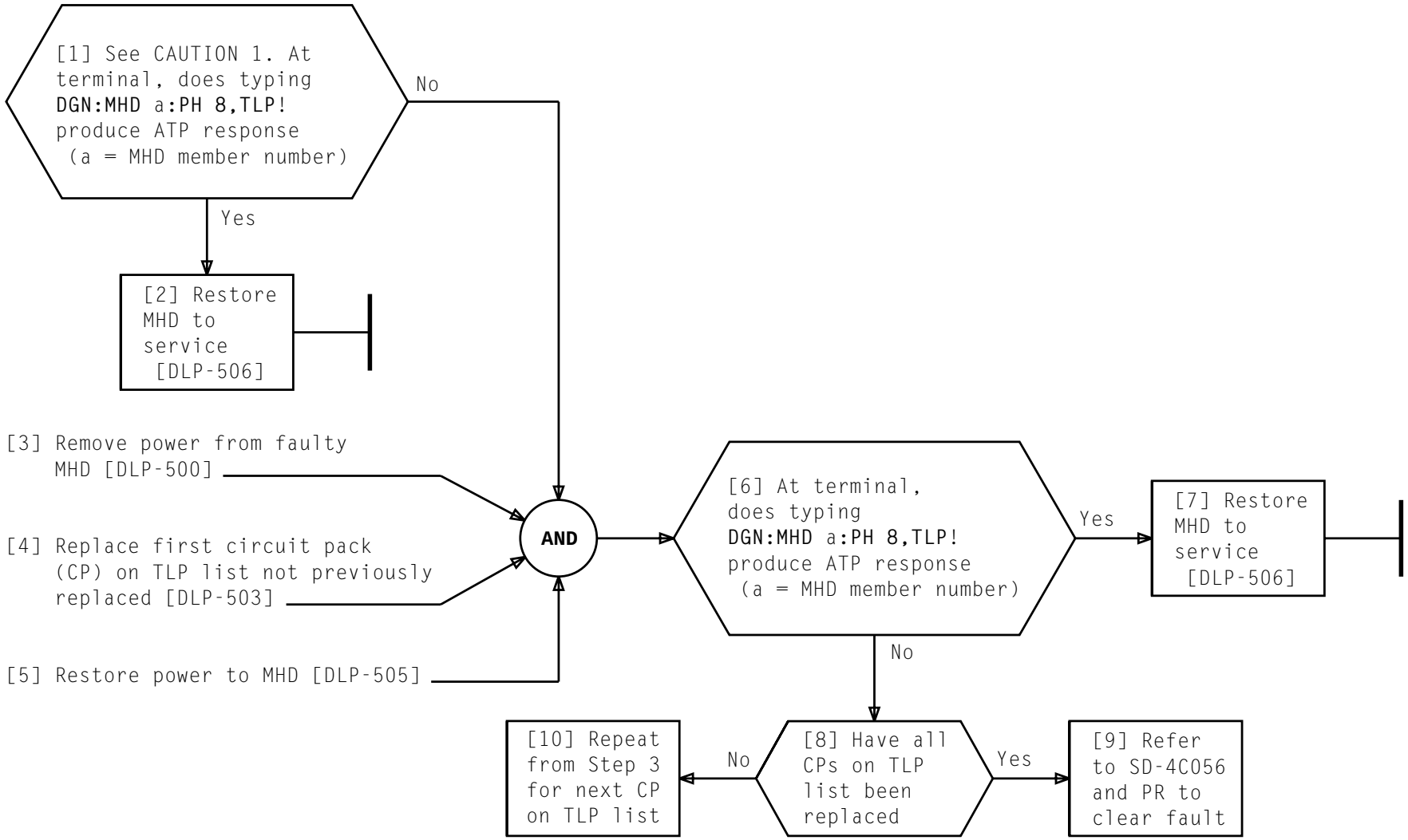
CLEAR CHANNEL (CH) DEMAND DIAGNOSTIC FAILURE USING TROUBLE LOCATING PROGRAM (TLP)



CLEAR MAIN STORE CONTROLLER (MASC) DEMAND DIAGNOSTIC FAILURE USING TROUBLE LOCATING PROGRAM (TLP)

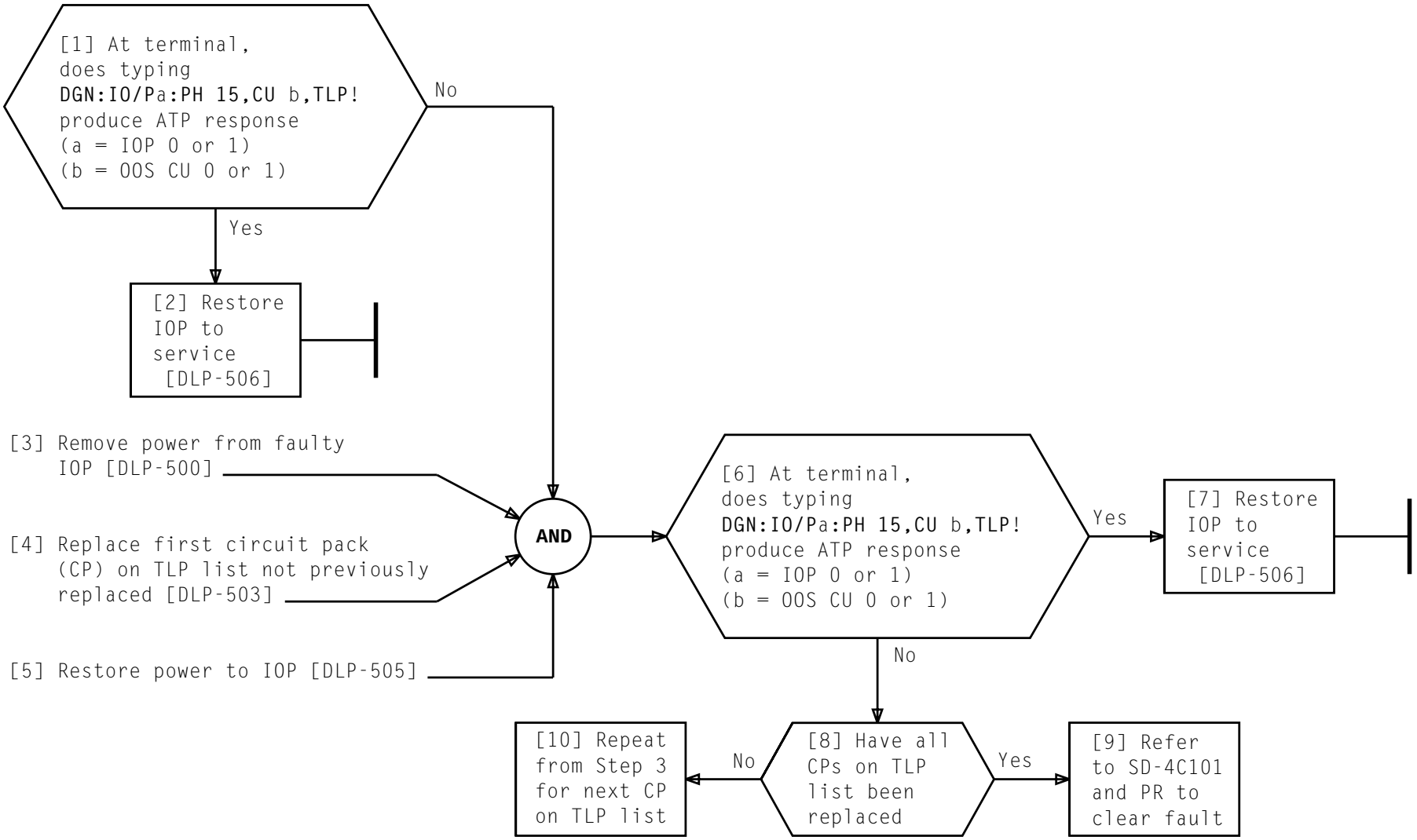


CLEAR DISK FILE CONTROLLER (DFC) DEMAND DIAGNOSTIC FAILURE USING TROUBLE LOCATING PROGRAM (TLP)

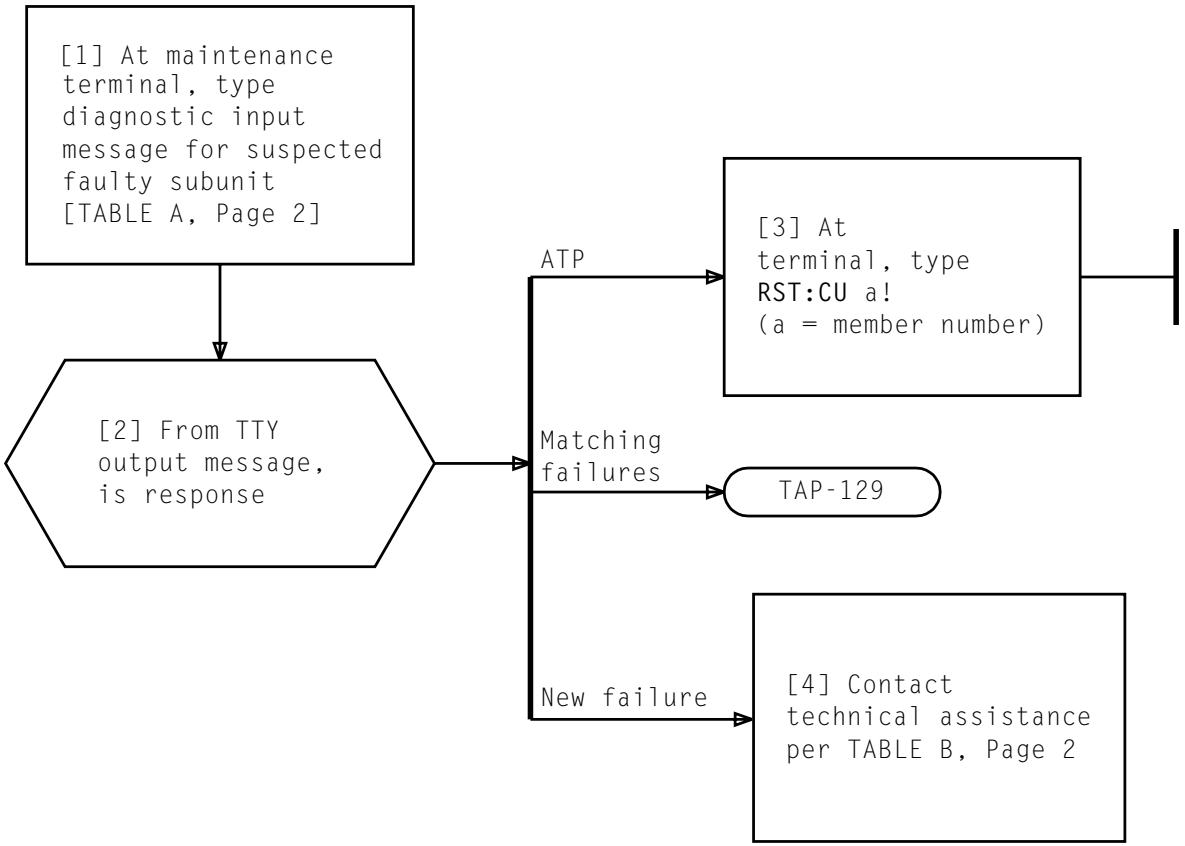


CAUTION 1
This phase destroys data stored on disk pack

CLEAR 300-MB MOVING HEAD DISK (MHD) DEMAND DIAGNOSTIC FAILURE USING TROUBLE LOCATING PROGRAM



CLEAR INPUT/OUTPUT PROCESSOR (IOP) DEMAND DIAGNOSTIC FAILURE USING TROUBLE LOCATING PROGRAM (TLP)

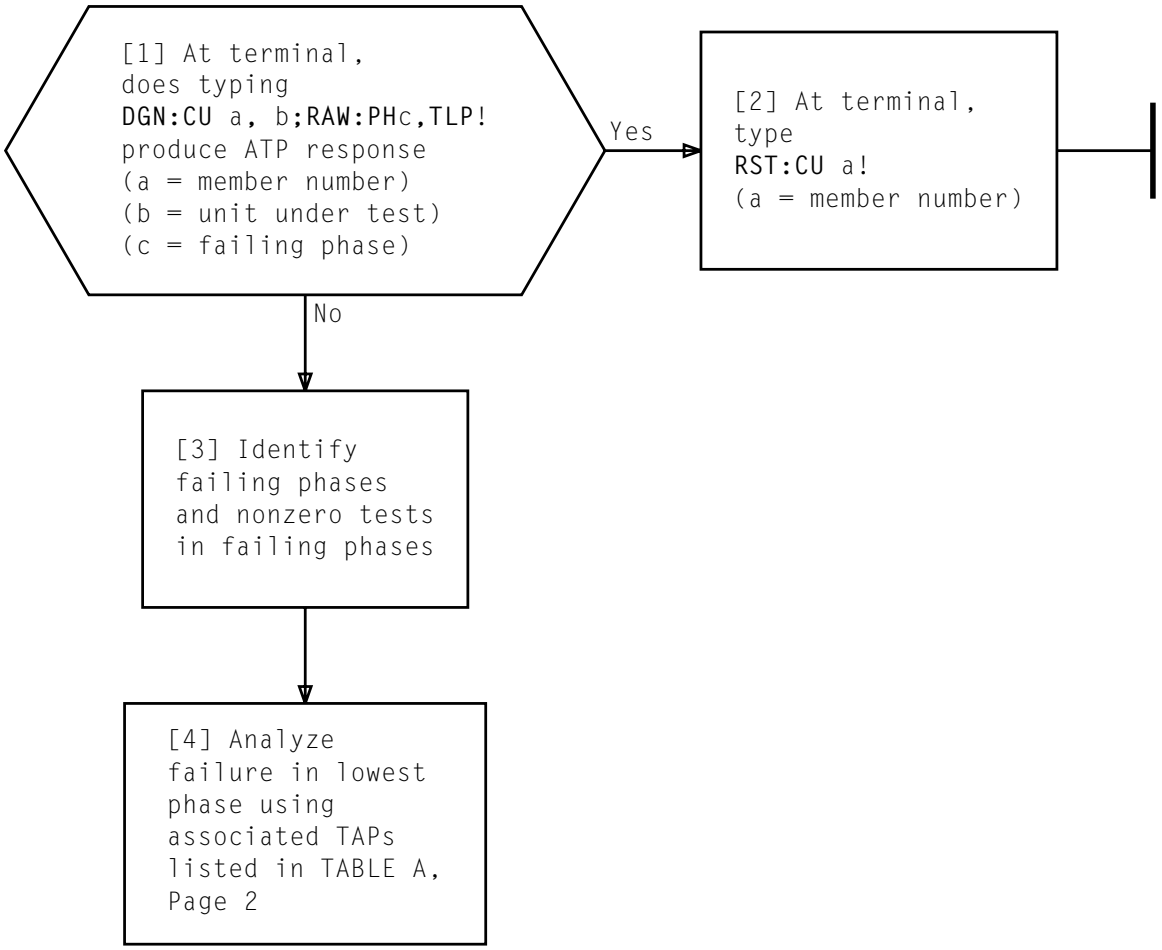


LOCALIZE CONTROL UNIT (CU) DIAGNOSTIC FAILURE USING DEMAND EXERCISE (DEX) OPTION

TABLE A	
SUBUNIT SUSPECTED FAULTY	**DIAGNOSTIC MESSAGE**
Central control (CC)	DGN:CUa,CCO;RPT5,DEX:PH1-95!
Mainstore controller including memory arrays (MASC)	DGN:CUa,MASCb;RPT5,DEX:PH1-95!
Store address translator (SAT)	DGN:CUa,SATo;RPT5,DEX:PH1-1O!
Cache store unit (CSU)	DGN:CUa,CSUo;RPT5,DEX:PH1-9O!
Utility circuit (UC)	DGN:CUa,UCO;RPT5,DEX:PH1-93!
Direct memory access controller (DMAC)	DGN:CUa,DMAb;RPT5,DEX:PH1-1O!
a = member number 0/1 b = unit number 0/1	

TABLE B	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

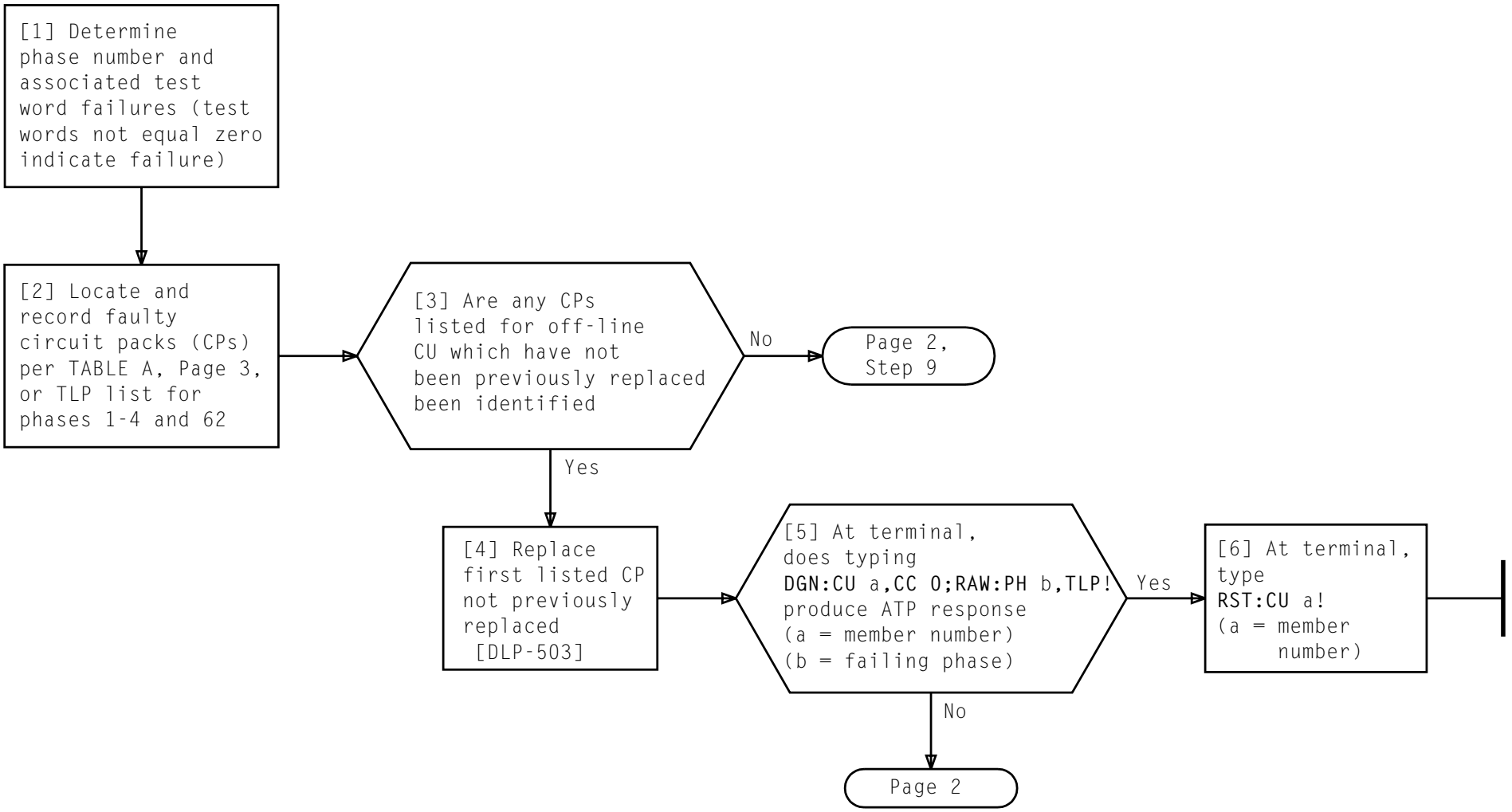
LOCALIZE CONTROL UNIT (CU) DIAGNOSTIC FAILURE USING DEMAND EXERCISE (DEX) OPTION



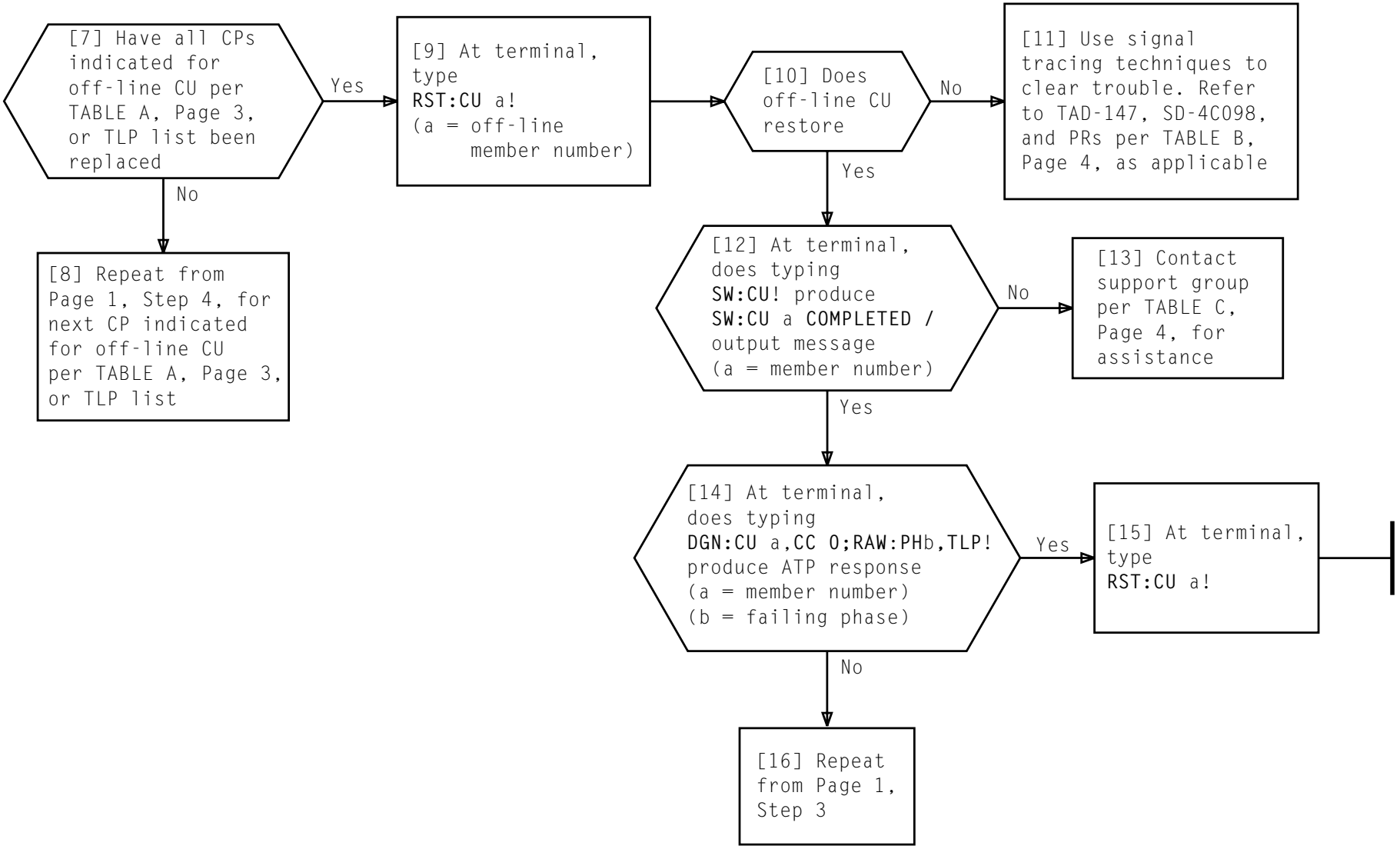
CLEAR CONTROL UNIT (CU) DIAGNOSTIC FAILURE USING RAW DATA OPTION

TABLE A			
PHASE	**CIRCUIT NAME**	**TAP**	**FS/SYM**
1-4, 62	Maintenance channel	TAP-130	FS 3/1
5-8, 10, 26-28	Microcontrol	TAP-131	FS 1/5
9, 70, 71	Microstore	TAP-132	FS 1/1, 3, 4
11, 12, 54-61	Special register (0/1)	TAP-133	FS 1/8, 9
13-22, 39, 52-54	Data manipulation units (0/1)	TAP-134	FS 1/6, 7
30-38, 83-88, 90-92	Writable microcode/microcontrol	TAP-135	FS 1/2, 3, 4
40-42, 46-49	Store address controller	TAP-136	FS 1/11
41, 43, 46-49	Store data control	TAP-137	FS 1/10
93	Emergency action interface	TAP-138	FS 6/1
1, 2, 4-41, 93, 95, 96	Main store controller	TAP-139	FS 10/1
1-10	Store address translator	TAP-140	FS 1/12
1-18, 90	Cache store unit	TAP-141	FS 1/13; 2/1, 2
1-18, 90, 93	Utility circuit	TAP-142	FS 4/2
1-3, 90	Dual serial channels	TAP-143	FS 3/1, 2, 3, 4
1-3	Application channels interface	TAP-144	FS 3/1, 2, 3, 4; 8/2, 3
1-10	Direct memory access controllers	TAP-145	FS 8/1
1-3, 8-40	DMAC dual serial channels	TAP-146	FS 8/2, 3

CLEAR CONTROL UNIT (CU) DIAGNOSTIC FAILURE USING RAW DATA OPTION



CLEAR CENTRAL CONTROL (CC) PHASES 1-4 AND 62 MAINTENANCE CHANNEL (MCH) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 1-4 AND 62 MAINTENANCE CHANNEL (MCH) FAILURES

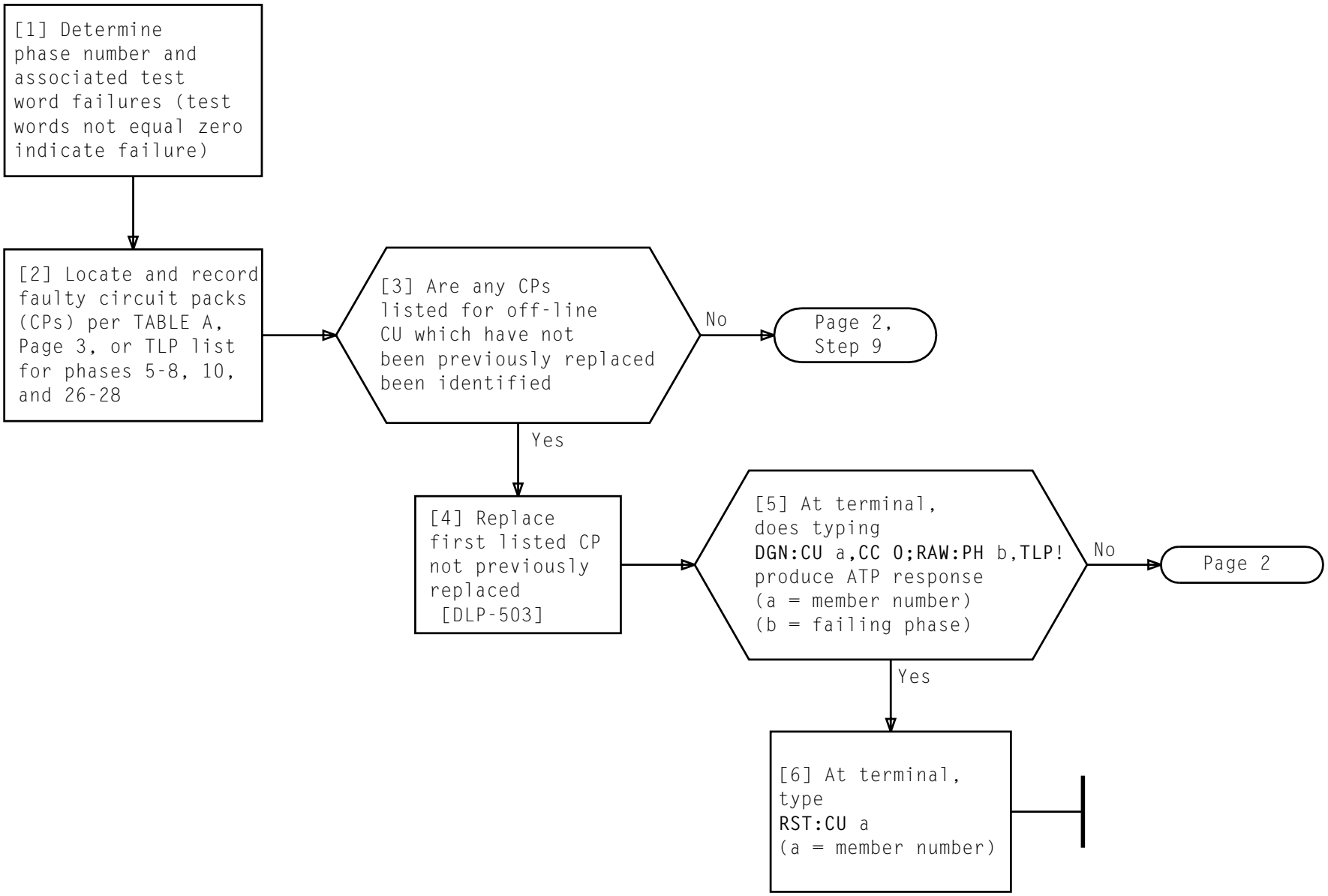
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, test 1	UN22C 56/60-028 (on-line); UN3B 56/60-092 (on-line)	Initialization
2-12	UN22C 56/60-028 (on-line); UN3B 56/60-092 (on-line); UN22C	On-line MCH buffer tests
13-17	UN22C 56/60-028 (on-line); UN3B 56/60-092 (on-line); UN22C	Initial on-line master MCH command execution tests
18-54	UN22C 56/60-028 (on-line); UN22C 56/60-028	On-line MCH buffer and shift register write and read tests
55-68	UN22C 56/60-028 (on-line); UN22C 56/60-028	Single shift on-line MCH shift register tests
Phase 1, test 69-82	UN22C 56/60-028 (on-line); UN22C 56/60-028	Invalid on-line master commands tests
Phase 2, test —		Initialization
1-10	UN22C 56/60-028; UN22C 56/60-028 (on-line); TN3 56/60-162	Test four valid start codes to slave MCH
11-51	UN22C 56/60-028; UN22C 56/60-028 (on-line)	Slave MCH buffer tests
Phase 2, test 52-103	UN22C 56/60-028; UN22C 56/60-028 (on-line)	Invalid start codes detected by slave tests
Phase 3, test 1-3	UN22C 56/60-028	Test initialization commands
4	UN22C 56/60-028; UN3B 56/60-092	Test initialization commands
5	UN22C 56/60-028	Test initialization commands
6-31	UN22C 56/60-028	Command parity, invalid commands, and clear status tests
32-35	UN22C 56/60-028; UN3B 56/60-092	Test CU stopped, start command, not stopped error, and stop command
36-52	UN22C 56/60-028; UN3B 56/60-092; UN2B 56/60-084; UN16B 56/60-020	Test CU stopped, start command, not stopped error, and stop command
Phase 3, test 53-100	UN22C 56/60-028	MCH micro-sequencer tests
Phase 62, test 1-3	UN22C 56/60-028; UN3B 56/60-092; UN21B 56/60-118; UN1C 56/60-072	Initialize and read status test
—	UN16B 56/60-028	—
4	UN22C 56/60-028; UN3B 56/60-092	Off-line CU to its MCH buffer tests
5-22	UN22C 56/60-028; UN3B 56/60-092; UN21B 56/60-118; UN1C 56/60-072	Off-line CU to its MCH buffer tests Clear panel interrupt in off-line MCH
23-26	UN22C 56/60-028; UN3B 56/60-092	Load master command and execute gating function tests
27-30	UN22C 56/60-028; UN3B 56/60-092; UN21B 56/60-118; UN1C 56/60-072	Off-line master commands tests
31-44	—	
Phase 62, test 45-47	UN22C 56/60-028	Off-line MCH initialize pulse point test

CLEAR CENTRAL CONTROL (CC) PHASES 1-4 AND 62 MAINTENANCE CHANNEL (MCH) FAILURES

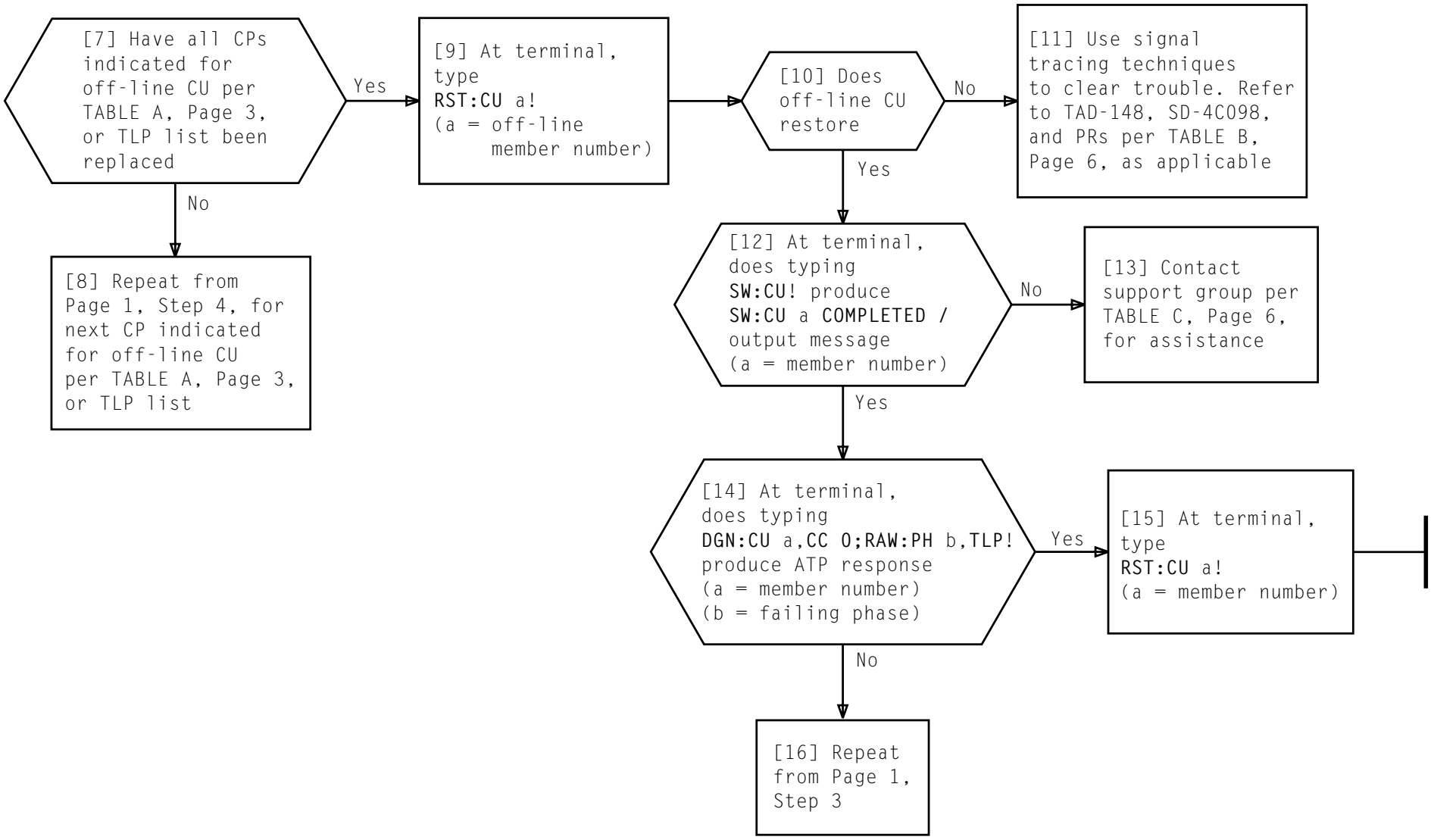
TABLE B	
PHASE NO.	**PR NO.**
1	4C27900
2	4C28000
3	4C28100
4	4C28200
62	4C33400

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASES 1-4 AND 62 MAINTENANCE CHANNEL (MCH) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCODE (MC) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCODE (MC) FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 4, test —	—	Initialization
↕ 1-32	UN22C 56/60-028	Microstore address bus (MSA) loop-around tests
Phase 4, test 33-135	UN22C 56/60-028	Microstore data bus load sequence and loop-around tests
Phase 5, test 1	UN22C 56/60-028	Clock circuit tests
↕ 2	UN135 56/60-066; UN2B 56/60-084; UN22C 56/60-028	Clock circuit tests
3	UN22C 56/60-028	Clock circuit tests
4-11	UN135 56/60-066; UN2B 56/60-084; UN22C 56/60-028	Clock circuit tests
12	UN135 56/60-066; UN2B 56/60-084; UN22C 56/60-028	MC parity
13-14	UN22C 56/60-028	MC parity
15-17	UN135 56/60-066; UN2B 56/60-084; UN22C 56/60-028	MC parity
18	UN22C 56/60-028	MC parity
Phase 5, test 19-46	UN135 56/60-066; UN2B 56/60-084; UN22C 56/60-028	MC parity
Phase 6, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	—
↕ 2	UN135 56/60-066; UN2B 56/60-084; UN3B 56/60-092; UN22C 56/60-028	Test bidirectional gating bus (BGB), processor destination bus (DST), and processor source bus (SRC) buses
3	UN22C 56/60-028	Test BGB, DST, and SRC buses
4	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN22C 56/60-028	Test BGB, DST, and SRC buses
5	UN22C 56/60-028	Test BGB, DST, and SRC buses
6	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN22C 56/60-028	Test BGB, DST, and SRC buses
7	UN22C 56/60-028	Test BGB, DST, and SRC buses
8-55	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN22C 56/60-028	Test BGB, DST, and SRC buses
56-71	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066 UN22C 56/60-028	Test of SRC and DST bus parity
Phase 6, test 72-113	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066 UN22C 56/60-028	Test of SRC and DST bus parity

CLEAR CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCODE (MC) FAILURES

TABLE A (Contd)

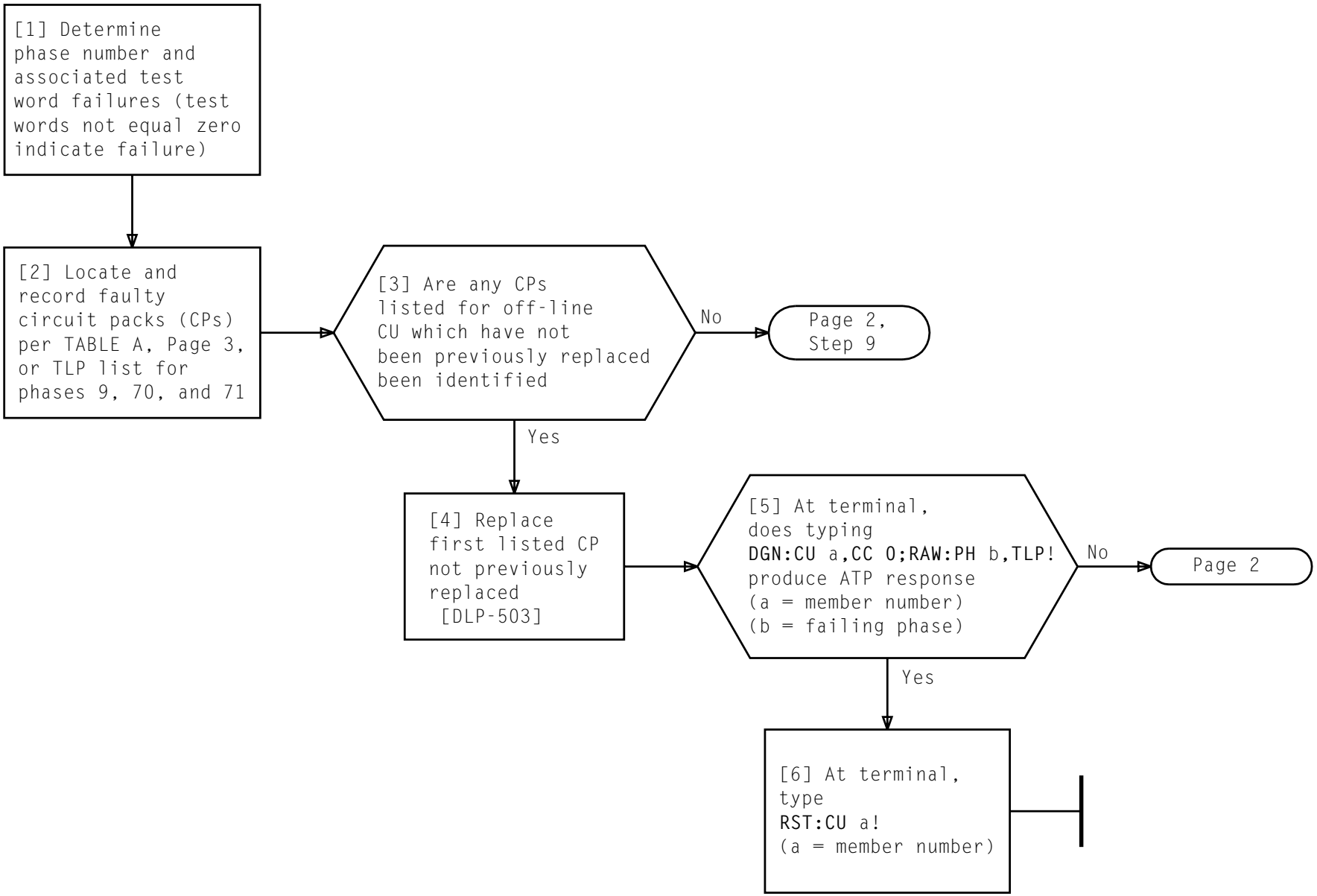
PHASE AND TEST FAILURE	SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER	COMMENTS
Phase 7, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	—
2-17	UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028; UN23C 56/60-078	Verify instruction register
18-49	UN1C 56/60-072; UN3B 56/60-092; UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Verify 'xmove' microinstruction
50-51	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN22C 56/60-028	Verify program status word (PSW) register
52	UN22C 56/60-028	Verify PSW register
53-82	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN22C 56/60-028	Verify PSW register
83-98	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Verify store instruction register (SIR)
99-103	UN1C 56/60-072; UN2B 56/60-084; UN135B 56/60-066; UN22C 56/60-028	Verify bits 3-0 of hardware status register (HSR)
104-106	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Verify bits 31 and 15 of store data register (SDR)
107-122	UN3B 56/60-092; UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Test path where MSA is determined from bits 15-8 of present memory address register (MAR) and from 'na' field of microinstruction register (MIR), bits 7-0
123-139	UN3B 56/60-092; UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Test JMP/CALL path through sequencer
Phase 7, test 140-156	UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028; UN23C 56/60-078	Test JMPX/CALLX instructions
Phase 8, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	—
2-17	UN1C 56/60-072; UN135 56/60-066; UN22C 56/60-028	Test JMPC microinstruction
18-33	UN1C 56/60-072; UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Test JMPC microinstruction
34-81	UN3B 56/60-092; UN135 56/60-066; UN6B 56/60-098	Test new marco opcode jam from half-word multiplexor
82-97	UN135 56/60-066; UN22C 56/60-028	Test multiplexor which drives 4-word stack
98-145	—	Test of 4-word stack
146-147	UN135 56/60-066; UN22C 56/60-028	Verify that a CALL is not executed when a JMP is requested
148-156	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN22C 56/60-028	Verify macro interrupt pending and sc=NEWOP will jam MSA to either 0x0003 or 0x0007
Phase 8, test 157-164	UN135 56/60-066	Verify that return address will come from MAR after a macro interrupt

CLEAR CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCODE (MC) FAILURES

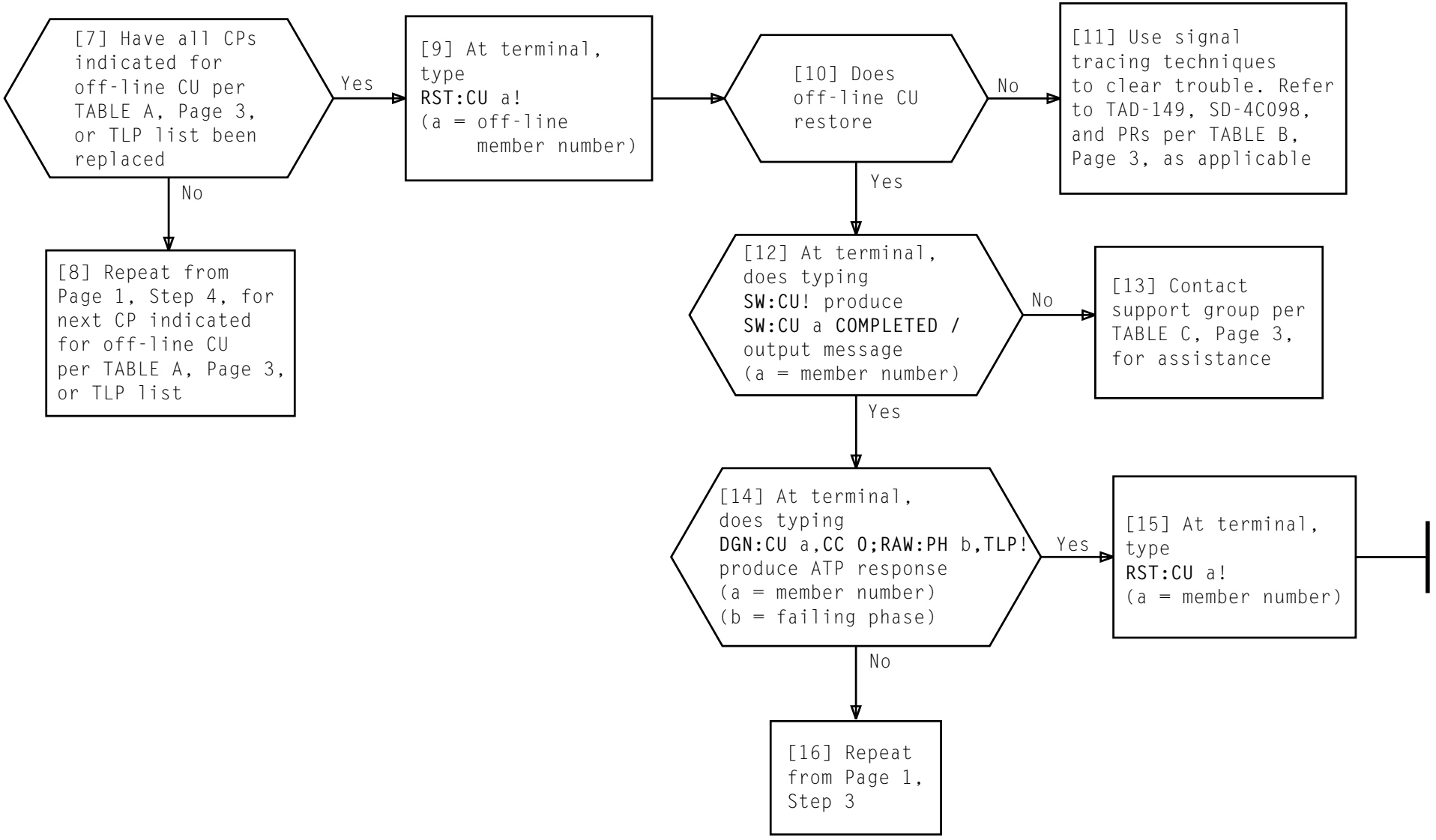
TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 10, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Test parity for JMPC, JMP, JMPX, CALL, and CALLX
2-11	UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028; UN23C 56/60-078	Test parity for JMPC, JMP, JMPX, CALL, and CALLX
Phase 10, test 12-21	UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028; UN23C 56/60-078	Verify parity for new macro opcode jam
22-38	UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028; UN23C 56/60-078	Verify parity of 4-word stack
39-54	UN135 56/60-066; UN22C 56/60-028; UN23C 56/60-078	Verify parity when using PSW and HSR for JMPCs
55-70	UN135 56/60-066; UN6B 56/60-098; UN22C 56/60-028	Verify parity when using instruction buffer (IB) and store data register (SDR) for JMPCs
Phase 10, test 71-72	UN135 56/60-066; UN22C 56/60-028	Verify parity for macro interrupt (MSA = 0x0003 or 0x0007)
Phase 26, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	—
Phase 26, test 2-431	UN3B 56/60-092; UN135 56/60-066	—
Phase 27, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	—
Phase 27, test 2-431	UN3B 56/60-092; UN135 56/60-066	—
Phase 28, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	—
Phase 28, test 2-431	UN3B 56/60-092; UN135 56/60-066	—

TABLE B	
PHASE NO.	**PR NO.**
5	4C28300
6	4C28400
7	4C28500
8	4C28600
10	4C28800
26	4C30100
27	4C30200
28	4C30300

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs



CLEAR CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES



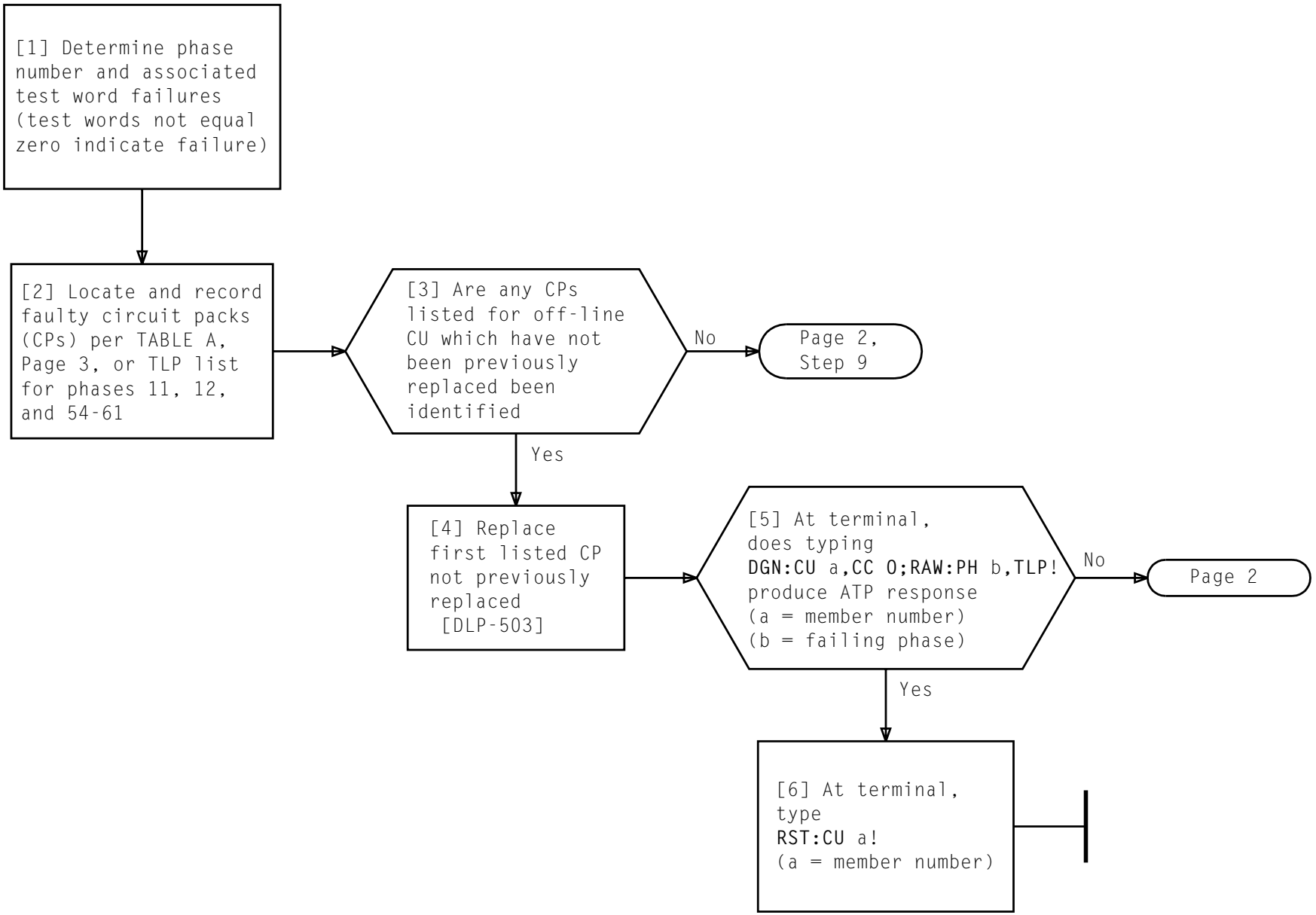
CLEAR CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CP AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 9, test 1	—	
↕ 2-9	UN22C 56/60-028; UN28B 56/60-036; UN135 56/60-066	Verify contents of read-only memory (ROM) in this slot
Phase 9, test 10-45	UN22C 56/60-028; UN28B 56/60-036; UN135 56/60-066	Verify contents of ROM in this slot
Phase 70, test 1	—	—
↕ 2-9	UN22C 56/60-028; UN28B 56/60-050; UN135 56/60-066	Verify contents of ROM in this slot
Phase 70, test 10-45	UN22C 56/60-028; UN28B 56/60-036; UN135 56/60-066	Verify contents of ROM in this slot
Phase 71, test 1	—	—
↕ 2-9	UN22C 56/60-028; UN28B 56/60-058; UN135 56/60-066	Verify contents of ROM in this slot
Phase 71 test 10-45	UN22C 56/60-028; UN28B 56/60-036; UN135 56/60-066	Verify contents of ROM in this slot

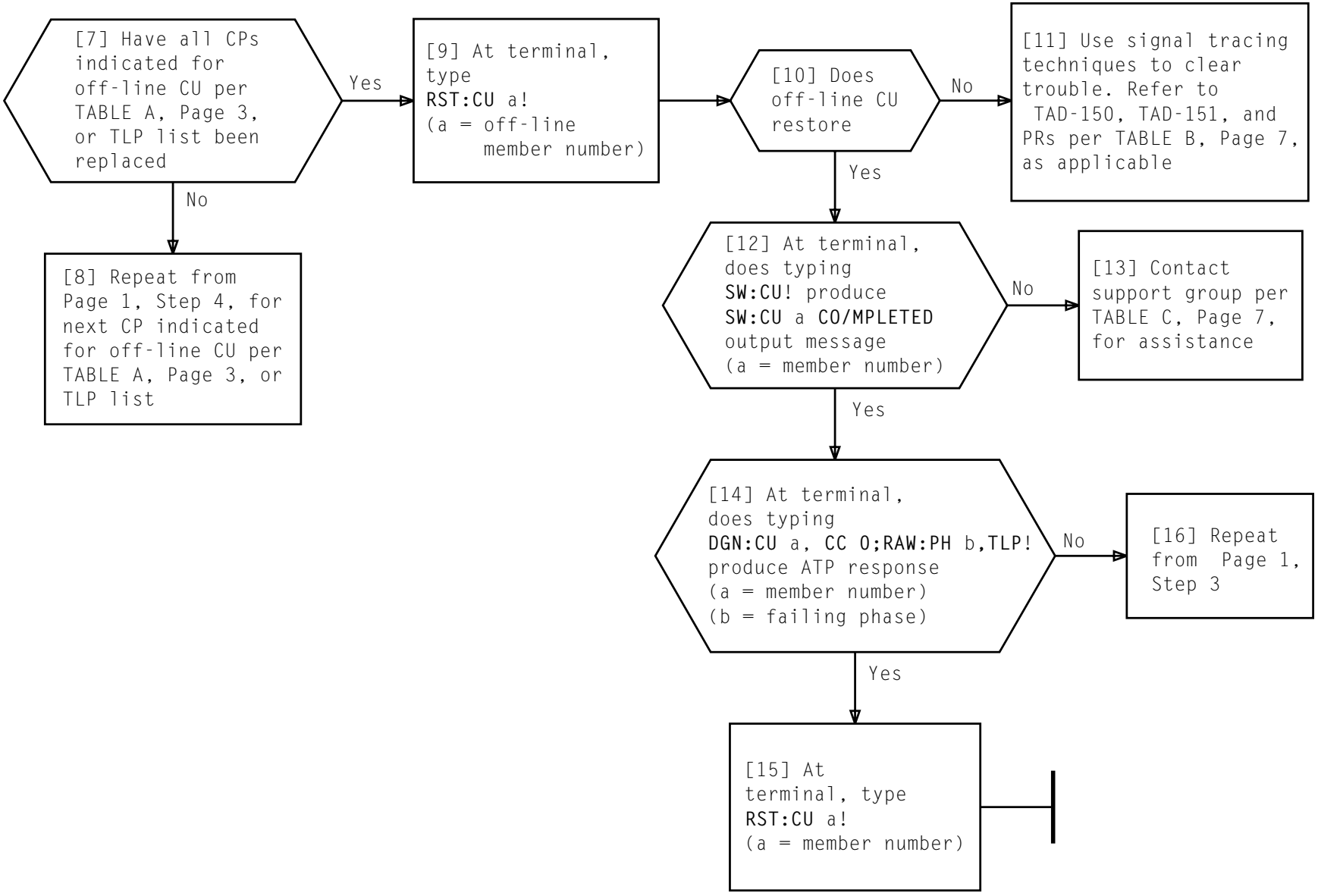
TABLE B	
PHASE NO.	**PR NO.**
9	4C28700
70	4C33500
71	4C33600

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 OR 1 FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 OR 1 FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 11, test 1	—	—
2-51	UN2B 56/60-084; UN3B 56/60-092	Test of program status word (PSW)
52	UN2B 56/60-084; UN3B 56/60-092	Test of hardware status register (HSR)
53-54	UN2B 56/60-084; UN3B 56/60-092; UN22C 56/60-028	Test of HSR
55-92	UN2B 56/60-084; UN3B 56/60-092	Test of HSR
93-94	UN2B 56/60-084; UN3B 56/60-092	Test of system status register (SSR)
95	UN22C 56/60-028	Test of SSR
96-103	UN2B 56/60-084; UN3B 56/60-092	Test of SSR
104-108	UN3B 56/60-092	Test of SSR
Phase 11, test 109-120	UN2B 56/60-084	Test of SSR
Phase 12, test 1	—	—
2-9	UN2B 56/60-084; UN3B 56/60-092	Test of pulse point register (PPR)
10	UN2B 56/60-084; UN2B 56/60-084 (on-line); UN133 56/60-146 UN133 56/60-146 (on-line)	Test of PPR
11-22	UN2B 56/60-084; UN3B 56/60-092	Test of PPR
23	UN2B 56/60-084; UN2B 56/60-084 (on-line); UN133 56/60-146 UN133 56/60-146 (on-line)	Test of PPR
24-35	UN2B 56/60-084; UN3B 56/60-092	Test of PPR
36	UN2B 56/60-084; UN2B 56/60-084 (on-line); UN133 56/60-146 UN133 56/60-146 (on-line)	Test of PPR
37-42	UN3B 56/60-092	Test of input/output disable
43-46	UN3B 56/60-092; UN22C 56/60-028	Test of input/output disable
47-67	UN2B 56/60-084; UN22C 56/60-028	Test of error indicator for invalid maintenance channel (MCH) order
68-71	UN2B 56/60-084	Test of error indicator for invalid MCH order
Phase 12, test 72-75	UN2B 56/60-084; UN3B 56/60-092; UN22C 56/60-028	Test of panel interrupt
Phase 54, test 1-115	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092 UN23C 56/60-078	Find low zero logic bit

CLEAR CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 OR 1 FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 55, test 1	—	—
2-33	—	Test of interrupt mask register
34-99	—	Test of interrupt source register
Phase 55, test 100-173	UN2B 56/60-084; UN3B 56/60-092	Test of interrupt logic
Phase 56, test 1	—	—
2-21	UN2B 56/60-084; UN3B 56/60-092	Interrupt timer and pretimer, sanity timer, and real-time counter pretimer
22-23	UN2B 56/60-084; UN22C 56/60-028	Interrupt timer and pretimer, sanity timer, and real-time counter pretimer
24-39	—	Test of real-time counter access
40-73	—	Test of real-time counter options
74-80	—	Test of timer chain and backup timer
Phase 56, test 81-94	UN2B 56/60-084; UN3B 56/60-092	Test of timed interrupt
Phase 57, test 1	—	—
Phase 57, test 2-33	UN2B 56/60-084; UN3B 56/60-092	Test of channel data register (CDR)
Phase 58, test 1-4	UN3B 56/60-092	Error register (ER) bits 16-19 and HSR bit 6 initial tests
5-8	UN3B 56/60-092; UN2B 56/60-084	ER bits 16-19 and HSR bit 6 initial tests
9-14	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092	ER bits 16-19 and HSR bit 6 initial tests
15	UN2B 56/60-084; UN3B 56/60-092	Response leads inactive, 1/11 checker error, and ER bit 18 tests
16-21	UN3B 56/60-092; UN2B 56/60-084; UN22C 56/60-028	Response leads inactive, 1/11 checker error, and ER bit 18 tests
22-23	UN2B 56/60-084; UN3B 56/60-092	Response leads inactive, 1/11 checker error, and ER bit 18 tests
24	UN3B 56/60-092	Response leads inactive, 1/11 checker error, and ER bit 18 tests
25-26	UN2B 56/60-084; UN3B 56/60-092	Response leads inactive, 1/11 checker error, and ER bit 18 tests
Phase 58, test 27-28	UN3B 56/60-092; UN2B 56/60-084	Response leads inactive, 1/11 checker error, and ER bit 18 tests

CLEAR CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 OR 1 FAILURES

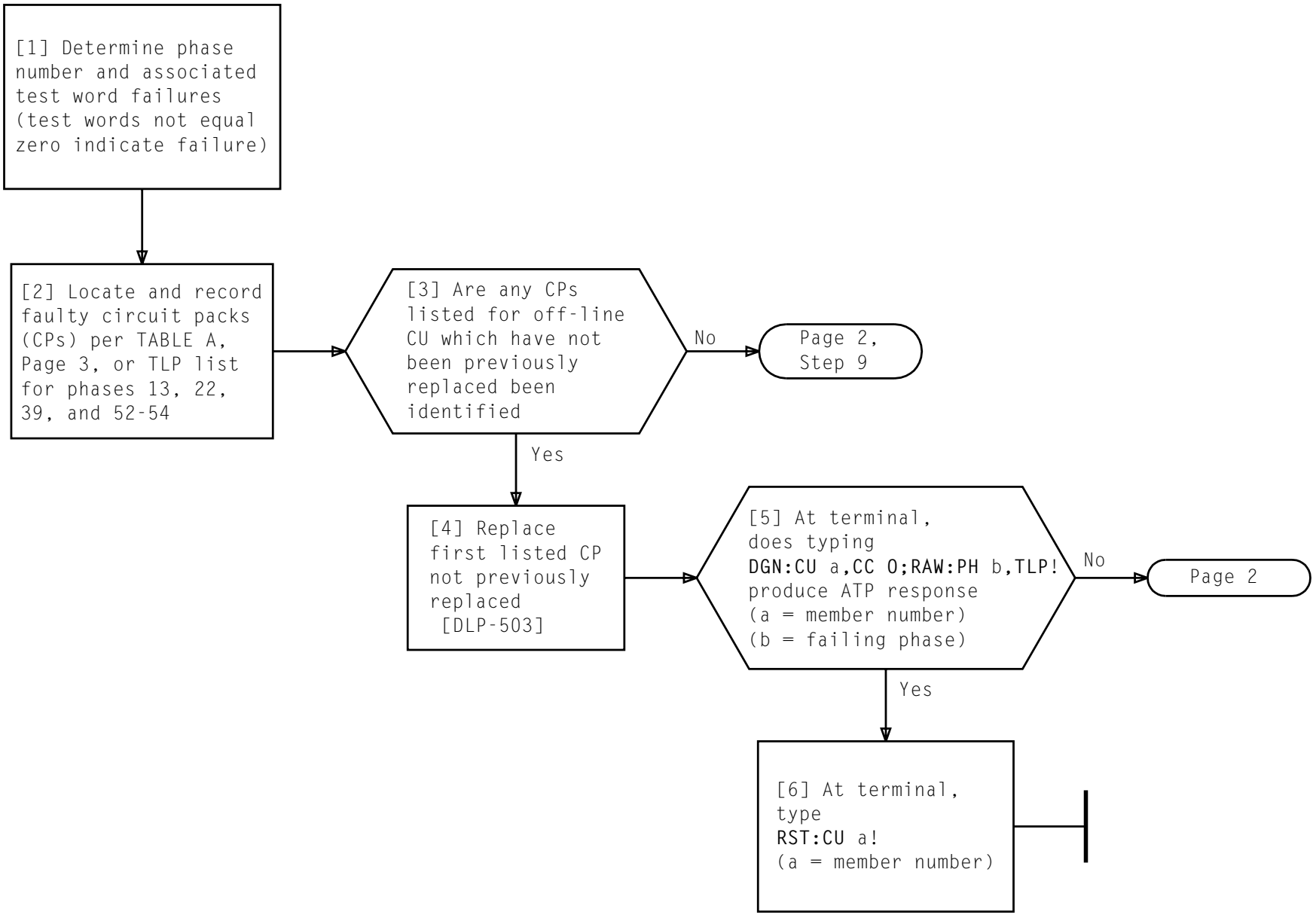
TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 58, test 29-32	UN2B 56/60-084; UN22C 56/60-028	1/11 checker on command leads and ER bit 17 tests
33	UN2B 56/60-084; UN3B 56/60-092	1/11 checker on command leads and ER bit 17 tests
34-35	UN3B 56/60-092; UN2B 56/60-084; UN22C 56/60-028	1/11 checker on command leads and ER bit 17 tests
36	UN2B 56/60-084; UN3B 56/60-092	1/11 checker on command leads and ER bit 17 tests
37	UN3B 56/60-092	1/11 checker on command leads and ER bit 17 tests
38	UN2B 56/60-084; UN3B 56/60-092	1/11 checker on command leads and ER bit 17 tests
39-42	UN3B 56/60-092; UN22C 56/60-028	1/11 checker on command leads and ER bit 17 tests
43-50	UN2B 56/60-084; UN3B 56/60-092	1/11 checker on command leads and ER bit 17 tests
51-52	UN3B 56/60-092	Acknowledge (ACK) state to ER bits 17 and 16 tests
Phase 58, test 53-67	UN2B 56/60-084	Verify no ACK to 2/6 codes
Phase 59, test 1	—	—
2-63	—	Test of invalid MCH order source for other CC hardware error interrupt
Phase 59, test 64-73	UN2B 56/60-084; UN3B 56/60-092	Test of invalid MCH order source for other CC hardware error interrupt
Phase 60, test 1-34	UN2B 56/60-084; UN135 56/60-066	Stop and switch test
35-38	UN2B 56/60-084; UN22C 56/60-028; UN22C 56/60-028 (on-line)	Stop and switch test
39-47	UN2B 56/60-084; UN3B 56/60-092	Sanity timer test
48-58	UN2B 56/60-084	Sanity timer test
59	UN2B 56/60-084	Error interrupt tests
Phase 60, test 60-73	UN2B 56/60-084; UN3B 56/60-092	Error interrupt tests

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 60, test 74-78	UN3B 56/60-092; UN2B 56/60-084 (on-line); UN133 56/60-146; UN133 56/60-146 (on-line)	Backup MCH tests
Phase 60, test 79-82	UN3B 56/60-092	Backup MCH tests
Phase 61, test —	—	Processor recovery message flushing
1-2	—	Pulse point interrupts
3-5	UN2B 56/60-084; TN10 56/60-154	Initialization parameter buffer
6-10	—	CC status indicator tests
11-26	TN983 29/33-102	Processor recovery message
27-38	UN2B 56/60-084; TN10 56/60-154	CC forces
39-43	UN2B 56/60-084; UN22C 56/60-028; UN22C 56/60-028 (on-line); UN133 56/60-146; UN133 56/60-146 (on-line)	CC forces
44-47	UN2B 56/60-084	CC forces
48-51	UN3B 56/60-092	CC forces
52-54	UN2B 56/60-084	CC forces
55-69	UN2B 56/60-084; TN10 56/60-154	CC forces
70-71	TN10 56/60-154	Maintenance mode clear
Phase 61, test 72-74	TN10 56/60-154	Self-tests

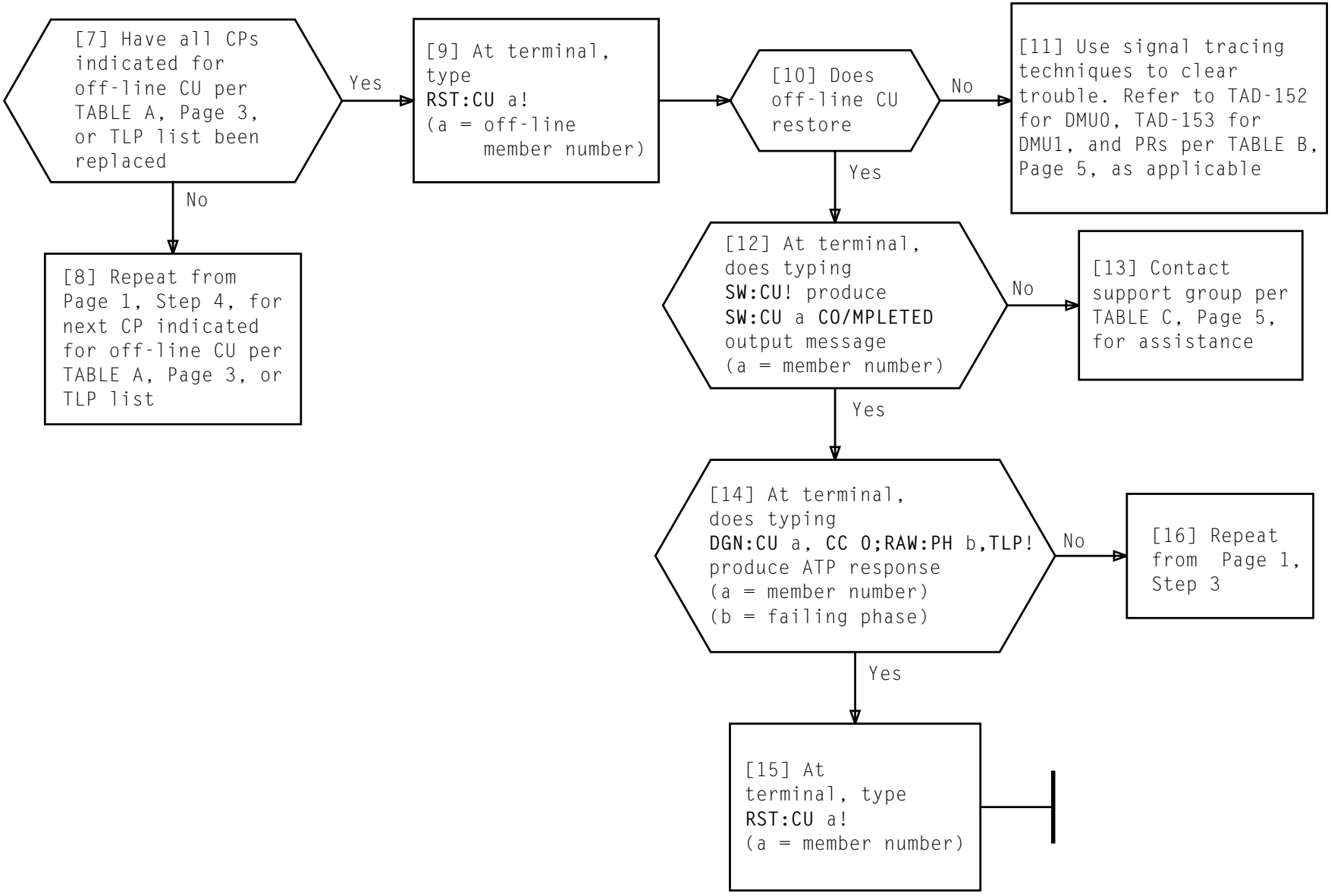
TABLE B	
PHASE NO.	**PR NO.**
11	4C28900
12	4C29000
54	4C32600
55	4C32700
56	4C32800
57	4C32900
58	4C33000
59	4C33100
60	4C33200
61	4C33300

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 OR 1 FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 13-22, 39, AND 52-54 DATA MANIPULATION UNIT (DMU) 0 OR 1 FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 13-22, 39, AND 52-54 DATA MANIPULATION UNIT (DMU) 0 OR 1 FAILURES

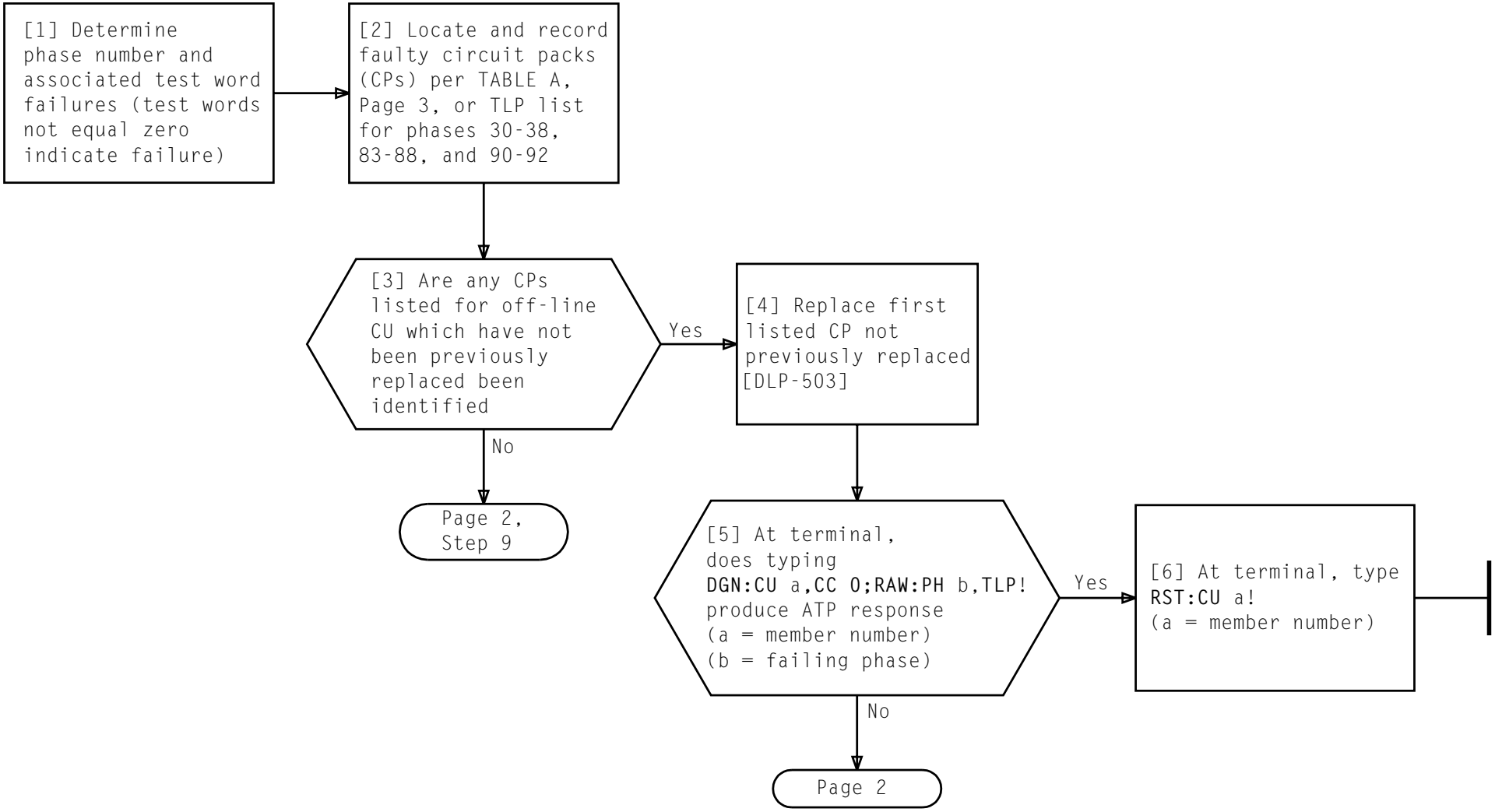
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 13, tests 1-17	UN1C 56/60-072; UN6B 56/60-098; UN23C 56/60-078	Gate through and byte rotator tests
Phase 14, tests 1-47	UN1C 56/60-072; UN6B 56/60-098; UN23C 56/60-078	Bit rotator test
Phase 15, tests 1-12	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092	Test of arithmetic logic unit (ALU) matcher
13	UN1C 56/60-072; UN2B 56/60-084	Test of ALU matcher
Phase 15, tests 14-140	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092 UN23C 56/60-078	Test of ALU matcher
Phase 16, tests 1-19	UN1C 56/60-072; UN23C 56/60-078	Q register test
Phase 17, tests 1-193	UN1C 56/60-072; UN2B 56/60-084; UN23C 56/60-078	Z flag test
194-202	UN1C 56/60-072; UN23C 56/60-078	Z flag test
Phase 17, tests 203-205	UN2B 56/60-084; UN3B 56/60-092	Z flag test
Phase 18, tests 1-86	UN1C 56/60-072; UN23C 56/60-078	Generator register tests
Phase 19, tests 1-460	UN1C 56/60-072; UN23C 56/60-078	ALU functions and gating paths and look-ahead-carry logic tests
Phase 20, tests 1-148 Phase 20, tests 149-227	UN1C 56/60-072; UN23C 56/60-078	Test of homogeneity circuit
Phase 21, tests 1-20	UN1C 56/60-072; UN23C 56/60-078	ALU loop-around test
Phase 22, tests 1-99	——	Temporary register test
100-197	——	Firm register test
198-200	——	Input from buffered/bidirectional gating register (BGR) to source multiplexor test
Phase 22, tests 201-210	UN1C 56/60-072; UN23C 56/60-078	Indirect firm/temporary register access
Phase 39, tests 1-9	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092	Test of source bus parity checker

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 39, tests 10-33	———	Test of source bus parity checker
34-49	———	Test of parity rotator
50-63	UN1C 56/60-072; UN3B 56/60-092	Test of bit rotator parity checker
Phase 39, tests 64-82	UN1C 56/60-072; UN43C 56/60-104	Test of destination bus parity generator
Phase 52, tests 1-29		"A" indirect select multiplexor test
30-56	UN1C 56/60-072; UN6B 56/60-098; UN23C 56/60-078	"A" indirect select multiplexor test
Phase 52, tests 57-88	UN1C 56-60-072; UN6B 56/60-098	Indirect rotator amount multiplexor test
Phase 53, tests 1-3	———	Mask read-only memory (ROM) test
Phase 53, tests 4-86	UN1C 56/60-072; UN6B 56/60-098; UN23C 56/60-078	Mask logic test
Phase 54, tests 1-115	UN1C 56/60-072; UN2B 56/60-084; UN3B 56/60-092 UN23C 56/60-078	Find low zero logic bit

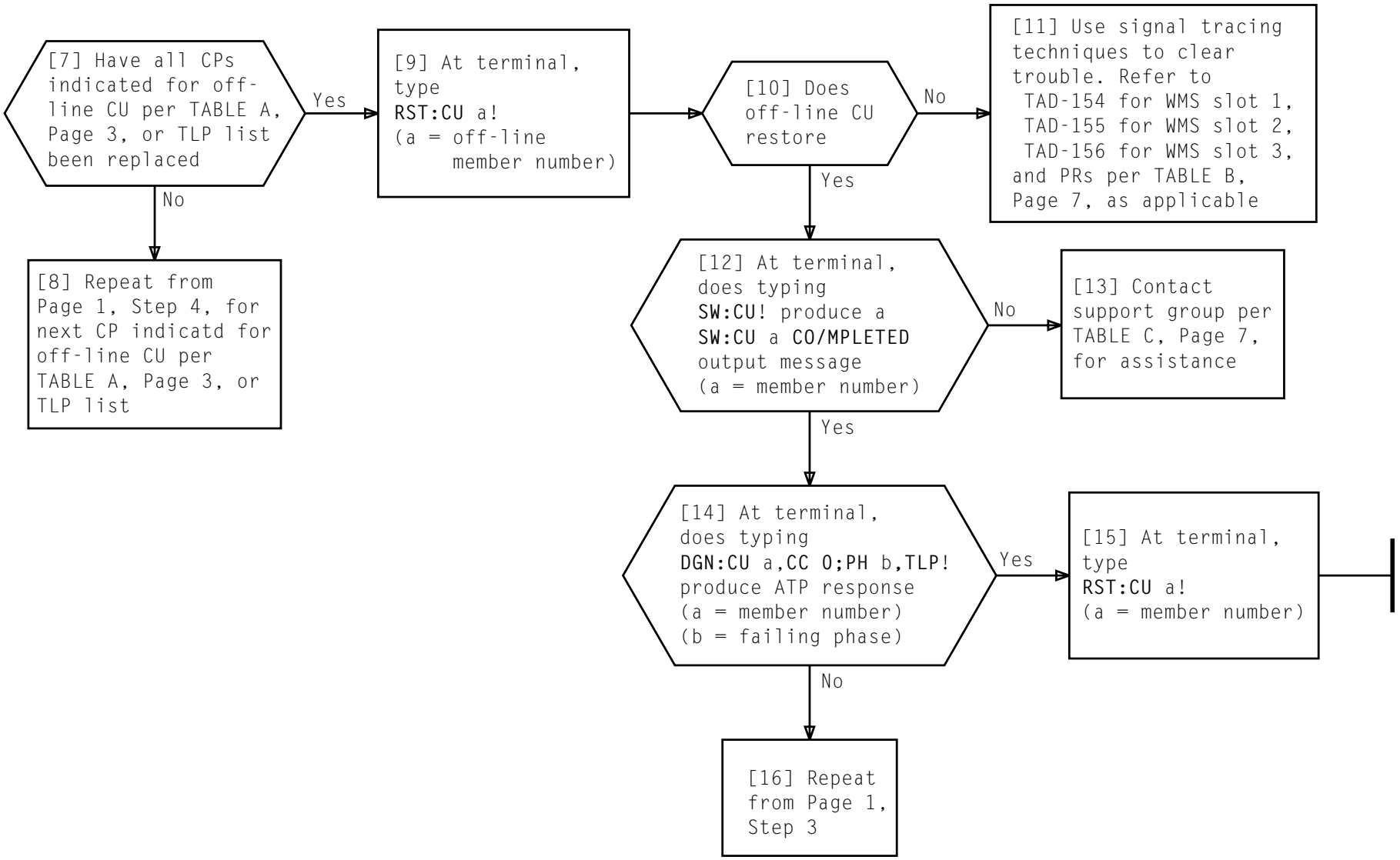
TABLE B	
PHASE NO.	**PR NO.**
13	4C29100
14	4C29200
15	4C29300
16	4C29400
17	4C29500
18	4C29600
19	4C29700
20	4C29800
21	4C29900
22	4C30000
39	4C31300
52	4C32400
53	4C32500
54	4C32600

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASES 13-22, 39, AND 52-54 DATA MANIPULATION UNIT (DMU) 0 OR 1 FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 30-38, 83-88, AND 90-92 WRITABLE MICROSTORE (WMS) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 30-38, 83-88, AND 90-92 WRITABLE MICROSTORE (WMS) FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 30, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify bidirectional gating bus (BGB) and microstore data bus (MSD) access to the WMS
↕ tests 2-37	UN48B 56/60-042	
Phase 30, test 38-109	UN48B 56/60-042	Verify BGB and MSD access to the WMS
Phase 31, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify bit 35 of BGB when reading WMS
↕ ↕ 2-10		Verify bit 35 of BGB when reading WMS
11-14		Verify 2 test location
15-18	UN48B 56/60-042	Test enabling of WMS
19	UN48B 56/60-042	Test illegal addresses on BGB
Phase 31, test 20-30	UN48B 56/60-042	Test illegal addresses on miscrostore (MS) address
Phase 32, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify BGB and MSD access to the WMS
↕ tests 2-109	UN48B 56/60-042	
Phase 32,		
Phase 33, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify BGB and MSD access to the WMS
↕ tests 2-109	UN48B 56/60-050	
Phase 33,		
Phase 34, tests 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify bit 35 of BGB when reading WMS
↕ ↕ 2-10		Verify bit 35 of BGB when reading WMS
11-14		Verify 2 test location
15-18	UN48B 56/60-050	Test enabling of WMS
19	UN48B 56/60-050	Test illegal addresses on BGB
Phase 34, tests 20-30	UN48B 56/60-050	Test illegal addresses on MS address

CLEAR CENTRAL CONTROL (CC) PHASES 30-38, 83-88, AND 90-92 WRITABLE MICROSTORE (WMS) FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 35, test 1	UN2B 56/60-084	Verify bit 35 of BGB when reading WMS
tests 2-10		Verify bit 35 of BGB when reading WMS
11-14		Verify 2 test location
15-18	UN48B 56/60-042	Test enabling of WMS
test 19	UN48B 56/60-042	Test illegal addresses on BGB
Phase 35, tests 20-30	UN48B 56/60-042	Test illegal addresses on MS address
Phase 36, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify BGB and MSD access to the WMS
tests 2-109		
Phase 36	UN48B 56/60-058	
Phase 37, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify bit 35 of BGB when reading WMS
2-10		Verify bit 35 of BGB when reading WMS
11-14		Verify 2 test location
15-18	UN48B 56/60-058	Test enabling of WMS
test 19	UN48B 56/60-058	Test illegal addresses on BGB
Phase 37, tests 20-30	UN48B 56/60-058	Test illegal addresses on MS address
Phase 38, tests 1-17	UN48B 56/60-042	
tests 18-24	UN48B 56/60-042	
35-51	UN48B 56/60-042	
52-68	UN48B 56/60-042	
69	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Addressing lead test
test 70-93	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Addressing lead test
Phase 38, tests 94-117	UN135 56/60-066; UN48B 56/60-042; UN22C 56/60-028; UN28B 56/60-036	MSD invalid signal
Phase 83, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify BGB and MSD access to the WMS
tests 2-109	UN48B 56/60-050	
Phase 83,		

CLEAR CENTRAL CONTROL (CC) PHASES 30-38, 83-88, AND 90-92 WRITABLE MICROSTORE (WMS) FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 84, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify bit 35 of BGB when reading WMS
2-10		Verify bit 35 of BGB when reading WMS
11-14		Verify 2 test location
15-18	UN48B 56/60-050	Test enabling of WMS
19	UN48B 56/60-050	Test illegal addresses on BGB
Phase 84, tests 20-30	UN48B 56/60-050	Test illegal addresses on MS address
Phase 85, tests 1-17	UN48B 56/60-050	
18-34	UN48B 56/60-050	
35-51	UN48B 56/60-050	
52-68	UN48B 56/60-050	
69-93	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Addressing lead test
Phase 85, tests 94-120	UN135 56/60-066; UN48B 56/60-050; UN22C 56/60-028; UN28B 56/60-058	MSD invalid signal
Phase 86, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	
tests 2-109	UN48B 56/60-058	Verify BGB and MSD access to the WMS
Phase 86,		
Phase 87, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Verify bit 35 of BGB when reading WMS
2-10		Verify bit 35 of BGB when reading WMS
11-14		Verify 2 test location
15-18	UN48B 56/60-058	Test enabling of WMS
19	UN48B 56/60-058	Test illegal addresses on BGB
Phase 87, tests 20-30	UN48B 56/60-058	Test illegal addresses on MS address
Phase 88, tests 1-68	UN48B 56/60-058	—
69-93	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	
Phase 88, tests 94-117	UN135 56/60-066; UN48B 56/60-042; UN22C 56/60-028; UN28B 56/60-036	

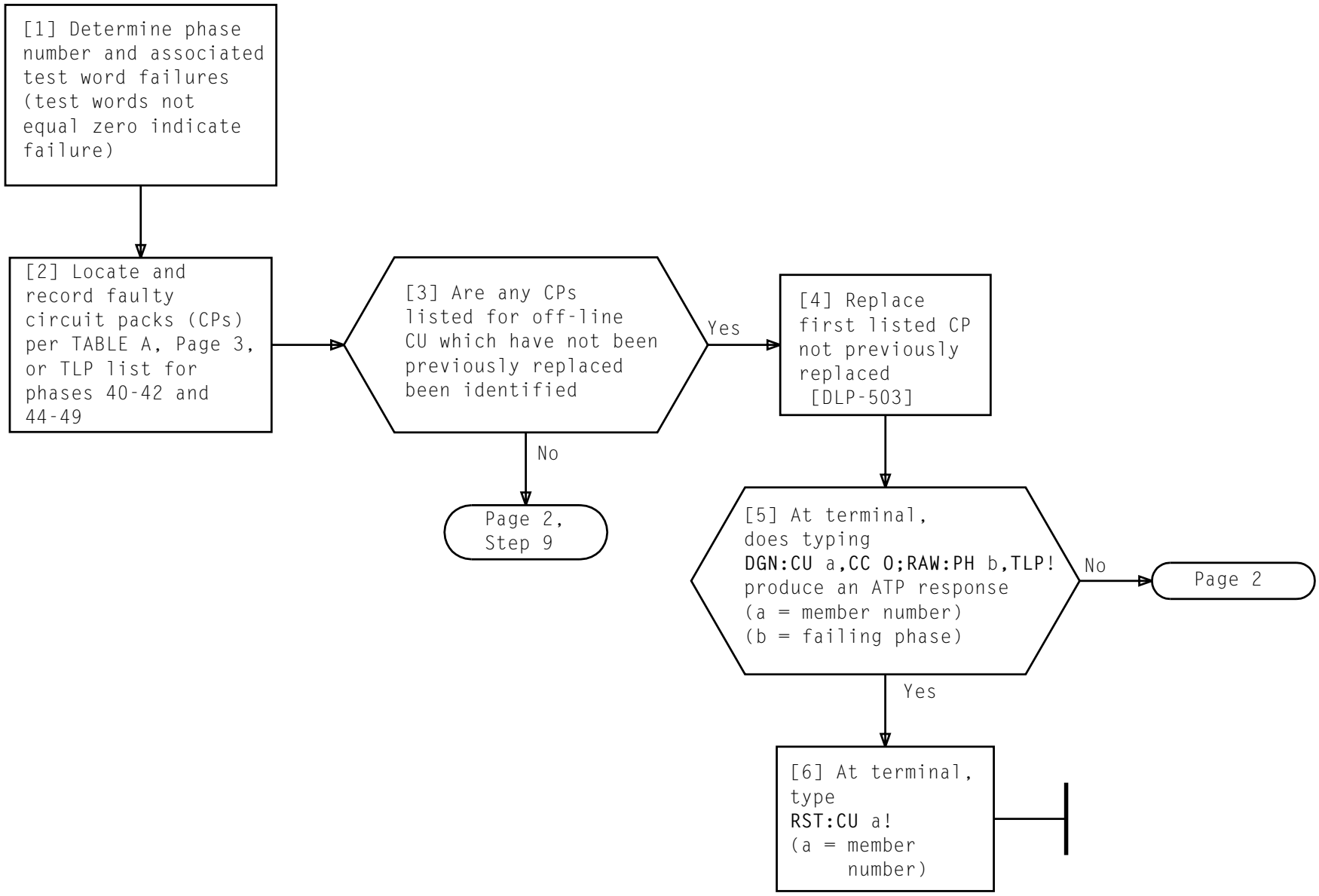
CLEAR CENTRAL CONTROL (CC) PHASES 30-38, 83-88, AND 90-92 WRITABLE MICROSTORE (WMS) FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 90, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	——
↕ ↕ 2-17	UN48B 56/60-042	——
18-38	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Addressing lead test
Phase 90, tests 39-64	UN135 56/60-066; UN48B 56/60-042; UN22C 56/60-028; UN28B 56/60-036	MSD invalid signal
Phase 91, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	——
↕ ↕ 2-17	UN48B 56/60-042	——
18-38	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Addressing lead test
Phase 91, tests 39-64	UN135 56/60-066; UN48B 56/60-042; UN22C 56/60-028; UN28B 56/60-036	MSD invalid signal
Phase 92, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	——
↕ ↕ 2-17	UN48B 56/60-042	——
18-38	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Addressing lead test
Phase 92, tests 39-64	UN135 56/60-066; UN48B 56/60-042; UN22C 56/60-028; UN28B 56/60-036	MSD invalid signal

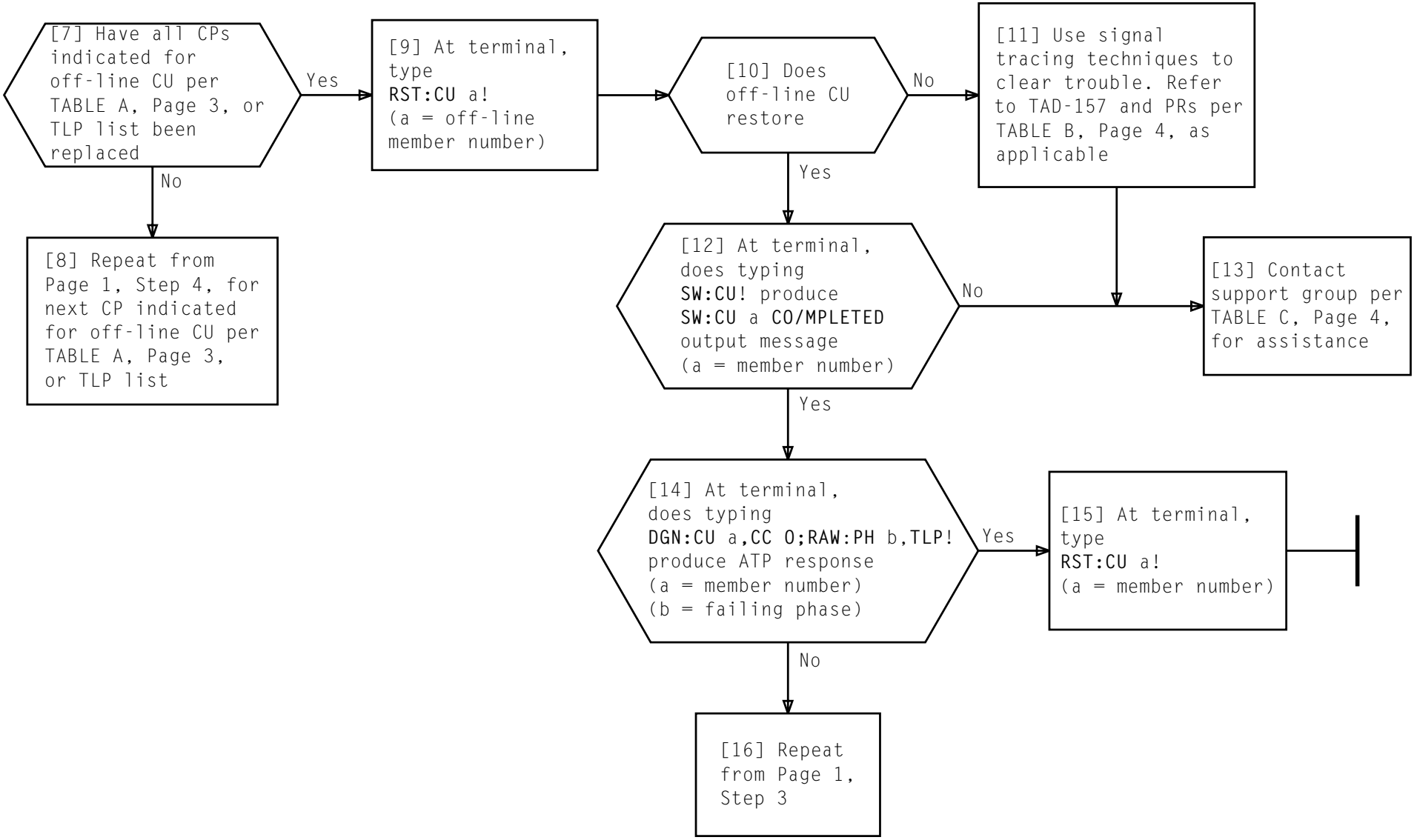
TABLE B	
PHASE NO.	PR NO.
30	4C30400
31	4C30500
32	4C30600
33	4C30700
34	4C30800
35	4C30900
36	4C31000
37	4C31100
38	4C31200
83	4C33700
84	4C33800
85	4C33900
86	4C34000
87	4C34100
88	4C34200
90	4C34300
91	4C34400
92	4C34500

TABLE C	
PRESENT SERVICE GROUP	NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASES 30-38, 83-88, AND 90-92 WRITABLE MICROSTORE (WMS) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 40-42 AND 44-49 STORE ADDRESS CONTROL (SAC) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 40-42 AND 44-49 STORE ADDRESS CONTROL (SAC) FAILURES

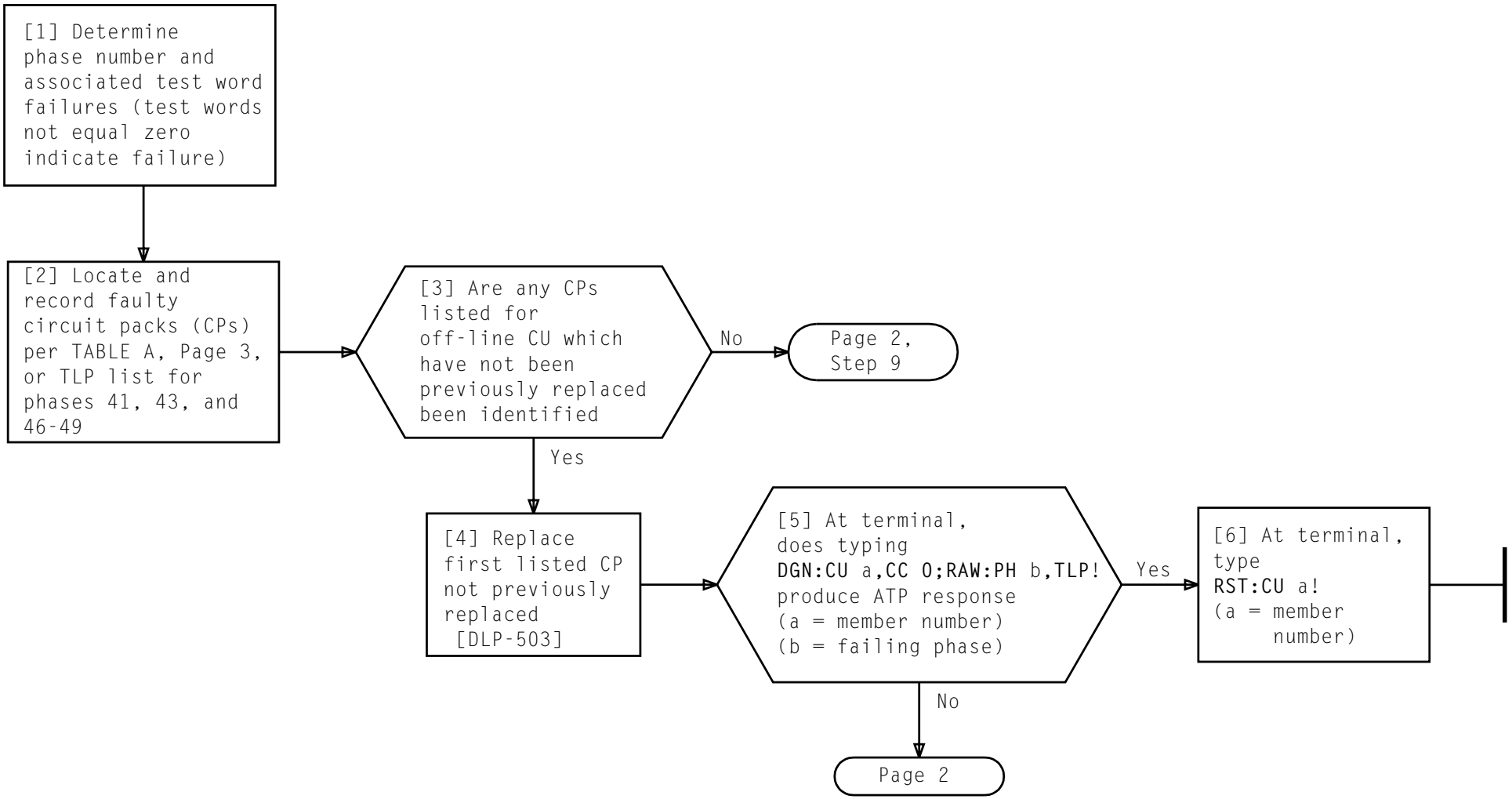
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 40, test 1	UN2B 56/60-084; UN135 56/60-066; UN22C 56/60-028	Destination bus to store control register (SCR)
2-36	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066; UN43C 56/60-104	Destination bus to SCR
37-150	UN135 56/60-066; UN43C 56/60-104	Microinstruction register to SCR
Phase 41, test 1	UN2B 56/60-084; UN22C 56/60-028	Test store data interface (SDI) registers of CC
2-113	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Test SDI registers of CC
Phase 42, test 1	UN2B 56/60-084; UN22C 56/60-028	Test store address interface (SAI) registers of CC
2-35	UN2B 56/60-084; UN3B 56/60-092; UN43C 56/60-104; UN45B 56/60-110	Test SAI registers of CC
36-81	UN2B 56/60-084; UN3B 56/60-092; UN43C 56/60-104	Test SAI registers of CC
82-89	UN43C 56/60-104	Program address register (PAR) shadow bits
Phase 42, test 90-106	UN2B 56/60-084; UN3B 56/60-092; UN43C 56/60-104	Test half-word/byte select check- circuitry
Phase 44, test 1	UN2B 56/60-084; UN22C 56/60-028	Test address incrementer circuitry
2-137	UN2B 56/60-084; UN3B 56/60-092	Test address incrementer circuitry
Phase 45, test 1	UN2B 56/60-084; UN22C 56/60-028	Test address incrementer circuitry
2-101	UN2B 56/60-084; UN3B 56/60-092	Test address incrementer circuitry
Phase 46, test 1	UN2B 56/60-084; UN22C 56/60-028	Half-word/byte available circuitry
2-12	UN2B 56/60-084	Half-word/byte available circuitry
13-216	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through half-word multiplexor (HM)
Phase 47, test 1	UN2B 56/60-084; UN22C 56/60-028	Data path through HM
2-161	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through HM
Phase 48, test 1	UN2B 56/60-084; UN22C 56/60-028	Data path through HM
2-161	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through HM

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 49, test 1	UN2B 56/60-084; UN22C 56/60-028	Data path through HM
2-161	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through HM

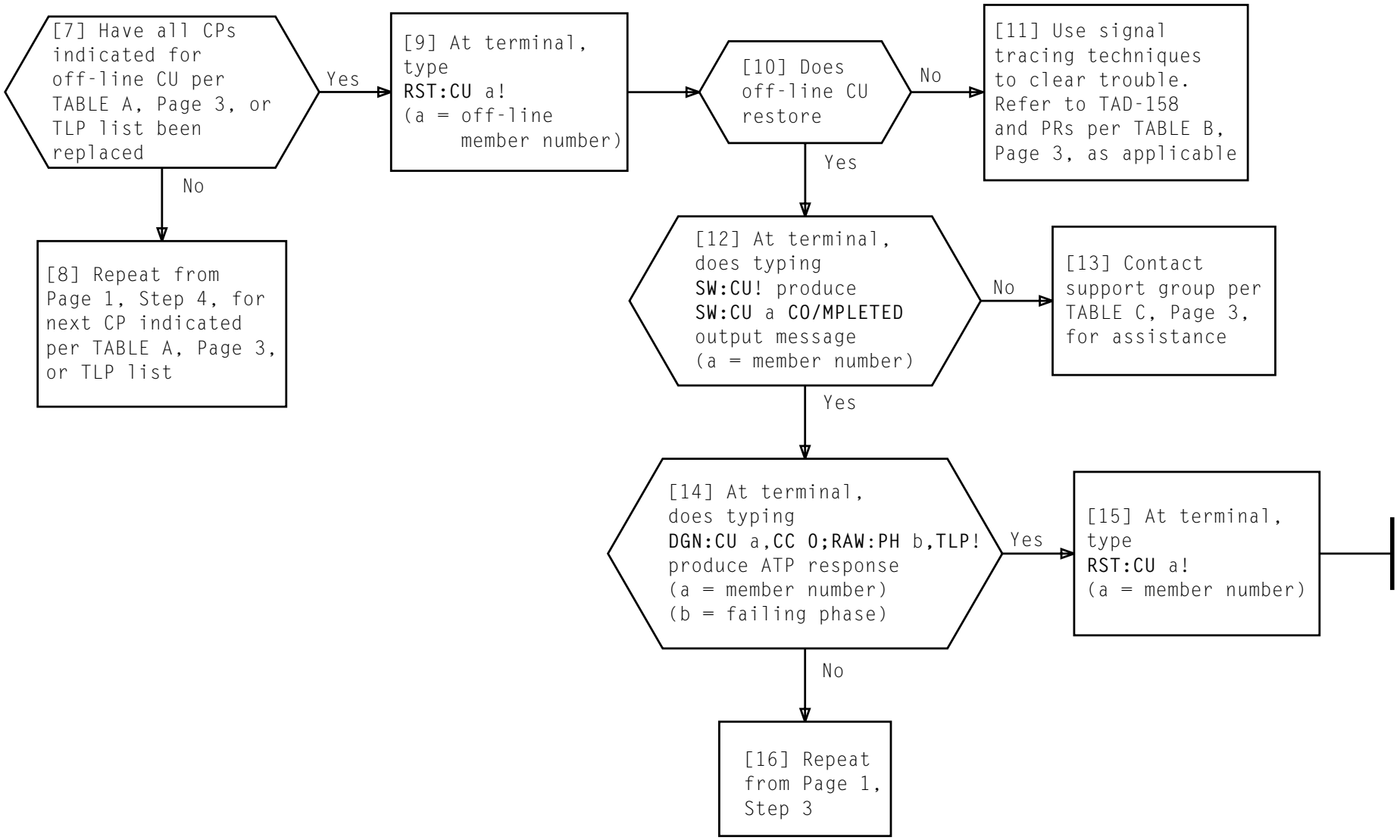
TABLE B	
PHASE NO.	**PR NO.**
40	4C31400
41	4C31500
42	4C31600
44	4C31800
45	4C31900
46	4C32000
47	4C32100
48	4C32200
49	4C32300

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASES 40-42 AND 44-49 STORE ADDRESS CONTROL (SAC) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASES 41, 43, AND 46-49 STORE DATA CONTROL (SDC) FAILURES



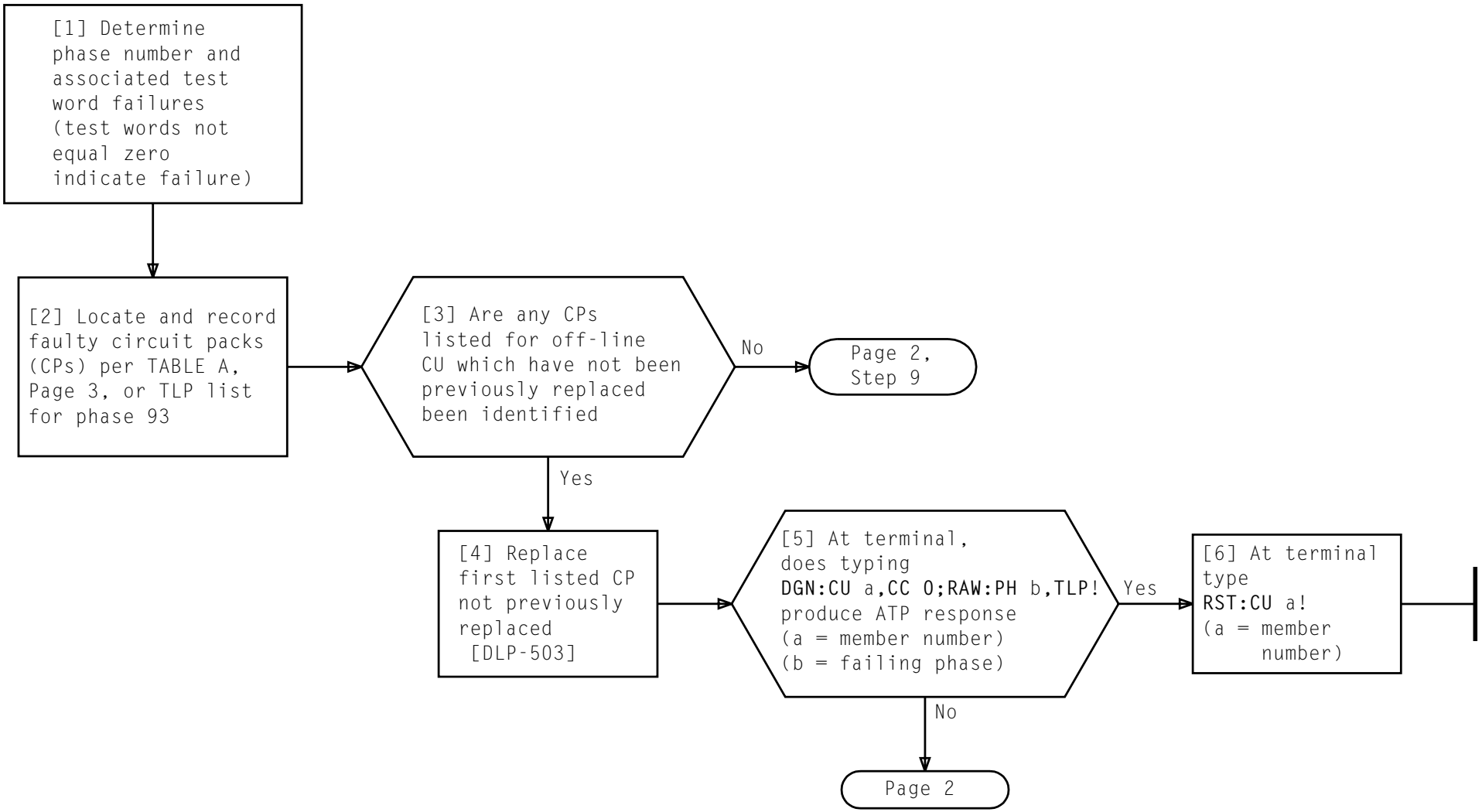
CLEAR CENTRAL CONTROL (CC) PHASES 41, 43, AND 46-49 STORE DATA CONTROL (SDC) FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 41, test 1	UN2B 56/60-084; UN22C 56/60-028	Test store data interface (SDI) registers of CC
2-13	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Test SDI registers of CC
Phase 43, test 1	UN2B 56/60-084; UN22C 56/60-028	Test instruction buffer (IB) parity circuit
2-13	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Test IB parity circuit
Phase 46, test 1	UN2B 56/60-084; UN22C 56/60-028	Half-word/byte available circuitry
2-12	UN2B 56/60-084	Half-word/byte available circuitry
13-216	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through half-word multiplexor (HM)
Phase 47, test 1	UN2B 56/60-084; UN22C 56/60-028	Data path through HM
2-161	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through HM
Phase 48, test 1	UN2B 56/60-084; UN22C 56/60-028	Data path through HM
2-161	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through HM
Phase 49, test 1	UN2B 56/60-084; UN22C 56/60-028	Data path through HM
2-161	UN2B 56/60-084; UN3B 56/60-092; UN6B 56/60-098	Data path through HM

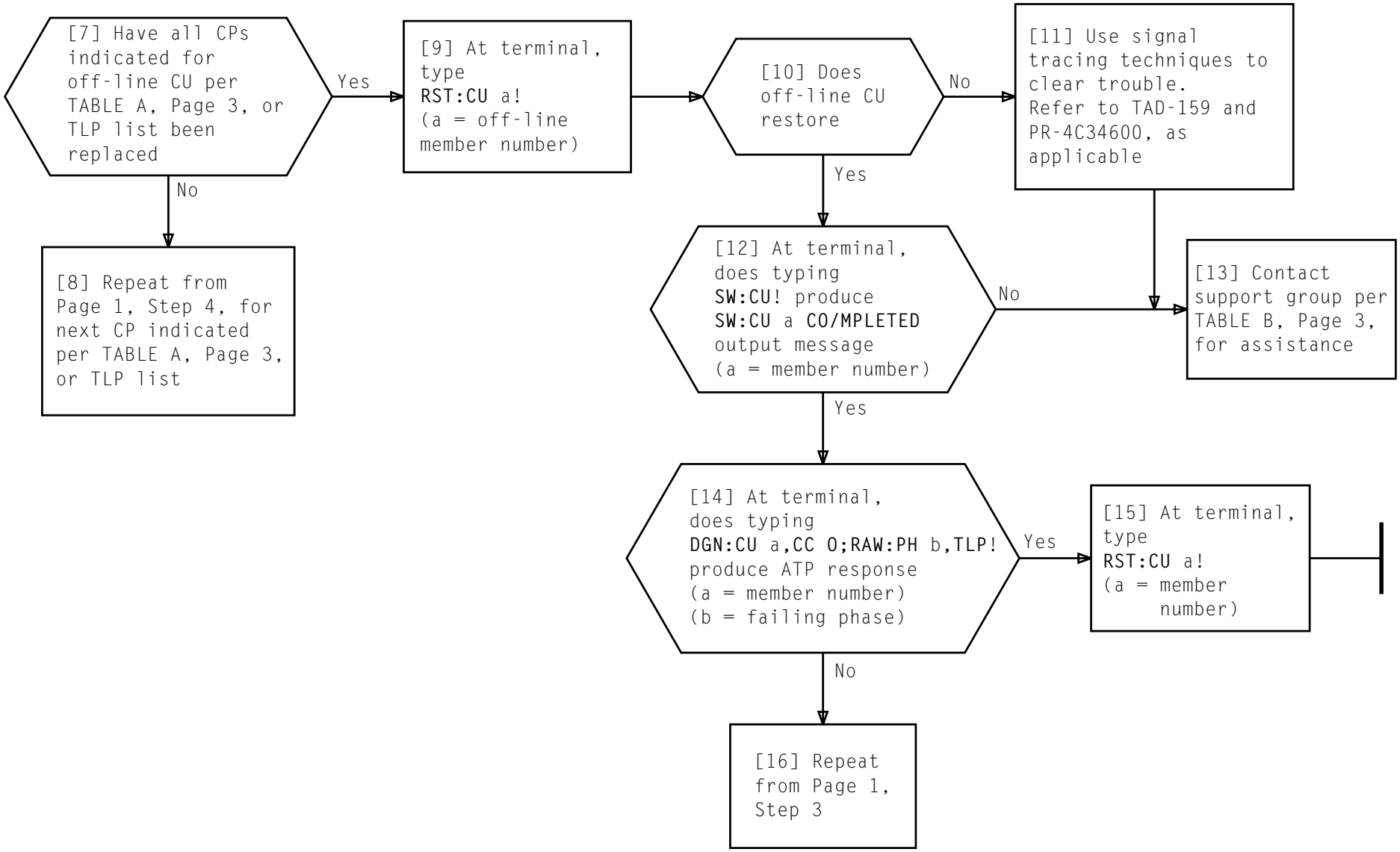
TABLE B	
PHASE NO.	**PR NO**
41	4C31500
43	4C31700
46	4C32000
47	4C32100
48	4C32200
49	4C32300

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL CC) PHASES 41, 43, AND 46-49 STORE DATA CONTROL (SDC) FAILURES



CLEAR CENTRAL CONTROL (CC) PHASE 93 EMERGENCY ACTION INTERFACE (EAI) DISPLAY FAILURES

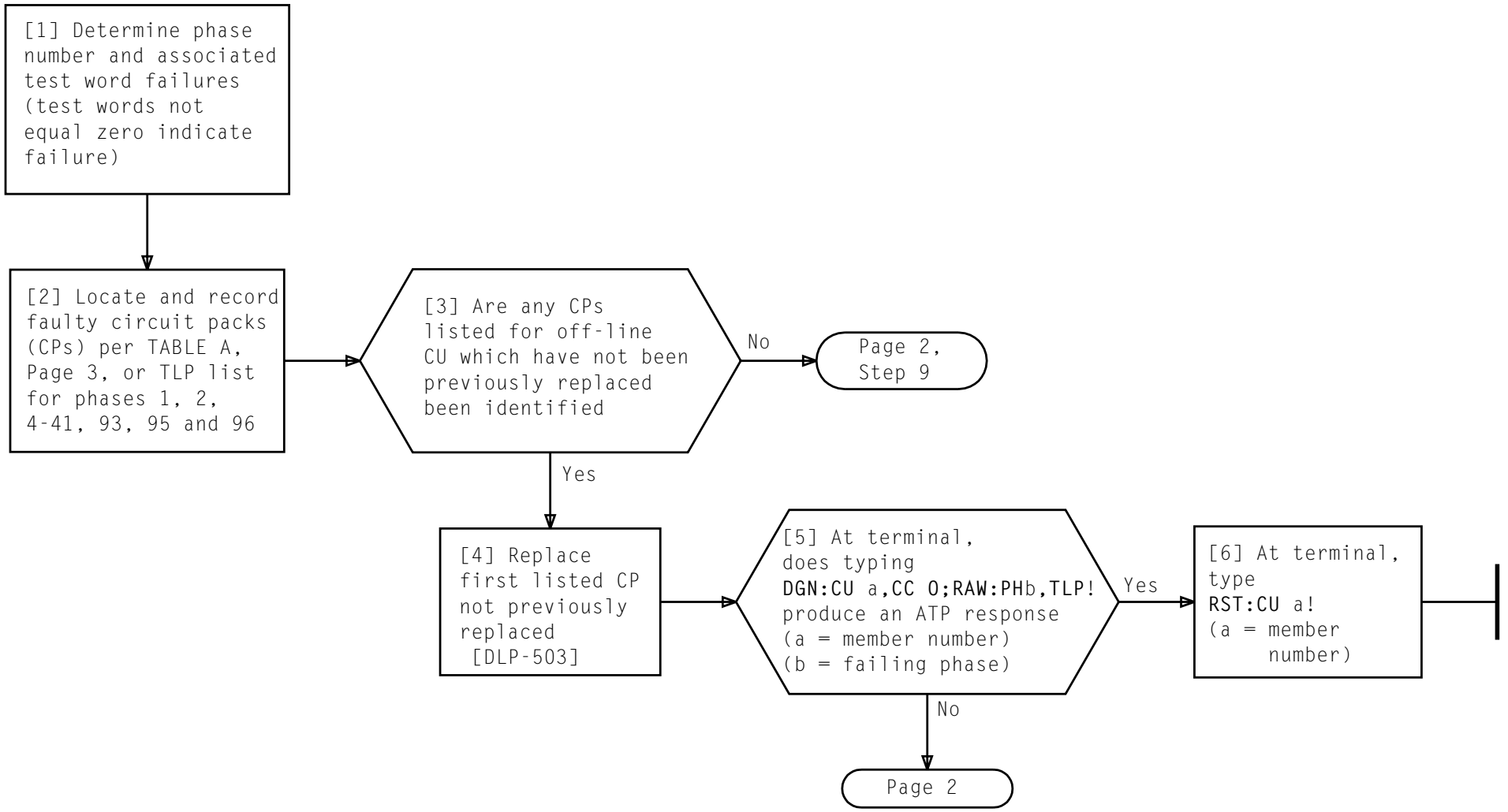


CLEAR CENTRAL CONTROL (CC) PHASE 93 EMERGENCY ACTION INTERFACE (EAI) DISPLAY FAILURES

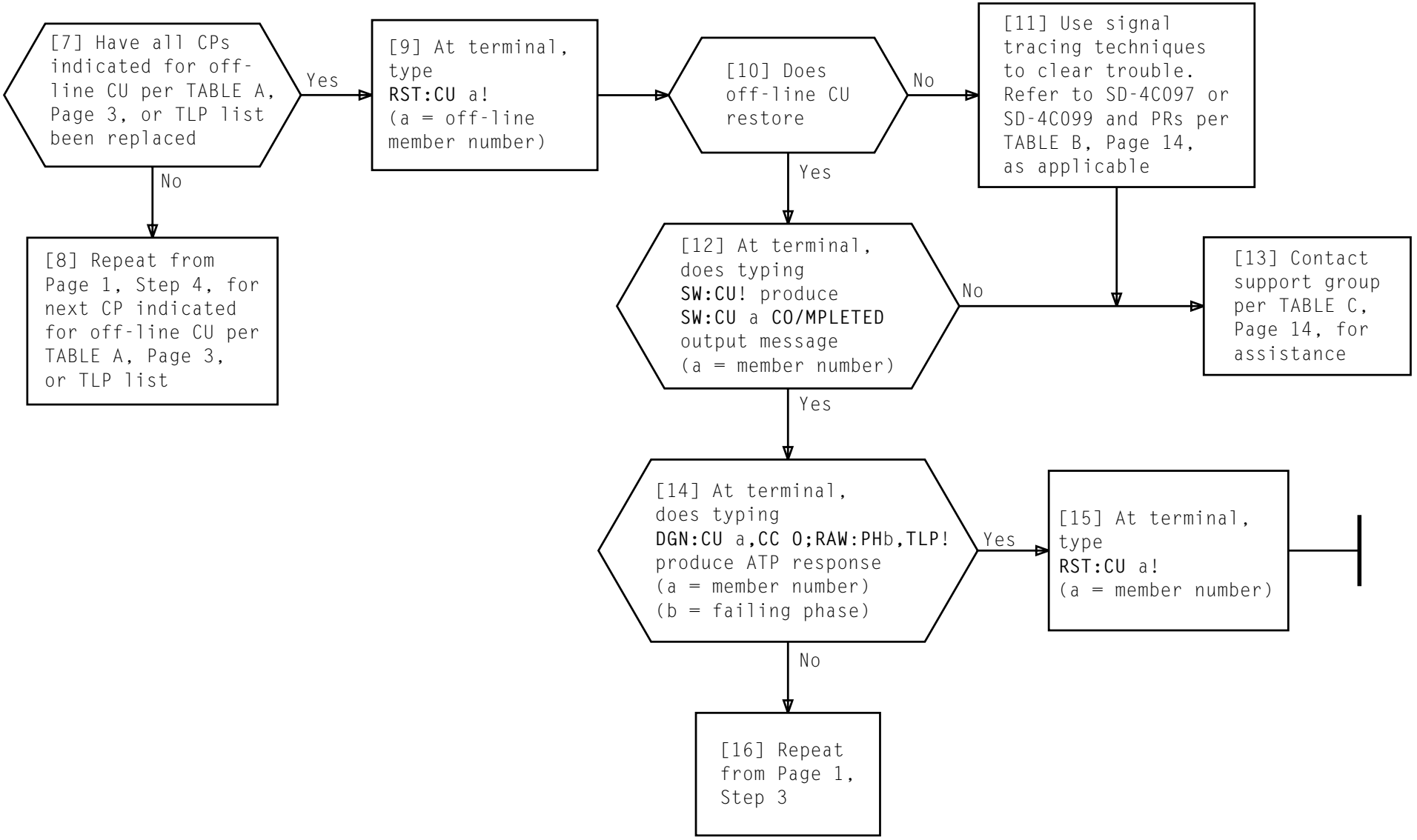
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 93, —	TN1O 56/6O-154; UN45B 56/6O-110	Processor recovery message (PRM) flushing
⇕ test 1-56	TN983 29/33-1O2 (peripheral control frame (PC FR)	PRM
	TN1O 56/6O-154; UN45B 56/6O-110	
Phase 93, test 57-59	TN983 29/33-1O2 (peripheral control frame (PC FR)	EAI display

TABLE B	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CENTRAL CONTROL (CC) PHASE 93 EMERGENCY ACTION INTERFACE (EAI) DISPLAY FAILURES



CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES



CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, test 1-3	UN2B 56/60-084; UN59 47/51-112	Test error B and C to be inactive
Phase 1, test 4-19	UN43C 56/60-104; UN59 47/51-112; UN45B 56/60-110	MAS response "STORE COMPLETE"
Phase 2, test 1-9	UN59 47/51-112; UN2B 56/60-084, UN45B 56/60-110	Address-loop-around tests
test 10-59	UN45B 56/60-110; UN6B 56/60-098; UN43C 56/60-104; UN59 47/51-112; UN133 56/60-146	Address-loop-around tests
test 60-67	UN45B 56/60-110; UN6B 56/60-098; UN43C 56/60-104, UN59 47/51-112; UN133 56/60-146	Address-loop-around tests
test 68-75	UN45B 56/60-110; UN6B 56/60-098; UN43C 56/60-104, UN59 47/51-112; UN133 56/60-146	Address-loop-around tests
Phase 2, test 76	UN59 47/51-112	Address-loop-around tests
Phase 4, test 1-90	UN6B 56/60-098; UN133 56/60-146; UN43C 56/60-104; UN59 47/51-112	Data communication bits 0-35
Phase 5, test 1-4	UN2B 56/60-084; UN59 47/51-112; UN43C 56/60-104	Test MASC error signals
test 5-40	UN2B 56/60-084; UN59 47/51-112; UN43C 56/60-104	MASC data and address parity check circuitry
test 41-47	UN45B 56/60-110; UN59 47/51-112; UN43C 56/60-104	MASC half-word and byte decoding
Phase 5, test 48-58	UN2B 56/60-084; UN45B 56/60-110; UN59 47/51-112; UN43C 56/60-104	Control lead parity tests
Phase 6, test 1-4	UN2B 56/60-084; UN3B 56/60-092; UN59 47/51-112	MAS maintenance commands inactive
test 5-31	UN2B 56/60-084; UN3B 56/60-092; UN59 47/51-112	MAS maintenance commands
Phase 6, test 32-37	UN2B 56/60-084; UN3B 56/60-092; UN59 47/51-112 UN43C 56/60-104	MY STORE TIMEOUT micro interrupt
Phase 7, test 1-5	UN59 47/51-112	Signal step MASC timing chain
test 6-12	UN59 47/51-112; UN135 56/60-066	Signal step MASC timing chain
test 13-14	UN59 47/51-112	Signal step MASC timing chain
test 15-16	UN59 47/51-112	Signal step MASC timing chain
Phase 7, test 17-18	UN59 47/51-112	Signal step MASC timing chain

CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 7, test 19-20	UN59 47/51-112	Signal step MASC timing chain
test 21-22	UN59 47/51-112	Signal step MASC timing chain
test-21-22	UN59 47/51-112	Signal step MASC timing chain
test 23-24	UN59 47/51-112	Signal step MASC timing chain
test 25-26	UN59 47/51-112	Signal step MASC timing chain
test 27-28	UN59 47/51-112	Signal step MASC timing chain
test 29-30	UN59 47/51-112	Signal step MASC timing chain
test 31-32	UN59 47/51-112	Signal step MASC timing chain
test 33-34	UN59 47/51-112	Signal step MASC timing chain
test 35-36	UN59 47/51-112	Signal step MASC timing chain
test 37-38	UN59 47/51-112	Signal step MASC timing chain
test 39-40	UN59 47/51-112	Signal step MASC timing chain
test 41-42	UN59 47/51-112	Signal step MASC timing chain
test 43-44	UN59 47/51-112	Signal step MASC timing chain
test 45-46	UN59 47/51-112	Signal step MASC timing chain
test 47-48	UN59 47/51-112	Signal step MASC timing chain
test 49-50	UN59 47/51-112	Signal step MASC timing chain
test 51-52	UN59 47/51-112	Signal step MASC timing chain
test 53-54	UN59 47/51-112	Signal step MASC timing chain
Phase 7, test 55-56	UN59 47/51-112	Signal step MASC timing chain
Phase 8, test 1-14	UN59 47/51-112	Extended refresh counter
Phase 8, test 15-24	UN59 47/51-112	Extended refresh counter
Phase 9, test 1-12	UN59 47/51-112	Test memory array response in a maintenance cycle
test 13-15	UN59 47/51-112	Test memory array response in refresh cycle
Phase 9, test 16-20	UN59 47/51-112	Test memory array response in normal cycles
Phase 10, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	UN59 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
Phase 10, test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests

CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 10, test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134 test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 10, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 11, test 1-7	UN2B 56/60-084; UN3B 56/60-092; UN135 56/60-066	Verify 50 nsec clock for microinstruction execution
test 8-13	UN135 56/60-066; UN43C 56/60-104	Verify 50 nsec clock for microinstruction execution
test 14-22	UN2B 56/60-084; UN135 56/60-066; UN43C 56/60-104	Verify 50 nsec clock for microinstruction execution
test 23-39	UN135 56/60-066; UN43C 56/60-104	Verify DST wait logic for extending microcode execution time
test 40-64	UN2B 56/60-084; UN135 56/60-066; UN43C 56/60-104	Verify SRC wait logic for extending microcode execution time
test 65-92	UN43C 56/60-104; UN6B 56/60-098	Verify NXTFA logic by performing a NXTFA test on MASCO MASAO
Phase 11, test 93-116	UN43C 56/60-104; UN6B 56/60-098	Verify NEWOPFA logic by performing a NEWOPFA test on MASCO MASAO
Phase 12, test 1-246	UN59 47/51-112; UN3B 56/60-092	Signal bit error correction tests
Phase 13, test 1-13	UN59 47/51-112; UN2B 56/60-084	Double-bit errors in single parity tree tests
Phase 13, test 14-53	UN59 47/51-112	Double-bit errors in multiple parity tree tests
Phase 14, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
Phase 14, test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry

CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 14, test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 14, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 15, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 15, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 16, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 16, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 17, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 17, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 18, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 18, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 19, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
Phase 19, test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 19, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 20, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 20, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 21, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 21, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 22, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 22, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 23, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 23, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 24, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
Phase 24, test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests

CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 24, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 25, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 25, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 26, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 26, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 27, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162;	Test MASC array address parity check circuitry
Phase 27, test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 27, test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162, UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 27, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162, UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 28, test 1-24	UN59 47/51-112	Test MASC array address parity check circuitry
test 25-46	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162, UN59 47/51-112	Test MASC array address parity check circuitry
test 47-90	UN59 47/51-112; UN135 56/60-066	Perform MASA tests
test 91-134	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162, UN59 47/51-112	Perform MASA tests
test 135-184	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162, UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 28, test 185-226	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162, UN59 47/51-112; UN135 56/60-066	Perform MASA tests
Phase 29, test 1-69	UN133 56/60-146; UN133 56/60-146 (on-line); UN43C 56/60-104; UN59 47/51-112	Address-loop-around on OFL MASCO
Phase 29, test 70-74	UN133 56/60-146; UN133 56/60-146 (on-line); UN43C 56/60-104; UN59 47/51-112	Address-loop-around on MASC1
Phase 30, test 1-78	UN6B 56/60-098; UN133 56/60-146; UN133 56/60-146 (on-line); UN43C 56/60-104; UN59 47/51-112	Data communication
Phase 31, test 1-12	UN133 56/60-146; UN133 56/60-146 (on-line); UN43C 56/60-104 (on-line)	Control lead parity tests
tests 13-20	UN133 56/60-146; UN133 56/60-146 (on-line); UN43C 56/60-104 (on-line); UN2B 56/60-084; UN3B 56/60-092	Other store error bits
Phase 31, test 21	UN133 56/60-146; UN133 56/60-146 (on-line); UN43C 56/60-104 (on-line); UN3B 56/60-092	Other store error bits

CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES

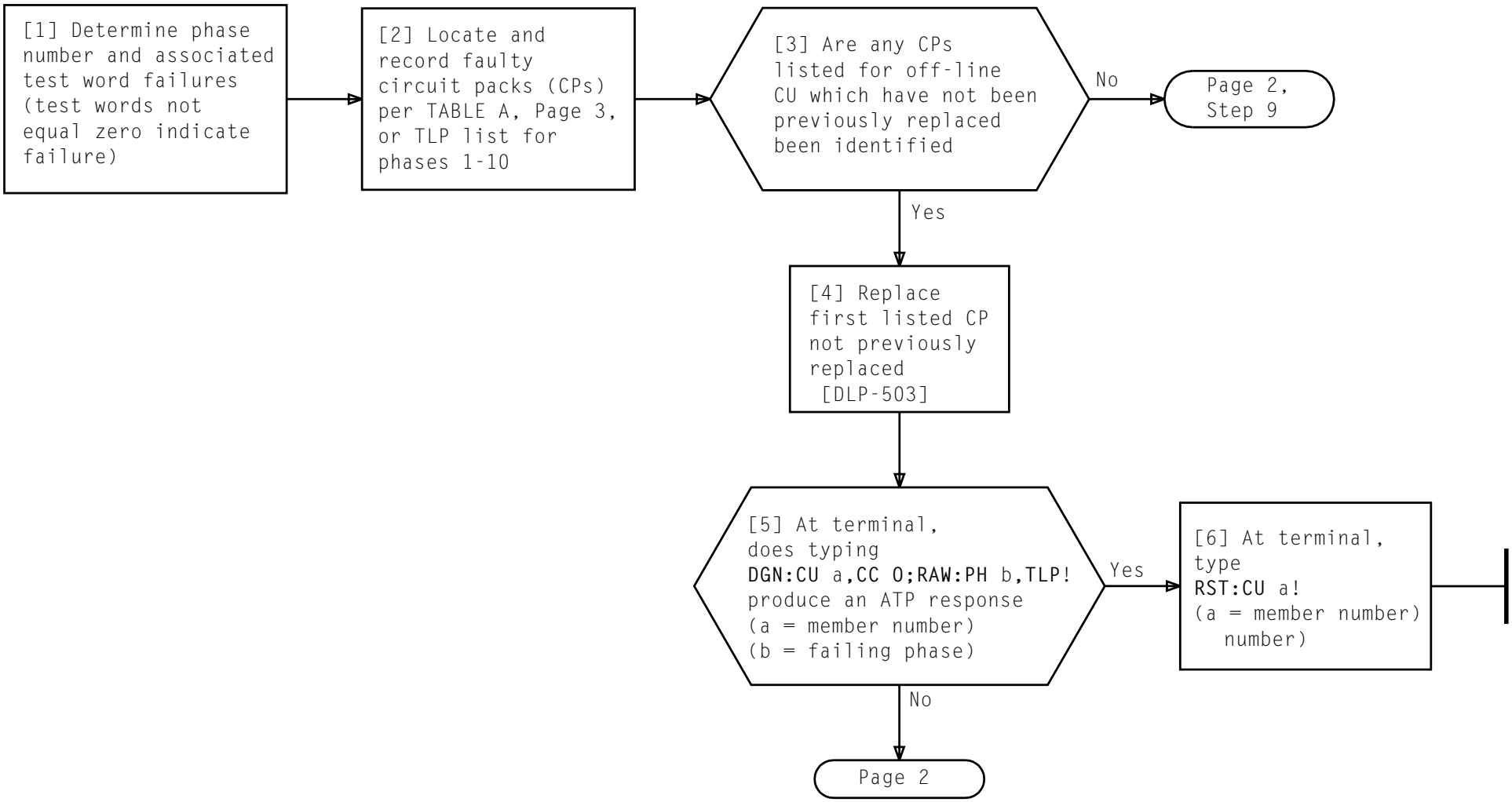
TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 32, test 1-39	UN2B 56/60-084; UN3B 56/60-092 UN135 56/60-066; UN59 47/51-112	Test MASC errors B and C micro interrupt
Phase 33, test 1-9	UN59 47/51-112; TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162	Tests patterns
Phase 34, test 1-9	UN59 47/51-112; TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162	Tests patterns
Phase 35, test 1-9	UN59 47/51-112; TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162	Tests patterns — memory march
Phase 36, test 1-9	UN59 47/51-112; TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162	Tests patterns
Phase 37, test 1-25 Phase 37, test 26-37	UN59 47/51-112; UN2B 56/60-084; UN3B 56/60-092 UN59 47/51-112; UN2B 56/60-084; UN3B 56/60-092	Test refresh data parity error and data Test MASC's ability to block errors C and D
Phase 38, test 1-66 Phase 38, test 67-83	UN45B 56/60-110; UN6B 56/60-098,UN43C 56/60-104; UN59 47/51-112 UN45B 56/60-110; UN6B 56/60-098; UN59 47/51-112; UN43C 56/60-104	Execute fetch instructions Execute 3B code out of offline MAS
Phase 39, test 1-12	UN133 56/60-146 (on-line); UN133 56/60-146; UN59 47/51-112	Slave (update) tests

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 40, test 1-28	UN59 47/51-112; TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162	Test pattern half-word memory march
Phase 41, test 1-12	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN133 56/60-146 (on-line); UN133 56/60-146; UN59 47/51-112	Slave (update) tests
Phase 93, test 1-777	UN59 47/51-112	Test reel and dup ref adr reg
Phase 95, test 1-12	UN59 47/51-112; TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162	Test memory using specified input parameters (interactive mode)
Phase 96, test 1-12	TN28 47/51-120, 126, 132, 138, 144, 150, 156, 162; UN133 56/60-146 (on-line); UN133 56/60-146; UN59 47/51-112	Slave (update) tests

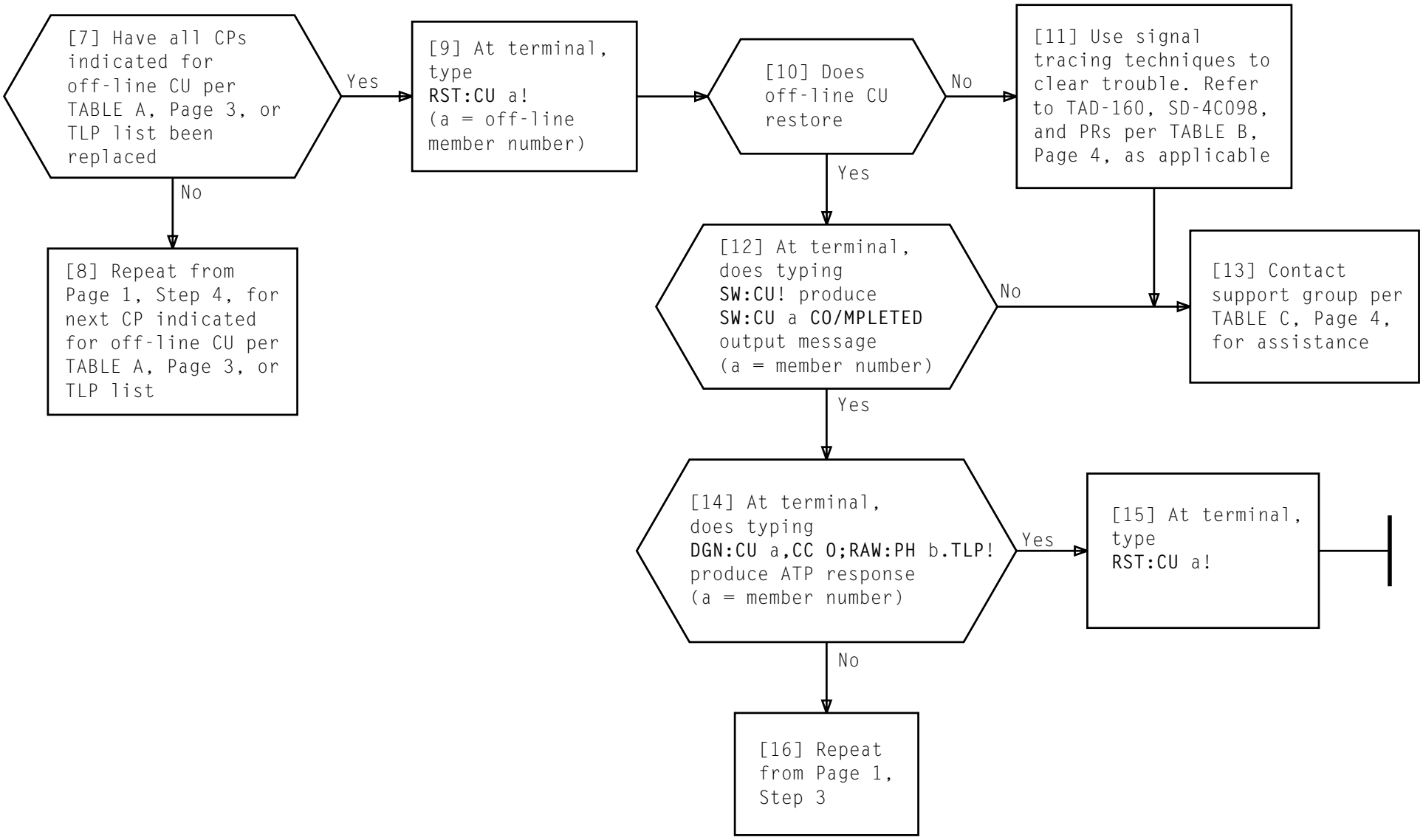
TABLE B			
PHASE NO.	PR NO.	PHASE NO.	PR NO.
	4C42100	26	4C44600
1	200	27	700
2	300	28	800
4	400	29	4C44900
5	500	30	4C45000
6	600	31	4C45100
7	700	32	200
8	800	33	300
9	4C42900	34	400
10	4C43000	35	4C45500
11	100	36	4C45600
12	200	37	700
13	300	38	800
14	400	39	4C45900
15	500	40	4C46000
16	600	41	050
17	700	93	100
18	800	95	200
19	4C43900	96	250
20	4C44000		300
21	100		400
22	200		500
23	300		600
24	400		700
25	500		800
			4C46900
			4C47000

TABLE C	
PRESENT SERVICE GROUP	NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR MAIN STORE CONTROLLER (MASC) INCLUDING MEMORY ARRAYS PHASES 1, 2, 4-41, 93, 95, AND 96 FAILURES



CLEAR STORE ADDRESS TRANSLATOR (SAT) PHASES 1-10 FAILURES



CLEAR STORE ADDRESS TRANSLATOR (SAT) PHASES 1-10 FAILURES

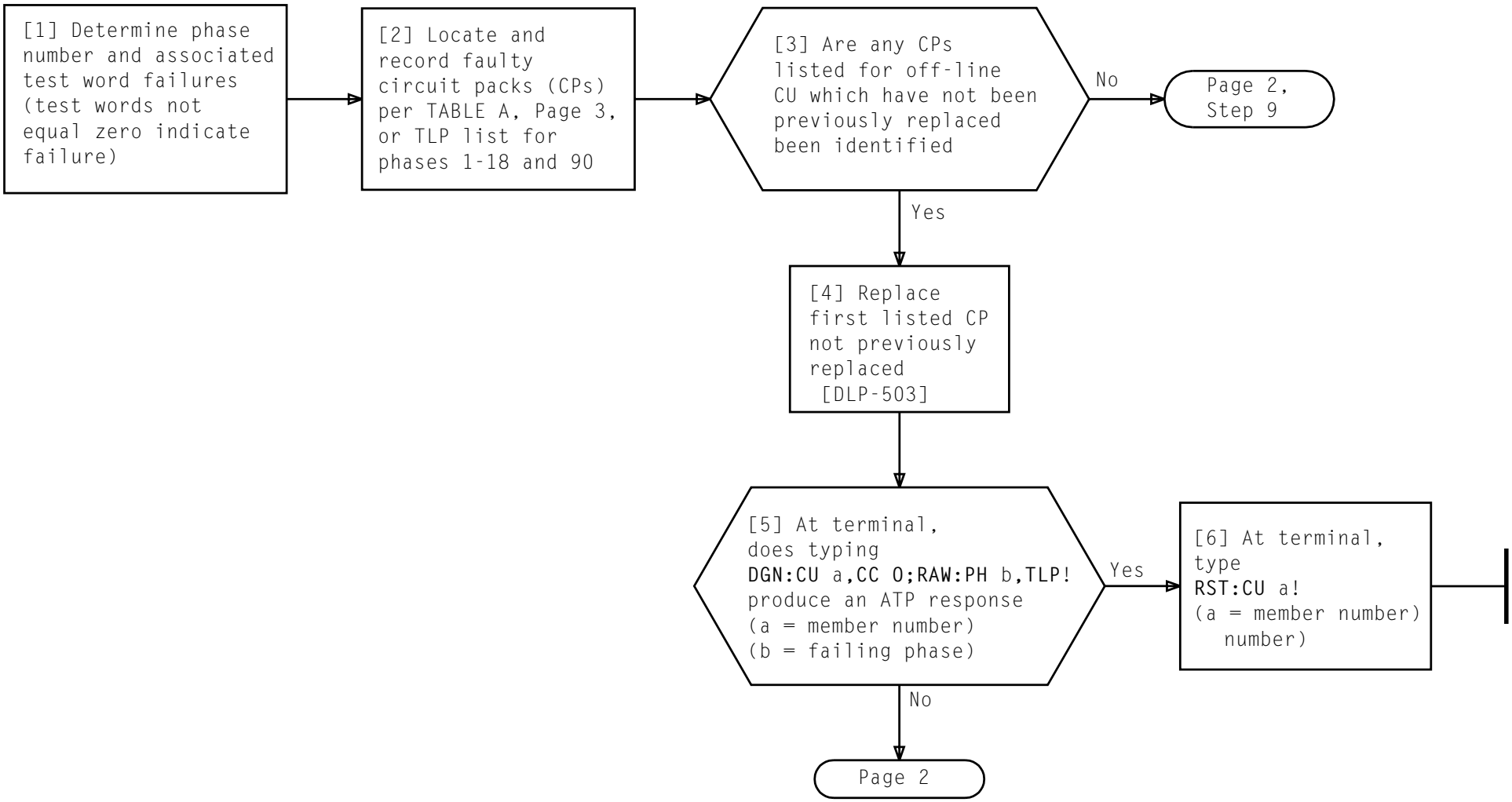
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, tests 1-6	UN43C 56/60-104	Control flip-flop and preliminary counter tests
Phase 2, tests 1-65 66-129 130-153 154-169 170-185 186-193 Phase 2, tests 194-200	 UN45B 56/60-110 UN45B 56/60-110	Address translation buffer A (ATBA) access tests ATBB access tests ATBA parity checker tests ATBB parity checker tests Store address register (SAR) parity checker tests Program status word (PSW) parity checker tests Test of ATB bypass mode affect on access to ATBs and inhibit of ATB parity error
Phase 3, tests 1-10 Phase 3, tests 11-19	UN45B 56/60-110	ATBA memory tests ATBB memory tests
Phase 4, tests 1-3 4-195 196-197 198-389 Phase 4, tests 390-391	 UN45B 56/60-110, UN43C 56/60-104 UN45B 56/60-110	ATBA invalidate tests Test of counter with ATBA ATBB invalidate tests Test of counter with ATBB Test that both ATBA and ATBB invalidate simultaneously
Phase 5, tests 1-15 Phase 5, tests 16-29	UN45B 56/60-110	Test of ATBA multiplexors Test of ATBB multiplexors
Phase 6, tests 1-13 Phase 6, tests 14-29	UN45B 56/60-110	Write control logic tests Test of parity generator over segment base register (SBR) and PRAFF
Phase 7, tests 1-3 4-49 50-95 96-99 Phase 7, tests 100-106	 UN45B 56/60-110	Test of ATB hit and miss Test of ATBA compare logic Test of ATBB compare logic Test of no ATB miss when in ATB bypass mode Test of double hit check logic and that error register (ER) bit 4 generates a microinterrupt when active
Phase 8, tests 1-33 Phase 8, tests 34-35	UN45B 56/60-110; UN3B 56/60-092; UN43C 56/60-104 UN45B 56/60-110; UN2B 56/60-084; UN3B 56/60-092; UN43C 56/60-104; UN135 56/60-066	Test of protection check logic Test of page fault check logic
Phase 9, tests 1-23	UN45B 56/60-110	Test matcher of duplicated store address translator (SAT) circuits
Phase 10, tests 1-9 10-25 Phase 10, tests 26-32	 UN45B 56/60-110	Main store interface tests SAR/ATB relocation address parity generator test Test of store go inhibit on ATB miss, ATB protection violation or ATB page fault

CLEAR STORE ADDRESS TRANSLATOR (SAT) PHASES 1-10 FAILURES

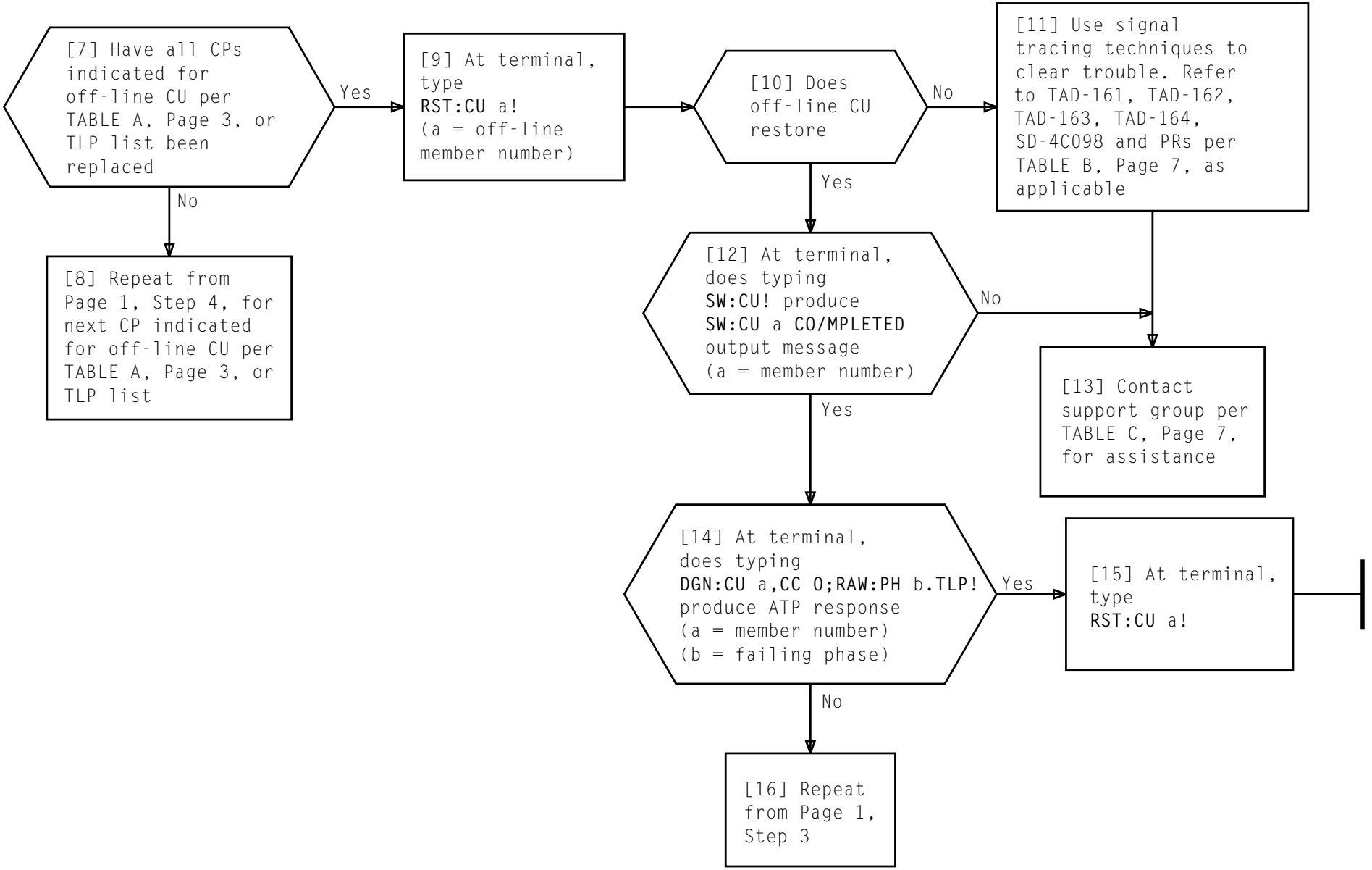
TABLE B	
PHASE NO.	PR NO.
1	4C49400
2	500
3	600
4	700
5	800
6	4C50000
7	100
8	200
9	300
10	4C50400

TABLE C	
PRESENT SERVICE GROUP	NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR STORE ADDRESS TRANSLATOR (SAT) PHASES 1-10 FAILURES



CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES



CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, tests 1-6	UN10B 56/60-124	Cache initial access test
7-11	UN10B 56/60-130	Cache initial access test
12-31	UN11B 56/60-138	Cache initial access test
32-70	UN45B 56/60-110	Interrupt stack enable tests
71-83	UN11B 56/60-138	Test of interrupt stack decoder
84-88	UN45B 56/60-110	Test of interrupt stack decoder
89-122	UN10B 56/60-124	Cache data bus test
123-156	UN10B 56/60-130	Cache data bus test
Phase 1, tests 157-224	UN11B 56/60-138	Cache data bus test
Phase 2, test 1		Initialization
tests 2-11	UN10B 56/60-124	Test of Tag A and B
12-21	UN10B 56/60-130	Test of Tag C and D
22-41		Test of Store A
42-61		Test of Store B
62-81		Test of Store C
Phase 2, tests 82-101	UN11B 56/60-138; UN45B 56/60-110	Test of Store D
Phase 3, tests 1-2	UN10B 56/60-124; UN11B 56/60-138	Internal stack enable and initial hit and miss counters tests
test 3	UN10B 56/60-130; UN11B 56/60-138	Internal stack enable and initial hit and miss counters tests
tests 4-7	UN10B 56/60-124; UN10B 56/60-130; UN11B 56/60-138	Internal stack enable and initial hit and miss counters tests
Phase 3, tests 8-66	UN10B 56/60-124; UN11B 56/60-138	Internal stack enable and initial hit and miss counters tests
Phase 4, tests 1-60	UN10B 56/60-124; UN11B 56/60-138	Test of matchers 4 and 3 on CAC0 (UN10), matcher output to cache hit/miss logic and cache store enable logic
Phase 5, tests 1-60	UN10B 56/60-130; UN11B 56/60-138	Test of matchers 1 and 3 on CAC1 (UN10), matcher output to cache hit/miss logic and cache store enable logic
Phase 6, tests 1-60	UN10B 56/60-130; UN11B 56/60-138	Test of matchers 4 and 2 on CAC1 (UN10), matcher output to cache hit/miss logic and cache store enable logic
Phase 7, tests 1-9		Test direct replacement
Phase 7, tests 10-14	UN11B 56/60-138	Test random replacement
Phase 8, tests 1-38		No enable test and test of cache tag mode A write control logic
39-70	UN10B 56/60-124	Test of cache tag mode B write control logic
71-79	UN11B 56/60-138; UN133 56/60-146	Test of cache/main store update interface
Phase 8, tests 80-81	UN11B 56/60-138; UN133 56/60-146; UN133 56/60-146 (on-line)	
Phase 9, tests 1		
2-36		Test of cache tag mode C write control logic
Phase 9, tests 37-38	UN10B 56/60-130	Test of cache tag mode D write control logic

CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 10, tests 1-2	UN10B 56/60-124	Test of address translation buffer A (ATBA) relocation address to tag memory modes A/C
test 3	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
4	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
5	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
6	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
7	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
8	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
9	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
10	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
11	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
12	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
13	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
14	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
15	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
16	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
17	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
18	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
19	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
20	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
21	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
22	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
23	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
24	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
25	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
26	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
27	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
28	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
29	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
30	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
31	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
32	UN10B 56/60-124	Test ATBA relocation address to tag memory modes A/C
Phase 10, test 33	UN10B 56/60-130	Test ATBA relocation address to tag memory modes A/C
Phase 11, tests 1-2	UN10B 56/60-124	Test ATBA relocation address to tag memory modes B/D
test 3	UN10B 56/60-130	Test ATBA relocation address to tag memory modes B/D
4	UN10B 56/60-124	Test ATBA relocation address to tag memory modes B/D
5	UN10B 56/60-130	Test ATBA relocation address to tag memory modes B/D
6	UN10B 56/60-124	Test ATBA relocation address to tag memory modes B/D
Phase 11, test 7	UN10B 56/60-130	Test ATBA relocation address to tag memory modes B/D

CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES

TABLE A (Contd)

PHASES AND TEST FAILURE	SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER	COMMENTS
Phase 11, test 8	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
9	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
10	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
11	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
12	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
13	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
14	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
15	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
16	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
17	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
18	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
19	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
20	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
21	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
22	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
23	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
24	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
25	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
26	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
27	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
28	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
29	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
30	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
31	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
32	UN10B 56/60-124	Test ATBB relocation address to tag memory modes B/D
Phase 11, test 33	UN10B 56/60-130	Test ATBB relocation address to tag memory modes B/D
Phase 12, tests 1-10	UN10B 56/60-124; UN11B 56/60-138	Tag modes A and B — address and data parity generation tests
Phase 12, tests 11-19	UN10B 56/60-130; UN11B 56/60-138	Tag modes C and D — address and data parity generation tests
Phase 13, tests 1-2	UN10B 56/60-124; UN2B 56/60-084; UN11B 56/60-138	Tag mode A — data parity check circuits
3-16	UN10B 56/60-124; UN2B 56/60-084	Tag mode A — data parity check circuits
17-24	UN10B 56/60-124; UN2B 56/60-084	Tag mode B — data parity check circuits
25-32	UN10B 56/60-130; UN2B 56/60-084	Tag mode C — data parity check circuits
33-40	UN10B 56/60-130; UN2B 56/60-084	Tag mode D — data parity check circuits
41-48	UN10B 56/60-124; UN2B 56/60-084	Tag modes A and B — address parity check circuit tests
49-56	UN10B 56/60-130; UN2B 56/60-084	Tag modes C and D — address parity check circuit tests
57-59	UN10B 56/60-124; UN2B 56/60-084	Tag modes A and B — address parity check inhibit tests
Phase 13, tests 60-62	UN10B 56/60-130; UN2B 56/60-084	Tag modes C and D — address parity check inhibit tests

CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES

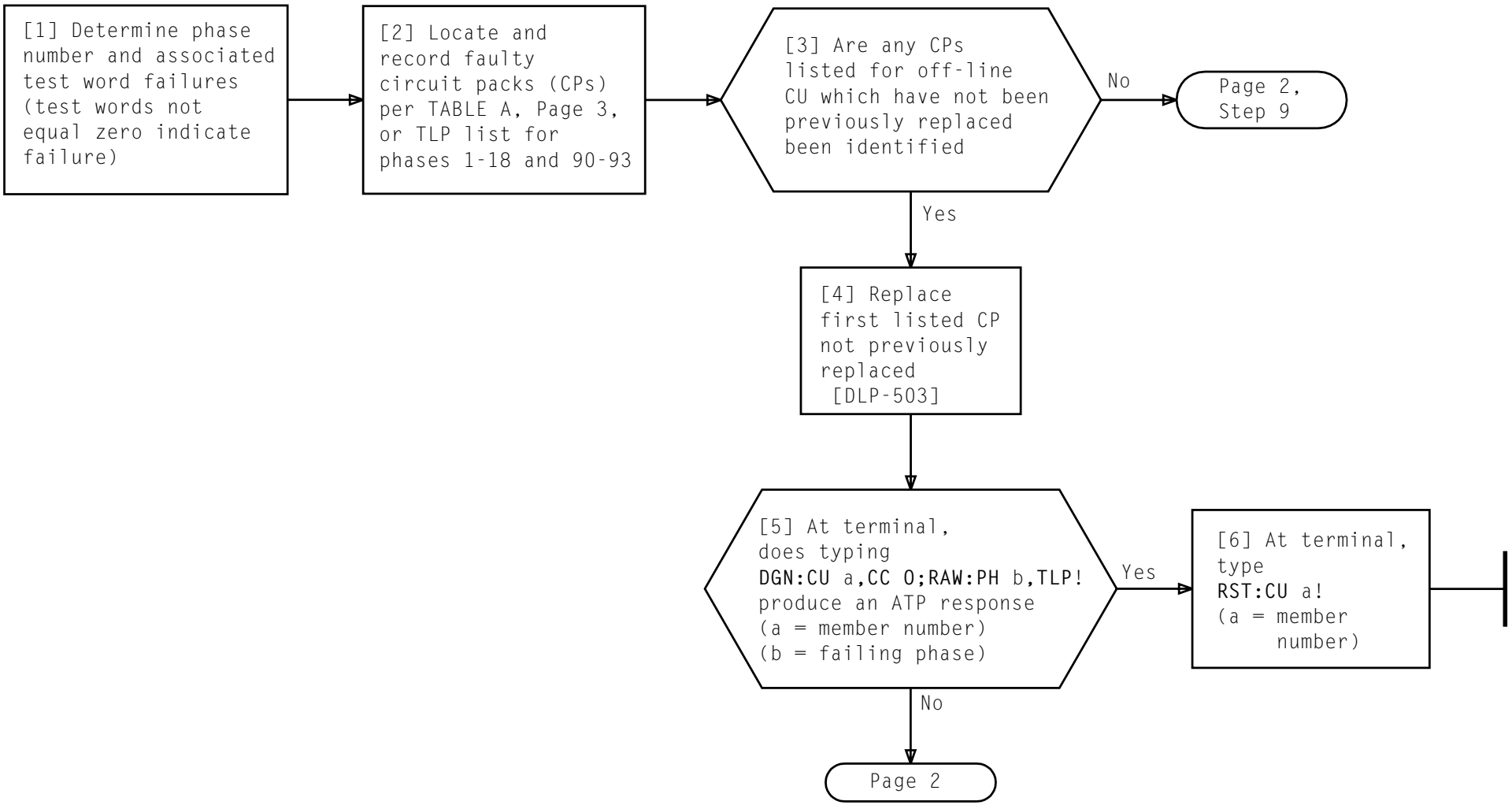
TABLE A (Contd)		
PHASES AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 14, tests 1-2	UN10B 56/60-124	Test of the hit and miss counters
test 3	UN10B 56/60-130	Test of the hit and miss counters
tests 4-30	UN10B 56/60-124	Test of the hit and miss counters
test 31	UN10B 56/60-130	Test of the hit and miss counters
tests 32-34	UN10B 56/60-124	Test of the hit and miss counters
test 35	UN10B 56/60-130	Test of the hit and miss counters
36	UN10B 56/60-124	Test of the hit and miss counters
37	UN10B 56/60-130	Test of the hit and miss counters
tests 38-40	UN10B 56/60-124	Test of counter inhibit logic
Phase 14, tests 41-43	UN10B 56/60-130	Test of counter inhibit logic
Phase 15, tests 1-23		Cache store write control logic tests — stack write operations
Phase 15, tests 24-53	UN11B 56/60-138	Cache store write control logic tests — write update operations
Phase 16, —		Cache store unit control logic test normal read operation
—	UN11B 56/60-138	Cache store control logic test — stack read operations
Phase 16, —	UN10B 56/60-124; UN10B 56/60-130; UN11B 56/60-138	Cache store unit control logic test — read operations
Phase 17, tests 1-12		Cache store read — multiple hit enable check circuit tests
Phase 17, tests 13-21	UN11B 56/60-138	Cache store write enable check circuit tests
Phase 18, tests 1-55	UN10B 56/60-124; UN10B 56/60-130; UN11B 56/60-138; UN45B 56/60-110	Cache exercise test
Phase 90, tests 1-55	UN10B 56/60-124; UN10B 56/60-130; UN11B 56/60-138; UN45B 56/60-110	Cache exercise test

CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES

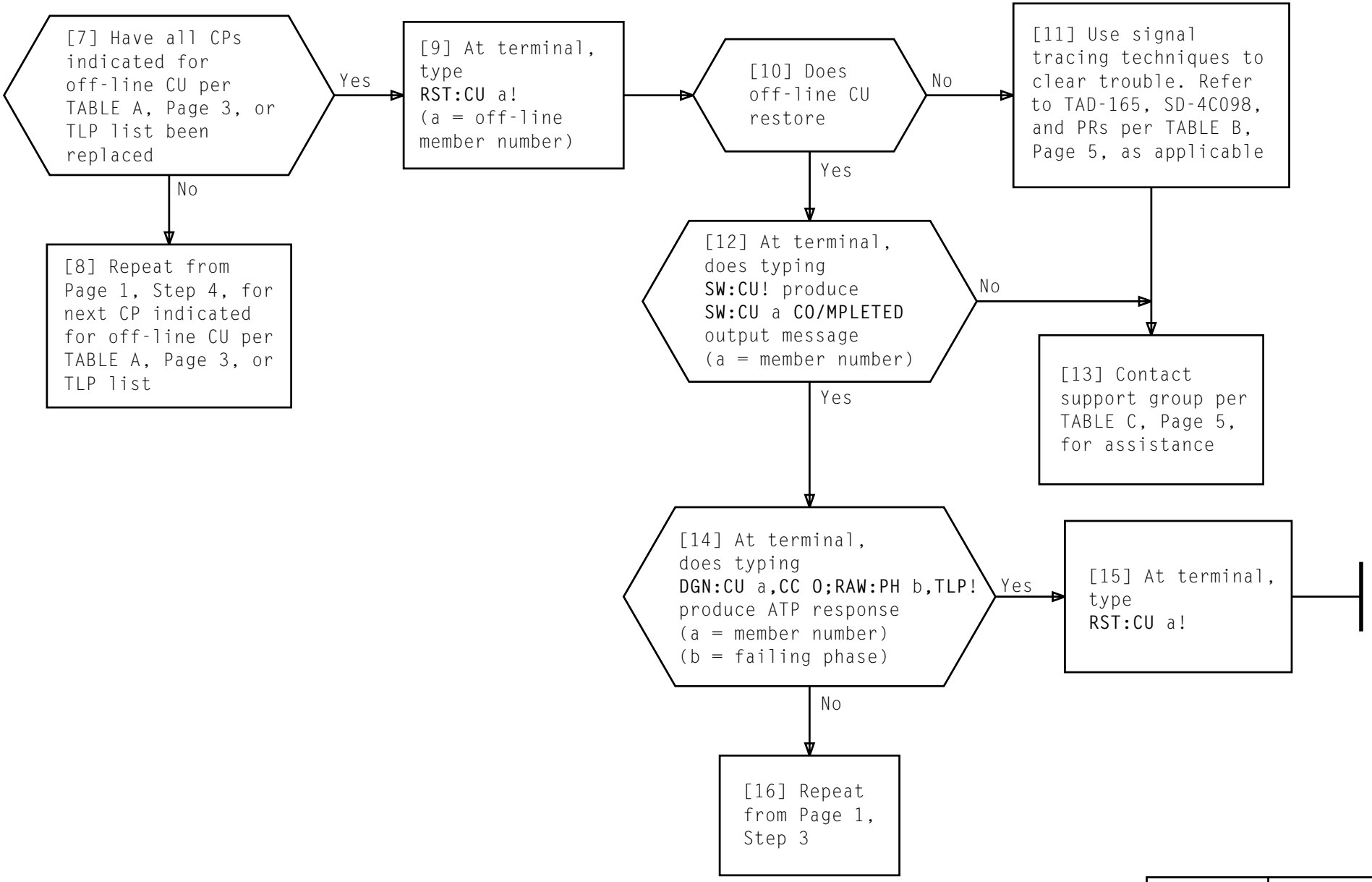
TABLE B			
PHASE NO.	PR NO.	PHASE NO.	PR NO.
	4C34700	10	4C35700
1	800	11	800
2	4C34900	12	4C35900
3	4C35000	13	4C36000
4	100	14	100
5	200	15	200
6	300	16	300
7	400	17	400
8	500	18	500
9	4C35600	90	4C36600

TABLE C	
PRESENT SERVICE GROUP	NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR CACHE STORE UNIT, CACHE CONTROL 0/1, CACHE MEMORY, OR CACHE MEMORY STRAPPING PHASES 1-18 AND 90 FAILURES



CLEAR UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES



CLEAR UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, tests 1-13	UN21B/61B 56/60-118; UN3B 56/60-092; UN23C 56/60-078	BGB access and enable to UC tests
Phase 2, tests 1-9 Phase 2, tests 10-23	UN21B/61B 56/60-118 UN21B/61B 56/60-118	Access matcher address tests Access matcher read/write tests
Phase 3, tests 1-17 Phase 3, tests 18-47	UN21B/61B 56/60-118 UN21B/61B 56/60-118	Block address matcher address tests Block address matcher read/write tests
Phase 4, tests 1-17 Phase 4, tests 18-47	UN21B/61B 56/60-118 UN21B/61B 56/60-118	Address matcher address tests Address matcher read/write tests
Phase 5, tests 1-17 Phase 5, tests 18-47	UN21B/61B 56/60-118 UN21B/61B 56/60-118	UID matcher address tests UID matcher read/write tests
Phase 6, tests 1-17 Phase 6, tests 18-55	UN21B/61B 56/60-118 UN21B/61B 56/60-118	Data matcher address tests Data matcher read/write tests
Phase 7, tests 1-19 | tests 20-43 Phase 7, tests 101-119	UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118	Event counter read/write tests Memory address counter read/write tests Event and transfer trace counters read/write tests
Phase 8, tests 1-5 | tests 6-21 | tests 101-108 Phase 8, tests 109, 124	UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118	Trace memory access tests UID buffers select and read/write tests Transfer trace buffer access paths tests UID buffers select and read/write tests
Phase 9, tests 1-61 | tests 101-117 Phase 9, tests 118-179	UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118	Trace memory read/write tests Transfer trace address tests Transfer trace buffer read/write tests
Phase 10, tests 1-10 tests 11-30 tests 31-33 tests 34-35 tests 36-43 tests 101-115 tests 116-135 tests 136-138 tests 139-140 Phase 10, tests 141-148	UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118 UN21B/61B 56/60-118	Trigger function tests Trigger function interrupt tests Trigger function condition matcher selection tests Trigger function select event counter tests Trigger function and together tests Trigger functions and UID results buffer tests Trigger functions interrupt tests Trigger function condition matcher selection tests Trigger function select event counter tests Trigger function and together tests
Phase 11, tests 1-32	UN21B/61B 56/60-118	Block matcher adder tests

CLEAR UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES

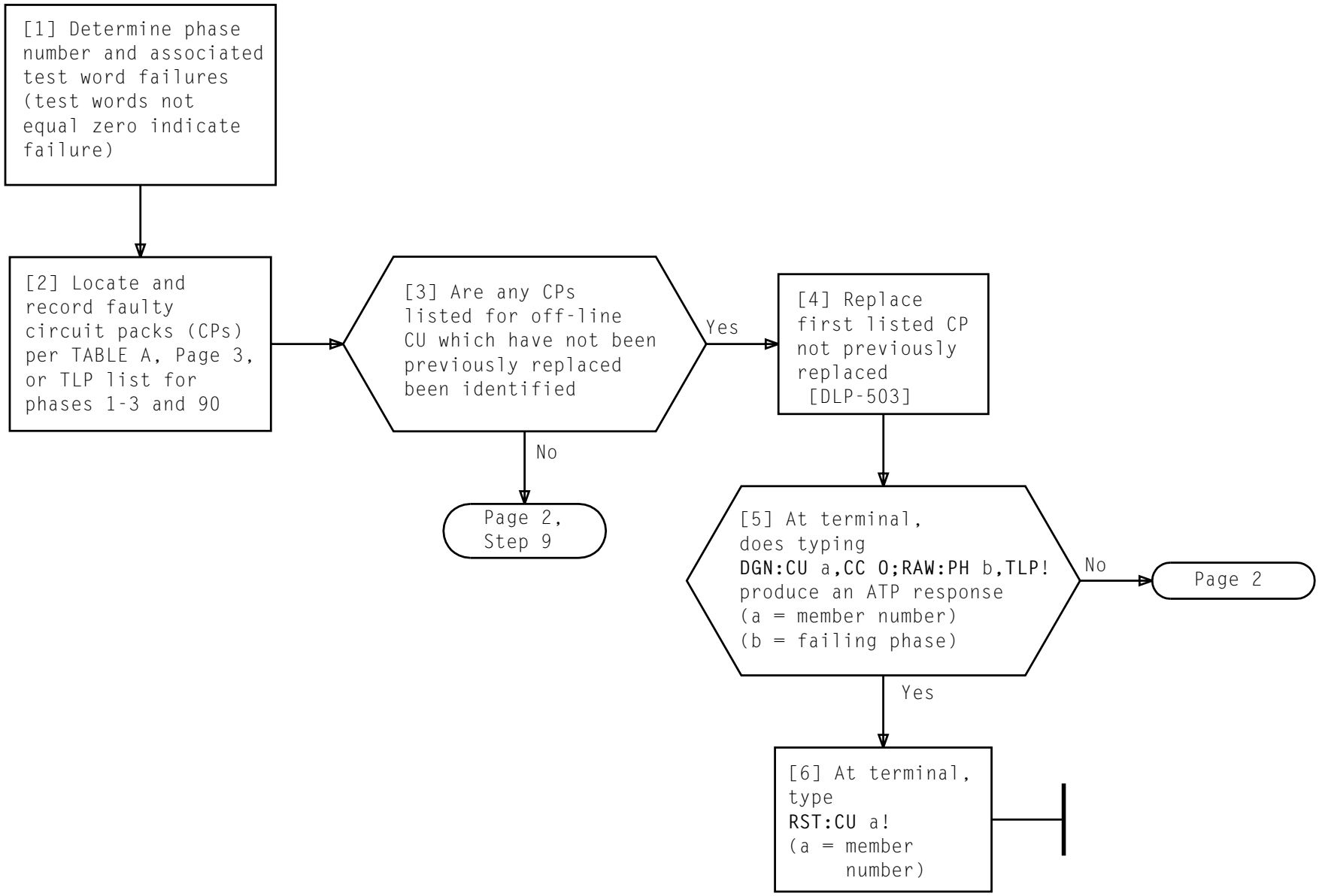
TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 12, tests 1-10	UN21B/61B 56/60-118	Triger function active flip-flop tests
tests 11-13	UN21B/61B 56/60-118	Instruction timing trigger function tests
tests 14-18	UN21B/61B 56/60-118	Stop match on full word and half word boundary operational codes tests
tests 19-23	UN21B/61B 56/60-118	Trigger function 0 block mode tests
tests 101-110	UN21B/61B 56/60-118	Trigger function active flip-flop tests
tests 111-113	UN21B/61B 56/60-118	Instruction timing trigger function tests
tests 114-118	UN21B/61B 56/60-118	Stop match on full word and half word boundary operational codes tests
Phase 12, tests 119-122	UN21B/61B 56/60-118	Trigger function 0 block mode tests
Phase 13, tests 1-11	UN21B/61B 56/60-118; UN43C 56/60-104	Access matcher trigger function tests
Phase 14, tests 1-20	UN21B/61B 56/60-118; UN6B 56/60-098	Data matcher trigger function tests
Phase 15, tests 1-20	UN21B/61B 56/60-118; UN43C 56/60-104, UN45B 56/60-110	Address matcher virtual address trigger function tests
Phase 16, tests 1-20	UN21B/61B 56/60-118; UN43C 56/60-104, UN45B 56/60-110	Address matcher physical addressing trigger function tests
Phase 17, tests 1-20	UN21B/61B 56/60-118; UN43C 56/60-104, UN45B 56/60-110	Address matcher physical addressing trigger function tests
Phase 18, tests 1-6	UN21B/61B 56/60-118; UN2B 56/60-084	UID matcher physical addressing trigger function tests
Phase 19, tests 1-13	UN21B/61B 56/60-118	Trigger function 0 incrementing of event counter tests
tests 14-32	UN21B/61B 56/60-118	Trigger function start trace and trace stop features tests
tests 101-113	UN21B/61B 56/60-118	Trigger function 0 incrementing of event counter tests
Phase 19, tests 114-132	UN21B/61B 56/60-118	Trigger function start trace and trace stop features tests
Phase 20, tests 1-95	UN21B/61B 56/60-118	Transfer trace run mode tests
Phase 20, tests 101-141	UN21B/61B 56/60-118	Transfer trace run mode tests
Phase 90, tests 1-5	UN21B/61B 56/60-118	External output of trigger function 0 tests
Phase 91, tests 1-5	UN21B/61B 56/60-118	External output of trigger function 1 tests
Phase 92, tests 1-5	UN21B/61B 56/60-118	External output of trigger function 2 tests
Phase 93, tests 1-5	UN21B/61B 56/60-118	External output of trigger function 3 tests

CLEAR UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES

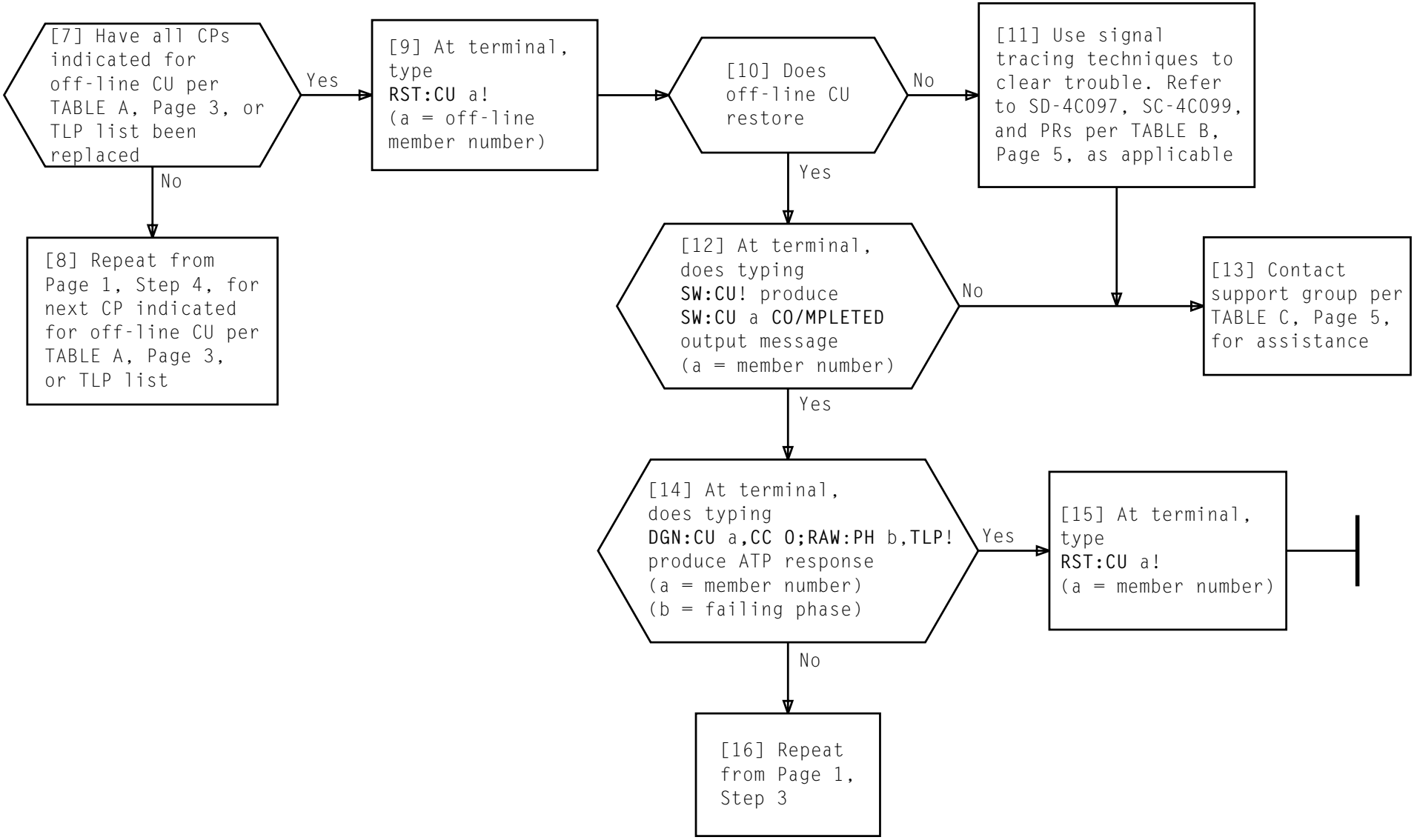
TABLE B			
PHASE NO.	PR NO.	PHASE NO.	PR NO.
1	4C52200	12	4C53300
2	300	13	400
3	400	14	500
4	500	15	600
5	600	16	700
6	700	17	800
7	800	18	4C53900
8	4C52900	90	4C54000
9	4C53000	91	100
10	100	92	200
11	4C53200	93	4C54300

TABLE C	
PRESENT SERVICE GROUP	NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES



CLEAR DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 90 FAILURES



CLEAR DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 90 FAILURES

TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, test 1	UN3B 56/60-092	No command test
test 2-4	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104	No command test
test 5	UN3B 56/60-092	No command test
test 7-9	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104; UN3B 56/60-092, UN2B 56/60-084	Test IOCLE and IOIDL commands
test 10-11	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104;	Test IOWCA command
test 12-15	UN2B 56/60-084; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 16	UN9B 38/42-88/96/104/112; UN9B 56/60-88/104; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
test 17-19	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104; UN3B 56/60-092; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 20	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104; UN2B 56/60-092; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 21-23	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
test 24-27	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104;	Test IORST and IOEACK commands
test 28	—	Test IORST and IOEACK commands
test 29	UN3B 56/60-092	Test IORST and IOEACK commands
test 30-33	—	Test IORINT and IOIACK commands
Phase 1, test 34-37	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104; UN2B 56/60-084	Test IORSR and IOSRACK commands
Phase 2, test 1-10	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104	Test operation code field in DSCH
test 11-13	UN3B 56/60-092; UN2B 56/60-084; UN1C 56/60-072;	FIFO tests
test 14	UN23C 56/60-078	FIFO tests
Phase 2, test 15-84	UN3B 56/60-092; UN2B 56/60-084	FIFO tests
Phase 3		Initialization
Phase 3, test 1-11		Write control/address register and read status register tests
test 12-13	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104	Induce sequencer error tests
test 14	UN9B 38/42-88/96/104/112; UN9B 56/60-80, 104;	Induce sequencer error tests
test 15	UN3B 56/60-092	Induce sequencer error tests
test 16-19		Induce sequencer error tests
test 20-28	UN3B 56/60-092; UN2B 56/60-084	Induce command error test
test 29-59		Induce device address error tests
Phase 3, test 60-80		Device address tests

CLEAR DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 90 FAILURES

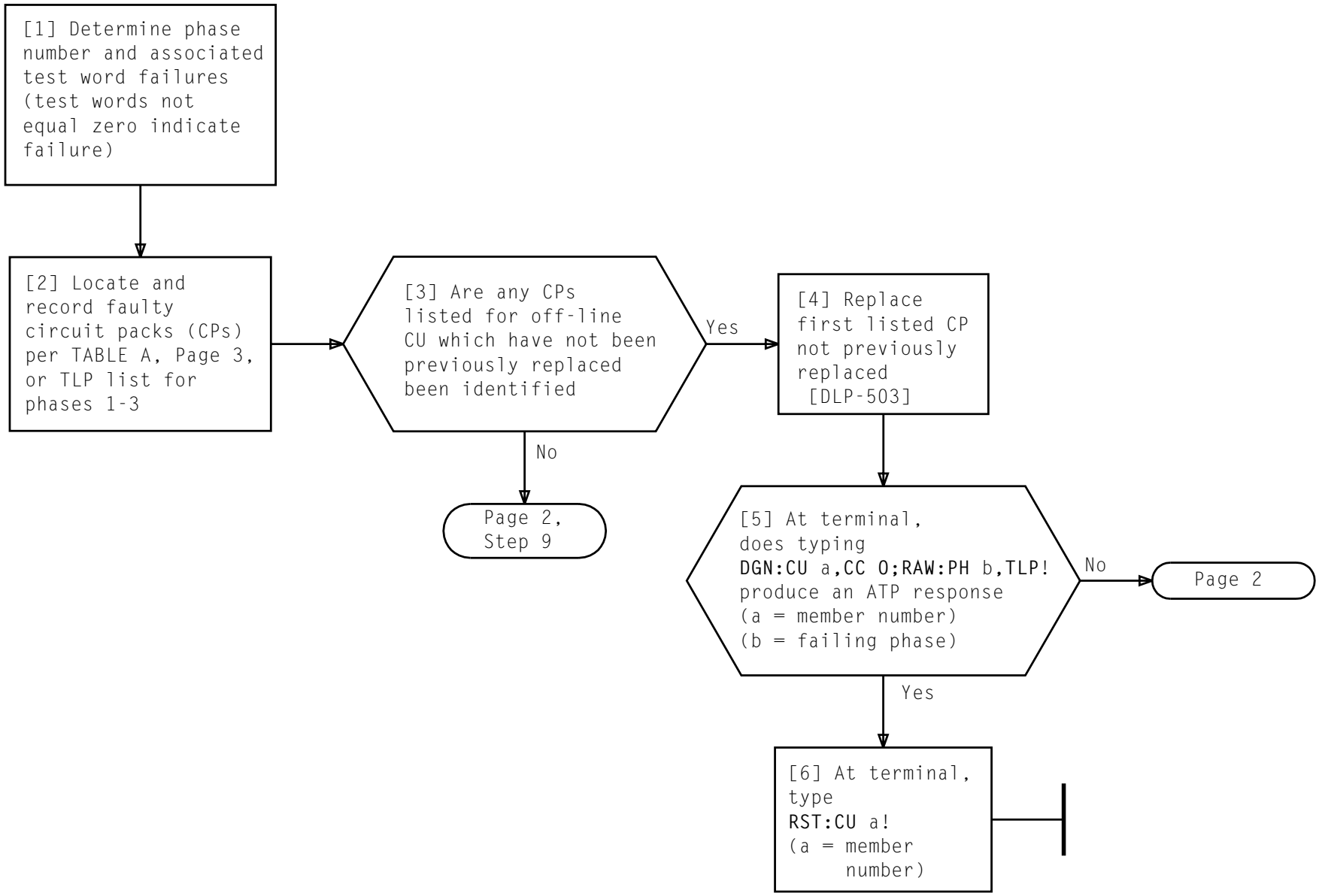
TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 90, test 1-100		Word transfer, CH 3/4, port device 0
test 401-500		Word transfer, CH 3/4, port device 1
test 801-900		Word transfer, CH 3/4, port device 2
test 1201-1300		Word transfer, CH 3/4, port device 3
test 1601-1700		Word transfer, CH 3/4, port device 4
test 2001-2100		Word transfer, CH 3/4, port device 5
test 2401-2500		Word transfer, CH 3/4, port device 6
test 2801-2900		Word transfer, CH 3/4, port device 7
test 3201-3300		Word transfer, CH 3/4, port device 8
test 3601-3700		Word transfer, CH 3/4, port device 9
test 4001-4100		Word transfer, CH 3/4, port device 10
test 4401-4500		Word transfer, CH 3/4, port device 11
test 4801-4900		Word transfer, CH 3/4, port device 12
test 5201-5300		Word transfer, CH 3/4, port device 13
test 5601-5700		Word transfer, CH 3/4, port device 14
test 6001-6100		Word transfer, CH 3/4, port device 15
test 101-200		Word transfer, CH 4/3, port device 0
test 501-600		Word transfer, CH 4/3, port device 1
test 901-1000		Word transfer, CH 4/3, port device 2
test 1301-1400		Word transfer, CH 4/3, port device 3
test 1701-1800		Word transfer, CH 4/3, port device 4
test 2101-2200		Word transfer, CH 4/3, port device 5
test 2501-2600		Word transfer, CH 4/3, port device 6
test 2901-3000		Word transfer, CH 4/3, port device 7
test 3301-3400		Word transfer, CH 4/3, port device 8
test 3701-3800		Word transfer, CH 4/3, port device 9
test 4101-4200		Word transfer, CH 4/3, port device 10
test 4501-4600		Word transfer, CH 4/3, port device 11
test 4901-5000		Word transfer, CH 4/3, port device 12
test 5301-5400		Word transfer, CH 4/3, port device 13
test 5701-5800		Word transfer, CH 4/3, port device 14
test 6101-6200		Word transfer, CH 4/3, port device 15
test 201-300		Block transfer, CH 3/4, port device 0
test 601-700		Block transfer, CH 3/4, port device 1
test 1001-1100		Block transfer, CH 3/4, port device 2
test 1401-1500		Block transfer, CH 3/4, port device 3
test 1801-1900		Block transfer, CH 3/4, port device 4
Phase 90, test 2201-2300		Block transfer, CH 3/4, port device 5

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 90, test 2601-2700		Block transfer, CH 3/4, port device 6
test 3001-3100		Block transfer, CH 3/4, port device 7
test 3401-3500		Block transfer, CH 3/4, port device 8
test 3801-3900		Block transfer, CH 3/4, port device 9
test 4201-4300		Block transfer, CH 3/4, port device 10
test 4601-4700		Block transfer, CH 3/4, port device 11
test 5001-5100		Block transfer, CH 3/4, port device 12
test 5401-5500		Block transfer, CH 3/4, port device 13
test 5801-5900		Block transfer, CH 3/4, port device 14
test 6201-6300		Block transfer, CH 3/4, port device 15
test 301-400		Block transfer, CH 4/3, port device 0
test 701-800		Block transfer, CH 4/3, port device 1
test 1101-1200		Block transfer, CH 4/3, port device 2
test 1501-1600		Block transfer, CH 4/3, port device 3
test 1901-2000		Block transfer, CH 4/3, port device 4
test 2301-2400		Block transfer, CH 4/3, port device 5
test 2701-2800		Block transfer, CH 4/3, port device 6
test 3101-3200		Block transfer, CH 4/3, port device 7
test 3501-3600		Block transfer, CH 4/3, port device 8
test 3901-4000		Block transfer, CH 4/3, port device 9
test 4301-4400		Block transfer, CH 4/3, port device 10
test 4701-4800		Block transfer, CH 4/3, port device 11
test 5101-5200		Block transfer, CH 4/3, port device 12
test 5501-5600		Block transfer, CH 4/3, port device 13
test 5901-6000		Block transfer, CH 4/3, port device 14
Phase 90, test 6301-6400		Block transfer, CH 4/3, port device 15

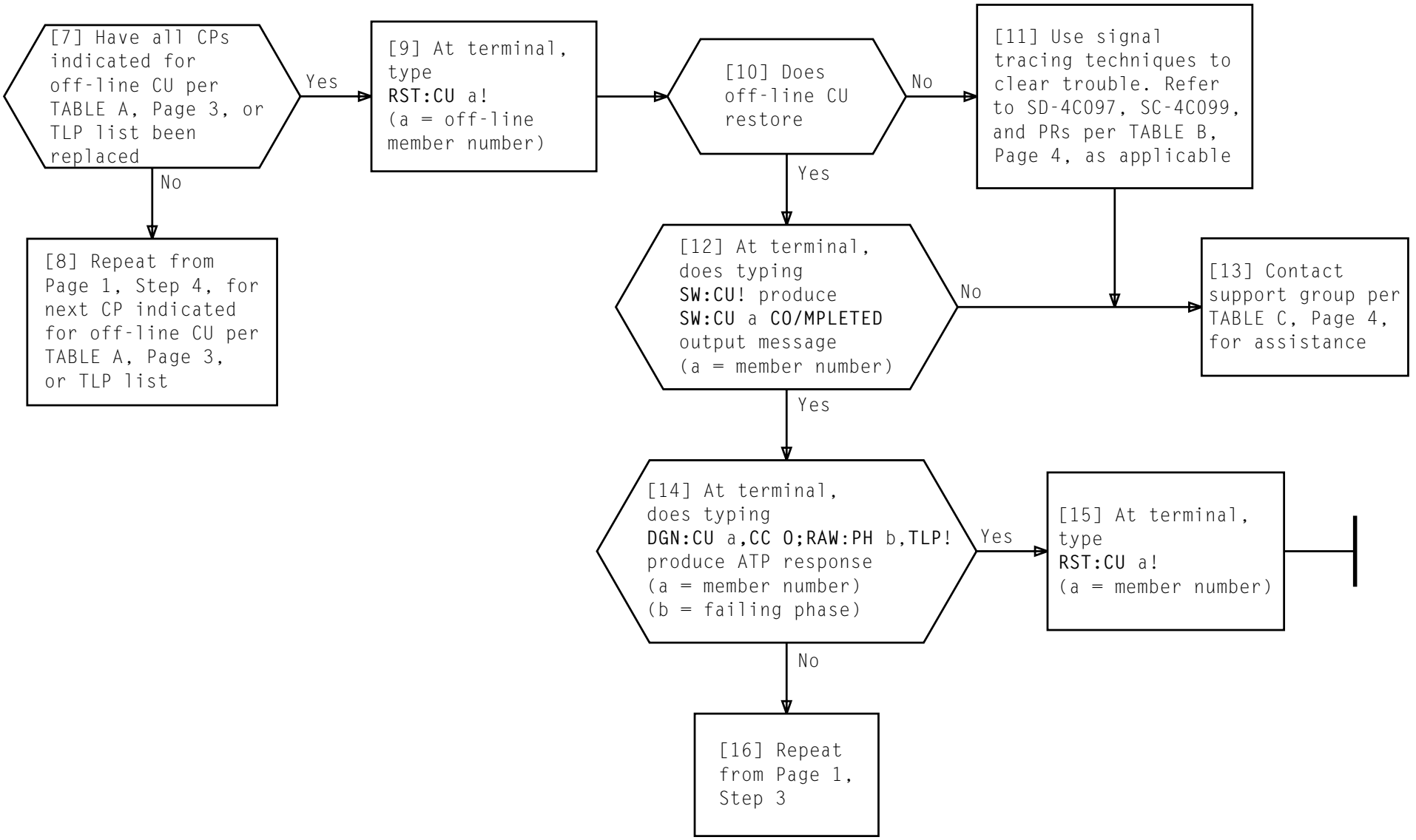
TABLE B	
PHASE NO.	**PR NO.**
	4C39500
1	600
2	700
3	800
90	4C39900

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

CLEAR DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 90 FAILURES



CLEAR APPLICATIONS CHANNELS INTERFACE (ACHI) PHASES 1-3 FAILURES

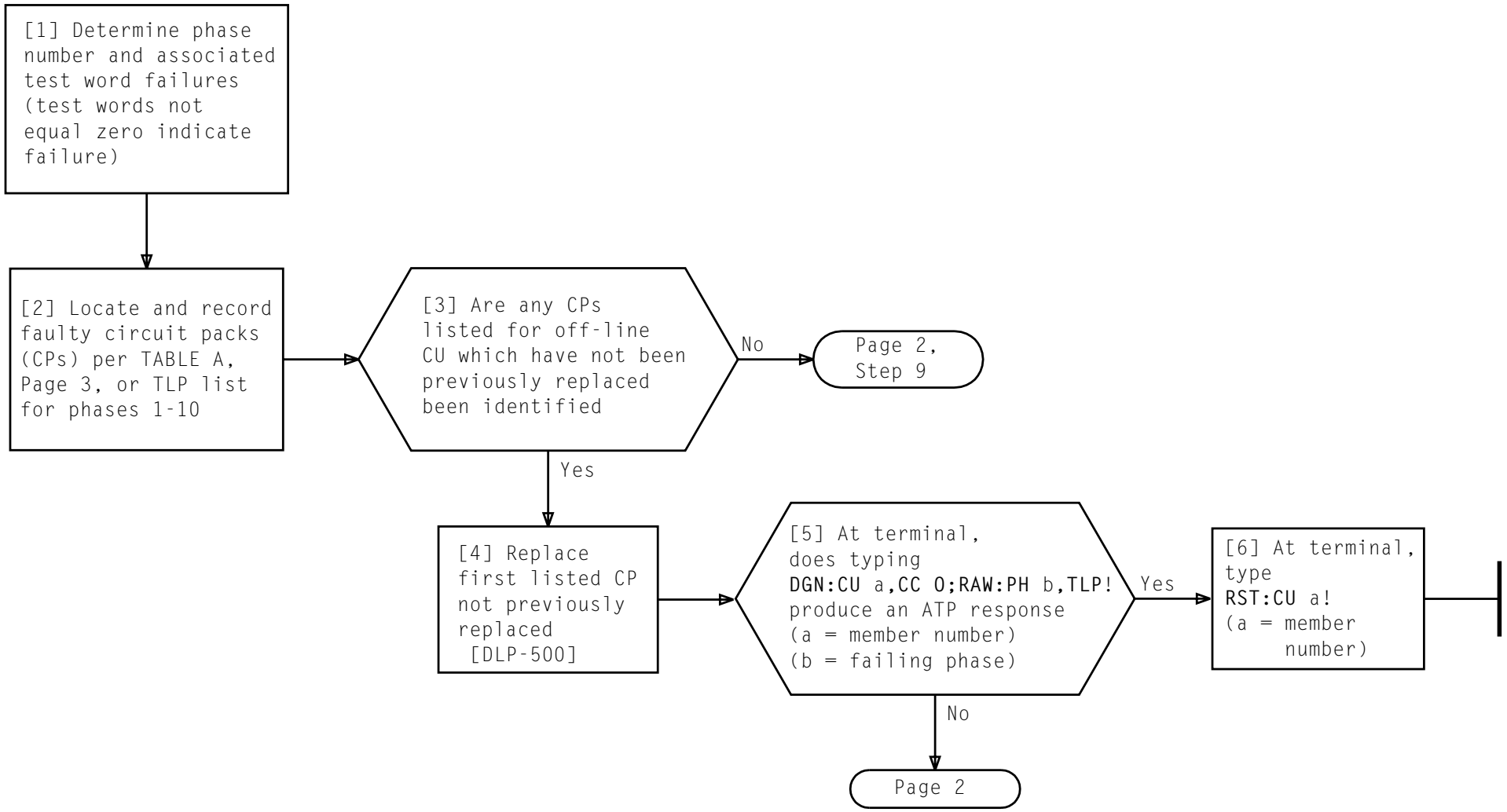


CLEAR APPLICATIONS CHANNELS INTERFACE (ACHI) PHASES 1-3 FAILURES

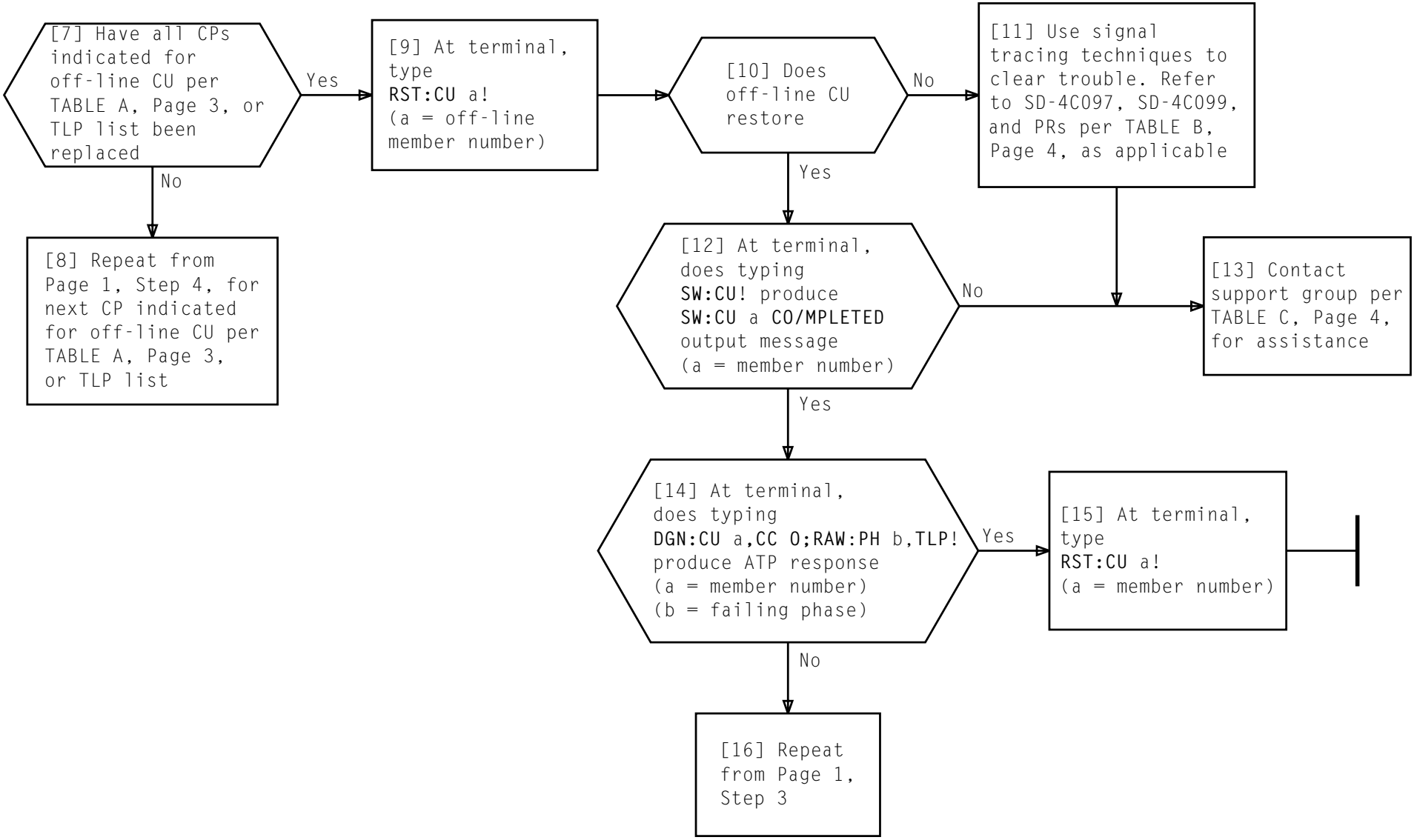
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, test 1	UN3B 56/60-092	No command test
test 2-4	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104	No command test
test 5	UN3B 56/60-092	No command test
test 6-9	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN3B 56/60-092, UN2B 56/60-084	Test IOCLE and IOIDL commands
test 10-11	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN2B 56/60-084	Test IOWCA command
test 12-15	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN2B 56/60-084; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 16	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
test 17-19	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN3B 56/60-092; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 20	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
Phase 1, test 21-23	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN3B 56/60-092; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
Phase 2, test 1-2	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104	Data loop-around
test 3	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104; UN2B 56/60-084; UN3B 56/60-092	Data loop-around
test 4-9	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104	Data loop-around
test 10	UN3B 56/60-092; UN2B 56/60-084; UN1C 56/60-072; UN23C 56/60-078	Data loop-around
test 11	UN2B 56/60-084; UN3B 56/60-092	Data loop-around
Phase 2, test 12-71	UN19B 38/42-88/96/104//112; UN19B 56/60-80/104	Data loop-around
Phase 3	UN19B 38/42-88/96/104/112; UN19B 56/60-80, 104	Initialization
, test 1-2	UN3B 56/60-092, UN19B 38/42-88, 96, 104, 112; UN19B 56/60-80, 104	OVRINHIO FF, INHIO, and CH error test
test 3-4	UN19B 38/42-80, 104	OVRINHIO FF, INHIO, and CH error test
test 5	UN19B 38/42-88, 96, 104, 112; UN19B 56/60-80, 104	OVRINHIO FF, INHIO, and CH error test
test 6	UN19B 38/42-88, 96, 104, 112; UN19B 56/60-80, 104; UN3B 56/60-092	OVRINHIO FF, INHIO, and CH error test
test 7	UN3B 56/60-092, UN2B 56/60-084	OVRINHIO FF, INHIO, and CH error test
test 8-13		
test 14-21		Service request test
test 22-29		Interrupt tests
Phase 3, test 30-31	UN19B 38/42-88, 96, 104, 112; UN19B 56/60-80, 104	Maintenance 2 FF tests

TABLE B	
PHASE NO.	**PR NO.**
1	4C27500
2	600
3	4C27700

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs



CLEAR DIRECT MEMORY ACCESS CONTROLLERS (DMAC) PHASES 1-10 FAILURES



CLEAR DIRECT MEMORY ACCESS CONTROLLERS (DMAC) PHASES 1-10 FAILURES

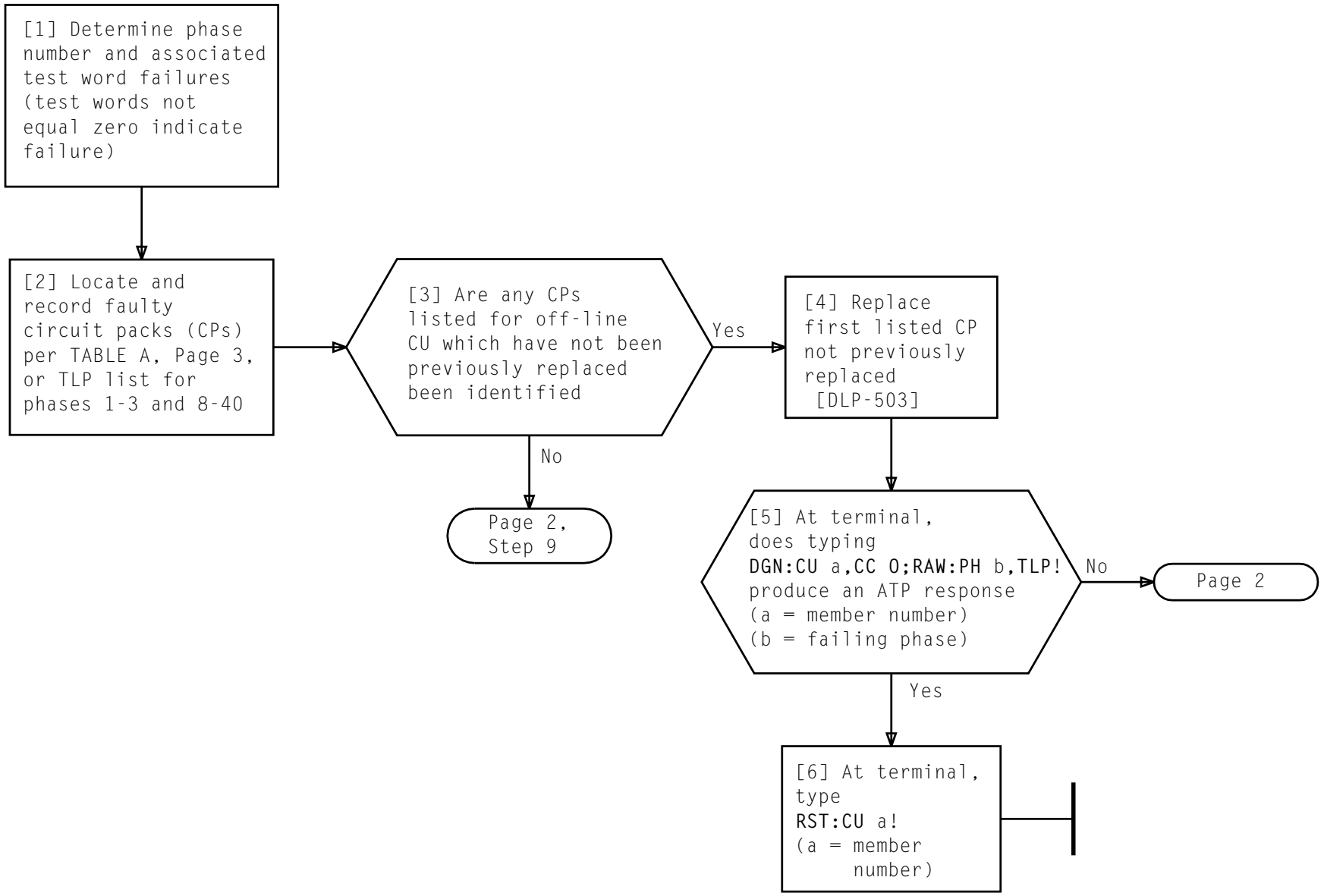
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, test 1	UN3B 56/60-092	No command test
test 2-4	UN46 47/51-088; UN3B 56/60-092; UN2B 56/60-084	No command test
test 5	UN3B 56/60-092	No command test
test 6-9	UN46 47/51-088; UN3B 56/60-092; UN2B 56/60-084	Test IOCLE and IOIDL commands
test 10-11	UN46 47/51-088; UN2B 56/60-084; UN45B 56/60-110	Test IOWCA command
test 12-15	UN46 47/51-088; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
test 16	UN46 47/51-88, 096; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
test 17-19	UN46 47/51-88, 096; UN3B 56/60-092; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 20	UN46 47/51-88, 096; UN2B 56/60-084	Test IOWD and IORD commands, CCIO bus data and parity leads
test 21-23	UN46 47/51-88, 96; UN3B 56/60-092; UN45B 56/60-110	Test IOWD and IORD commands, CCIO bus data and parity leads
test 24-27	UN46 47/51-088; UN2B 56/60-084	Test IORST and IOEACK commands
test 28	UN46 47/51-088, 96	Test IORST and IOEACK commands
test 29	UN3B 56/60-092	Test IORINT and IOIACK commands
test 30-33	UN46 47/51-088, 096; UN3B 56/60-092; UN2B 56/60-084	Test IORSR and IOSRACK commands
test 34-37	UN46 47/51-088, UN2B 56/60-084	Test IORSR and IOSRACK commands
test 38-53	UN46 47/51-088; 096	Test DMA response to its CH addresses
Phase 1, test 54-65	UN46 47/51-088, 096	
Phase 2, test 1	UN3B 56/60-092; UN2B 56/60-084; UN46 47/51-088	Read status tests
test 2	UN46 47/51-088, 096	Read status tests
test 3-7	UN46 47/51-088, 096	Read status tests
test 8-27	UN46 47/51-088, 096	Read status tests
test 28-32	UN46 47/51-088, 096	Read status tests
Phase 2, test 33-51	UN46 47/51-088, 096	Read status tests
Phase 3, test 1-143	UN46 47/51-088, 096	DMA internal register write and read tests
Phase 3, test 144-1175	UN46 47/51-088, 096	DAM RAM write and read tests
Phase 4, test 1-9	UN46 47/51-088	Operational mode tests
test 10-75	UN46 47/51-088	Maintenance mode tests
Phase 4, 76-139	UN46 47/51-088	Maintenance mode tests

CLEAR DIRECT MEMORY ACCESS CONTROLLERS (DMAC) PHASES 1-10 FAILURES

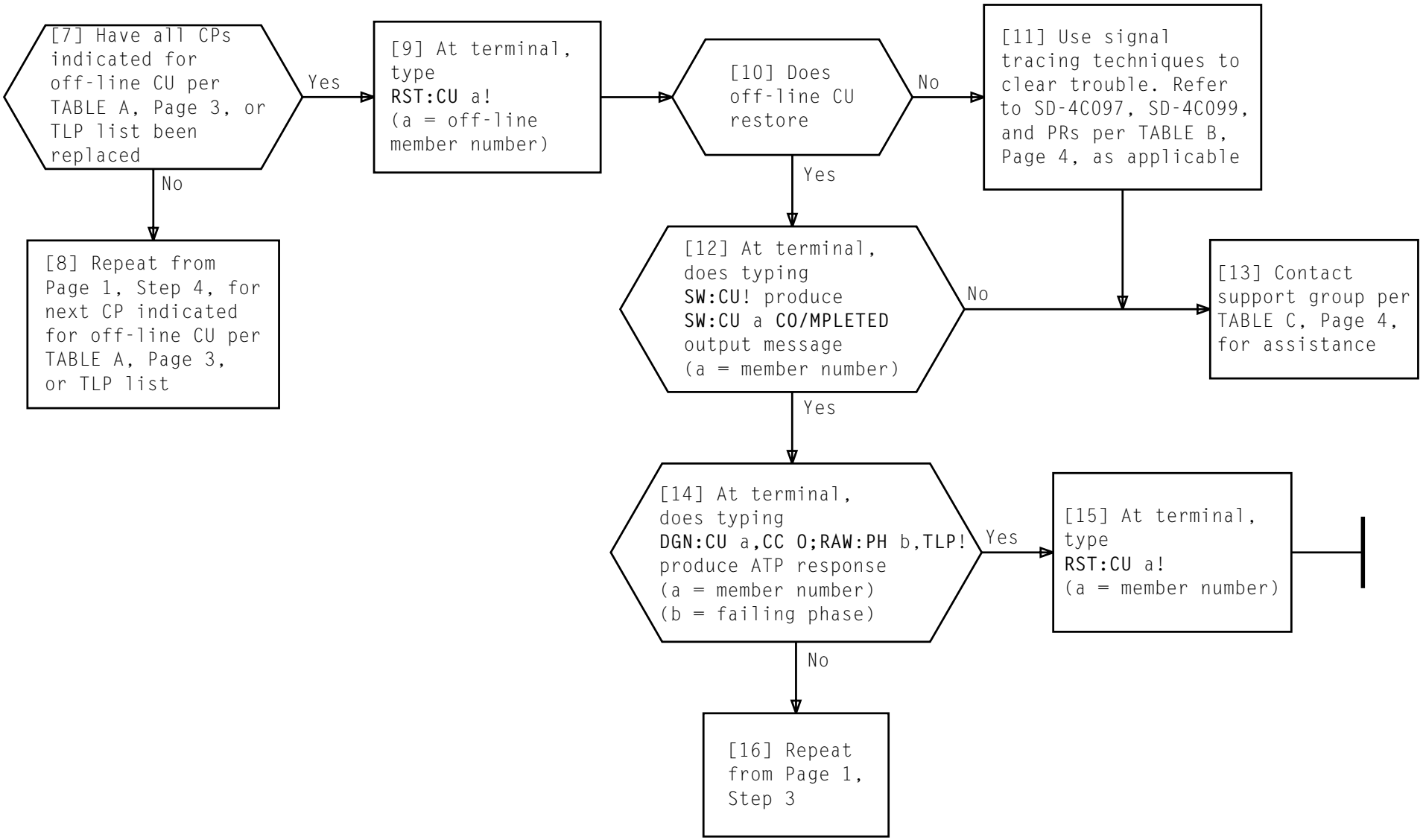
TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 5, test 1-35	UN46 47/51-088	Priority circuit tests
Phase 6, 1-159	UN46 47/51-088	MAS address loop-around
Phase 7, test 1-36 ¦ test 37-73 Phase 7, test 74-79	UN46 47/51-088, 096; UN133 56/60-146 UN46 47/51-088 UN46 47/51-088	Read data from mainstore Write data to mainstore Read and clear of mainstore tests
Phase 8, test 1-22 ¦ test 23-47 ¦ test 101-113 ¦ test 114-155 Phase 8, test 201-261	UN46 47/51-088 UN46 47/51-088 UN46 47/51-088; UN9B 47/51-80, 104 UN46 47/51-088	Mainstore error tests Internal error tests RAM parity checking tests DIO interface tests Channel status register tests
Phase 9, test 1-154	UN10B 56/60-124 (on-line); UN133 56/60-146, UN11B 56/60-138; UN46 47/51-088	Cache tag invalidation test
Phase 10, test 1-154	UN10B 56/60-124, UN133 56/60-146; UN46 47/51-088	Cache tag invalidation test

TABLE B	
PHASE NO.	**PR NO.**
1	4C37950
2	4C38050
3	¦ 150
4	¦ 250
5	¦ 350
6	¦ 450
7	¦ 550
8	¦ 650
9	¦ 750
10	4C38850

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs



CLEAR DIRECT MEMORY ACCESS (DMCH) DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 8-40 FAILURES



CLEAR DIRECT MEMORY ACCESS (DMCH) DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 8-40 FAILURES

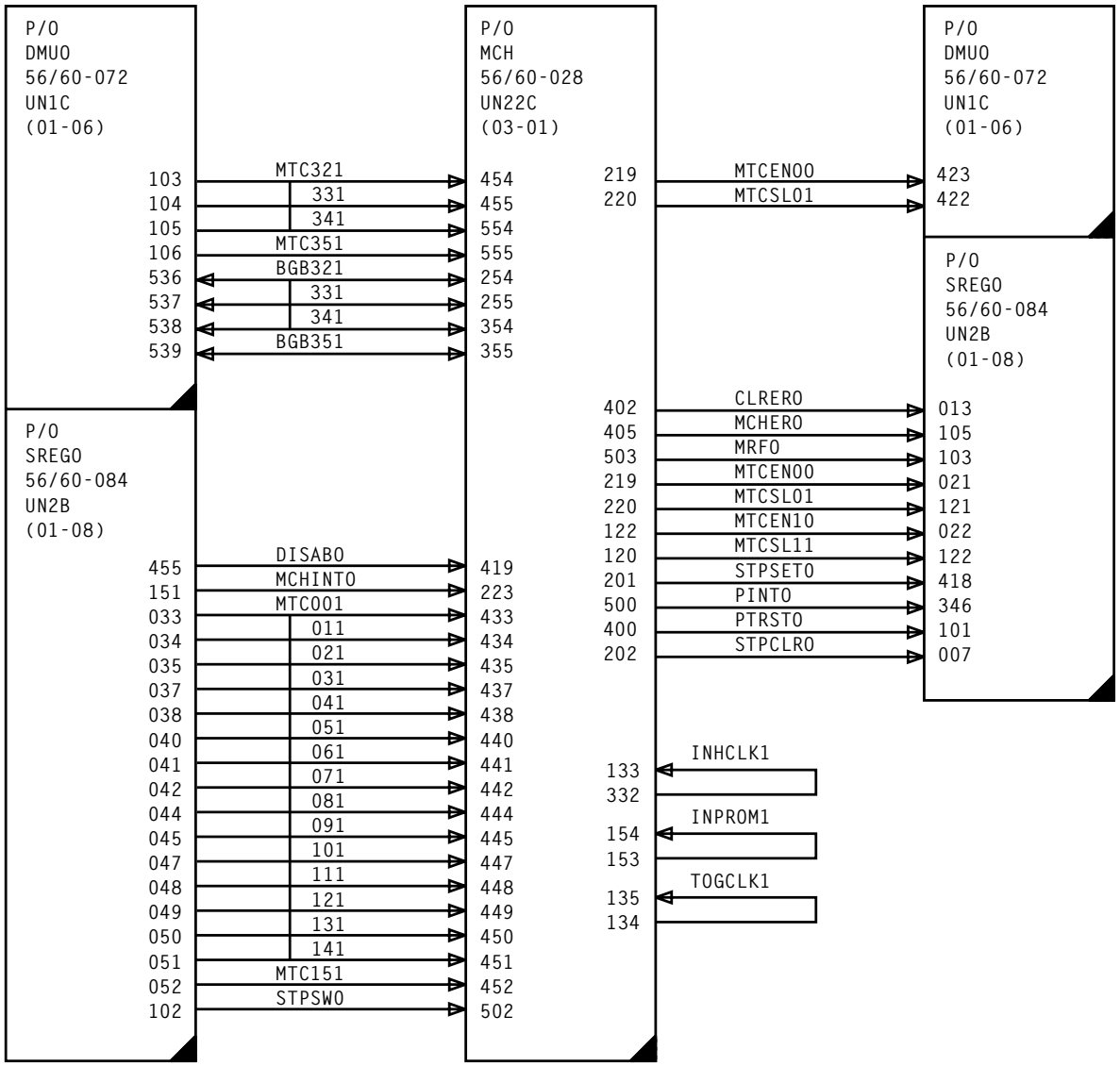
TABLE A		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 1, test 2-4	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Addressing tests
¦ test 5-13	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	DIOWD and DIORD command leads, DIO bus data leads
Phase 1, test 14-39	UN46 47/51-088, 96; UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	DIO data parity tests
Phase 2, test 1-10	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Test operation code field in DSCH
¦ test 11-13	UN3B 56/60-092; UN2B 56/60-084; UN1C 56/60-072; UN23C 56/60-078	FIFO tests
¦ test 14	UN2B 56/60-084; UN3B 56/60-092	FIFO tests
Phase 2, test 15-083	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	FIFO tests
Phase 3, test 1-11	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Initialization
¦ test 12-13	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Write control/address register and read status register tests
¦ test 14	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104; UN3B 56/60-092	Induce sequence error tests
¦ test 15	UN3B 56/60-092; UN2B 56/60-084	Induce sequence error tests
¦ test 16-19	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Induce sequence error tests
¦ test 20-29	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Induce sequence error tests
¦ test 30-60	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Induce device address error tests
Phase 3, test 61-81	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Device address tests
Phase 8-23, test 1-6	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Initialization and port under test nonselection test
Phase 8-23, test 7-18	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Test interrupts and service requests from DSCH to itself

TABLE A (Contd)		
PHASE AND TEST FAILURE	**SUSPECTED FAULTY CPs AND LOCATION IN REPLACEMENT ORDER**	**COMMENTS**
Phase 8-23, test 19-20 test 21-24 Phase 8-23, test 25-32	UN3B 56/60-092; UN9B 38/42-88, 96, 104, 112; UN9B 56/60 80-104 UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104	Test DSCH enabled if INHIO reset and Op-code clearing of interrupts and service requests Test masking, Op-code clear interrupts, and Op-code clear service requests
Phase 24-39, test 1-4 Phase 24-39, test 5-10	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104; TN69B 47/51-058 UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104; TN69B 47/51-058	Put D2SBS in maintenance mode and read status Loop data through D2SBS save register
Phase 40, test 1-10 test 11-40 test 41-73 test 74-119 test 101-174 Phase 40, test 201-308	UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104; TN69B 47/51-58 UN9B 38/42-88, 96, 104, 112; UN9B 56/60-80, 104; TN69B 47/51-58 TN69B 47/51-58; UN46 47/51-88; UN9B 38/42-88, 96, 104, 112 UN46 47/51-88; UN9B 38/42-88, 96, 104, 112 UN46 47/51-88, 96; UN9B 38/42-88, 96, 104, 112 UN46 47/51-88, 96; UN9B 38/42-88, 96, 104, 112	Test access to DDSBS Loop data through DDSBS save register Test interrupts and serivce requests from DDSBS to DSCH Word transfer tests Block transfer tests Expand device block transfer tests

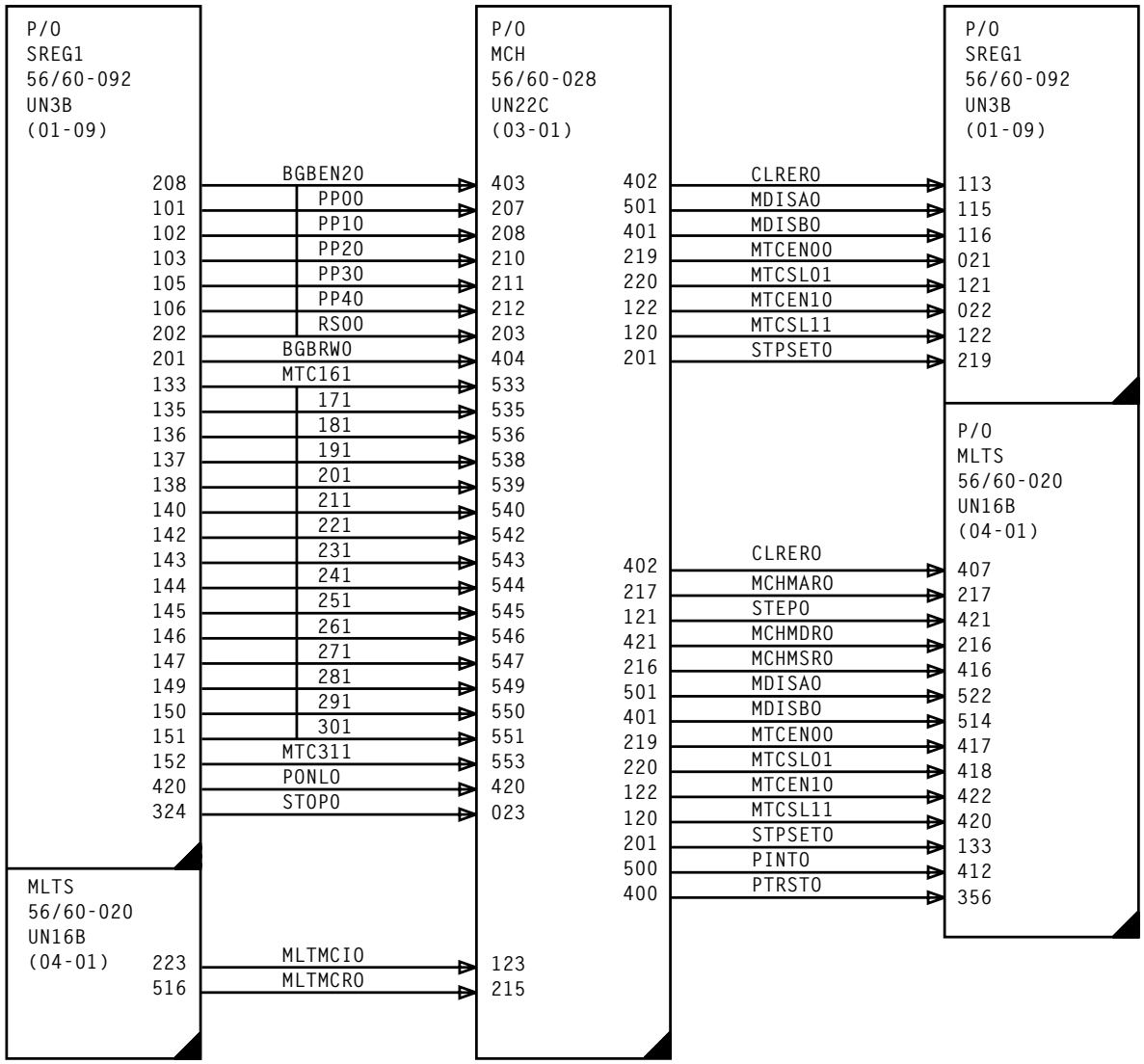
TABLE B	
PHASE NO.	**PR NO.**
1	4C38950
2	4C39050
3	150
8-23	250
24-39	350
40	4C39450

TABLE C	
PRESENT SERVICE GROUP	**NEXT LEVEL OF SERVICE HIERARCHY TO CONTACT**
Local craft	SCCS
SCCS	ESAC
ESAC	RTAC
RTAC	PECC
PECC	Bell Labs

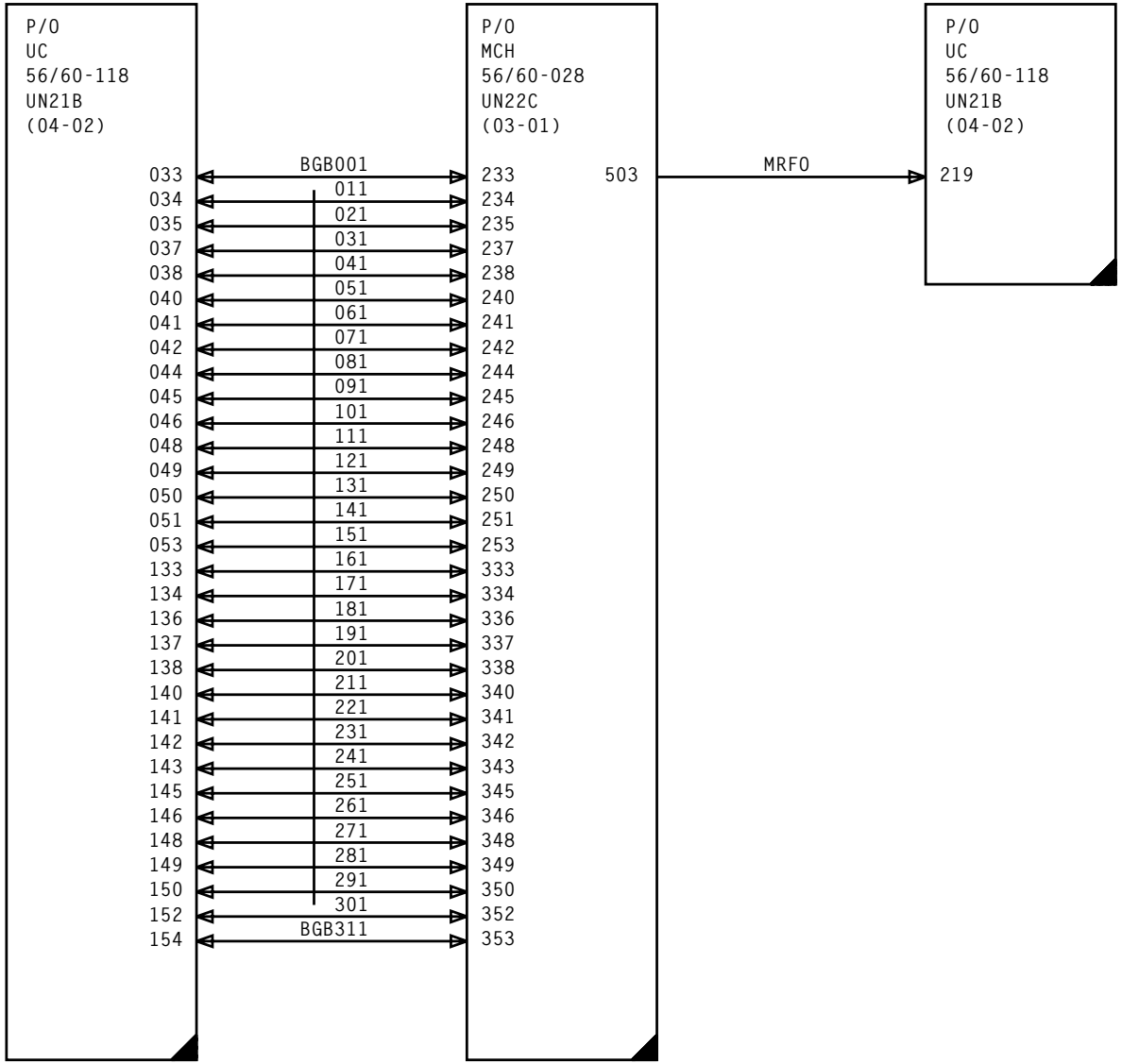
CLEAR DIRECT MEMORY ACCESS (DMCH) DUAL SERIAL CHANNELS (DSCH) PHASES 1-3 AND 8-40 FAILURES



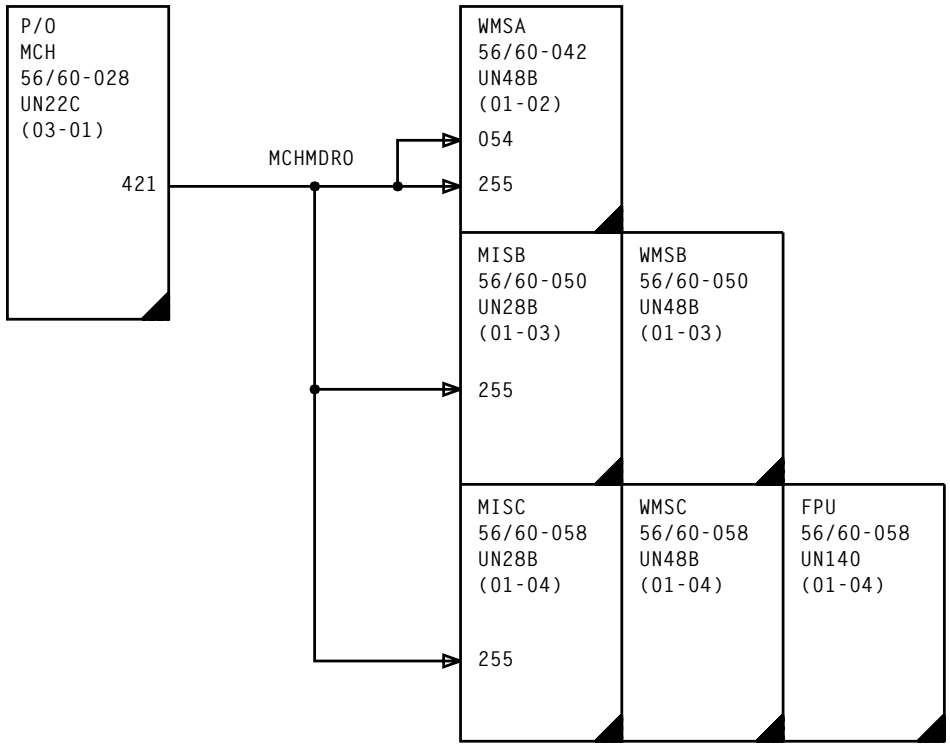
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



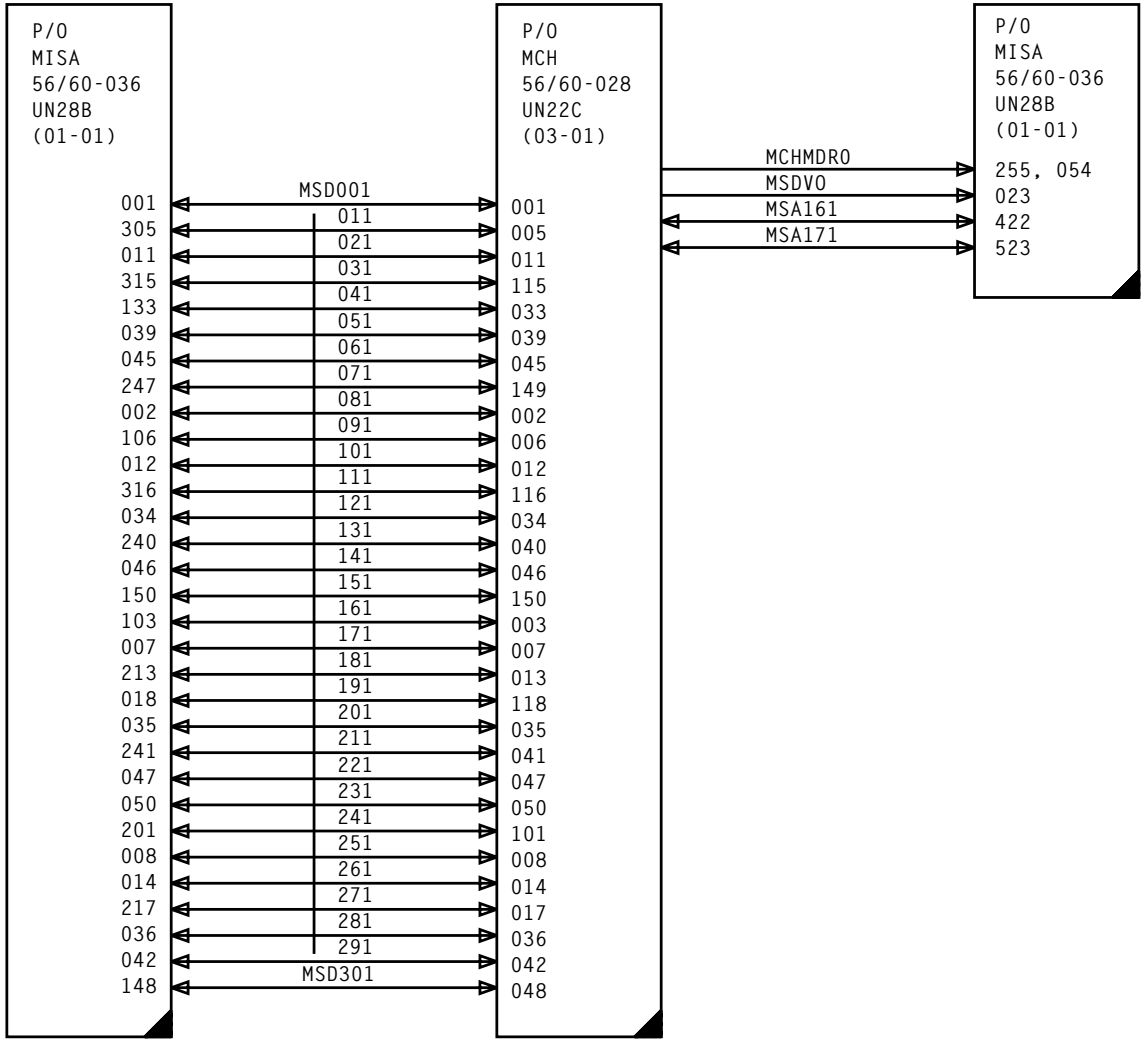
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



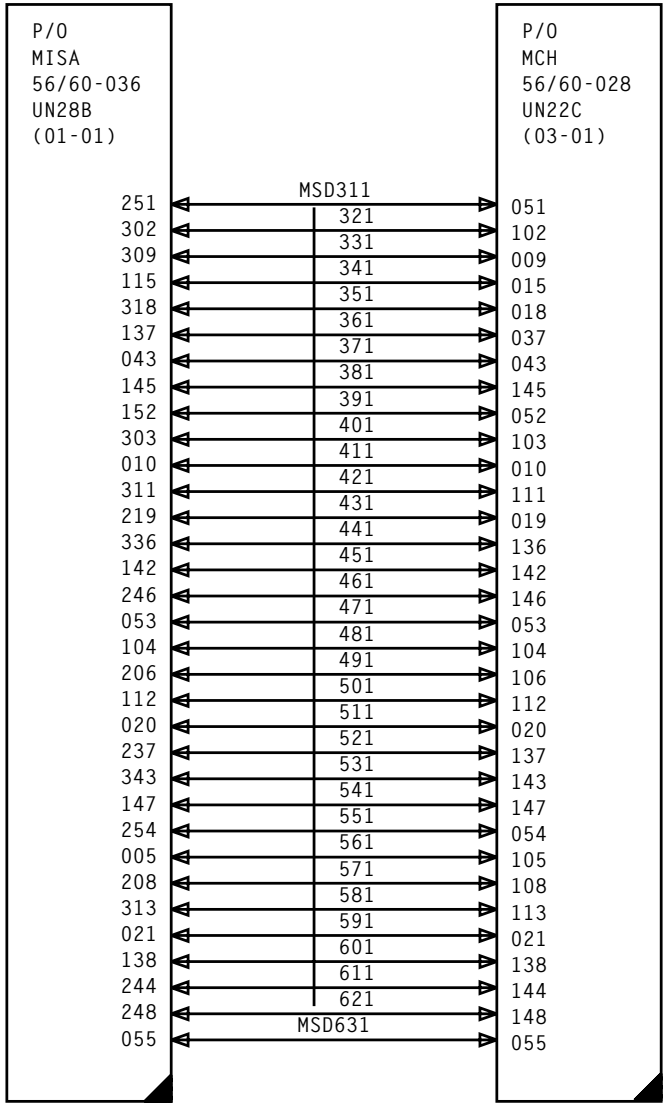
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



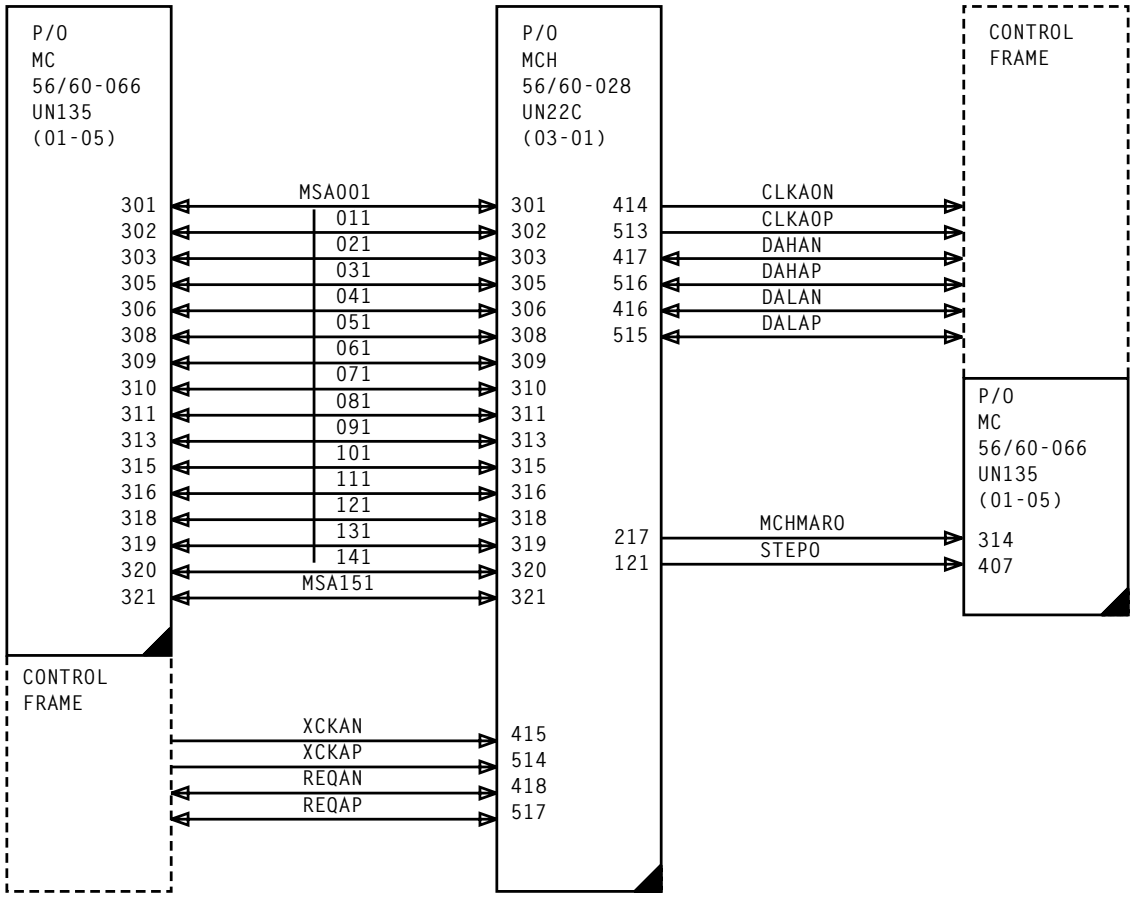
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



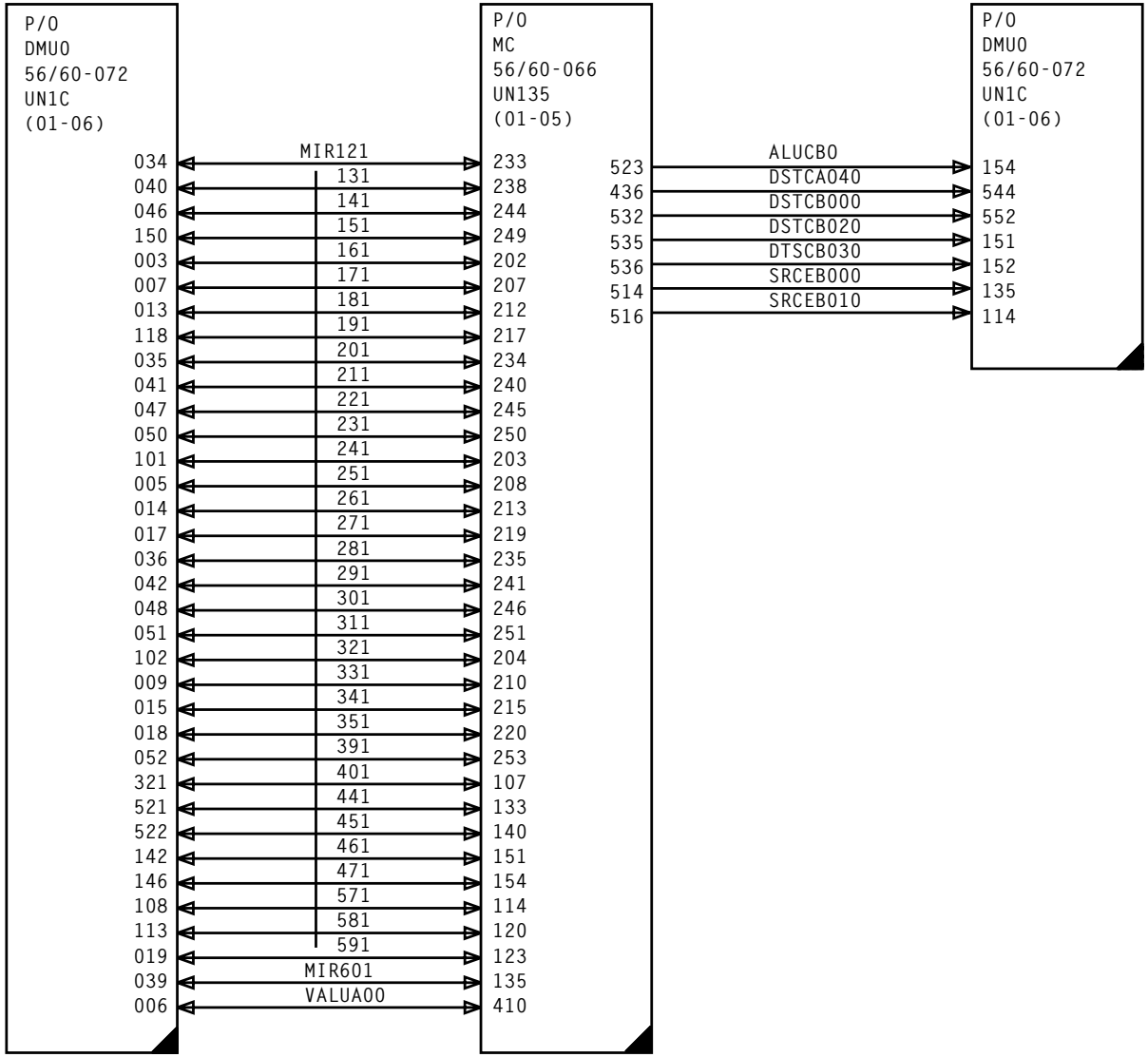
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



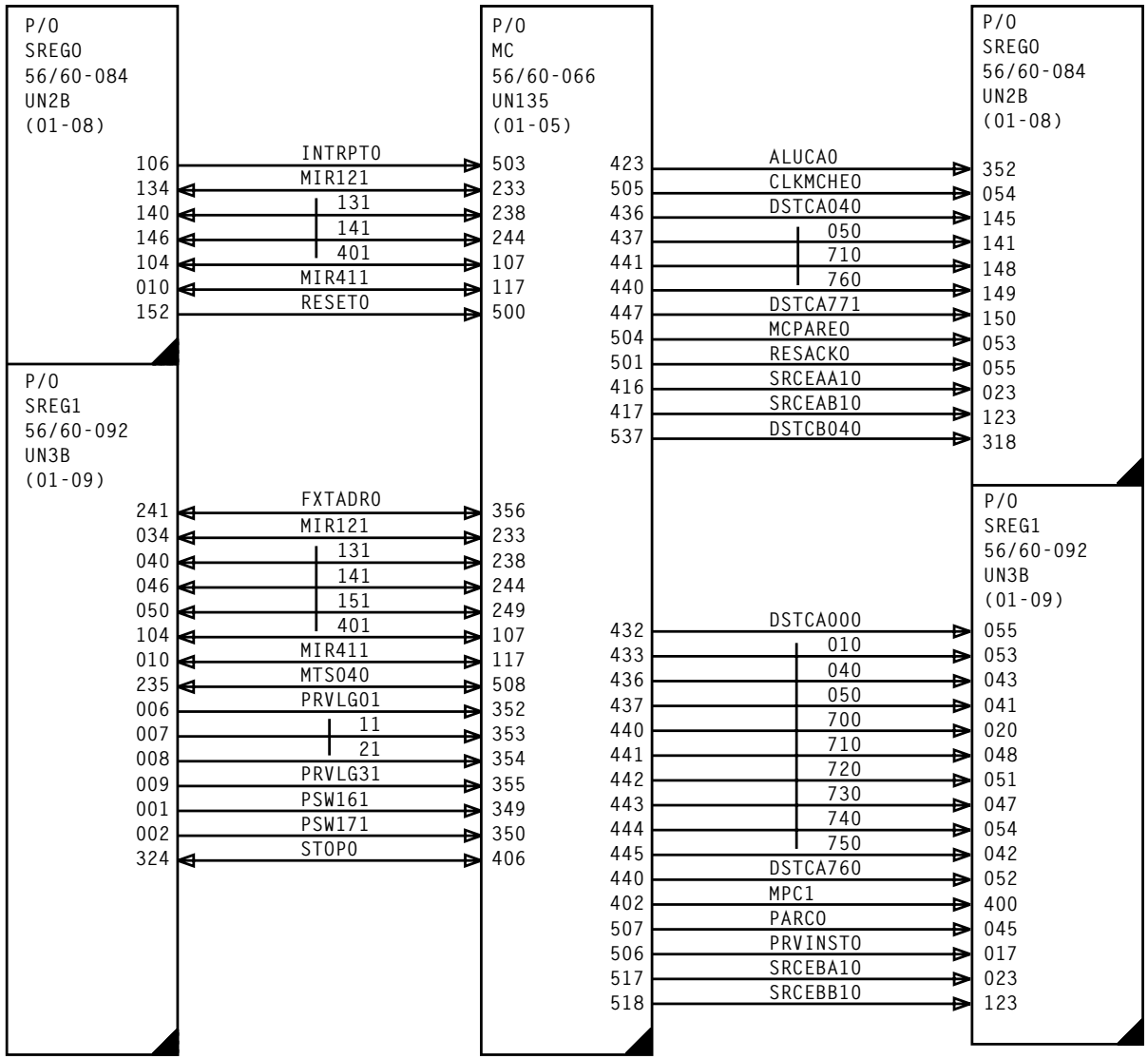
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



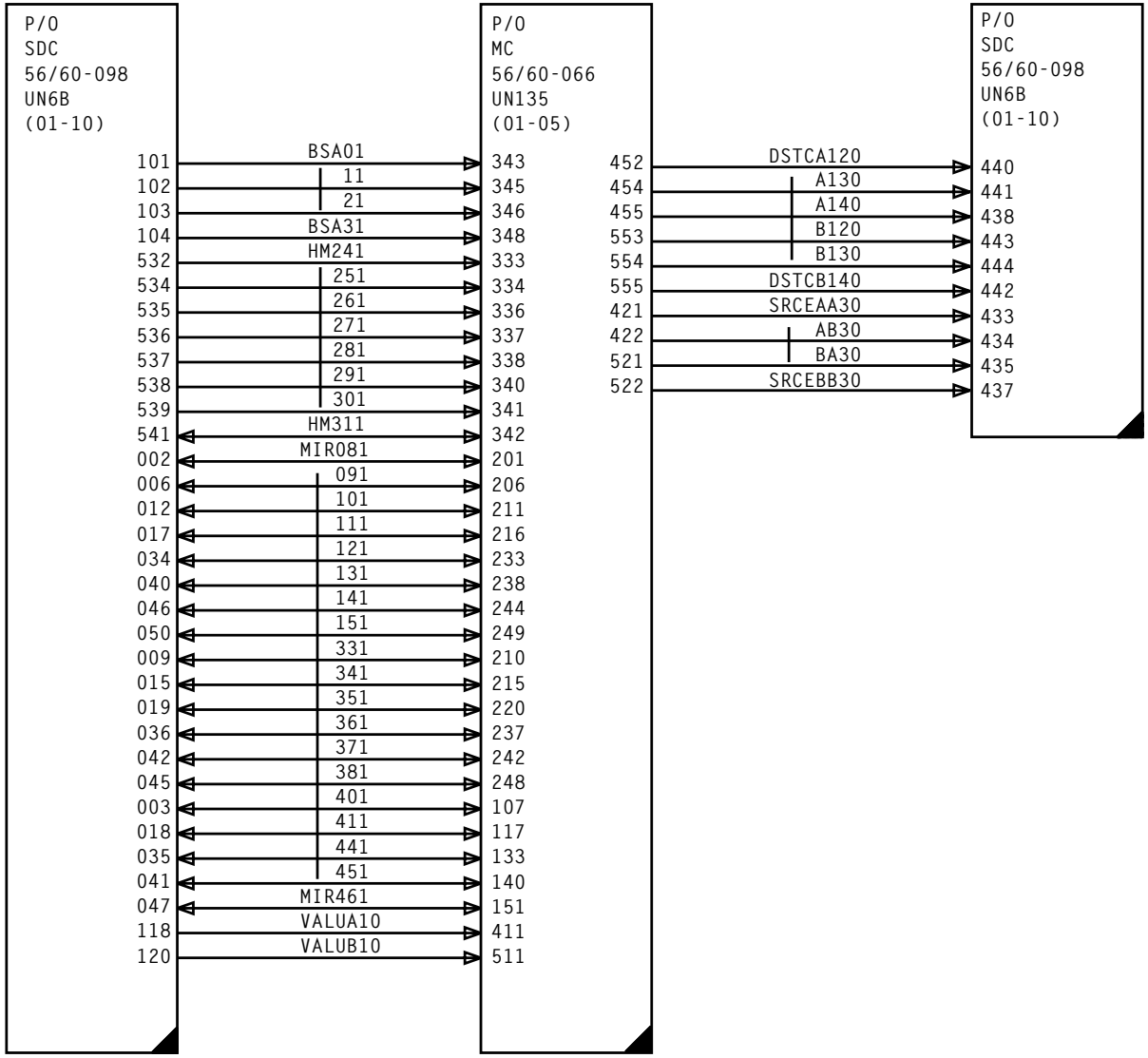
CENTRAL CONTROL (CC) PHASES 1-4 AND 62
MAINTENANCE CHANNEL (MCH) FAILURES



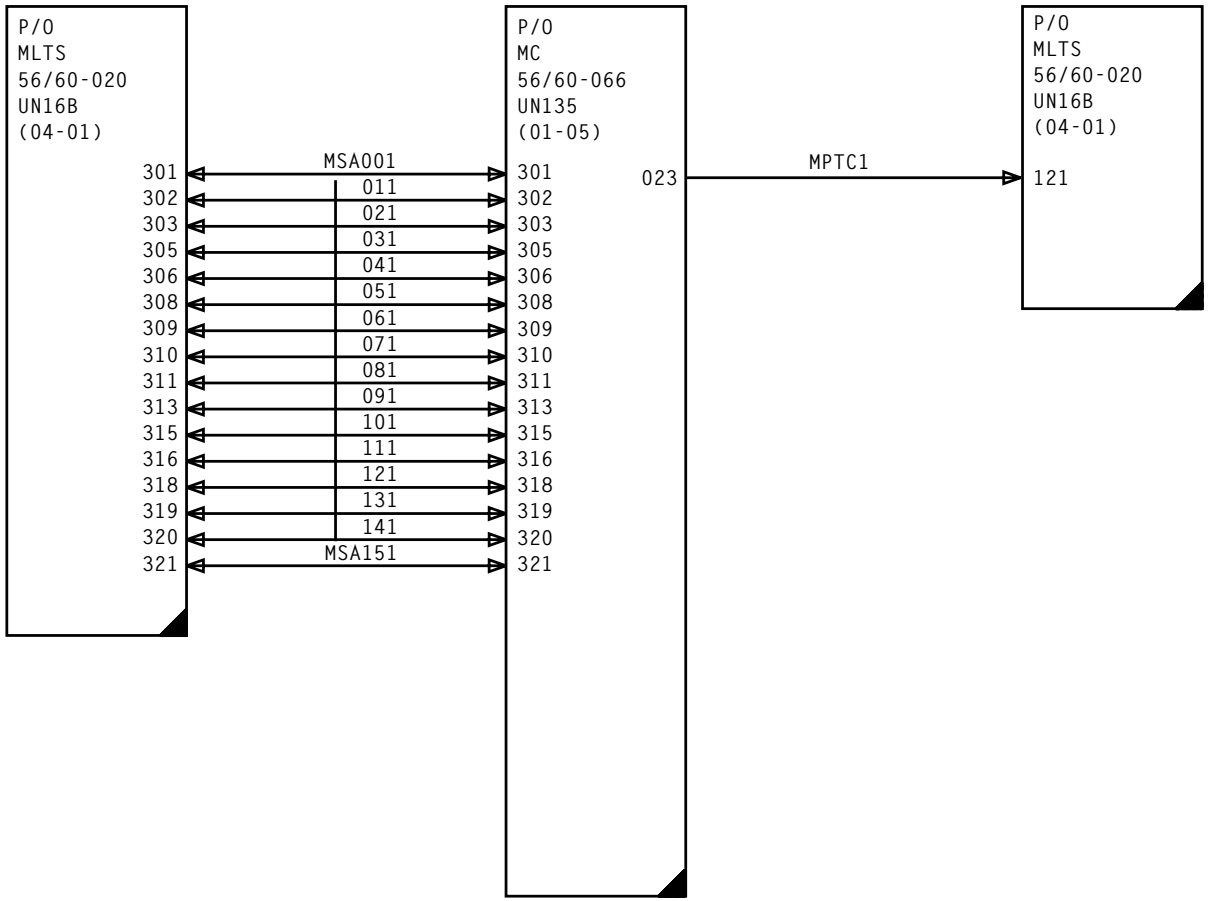
CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCONTROL (MC) FAILURES



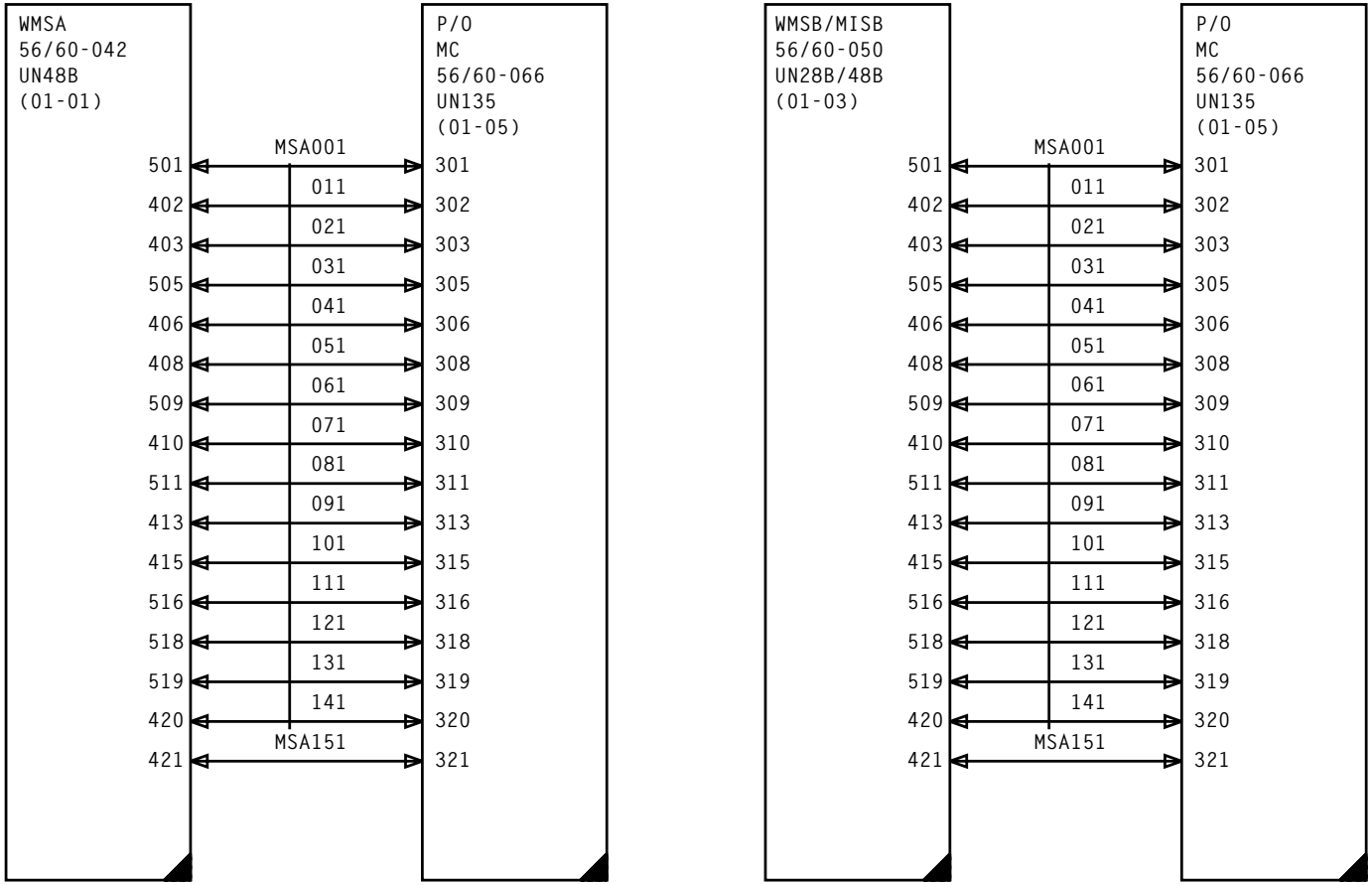
CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28
MICROCONTROL (MC) FAILURES



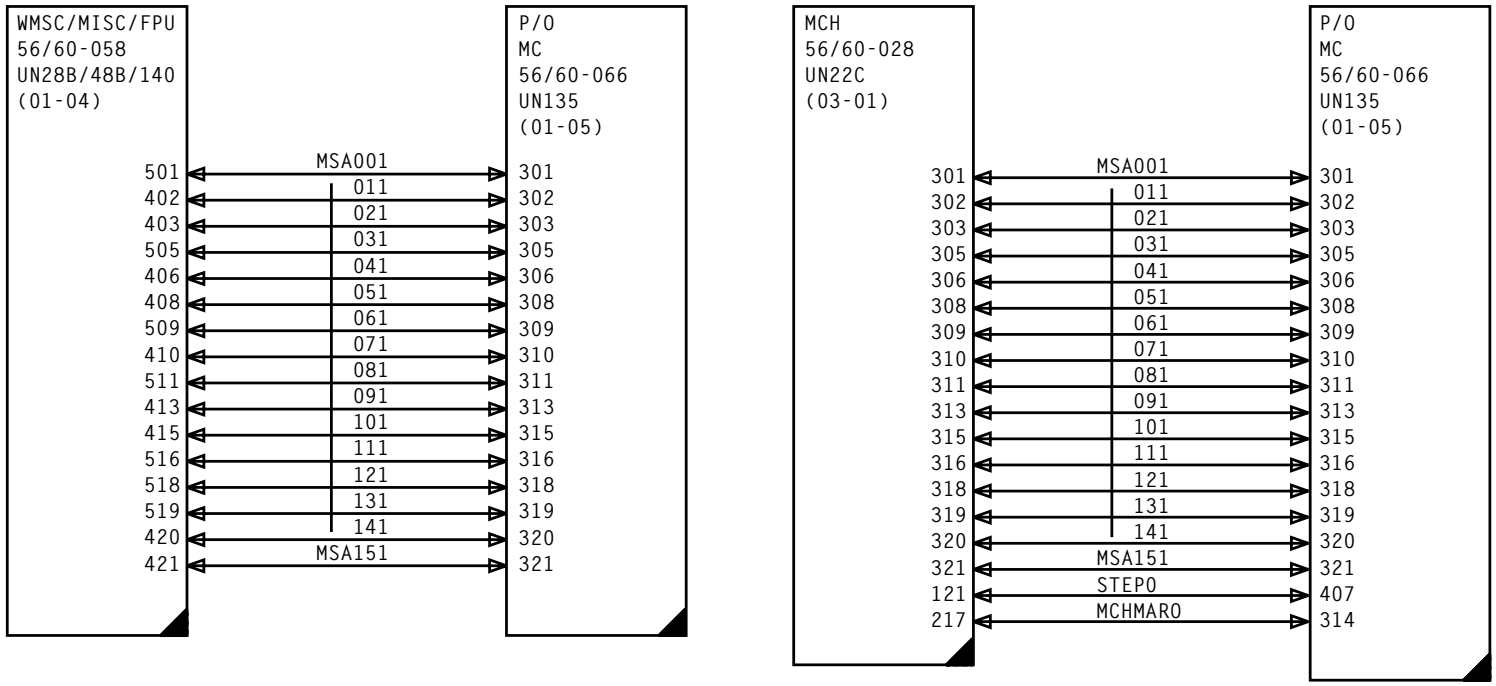
CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28
MICROCONTROL (MC) FAILURES



CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28
MICROCONTROL (MC) FAILURES



CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28
MICROCONTROL (MC) FAILURES



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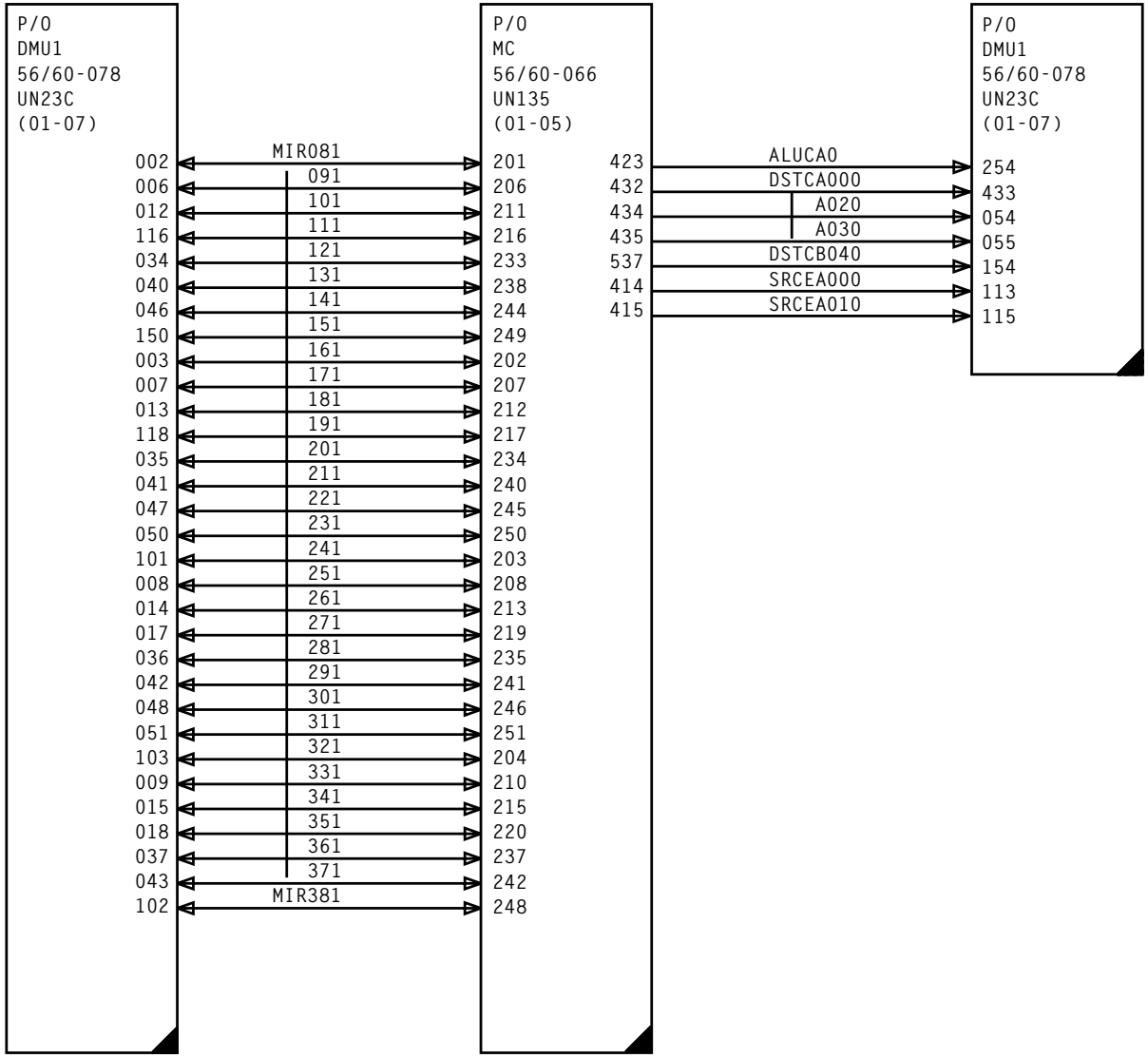
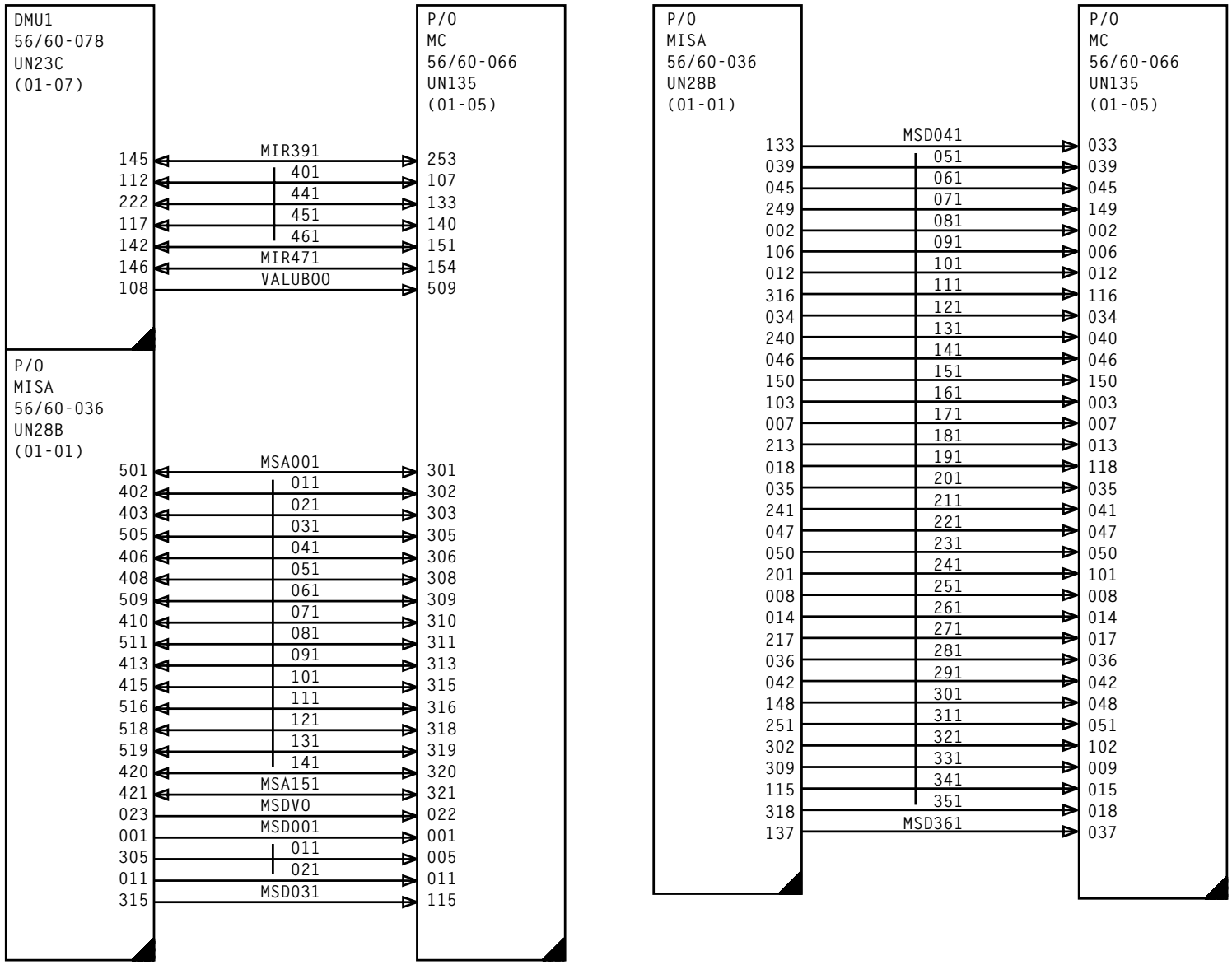
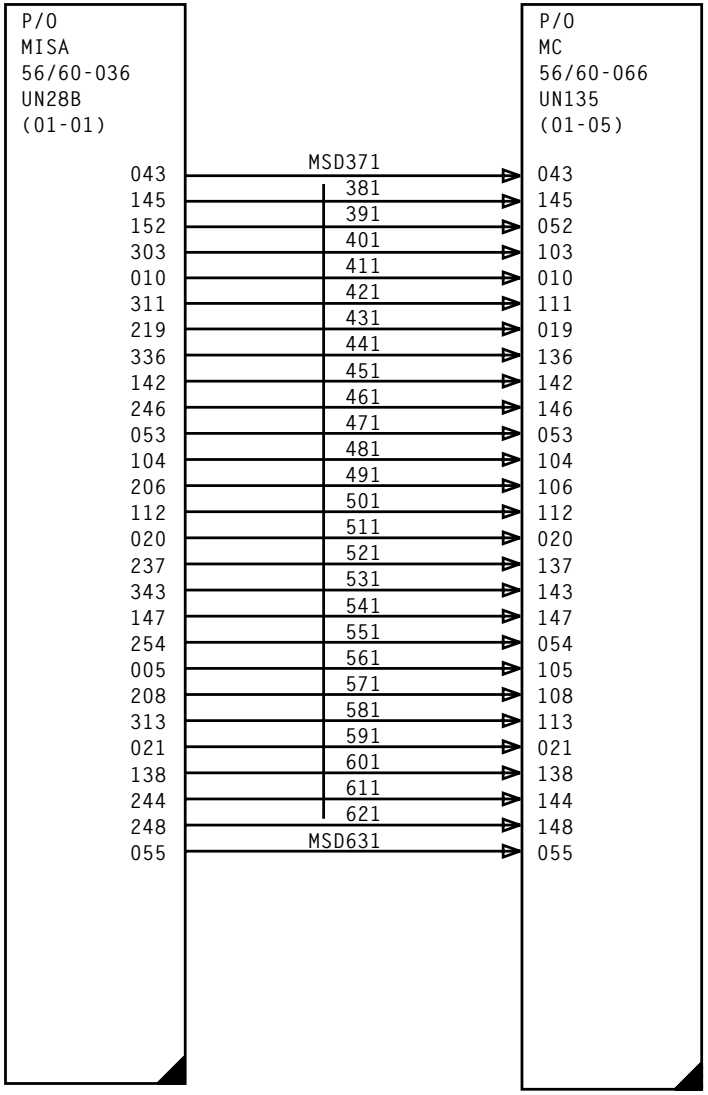


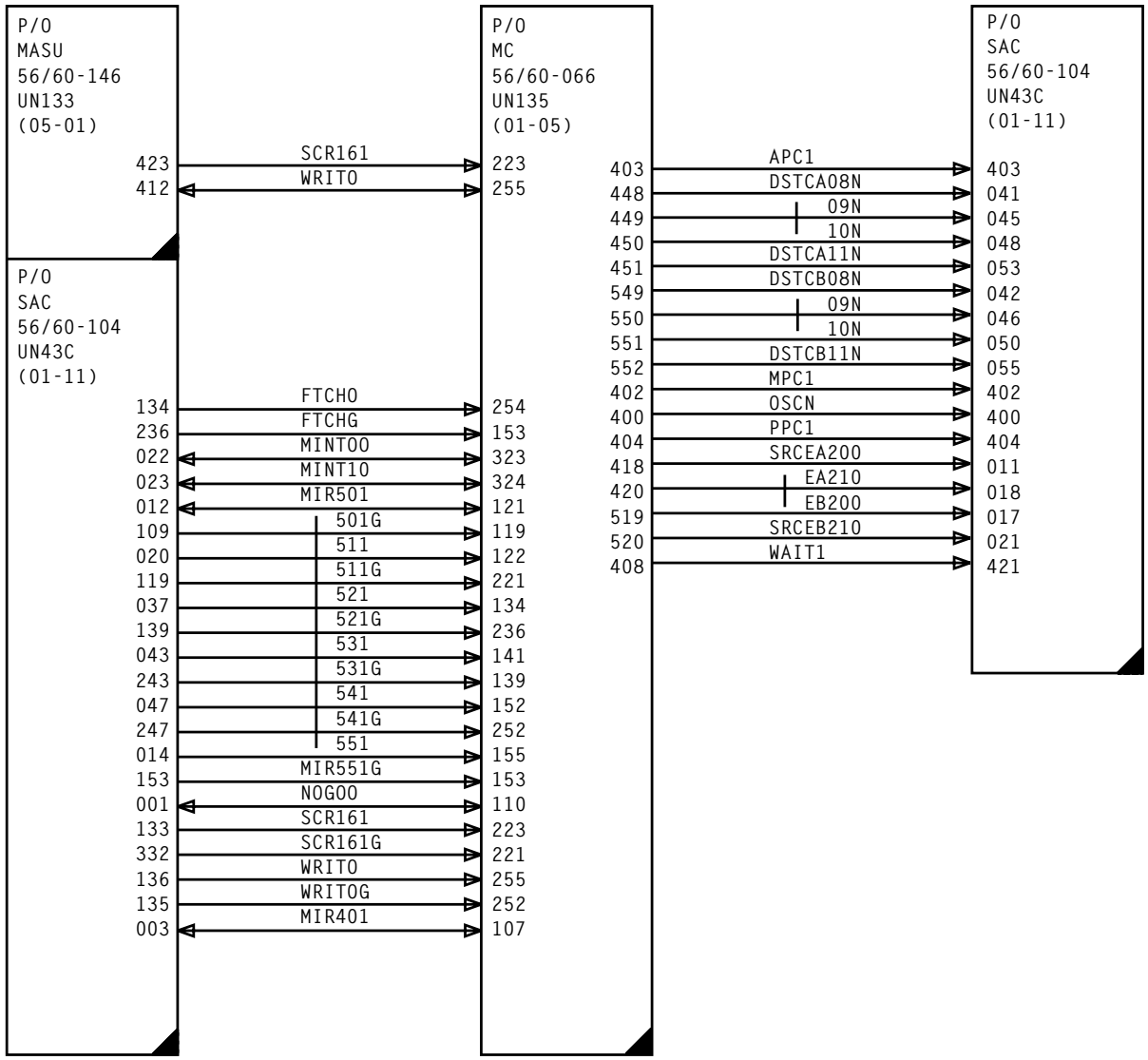
CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCONTROL (MC) FAILURES



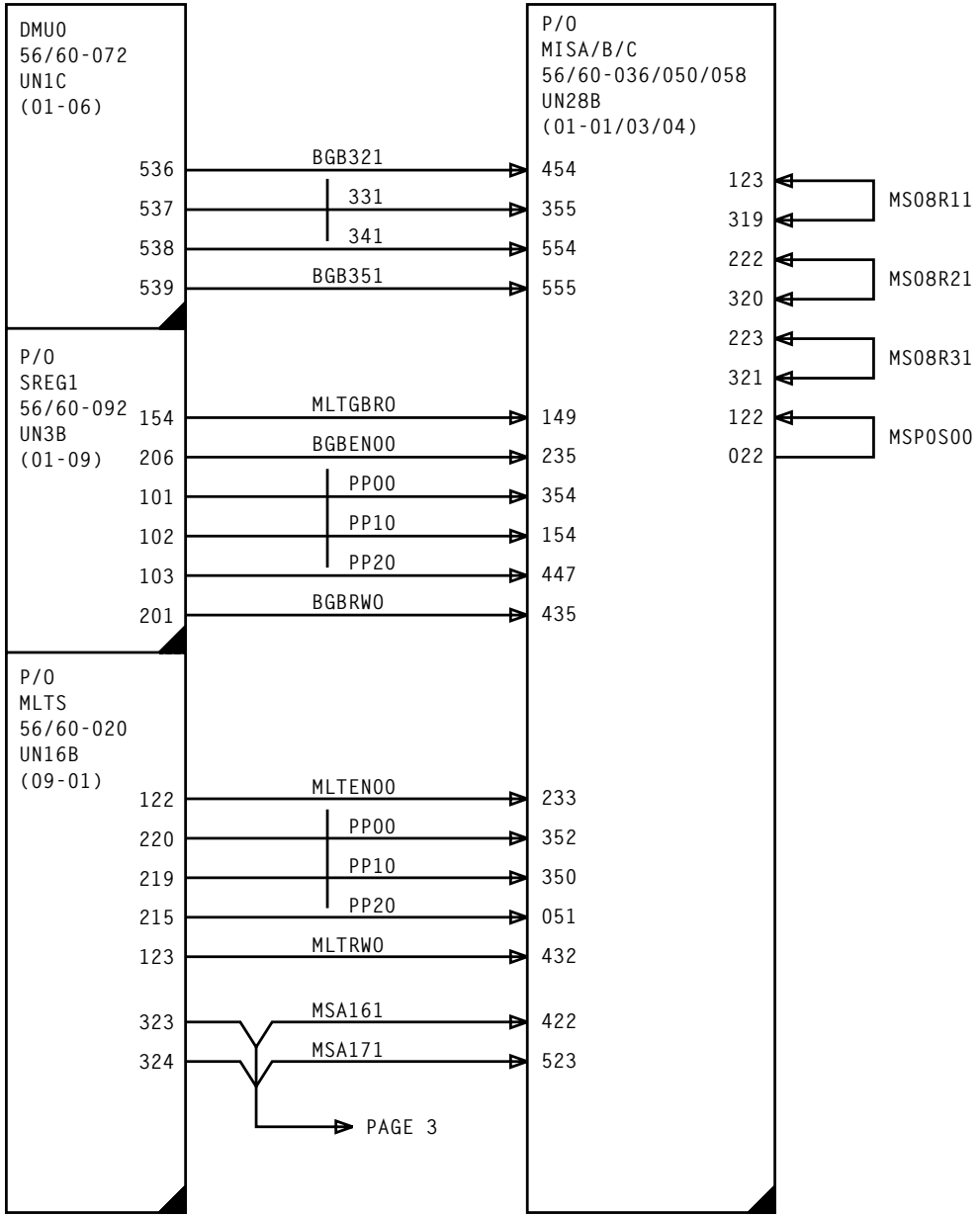
CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCONTROL (MC) FAILURES



CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28
MICROCONTROL (MC) FAILURES



CENTRAL CONTROL (CC) PHASES 5-8, 10, AND 26-28 MICROCONTROL (MC) FAILURES



CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES

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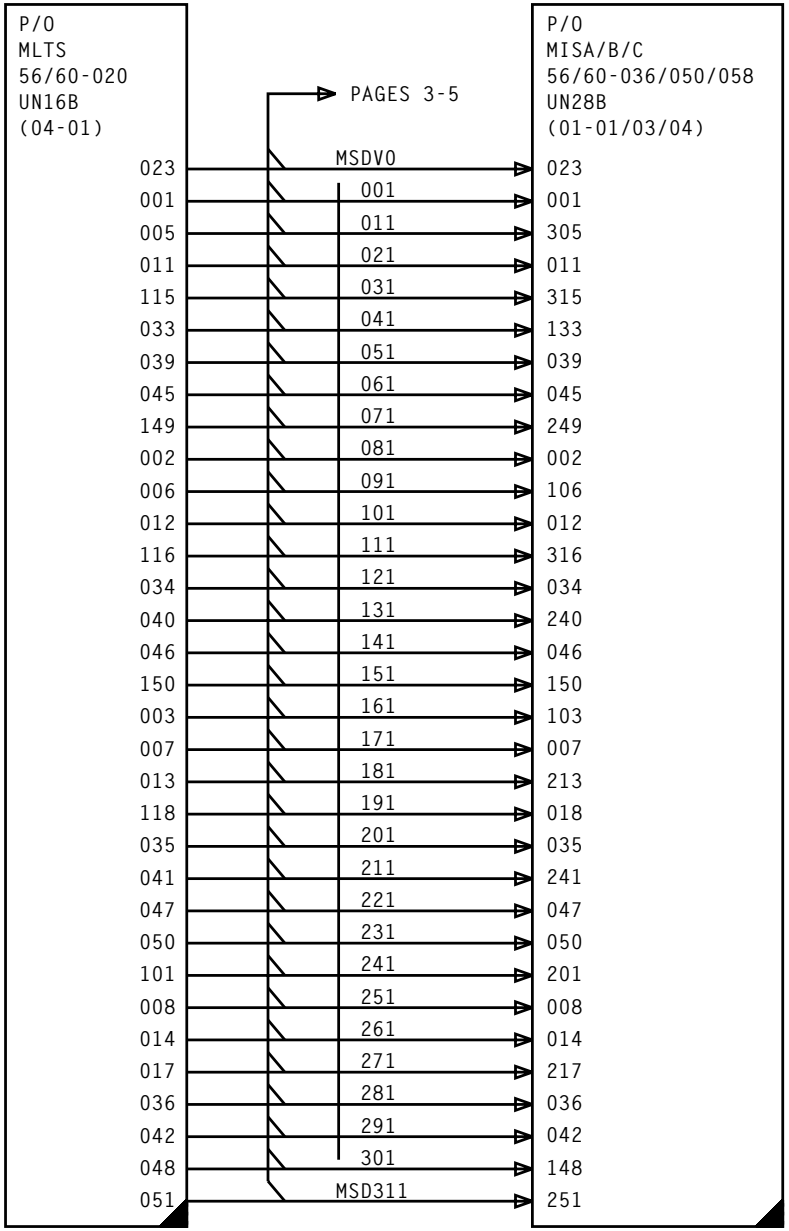
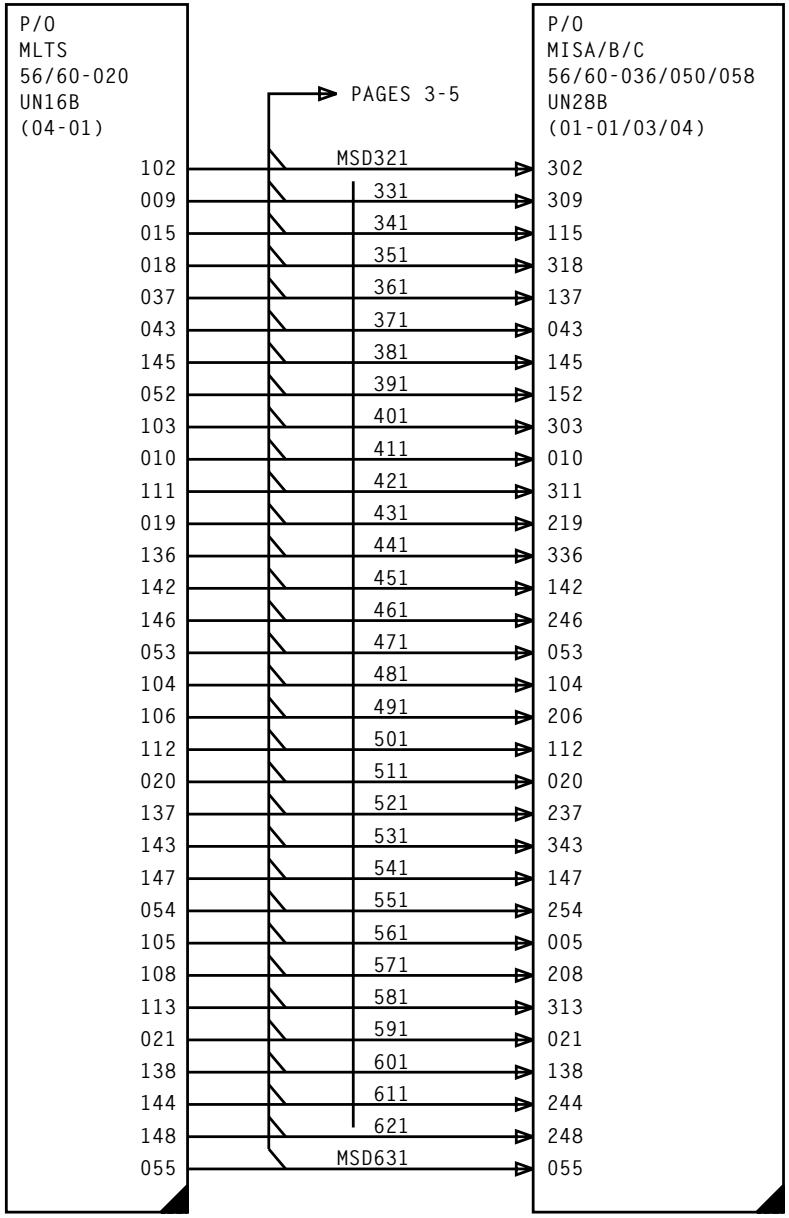
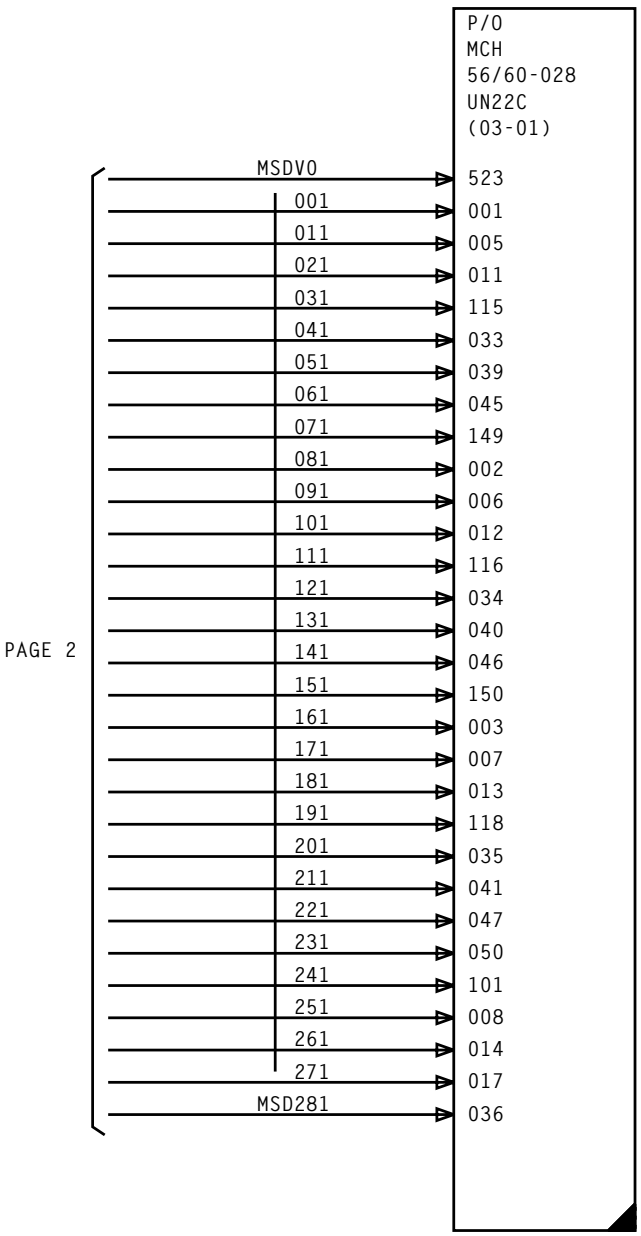
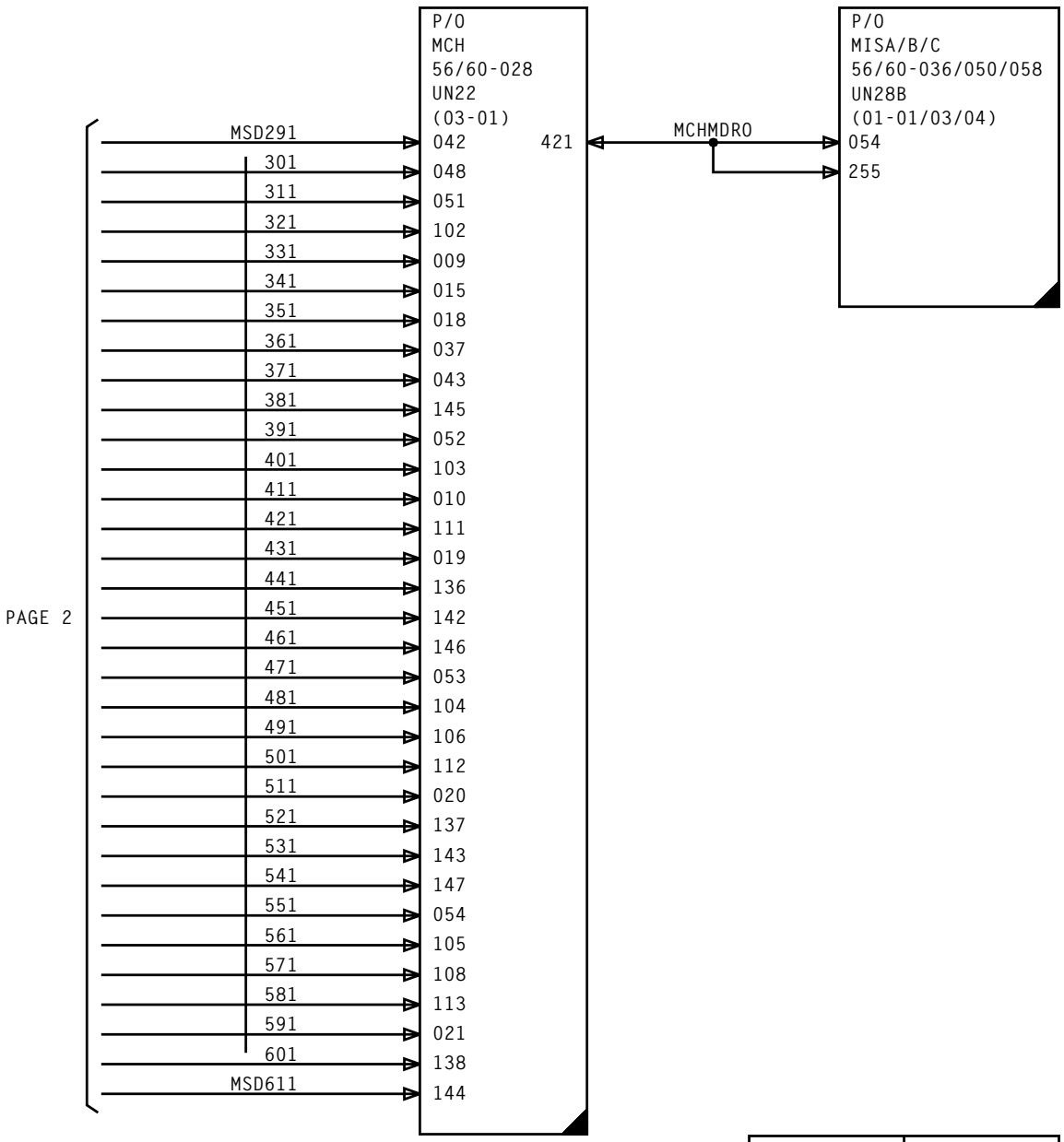


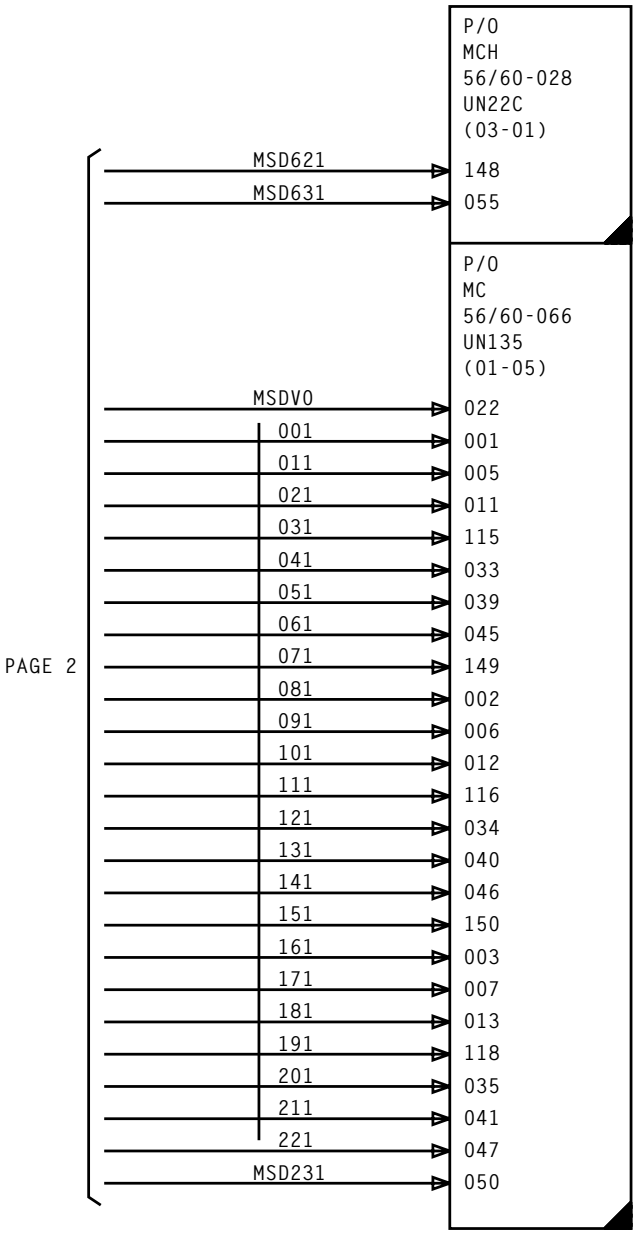


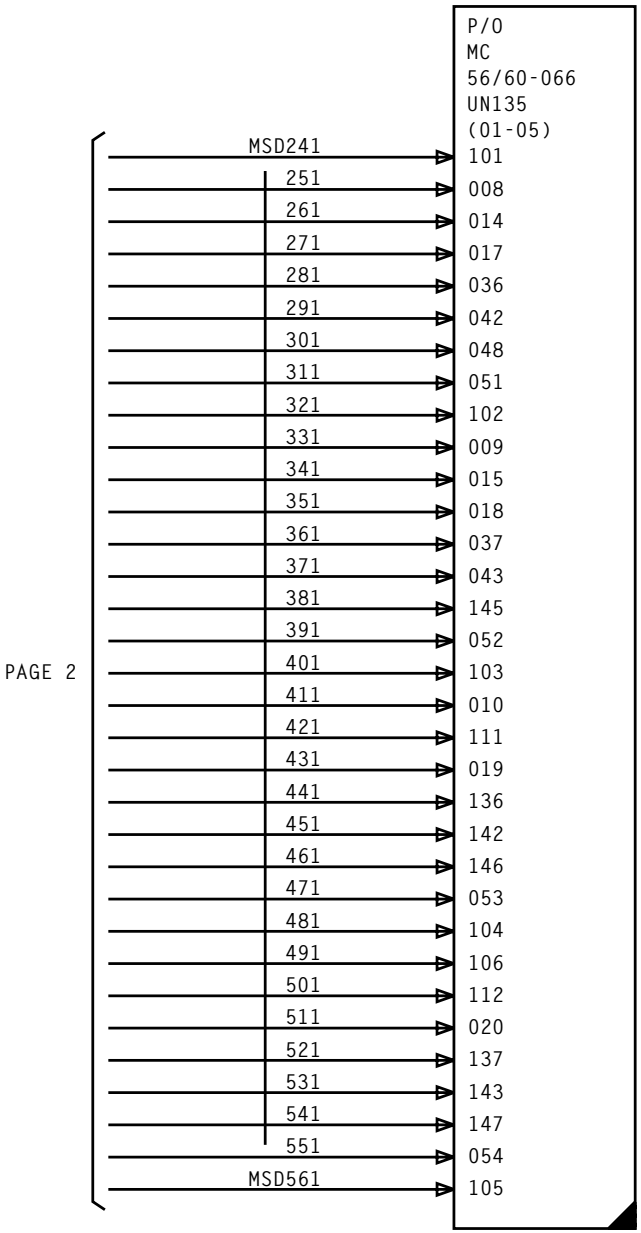
CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES



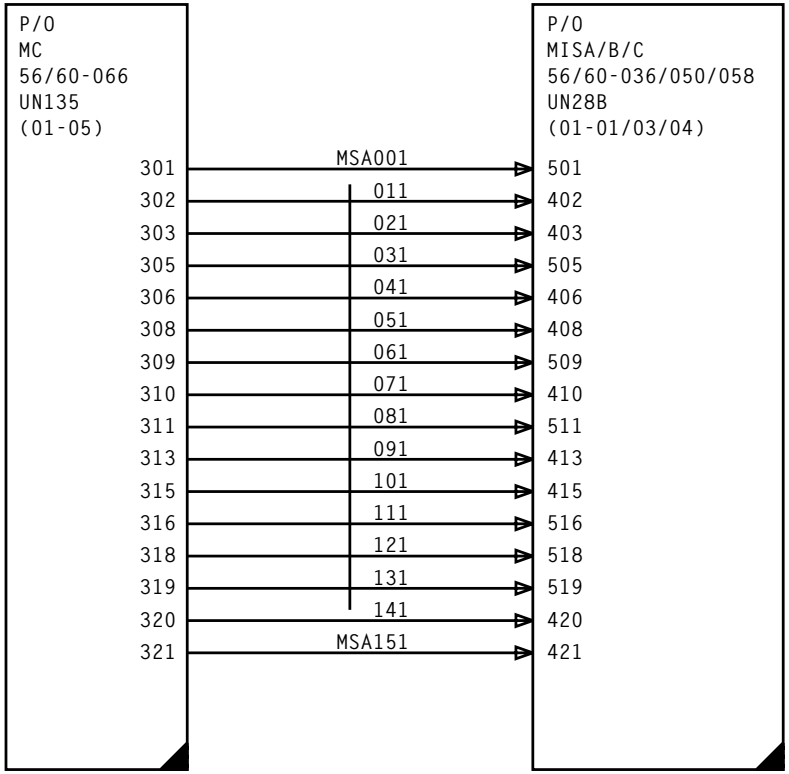


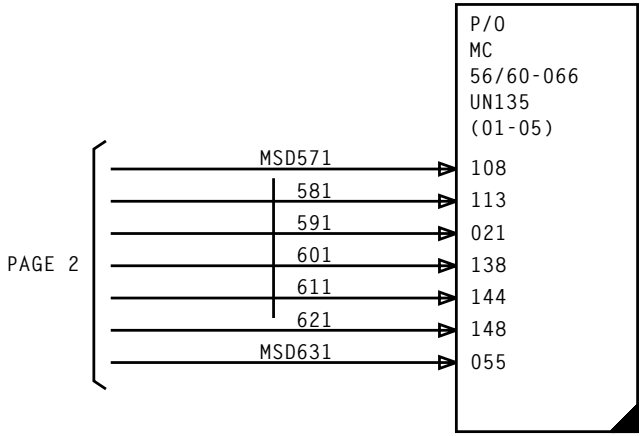
CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTROE (MIS) FAILURES



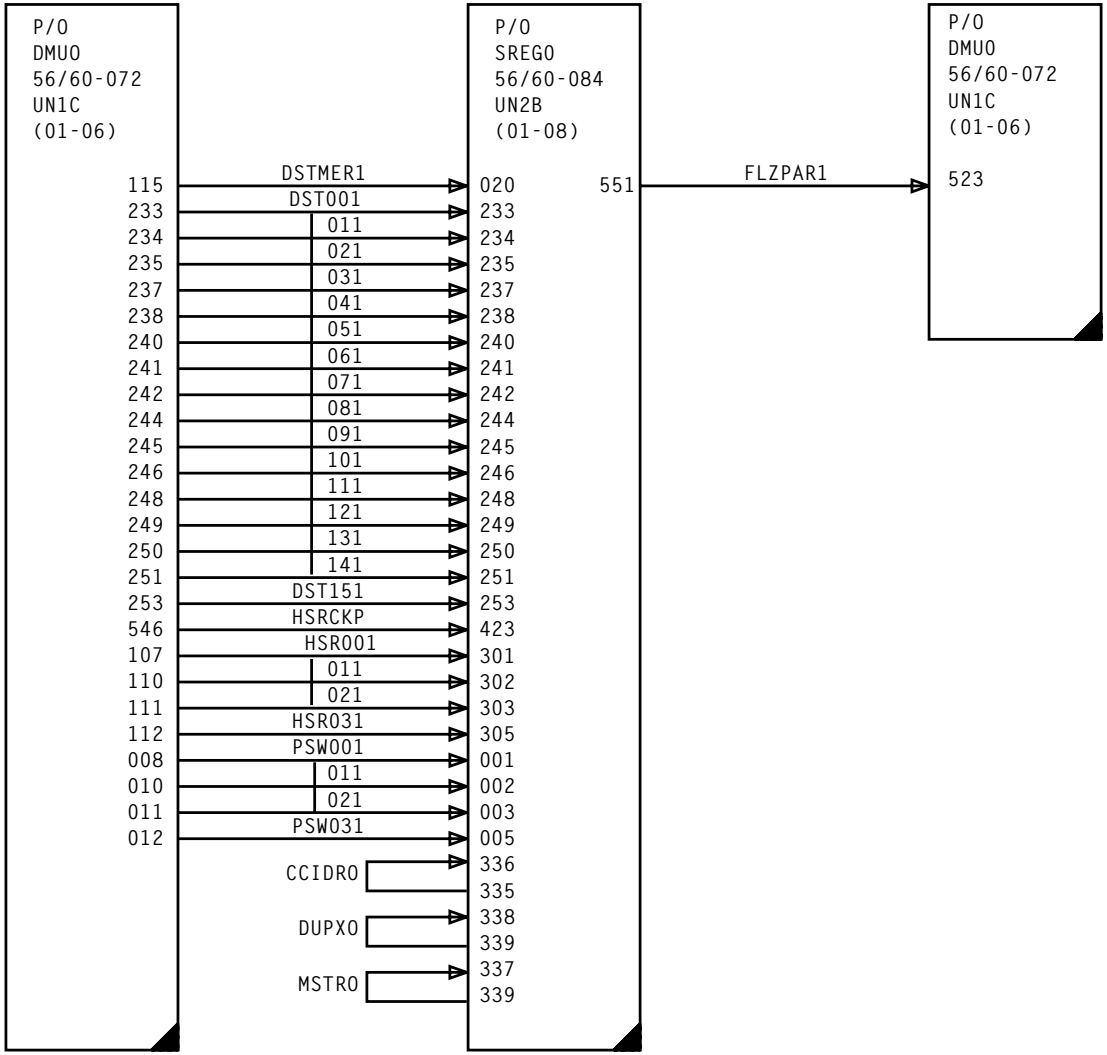


CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES

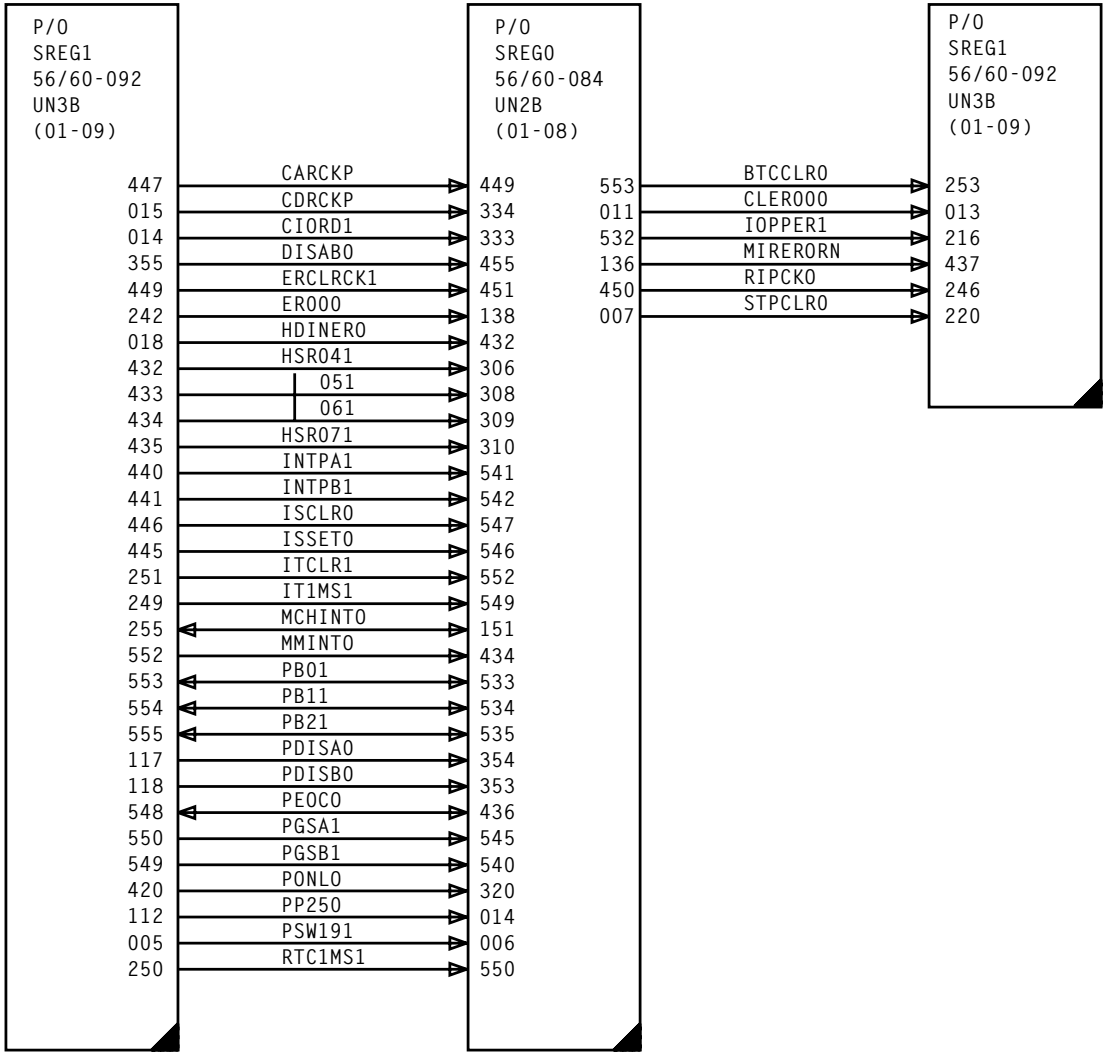




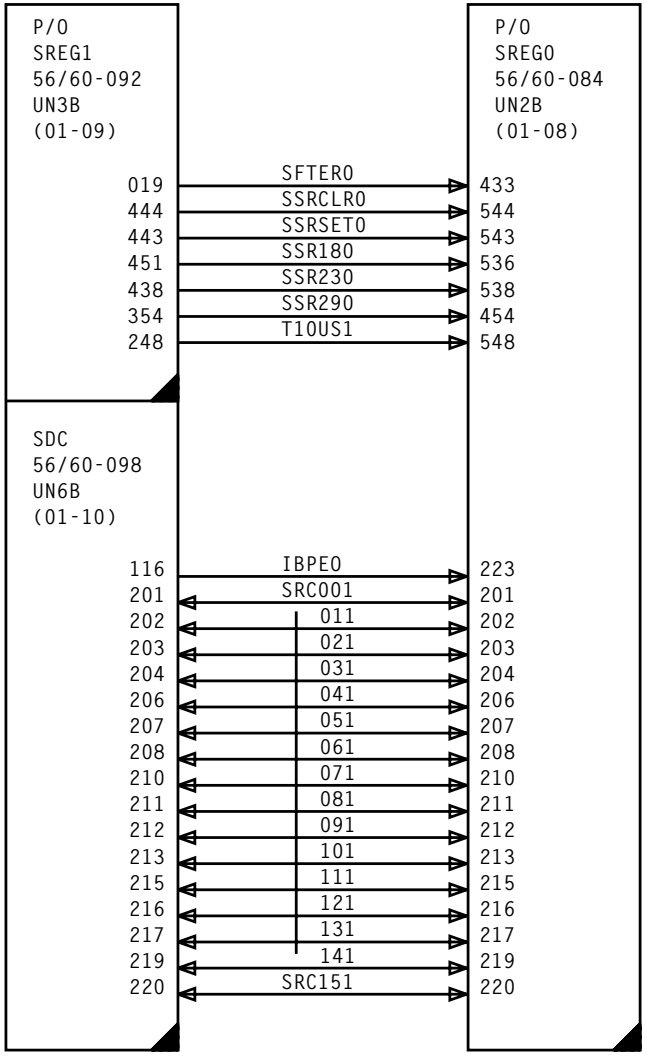
CENTRAL CONTROL (CC) PHASES 9, 70, AND 71 MICROSTORE (MIS) FAILURES



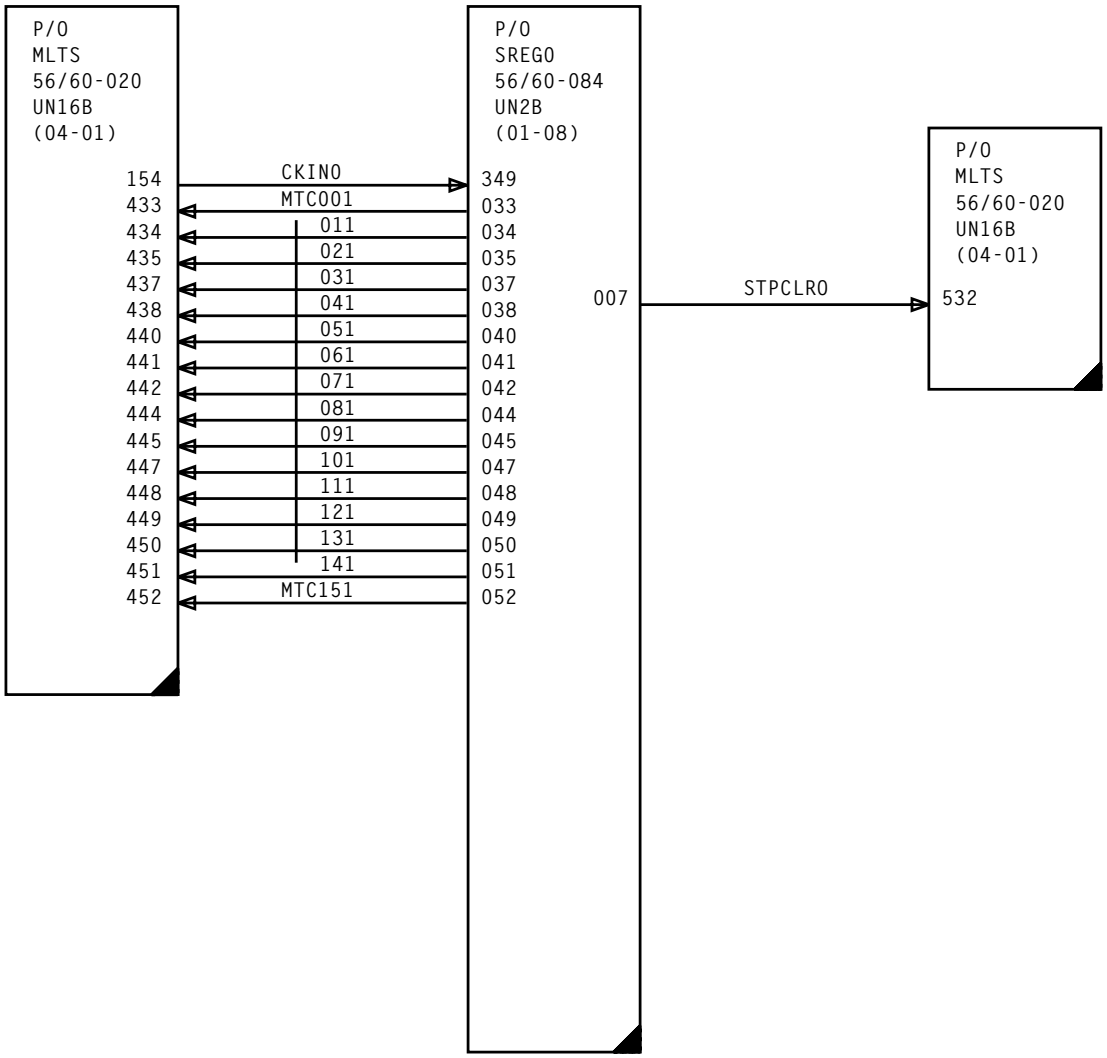
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 FAILURES



CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 FAILURES



CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 FAILURES



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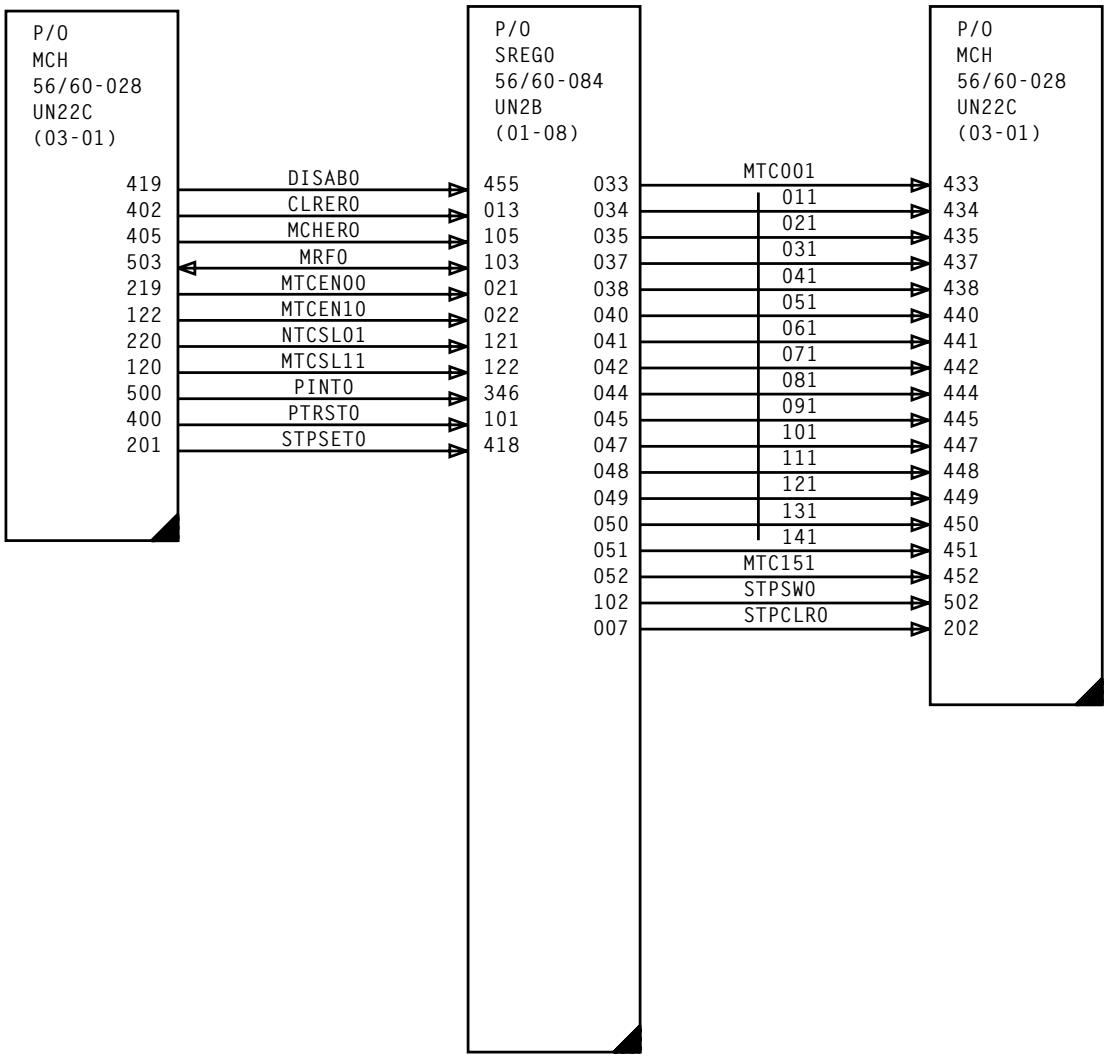

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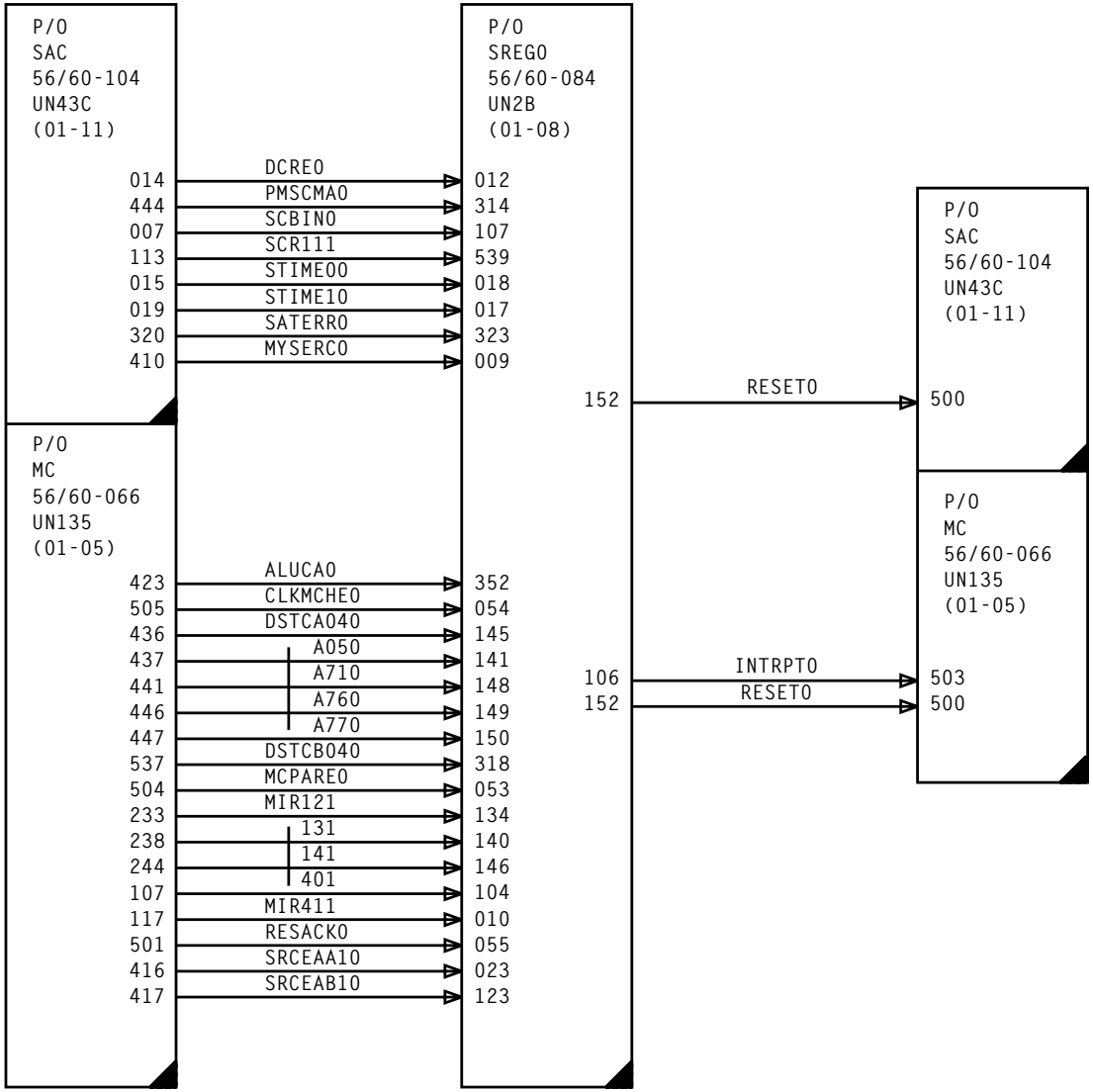
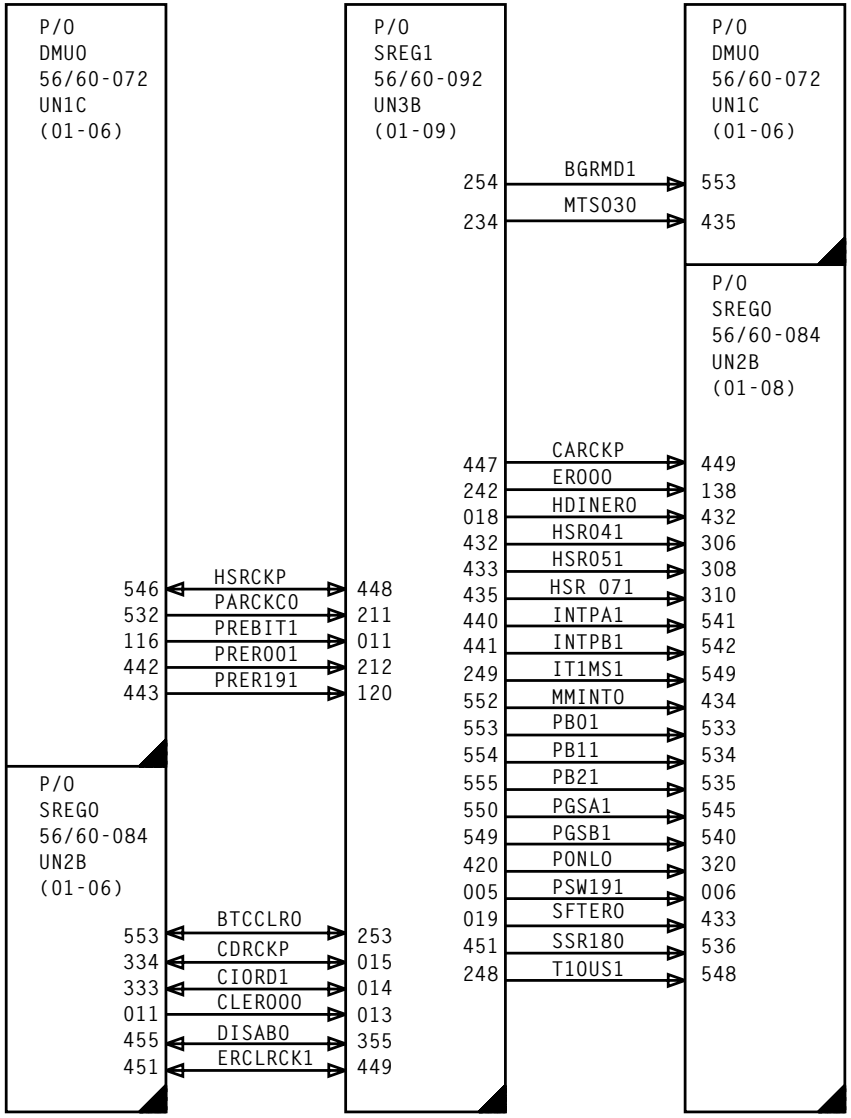
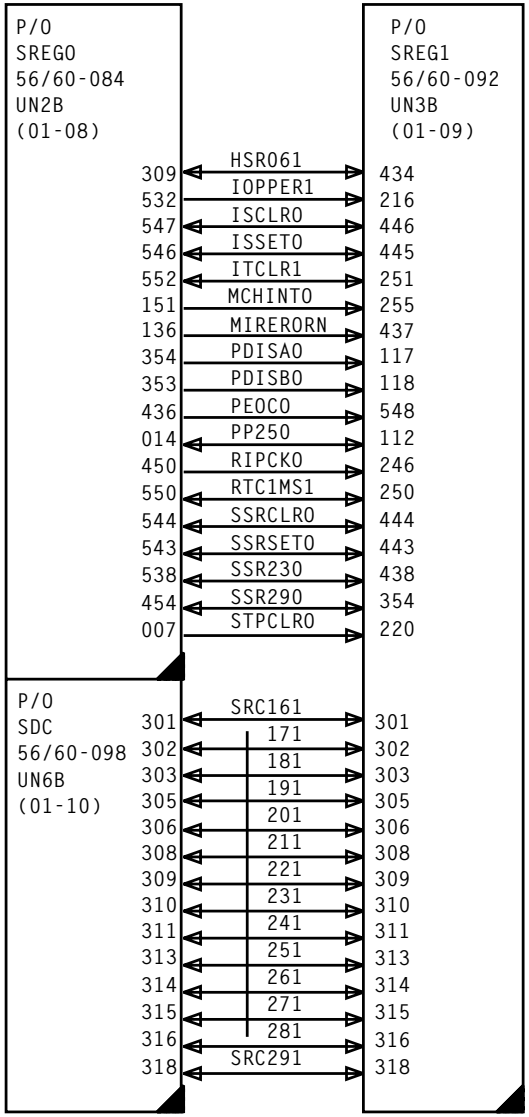


CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 0 FAILURES



CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



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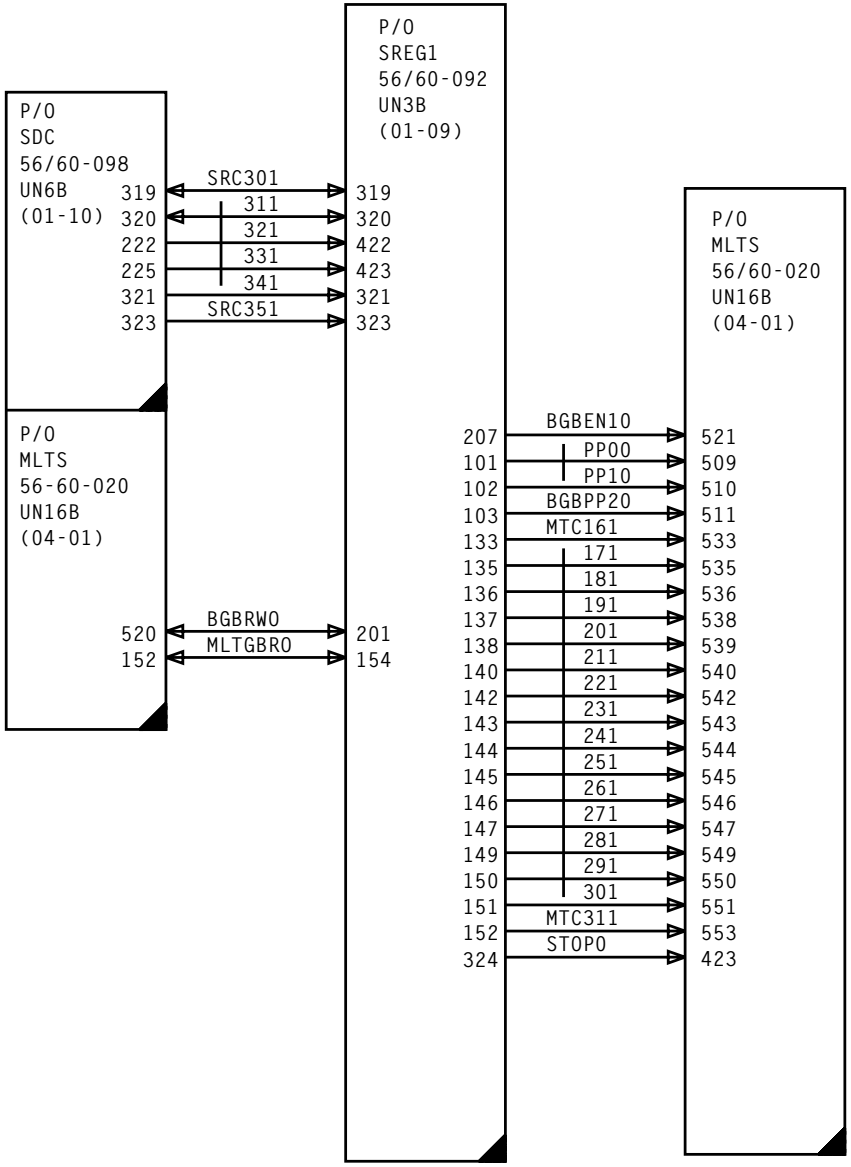

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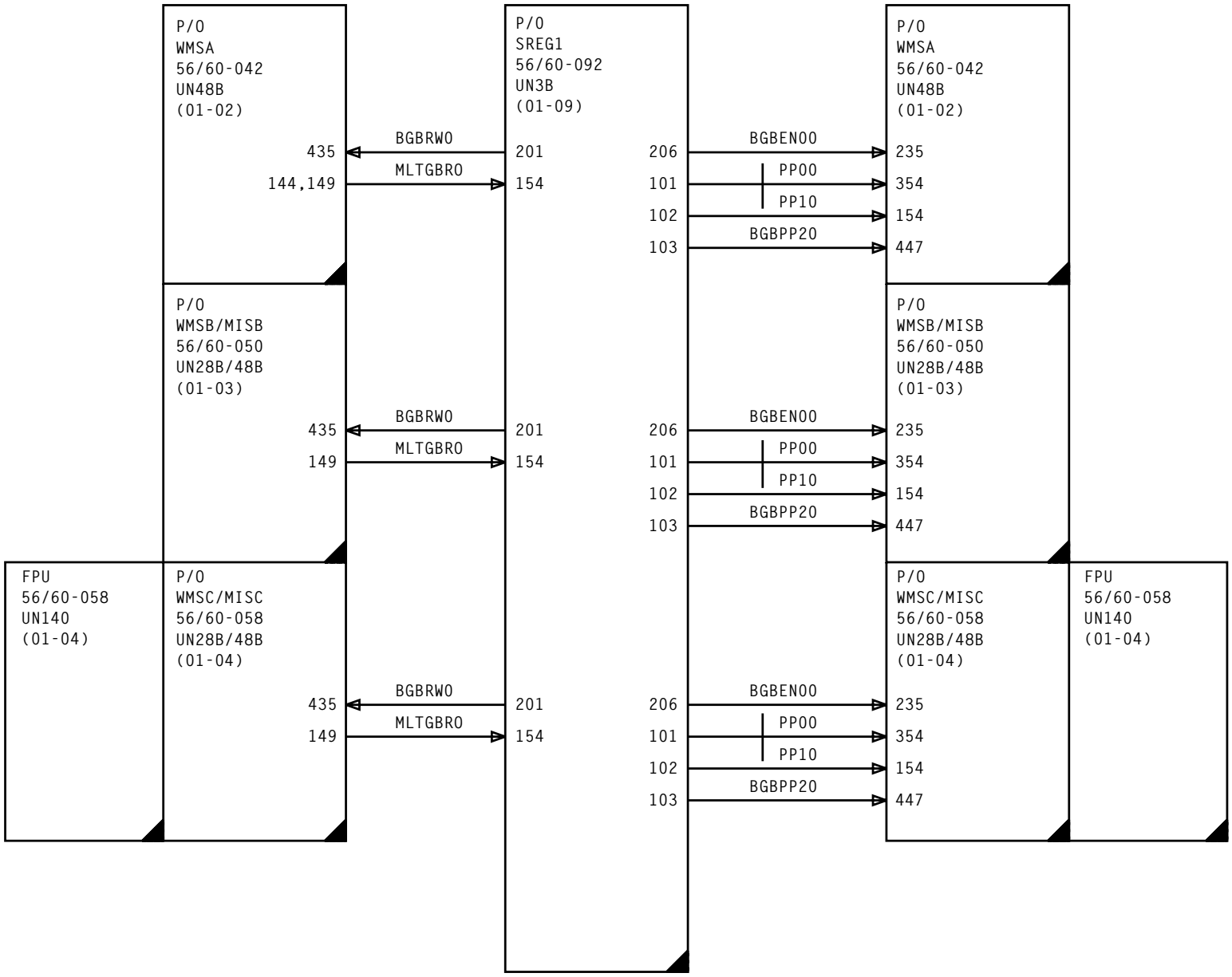
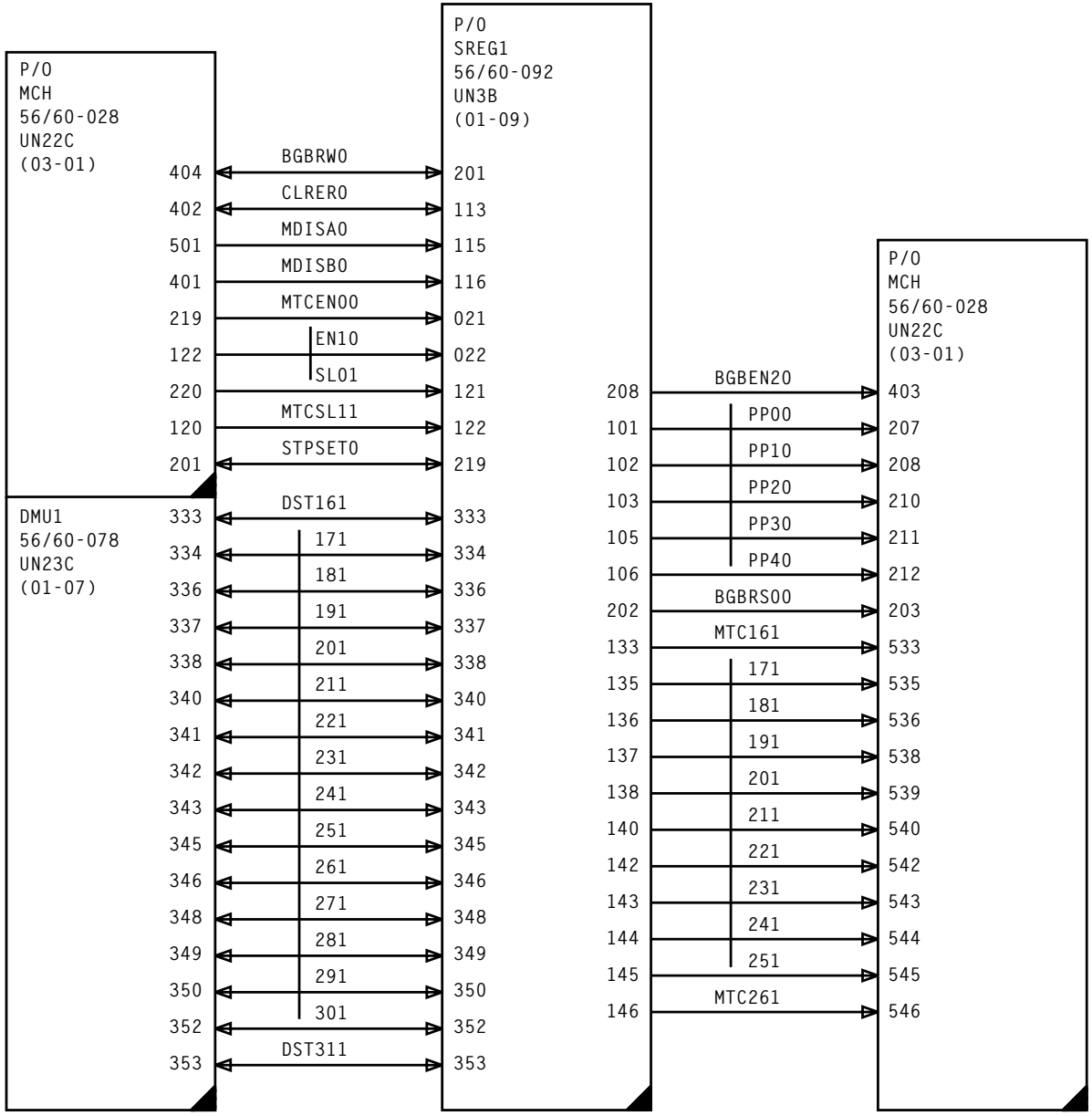
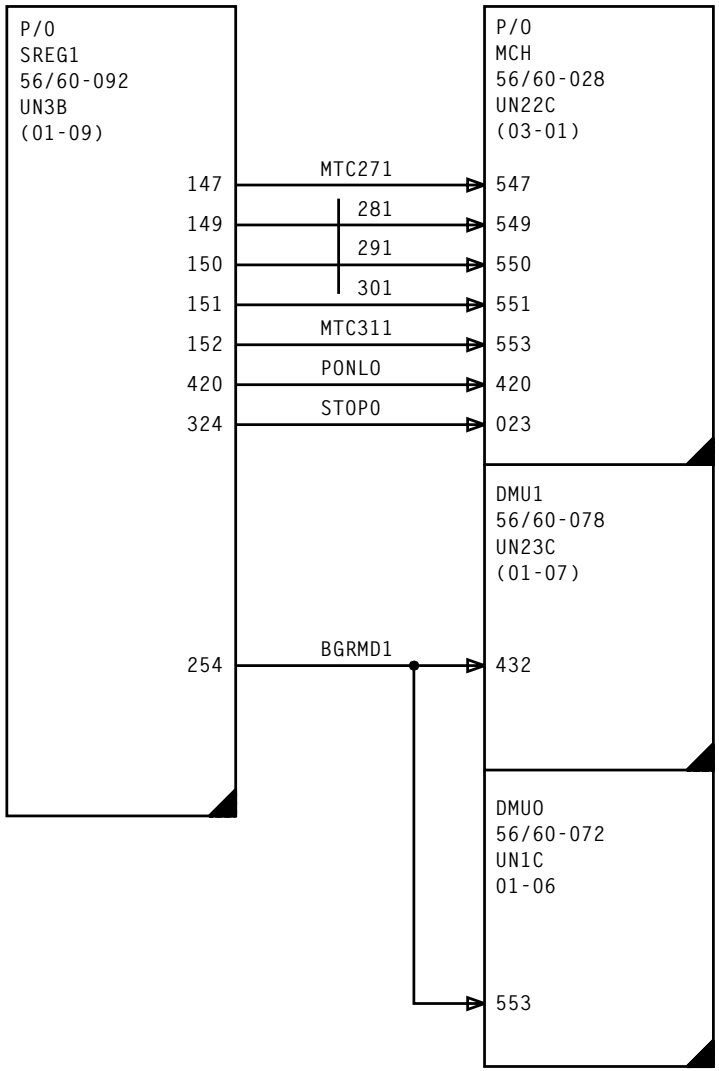


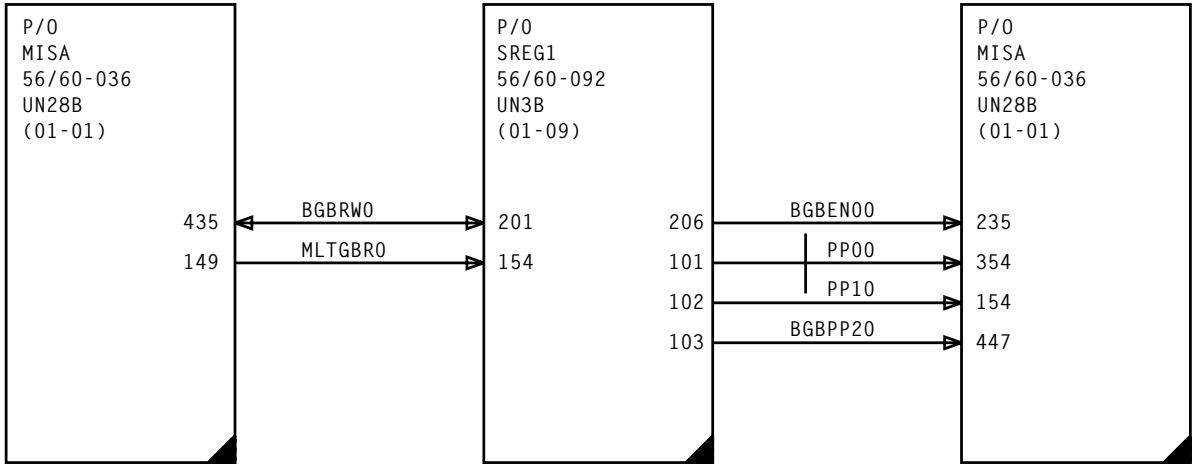
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



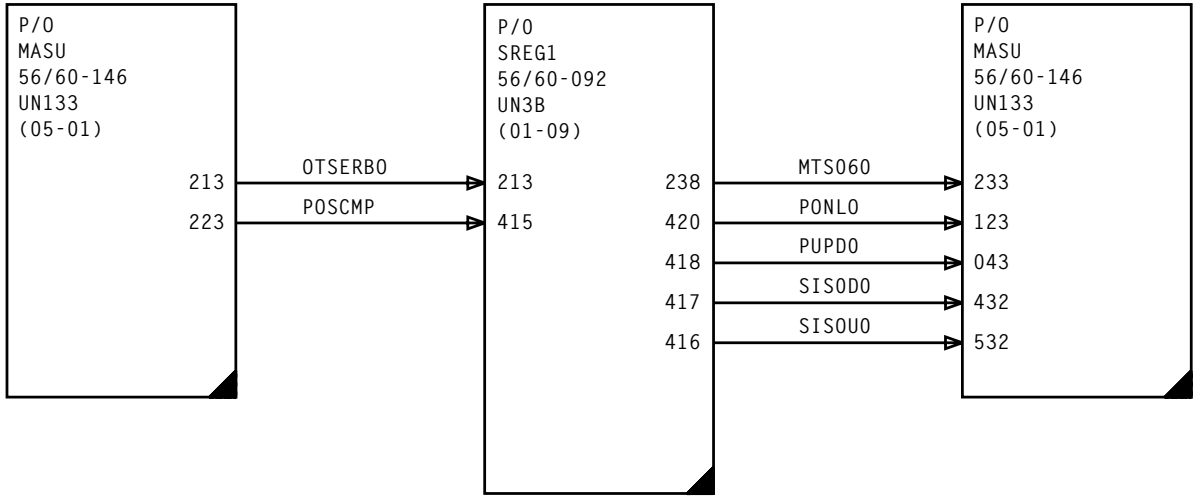
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



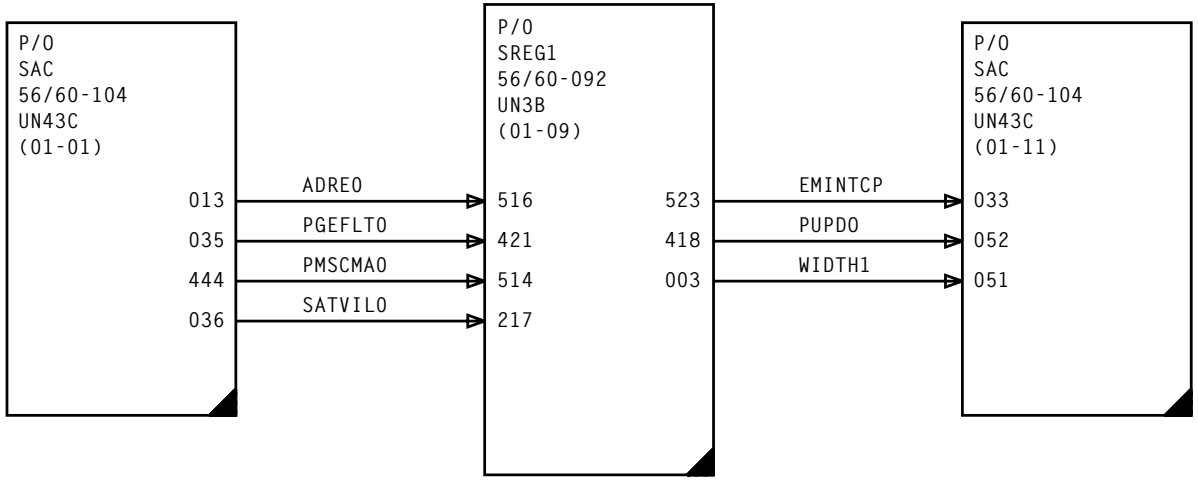
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



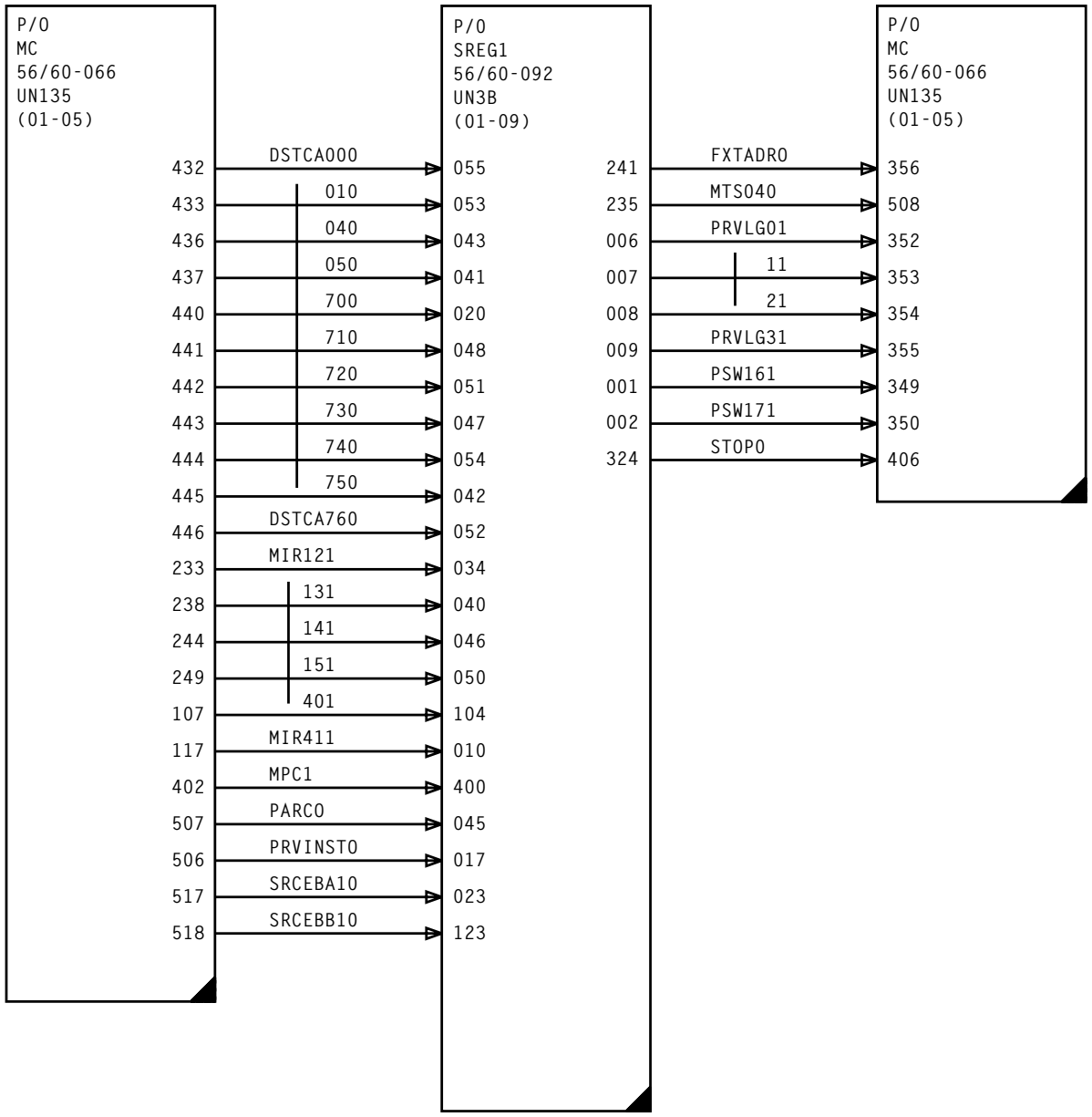
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



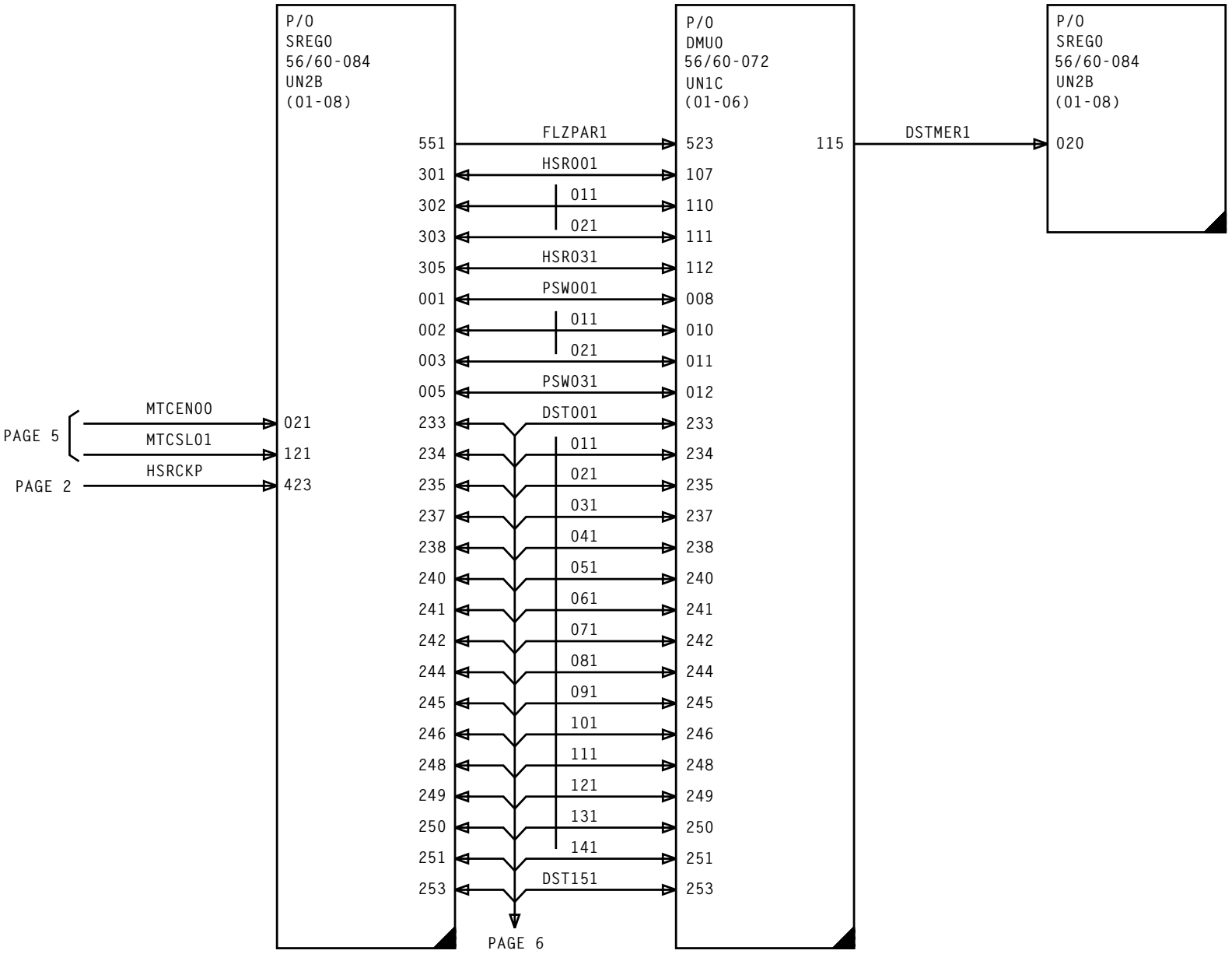
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



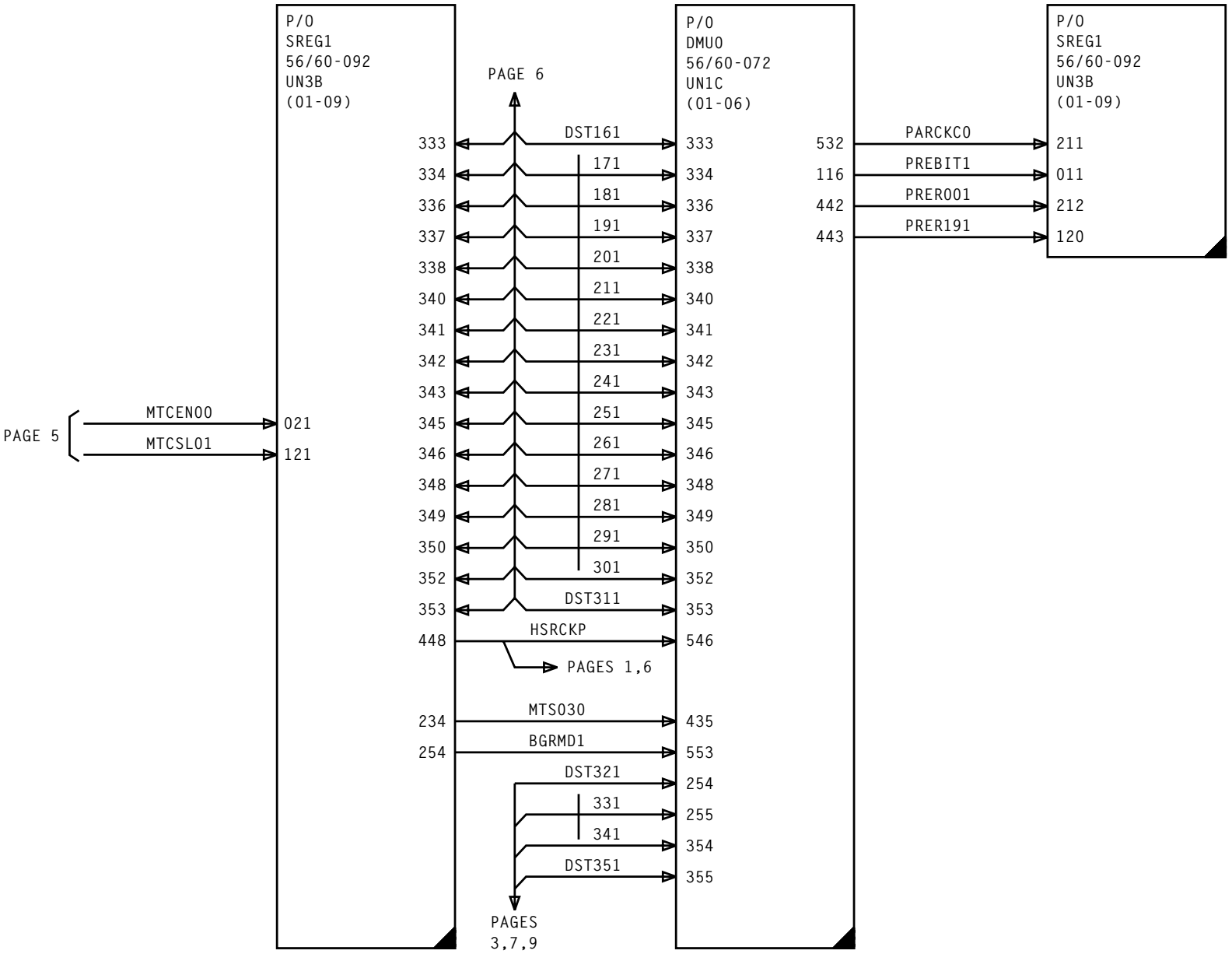
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



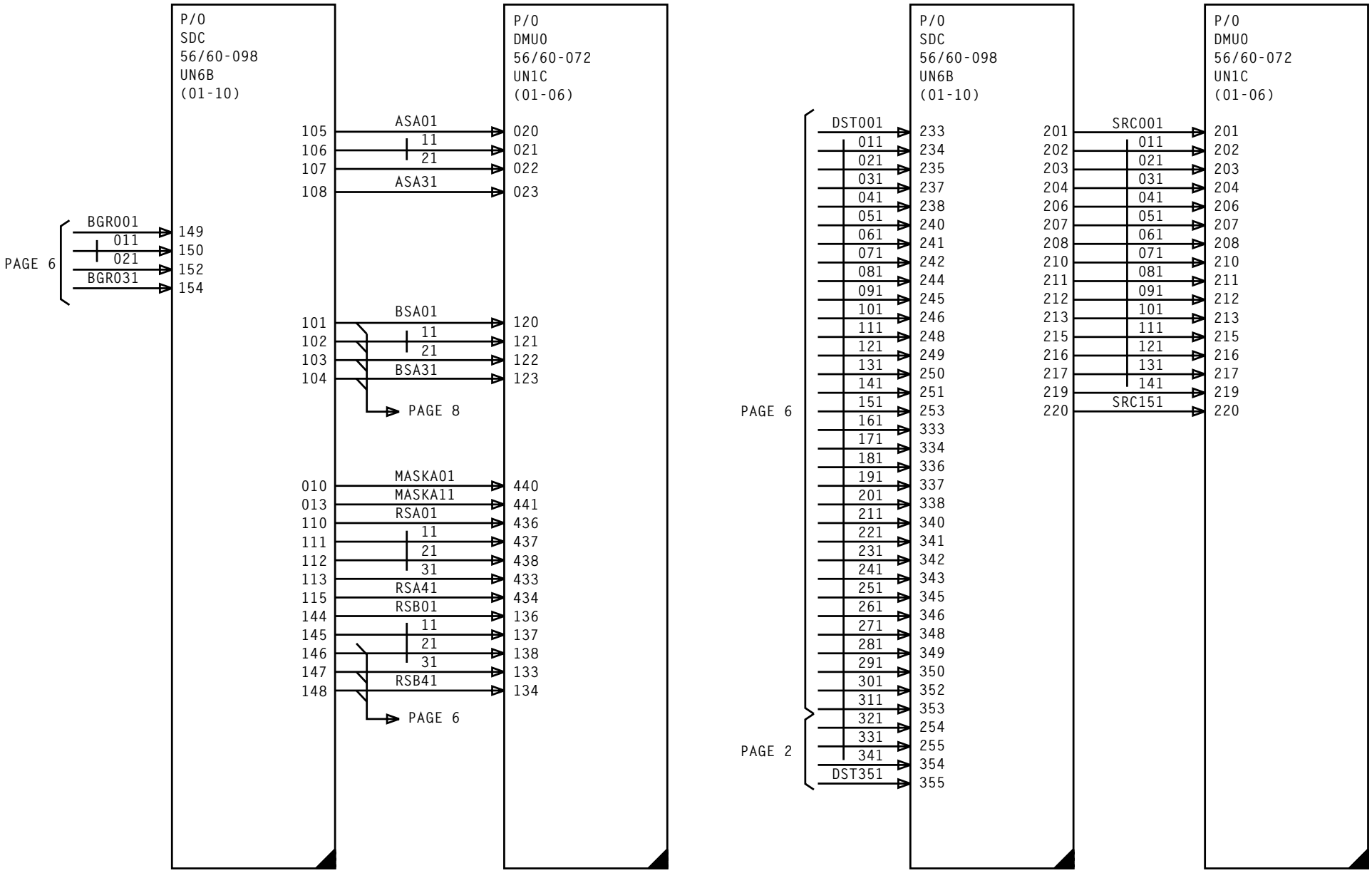
CENTRAL CONTROL (CC) PHASES 11, 12, AND 54-61 SPECIAL REGISTER 1 FAILURES



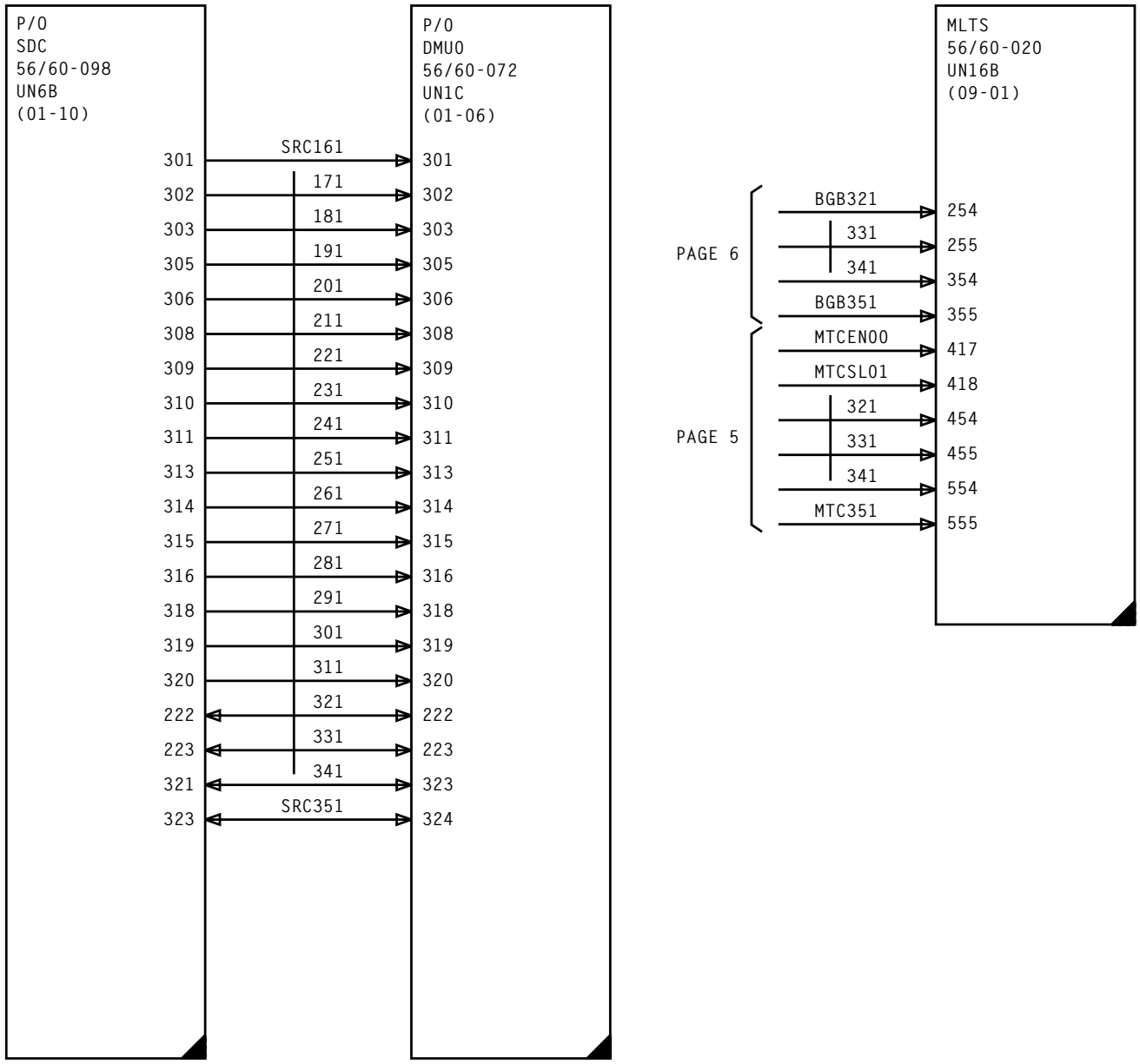
CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 0 FAILURES



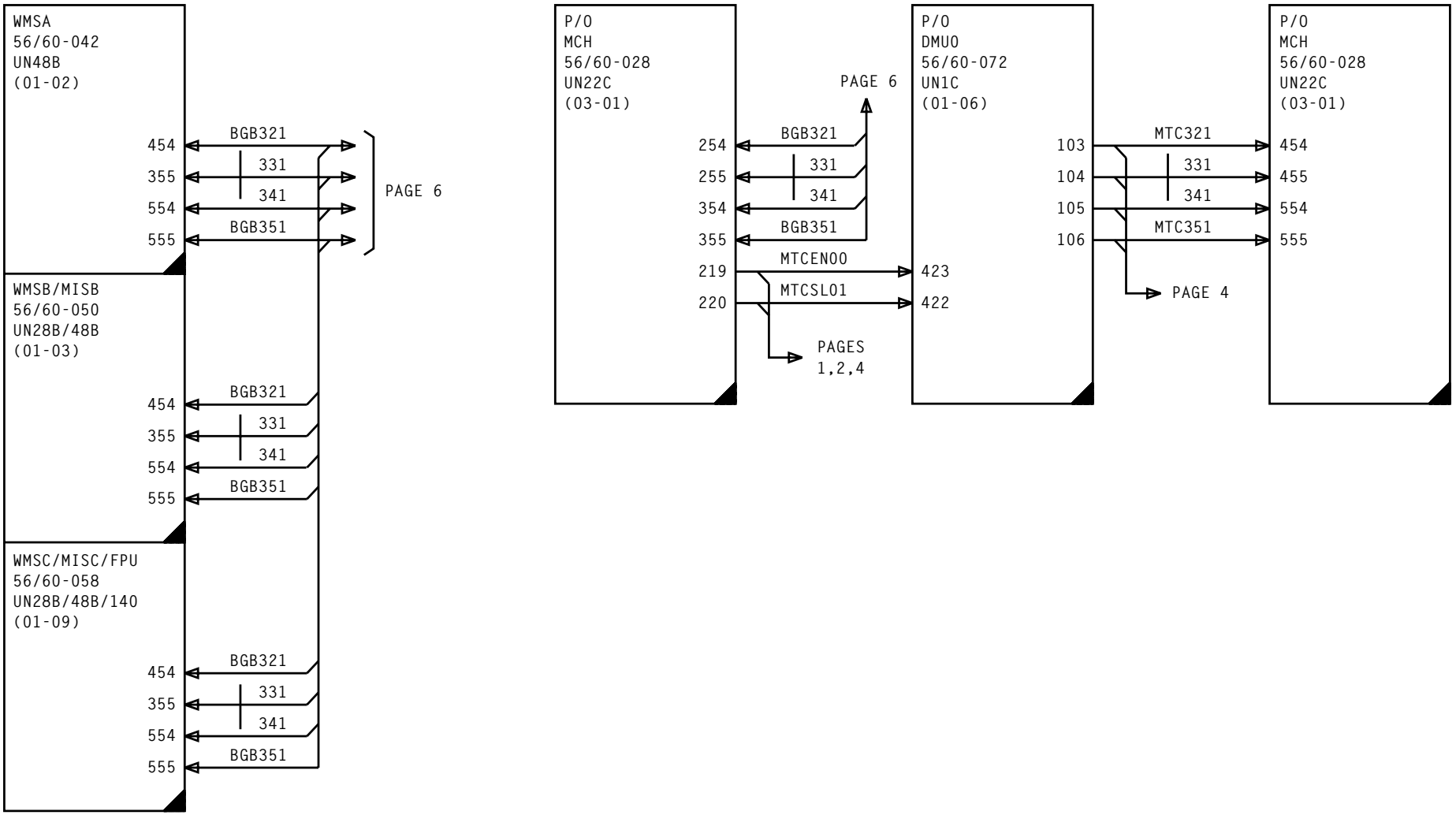
CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 0 FAILURES



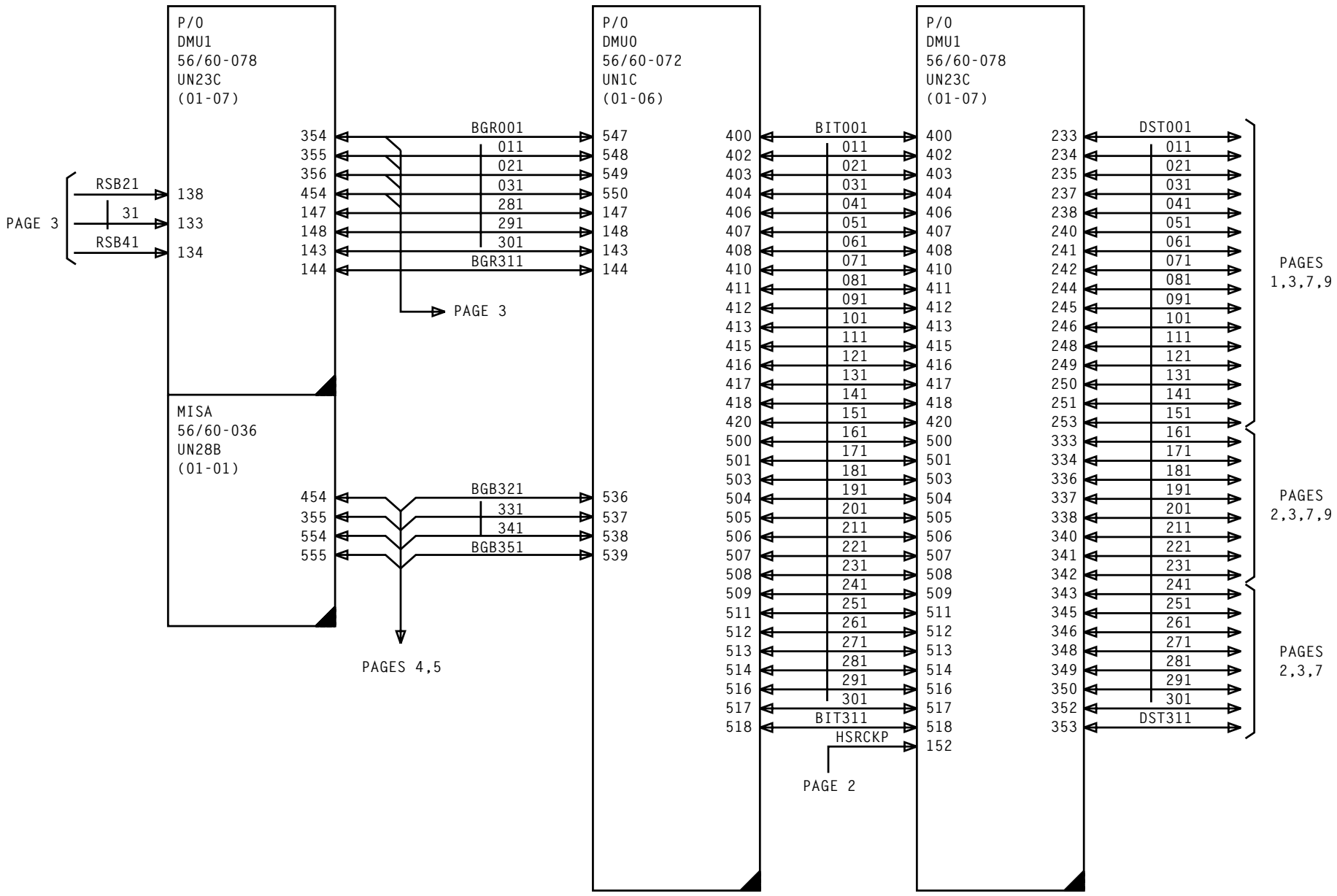
CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 0 FAILURES



CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 0 FAILURES



CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 0 FAILURES



CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
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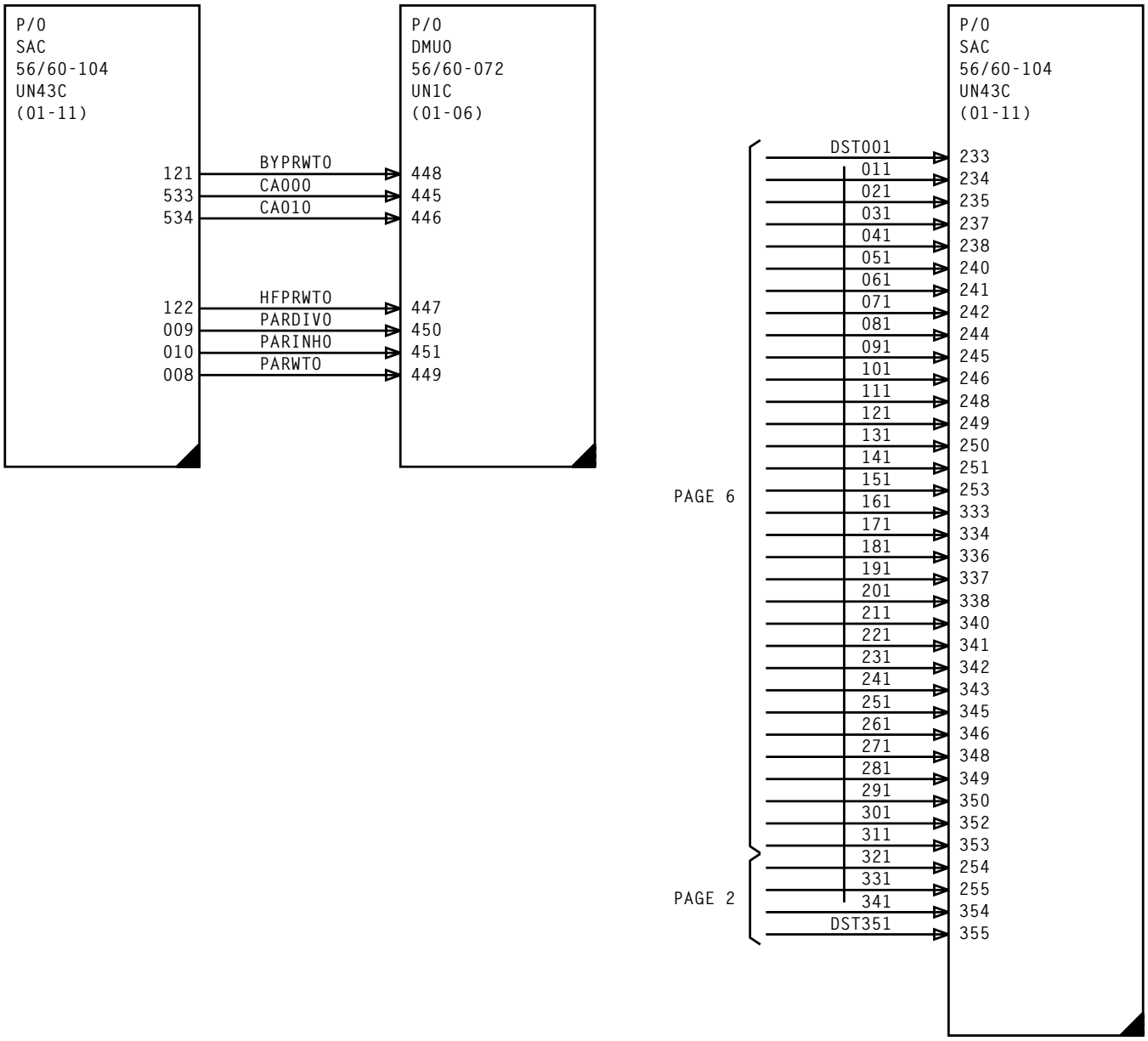

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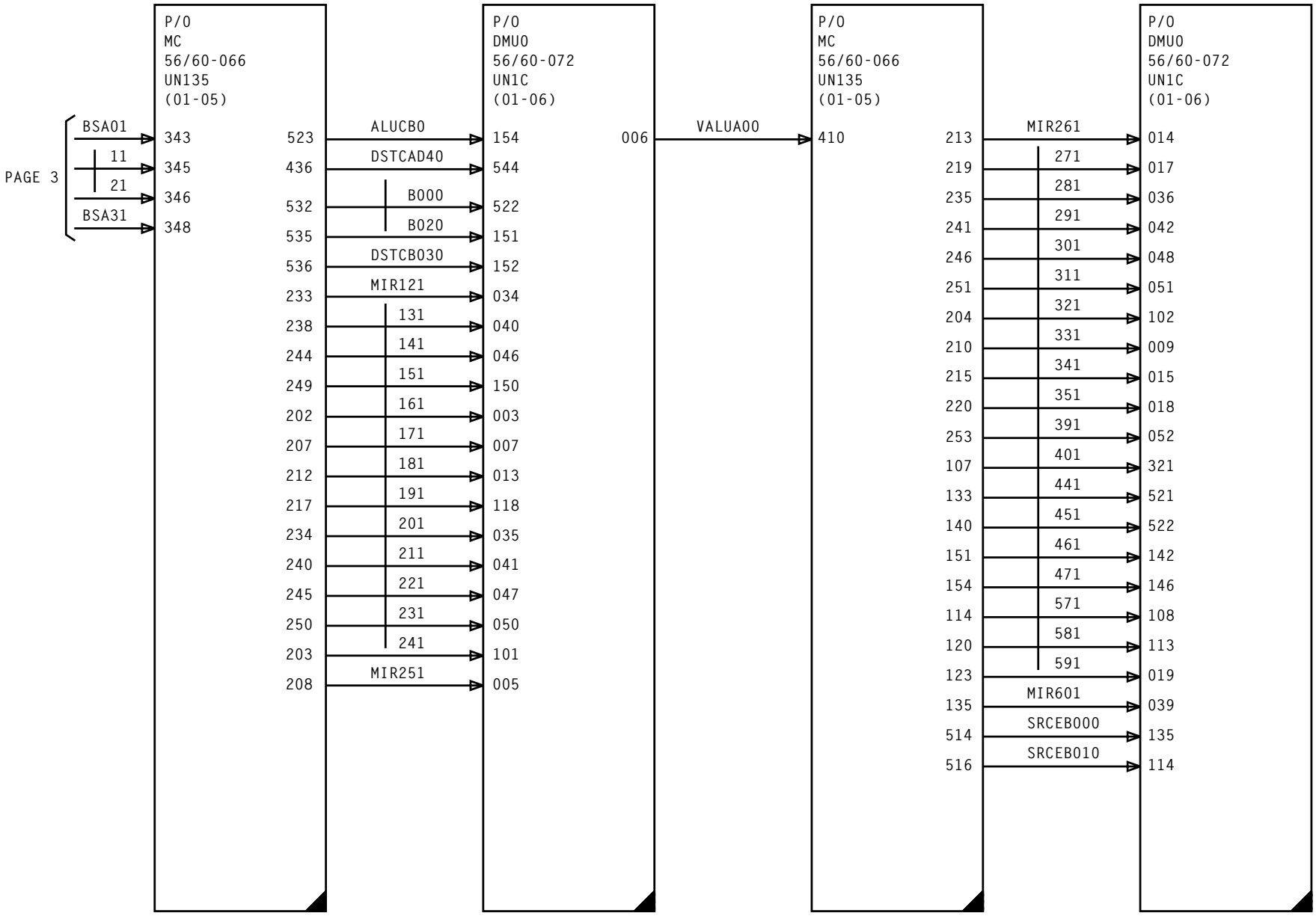

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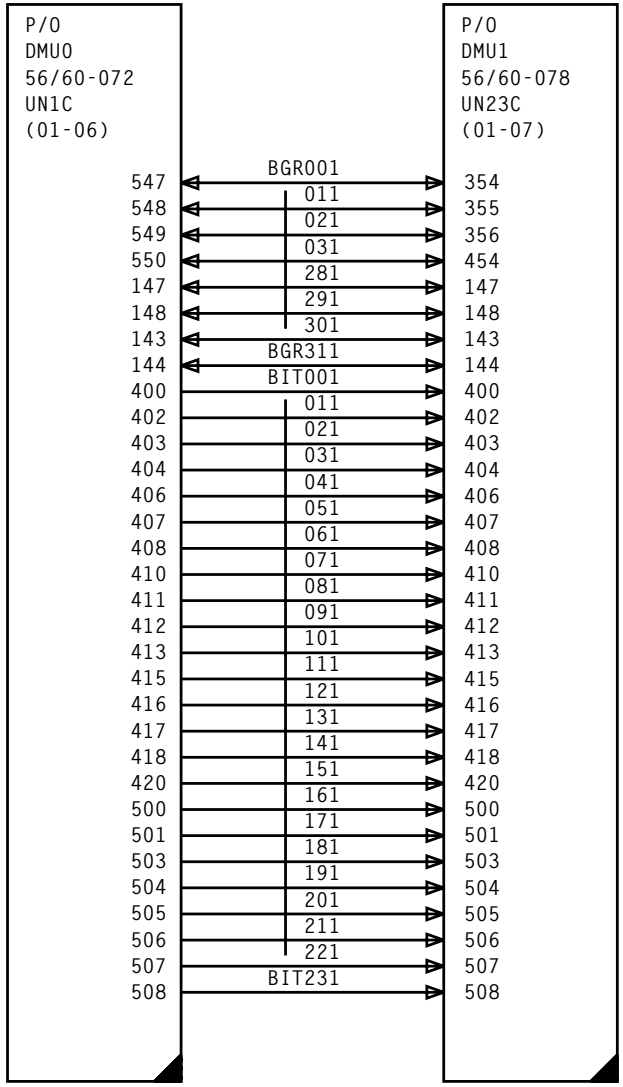
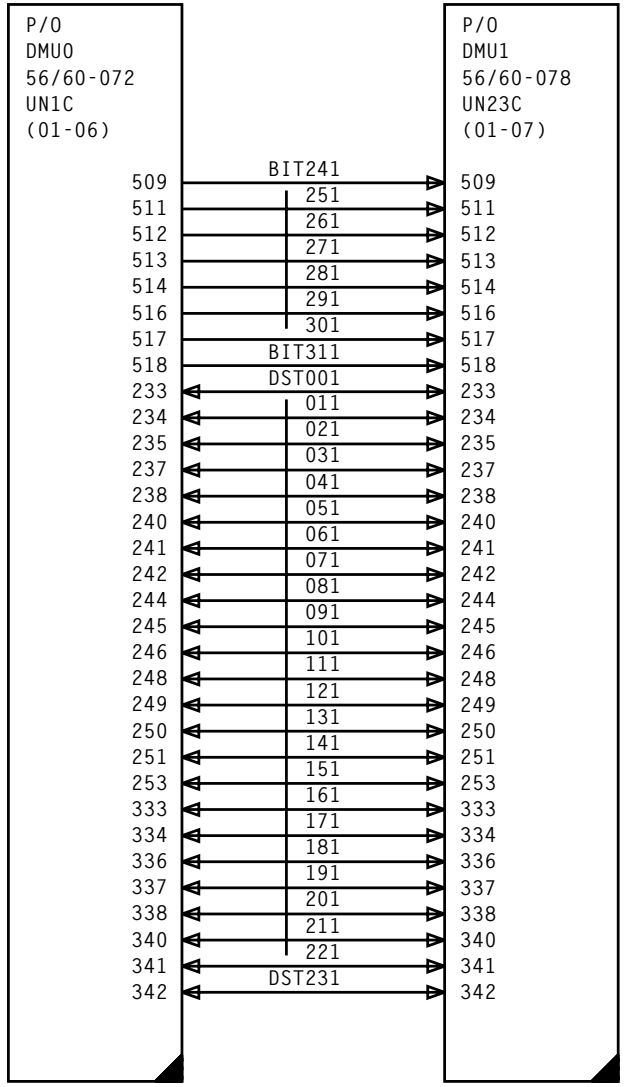
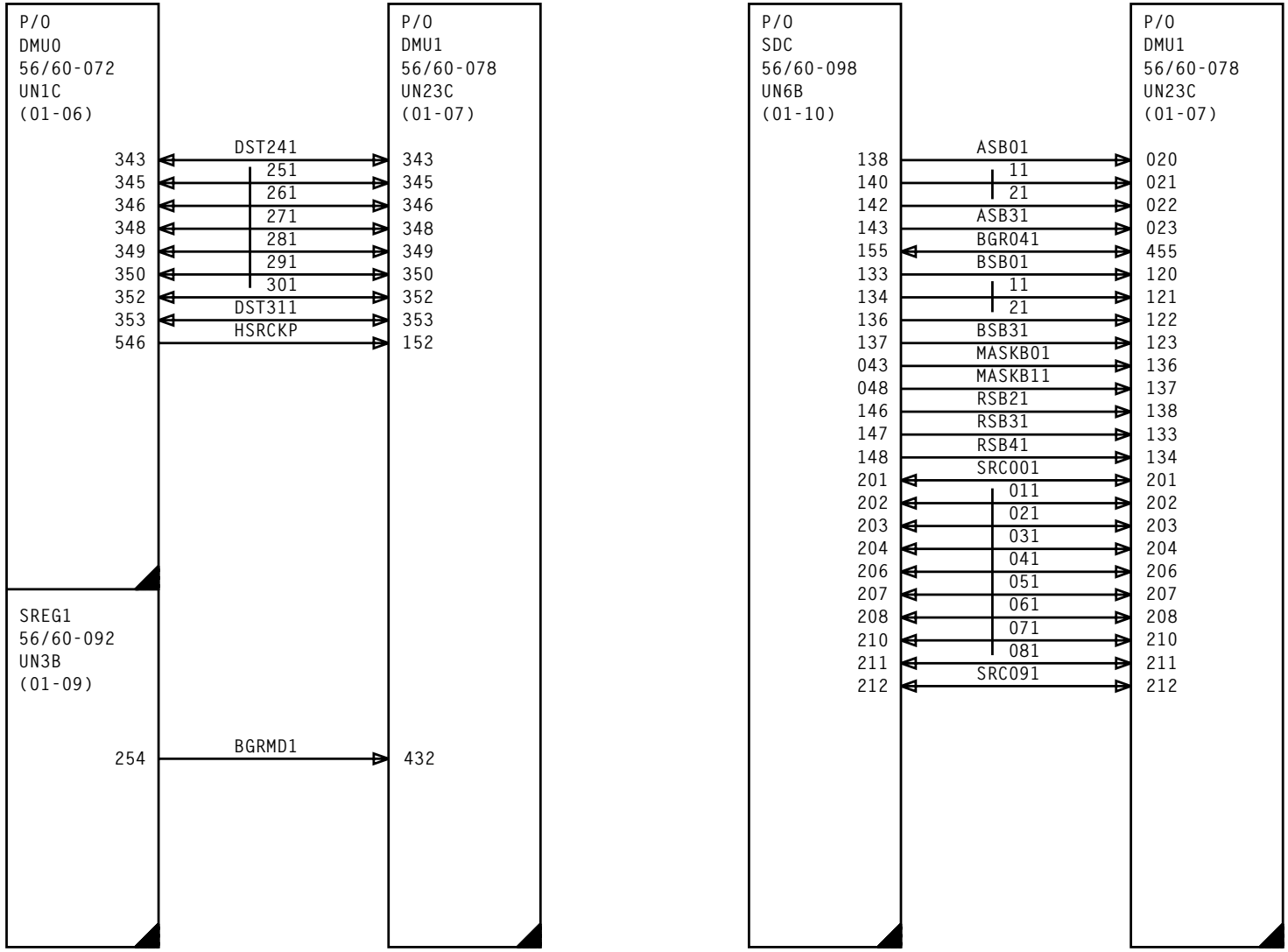
DATA MANIPULATION UNIT 0 FAILURES





CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 1 FAILURES



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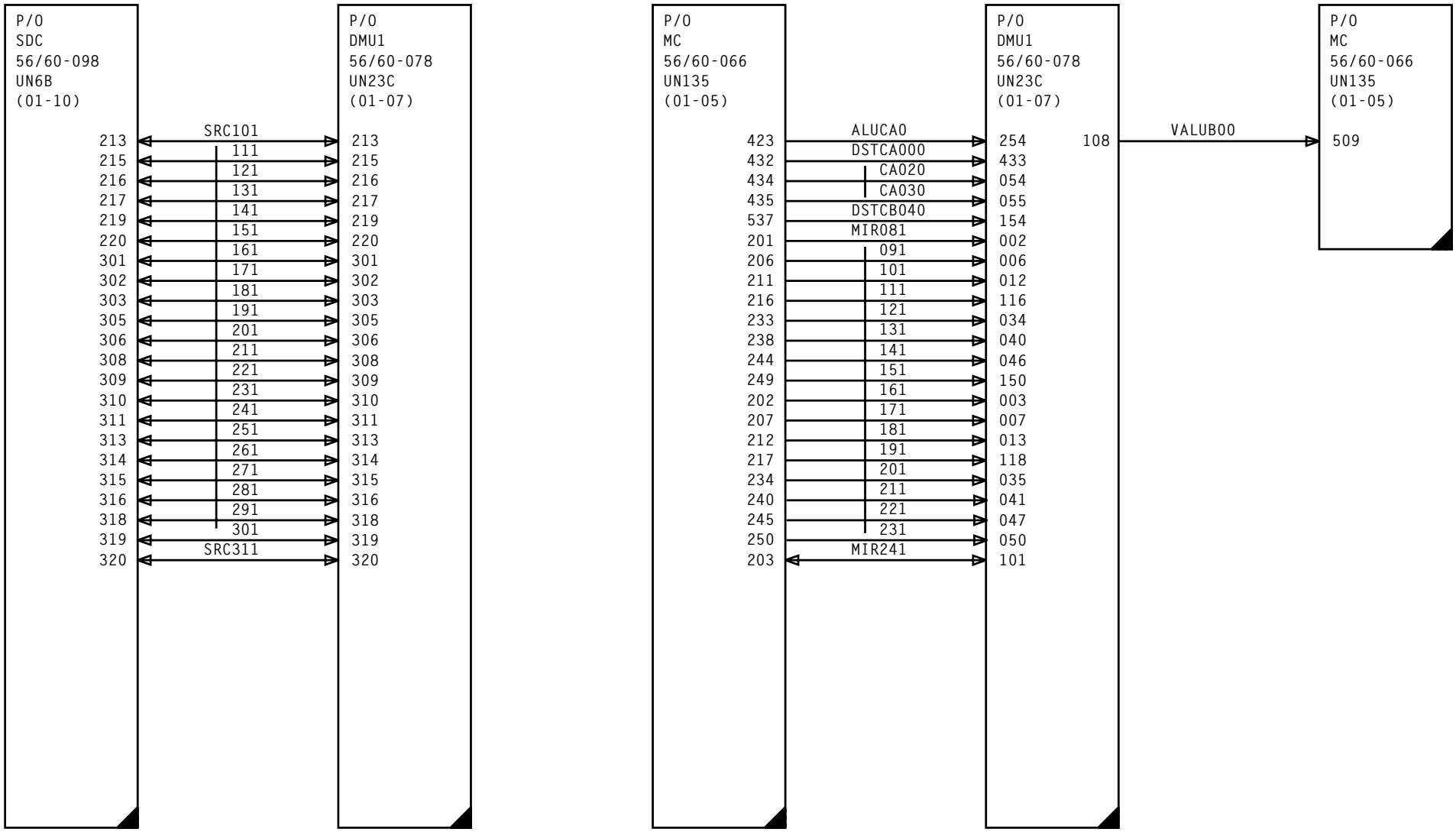
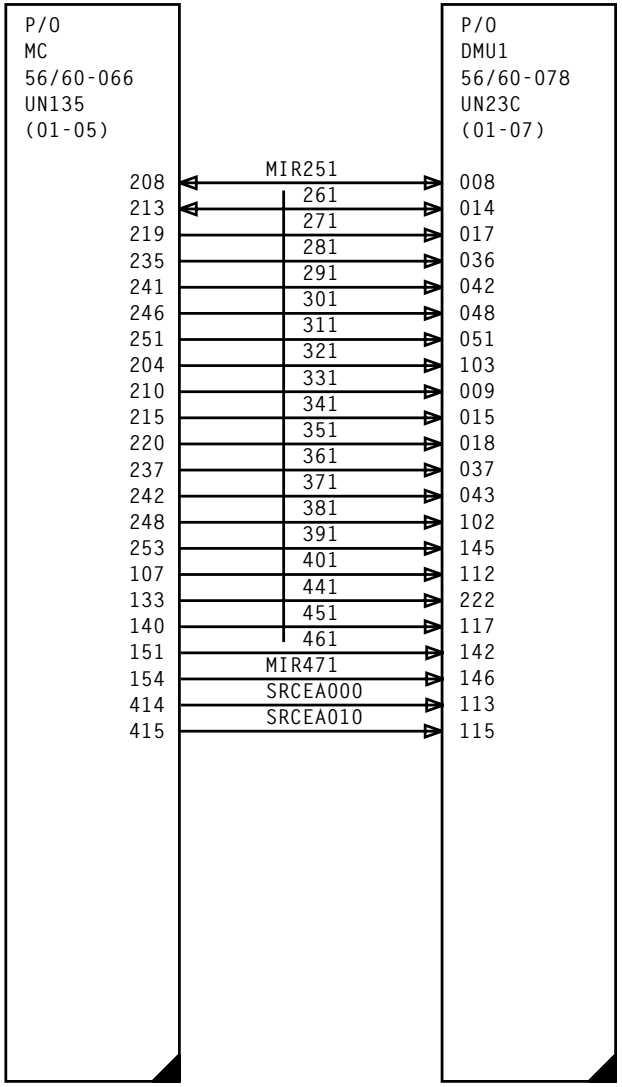
DATA MANIPULATION UNIT 1 FAILURES



CENTRAL CONTROL (CC) PHASES 13–22, 39, AND 52–54
DATA MANIPULATION UNIT 1 FAILURES



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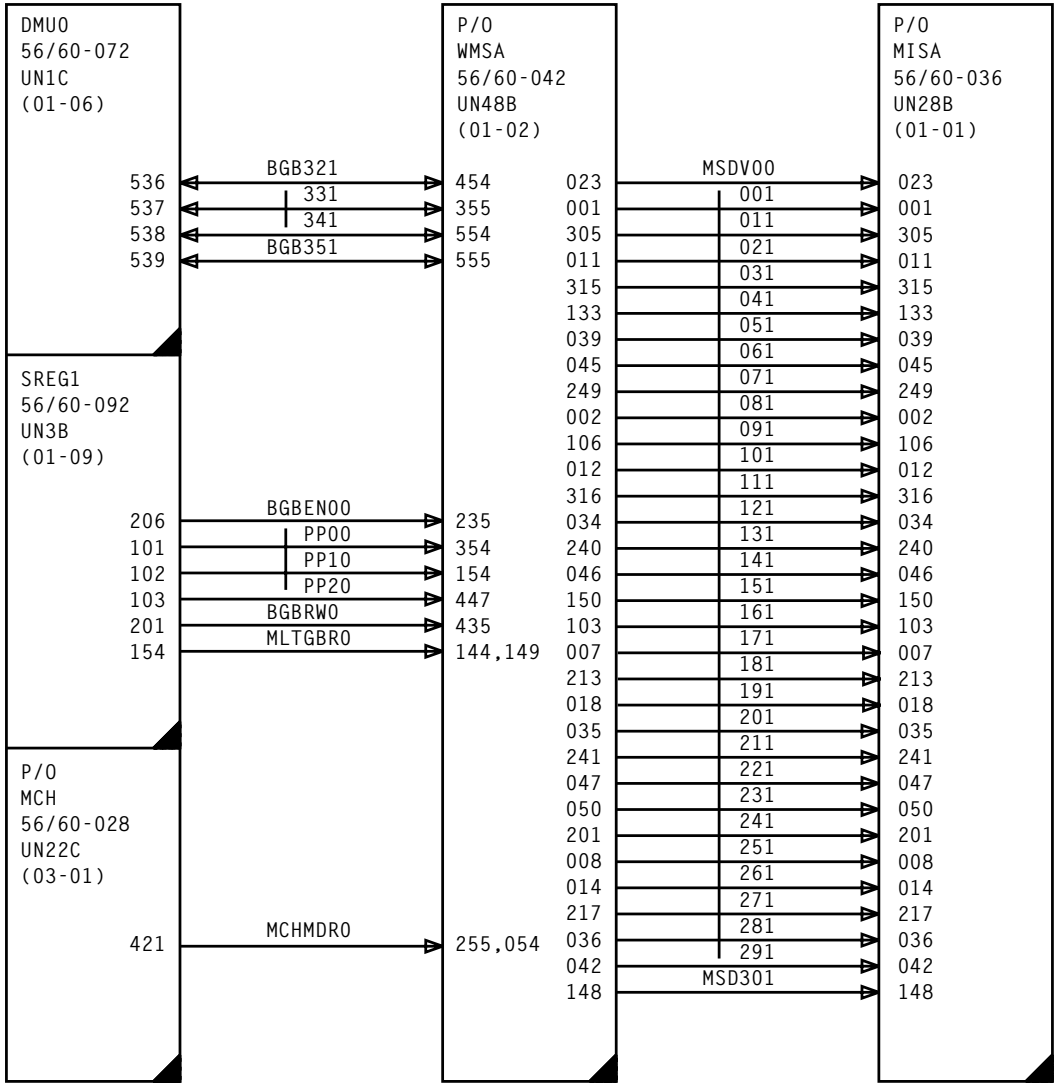
DATA MANIPULATION UNIT 1 FAILURES



CENTRAL CONTROL (CC) PHASES 30–38, 83–88, AND 90–92 WRITABLE MICROSTORE (WMS) SLOT 1 FAILURES

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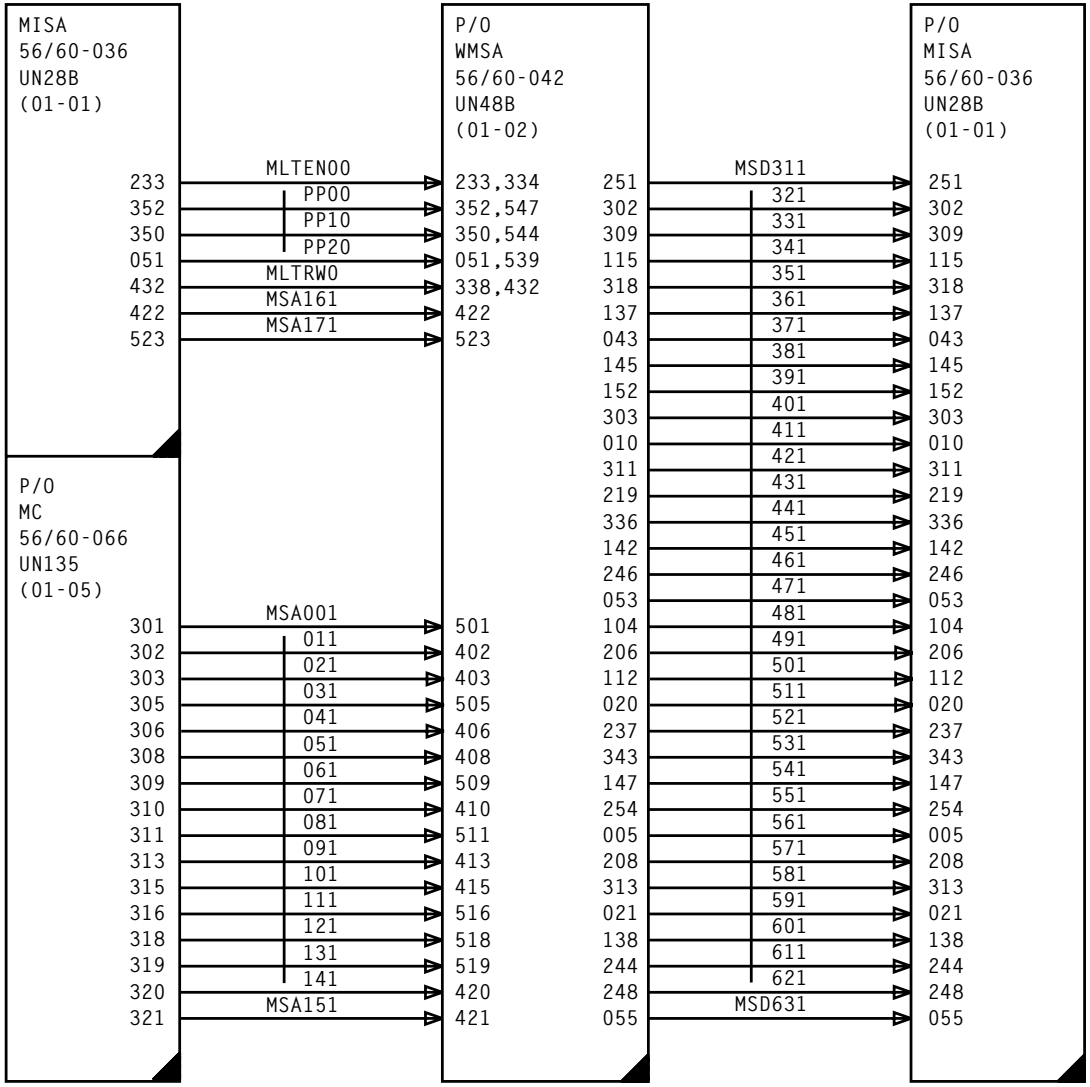
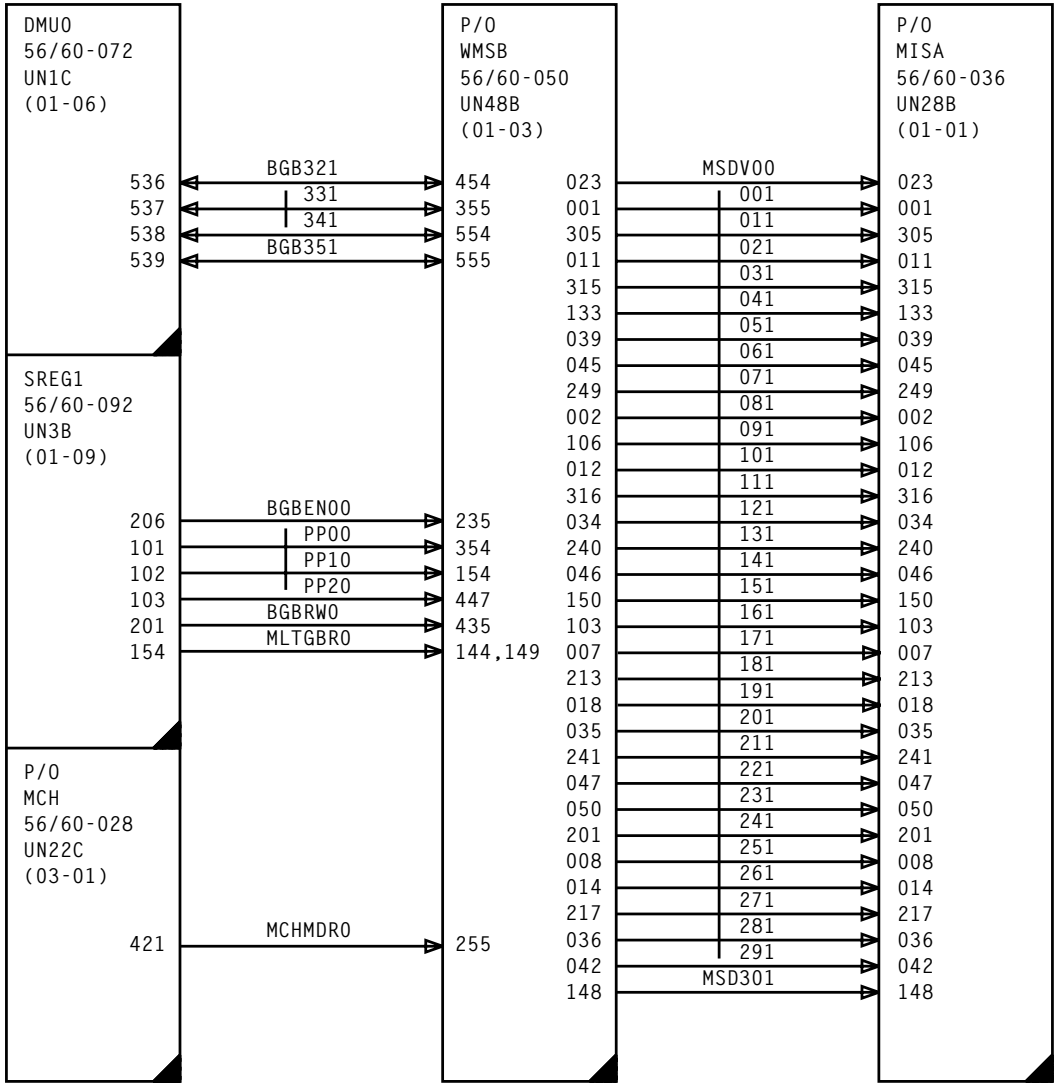
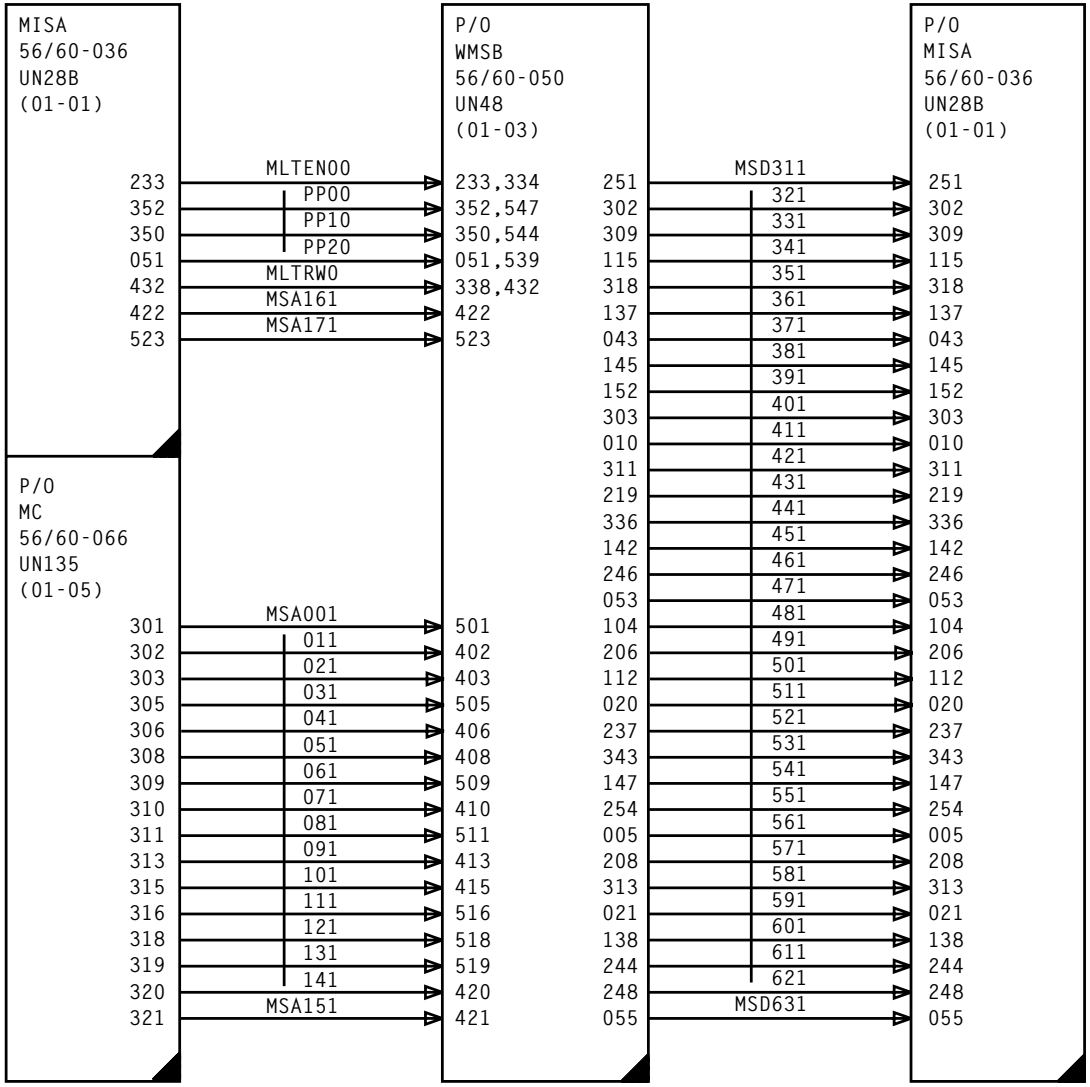


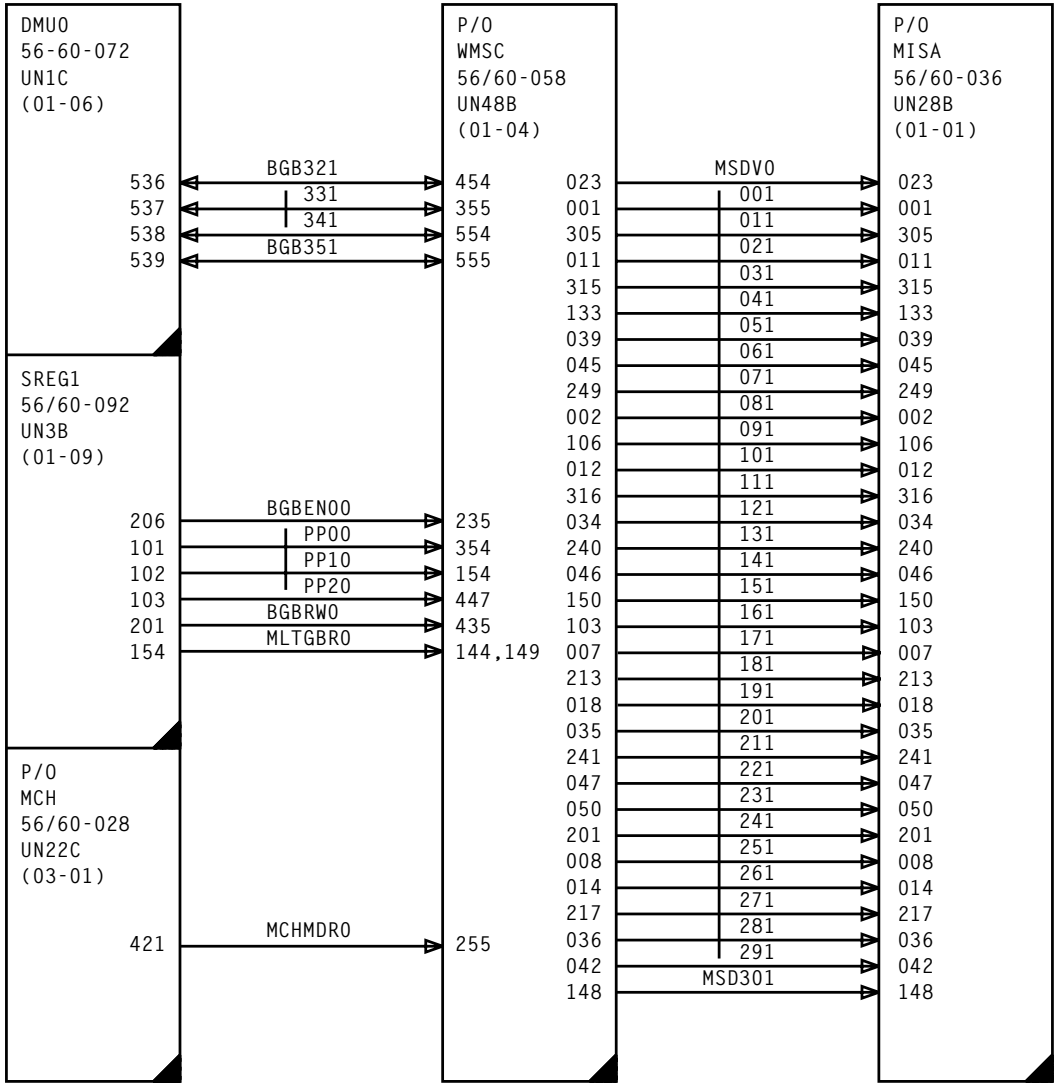
CENTRAL CONTROL (CC) PHASES 30-38, 83—88, AND 90—92 WRITABLE MICROSTORE (WMS) SLOT 1 FAILURES



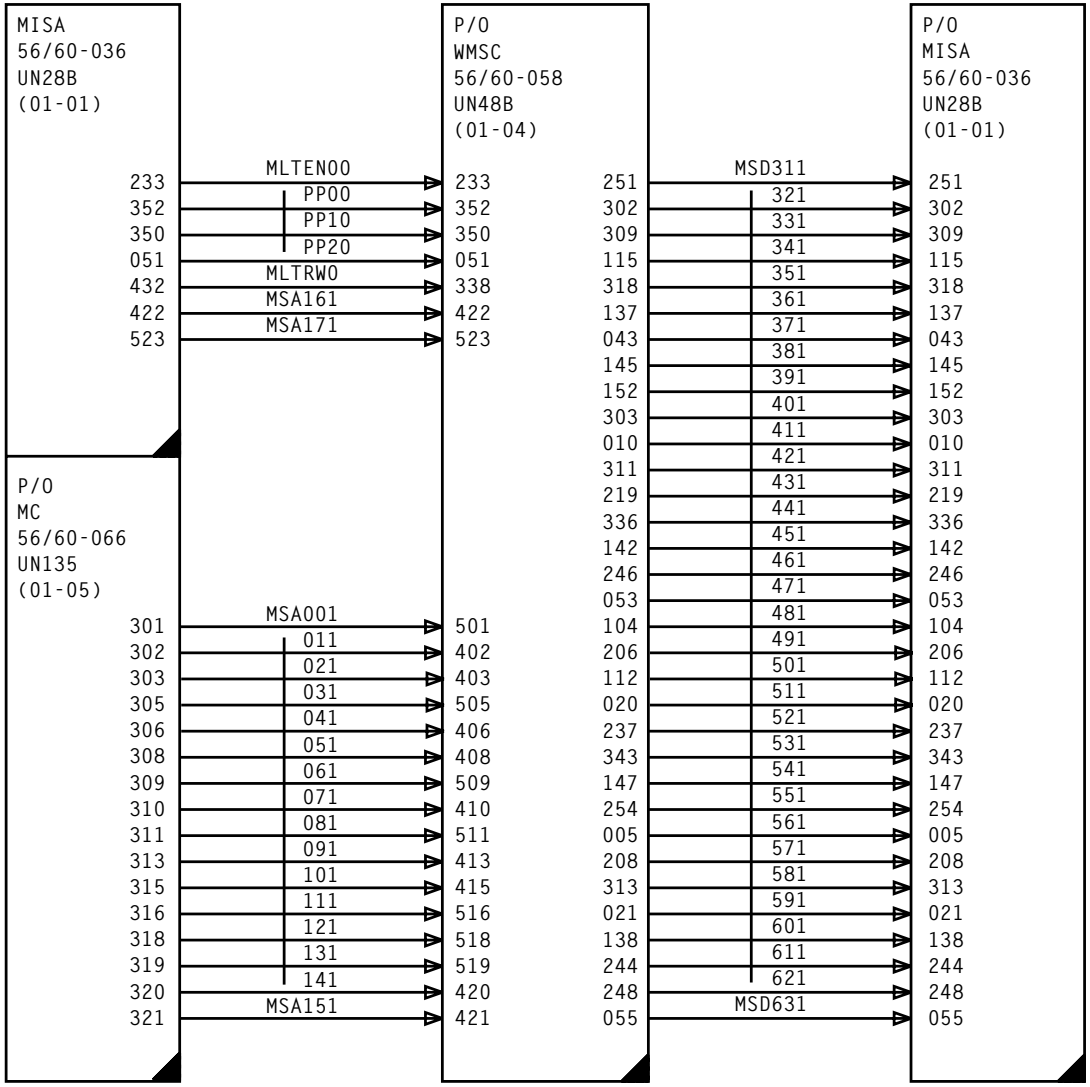
CENTRAL CONTROL (CC) PHASES 30-38, 83—88, AND 90—92
WRITABLE MICROSTORE (WMS) SLOT 2 FAILURES



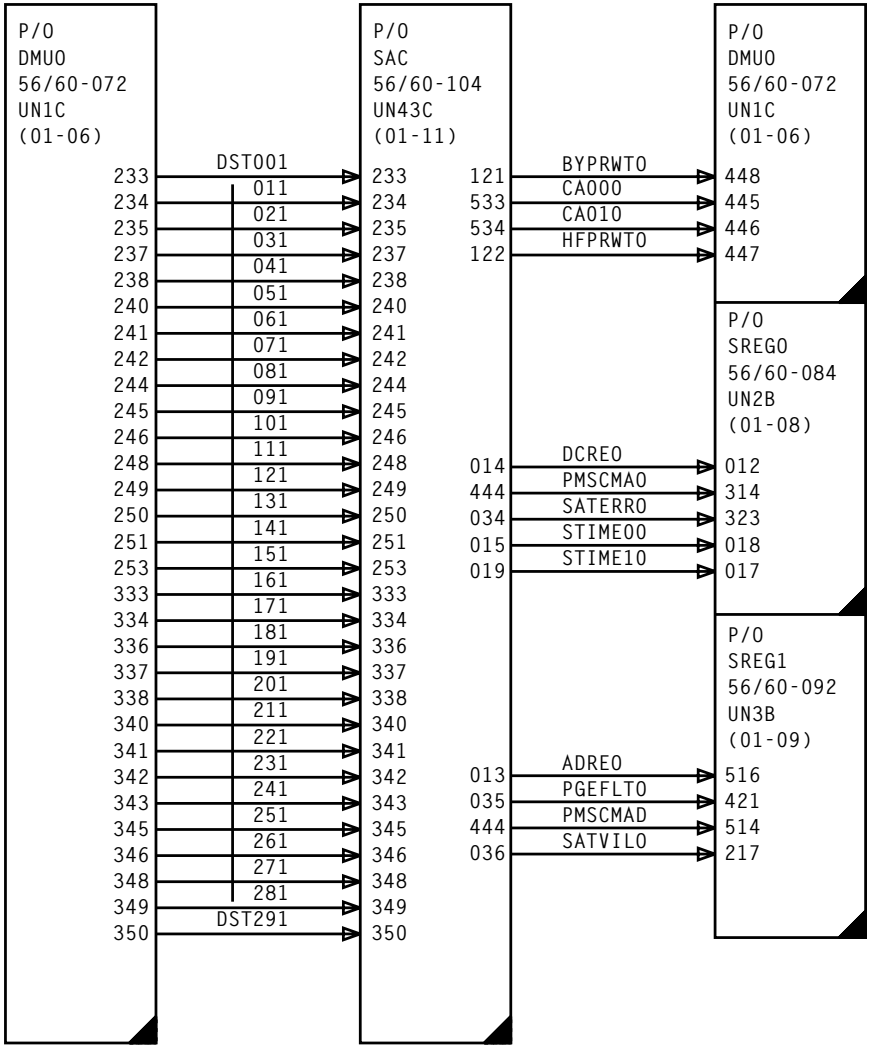
CENTRAL CONTROL (CC) PHASES 30-38, 83–88, AND 90–92
WRITABLE MICROSTORE (WMS) SLOT 2 FAILURES



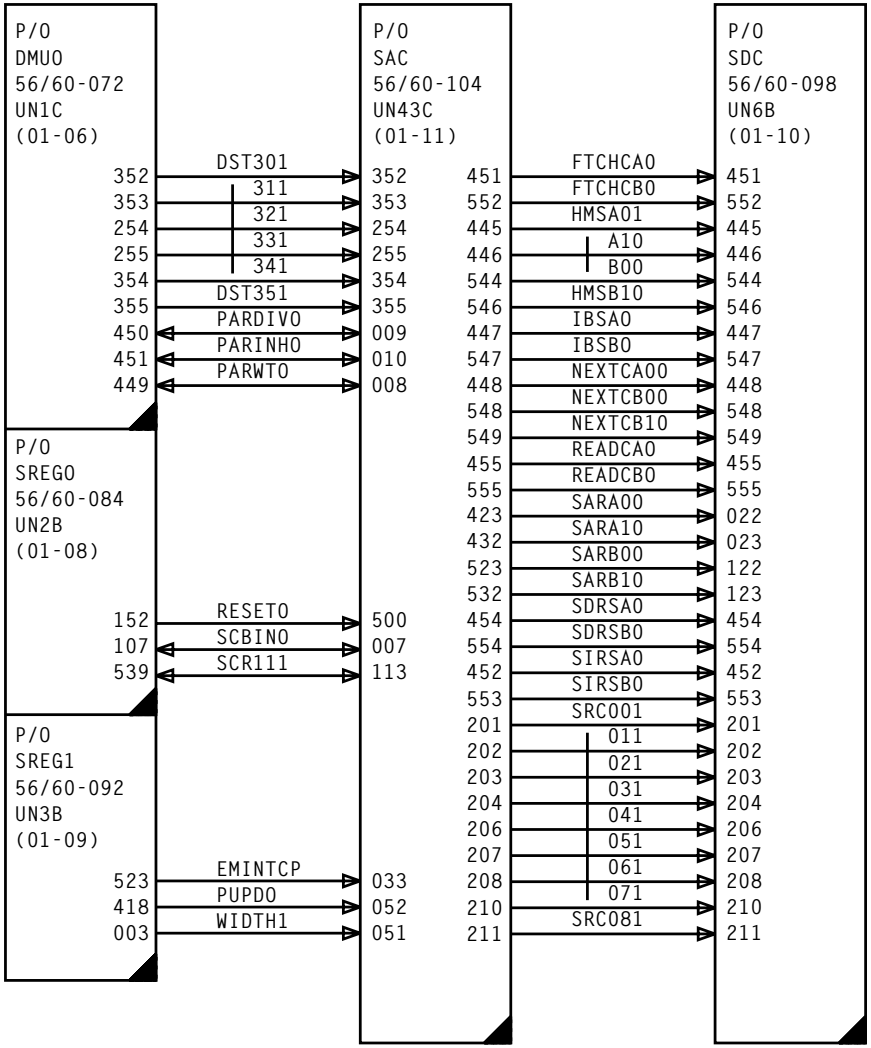
CENTRAL CONTROL (CC) PHASES 30-38, 83—88, AND 90—92
WRITABLE MICROSTORE (WMS) SLOT 3 FAILURES



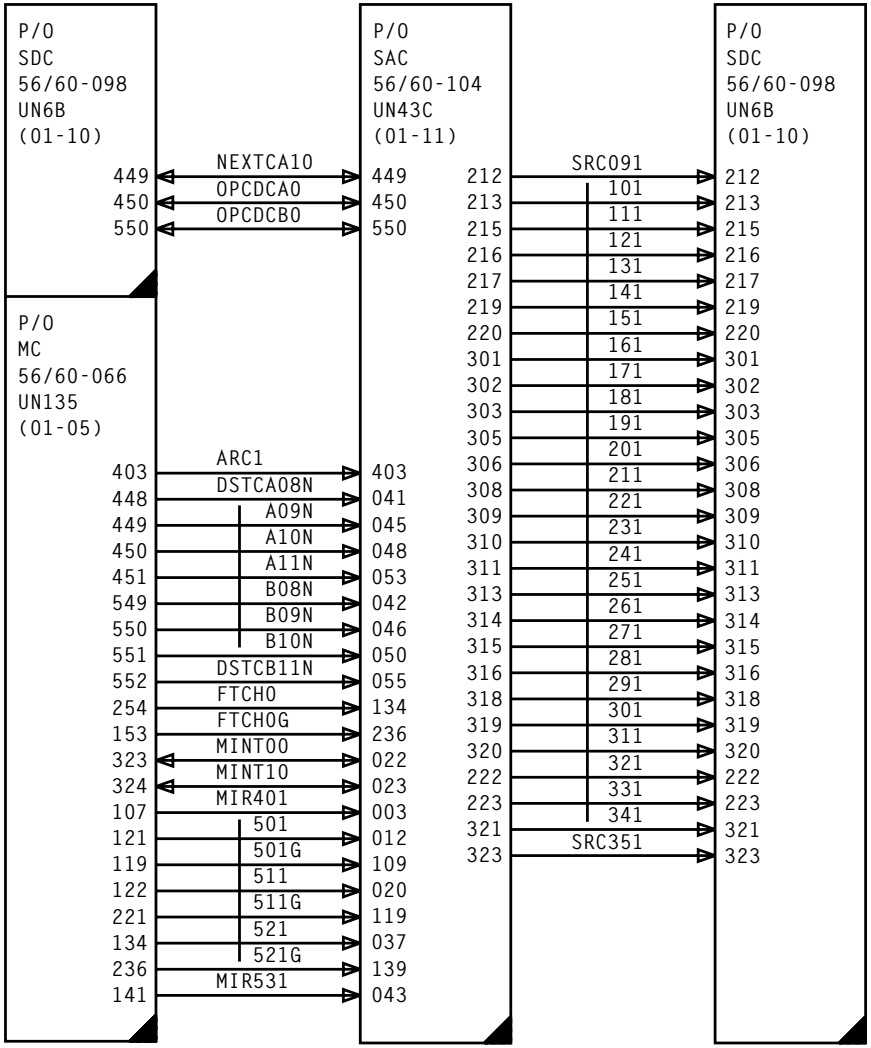
CENTRAL CONTROL (CC) PHASES 30-38, 83—88, AND 90—92
WRITABLE MICROSTORE (WMS) SLOT 3 FAILURES



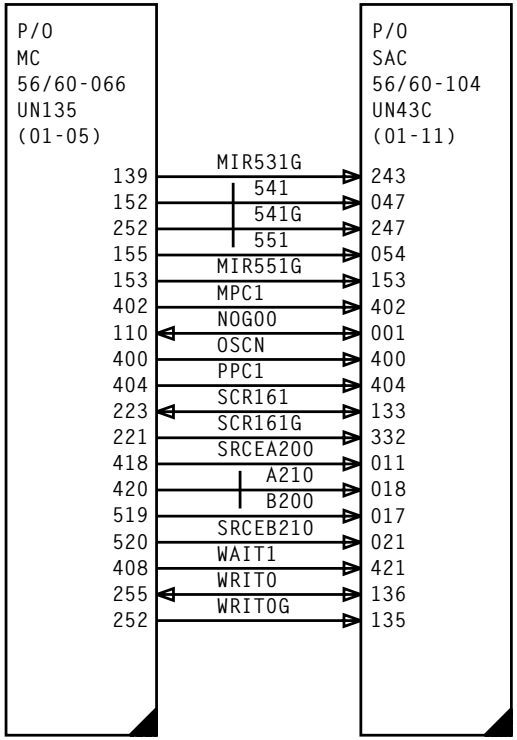
CENTRAL CONTROL (CC) PHASES 40-42 AND 44—49
STORE ADDRESS CONTROL (SAC) FAILURES



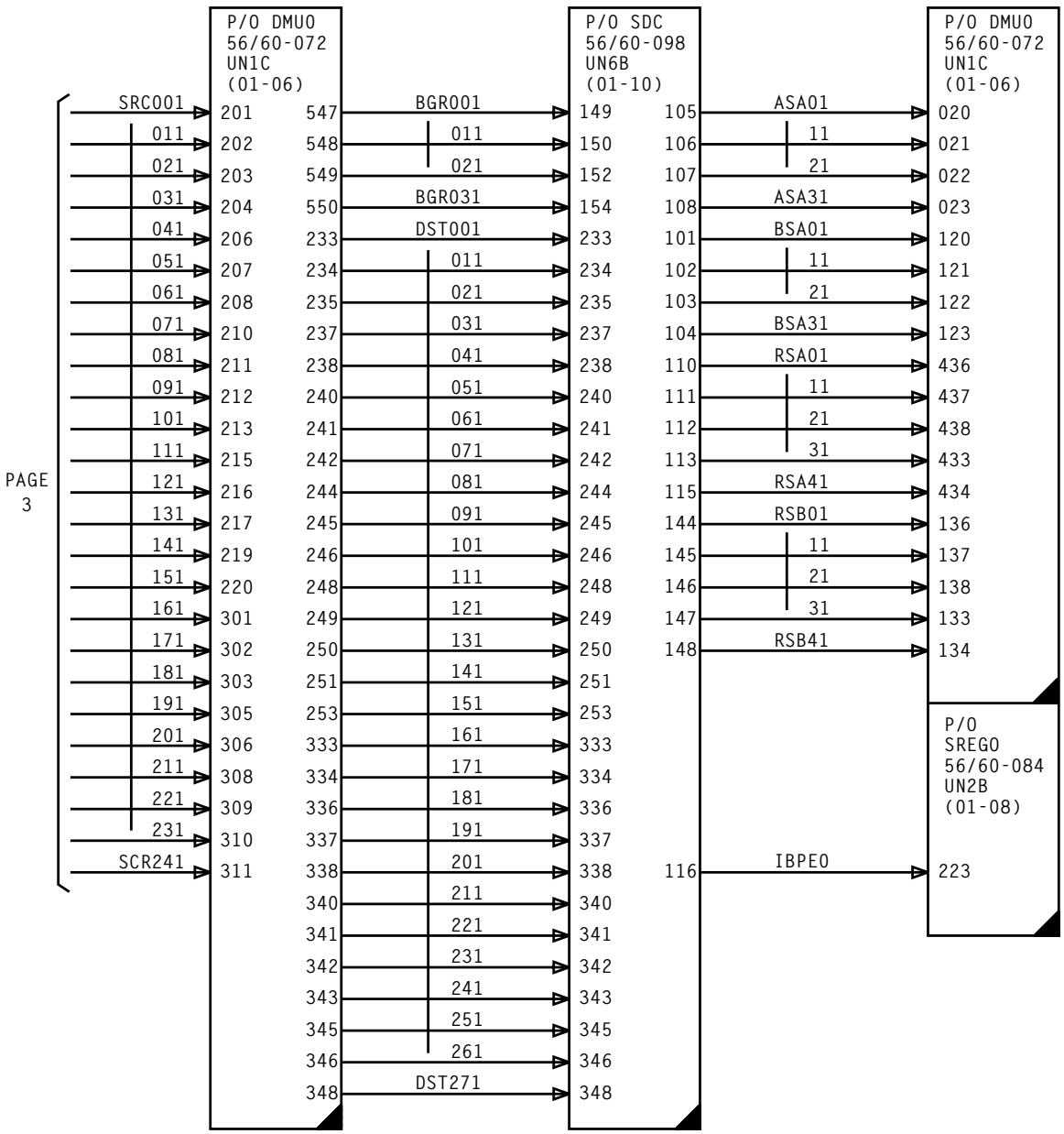
CENTRAL CONTROL (CC) PHASES 40-42 AND 44—49
STORE ADDRESS CONTROL (SAC) FAILURES



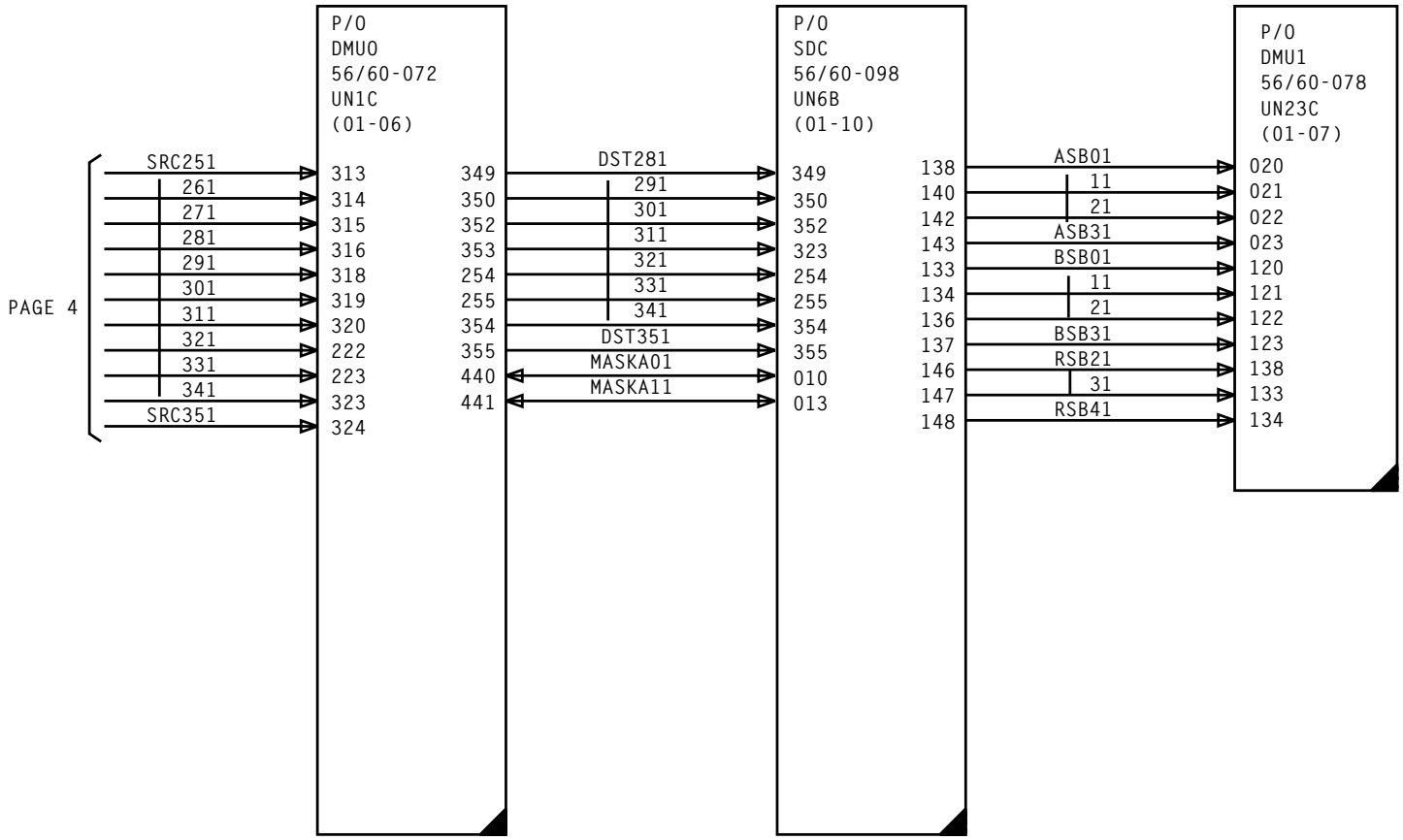
CENTRAL CONTROL (CC) PHASES 40-42 AND 44—49
STORE ADDRESS CONTROL (SAC) FAILURES



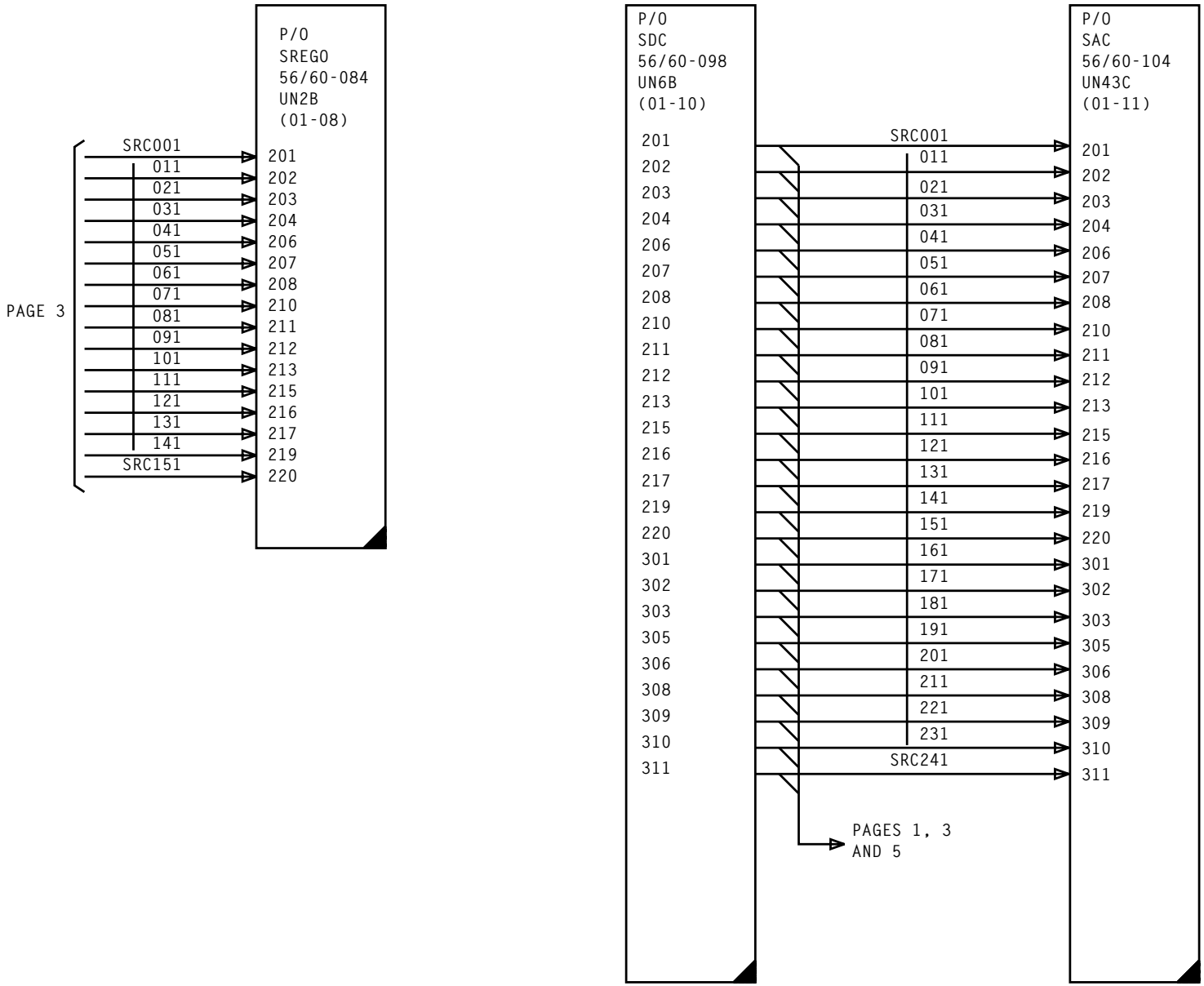
CENTRAL CONTROL (CC) PHASES 40-42 AND 44—49
STORE ADDRESS CONTROL (SAC) FAILURES



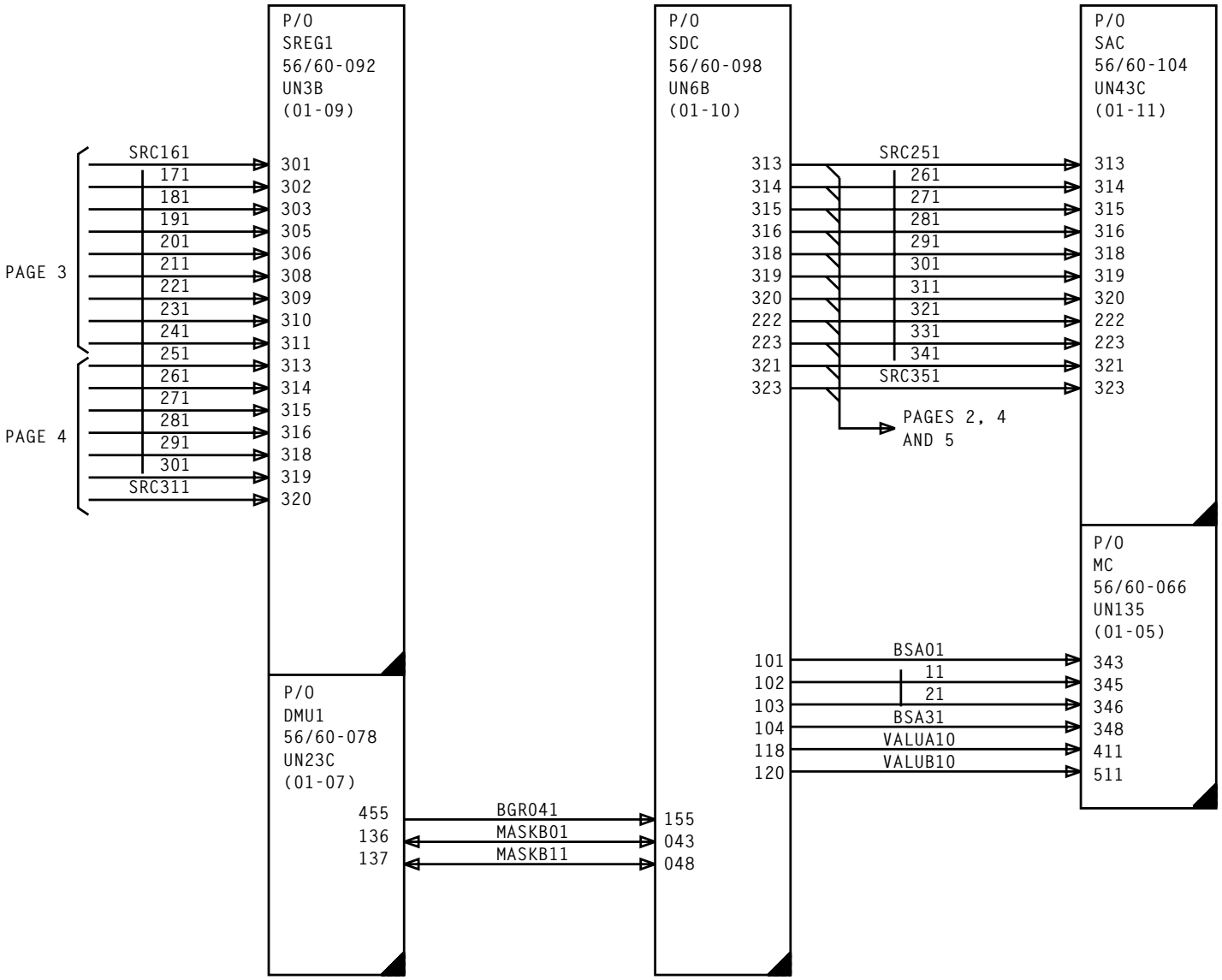
CENTRAL CONTROL (CC) PHASES 41, 43, AND 46—49
STORE DATA CONTROL (SDC) FAILURES



CENTRAL CONTROL (CC) PHASES 41, 43, AND 46—49
STORE DATA CONTROL (SDC) FAILURES



CENTRAL CONTROL (CC) PHASES 41, 43, AND 46—49
STORE DATA CONTROL (SDC) FAILURES



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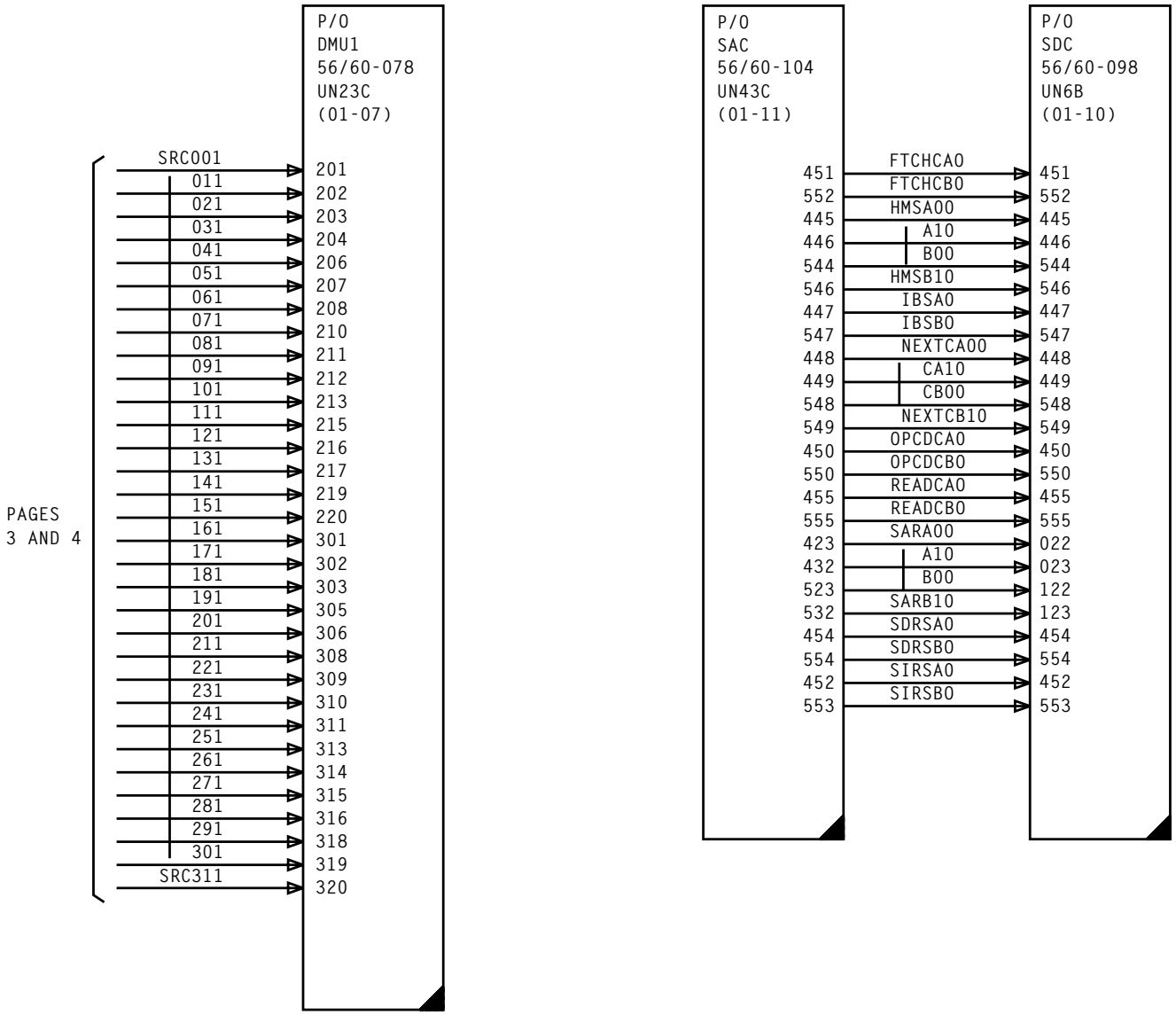
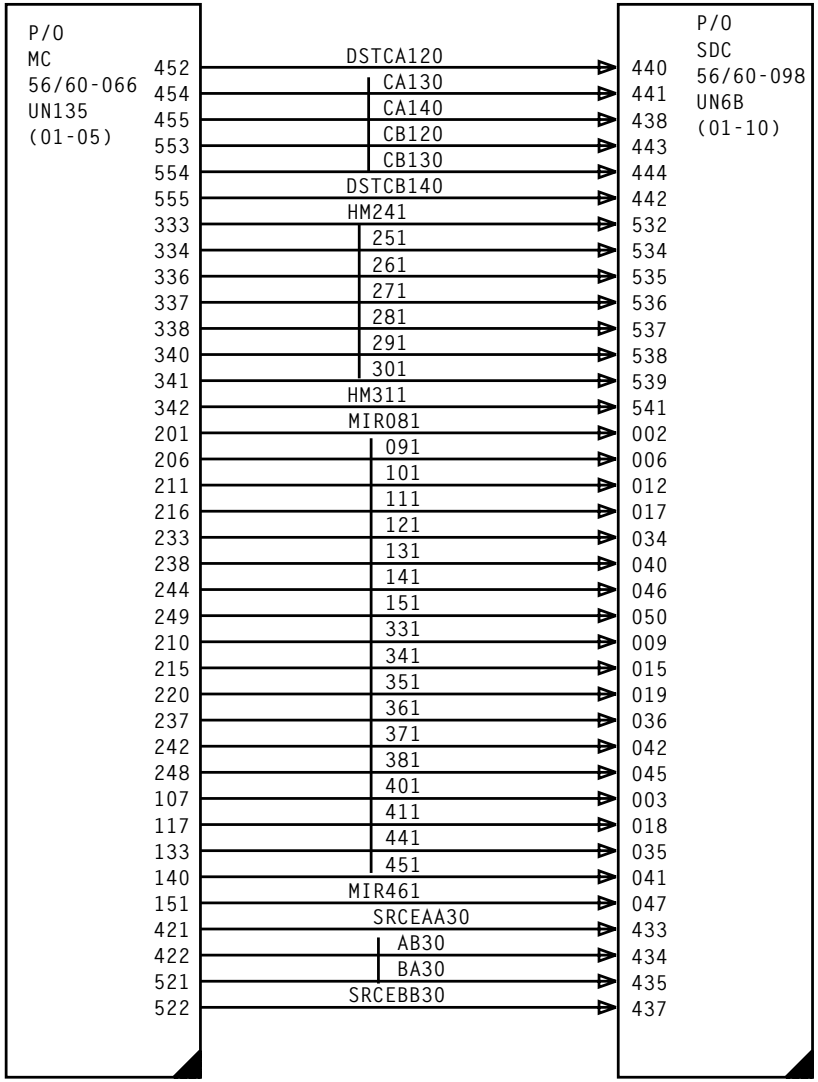
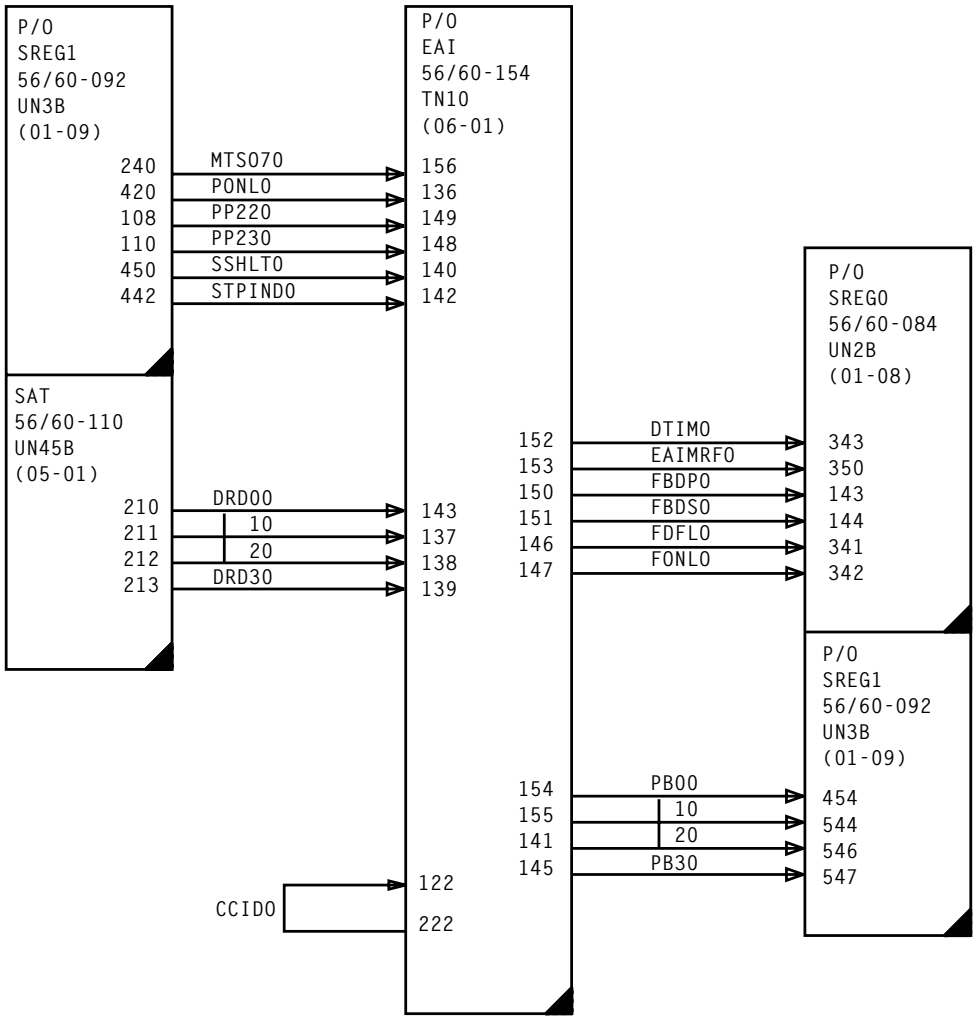
STORE DATA CONTROL (SDC) FAILURES



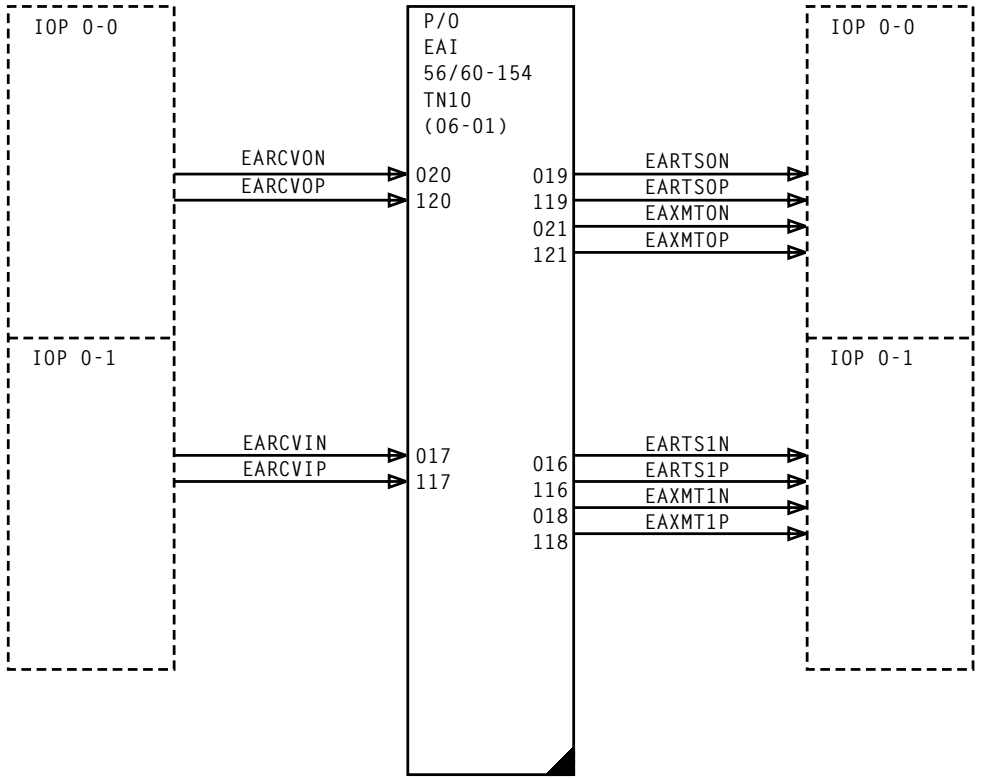
CENTRAL CONTROL (CC) PHASES 41, 43, AND 46—49
STORE DATA CONTROL (SDC) FAILURES



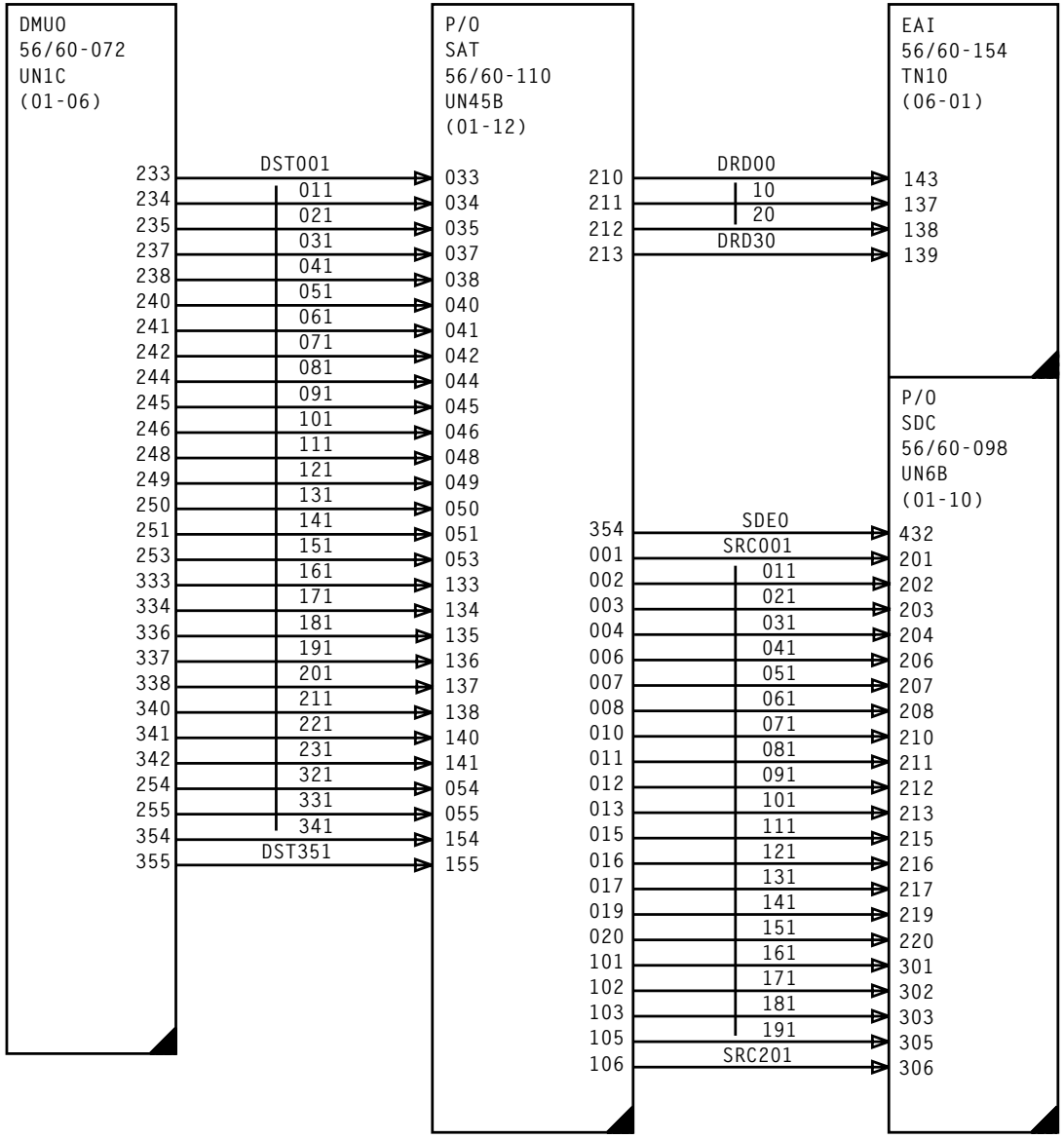
CENTRAL CONTROL (CC) PHASES 41, 43, AND 46—49
STORE DATA CONTROL (SDC) FAILURES



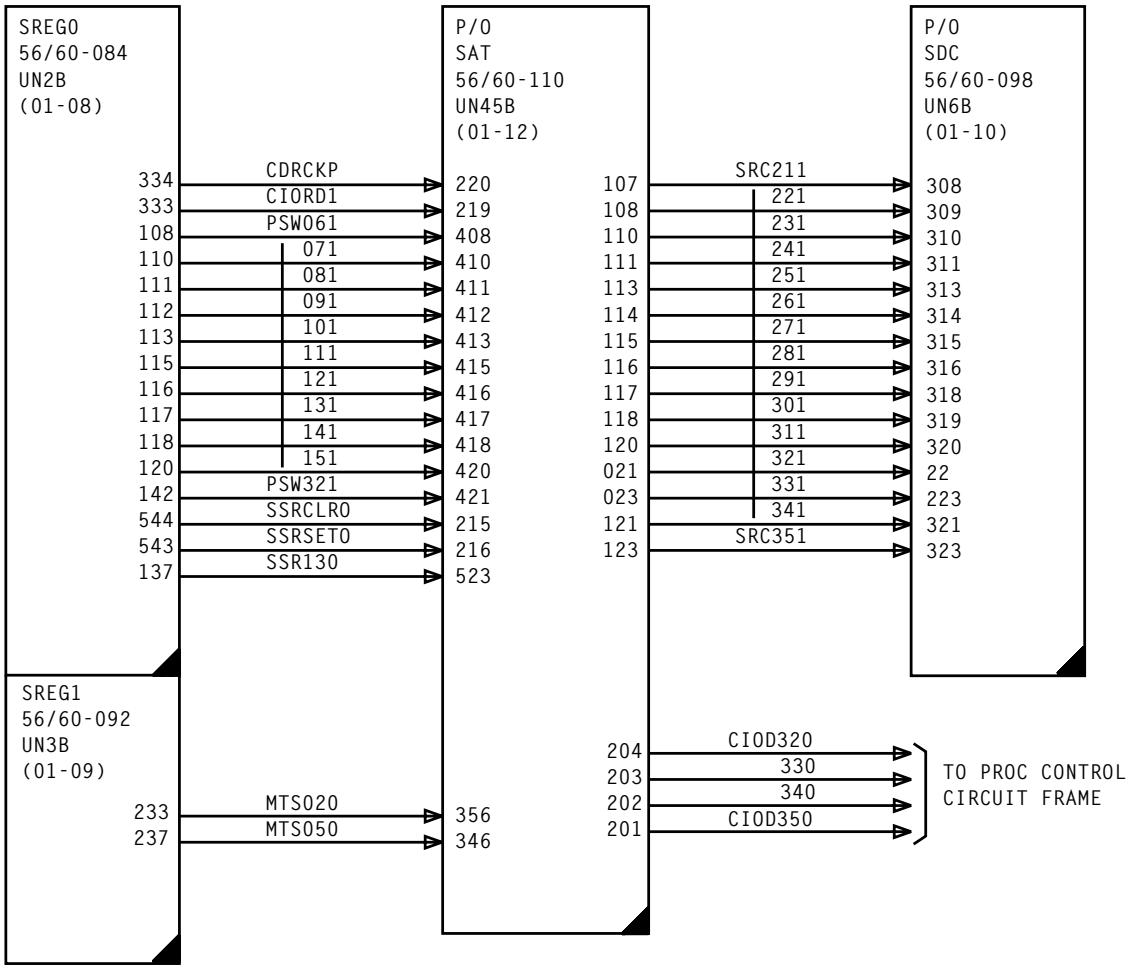
CENTRAL CONTROL (CC) PHASE 93 EMERGENCY ACTION INTERFACE (EAI) DISPLAY FAILURES



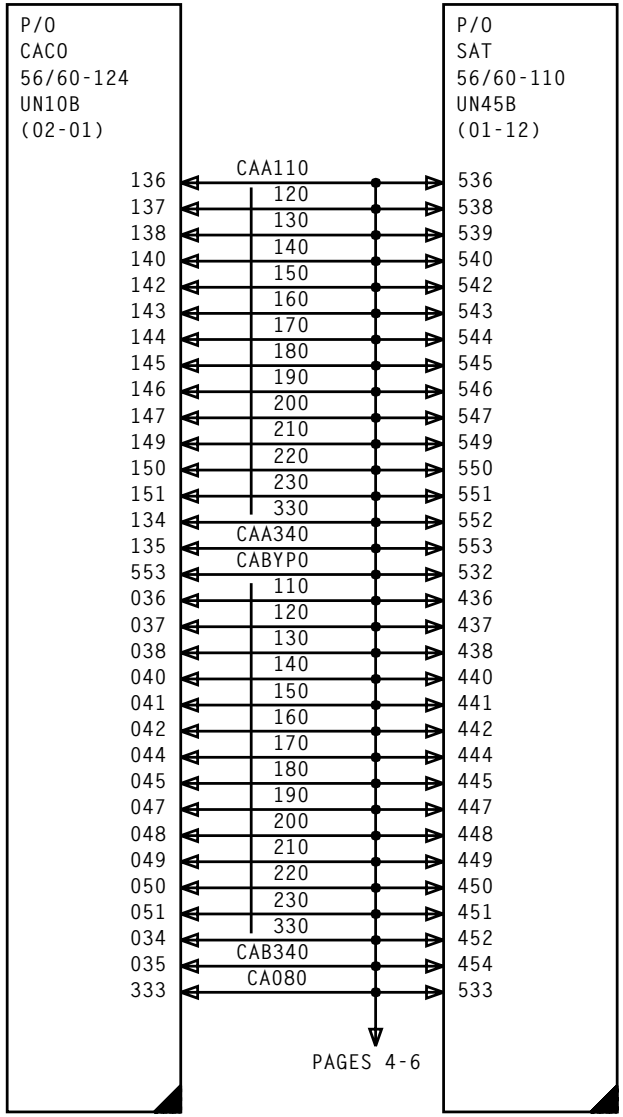
CENTRAL CONTROL (CC) PHASE 93 EMERGENCY ACTION INTERFACE (EAI) DISPLAY FAILURES



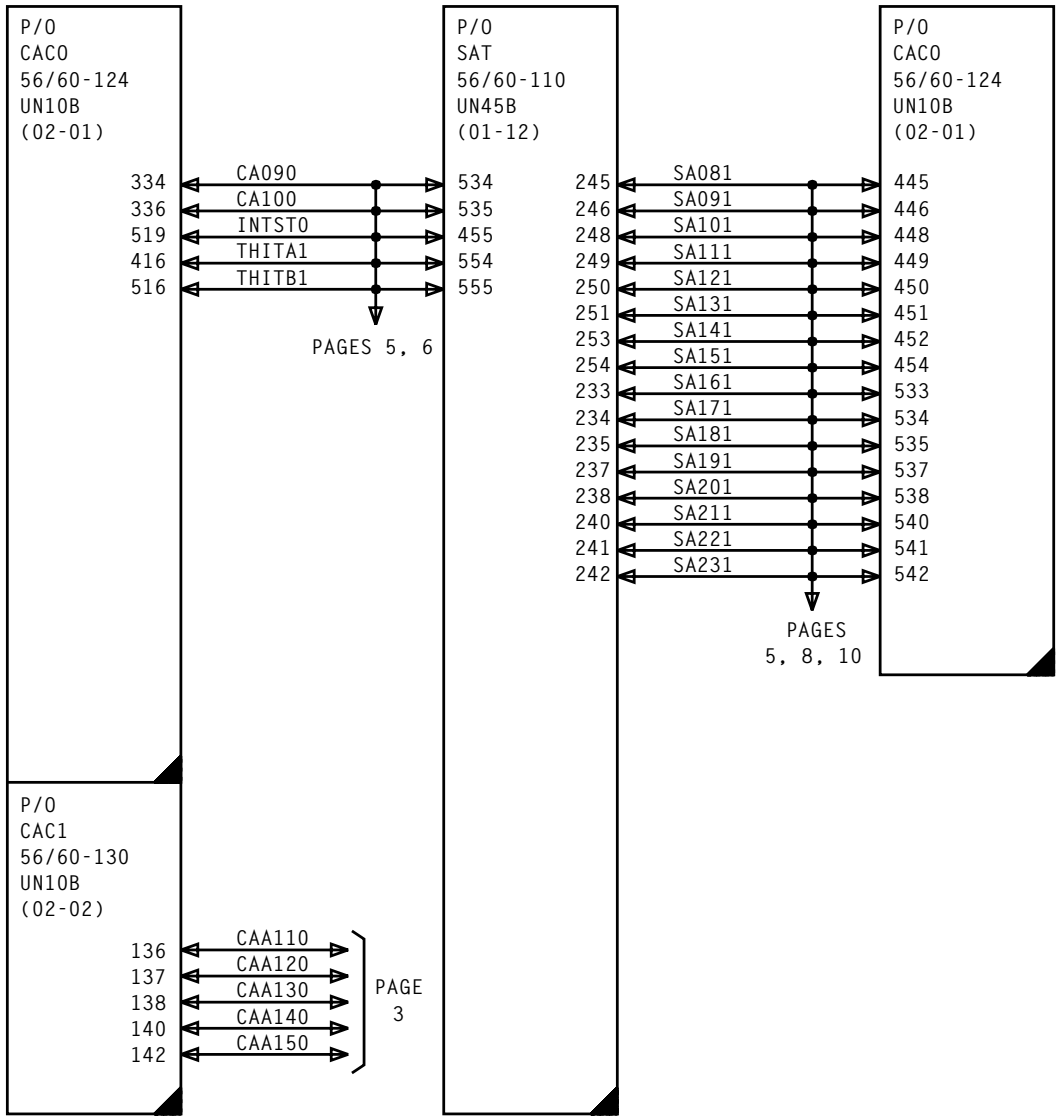
CONTROL UNIT (CU) — STORE ADDRESS TRANSLATOR (SAT)
PHASES 1-10 FAILURES



CONTROL UNIT (CU) — STORE ADDRESS TRANSLATOR (SAT)
PHASES 1-10 FAILURES



CONTROL UNIT (CU) – STORE ADDRESS TRANSLATOR (SAT)
PHASES 1-10 FAILURES



CONTROL UNIT (CU) — STORE ADDRESS TRANSLATOR (SAT)
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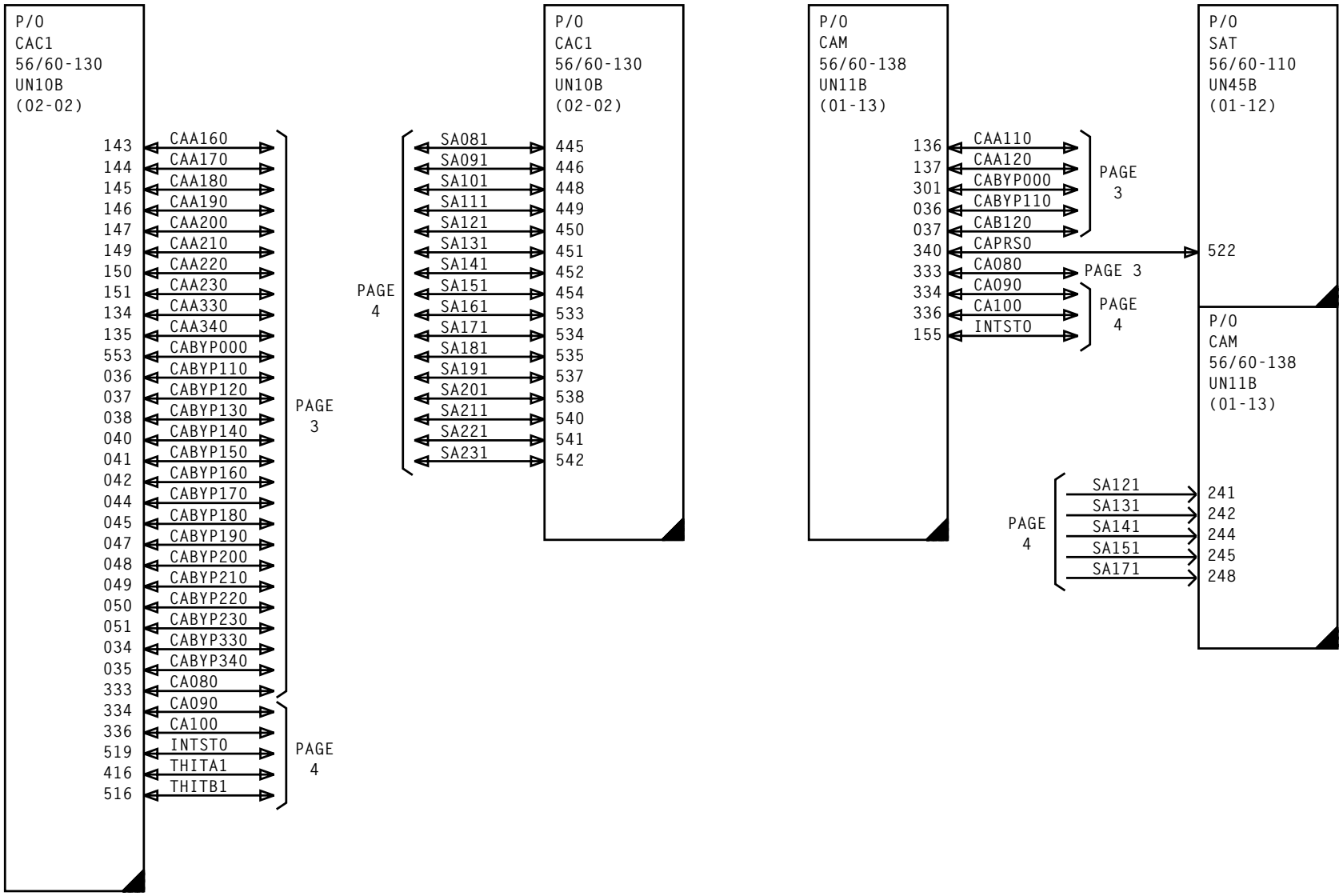
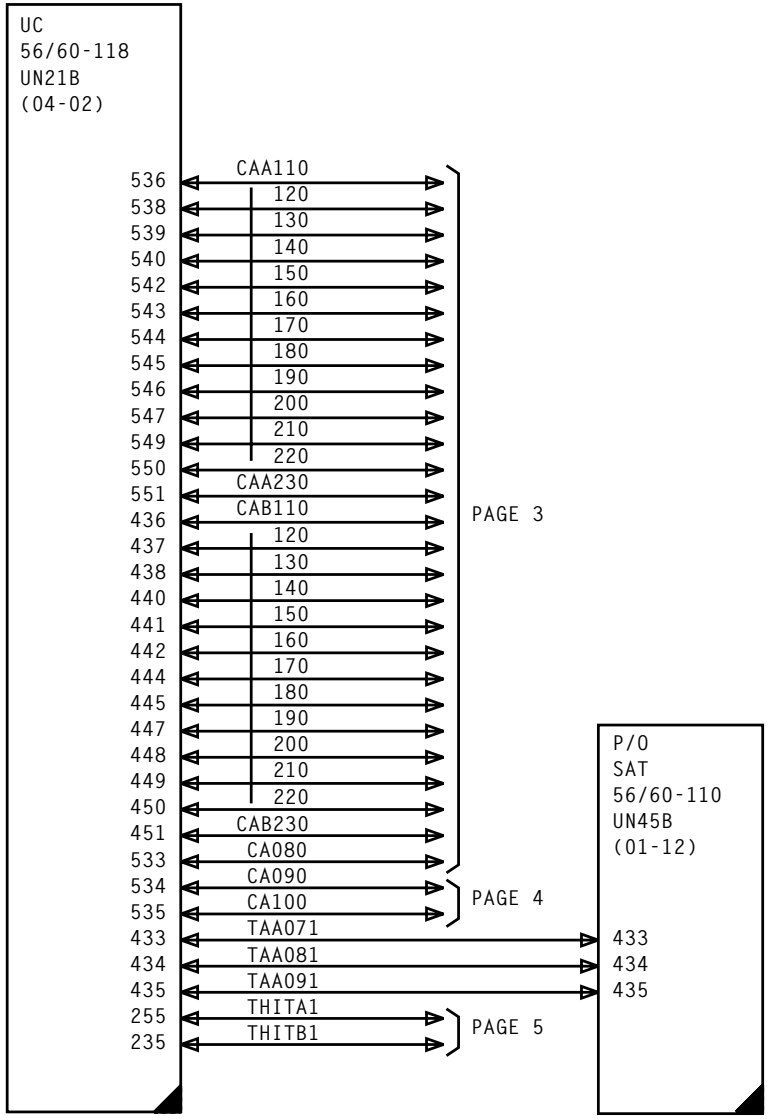


CONTROL UNIT (CU) — STORE ADDRESS TRANSLATOR (SAT)
PHASES 1-10 FAILURES



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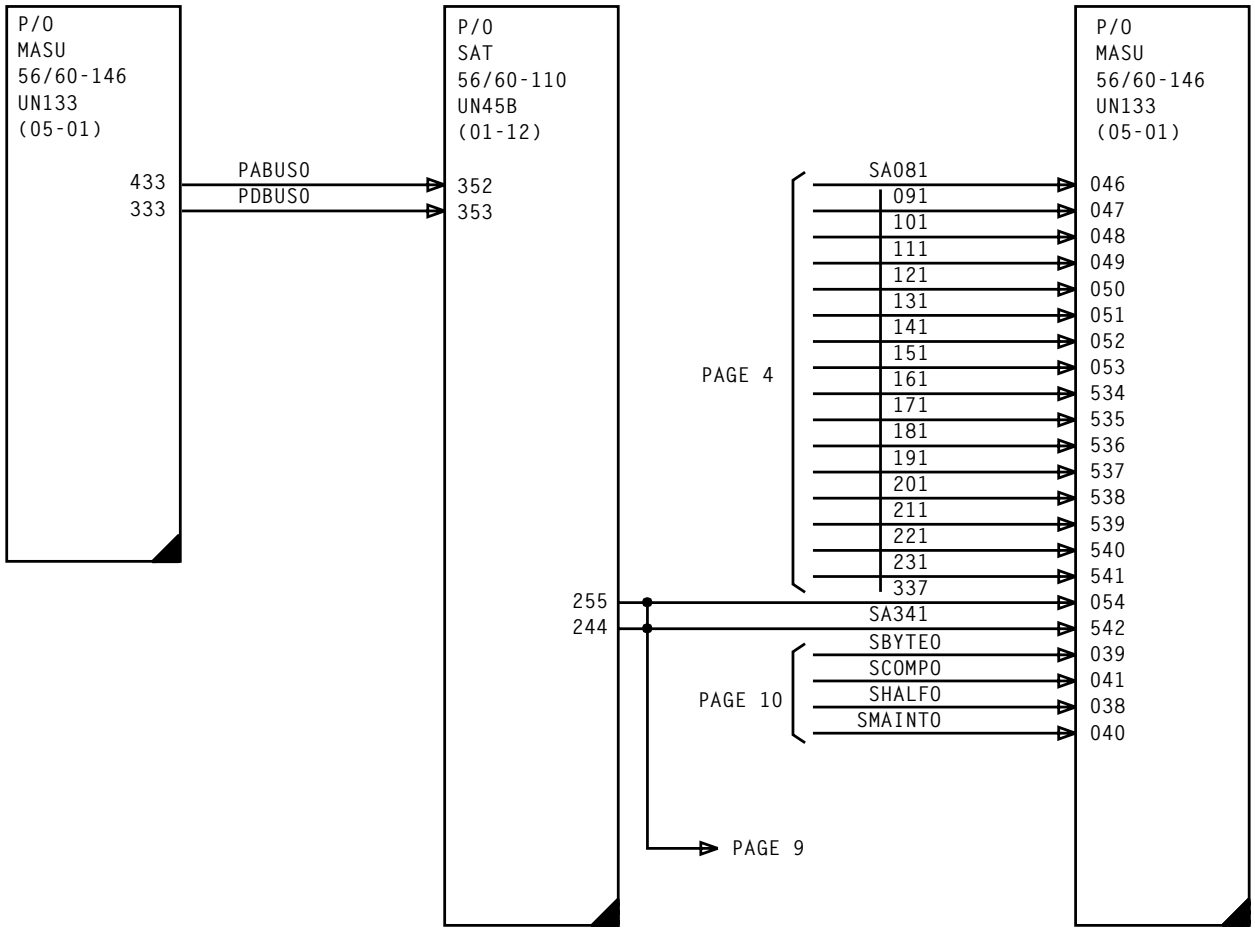
PHASES 1-10 FAILURES



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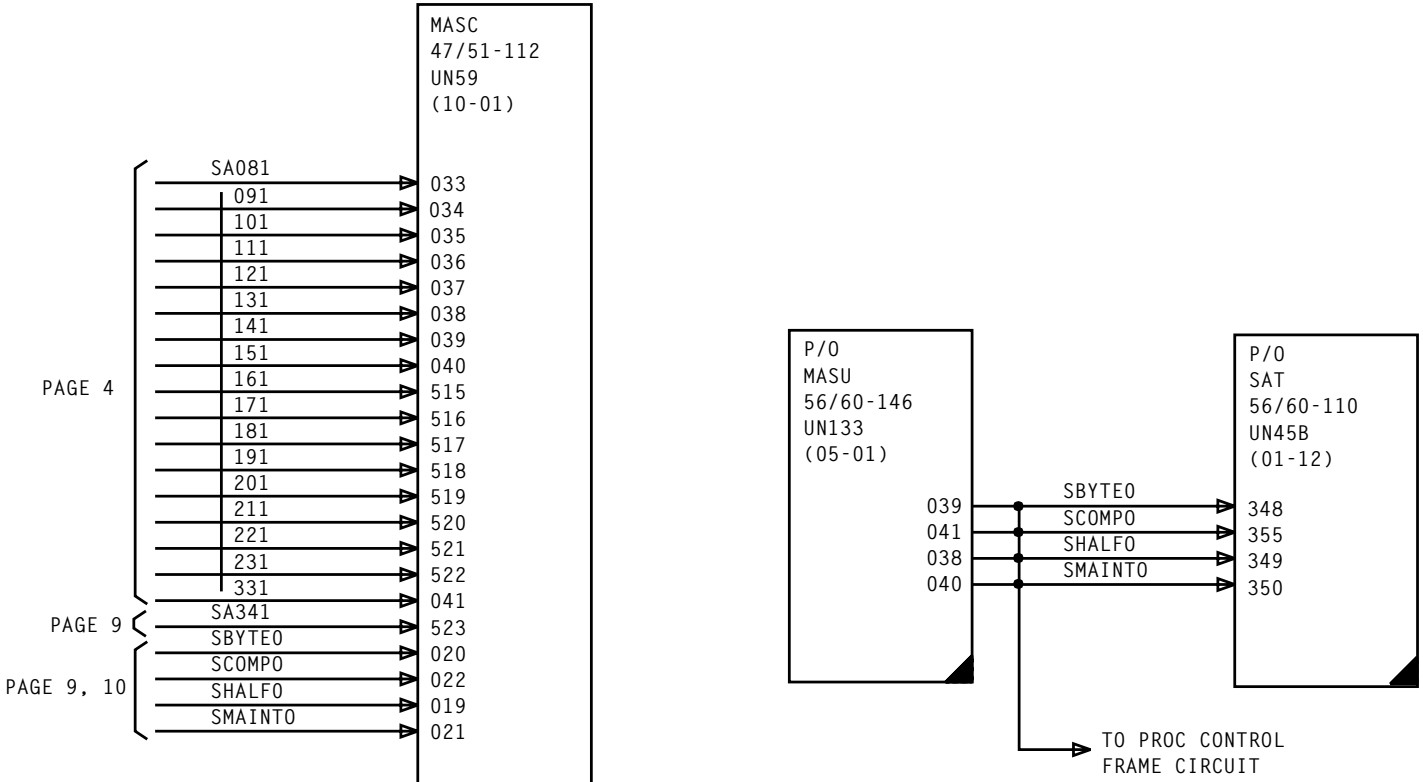
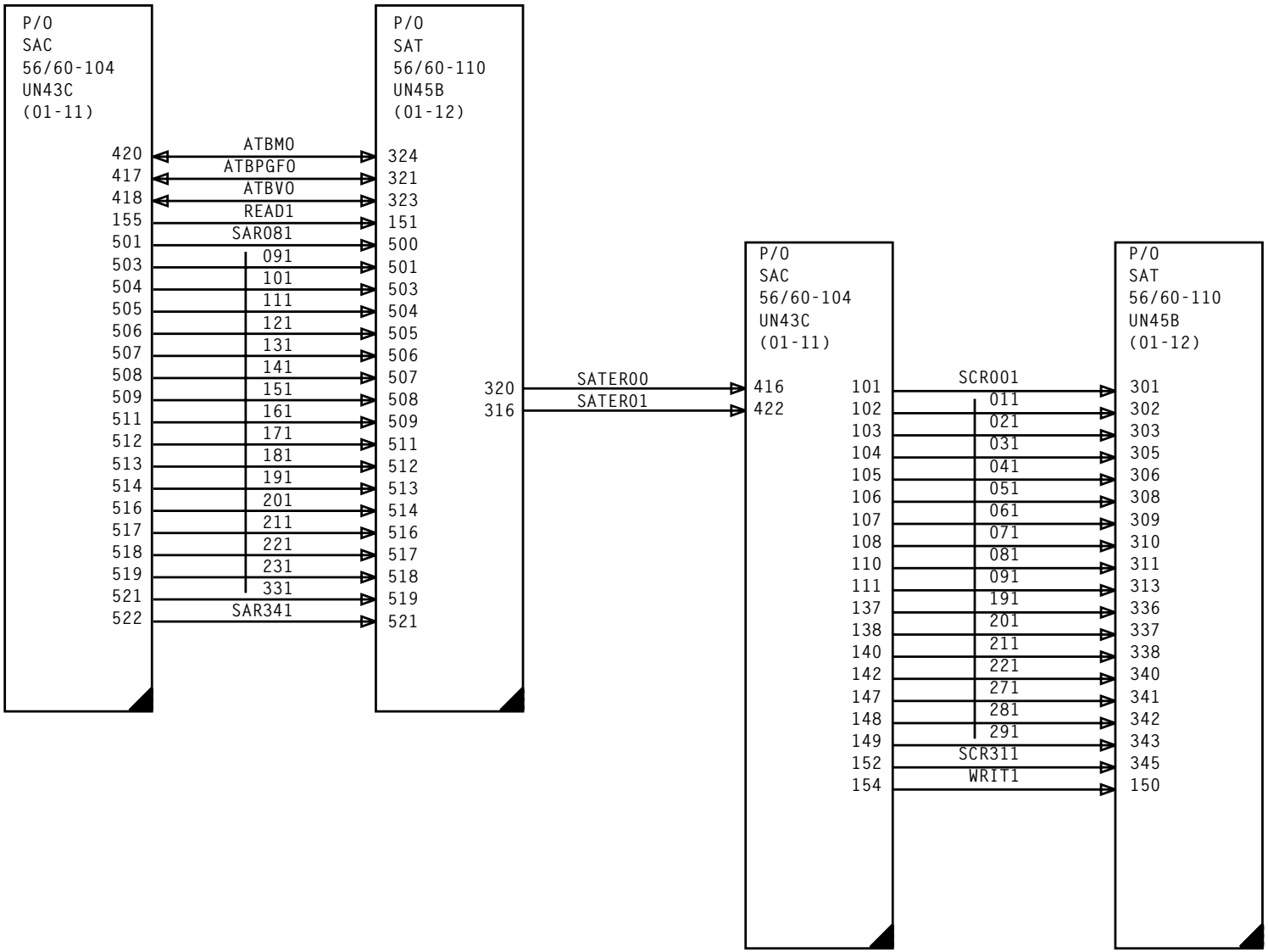
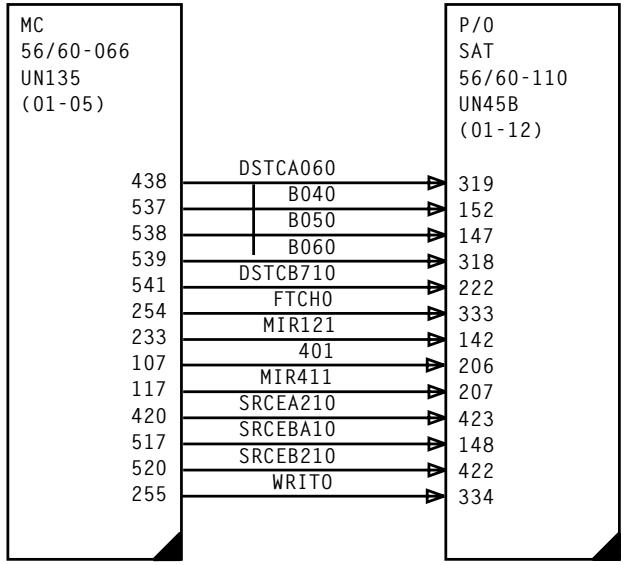


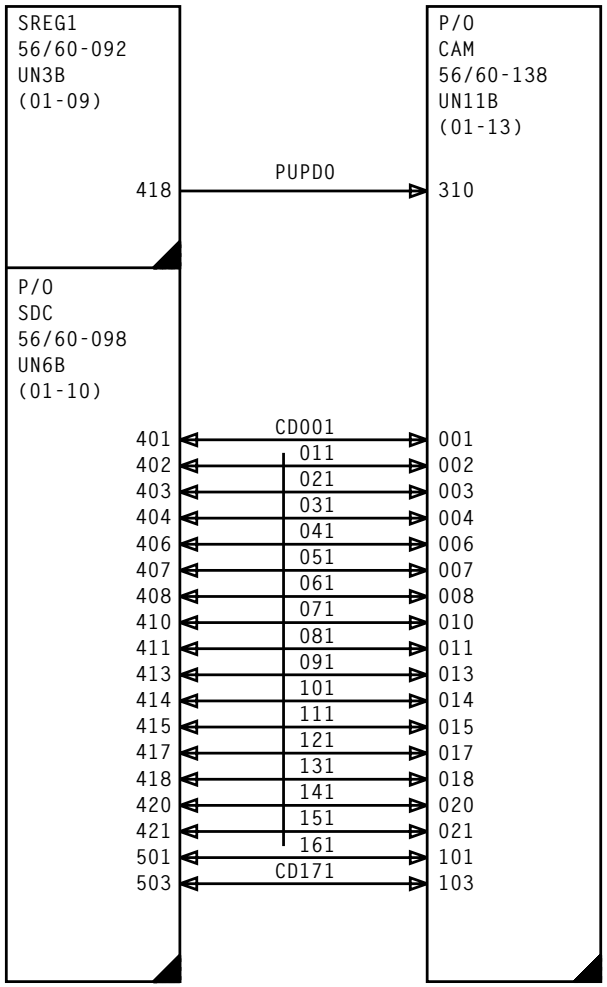
CONTROL UNIT (CU) – STORE ADDRESS TRANSLATOR (SAT)
PHASES 1-10 FAILURES

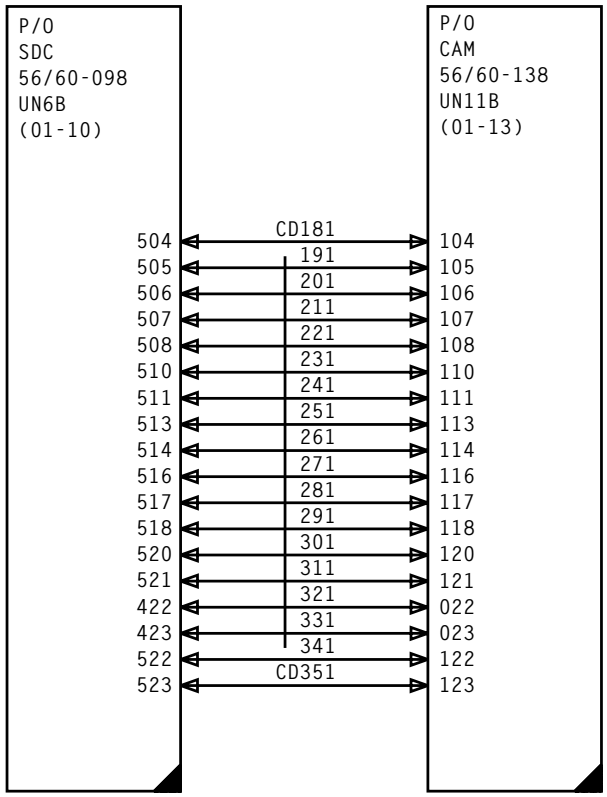


CONTROL UNIT (CU) — STORE ADDRESS TRANSLATOR (SAT)
PHASES 1-10 FAILURES

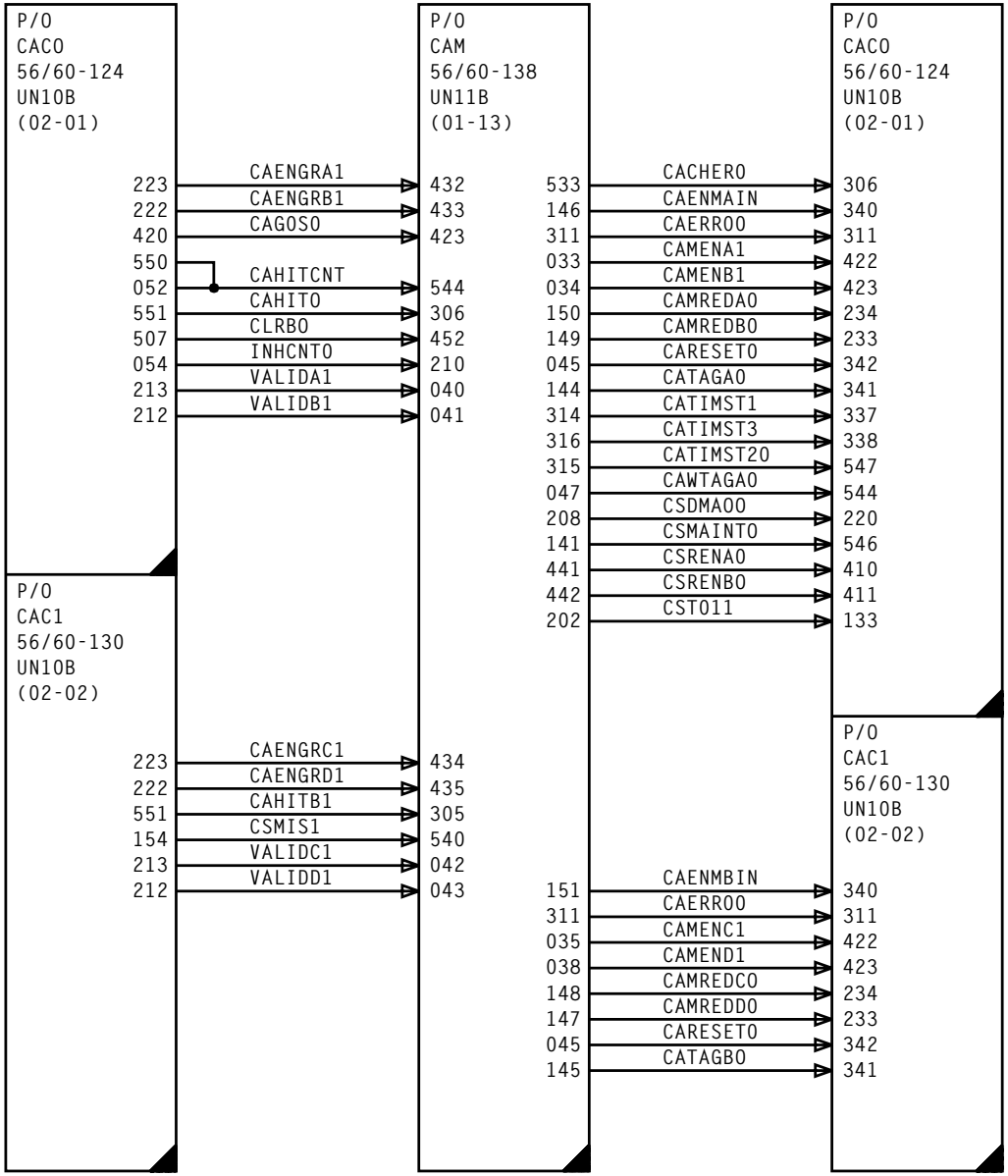


CONTROL UNIT (CU) — STORE ADDRESS TRANSLATOR (SAT) PHASES 1-10 FAILURES

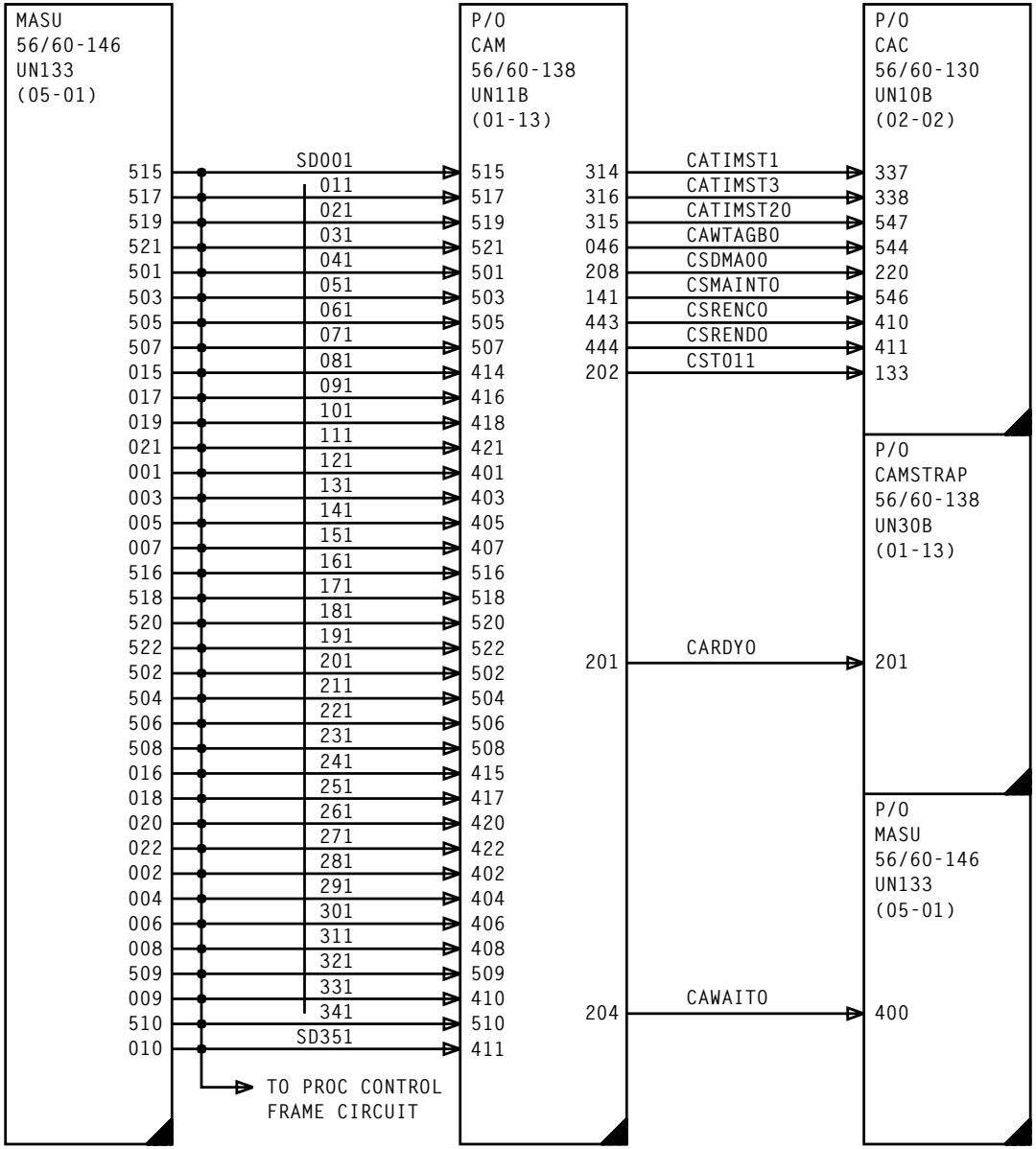




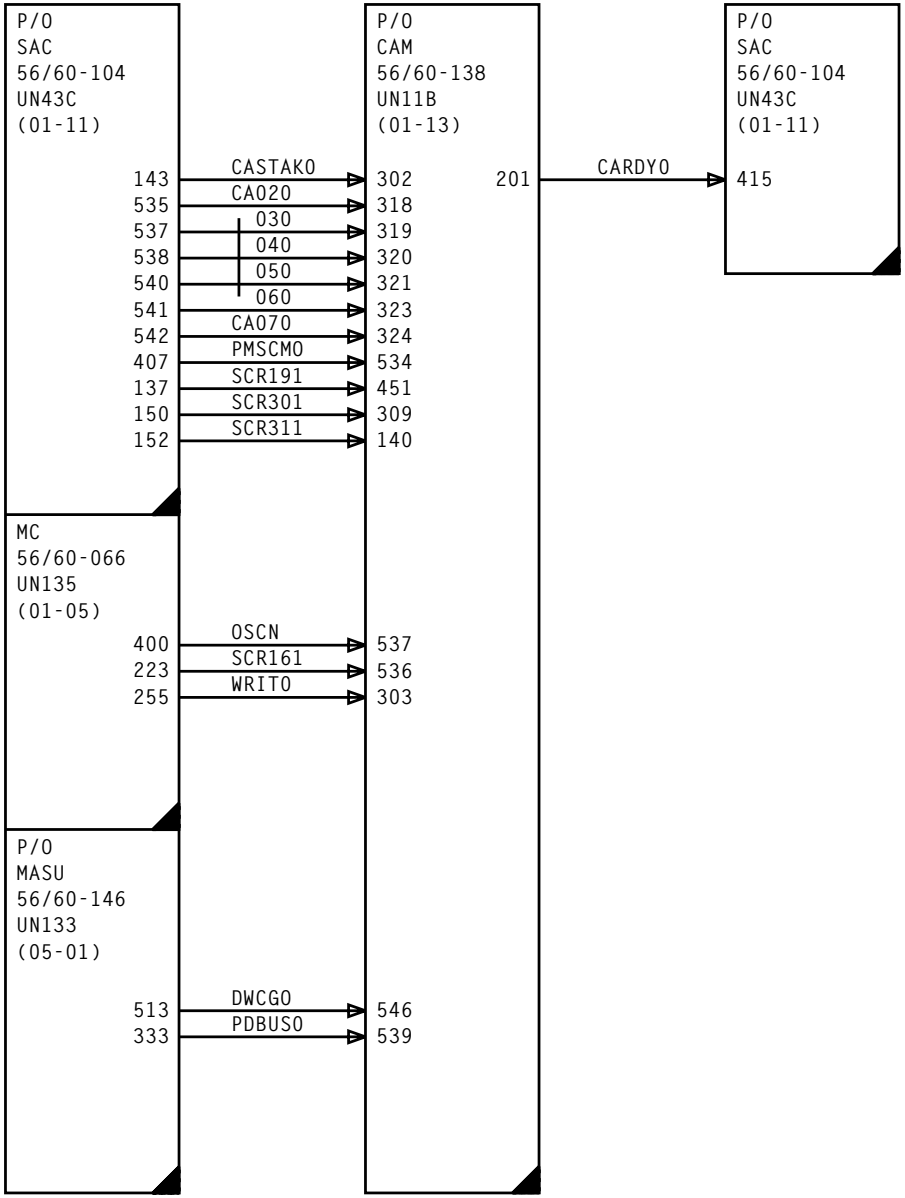
CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE MEMORY (CAM) FAILURES

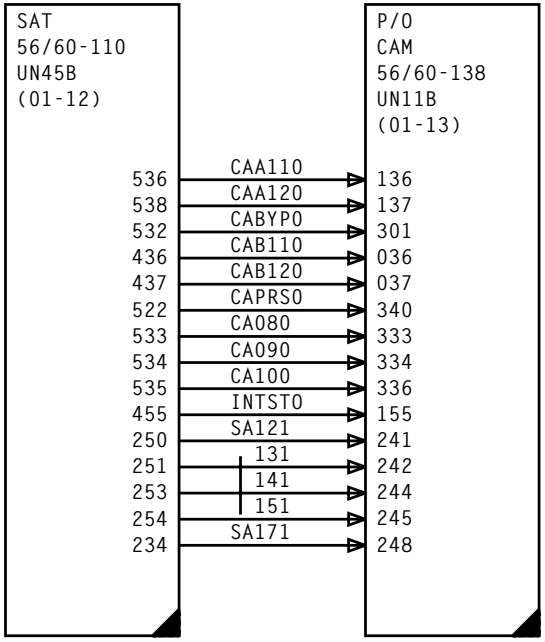


CONTROL UNIT (CU) — CACHE STORE UNIT (CSU) — CACHE MEMORY (CAM) FAILURES

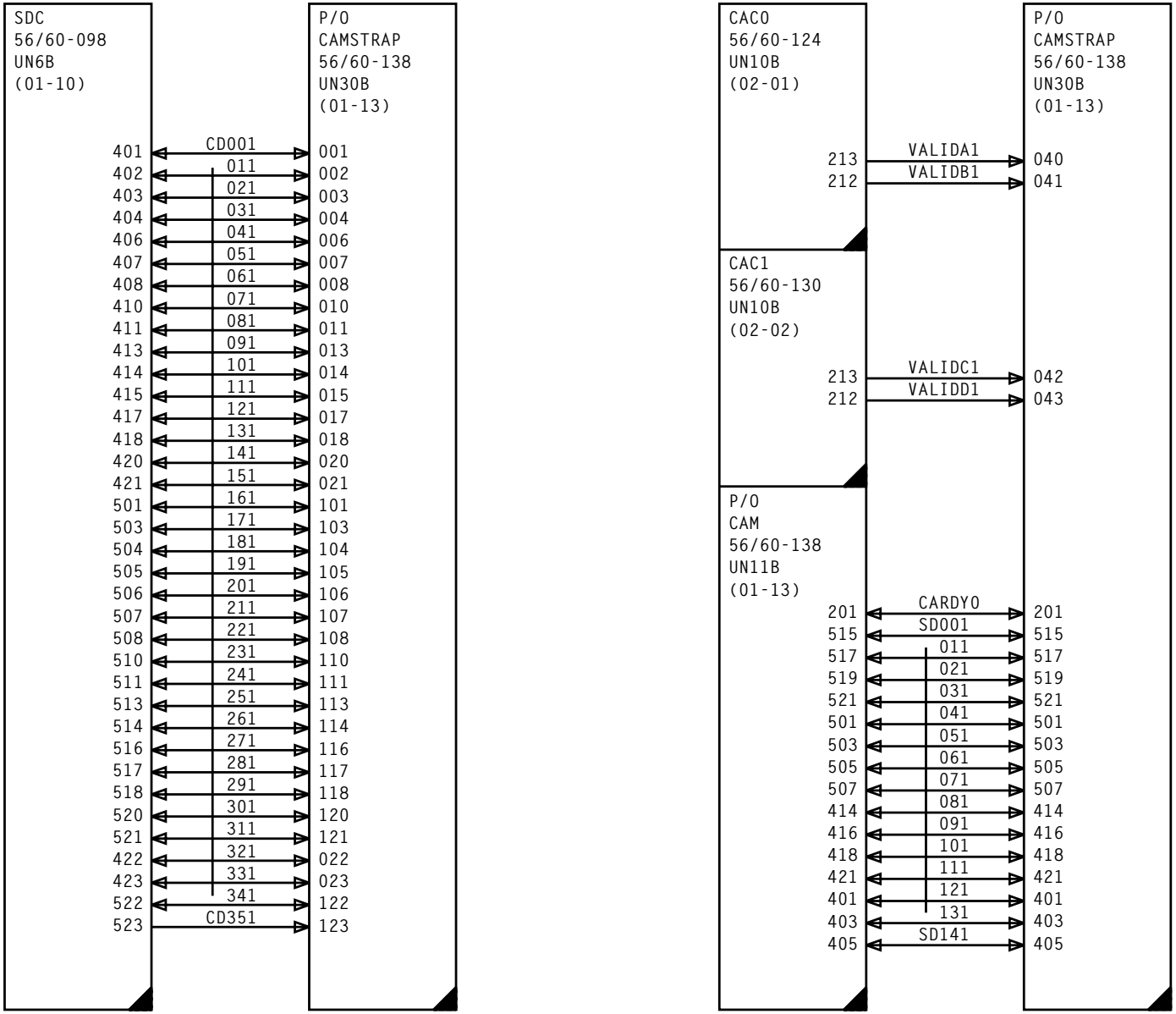


CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE MEMORY (CAM) FAILURES





CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE MEMORY (CAM) FAILURES



CONTROL UNIT (CU) — CACHE STORE UNIT (CSU) — CACHE MEMORY STRAPPING (CAMSTRAP) FAILURES

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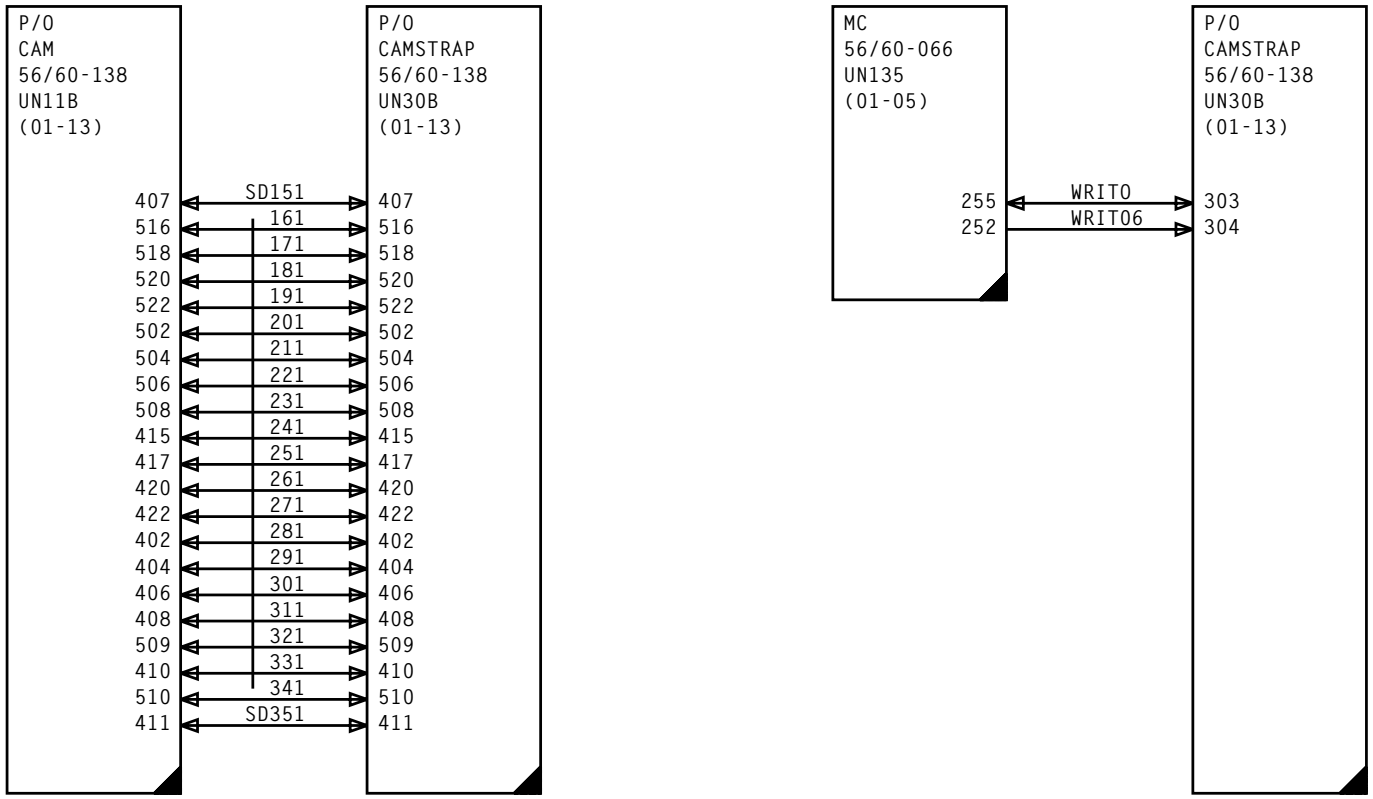
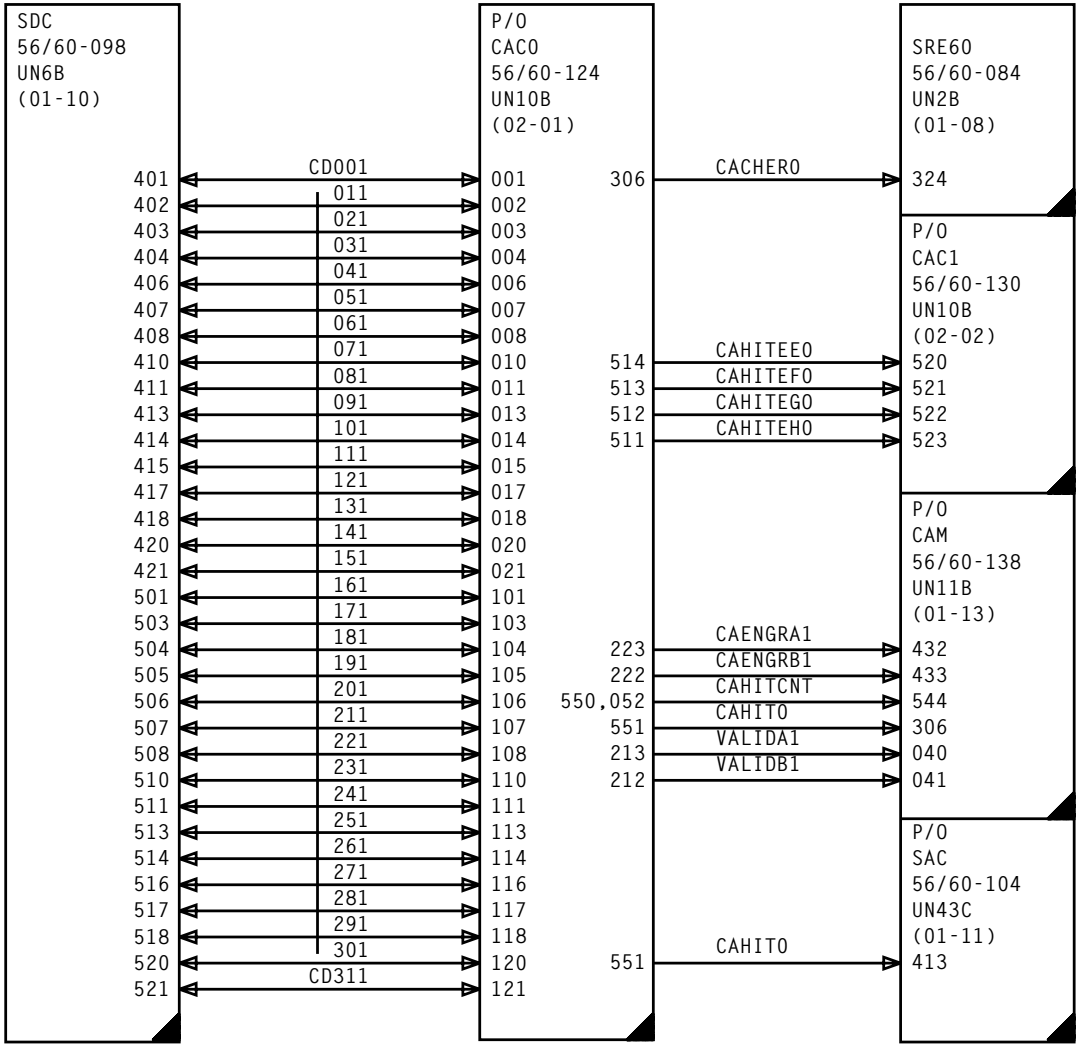
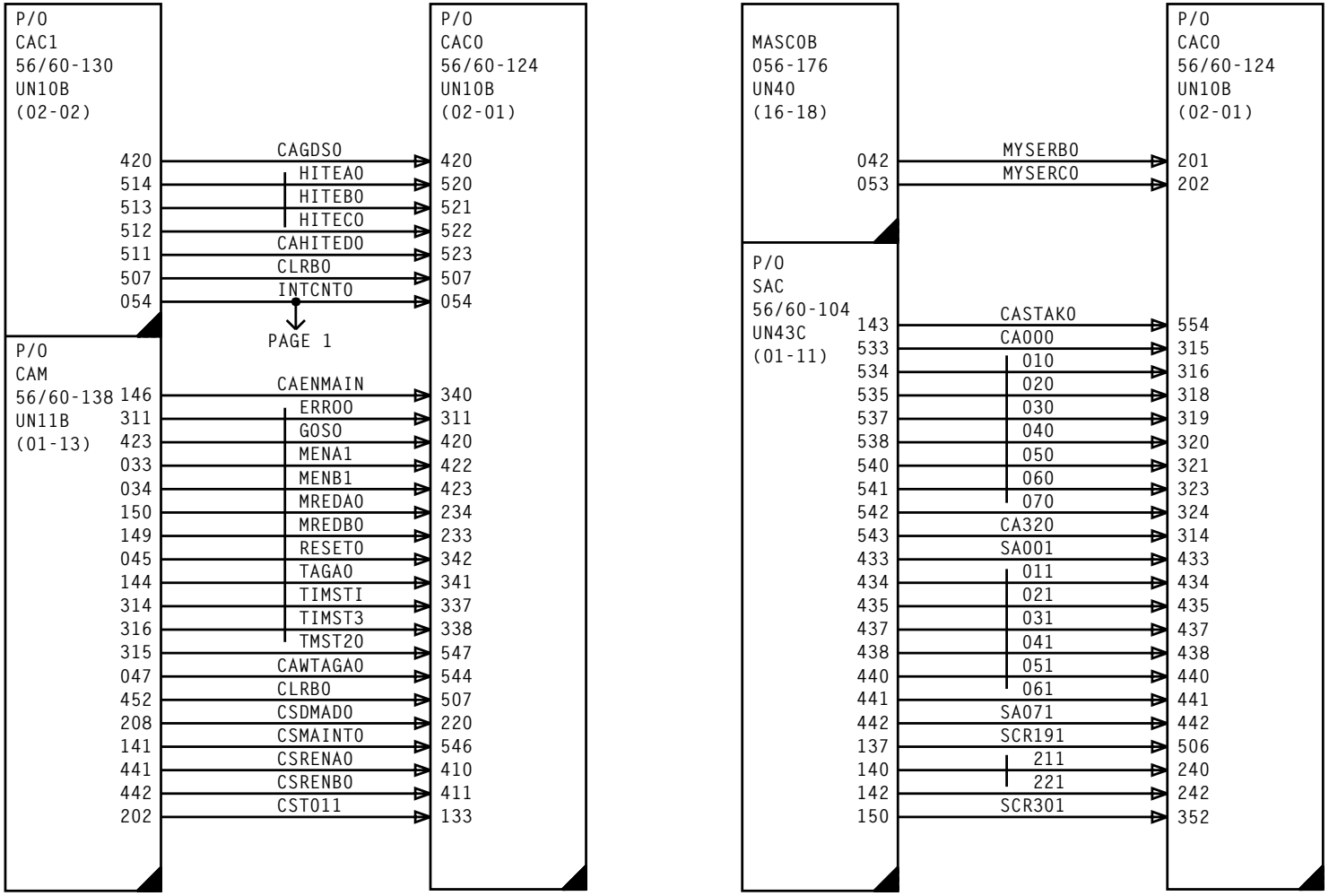


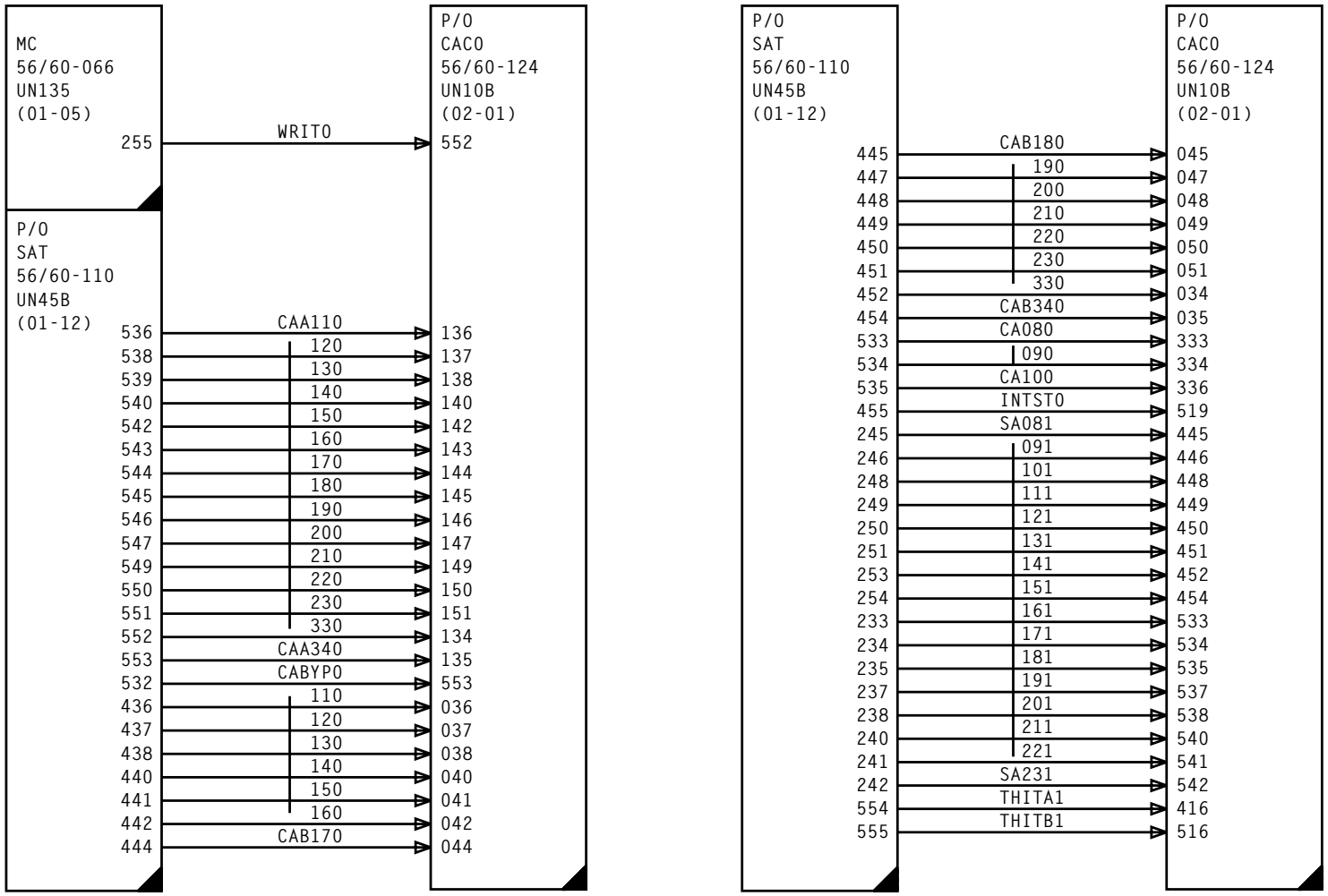
CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE MEMORY STRAPPING (CAMSTRAP) FAILURES



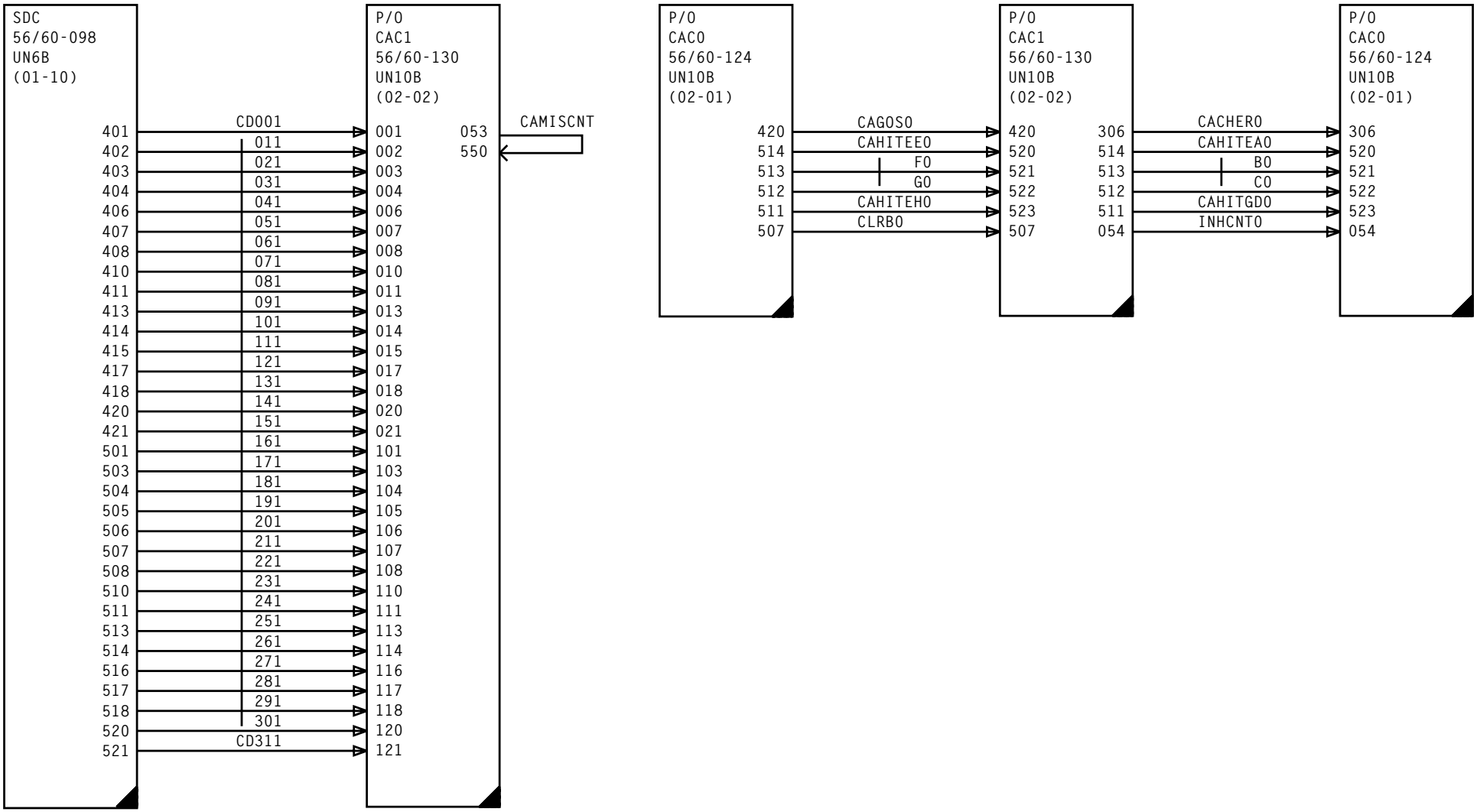
CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE CONTROL 0 (CAC0) FAILURES



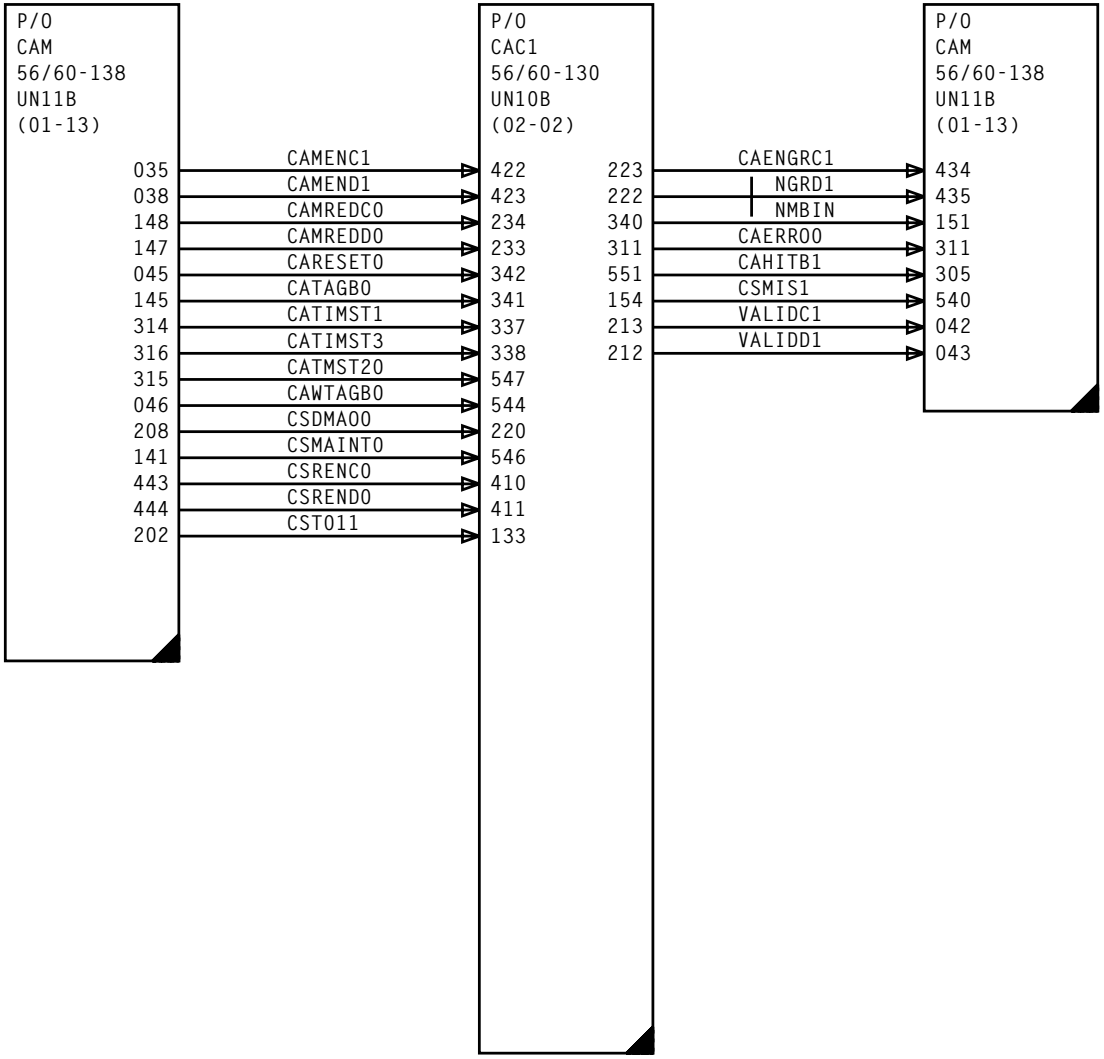
CONTROL UNIT (CU) — CACHE STORE UNIT (CSU) — CACHE CONTROL 0 (CAC0) FAILURES



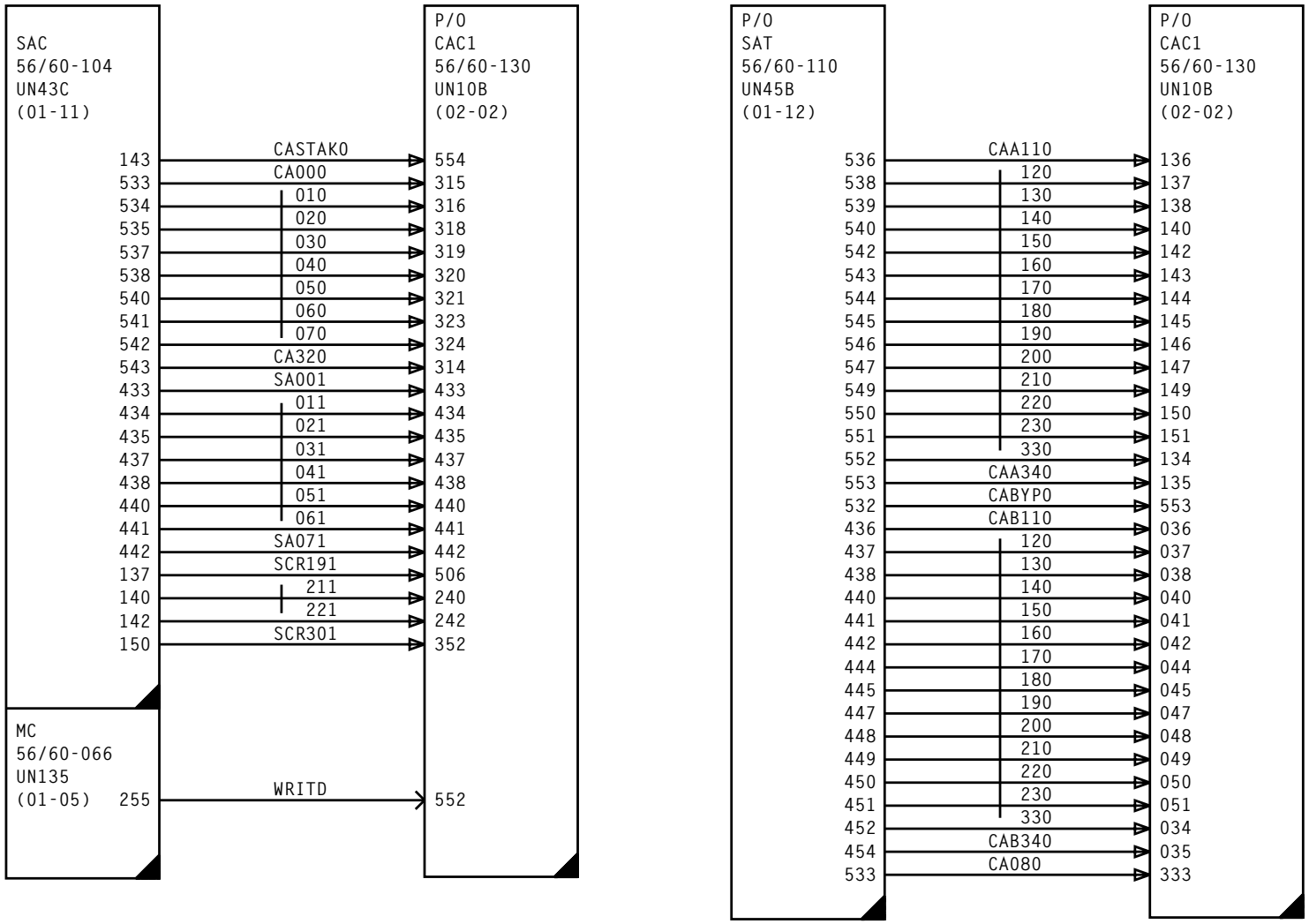
CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE CONTROL 0 (CAC0) FAILURES



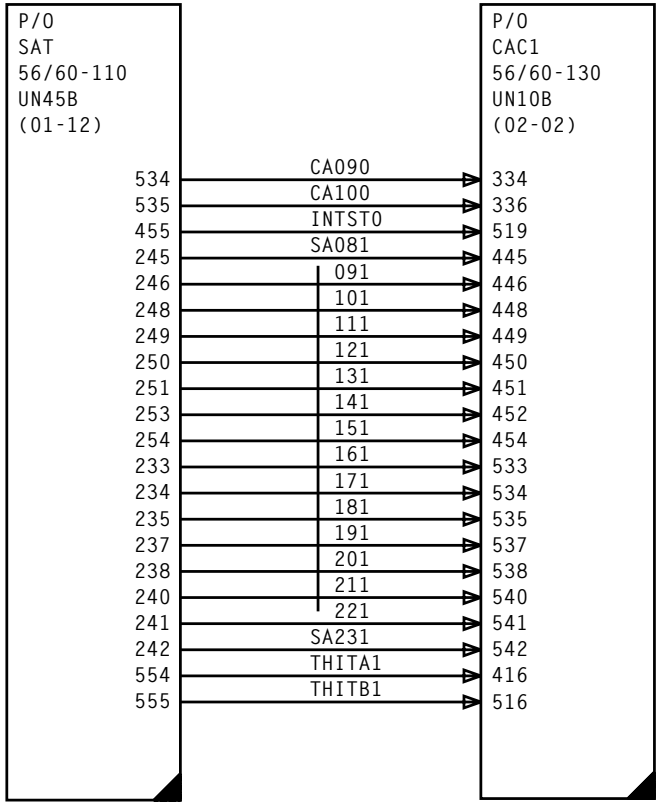
CONTROL UNIT (CU) — CACHE STORE UNIT (CSU) — CACHE CONTROL 1 (CAC1) FAILURES



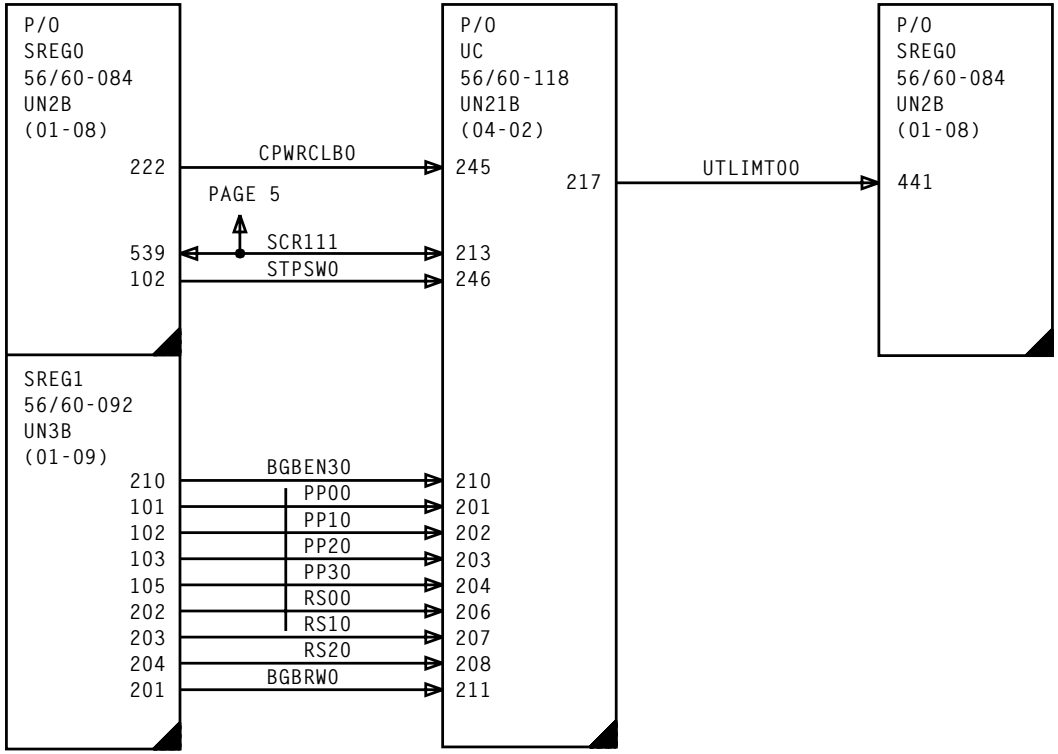
CONTROL UNIT (CU) — CACHE STORE UNIT (CSU) — CACHE CONTROL 1 (CAC1) FAILURES



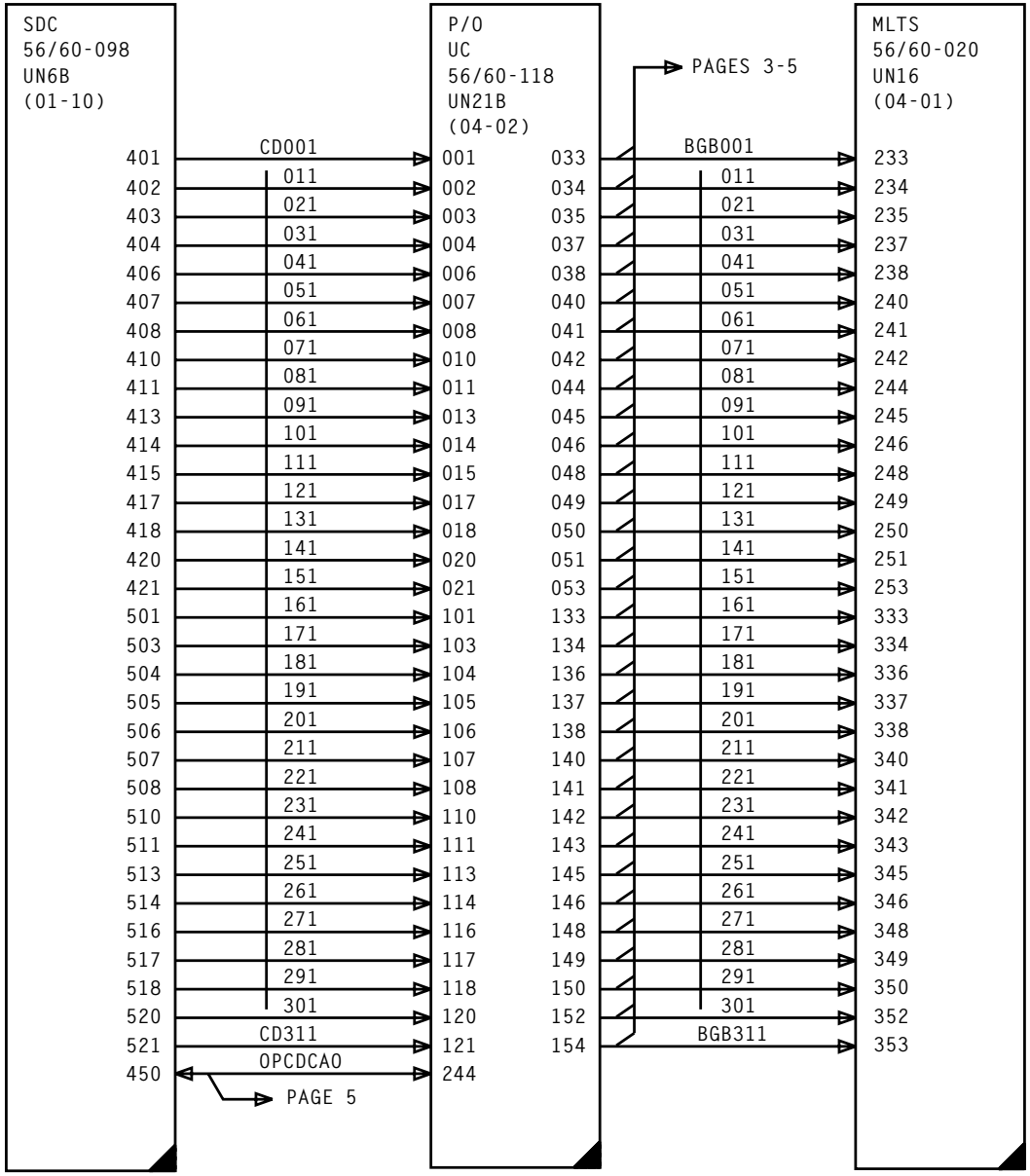
CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE CONTROL 1 (CAC1) FAILURES



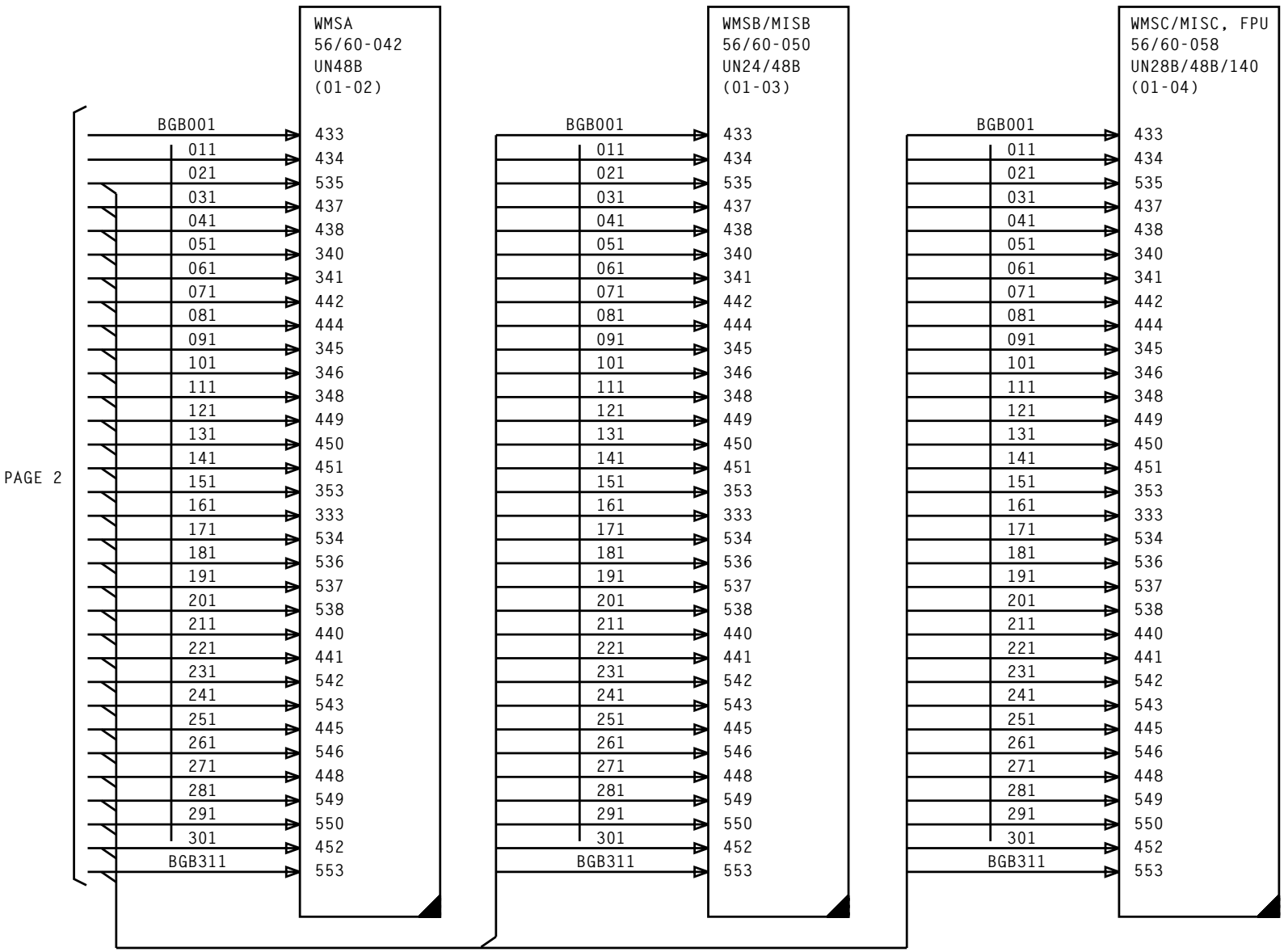
CONTROL UNIT (CU) – CACHE STORE UNIT (CSU) – CACHE CONTROL 1 (CAC1) FAILURES



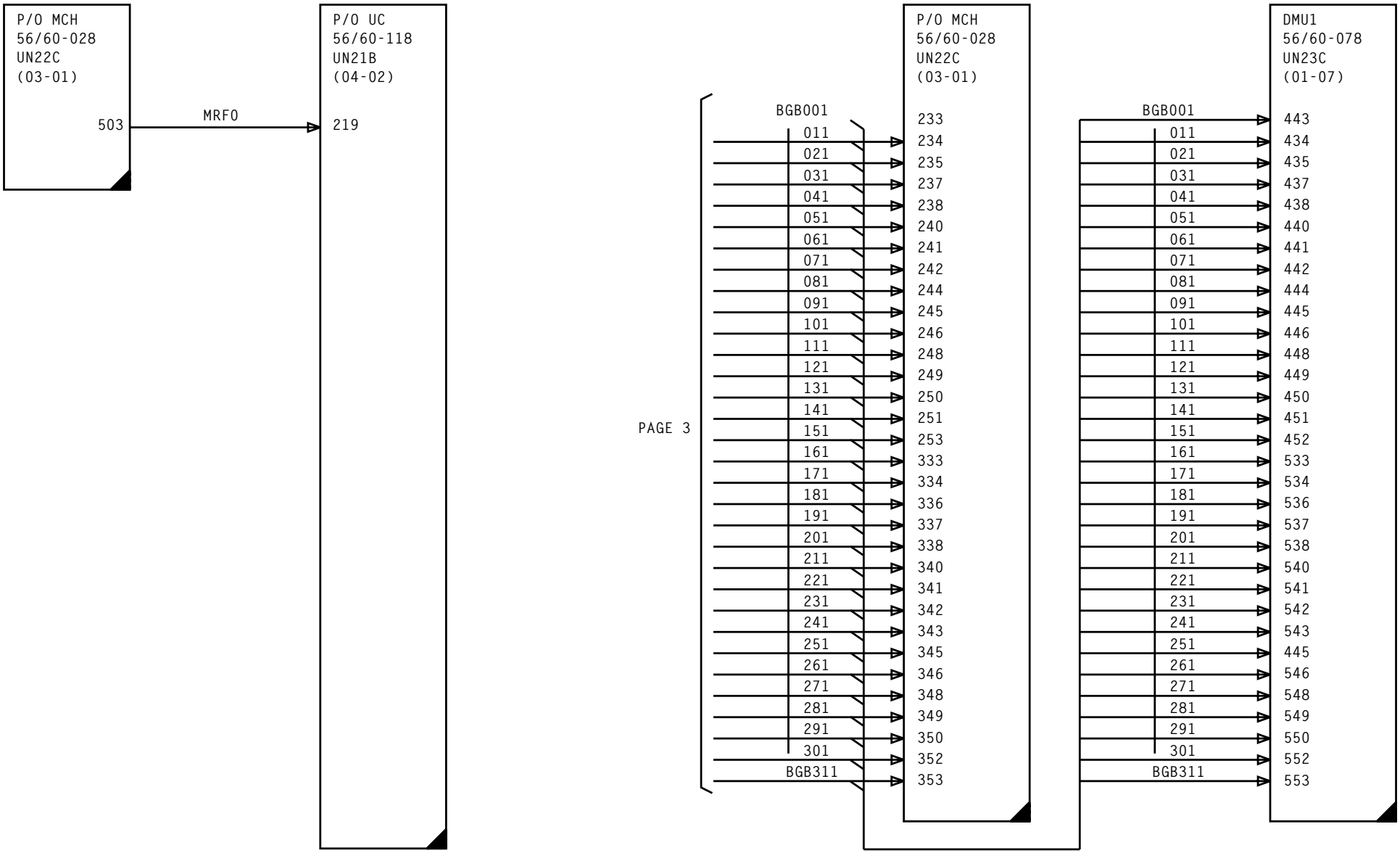
CONTROL UNIT (CU) – UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES



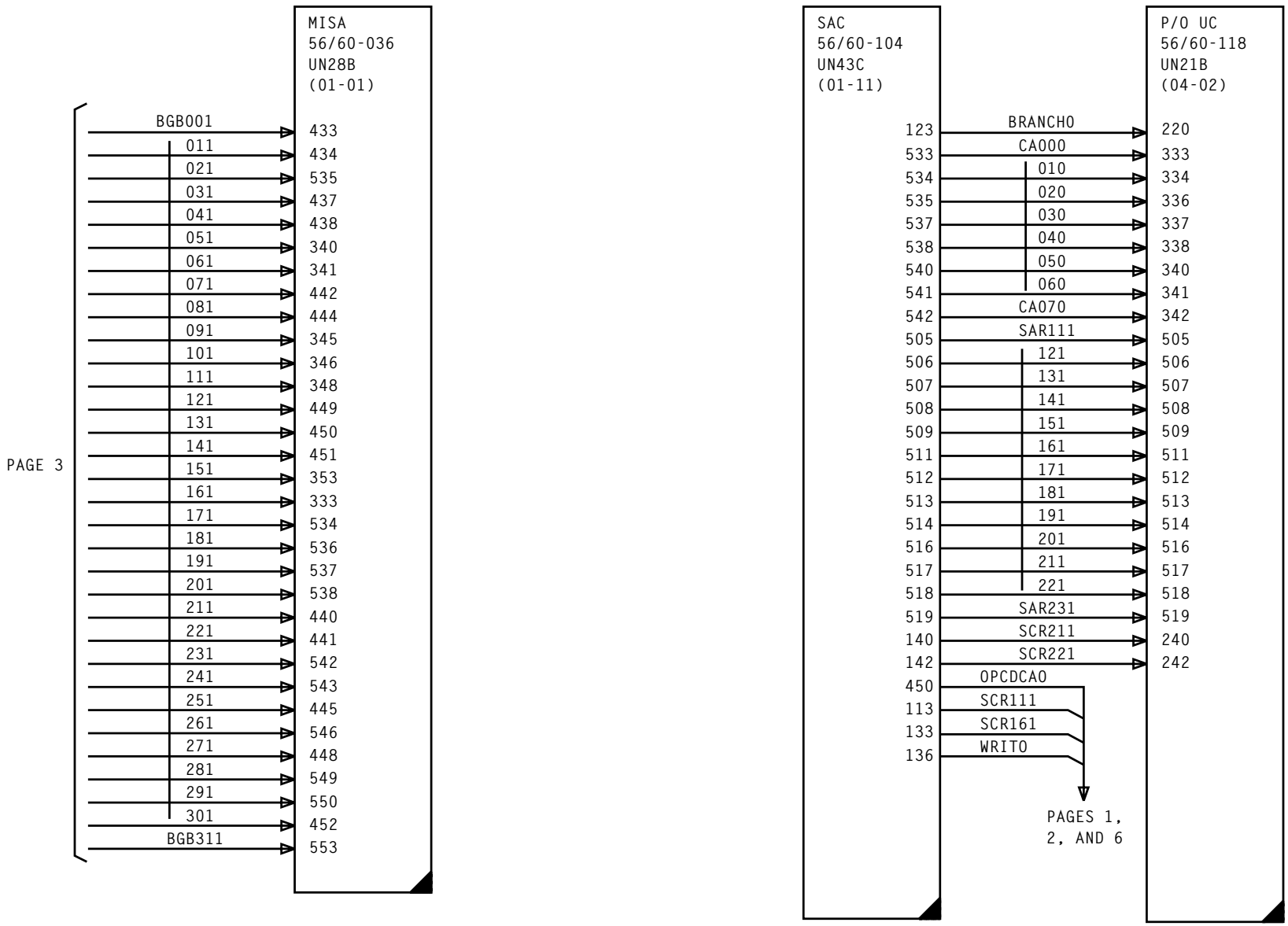
CONTROL UNIT (CU) – UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES



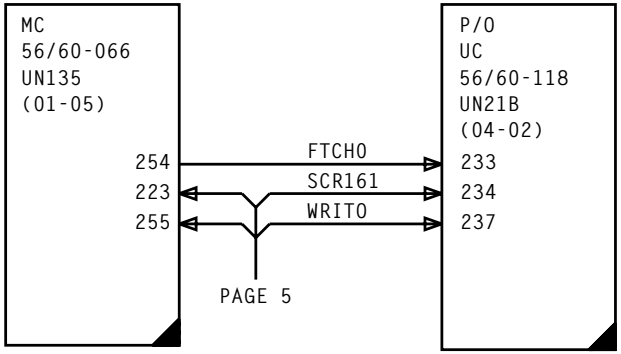
CONTROL UNIT (CU) — UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES

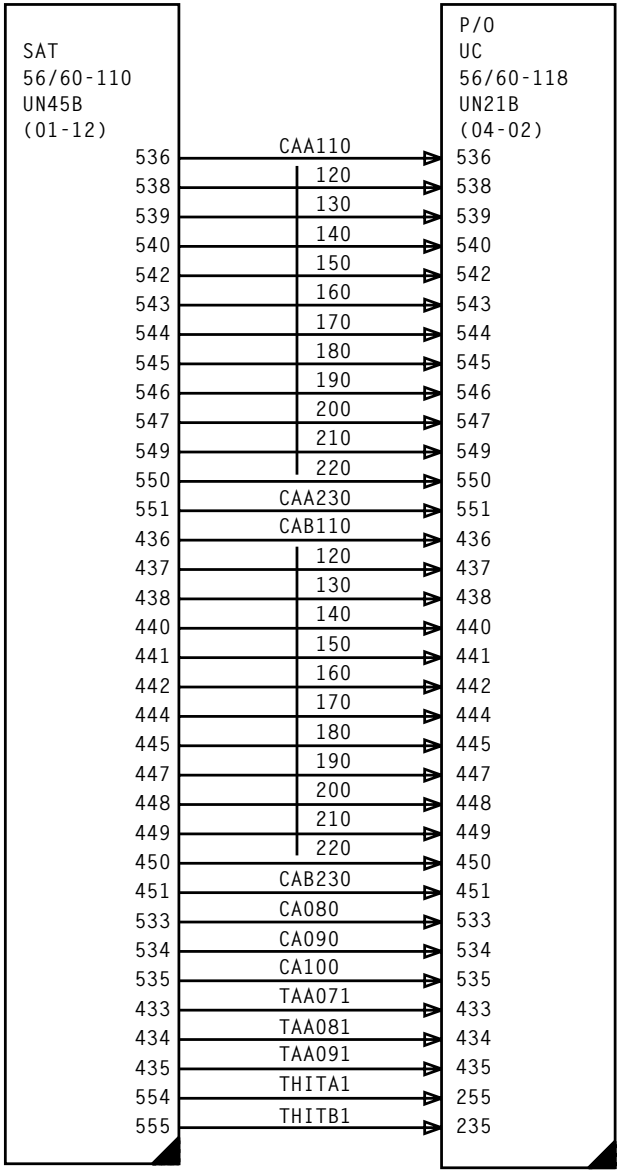


CONTROL UNIT (CU) – UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES



CONTROL UNIT (CU) – UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES





CONTROL UNIT (CU) – UTILITY CIRCUIT (UC) PHASES 1-18 AND 90-93 FAILURES

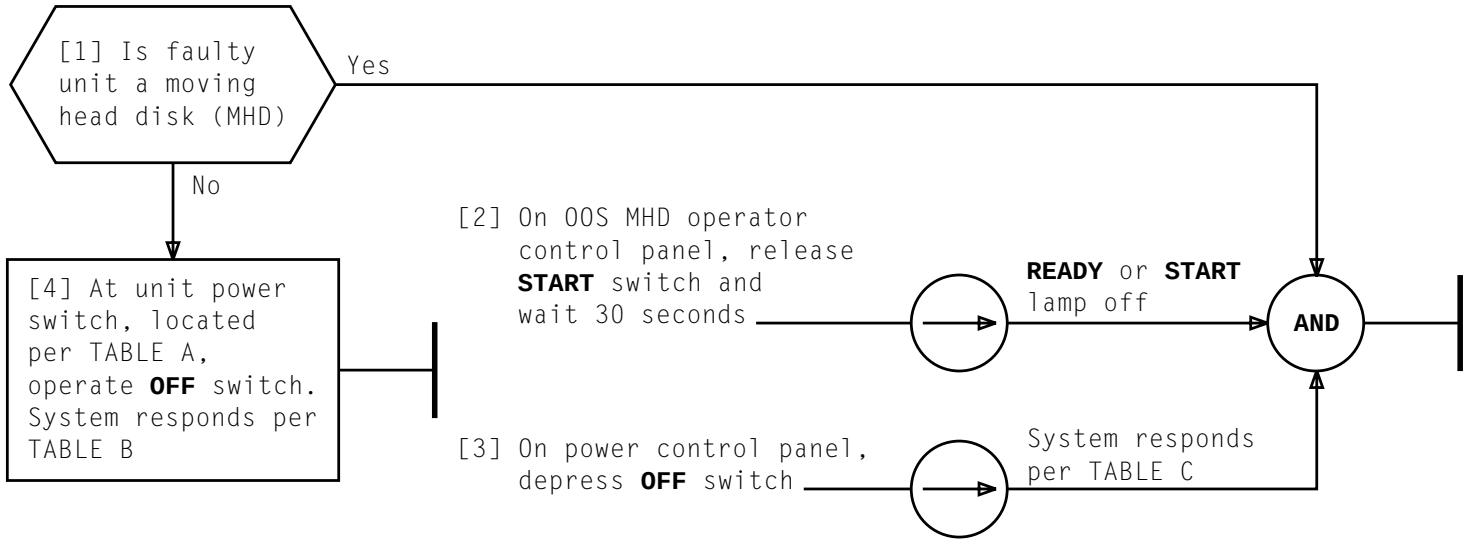


TABLE A

UNIT	POWER SWITCH	PC FRAME
CU 0	**TN5**	Bay 0
CU 1	**TN5**	Bay 1
DFC 0	**TN3**	Bay 0
DFC 1	**TN3**	Bay 1
IOP 0	**TN6**	Bay 0
IOP 1	**TN6**	Bay 1

Legend: CU = control unit
DFC = disk file controller
IOP = input/output processor
PC = processor control

TABLE B

ITEM	RESPONSE
1	Major audible alarm
2	REPT:PO/WER DO/WN message received
3	At terminal display page 102, unit label indicates UNAV or OOS
4	At unit power switch, OFF LED lighted

TABLE C

ITEM	RESPONSE
1	Minor audible alarm
2	Power control panel **OFF** and **ALERT** LEDs lighted
3	Aisle pilot lamp lighted
4	REPT:PO/WER DO/WN MHD*a* * message received

* a = 0, 1, 2, or 3

REMOVE POWER FROM UNIT

1. On terminal display page 102, type message indicated in TABLE A

   NOTE: All subunits removed from service before unit **RMV CO/MPLETED**message received

   Response: Minor audible alarm.
   RMV CO/MPLETEDmessage received.
   Unit label indicates OOS MAN.
   OOS LED lighted on unit power switch

End of procedure

TABLE A

UNIT	INPUT MESSAGE*
CU	RMV:CU a!
DFC	RMV:DFC a!
DUIC	RMV:DUIC a!
IOP	RMV:IO/Pa!
MHD	RMV:MHD a!
MTC	RMV:MTC a!
MTTYC	RMV:MTTYC a!
SCSDC	RMV:SCSDC a!
SDLC	RMV:SDLC a!
TTYC	RMV:TTYC a!

* a = unit member number

Legend:
CU = control unit
DFC = disk file controller
DUIC = direct user interface controller
IOP = input/output processor
MHD = moving head disk
MTC = magnetic tape controller
MTTYC = maintenance TTY controller
SCSDC = scanner and signal distributor controller
SDLC = synchronous data link controller
TTYC = TTY controller

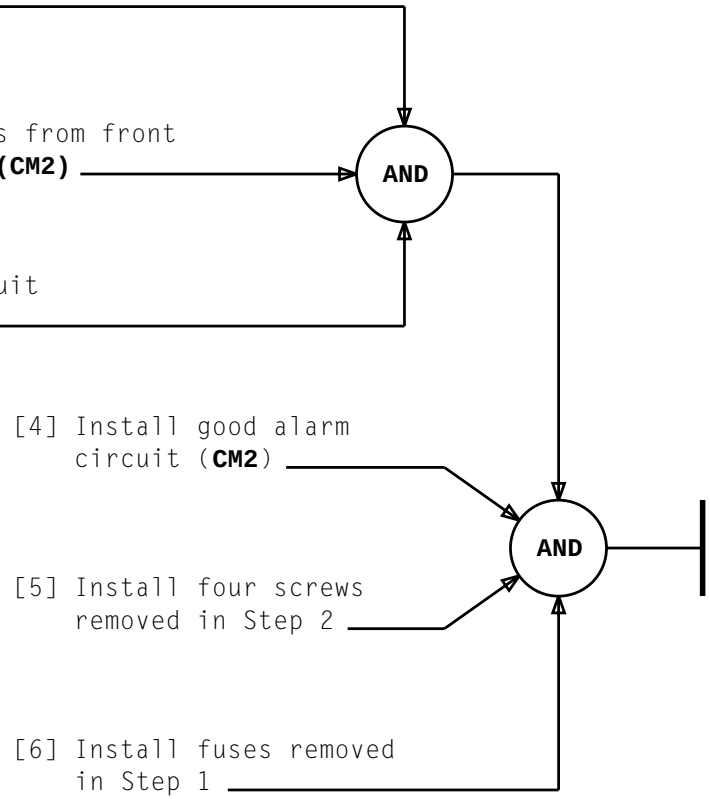
REMOVE UNIT FROM SERVICE VIA INPUT MESSAGE

At power distribution (PD) frame control panel:

[1] Remove fuses **INVOLT A, INVOLT B**, and **CHG CKT**

[2] Remove four screws from front of alarm circuit **(CM2)**

[3] Remove alarm circuit (**CM2**) CP



[4] Install good alarm circuit (**CM2**)

[5] Install four screws removed in Step 2

[6] Install fuses removed in Step 1

DANGER 1
—48V battery supply present inside frame

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REPLACE ALARM CIRCUIT CM2 CIRCUIT PACK (CP)

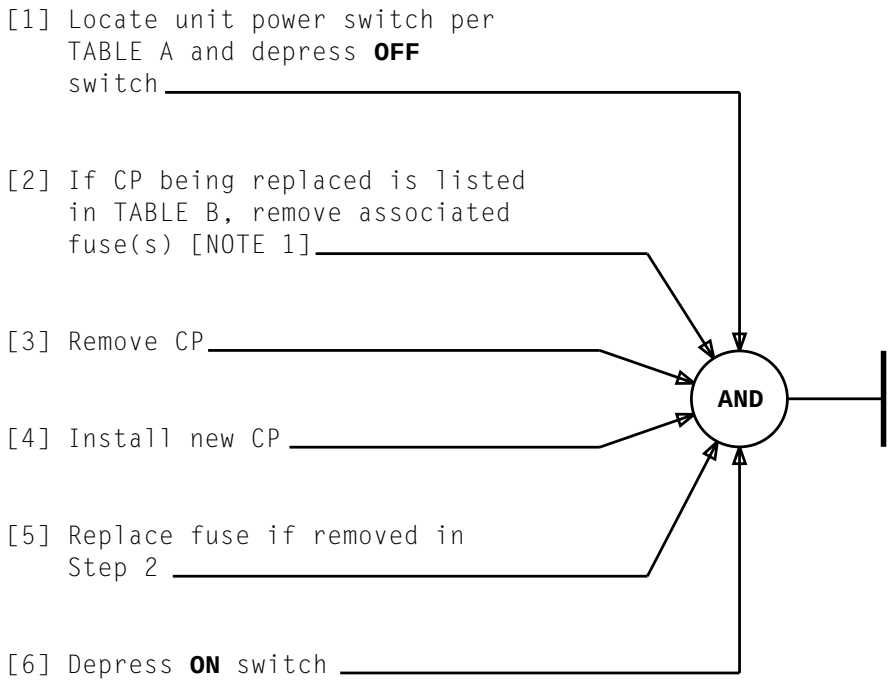


TABLE A

UNIT	POWER SWITCH	FRAME	LOCATION
CU 0	**TN 5**	PC bay 0	56-162
CU 1	**TN 5**	PC bay 1	56-162
DFC 0	**TN 3**	PC bay 0	47-074
DFC 1	**TN 3**	PC bay 1	47-074
IOP 0	**TN 6**	PC bay 0	29/38-162*
IOP 1	**TN 6**	PC bay 1	29/38-162*

* If optional main store and IOP growth unit is not installed, these units move up one level

TABLE B

CIRCUIT PACK	LOCATION	FUSE
DFC TN 3	47-074	**F5A**
Power unit C	47-016	**F6**
Power unit C	47-016	**F6A**
Power unit D	47-178	**F9**
Power unit D	47-178	**F9A**
CPU TN 5	56-162	**F10A**
Power unit B	56-178	**F11**
Power unit B	56-178	**F11A**
Power unit A	56-016	**F12**
Power unit A	56-016	**F12A**
Power unit G	29/38-016*	**F15**
Power unit G	29/38-016*	**F15A**
Power unit F	38-178	**F16**
Power unit F	38-178	**F16A**
PC 1 TN 9	29/38-032*	**F17**
PC 1 TN 9	29/38-032*	**F17A**
PC 2 TN 9	38-052	**F18**
PC 2 TN 9	38-052	**F18A**
PC 3 TN 9	38-022	**F19**
PC 3 TN 9	38-022	**F19A**
Power unit E	38-016	**F20**
Power unit E	38-016	**F20A**
PC 0 TN 9	29/38-072*	**F21**
PC 0 TN 9	29/38-072*	**F21A**
IOP TN 6	29/38-162*	**F22A**
Power unit H	29/38-178*	**F23**
Power unit H	29/38-178*	**F23A**
494GA power unit	29/38-024*	**F24**
495GA power unit	29/38-024*	**F24A**

* If optional main store and IOP growth unit is not installed, these units move up one level

NOTE 1
If CP is a power unit, indicator fuse must be removed before load fuse is removed and must be reinstalled after load fuse is reinstalled

REPLACE CIRCUIT PACK (CP)

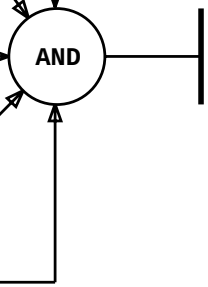
[1] If input/output processor (IOP) is not already removed from service, at terminal, type: RMV:IO/Pa! (a = member number of IOP)

[2] On **TN6**, at location 29/38-162, depress **OFF** switch

[3] Remove **UN33B** circuit pack from IOP and install replacement circuit pack

[4] On **TN6**, at location 29/38-162, depress **ON** switch

[5] Restore IOP to service. At terminal, type: RST:IO/Pa!



REPLACE SCANNER AND SIGNAL DISTRIBUTOR (SCSD) UN33B CIRCUIT PACK

1. At unit power switch located per TABLE A, operate **ON** switch

   Response: REPT:PO/WER UPmessage received. At terminal display page 102, unit label indicates OOS or OOS MAN. At unit power switch, **OOS** LED lighted

2. If unit is an MHD, at MHD operator control panel, depress **START** key

   Response: **START** or **READY** lamp lighted in 30 seconds

End of procedure

TABLE A

UNIT	POWER SWITCH	FRAME
CU 0	**TN5**	PC bay 0
CU 1	**TN5**	PC bay 1
DFC 0	**TN3**	PC bay 0
DFC 1	**TN3**	PC bay 1
IOP 0	**TN6**	PC bay 0
IOP 1	**TN6**	PC bay 1
MHD 0	ED-4C194	MHD 0
MHD 1	ED-4C194	MHD 1
MHD 2	ED-4C194	MHD 2
MHD 3	ED-4C194	MHD 3

Legend: CU = control unit
DFC = disk file controller
IOP = input/output processor
MHD = moving head disk
PC = processor control

RESTORE POWER TO UNIT

1. On terminal display page 102, type message indicated in TABLE A

   NOTE: All subunits except input/output processor subunits restored to service before RST:CO/MPLETEDmessage received

   Response: RST:CO/MPLETEDmessage received. Unit label indicates ACT (CU indicates STBY). **OOS** LED off at unit power switch

End of procedure

TABLE A

UNIT	INPUT MESSAGE*
CU	RST:CU a!
DFC	RST:DFC a!
DUIC	RST:DUIC a!
IOP	RST:IO/Pa!
MHD	RST:MHD a!
MTC	RST:MTC a!
MTTYC	RST:MTTYC a!
SCSDC	RST:SCSDC a!
SDLC	RST:SDLC a!
TTYC	RST:TTYC a!

*a = faulty unit member number

Legend:
CU = control unit
DFC = disk file controller
DUIC = direct user interface controller
IOP = input/output processor
MHD = moving head disk
MTC = magnetic tape controller
MTTYC = maintenance TTY controller
SCSDC = scanner and signal distributor controller
SDLC = synchronous data link controller
TTYC = TTY controller

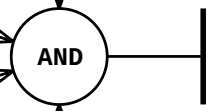
RESTORE UNIT TO SERVICE VIA INPUT MESSAGE

[1] On power distribution frame, insert charge probe firmly into indicator fuse position and hold

[2] See CAUTION 1. On power distribution frame control panel, depress and hold **CAP CHG SW** switch closed until **CAP CHG** LED goes off, then release

[3] Install good fuse in load fuse position

[4] Remove charge probe and install good fuse in indicator fuse position



CAUTION 1
Step 3 must be performed within 12 seconds after completion of Step 2; otherwise, fuse operation will occur when fuse is inserted in filter fuse position

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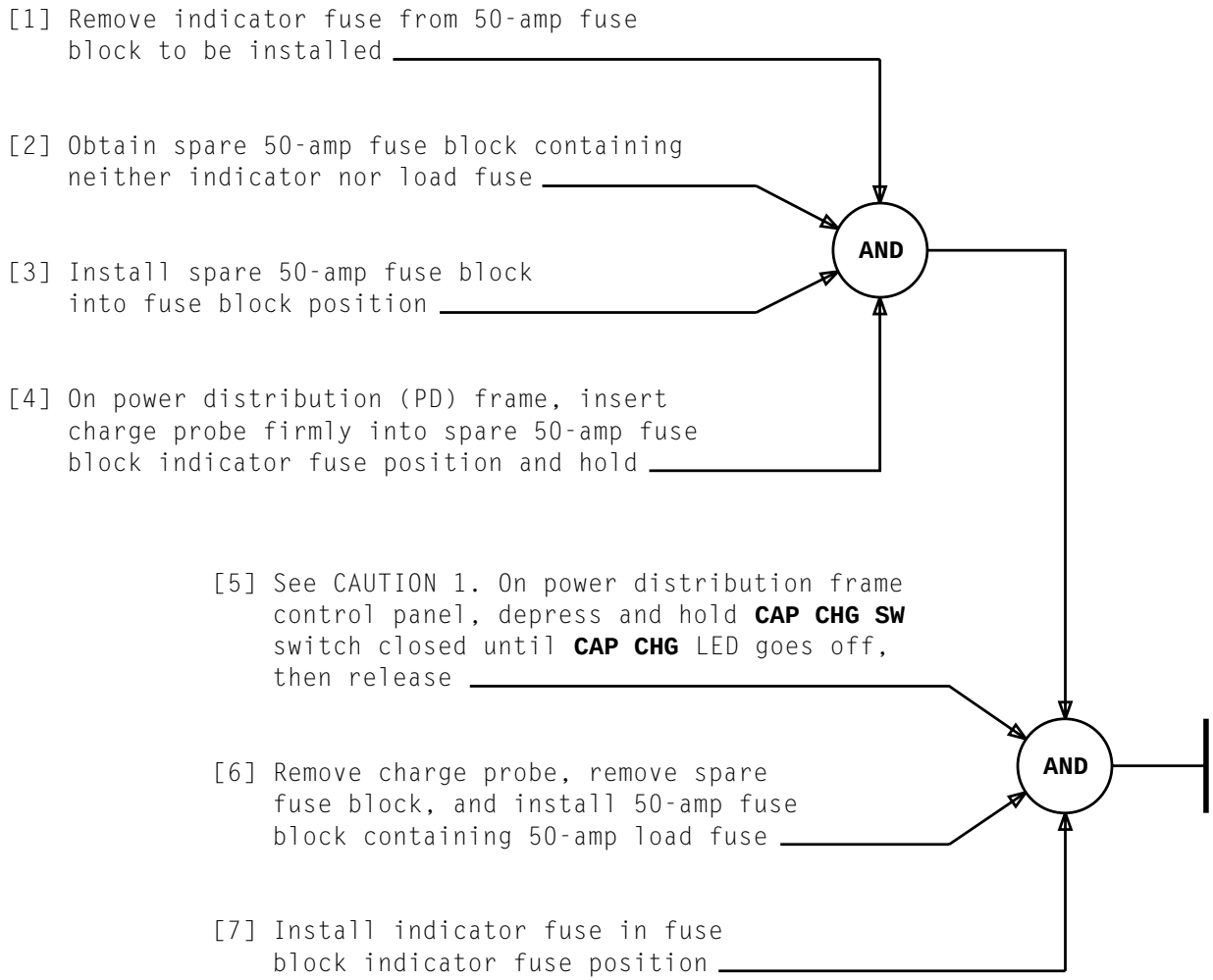
CHARGE FILTER-FUSE PANEL LOAD DISTRIBUTION FUSE CIRCUIT



CAUTION 1

Step 6 must be performed within 12 seconds after completion of Step 5; otherwise, fuse operation will occur when fuse block containing load fuse is installed

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CHARGE 40-60 AMP HIGH-CURRENT FUSE PANEL CIRCUIT

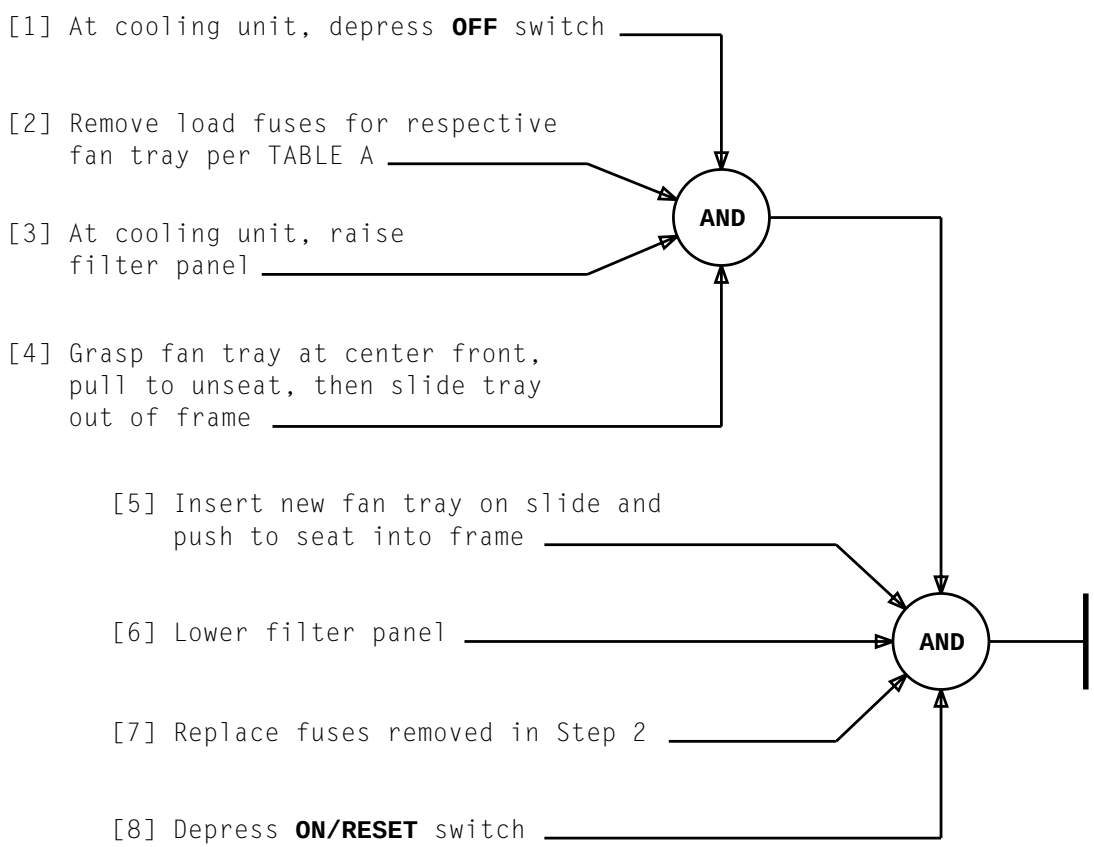

TABLE A	
COOLING UNIT	**LOAD FUSES**
Left fan tray	**F4A** **F3A**
Right fan tray	**F2A** **F1A**

REPLACE FAN TRAY

1. Type command code indicated in TABLE A at terminal display page 102 line 4

   NOTE: Any subunits are removed from service before unit **RMV CO/MPLETED**message received

   Response: Minor audible alarm.
   RMV CO/MPLETEDmessage received.
   Unit label indicates OOS.
   At unit power switch, **OOS** LED lighted

End of procedure

TABLE A

UNIT	COMMAND CODE
CU 0	300
CU 1	301
DFC 0	310
DFC 1	311
MHD 0	320
MHD 1	321
IOP 0	330
IOP 1	331

Legend: CU = control unit
DFC = disk file controller
IOP = input/output processor
MHD = moving head disk

REMOVE UNIT FROM SERVICE VIA COMMAND CODE

1. Type command code indicated in TABLE A at terminal display page 102 line 4

   NOTE: All subunits restored to service before unit RST CO/MPLETEDmessage received

   Response: RST CO/MPLETEDmessage received.
   Unit label indicates ACT (CU indicates STBY).
   At unit power switch, **OOS** LED off

End of procedure

TABLE A

UNIT	COMMAND CODE
CU 0	200
CU 1	201
DFC 0	210
DFC 1	211
MHD 0	220
MHD 1	221
IOP 0	230
IOP 1	231

Legend: CU = control unit
DFC = disk file controller
IOP = input/output processor
MHD = moving head disk

RESTORE UNIT TO SERVICE VIA COMMAND CODE

ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE
TPG-000		TAP-133		DLP-502							
IXL-001		TAP-134		DLP-503							
TAD-100		TAP-135		DLP-504							
TAP-101		TAP-136		DLP-505							
TAP-102		TAP-137		DLP-506							
TAP-103		TAP-138		DLP-507							
TAP-104		TAP-139		DLP-508							
TAP-105		TAP-140		DLP-509							
TAP-106		TAP-141		DLP-510							
TAP-107		TAP-142		DLP-511							
TAP-108		TAP-143		CKL-891							
TAD-109		TAP-144		TNG-893							
TAD-110		TAP-145		DPL-895							
TAD-111		TAP-146									
TAD-112		TAD-147									
TAD-113		TAD-148									
TAD-114		TAD-149									
TAD-115		TAD-150									
TAD-116		TAD-151									
TAD-117		TAD-152									
TAD-118		TAD-153									
TAD-119		TAD-154									
TAP-120		TAD-155									
ISD-121		TAD-156									
TAP-122		TAD-157									
TAP-123		TAD-158									
TAP-124		TAD-159									
TAP-125		TAD-160									
TAP-126		TAD-161									
TAP-127		TAD-162									
TAP-128		TAD-163									
TAP-129		TAD-164									
TAP-130		TAD-165									
TAP-131		DLP-500									
TAP-132		DLP-501									