

SPECIAL-PURPOSE REGISTER BIT ASSIGNMENTS

1. SYSTEM STATUS REGISTER (SS)

BIT	DESIGNATION	FUNCTION
0	Address Match Enable (AME)	Enables the match between store address register (SAR) and the address input register.
1	Block Hardware Check (BHC)	Disables the output of the error register (bits 0 through 13).
2	Block Interrupt (BIN)	Disables all interrupts.
3	Block Timer Check (BTC)	Blocks the input and output from the program timer.
4	Data Match Enable (DME)	Enables the match between store data register (SDR) and the data input register.
5	Halt (HLT)	Drives the control panel lamp which indicates the 3A CC is in a program halt condition.
6	Initialization Sanity Check 1 (ISC1)	Checks sanity of hardware initialization routine. If a failure is detected, a switch to the other 3A CC will occur.
7	Initialization Sanity Check 2 (ISC2)	Checks sanity of hardware initialization routine. If a failure is detected, the main memory will be reloaded.
8	Lock Off-Line (LOF)	Disables the I/O channels to prevent interference with on-line 3A CC.
9	Lock On-Line (LON)	Forces all hardware switch messages to initialize this 3A CC and keep it on-line.
10	Manual (MAN)	Drives the manual lamp on the control panel which indicates 3A CC (off-line) is in manual mode.
11	Microinterpret Mode (MINT)	Blocks the gating from the microstore into micro-instruction register (MIR). Enables the gating from main memory into the MIR.
12	Control (CC)	Indicates whether this 3A CC is on-line (CC=1) or off-line (CC=0) and controls various functions which protect on-line 3A CC from the off-line 3A CC.
13	Reject (REJ)	Drives the control panel lamp which indicates that a panel operation was not performed.

NOTICE

Not for use or disclosure outside the
Bell System except under written agreement

1. SYSTEM STATUS REGISTER (SS) (Contd)

BIT	DESIGNATION	FUNCTION
14	Stop (STP)	Jams the MAR to a maintenance address causing all zeros to be read out of microstore.
15	Disable I/O (DISIO)	
16	Privileged Function (PRF) (not used)	
17	Display (DISP)	Disables the gating from the PA to the display buffer on all transfers.
18	Block Bus Parity Check (BPC)	Disables the data bus parity checker.
19	ISC3BT	
20	Central Control 0 (CC 0)	Always 1 in 3A CC 0 so that program knows which 3A CC it is running in.
21	CC 1	Always 1 in 3A CC 1 so that program knows which 3A CC it is running in.

Note: The out-of-service (OS) bit is a status bit stored in memory. It indicates that some abnormal condition is present and that this 3A CC should not be put on-line.

The store-out-of-sync (SOS) bit is a status bit stored in memory. It indicates that the on-line and off-line stores are not in sync.

Both bits are set and reset by software.

2. ERROR REGISTER (ER)

BIT	DESIGNATION	CAUSES	IF
0	To decoder error	3A CC switch	Any bit 0-9=1 AND block hardware check (BHC) = 0 AND lock on-line (LON) = 0 then set stop bit and switch ----- If BHC = 0 AND LON = 1 initialize
1	From decoder error		
2	Instruction buffer (IB) X, Y field error		
3	Bus parity error		
4	Data manipulation logic (DML) mismatch		
5	MAR parity error		
6	Clock error		
7	Miscellaneous decoder error		
8	MAR - return address register (RAR) mismatch		
9	Function register parity error		
10	My store write protect	Initialization	Any bit 10-13=1 AND BHC=0
11	My store error		
12	My store fast time-out		
13	Branch allowed error		
14	Other store write protect	Interrupt	Any bit 14-21=1 [Also a bit in interrupt set register (IS) is set]
15	Other store error		
16	Other store fast time-out		
17	I/O multiple channel select		
18	Program timer reset received by on-line 3A CC		
19	Switch received by on-line 3A CC		
20	I/O channel error		
21	I/O bad parity received		

3. MICROCONTROL STATUS REGISTER (MCS)

BIT	DESIGNATION	CC	FUNCTION	INPUT SOURCE	ERROR DETECTION FACILITIES
0	Condition Flip-Flop (CF)	0	Indicates a branch condition for the microprogram control.	Set and cleared by miscellaneous decoder and may be gated to/from other control bits.	S-A-0 and S-A-1 will result in bad parity on MAR and will be detected.
1	CF	1			
2	Data Manipulation Logic Status (DS)	0	Used as a branch condition for the microprogram control.	Set and cleared according to results of certain data manipulation logic operations and by I/O channel status in some cases.	S-A-0 and S-A-1 will result in bad parity on MAR and will be detected.
3	DS	1			
4	Test Register 1 (TR1)	0	Used as a branch condition for the microprogram control.	Set and cleared by miscellaneous decoder and by I/O channel status in some cases.	S-A-0 and S-A-1 will result in bad parity on MAR and will be detected.
5	TR1	1			
6	Test Register 2 (TR2)	0	Used as a branch condition for the microprogram control.	Set and cleared by miscellaneous decoder and by I/O channel status in some cases.	S-A-0 and S-A-1 will result in bad parity on MAR and will be detected.
7	TR2	1			
8	Data Ready (DR)	0	Indicates the last main memory operation has been completed.	Set by a combination or one of the store completion signals from main memory. Cleared by any signal which initiates a main memory operation.	Failure detected by MAR RAR mismatch.
9	DR	1			
10	Return Address Register Update (RU)	0	Controls function of RAR. When RU=1, then RAR is used as a duplicate of MAR to check gating of MIR and microprogram store to the MAR. When RU=0, the RAR is used to save a return address from a microsubroutine.	Set by the same control signal that gates out of the RAR. Cleared by miscellaneous decoder.	S-A-0 will be detected when the crosspoint which clears the RU bit is activated. S-A-1 will cause either a decoder failure or a branch to error routine which will cause a switch of 3A CCs (duplex operation).
11	RU	1			

3. MICROCONTROL STATUS REGISTER (MCS) (Contd)

BIT	DESIGNATION	CC	FUNCTION	INPUT SOURCE	ERROR DETECTION FACILITIES
12	IFF	0			
13	IFF	1			
14	OPF	0			
15	OFF	1			
16	Microaddress Register Parity (MARP)	0	This bit is used in the checking of the address accessed in the microstore from MAR.	Set and cleared according to parity of contents in MAR.	S-A-0 and S-A-1 will result in bad parity checks of MAR.
17	MARP				
18	ERU	0			
19	ERU	1			
P _L	Set to 1				
P _H	Set to 1				

4. INTERRUPT STATUS

4.01 The interrupt facility consists of an interrupt set register (IS) and an interrupt mask (IM) register. The IS buffers the input signal that requests the interrupt until the 3A CC is able to transfer its control and recognize the interrupt. The IM is used to mask out interrupts such as stuck interrupts or interrupts of a lower priority.

4.02 The interrupt facility allows interrupts to occur at 16 different levels. Each of these levels can be individually masked by the 16 bits of the IM register. However, only nine of the 16 levels are defined and shown in the table according to bit location in the IS register. The highest level or priority of interrupt is the utility interrupt (bit 1 set); the lowest is a manual panel execute (bit 13 set). If the corresponding bit is set, the interrupt is present or, if the corresponding bit is clear, the interrupt is not present. If the corresponding bit is also set in the IM register, the interrupt will not be allowed to occur (blocked). If the corresponding bit is clear in the IM register, the interrupt will be allowed to occur (not blocked).

BIT	FUNCTION
0	
1	Utility interrupt (external)
2	
3	Address or data match
4	
5	Error register (interrupt class)
6	
7	OCC
8	TC 5
9	TC 10
10	TTY and tape-even (external)
11	TTY and tape-odd (external)
12	
13	Manual panel execute
14	
15	
P _L	
P _H	

3A CC STATUS REGISTER LAYOUT

OPERATION

4.03 Depending on the time of the interrupt relative to a microsequence, a period of up to one complete instruction sequence may elapse before the interrupt is acknowledged by the microprogram control. When the all zeros location of microstore is accessed at the end of an OP code, the microprogram control tests for interrupts. If an unmasked interrupt is present and the block interrupt (BIN) is not set, a hard-wired interrupt address is gated into the MAR regardless of whether or not a previous main memory fetch is completed (DR=1). This address initiates a routine in microstore that tests for the highest level of interrupt within the IS and translates the bit position of that interrupt to a data constant. This constant points to the main memory program which handles that type of interrupt. During this process, the microprogram control sets and clears the BIN. The BIN is used by the microprogram control to block any additional interrupts. This provides the interrupt program time to set up and handle the present interrupt without others interfering.

4.04 A software check, which is a part of the periodic detection test, is used to detect faults in the interrupt facility.

5. MAIN MEMORY STATUS (MMS)

BIT	DESIGNATION	CC	FUNCTION
0	Memory Maintenance (MM) 1	0	Used with MM2 and RW to formulate the command sent in a memory operation.
1	MM1	1	Same as bit 0.
2	MM2	0	Used with MM1 and RW to formulate the command sent in a memory operation.
3	MM2	1	Same as bit 2.
4	Read or Write (RW)	0	Indicates whether memory is to perform a read or write operation.
5	RW	1	Same as bit 4.
6	Idle (IDL)	0	Indicates all memory operations be performed on the other 3A CC memory and not the memory associated with this 3A CC.
7	IDL	1	Same as bit 6.
8	Update (UPD)	0	Indicates whether to update the off-line memory or not.
9	UPD	1	Same as bit 8.
10	Isolate (ISO)	0	Prevents the other 3A CC from accessing the associated memory for this 3A CC.
11	ISO	1	Same as bit 10.
12	Block Double Store Read (BDSR)	0	
13	BDSR	1	
14	Compliment Write (CWO)		Also gated to bit 16 of gating bus (GB).
15	Block Error Checks (BECO)		Also gated to bit 16 of GB.
P _L	Set to 0		
P _H	Set to 1		

3A CC STATUS REGISTER LAYOUT