Network Services Complex J4A017
Description
Common Channel Signaling Systems

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Tables

1. Overview

1.01 This practice provides a description of the Network Services Complex (NSCX) equipment. It is intended to serve as an overall reference for the planning, operation, and administration stages of the NSCX for system engineering and the craftpersons associated with the system. The following subjects are included:

- Physical descriptions
- Functional descriptions
- Network service complex controls and indicators
- Power requirements
- Maintenance philosophy.

1.02 This practice is being reissued to:

- Incorporate the new 2 Gbyte Hard Disk Unit information.
- Incorporate information on the new Automatic Speech Recognition (ASR) feature.

1.03 This practice does not contain admonishments.

1.04 AT&T welcomes your comments on this practice. Your comments will aid us in improving the quality and usefulness of AT&T documentation. Please use the Feedback Form provided in this practice or call the AT&T Documentation Comment Hot-Line Service (1-800-334-0404 or (919)727-6681 in North Carolina).

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1.06 Every effort was made to ensure that the information in this practice was complete and accurate at the time of printing. However, information is subject to change.

1.07 This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the installation manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

1.08 Part 9 lists the abbreviations and acronyms with applicable terms used in this practice.

1.09 This practice is issued by:

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2. General

Purpose of the Network Services Complex

2.01 Network Service Complexes are families of equipment frames that provide teleconferencing and Direct Services Dialing Capability (DSDC) features between two or more physically remote locations over the toll and local telephone networks. Figure 1 shows the interface between the NSCX and a 4ESS™ switch. There are two NSCX configurations designed to support these features. Each of these configurations include common software and firmware that implement common NSCX functions. The NSCX generic program for each type of NSCX consists of the common software combined with the appropriate feature software.

2.02 Each NSCX provides automated caller (customer or operator) interactive capabilities for telephone network services. These interactive capabilities consist of:

- Playing recorded announcements that contain instructions or prompts to callers
- Receiving touch-tone dialed signals that correspond to a chosen service option, or a telephone directory number.
- Collecting single digit (1-9) spoken words from callers that correspond to a chosen service option or a telephone number (DSD only).

2.03 The two NSCX configurations and their uses are:

(a) **Voice-Only Teleconferencing:** This NSCX is used for customer- and/or operator-established conference calls for voice or voice and analog graphics use only. Figure 2 shows a block diagram of a Voice Only interface. This complex is equipped with two 64-port audio bridges. Each audio bridge combines and distributes the Pulse Code Modulation (PCM) voice samples of speakers on a conference to other participants of the conference. Trunks are assigned to only 60 ports of each audio bridge. Each teleconferencing NSCX is equipped with 120 intraoffice trunks. At least one trunk is reserved for operator access. Conferences may range in size from 3 to 59 ports (conference legs) per audio bridge. Each audio bridge can support many active conferences simultaneously, provided the total conference legs do not exceed the 59 ports available for service.

(b) **Direct Services Dialing Capability:** This NSCX is used to implement DSDC services (Figure 3). The first DSDC service to use this NSCX is the Advanced 800 Service. The Courtesy Response and Call Prompter features use this NSCX.

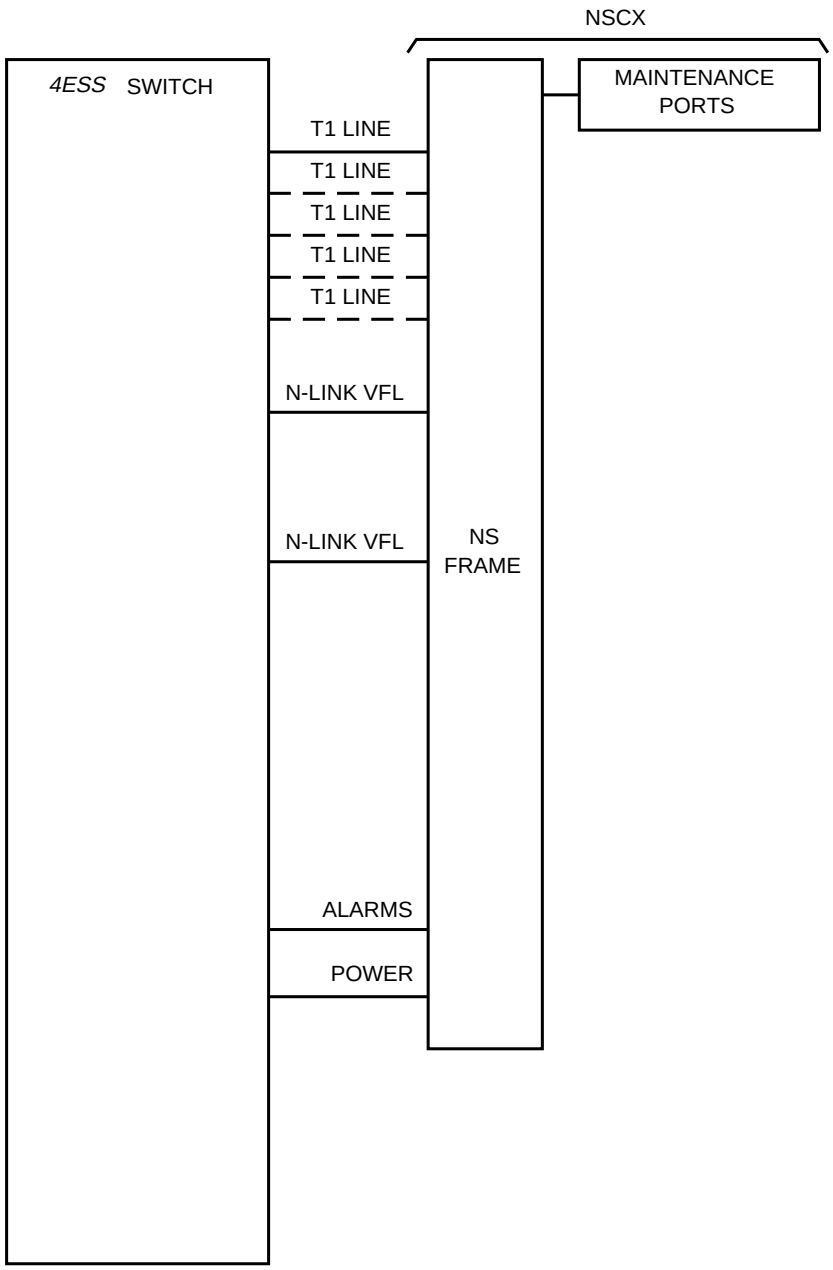


Figure 1. NSCX Interface

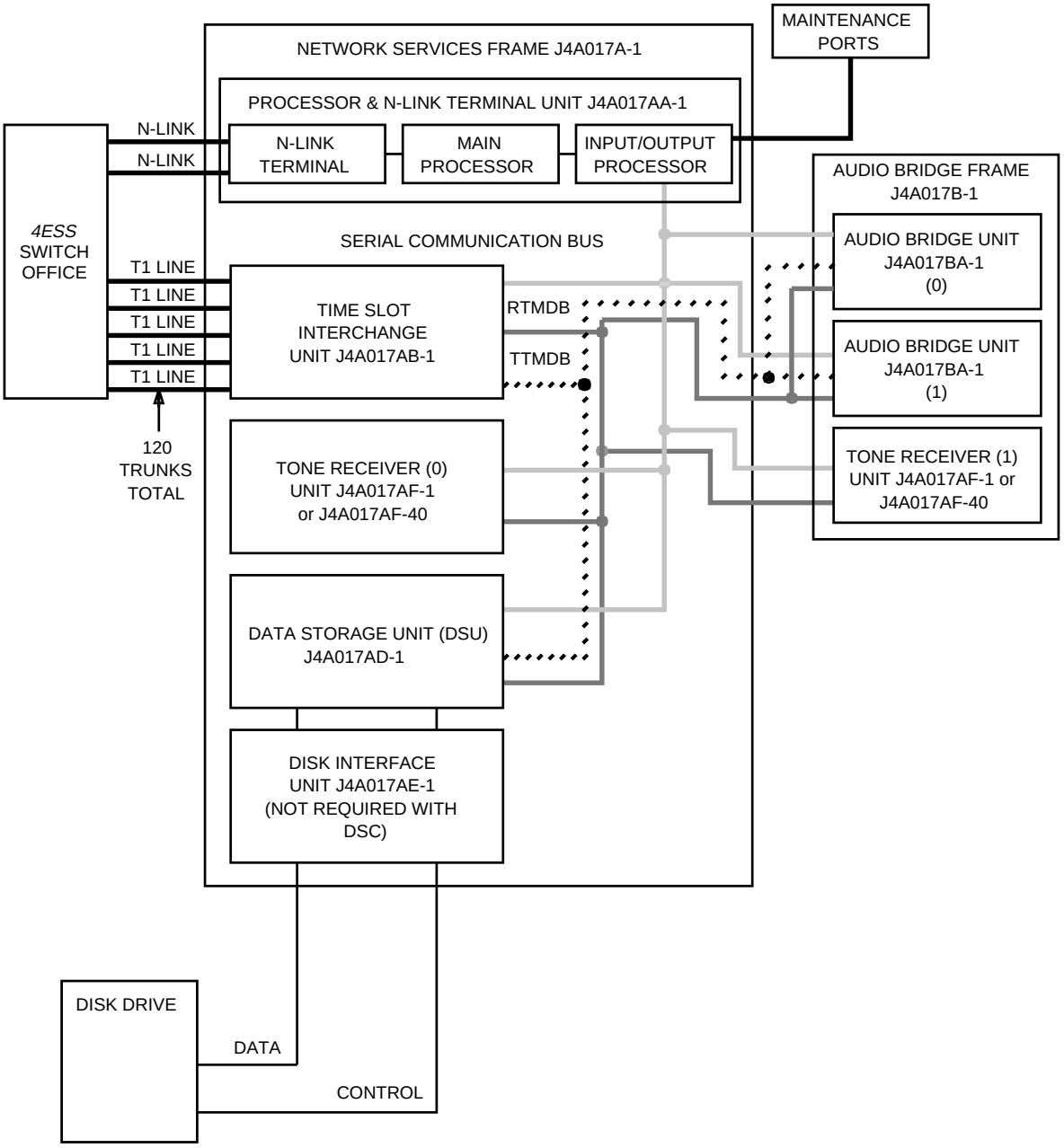


Figure 2. Audio Teleconferencing Complex

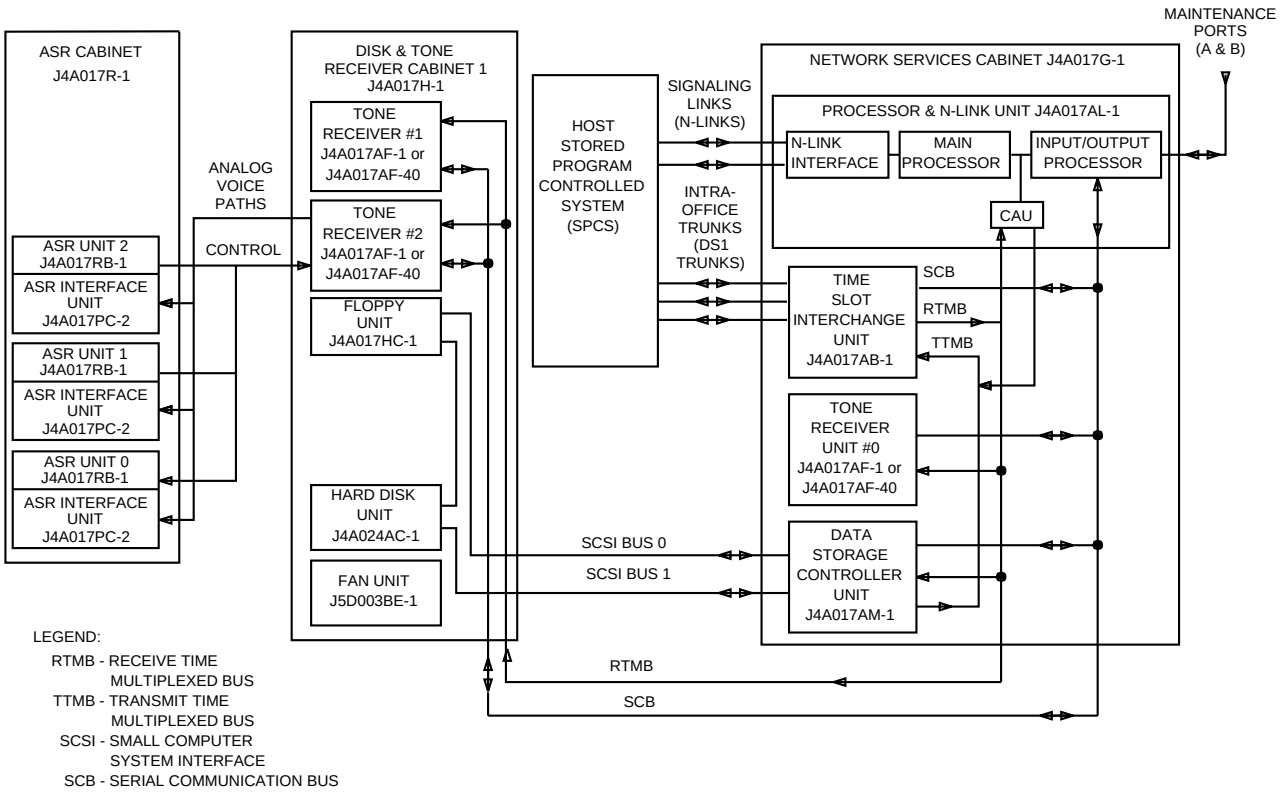


Figure 3. DSD8 NSCX Complex

Equipment Characteristics

2.04 Network Service Complexes must be supported by a host Stored Program-Controlled Switching (SPCS) system with access to the Common Channel Interoffice Signaling (CCIS) system. The 4ESS switch, equipped with the 4E7 or later generic program, was used to support the first NSCXs.

2.05 Each NSCX is interfaced to the SPCS system by intraoffice Digital Service 1 (DS1) digital trunks terminated on Digital Interface Frames (DIFs) and a single pair of N-links to CCIS terminal group frames. In addition, major and minor alarm outputs from each NSCX are connected to the SPCS system office alarm system.

2.06 All NSCX trunks must be terminated on a DIF via a Digital Cross-Connect (DSX-1) frame. The voice-only teleconferencing NSCX requires 120 terminations (five DS1 trunks). Each DSDC NSCX requires 24, 48, or 72 terminations (one, two, or three DS1 trunks). The five DS1 trunks from a single teleconferencing NSCX must be spread over several (as many as five) digital interface units. The DS1 trunks from each of several DSDC NSCXs should be terminated on different DIFs.

2.07 On a NSCX equipped with ASR, all trunks must be equipped with echo cancelers to prevent the customer's announcement from being recognized as caller input. The echo canceler on DS1-1, Trunk 1 must be deactivated so the announcement data can pass.

2.08 The number of NSCXs that may be engineered for an 4ESS switch is limited to 28. Since each teleconferencing NSCX contains simplex hardware, two or more NSCXs are normally provided in an office for each type of NSCX service (voice, voice and data, and DSDC) required.

2.09 Each type of NSCX is fully equipped for a particular service. One type of NSCX cannot be easily converted to another NSCX type.

2.10 Power (–48 V DC and 208 V AC) to NSCXs from power distribution frames should be assigned as described in Part 6 of this practice.

2.11 The maintenance interface unit in the network services frame is equipped with two 201D data sets for interconnecting the two N-links required for each NSCX. A maintenance jack assembly provides test access to the two N-links. The maintenance interface unit is also equipped with RS-232C-type connectors which provide access to two Input/Output Processor (IOP) maintenance ports. These two ports provide maintenance access to the NSCX from local data terminal equipment and remote operations, administration, and maintenance facilities.

3. Physical Description

General

3.01 All of the hardware for the NSCX except for the ASR is contained in equipment frames. The ASR hardware is contained in a cabinet. The equipment frames used for each NSCX are 7 feet high, 2 feet 2 inches wide, and 18 inches deep. All the units mounted in each frame contain FASTECH® power unit circuit packs arranged according to function. Horizontal equipment locations are specified in increments of 1/8 inch. Integrated circuits of the dual in-line package variety and discrete components are both used in the circuit packs. Most power units are mounted in the same unit in which they are used and adjacent to the circuit pack group served. Each circuit pack and power unit is labeled on designation strips to indicate its identity and boundaries. The controls and indicators provided on two circuit pack types and on other frame equipment are described in Part 5.

3.02 The ASR cabinet is 6 feet tall, 2-feet 6-inches wide, and 1-foot 7SR cabinet is 6 feet tall, 34 inches wide, and 19-1/8 inches deep. The ASR Unit contains slots for AT* computer type circuit packs. The ASR unit also contains a power supply, a power switch, and three fans.

Equipment Arrangements

3.03 Each NSCX consists of several frames. The number of frames vary depending on the type of NSCX. The quantity of frames for each type of NSCX is shown in the following paragraphs.

3.04 Voice-Only Teleconferencing NSCX:

- One network services frame (J4A017A-1)
- One moving head disk frame (J1C131B-1)
- One audio bridge frame (J4A017B-1, List 1 and 2) equipped with two audio bridge units and one tone receiver unit.

3.05 Voice and Analog Graphics Teleconferencing NSCX:

- One network services frame (J4A017A-1)
- One moving head disk frame (J1C131B-1)
- One audio bridge frame (J4A017B-1, List 1 and 2) equipped with two audio bridge units and one tone receiver unit.

3.06 Direct Services Dialing Capability NSCX DSD8 or later without ASR:

- One network services frame (J4A017G-1)
- One disk and tone receiver frame (J4A017H-1).

3.07 Direct Services Dialing Capability NSCX DSD8 or later with ASR:

- One network services frame (J4A017G-1)
- One disk and tone receiver frame (J4A017H-1)
- One ASR cabinet (J4A017R-1).

Network Services Frame (J4A017A-1)

3.08 The network services frame is the basic frame required in each NSCX type, except the DSDC application using DSD8 generic or later, which uses a J4A017G-1 network services frame. The basic frame is equipped with one each of the following units (Figure 4):

- Processor and N-link terminal unit (J4A017AA-1)
- Time slot interchange unit (J4A017AB-1)
- Maintenance interface unit (J4A017AC-1)
- Data storage unit (J4A017AD-1)
- Disk connector unit (J4A017AE-1)
- Tone receiver unit (J4A017AF-1 or J4A017AF-40)
- Fuse panel (J4A017AG-1)
- Filter unit (J1A053AA-1, L100).

NOTE:
Network services frames in a system that has been upgraded to DSD8 may be equipped with a J4A017AL-1 Processor & N-Link Unit and a J4A017AM-1 Data Storage Controller Unit. The information for these units are explained in paragraphs 3.32 and 3.35.

* AT is a registered trademark of International Business Machines Corp.

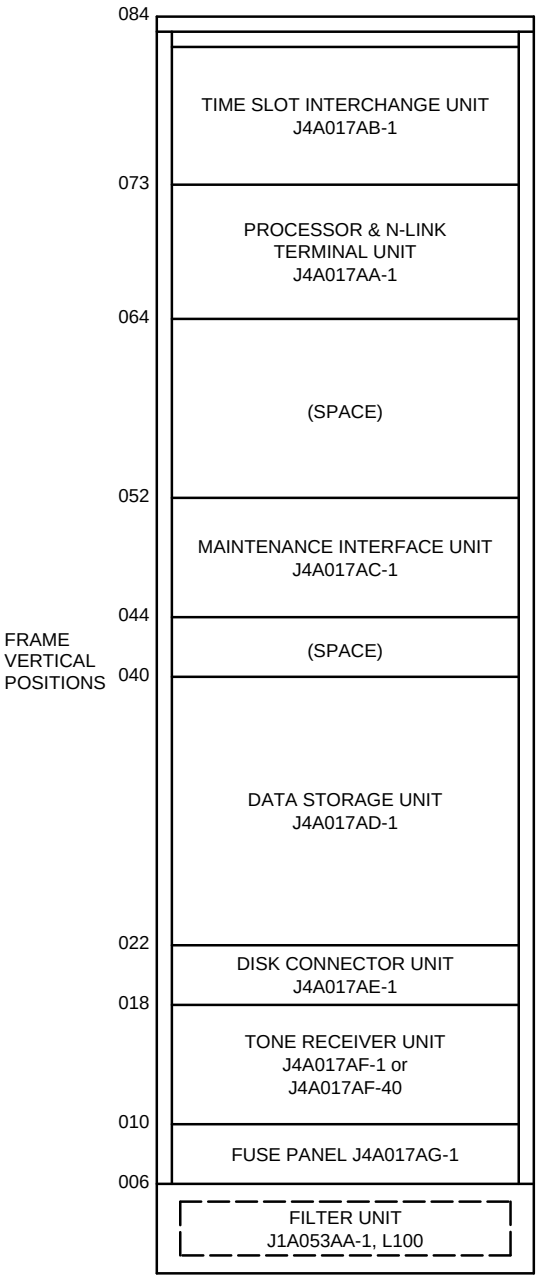


Figure 4. Network Services Frame (J4A017A-1) — Equipment Identification

A. Processor and N-Link Terminal Unit (J4A017AA-1)

3.09 The processor and N-link terminal unit (Figure 5) contains the NSCX main processor, IOP, and the N-link terminal. This unit consists of 14 circuit packs and one 495JA power unit. Unit (and frame) List options 2 and 3 each provide an additional 256 K of Random Access Memory (RAM) to the basic 512 K memory (TN641 circuit packs). The TN643 circuit pack (MC-4A020A1) contains the IOP firmware. The TN639 circuit pack (MC-4A018A1) contains the N-link terminal firmware. The TN642/TN636 circuit pack has been replaced by a TN637 pack for 4NSDSD6/4NSTC6 generic. A test access connector at horizontal location 050 is provided for engineering development use only. Circuit pack boundaries for the processor, IOP, and N-link terminal unit are outlined on the unit designation strip.

B. Time Slot Interchange Unit (J4A017AB-1)

3.10 The time slot interchange unit (Figure 6) consists of nine circuit packs, one 495JA power unit, and one 494G1 power unit when fully equipped. The unit can be equipped with TN674, TN675, or TN676 circuit packs to interface a maximum of five DS1 trunks. All teleconferencing NSCXs are equipped for five DS1 trunks. The DSDC NSCX is equipped for one, two, or three DS1 trunks. The TN674, TN675, or TN676 equipment locations for the the five DS1 trunks are as follows:

- First DS1 trunk - equipment location 04-082
- Second DS1 trunk - equipment location 04-090
- Third DS1 trunk - equipment location 04-098
- Fourth DS1 trunk - equipment location 04-106
- Fifth DS1 trunk - equipment location 04-114.

3.11 The TN674, TN675, and TN676 circuit packs are designed to interface different DS1 trunk cable lengths to the DSX-1 cross-connect frame. The time slot interchange unit list options are:

- List 2 (TN674) - 0 to 220 feet
- List 3 (TN675) - 220 to 440 feet
- List 4 (TN676) - 440 to 655 feet.

C. Maintenance Interface Unit (J4A017AC-1)

3.12 The maintenance interface unit (Figure 7) consists of two 201D-L1B data sets, two jack assemblies, two terminal strips, and four RS-232C-type connectors with two associated 552A keys (two- position rotary switches) labeled A and B. AT&T 592-033-100 *Data Set 201D Description and Operation* provides a description of the 201D-type data set. The maintenance jack assembly provides maintenance access to the two NSCX N-links. The telephone and teletypewriter jack assembly is connected to the host office interframe communications facilities on an office-engineered basis. The two terminal strips are used to connect the NSCX DS1 trunks, N-links, and office alarm outputs to the host office facilities. These two terminal strips are also used to interconnect interframe wiring within the NSCX. The four RS-232C-type connectors and associated keys (A and B) serve to interface the two IOP maintenance ports with local and/or remote data terminal equipment.

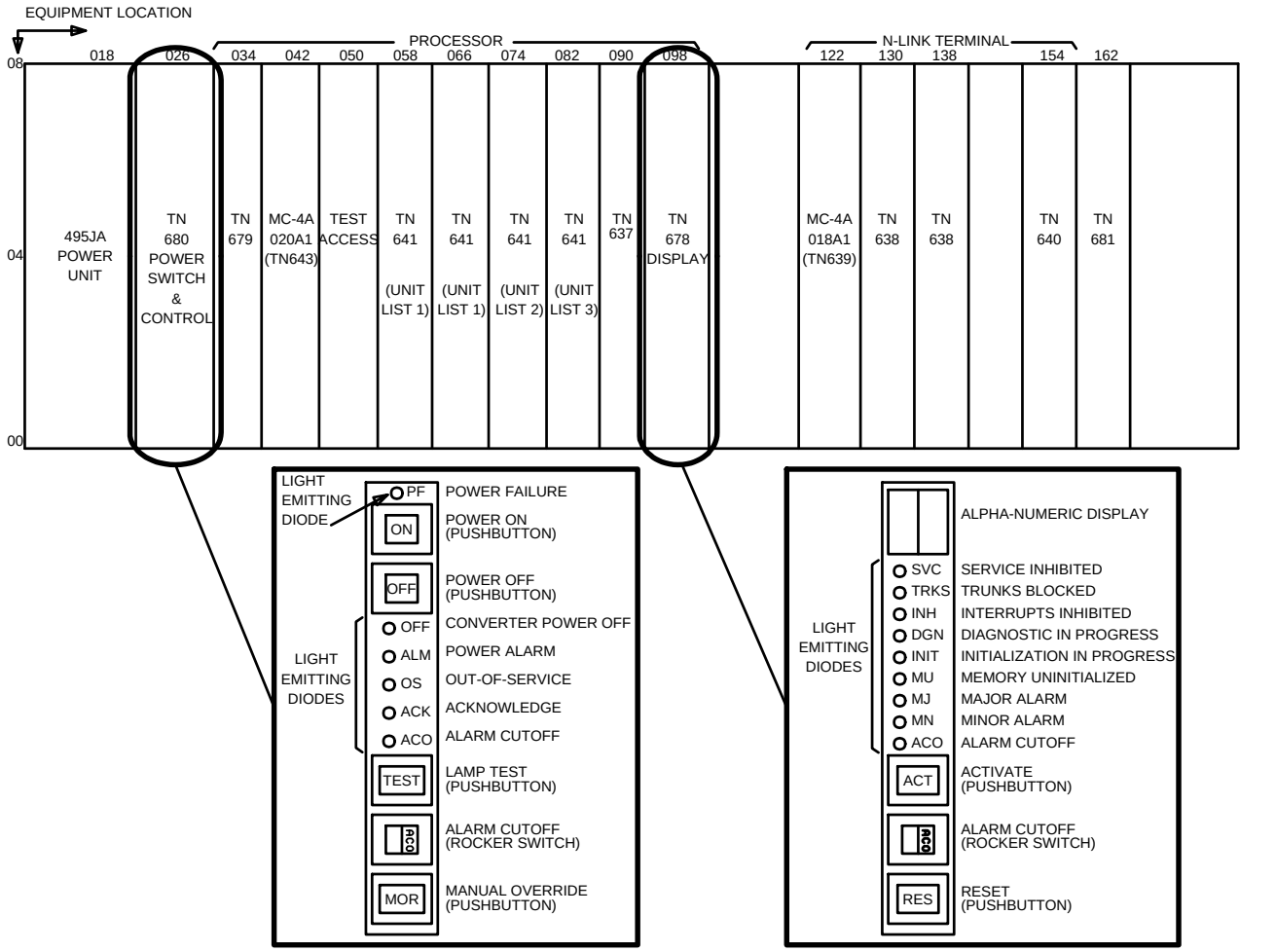


Figure 5. Processor and N-Link Terminal Unit J4A017AA-1 — Equipment Identification

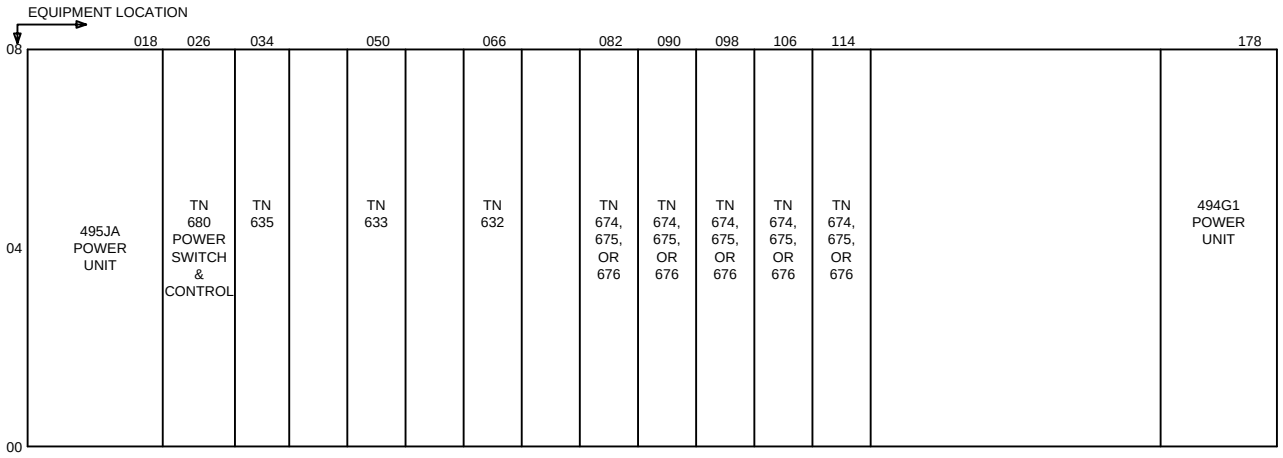


Figure 6. Time Slot Interchange Unit—Equipment Identification

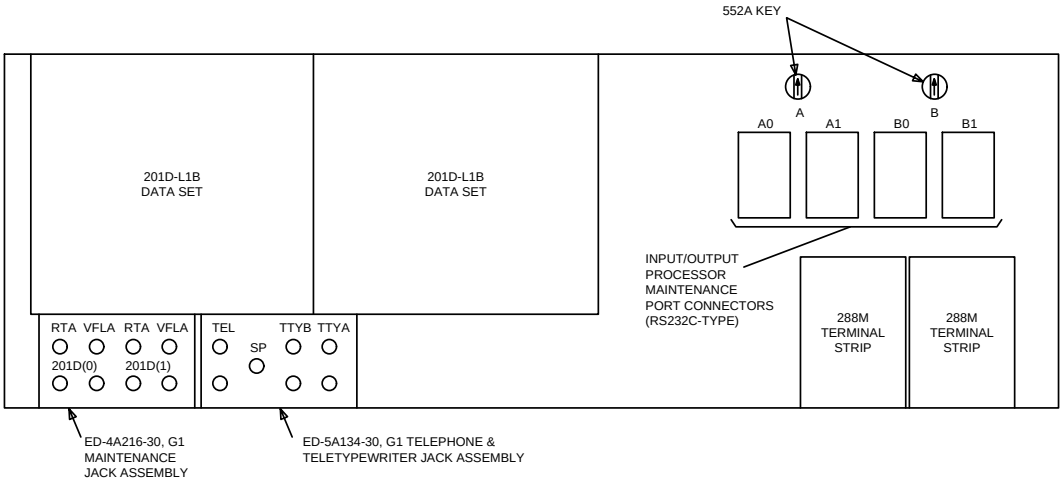


Figure 7. Maintenance Interface Unit—Equipment Identification

D. Data Storage Unit (J4A017AD-1)

3.13 The data storage unit (Figure 8) consists of 16 circuit packs and three 495JA power units. A test access connector at location 04-090 is provided for engineering development use only. Three TN62B circuit packs (MC-4A017A1, MC-4A017B1, MC-4A017C1/MC-4A017C1B) provide firmware memory storage for the microprocessor-based data storage unit. For Direct Services Dialing Capability NSCXs, one or two more data storage units can be equipped in the direct services dialing frame (J4A017H-1).

E. Disk Connector Unit (J4A017AE-1)

3.14 The disk connector unit (Figure 4) consists of two cable connectors used to connect the moving head disk drive to the network services frame. The moving head disk drive is located within the lower part of the moving head disk frame. For Direct Services Dialing Capability NSCXs, one or two additional disk connector units can be equipped in the direct services dialing frame (J4A017H-1).

F. Tone Receiver Unit (J4A017AF-1 or J4A017AF-40)

3.15 The tone receiver unit (Figure 9) consists of eight circuit packs one 495JA power unit. An additional circuit pack is required if ASR is provided. The TN645 circuit pack (MC-4A021A1 without ASR, MC-4A069A1 with AS) provides firmware storage for the microprocessor-based tone receiver unit. This unit provides 24 channels of digital tone receivers. In order to provide ASR capabilities the tone receiver must be version J4A017AF-40 and an additional circuit pack is added. This circuit pack is the TN1811 (MC-4A068A1) and provides the control and data interface to the ASR interface. For voice-only teleconferencing NSCXs, two tone receiver units are required. In this case, the second tone receiver unit is equipped in the audio bridge frame (J4A017B-1). For Direct Services Dialing Capability NSCXs, one or two more tone receiver units can be equipped in the direct services dialing frame (J4A017H-1).

G. Fuse Panel (J4A017AG-1)

3.16 The fuse panel (Figure 10) consists of four fuse blocks, one 131J1 power unit, and one 131N1A power unit. The fuse blocks are equipped with alarm- type fuses. The fuses distribute +12 V, +24 V, and –48 V (as required) to the units in the network services frame.

H. Filter Unit (J1A053AA-1, L100)

3.17 The filter unit is located in the base of the network services frame (Figure 4). The filter unit provides protection from short voltage transients that may appear on the two –48 V power feeders from the power distribution frame. This unit also filters the +12 V output of the 131J1 power unit located in the fuse panel.

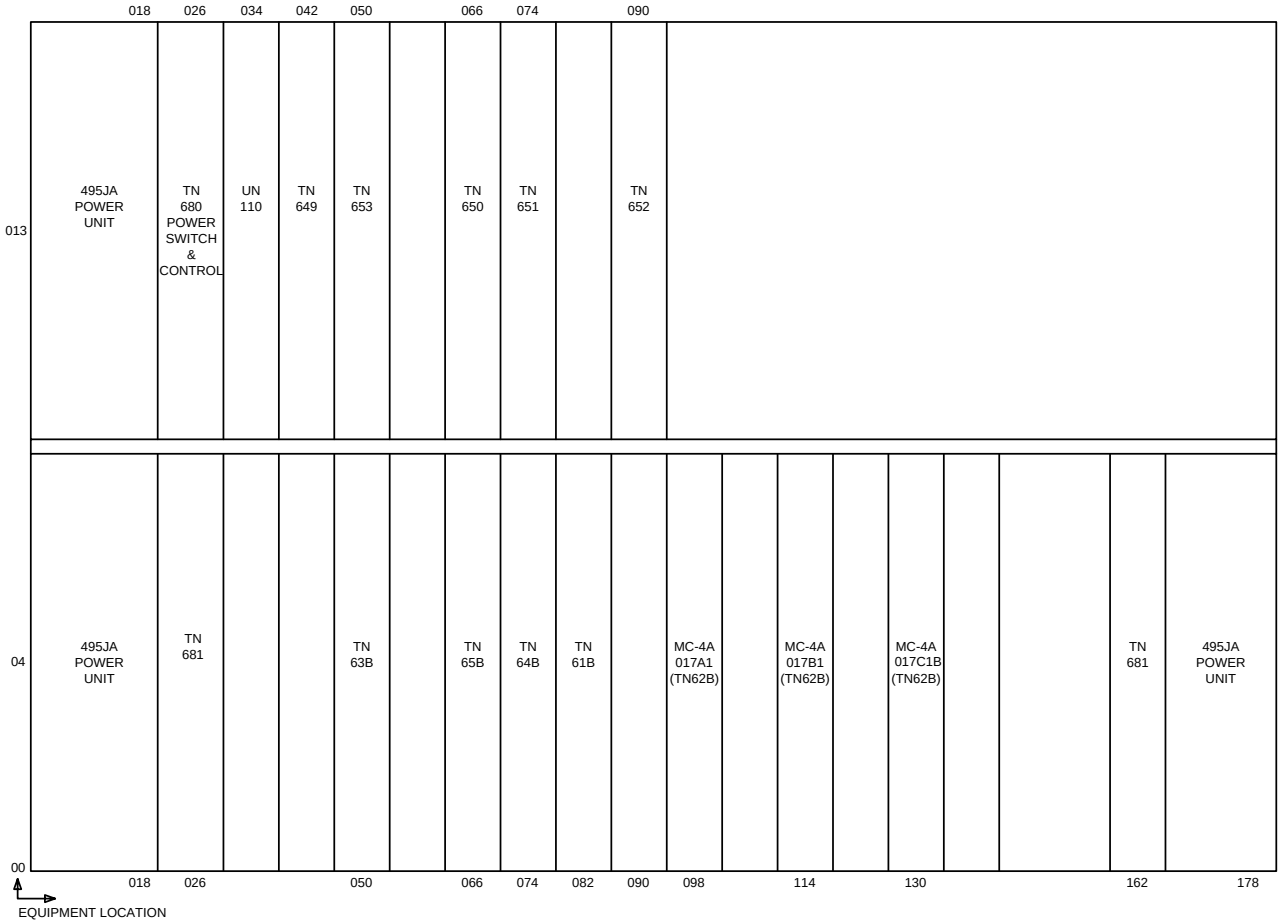


Figure 8. Data Storage Unit J4A017AD-1 — Equipment Identification

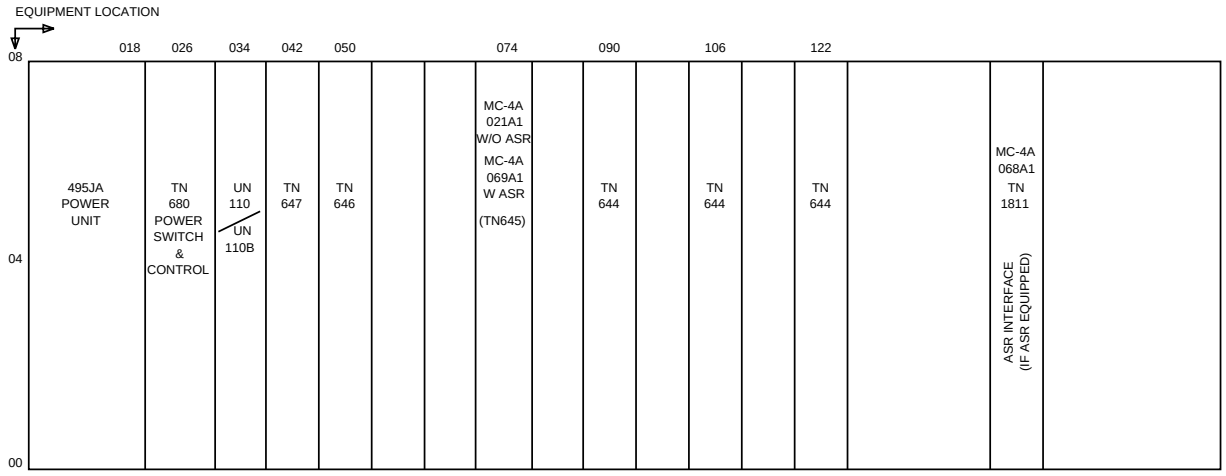


Figure 9. Tone Receiver Unit J4A017AF-1 or J4A017AF-40 — Equipment Identification

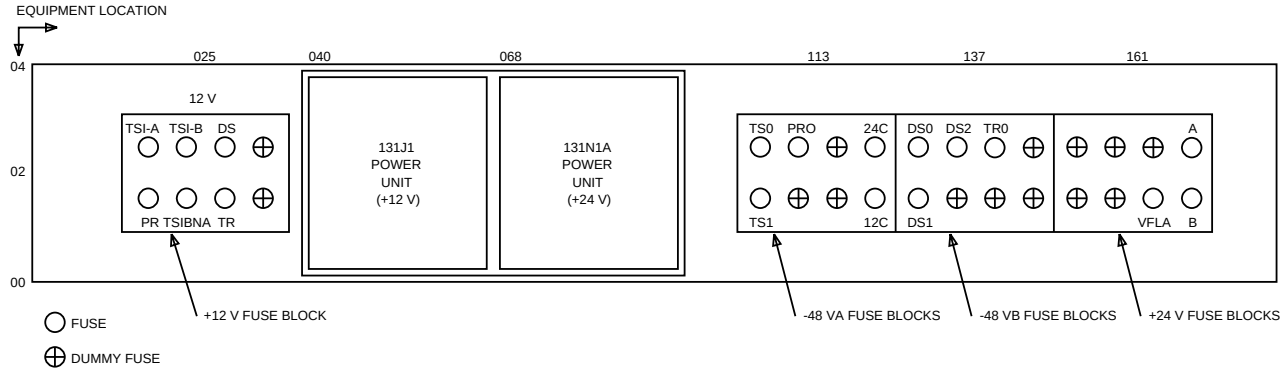


Figure 10. Fuse Panel J4A017AG-1 — Equipment Identification

Audio Bridge Frame (J4A017B-1)

3.18 The audio bridge frame (Figure 11) is required in teleconferencing NSCXs.

3.19 In a voice-only or voice and analog graphics teleconferencing NSCX, the audio bridge frame (Lists 1 and 2) is equipped with:

- Two audio bridge units (J4A017BA-1)
- One tone receiver unit (J4A017AF-1 or J4A017AF-40).
- Fuse panel (J4A017BB-1, L1, L2)
- Filter unit (J1A053AA-1, L100).

3.20 Each audio bridge unit provides 64 ports. Trunks are assigned to 60 of the 64 ports in each unit. The remaining four ports of each audio bridge unit are used for maintenance purposes. The tone receiver unit in the network services frame, together with the tone receiver unit in the audio bridge frame, provides a total of 48 digital tone receivers for a voice-only or voice and analog graphics teleconferencing NSCX.

A. Audio Bridge Unit (J4A017BA-1)

3.21 The audio bridge unit (Figure 12) consists of 44 circuit packs and six 495JA power units arranged in three equipment rows. The TN661 circuit pack (MC-4A022A1) and the TN62 circuit packs (MC- 4A016A1, MC-4A016B1, and MC-4A016C1) provide firmware storage for the microprocessor-based unit. A test access connector at location 13-114 is provided for engineering development use only.

B. Fuse Panel (J4A017BB-1)

3.22 The fuse panel (Figure 13) consists of three fuse blocks and one 131J1 power unit. The fuse blocks are equipped with alarm-type fuses. The List 2 option provides the additional fuses required to distribute +12 V and –48 V to the tone receiver unit and the second audio bridge unit (required for voice-only teleconferencing NSCXs). The List 1 option provides fuses to distribute +12 V and –48 V to the single audio bridge unit required for voice and data teleconferencing NSCXs.

C. Filter Unit (J1A053AA-1, L100)

3.23 The filter unit is located in the base of the audio bridge frame (Figure 11). The filter unit provides protection from short voltage transients that may appear on the two –48 V power feeders from the power distribution frame. This unit also filters the +12 V output of the 131J1 power unit located in the fuse panel.

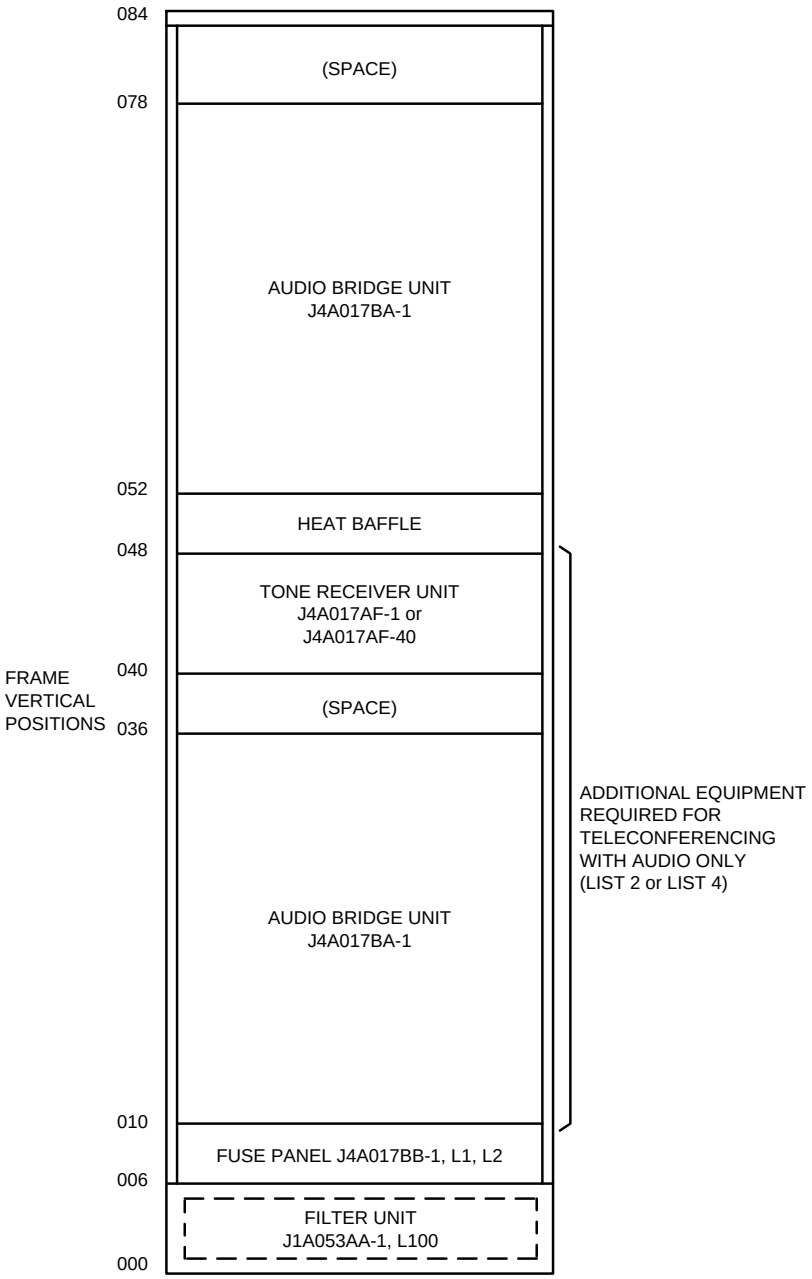


Figure 11. Audio Bridge Frame J4A017B-1 — Equipment Identification

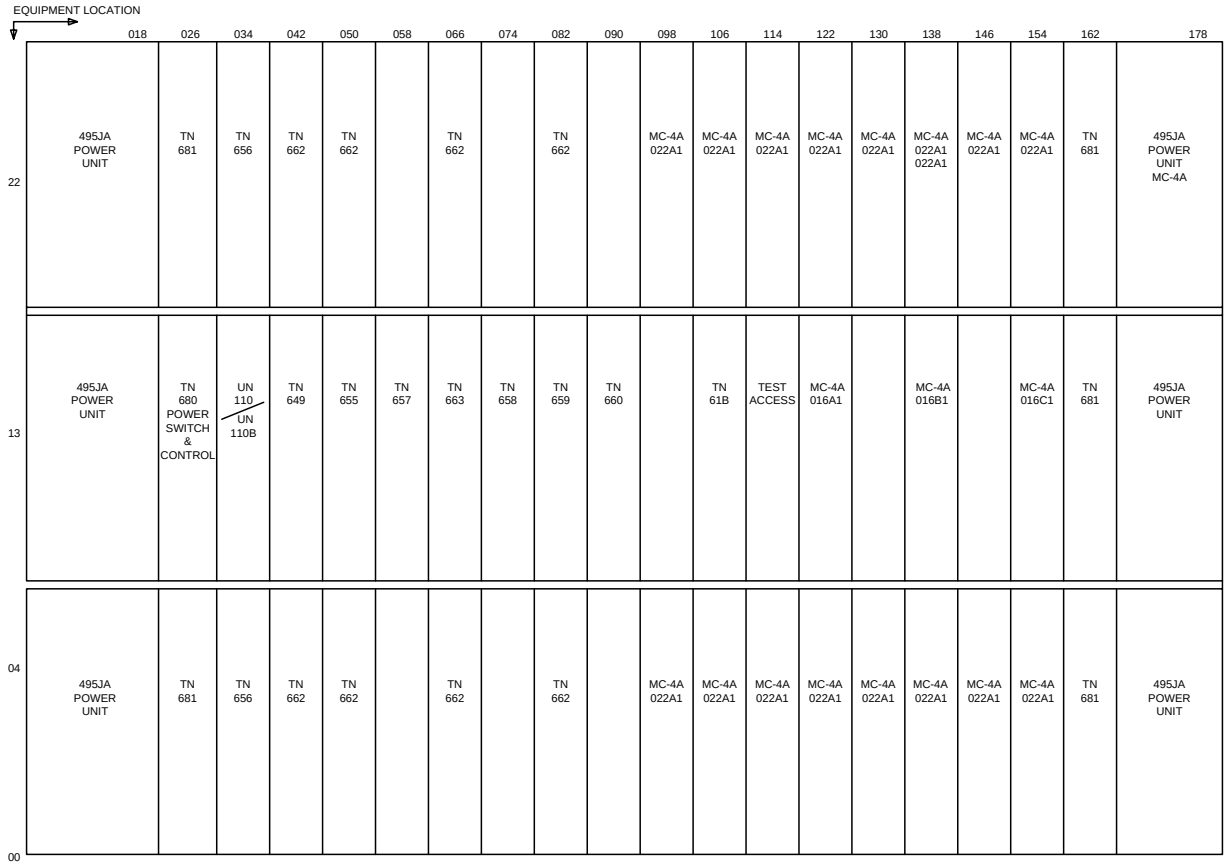


Figure 12. Audio Bridge Unit J4A017BA-1 — Equipment Identification

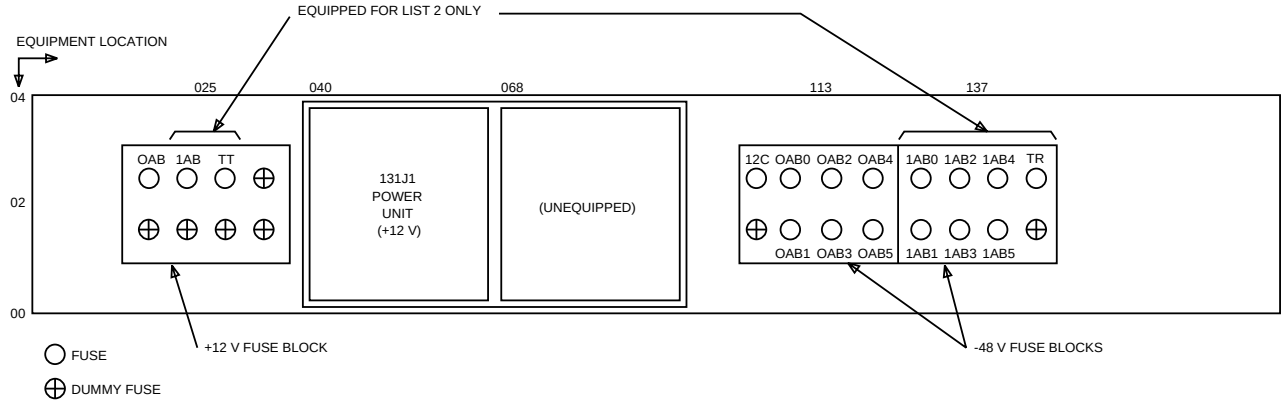


Figure 13. Fuse Panel J4A017BB-1 — Equipment Identification

Direct Services Dialing Frame (J4A017H-1)

3.24 The Direct Services Dialing (DSD) frame (Figure 14) is required for a Direct Services Dialing Capability (DSDC) NSCX when more than 24 trunks are required with DSD6 generic; for DSD7 or later generic, this frame will not be used. The direct services dialing frame can provide facilities for 24 or 48 trunks in addition to the 24-trunk capacity of the DSD6 network services frame. The direct services dialing frame is equipped as follows:

- One or two data storage units (J4A017AD-1)
- One or two disk connector units (J4A017AE-1)
- One or two tone receiver units (J4A017AF-1 or J4A017AF-40)
- One fuse panel (J1A017DA-1)
- One filter panel (J1A053AA-1, L100).

A. Data Storage Unit (J4A017AD-1)

3.25 The data storage unit (Figure 8) consists of 16 circuit packs and three 495JA power units. Three TN62B circuit packs (MC-4A017A1, MC-4A017B1, and MC4A017C1) provide firmware memory storage for the microprocessor-based data storage unit.

B. Disk Connector Unit (J4A017AE-1)

3.26 The disk connector unit (Figure 14) consists of two cable connectors used to connect the moving head disk drive to the direct services dialing frame. The moving head disk drive is located within the lower part of the moving head disk frame.

C. Tone Receiver Unit (J4A017AF-1 or J4A017AF-40)

3.27 The tone receiver unit (Figure 9) consists of eight circuit packs one 495JA power unit. An additional circuit pack is required if ASR is provided. The TN645 circuit pack (MC-4A021A1 without ASR, MC-4A069A1 with AS) provides firmware storage for the microprocessor-based tone receiver unit. This unit provides 24 channels of digital tone receivers. In order to provide ASR capabilities the tone receiver must be version J4A017AF-40 and an additional circuit pack is added. This circuit pack is the TN1811 (MC-4A068A1) and provides the control and data interface to the ASR interface. For voice-only teleconferencing NSCXs, two tone receiver units are required. In this case, the second tone receiver unit is equipped in the audio bridge frame (J4A017B-1). For Direct Services Dialing Capability NSCXs, one or two more tone receiver units can be equipped in the direct services dialing frame (J4A017H-1).

D. Fuse Panel (J4A017DA-1)

3.28 The fuse panel (Figure 15) consists of three fuse blocks and one 131J1 power unit. The fuse blocks are equipped with alarm-type fuses. The fuses distribute –48 V and +12 V as required to the units on the direct services dialing frame.

E. Filter Unit (J1A053AA-1, L100)

3.29 The filter unit (Figure 14) is located in the base of the direct services dialing frame. The filter unit provides protection from short voltage transients that may appear on the two –48 V power feeders from the power distribution frame. This unit also filters the +12 V output of the 131J1 power unit located on the fuse panel.

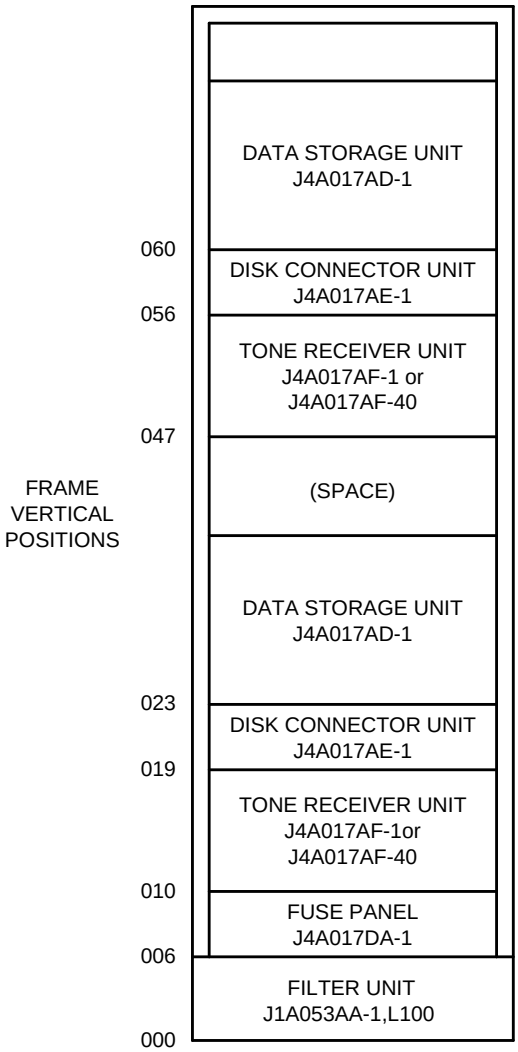


Figure 14. Direct Services Dialing Frame J4A017H-1 — Equipment Identification

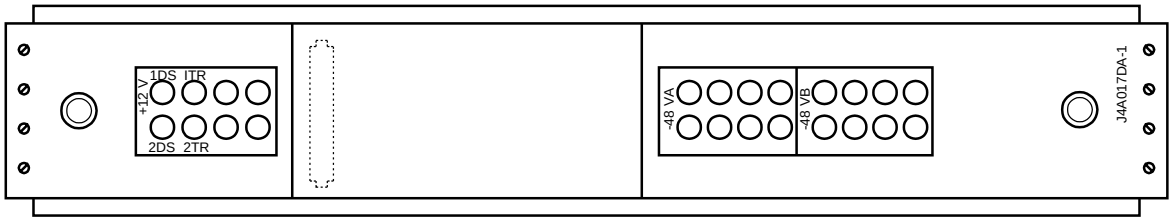


Figure 15. Fuse Panel J4A017DA-1 — Equipment Identification

Network Services Frame (J4A017G-1)

3.30 The network services frame J4A017G-1 is the basic frame required for a DSD8 generic or later network services complex. It is equipped with each of the units listed (Figure 16):

- Processor and N-link terminal unit (J4A017AL-1)
- Time slot interchange unit (J4A017AB-1)
- Maintenance interface unit (J4A017AC-1)
- Data storage controller unit (J4A017AM-1)
- Tone receiver unit (J4A017AF-1 or J4A017AF-40)
- Fuse panel (J4A017GA-1)
- Filter unit (J1A053AA-1, List 100).

3.31 The List 2 network services frame provides the one megabyte memory circuit pack. A second List 2 circuit pack is available for memory growth. List 3 is for the centralized update feature.

A. Processor and N-link Terminal Unit (J4A017AL-1)

3.32 The processor and N-link terminal (Figure 17) contains the NSCX main processor, IOP, N-link, and centralized announcement update pack. This unit consists of 12 circuit packs and two 495JA power units. Unit List option 2 provides one megabyte of memory (maximum quantity of 2). Unit List option 3 provides the centralized announcement updates. The TN1590 circuit pack (MC-4A055A1) contains the IOP firmware. The TN639 circuit pack (MC-4A018A1) contains the N-link terminal interface. The TN637 circuit pack is the main processor.

B. Time Slot Interchange Unit (J4A017AB-1)

3.33 The time slot interchange unit is discussed in paragraphs 3.10 and 3.11. (Figure 6).

C. Maintenance Interface Unit (J4A017AC-1)

3.34 The maintenance interface unit is discussed in paragraph 3.12 (Figure 8).

D. Data Storage Controller Unit (J4A017AM-1)

3.35 The Data Storage Controller (DSC) unit (Figure 18) consists of 13 circuit packs and two 495JA power units. A test access connector is provided for engineering development use. The TN1577 circuit pack (MC-4A200A) provides firmware memory storage for the microprocessor-based data storage controller unit. Only one DSC is required for the NSCX since the DSC can handle a total of 72 trunks.

E. Tone Receiver Unit (J4A017AF-1 or J4A017AF-40)

3.36 The tone receiver unit is discussed in paragraph 3.15 (Figure 10).

F. Fuse Panel Unit (J4A017GA-1)

3.37 The fuse panel (Figure 19) consists of four fuse blocks, one 131J1 power unit, and one 131N1A power unit. The fuse blocks are equipped with alarm type fuses. The fuses distribute the +12 V, +24 V, and –48 V to the units of the NSCX (as required).

G. Filter Unit (J1A053AA-1, L100)

3.38 Paragraph 3.17 discusses the filter unit (Figure 4).

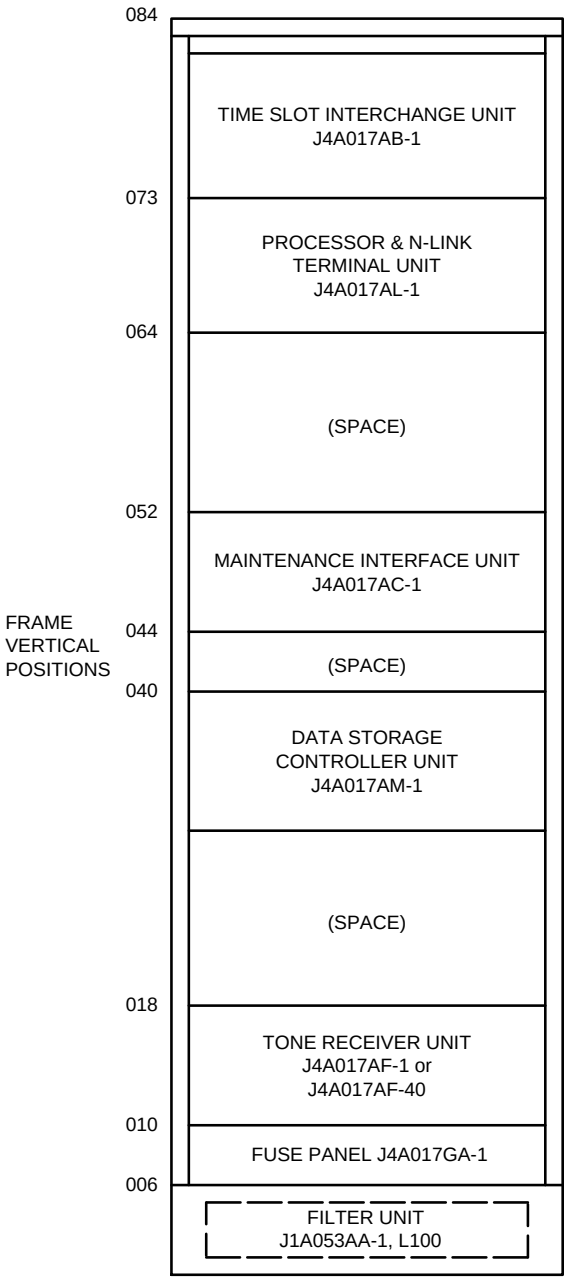


Figure 16. Network Services Frame J4A017G-1 — Equipment Identification

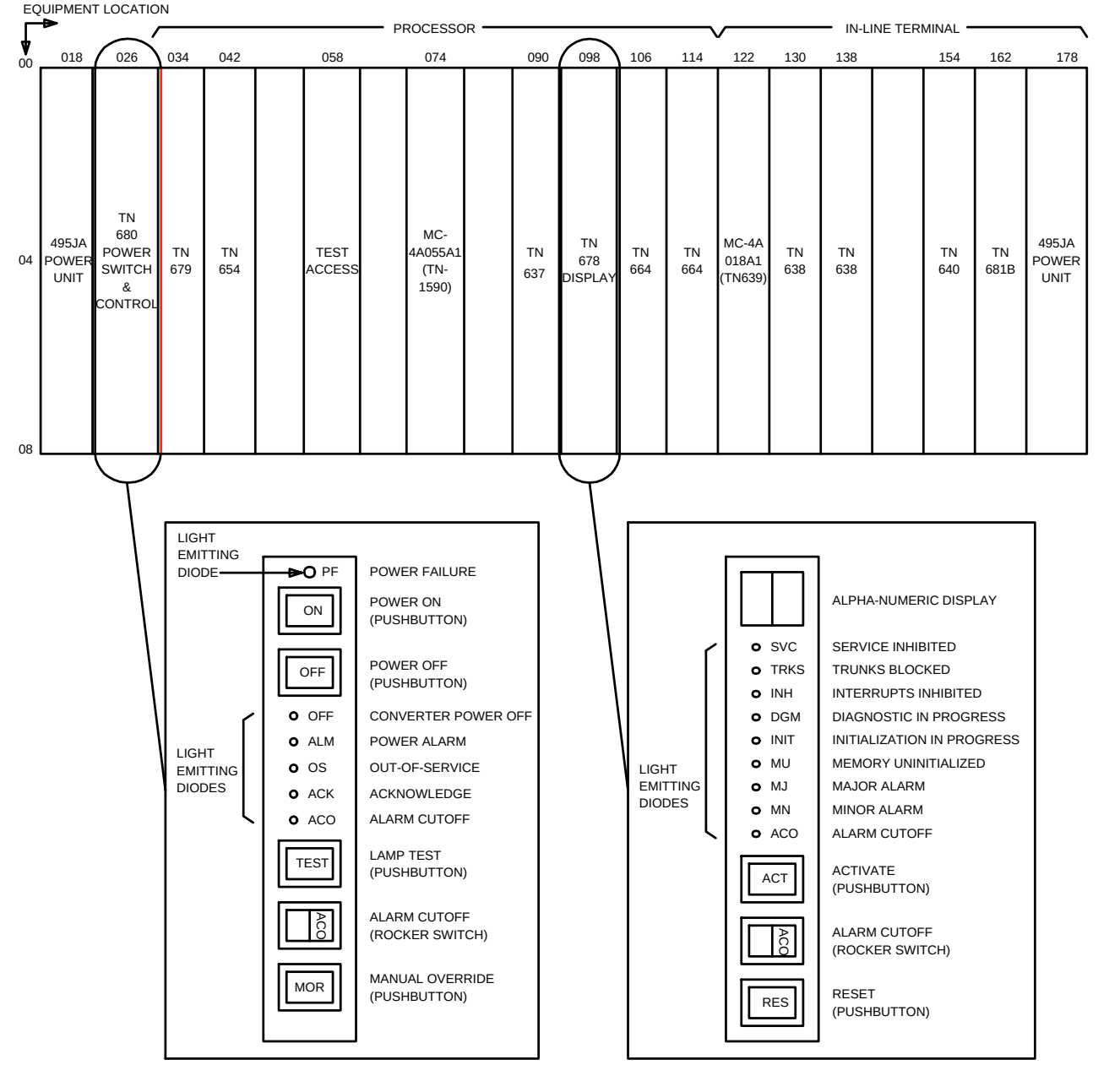


Figure 17. Processor and N-link Terminal Unit J4A017AL-1 — Equipment Identification

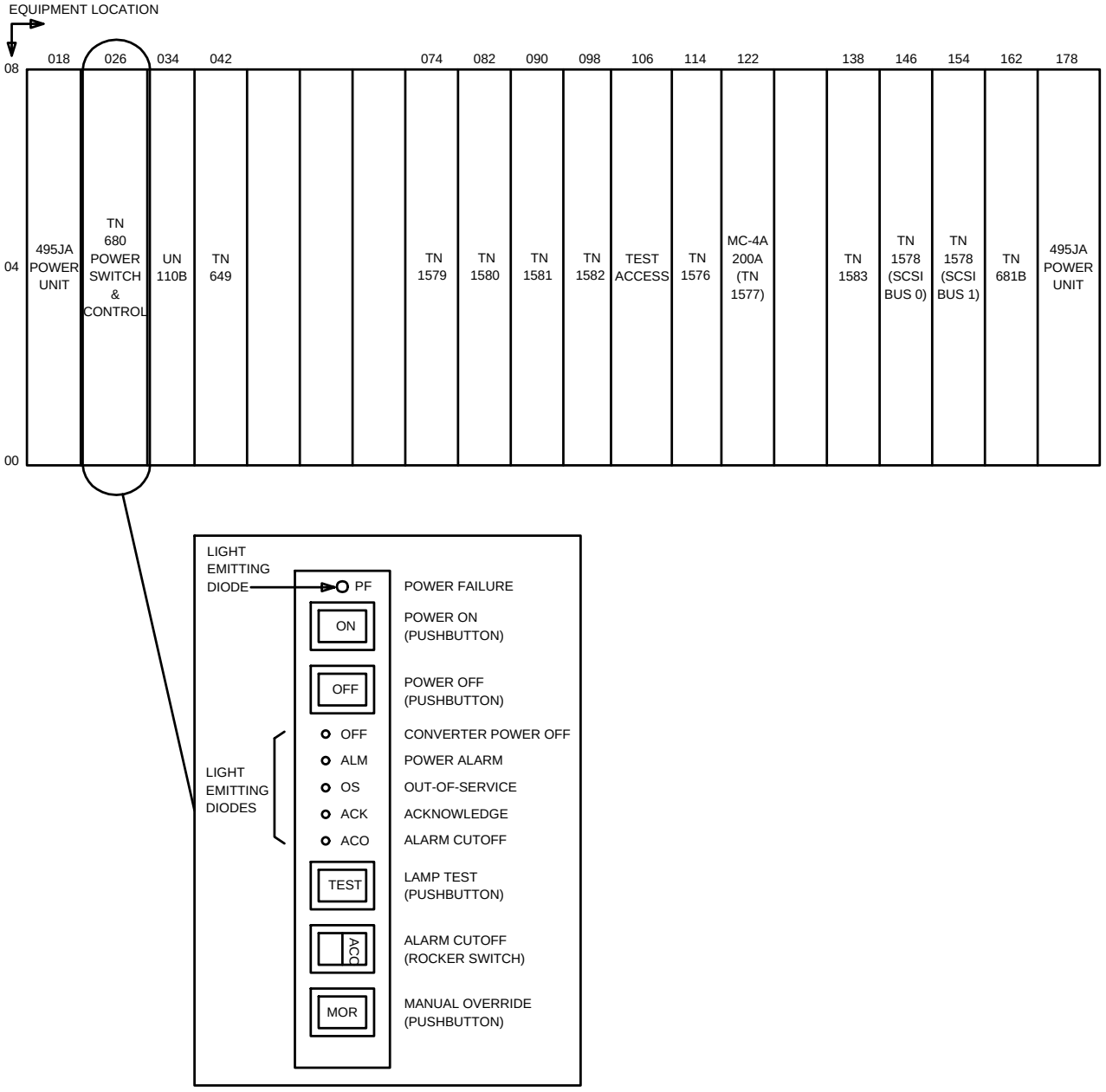


Figure 18. Data Storage Controller Unit J4A017AM-1 — Equipment Identification

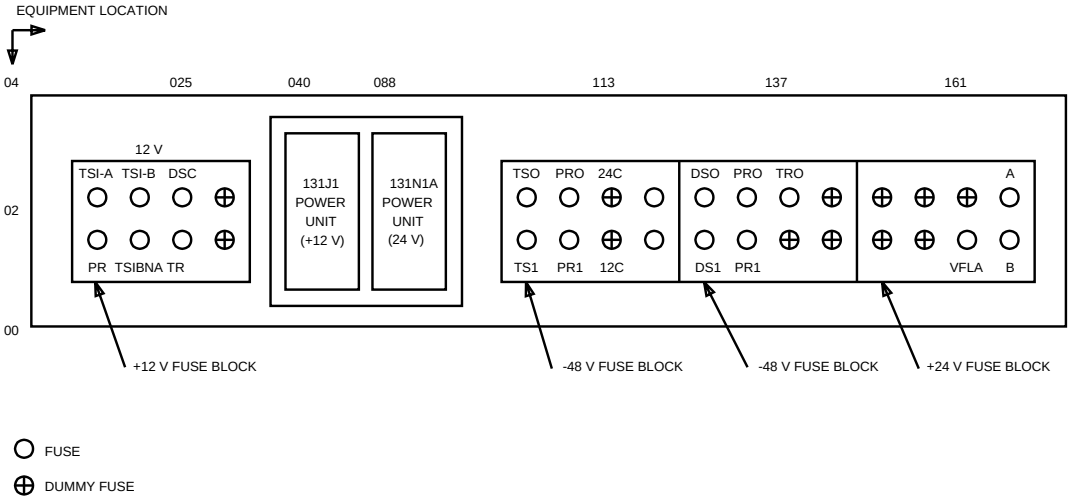


Figure 19. Fuse Panel J4A017GA-1 — Equipment Identification

Disk And Tone Receiver Frame (J4A017H-1)

3.39 The disk and tone receiver frame is used in the DSDC type NSCX using DSD8 or later generic program. The network services frame J4A017G-1 has facilities for 24 direct services dialing trunks. When more than 24 trunk capacity is required, additional units must be provided in the disk and tone receiver frame. The floppy disk unit and hard disk storage are also included in the disk and tone receiver frame. These units are a requirement for all DSD8 NSCXs. The disk and tone receiver frame will always be equipped with one floppy disk unit, hard disk units, and a fan unit. This frame would require one additional Tone Receiver (TR) for DSD 48 trunks and a second additional TR for DSD 72 trunks. The disk and tone receiver frame can be composed of (Figure 20):

- 0, 1, or 2 tone receiver units J4A017AF-1 or J4A017AF-40
- 1 floppy disk unit J4A017HC-1
- 1 hard disk unit J4A017HA-1
- 1 fan unit J5D003BE-1
- Fuse panel (J4A017HD-1)
- Filter unit J1A053AA-1, L100.

Tone Receiver Unit (J4A017AF-1 or J4A017AF-40)

3.40 The tone receiver unit (Figure 9) is discussed in paragraph 3.15.

Floppy Disk Unit (J4A017HC-1)

3.41 The floppy disk unit (Figure 21) consists of:

- Floppy drive
- Small Computer System Interface (SCSI) single-ended to differential-ended converter board
- SCSI single-ended disk drive controller.

Hard Disk Unit (J4A024AC-1)

3.42 The hard disk drive unit (Figure 22) consists of:

- Hard disk circuit pack (TN1972)
- Power control circuit pack (UN356).

Fan unit (J5D003BE-1)

3.43 The J5D003BE-1 fan unit provides the cooling required for the hard disk units.

Fuse Panel Unit (J4A017HD-1)

3.44 The fuse panel distributes the +5 V, +12 V and –48 V DC as required to the units. The fuse blocks are equipped with alarm type fuses. The fuse panel (Figure 23) is composed of:

- Four fuse blocks
- One 131J1 power unit
- One 131F1 power unit.

Filter Unit (J1A053AA-1, L100)

3.45 The filter unit is discussed in paragraph 3.17.

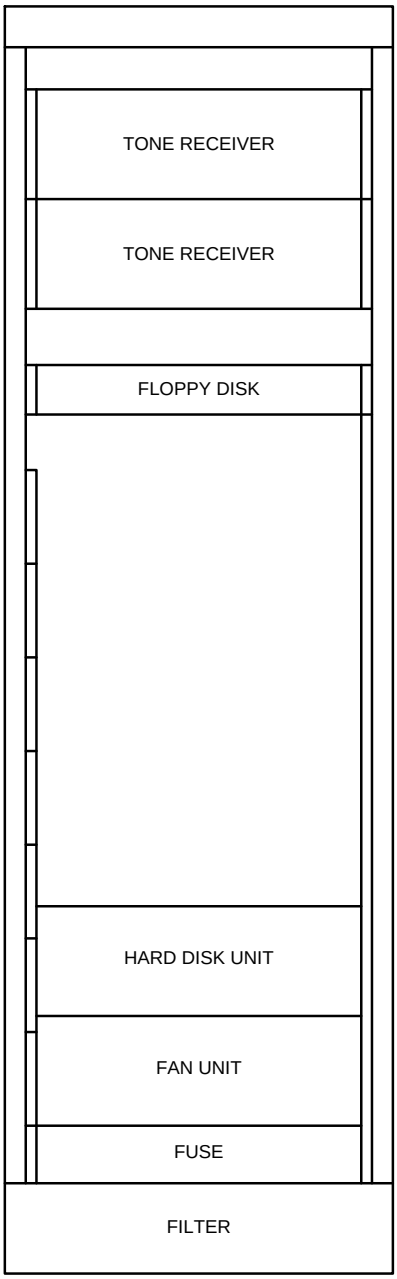


Figure 20. Disk and Tone Receiver Frame J4A017H-1 — DSD8 Equipment Identification

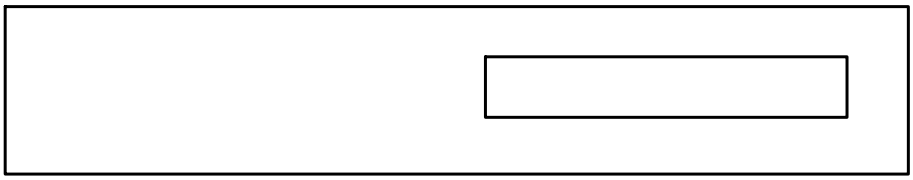


Figure 21. Floppy Disk Unit J4A017HC-1

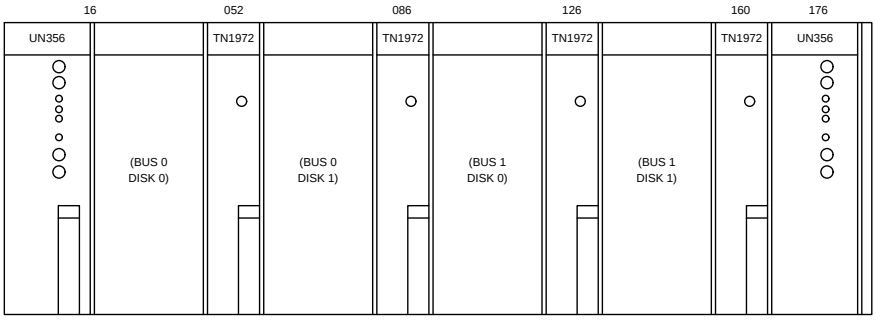


Figure 22. Hard Disk Unit J4A024AC-1

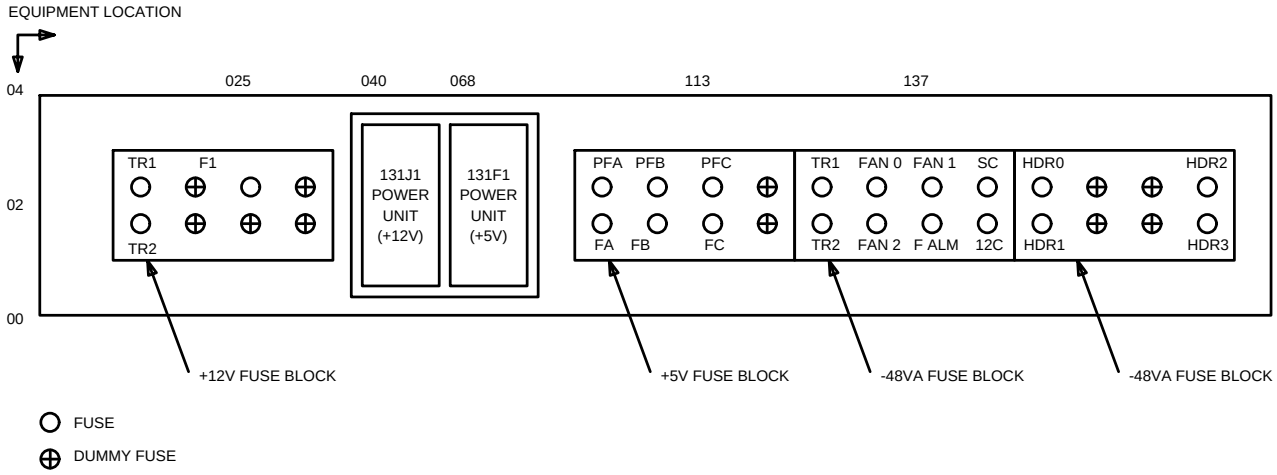


Figure 23. DSD8 Fuse Panel Unit J4A017HD-1 List 2

Moving Head Disk Frame (J1C131B-1)

3.46 The moving head disk frame (Figure 24) is required for the NSCX applications only. This frame provides disk data storage for recorded announcements and general data storage for the network services frame. The moving head disk frame is equipped as follows:

- Disk file inverter (ED-4C172-30)
- Inverter control unit (J1C131AA-1)
- Moving head disk drive (KS-22072, L1 or L2).

A. Disk File Inverter (ED-4C172-30)

3.47 The disk file inverter (Figure 24) consists of a microprocessor-controlled –48 V to 208 V AC inverter and a cooling fan. This unit interfaces with the moving head disk drive and the inverter control unit to provide an uninterrupted source of 208 V AC to the moving head disk drive.

B. Inverter Control Unit (J1C131AA-1)

3.48 The inverter control unit (Figure 25) consists of a control panel, –48 V fuse, and inverter control circuits. This unit is located below the disk file inverter. It is used to control the 208 V AC input power to the moving head disk drive.

C. Moving Head Disk Drive (KS-22072, L1 or L2)

3.49 The moving head disk drive (Figure 24) is a commercially manufactured 300-megabyte disk drive containing a removable disk pack (KS-22048, L1 or L2). This equipment is manufactured by Control Data Corporation (L1) (frame List 6) and Century Data Systems, Incorporated (L2) (frame List 7). The moving head disk drive is housed in a 1-foot 10-inch wide, 3-foot deep, and 3-foot high cabinet. The disk cabinet is placed in the lower portion of the moving head disk frame. The moving head disk drive is powered from a 208 V AC receptacle located on the rear of the inverter control unit. All disk drive operating voltages are derived internally. A circuit breaker/switch is provided on the disk drive to switch the 208 V AC input voltage on and off. Two connectorized cables (network services frame List 7 or List 8) provide the data and control interface with the network services frame. Further information on physical description, interfaces, functional description, power, and maintenance of the moving head disk drive is provided in AT&T 254-301-210 *AT&T 3B20D Model 1 Computer 300-Megabyte Disk Drive General Description*.

3.50 The KS-22048, L1 or L2 disk pack is a removable, 300-megabyte, multiple-disk, data storage module. The disk pack consists of ten oxide-coated disks stacked vertically between a top and bottom cover disk. The disk diameter is 14 inches. The ten disks provide 19 data storage surfaces and one surface for servo positioning and index/timing purposes.

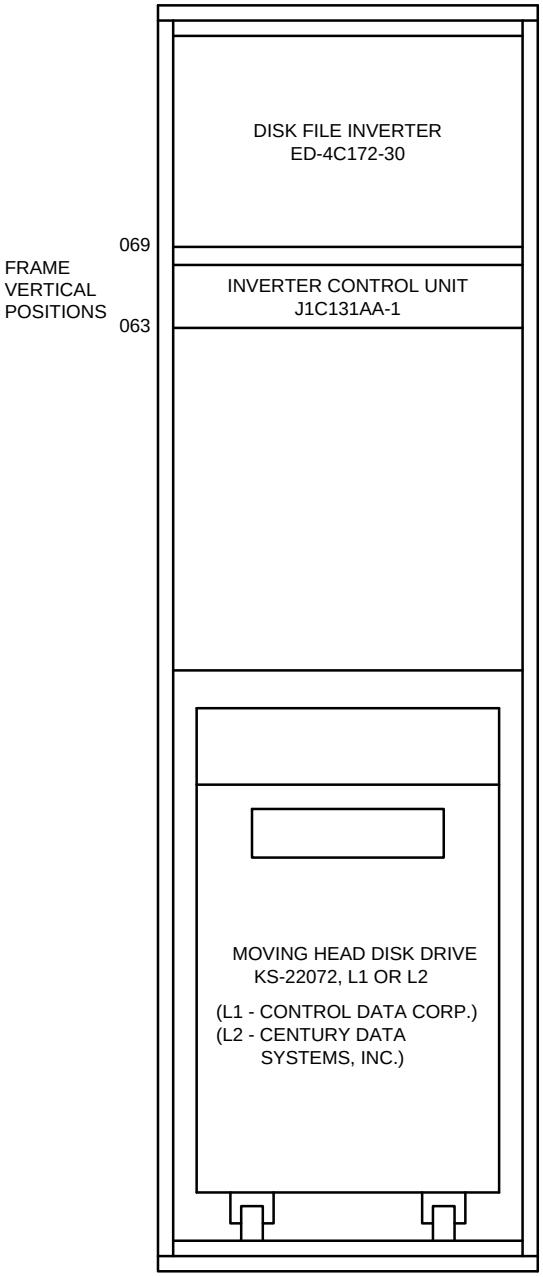


Figure 24. Moving Head Disk Frame J1C131B-1 — Equipment Identification

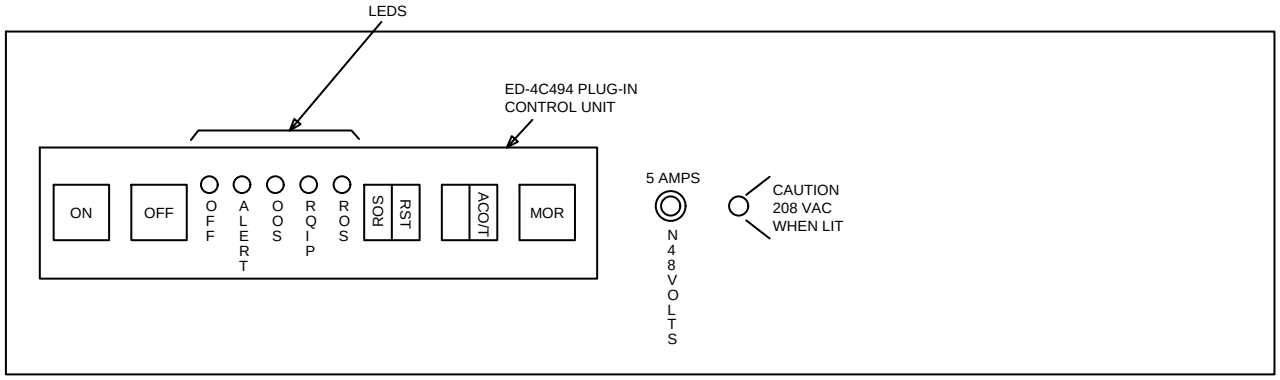


Figure 25. Inverter Control Unit J1C131AA-1 — Equipment Identification

Automatic Speech Recognition Cabinet (J4A017R-1)

3.51 The ASR cabinet (see Figure 26) consists of the following units:

- Fuse and Filter unit (J4A017RA-1)
- ASR units 0, 1, and 2 (J4A017RB-1)
- ASR Interface units 0, 1, and 2 (J4A017PC-2).

A. Fuse and Filter Unit

3.52 The Fuse and Filter unit (Figure 27) is composed of the DC-to-DC converter unit, fuse blocks, and filter capacitors. The 131F1 DC-to-DC converter unit converts the -48 V DC supply voltage to +5 V DC necessary for the operation of the ASR Interface unit. The 131J1 DC-to-DC converter unit converts the -48 V DC supply voltage to +12 V DC. The fuse blocks provide the fusing for the -48 V, +12 V, and +5 V supply voltage to the equipment in the ASR cabinet. The filter capacitors filter the supply voltage to lessen the variation in the supply voltage.

B. Automatic Speech Recognition Units

3.53 The ASR units (Figure 28) collect, decode, and report spoken words. These decoded words are passed back to the TR unit associated with that ASR unit. The ASR cabinet is equipped with three ASR units. Each ASR unit directly interfaces with a single TR unit and supports 24 channels of speech recognition.

C. Automatic Speech Recognition Interface Units

3.54 The ASR Interface units (Figure 28) contain both floppy and hard disk drives. The hard drive stores the ASR unit software and recognition codes. The ASR cabinet is equipped with three ASR interface units.

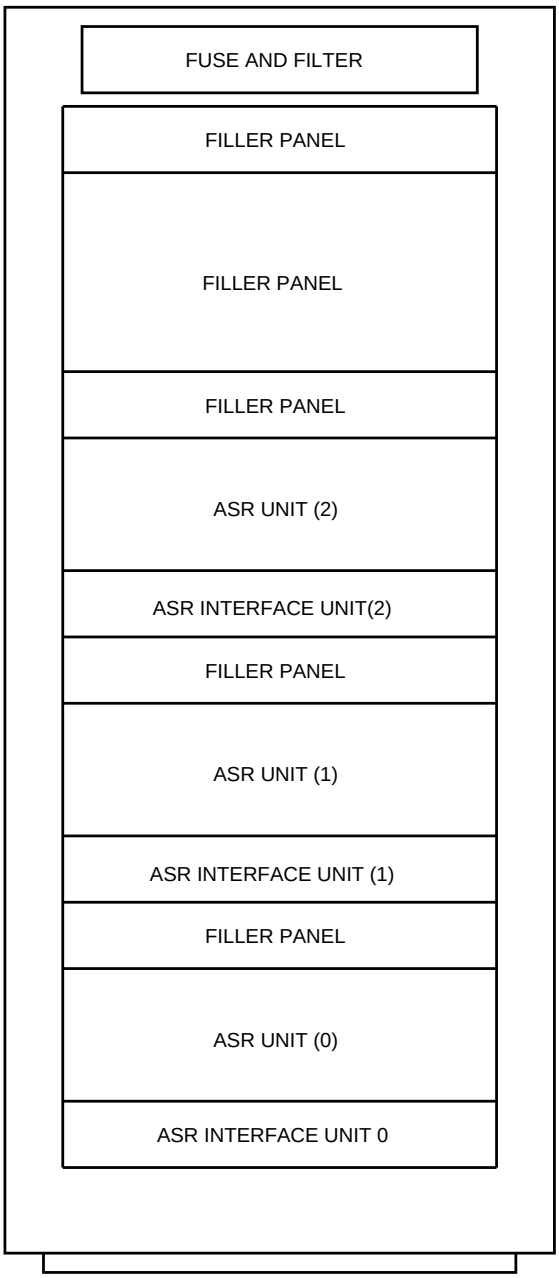


Figure 26. Automatic Speech Recognition Cabinet

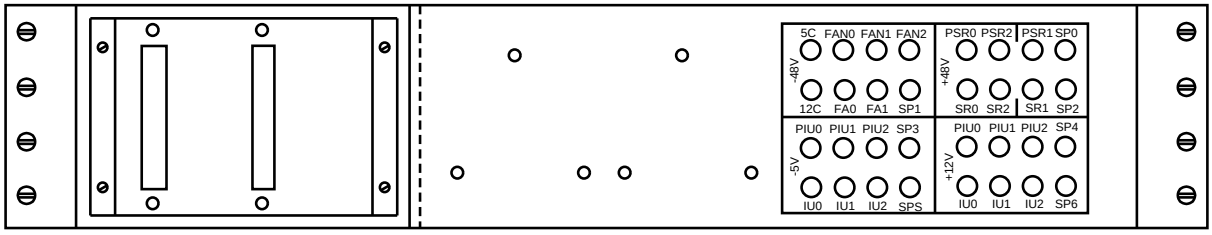


Figure 27. Fuse Panel J4a017RA-1 — Equipment Identification

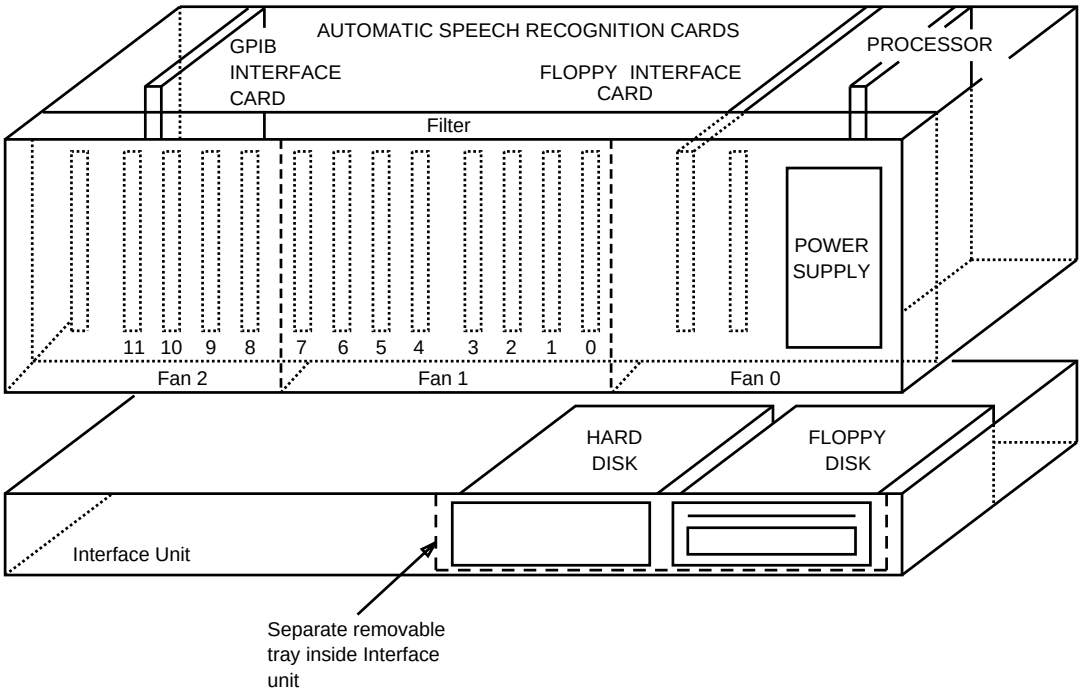


Figure 28. ASR Unit and ASR Interface Unit

4. Functional Description

Introduction

4.01 This part provides a functional description of the NSCX frames and units housed within the frames. The following subjects are included in this section:

- General description of NSCX functions
- NSCX configurations
- Functional description of NSCX frames and units.

4.02 Functional descriptions of NSCX equipment is based on the following schematic drawings:

- SD-4A112-01 - Network services frame J4A017A-1
- SD-4A113-01 - Processor unit
- SD-4A114-01 - Time slot interchange unit
- SD-4A115-01 - Data storage unit
- SD-4A116-01 - Tone receiver unit
- SD-4A117-01 - Audio bridge frame
- SD-4A118-01 - Audio bridge unit
- SD-4A124-01 - NSCX application schematic
- SD-4A139-01 - Network services frame J4A017G-1 (basic for DSD8 generic)
- SD-4A140-01 - Processor unit J4A017AL-1 (DSD8 generic or later)
- SD-4A141-01 - Data storage controller
- SD-4A143-01 - Floppy disk unit
- SD-4A144-01 - Disk and tone receiver frame
- SD-4A168-01 - 2 Gbyte hard disk unit (DSD8 generic or later)
- SD-4A200-01 - ASR cabinet
- SD-4A201-01 - ASR unit
- SD-4A179-01 - ASR Interface Unit
- SD-5D019-01 - Fan Unit.

4.03 If this practice is to be used with equipment or apparatus reflecting later issues of the schematic drawings, reference should be made to the appropriate schematic drawings and circuit descriptions. This will enable the user to determine the extent of changes and the manner in which this practice may be affected.

General

4.04 The NSCX provides teleconferencing features and Direct Services Dialing Capability (DSDC) features for use with the toll network. The NSCX is entirely digital, and the hardware units within the NSCX are simplex. Many NSCXs may be installed in various host offices to provide a high availability of services nationwide.

4.05 The teleconferencing feature provides a bridging service for callers using the Direct Distance Dialing (DDD) and Circuit Switched Digital Capability (CSDC) networks. This service provides a caller with voice-only or voice and analog graphics teleconferencing on a direct-dialed add-on basis or by using the meet-me feature. A subscriber can also use this service with reservation and operator-assisted options. The teleconferencing feature also provides the caller (customer or operator) an interactive capability for establishing and controlling conferences.

4.06 The DSDC feature provides an interactive interface with callers via reception of dialed tones or spoken words (if equipped with ASR) and transmission of recorded announcements. Announcements may be standard recorded announcements, alert tones, or instructional prompts to the caller. The first DSDC service to use the NSCX was the Advance 800 Service. Two examples of these NSCX services are Call Prompter and Courtesy Response.

Direct Services Dialing Capability

4.07 The DSDC consists of sets of network features that can be summoned to provide service offerings. The DSDC architecture contains two key elements. These are an Network Control Point (NCP) and an Action Control Point (ACP). The NCP is a processor with an associated data base which contains instructions on handling calls for specific services. The ACP is a switching system that processes calls after requesting and receiving instructions from the NCP [via the Common Channel Interoffice Signaling (CCIS) network]. The ACP must be a Stored Program-Controlled System (SPCS) with access to the CCIS network. One or more NSCXs, configured to provide DSDC services, are collocated with the ACP switching system. The ACP serves as the host for the collocated NSCXs. When a DSDC call requires interaction with the service subscriber, the NSCX is used by the host.

4.08 The NSCX provides a sophisticated interactive interface with DSDC service subscribers via reception of dialed tones or spoken words (if equipped with ASR) and/or transmission of recorded announcements (via DS1 intraoffice digital trunks). Announcements may be standard recorded announcements, alert tones, or instructional prompts to the service subscriber. Many DSDC calls may require only routing instructions be obtained from the service subscribers' data base at the NCP to enable the ACP to properly route these calls.

Teleconferencing

4.09 Both types of teleconferencing NSCXs (voice-only and voice and analog graphics) are collocated with a host SPCS. Each teleconferencing NSCX is programmed to provide subscriber control for establishing conferences. Conferences may range in size from 3 to 59 voice-only conference legs and from 3 to 60 data bridge conference legs. At least one audio bridge port is reserved for operator access. Each teleconferencing NSCX can support many active conferences simultaneously. Voice teleconferencing NSCXs may be used to bridge conference legs via the voice band DDD network.

Network Services Complex Configurations

4.10 Figure 29 shows the functional interface to the host SPCS and the NSCX frame configurations required to implement the DSDC feature generic DSD8 or later.
This DSDC NSCX consists of:

- Network services frame J4A017G-1
- Disk and tone receiver frame J4A017H-1
- Three DS1 lines (24 channels each - total of 72 trunks)
- ASR Cabinet (if equipped with ASR) J41017R-1.

4.11 The voice-only or voice and analog graphics teleconferencing NSCX (Figure 30) consists of a network services frame, a moving head disk frame, and an audio bridge frame. For this application, the audio bridge frame is equipped with two 64-port audio bridge units and one tone receiver unit (one identical tone receiver unit is always equipped in the network services frame). Also, up to five DS1 trunks (120 digital channels) are required to interface the host SPCS.

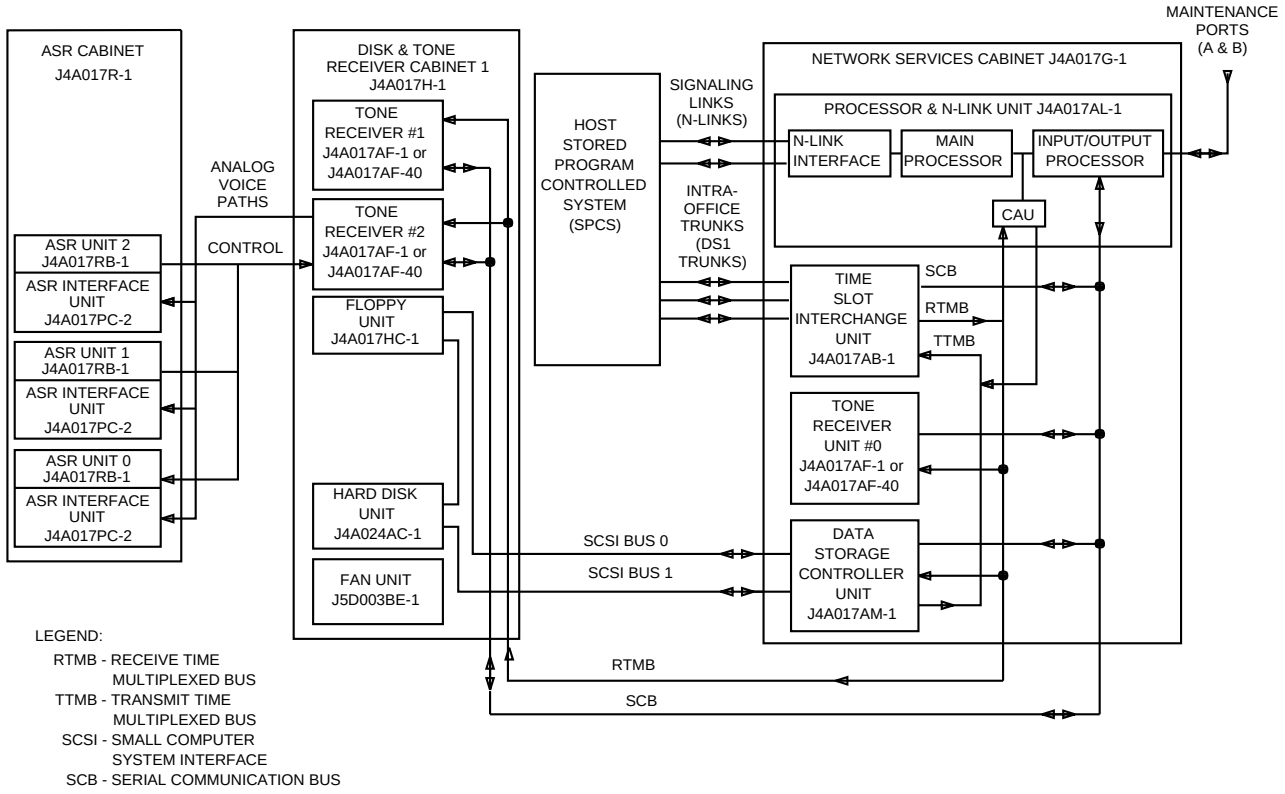


Figure 29. Direct Services Dialing Capability NSCX — Functional Block Diagram DSD8 or Later Generic

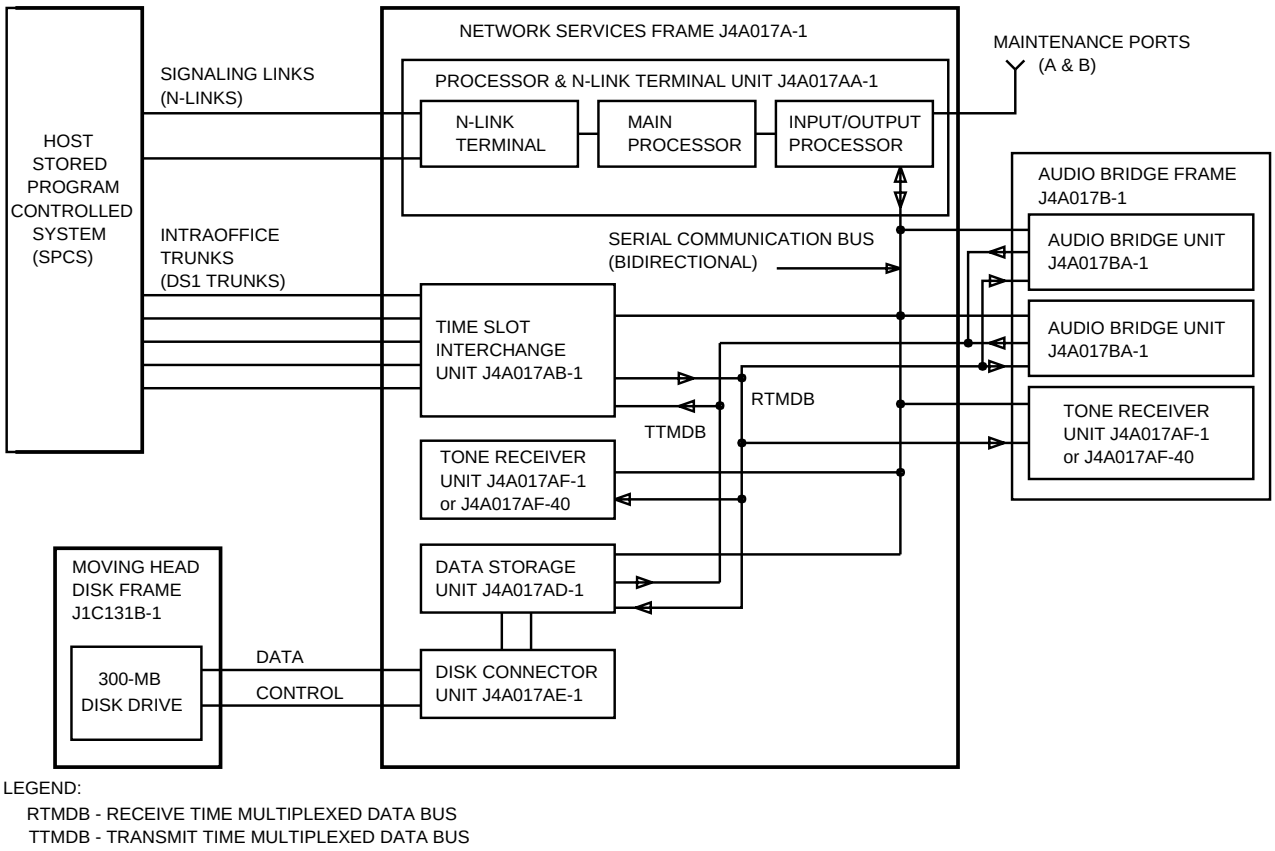


Figure 30. Voice-Only or Voice and Analog Graphics Teleconferencing Network Services Complex — Functional Block Diagram

Network Services Complex Bus Configurations

4.12 The Network Services (NS) frame provides interface connections between units within the frame, to other NSCX frames, and to the host SPCS office.

4.13 The various units in the NSCX frames are interconnected via a common bus and configuration data leads. These interconnections provide the timing, control, and data buses between the units within the network services frame, audio bridge frame, direct services dialing frame, and the disk and tone receiver frame. The common bus consists of the following bus groups:

- Timing bus
- Receive Time Multiplexed Data Bus (RTMBD)
- Transmit Time Multiplexed Data Bus (TTMBD)
- Serial Communication Bus (SCB).

4.14 All NSCX master timing and synchronization signals (except N-link signaling) are supplied by the NS frame time-slot interchange unit via the timing bus. This bus includes a 16.384-MHz clock which is synchronized to one of the DS1 trunks to maintain synchronization with the host switching office.

4.15 The NS frame time-slot interchange unit distributes caller data to the other units over a 256 time-slot data bus called the RTMDB. The other units transmit caller data to the time-slot interchange unit over a similar bus called the TTMDB. These two buses provide sufficient internal data transmission capacity to handle all the unit-to-unit data transfer needs within the NSCX. The time slots on the RTMDB and TTMDB are uniquely assigned to the appropriate NSCX units.

4.16 The NS frame main processor communicates with other NSCX units over a serial, bidirectional, party-line bus called the serial communication bus. This bus consists of a data signal and an enable signal. The NS frame processor and N-link terminal unit IOP is the master of this bus and controls all bus activities. The enable signal indicates the beginning and end of each message transmission. Requests to transmit on the serial communication bus are provided by dedicated interrupt leads from each unit to the processor and N-link terminal unit IOP.

4.17 Configuration data leads are connected from the NS frame processor and N-link terminal unit to each of the other NSCX units. These leads enable the main processor to control transmit access to the TTMDB and serial communication bus during fault conditions.

4.18 Individual unit circuit pack interface connections are discussed in the functional description of each unit.

Network Services Complex Frames (SD-4A112-01 [J4A017A-1])

4.19 The J4A017A-1 NS frame houses five units that perform specific NSCX functions. This frame is used in TC network services applications. The units are (Figure 31):

- Processor and N-link terminal unit (SD-4A113-01 [J4A017AA-1])
- Time slot interchange unit (SD-4A114-01 [J4A017AB-1])
- Data storage unit (SD-4A115-01 [J4A017AD-1])
- Tone receiver unit (SD-4A116-01 [J4A017AF-1 or J4A017AF-40])
- Maintenance interface unit (J4A017AC-1).

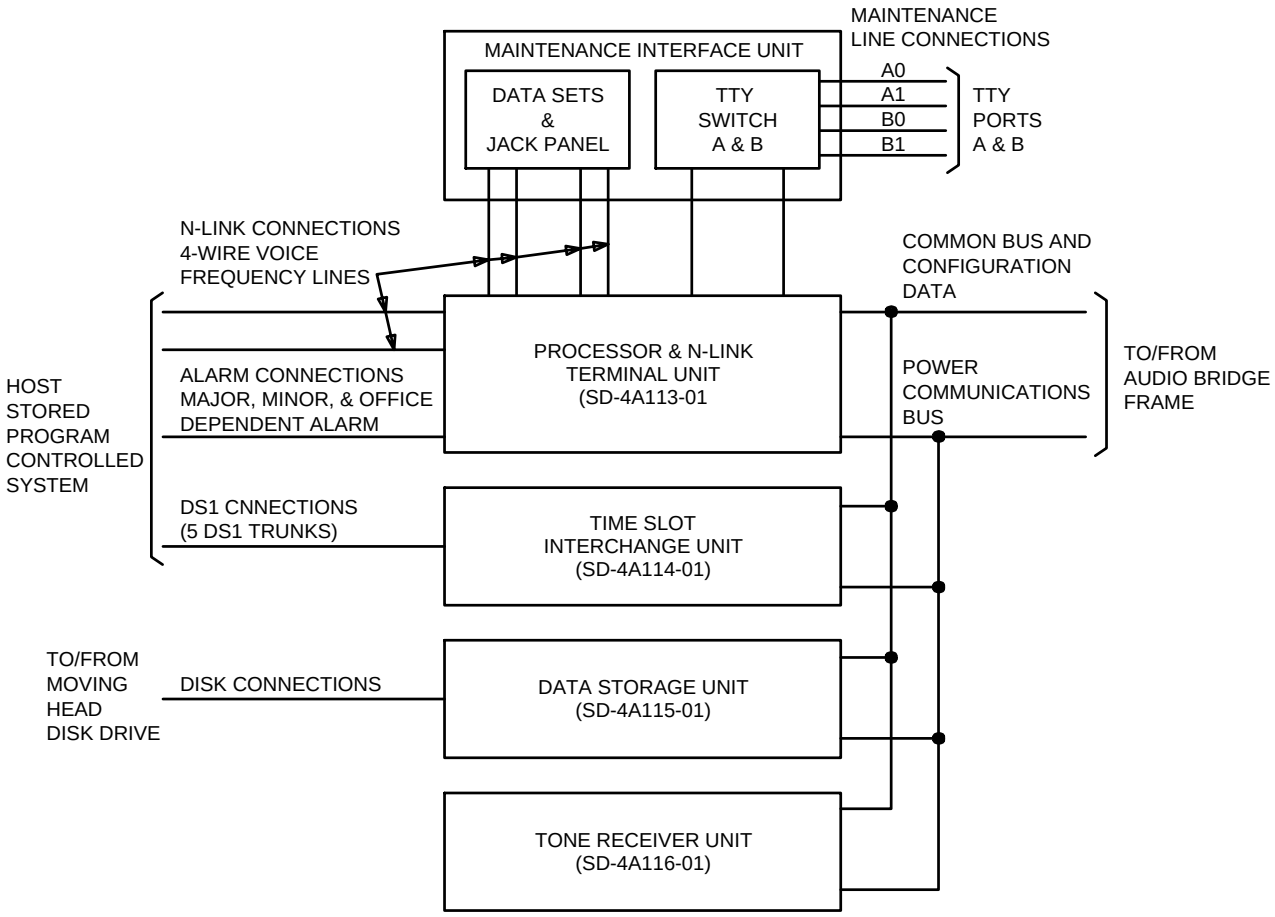


Figure 31. Network Services Frame — Functional Block Diagram (SD-4A112-01 [J4A017A-1])

A. Processor and N-link Terminal Unit (SD-4A113-01)

General

4.20 The processor and N-link terminal unit provides overall control of the NSCX. It performs call processing, maintenance, fault recovery, diagnostics, and audits for the NSCX. The various modules in the processor and N-link terminal unit are interconnected via a parallel address, data, and control bus called the system bus. The modules are designed with bus master circuitry and/or bus slave circuitry. Modules designed with bus master circuitry may obtain use of the bus and initiate data transfers on it. Modules designed with bus slave circuitry are the object of data transfers only. The main processor, IOP, and memory refresh controller are the only modules on the system bus designed with bus master circuitry. Modules on the bus designed with slave bus circuitry include the main memory, interrupt controllers, timers, N-link terminal, main memory protection circuit, unit cutoff registers, display drivers, and other maintenance registers.

4.21 The processor and N-link terminal unit is divided into eight functional areas (Figure 32):

- Main processor (TN637)
- Main memory (TN641)
- Input/output processor (TN643 and TN679)
- Processor display board (TN678)
- N-link terminal unit (TN640, two TN638, and TN639)
- Link processor (TN639)
- Serial link interface (TN638)
- Voice frequency link access (TN640).

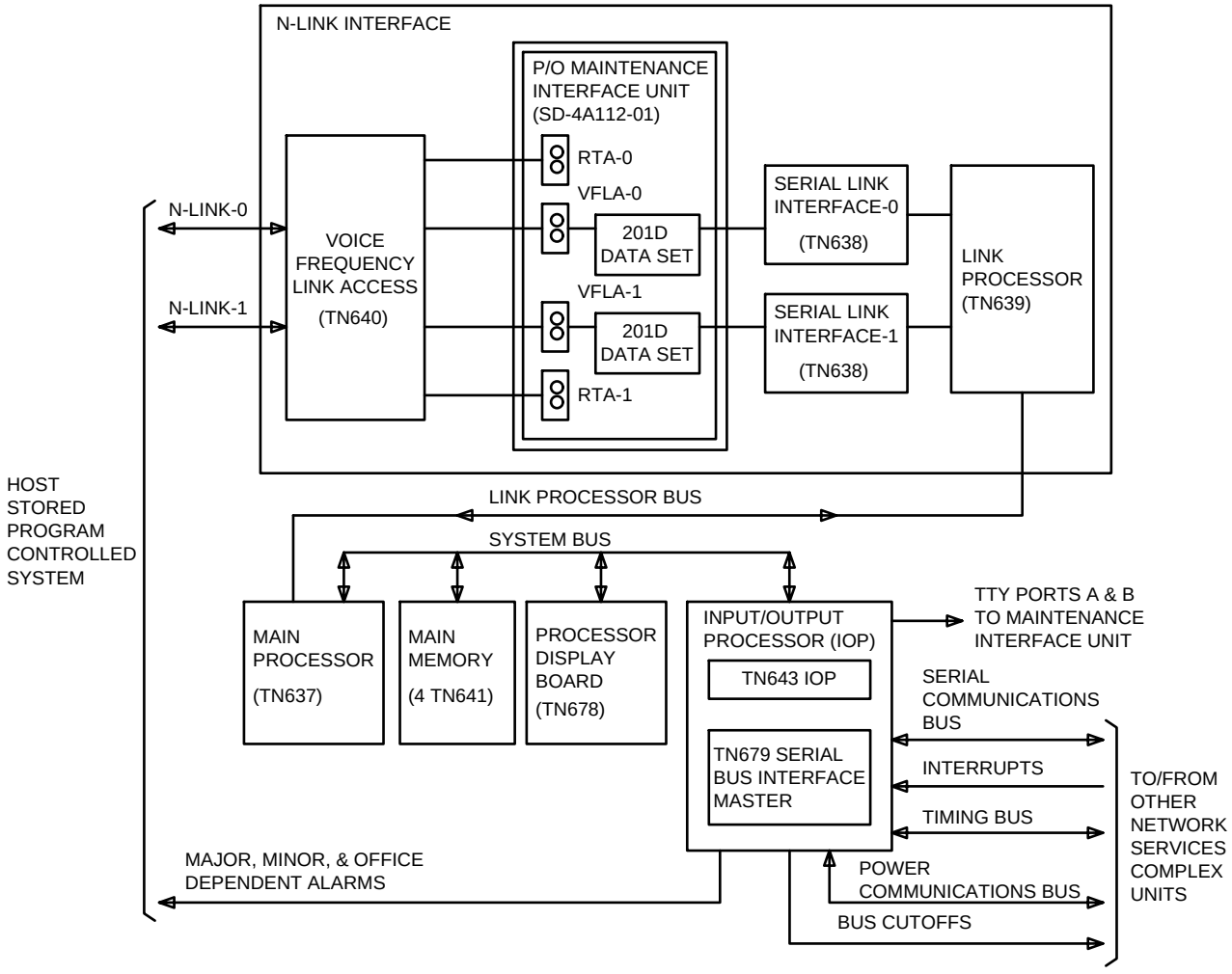


Figure 32. Processor and N-Link Terminal Unit — Functional Block Diagram (SD-4A113-01)

Main Processor (TN637)

4.22 The principal function of the main processor is to serve as the main NSCX processor. All operational, maintenance, audit, and diagnostic work for the NSCX is either performed or controlled by the main processor. The main processor's program is stored in main memory. A backup copy of the program is stored on the moving head disk unit. The program is loaded into main memory by the IOP during system reinitialization.

4.23 The main processor is one of three bus master modules which can control the system bus. The processor is contained on a single circuit pack (TN637) along with several peripheral devices used by the main processor. These devices are bus slave modules on the system bus and can therefore be accessed by the main processor and the IOP. These devices include various status and error registers, interrupt controllers, timers, memory protection circuits, N-link terminal interface and maintenance ports.

4.24 The main processor consists of a 16-bit microprocessor and associated matching clock and system bus interface circuits. The main processor operation and/or its access to the system bus are controlled by two bits in the IOP status and control register. These features enable the IOP to control the NSCX during initialization and generic software loading routines.

Main Memory (TN641)

4.25 The main memory consists of four TN641 circuit packs which reside on the system bus. The system bus address range allows up to 1 megabyte of memory.

4.26 Each TN641 circuit pack is divided into two 128 KB blocks which can be assigned as any of the eight 128 KB blocks in the address space via backplane straps. Each block consists of two 64 KB banks. One bank interfaces with the lower half of the system data bus (bits 0 through 7). The other bank interfaces with the upper half of the system data bus (8 through 15). Any consecutive bytes can be accessed as a 16-bit word. Words aligned with even address boundaries can be accessed in one bus cycle. Words aligned on odd address boundaries require two bus cycles. Six additional memory bits for each 2-byte word are used to store an error detection and correction code calculated over each 16-bit word. Uncorrectable errors result in an interrupt of the main processor so that fault recovery programs can be invoked.

4.27 The main memory fabric is implemented using dynamic Random Access Memory (RAM) integrated circuits which require a periodic refresh cycle. A refresh command is periodically sent to each memory circuit pack by the memory refresh controller. The operating program and data used by the main processor is stored in the main memory. Since this memory is volatile, a loss of power to the unit will destroy the contents of the memory. Therefore, during power-up or bootstrap, the memory must be loaded from disk. This operation is performed by the IOP which contains firmware stored in Erasable Programmable Read-Only Memory (EPROM). Programs are loaded from disk only during NSCX initialization and fault recovery procedures. Paging from disk is not done during normal operation.

Input/Output Processor (TN643 and TN679)

4.28 The IOP consists of two circuit packs (TN643 and TN679). Circuit pack TN643 contains the circuitry for IOP functions. Circuit pack TN679 contains the circuitry for the serial bus interface master. The IOP functions mainly as a direct memory access controller for all units and TTY port input/output operations. Since the IOP program is contained in EPROM, the program is also used for bootstrap and other recovery and utility functions. The IOP is a complete processing system using a single 16-bit 8086 microprocessor. The IOP also contains RAM and EPROM, system bus and serial communications bus interfaces, timers, TTY ports, and other miscellaneous hardware.

4.29 The 8086 microprocessor interfaces with the system bus and an internal IOP bus, called the resident bus. The resident bus connects all of the local IOP peripheral devices together. These devices include the serial communications bus interface, the IOP memory, and two TTY ports. The IOP controls all serial communications bus activity. The IOP memory consists of 64 KB of EPROM and 8 KB of RAM. The IOP program is contained in the EPROM. Addresses generated by the IOP to this EPROM are mapped from the upper 64 K main memory address spectrum to the IOP resident bus. The RAM serves as a data storage facility for the IOP. The RAM is comprised of static devices which do not require periodic refreshing to maintain the data contents. Addresses generated by the IOP to this RAM are mapped from the lowest 8 K of the main memory address spectrum to the IOP resident bus.

4.30 Two ASCII start-stop TTY ports reside on the IOP resident bus. Each port consists of a Universal Asynchronous Receive-Transmit (UART), RS-232C drivers and receivers for both data and modem control, and baud rate generation hardware. During normal NSCX operation, the two TTY ports are set to operate in the half-duplex mode at 1200 baud. However, TTY port B can be reconfigured by the user to operate at the standard rates of 1200, 2400, 4800, or 9600 baud.

4.31 The two UARTs provide TTY access to the NSCX via two key switches (A and B) and four RS- 232C connectors (A0, A1, B0, and B1) located on the maintenance interface unit. Switch A transfers control only between the A0 and A1 connectors. Output data may be simultaneously monitored via both connectors (A0 and A1). Switch B transfers all port functions between connectors B0 and B1. These two TTY ports provide the primary control and display facility for the NSCX. They may be interfaced to a dedicated or shared data terminal arrangement in the host office and to a remote operations, administration, and maintenance facility. The local data terminal equipment may include a keyboard/display terminal, printer, and flexible diskette data storage/playback equipment. When the main processor is in the maintenance mode, only TTY port A is active.

Processor Display Board (TN678)

4.32 The processor display board is a TN678 circuit pack which contains a control and display panel. The processor and display board resides on the system bus to provide main processor and IOP access to several error, maintenance control, and display registers. These circuits provide limited control and display functions essential to the bootstrapping of the NSCX. The display section provides a summary of main processor and NSCX status and error conditions. The alphanumeric display is used to indicate a failing test state or level of initialization. These displays are designed to give an immediate indication of NSCX status and error conditions and to aid in repairing the NSCX when TTY ports are inoperative.

4.33 When depressed simultaneously, the activate and reset switches will force a complete NSCX reinitialization. A rocker switch is also provided to disable the three NSCX alarms (major, minor, and office-dependent alarm) to the host office. An 8-bit error register controls the major and minor alarm relays. The office-dependent alarm is activated by either a major or minor alarm condition. The office-dependent alarm output may be used by the host office to automatically generate an NSCX identification message. Four bits of the error register drive the minor alarm relay and the remaining four error bits drive the major alarm relay. The major alarm relay can also be directly activated by a power alarm signal output from the processor and N-link terminal unit power control circuit pack (TN680).

4.34 Other circuits contained in the processor display board include several maintenance control registers and control logic for operation of the power communications bus. A 24-bit register is provided to trap the system bus address during error conditions.

A 16-bit maintenance register provides various control functions along with eight read-only strap bits used by the bootstrap and other programs. Two 24-bit cutoff registers enable the main processor to control access of each unit to the TTMDB and serial communications bus.

N-Link Terminal Unit (TN640, TN638, and TN639)

4.35 The N-link terminal unit consists of four circuit packs (TN640, two TN638, and TN639) and two 201D-L1B data sets. These circuits provide two autonomous N-links between the main processor and the host SPCS. The N-links function as a communications channel for NSCX signaling and other call-related data.

4.36 The N-link communications are implemented using the N-link protocol. The Voice Frequency Link (VFL) access circuit (TN640) and modems handle the first-level protocol. This protocol defines how individual bits are represented by electrical signals. The second level protocol is handled by the link processor (TN639) and the two serial link interface circuits (TN638). This protocol defines how the individual bits handled by the first level protocol are grouped into larger units of information. The third-level protocol is handled by the link processor (TN639). This protocol assembles the large units of information into complete N-link messages. The N-link protocols above the third level are handled by the main processor N-link interface program. The various N-link messages are routed by function to the appropriate NSCX program.

Link Processor (TN639)

4.37 The link processor is an 8-bit microprocessor-based circuit pack with an 8-bit parallel data bus (link processor bus) and a 16-bit address bus (64 KB of address space). It includes a RAM, EPROM, interrupt controller, timers, UART, and an extended bus interface. It also includes initialization, error, and status registers. All link processor devices reside on the link processor bus. The link processor bus interfaces with the system bus.

4.38 The link processor provides up to 16 KB of EPROM and up to 48 KB of usable RAM. The total memory is limited to 56 KB. The data contents of the dynamic RAM is maintained by a periodic refresh cycle. Link processor firmware contained in the EPROM is an interrupt-driven operating system.

Serial Link Interface (TN638)

4.39 A serial link interface circuit pack performs the parallel to serial, serial to parallel, and 8-bit Cyclic Redundancy Check (CRC) generation and checking for each VFL. It also provides parallel input and output ports for status and control leads to the VFL access circuit and associated modem. The link processor controls each of the two serial link interface circuits. Data is passed to and from the link processor via several registers. These registers include a 3-byte transmit register, a 3-byte receive register, a modem control register, a modem status register, and an error source register. A link sequencer is also provided in each circuit to sequence the serial transmitter and receiver. A 2-byte receive synchronization register and comparator are also included in each circuit to detect Synchronization Signal Units (SYU) and synchronize the link sequencer with the far-end.

Voice Frequency Link Access (TN640)

4.40 The VFL access circuit is located between two modems and the two VFLs. It contains relays, attenuators, and amplifiers to provide loopback, test access, and proper signal levels on each VFL. It is controlled and monitored by the serial link interface modem status and control registers. The two 4-wire VFLs (N-links) are connected to two similar terminal units in the host office.

B. Time Slot Interchange Unit (SD-4A114-01 [J4A017AB-1])

General

4.41 The time slot interchange unit interfaces with the host office DS1 intraoffice trunks and performs the necessary switching functions to connect DS1 channels to the appropriate NSCX units. All NSCX timing and synchronization signals are also provided by this unit. Unlike all other NSCX units, the time slot interchange unit does not contain a microprocessor. However, the unit operates autonomously via the use of sequential timing signals. The NSCX main processor provides all necessary maintenance and channel connect/disconnect control information via the serial communications bus. The time slot interchange unit is divided into three functional areas (Figure 33):

- DS1 interface (TN674, TN675, or TN676)
- Time slot interchange circuit (TN632)
- Timing and control circuits (TN633 and TN635).

DS1 Interface (TN674, TN675, or TN676)

4.42 The DS1 interface consists of up to five circuit packs. Three circuit pack types are designed to interface different DS1 intraoffice trunk lengths:

- TN674 — 0 to 220 feet
- TN675 — 220 to 440 feet
- TN676 — 440 to 655 feet.

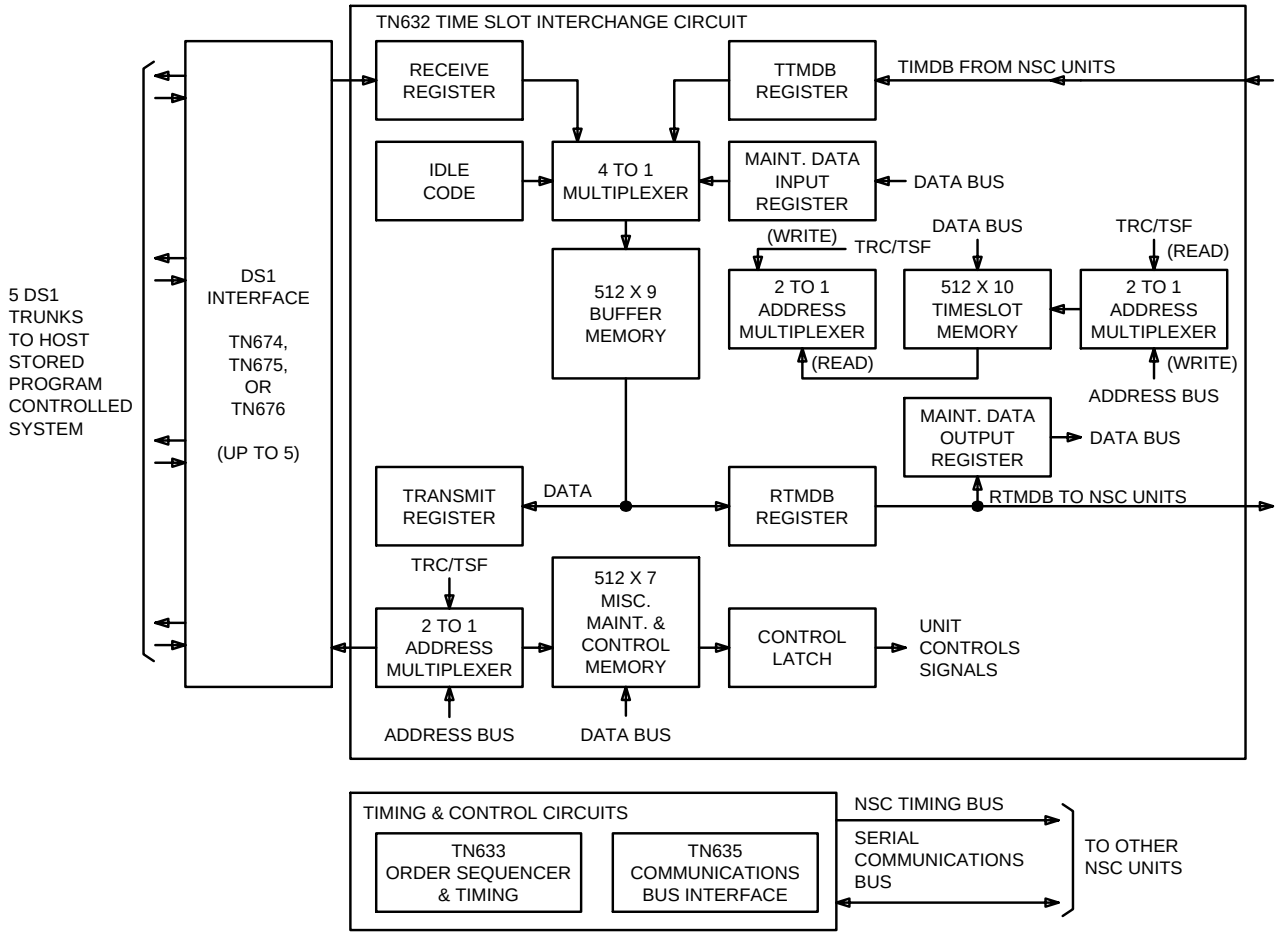
4.43 The time slot interchange unit is equipped with up to three DS1 interface circuit packs for the DSDC application. The teleconferencing application requires five DS1 interface circuit packs. Each DS1 interface circuit pack accommodates one DS1 trunk (24 channels) using the standard DS1 serial format. Since all NSCX signaling is handled via the N-link, signaling information normally contained in the DS1 format is not used.

Time Slot Interchange Circuit (TN632)

4.44 The DS1 interface terminates the incoming DS1 trunks, extracts timing and synchronization information, provides slip compensation, and converts the serial data into a parallel format. In the receiving direction, the five digroups (DS1 trunks) are multiplexed into 128 time slots (120 active and 8 maintenance) and routed to the TN632 time slot interchange circuit. The time slot interchange circuit provides synchronous time slot interchange switching to connect the DS1 interface to the appropriate NSCX units. In the transmitting direction, the DS1 interface converts the parallel transmit data from the TN632 time slot interchange circuit format (128 time slots) into five 24 channel (DS1 trunk) digroups. The five transmit digroups are then individually formatted and transmitted over the outgoing DS1 trunks along with synchronization information.

Timing and Control Circuits (TN633 and TN635)

4.45 The TN633 circuit pack generates the timing and synchronization signals required by each NSCX unit, including the time slot interchange unit. The TN635 communications bus interface circuit pack provides the control interface to the main processor.



LEGEND:
NSC - NETWORK SERVICES COMPLEX
RTMDB - RECEIVE TIME MULTIPLEXED DATA BUS
TRC - TWISTED RING COUNTER
TSC - TIME SLOT COUNT
TTMDB - TRANSMIT TIME MULTIPLEXED DATA BUS

Figure 33. Time Slot Interchange Unit — Functional Block Diagram (SD-4A114-01)

C. Data Storage Unit (SD-4A115-01 [J4A017AD-1])

General

4.46 The data storage unit, in conjunction with a 300-MB disk drive, provides disk-based recorded announcements and general data storage for the NSCX. Announcements are output in Pulse Code Modulation (PCM) format over TTMDB time slots assigned for use by the data storage unit. Up to 24 announcements may be output (played) simultaneously. Up to 2000 unique announcements may be cataloged, and up to 32 announcements can be linked into a single playback. Disk storage capacity is 256 one-half second announcements, 12,122 one second announcements, and 10 MB of data storage. A backup copy of the NSCX operating program is stored on disk in the data storage area. This program is transferred via the serial communications bus to the NSCX main memory during system recovery and initialization.

4.47 The data storage unit also provides an announcement recording capability via a single RTMDB time slot. This feature is currently used by the Operations Network Administration Center to produce the initial disk pack required by each NSCX. The NSCX generic program and announcement updates may be loaded from flexible diskettes onto the disk via the serial communications bus and TTY maintenance ports.

4.48 The data storage unit is divided into five functional areas (Figure 34):

- Peripheral interface controller (TN61B) and micro-program control storage (TN62)
- Disk storage interface (UN110B, TN649, and TN653)
- Playback buffer (TN652 and TN651)
- Record buffer (TN650)
- Moving head disk interface (TN65B, TN64B, and TN63B).

Peripheral Interface Controller (TN61B) and Microprogram Control Storage (TN62)

4.49 The data storage unit is controlled by a high-speed sequencer-driven microprocessor called the Peripheral Interface Controller (PIC). The PIC is designed to perform all common arithmetic, logic, and sequencer flow control operations. It is contained on one circuit pack (TN61B). Operation of the PIC is controlled by firmware on three TN62 Programmable Read-Only Memory (PROM) circuit packs. These three memory circuits provide a total storage capacity of 12 K microprogram words. A bidirectional PIC data bus provides a common path for data movement within the data storage unit. The transfer of all data over this bus is controlled by the PIC.

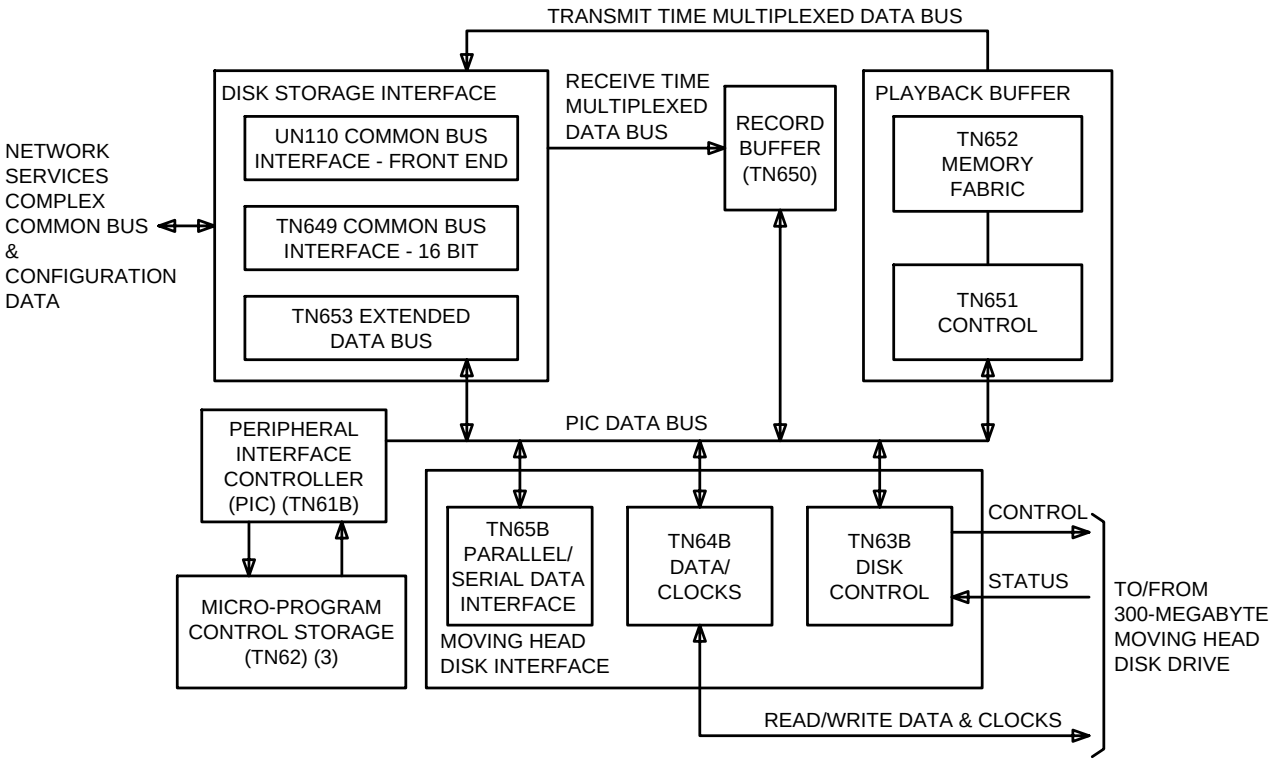


Figure 34. Data Storage Unit — Functional Block Diagram (SD-4A115-01)

Disk Storage Interface (UN110B, TN649, and TN653)

4.50 The disk storage interface consists of three circuit packs. These circuits contain the necessary communication registers and control logic to interface the unit with the TTMDB, RTMDB, timing bus, and serial communications bus. The UN110B circuit pack interfaces the playback buffer announcement data over the TTMDB to the time slot interchange unit. The TTMDB is also routed to the TN653 circuit pack for maintenance monitoring purposes. The UN110B circuit pack also interfaces the RTMDB to the record buffer via the TN653 circuit pack.

Playback Buffer (TN652 and TN651)

4.51 The playback buffer serves to buffer the PCM data from the moving head disk interface to 32 evenly-spaced TTMDB channels assigned to the data storage unit. Eight of these channels are used for generated tones and maintenance purposes. The remaining 24 TTMDB channels are reserved for announcement playback. The TN652 memory fabric provides 32 RAM playback buffers. Each buffer holds 2.048 seconds of PCM voice data at the 64-kilobit PCM data rate (16 KB per buffer). The PIC transfers PCM data from the moving head disk interface to the playback buffer memory via the PIC data bus and TN651 control circuit pack.

Record Buffer (TN650)

4.52 The record buffer serves to buffer PCM voice data input over a DS1 channel and routed over a specified RTMDB time slot to the data storage unit. Each PCM byte received is autonomously written into the record buffer at the DS1 frame rate (128 usec). The buffered voice data is transferred to the disk via the moving head disk interface. Like the playback buffer, record buffer access is also on a time-shared basis. the record buffer is a 64 K by 22 bit RAM.

Moving Head Disk Interface (TN65B, TN64B, and TN63B)

4.53 The moving head disk interface consists of three circuit packs (TN65B, TN64B, and TN63B). These circuits contain the logic, registers, and cable drivers/receivers for disk addressing control, read/write data, and error checking. Data is transferred to and from the moving head disk drive in a serial bit format at the rate of 10-megabits/second. The TN65B circuit pack contains a 32-word buffer memory and parallel/serial conversion circuits. An error correction code, stored on the disk along with the associated data, is checked for errors during the parallel-to-serial conversion. The PIC invokes fault recognition procedures when disk errors exceed a maximum allowable error density. The TN64B circuit pack provides read/write data and clock circuitry. The TN63B circuit pack provides disk control circuitry.

Moving Head Disk Drive

4.54 Disk data storage is provided by a 10-platter removable disk pack controlled by a 300 MB random access disk drive. The 10 platters provide 19 data faces and one clock/servo face. The clock/servo face provides prerecorded index, timing, and servo-positioning data used as a reference for the 19 data faces. The disk drive contains 19 read/write heads and one head for the clock/servo face. Only one of the 19 read/write heads can be active at a time. The head assembly is positioned as a unit (that is, all heads are moved simultaneously).

4.55 The disk faces are divided into 815 aligned annular tracks. Only 367 of the 815 tracks are used due to announcement playback timing requirements. The corresponding tracks on all 19 data faces are called cylinders. Each track has 32 sectors, and each sector holds 512 bytes of data. Each track holds 2 seconds of recorded information. Of the 367 cylinders used, 14 provide storage for 265 one-half second announcements, 319 provide storage for 12,122 one-second announcements, 32 are used for data storage (10 MB), and 2 are used for maintenance data.

D. Tone Receiver Unit (SD-4A116-01 [J4A017AF-1 or J4A017AF-40])

General

4.56 The tone receiver unit detects, collects, and reports touch-tone service signals dialed by callers to initiate and control conferences or other network services. It interfaces with the serial communication bus to receive control information and to report digits received to the main processor. Synchronization and master timing information is derived from the timing bus. The tone receiver unit provides 24 digital tone receivers. The network services frame is equipped with one tone receiver unit. Additional tone receiver units are located in other NSCX frames [e.g., Audio Bridge (AB) and Direct Service Dialing (DSD) frames]. The incoming tone signals are received in PCM format and routed to each of the receivers over fixed-assigned RTMDB time slots. The tone receiver unit also provides control and data interface to the Automatic Speech Recognition (ASR) unit. The tone receiver unit is divided into three (four if equipped with ASR) functional areas (Figure 35):

- Data and timing interface (UN110/UN110B, TN647, and TN646)
- Unit controller (TN645)
- Tone receivers (TN644)
- ASR Interface (if equipped with ASR) (TN1811).

Data and Timing Interface (UN110/UN110B, TN647, and TN646)

4.57 The data and timing interface consists of three circuit packs (UN110/UN110B, TN647, and TN646). These circuits contain the communication registers and control logic to interface the unit with the RTMDB, timing bus, and serial communications bus. The UN110/UN110B and TN647 circuit packs contain status and error source registers, input/output buffers, and RAM data buffers to store the transient data to and from the main processor. An 8-bit (plus parity) bidirectional data bus interconnects the unit controller (TN645) with data and timing interface circuits, and with three TN644 tone receiver circuit packs.

4.58 The UN110/UN110B circuit pack also interfaces the timing bus and RTMDB from the time slot interchange unit. The RTMDB is routed to the TN646 circuit pack for parallel-to-serial conversion, channel selection, and distribution to the three TN644 tone receiver circuit packs.

Unit Controller (TN645, MC4A021, MC4A069 with ASR)

4.59 The unit controller is an 8-bit microprocessor contained on a single TN645 circuit pack. The controller decodes and executes the autonomous operational and maintenance orders received from the main processor. It also coordinates the message formatting on all data transferred from the unit to the main processor. When instructed by the main processor, the controller will activate and monitor the specified tone receiver for a digit being present, collect the digit, perform interdigital timing, format the response, and report it to the main processor. The controller sets the tone receiver to operate in the touch-tone service mode or the multifrequency mode as specified by the activate order. When a deactivate order is received, the specified tone receiver is disabled. Any number of the 24 tone receivers can be in the active mode simultaneously. Operational and maintenance orders to the ASR unit are reformatted and passed to the ASR interface circuit pack (TN1811).

Tone Receivers (TN644)

4.60 Each of the three TN644 circuit packs contains eight digital tone receivers that can be individually configured in the touch-tone service reception mode or the multifrequency reception mode. (No NSCX services use the multifrequency reception mode at this time). Each tone receiver consists of a digital signal processor containing a Read-Only Memory (ROM) programmed to perform both types of signal detection. An 8-bit mode control register connected to the unit data bus allows the unit controller to set the operating mode

of each tone receiver. Eight consecutive serially-formatted RTMDB channels are routed to the eight tone receivers, along with RTMDB timing and synchronization signals. A digit present signal is output from each tone receiver to the unit controller. The serial output of the digital signal processors are converted to the parallel format of the unit data bus by shift registers on each of the TN644 circuit packs. Each tone receiver can be individually reset by the unit controller.

ASR Interface (TN1811, MC4A068)

4.61 The ASR Interface receives commands from the TR controller on an RS-232 link operating at 9600 baud and it reformats these commands and passes the information to the ASR unit associated with that TR unit on an IEEE-488 (Institute of Electrical Electronic Engineers) bus. It also converts the 24 TMBD channels to that TR unit into 24 individual analog channels which the ASR cards use. An additional analog channel is used as a reset control to the ASR unit. This signal is connected to the hardware reset signal for the TR unit.

4.62 The IEEE-488 bus between the ASR interface and the ASR unit is controlled by the ASR interface. The ASR unit signals an SRQ Service Request (SRQ) when it needs the attention of the ASR interface to transfer one or more of the following:

- Digit report
- Diagnostic report
- Error report.

4.63 A combination of the above requests require separate SRQs and messages for each report. The ASR interface will read the serial response buffer from the ASR unit to determine the request type. The ASR interface then sends a message to the ASR unit to read the appropriate register as indicated by the serial response buffer. The ASR interface then goes into data transfer mode and the ASR unit will write the requested data to the IEEE-488 bus until it is finished. At that point the ASR interface returns to the command mode to await the next transfer.

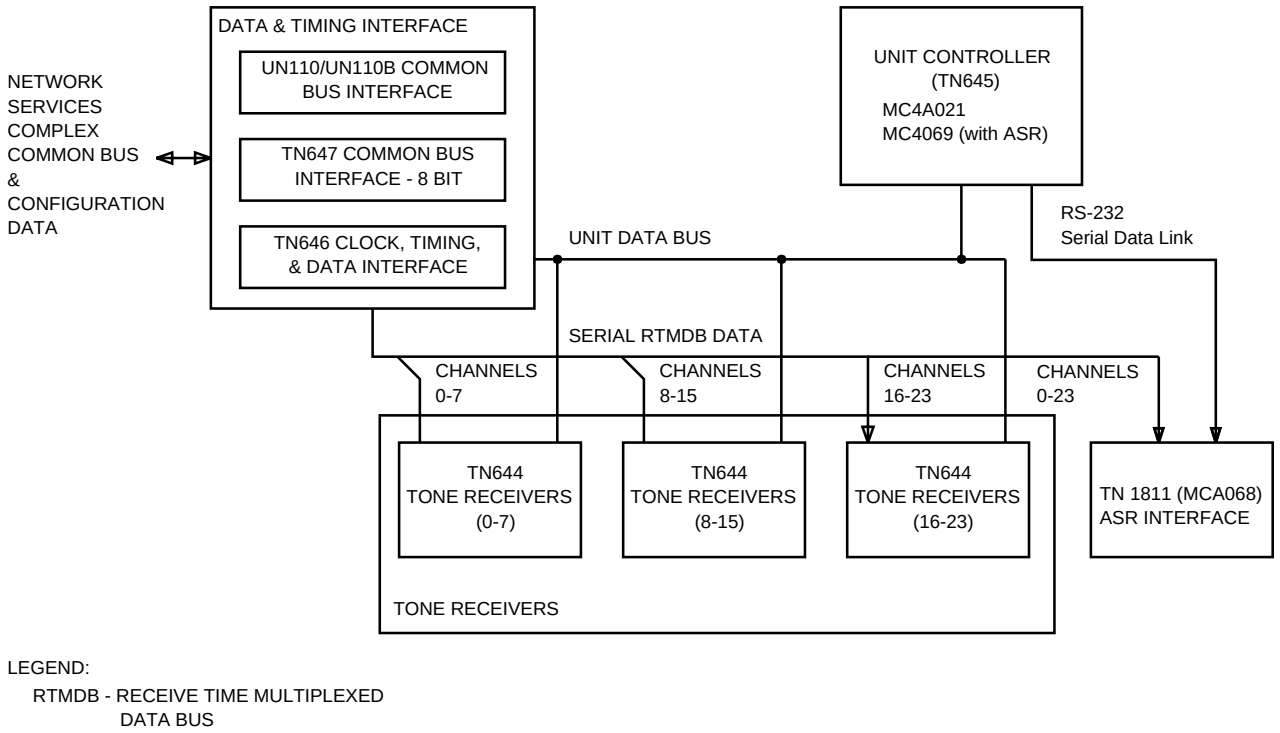


Figure 35. Tone Receiver Unit — Functional Block Diagram (SD-4A116-01)

Audio Bridge Frame (SD-4A117-01 [J4A017AB-1])

4.64 The audio bridge frame provides connections between units within the frame and interface connections to other NSCX frames. The audio bridge frame houses three units that perform specific NSCX functions. The units are (Figure 36):

- Two audio bridge units (SD-4A118-01 [J4A017BA-1])
- Tone receiver unit (SD-4A116-01 [J4A017AF-1 or J4A017AF-40]).

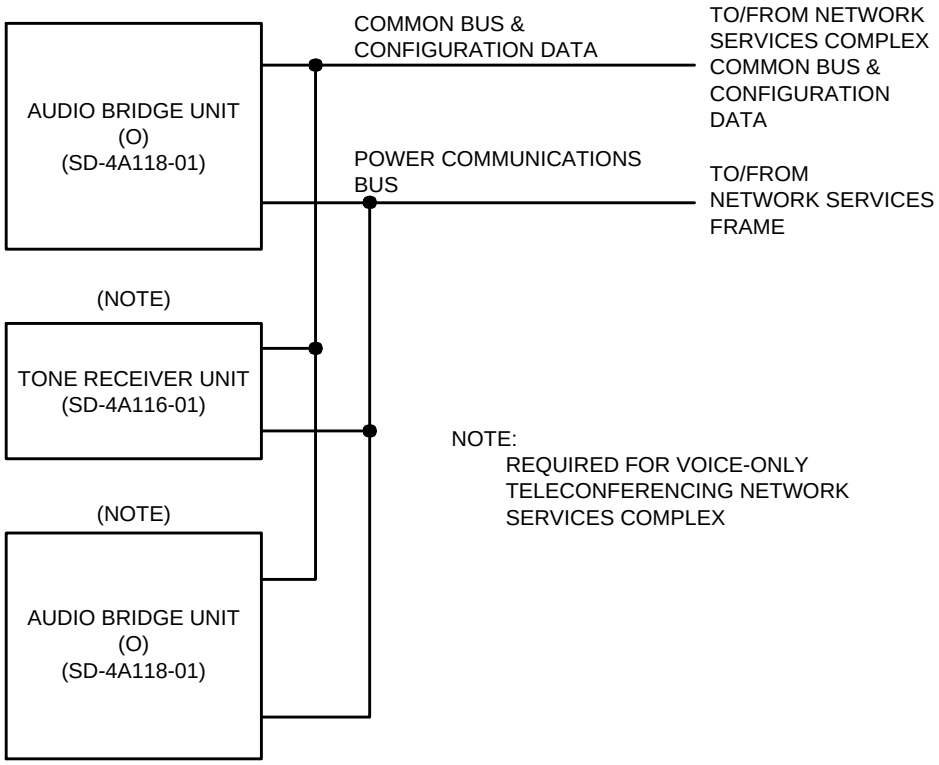


Figure 36. Audio Bridge Frame — Functional Block Diagram (SD-4A117-01)

4.65 The tone receiver unit and two audio bridge units are required for the voice-only teleconferencing configuration. The tone receiver unit in the audio bridge frame supplements the tone receiver unit in the network services frame (the tone receiver unit is discussed in the Network Services Frame section of this chapter). The two tone receiver units provide a pool of 48 tone receivers for the voice-only teleconferencing NSCX.

4.66 A common bus connection interfaces the audio bridge frame units with the NSCX serial communications bus, timing bus, RTMDB, and the TTMDB. These connections provide a communications path to and from the main processor, master timing and synchronization signals, and access to the two time multiplexed data buses to and from the time slot interchange unit in the network services frame. Configuration data and control leads provide bus cutoffs, interrupt leads associated with the serial communications bus, and frame-level strapping for unit codes and time multiplexed bus channel assignments.

A. Audio Bridge Unit (SD-4A118-01 [J4A017BA-1])

General

4.67 The audio bridge unit provides a pool of 60 ports which can be used to support conferences of variable sizes. Four additional ports per bridge are provided for maintenance purposes. Each port is assigned to a specific time slot (channel) on the RTMDB and TTMDB. The audio bridge unit is entirely digital. It is designed for multipoint bridging of both voice and data PCM-encoded analog signals and can therefore bridge data signals between analog graphics terminals. However, no special provisions are made for protocol or other special characteristics of a given terminal.

4.68 Conferences may range in size from 3 to 59 ports with one port reserved for operator access. Each audio bridge unit can support many active conferences simultaneously provided the total number of conference legs do not exceed 59. Each port provides echo cancellation, noise limitation, and automatic gain control. The speech data received over any given port is bridged (summed) with the speech data from other ports of the conference and broadcast to all conferees. The speech data received by any given port is deleted from the outgoing bridged data to that port. The audio bridge unit provides various conference options which are implemented via control information received from the main processor. These options include the ability to:

- Limit specified conference legs to listen-only status.
- Limit the number of ports from which speech data is simultaneously summed into the outgoing bridge data.
- Establish priority of port speech data to be added to the bridge.

4.69 The audio bridge unit is divided into six functional areas (Figure 37):

- Peripheral interface controller (TN61B) and microprogram control storage (TN62))
- Peripheral unit control bus interface (UN110/UN110B and TN649)
- Framing, timing, and data transfer (TN655, TN656, TN657, and TN663)
- Echo cancellation (TN662)
- Speech detection (TN661 and TN660)
- Conference summation (TN658 and TN659).

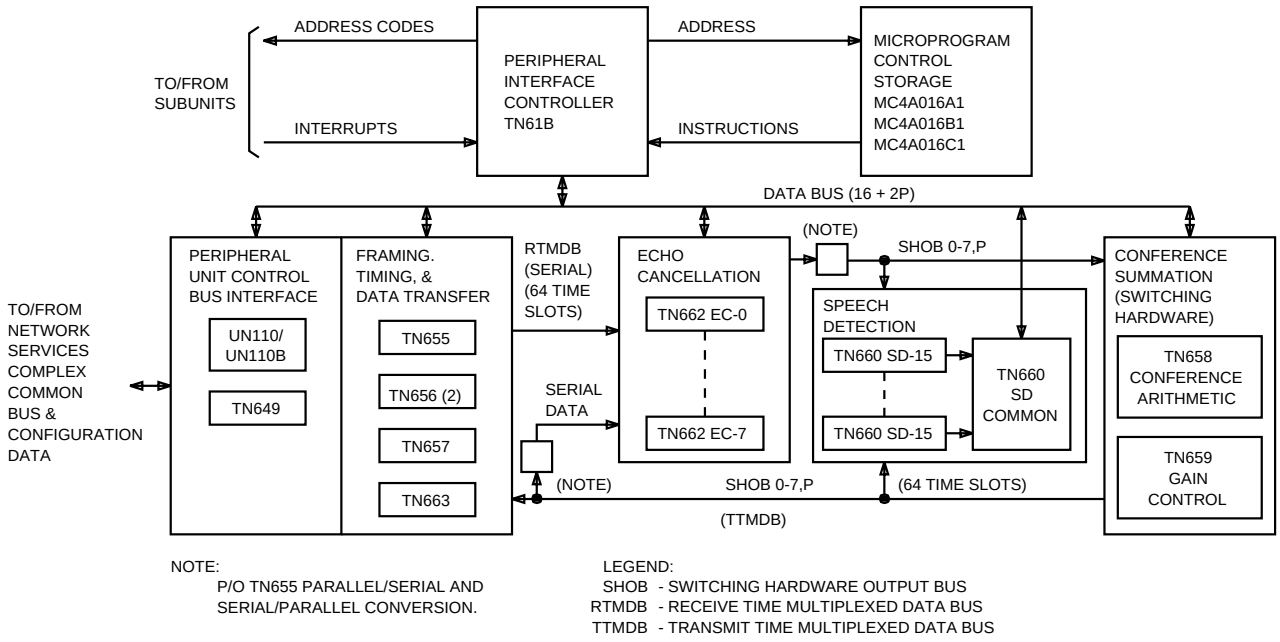


Figure 37. Audio Bridge Unit — Functional Block Diagram (SD4A118-01)

Peripheral Interface Controller (TN61B) and Microprogram Control Storage (TN62)

4.70 The audio bridge unit is controlled by the PIC contained on the TN61B circuit pack. This 16-bit microprocessor is also used in the data storage unit and provides the same features as in that application. Operation of the PIC is controlled by firmware contained on three TN62 PROM circuit packs. These three memory circuits provide a total storage capacity of 12 K microprogram words. An internal bidirectional data bus (16 bits plus byte parity) provides a common path for the movement of control data within the unit. The transfer of all data over this bus is controlled by the PIC.

4.71 The PIC controls the status of every conference by writing conference control information into a switching hardware control memory. The PIC receives instructions from the main processor to set up and control various conference options. The PIC scans the speech detection speech-level registers periodically to obtain information about the speech level of every conferee in a conference. This information is changed into control data and written into the switching hardware control memory to control the conference noise and speech level. The PIC controls the operation of the echo canceler hardware by writing control data into the echo canceler control registers.

Peripheral Unit Control Bus Interface (UN110/UN110B and TN649)

4.72 The peripheral unit control bus interface consists of two circuit packs (UN110/UN110B and TN649). These circuits contain the necessary communication registers and control logic to interface the unit with the TTMDB, RTMDB, timing bus, and serial communications bus. Serial communications bus interface circuits include status and error source registers, input/output data buffers, and RAM data buffers to store the transient data to and from the NSCX main processor. The PIC is provided access to these circuits via the internal 16-bit data bus.

4.73 The UN110/UN110B circuit pack provides the drivers, receivers, and parity generation/check circuits required to interface the TTMDB, RTMDB, and timing bus to the framing, timing, and data transfer circuits. This circuit also includes a time slot select circuit which outputs a signal to framing, timing, and data transfer circuitry on every fourth count of the 256 time slot count. These signals are used to multiplex the PCM data on 64 RTMDB and TTMDB channels within the unit. Assignment of these 64 RTMDB and TTMDB channels for each audio bridge unit is determined by a time slot offset code to the UN110/UN110B circuit pack. This offset code is hard-wired for each unit during installation.

Framing, Timing, and Data Transfer (TN655, TN656, TN657, and TN663)

4.74 The framing, timing, and data transfer circuits consist of five circuit packs. These circuits provide timing and PCM data distribution to and from echo cancellation, speech detection, and conference summation circuitry. The incoming parallel data on 64 RTMDB time slots is converted to the serial format required by the echo cancelers and back to the parallel format for the switching hardware input bus. The parallel data from the switching hardware output bus is also converted to serial format for the echo cancelers. These circuits also insert the 64 time slots of parallel-formatted data from the switching hardware output bus into every fourth time slot of the outgoing TTMDB.

Echo Cancellation (TN662)

4.75 Echo cancellation hardware is contained on eight TN662 circuit packs. These circuits provide an echo cancellation circuit for each of the 64 ports. Each circuit pack contains eight echo cancellation circuits. Each echo cancellation circuit receives the incoming and outgoing serially-formatted PCM data during its assigned time slot and modifies the incoming data to cancel the echo. A fixed threshold is used to compute the echo level. The modified input data is serially output during the assigned time slot and routed via the framing, timing, and data transfer circuitry to the switching hardware input bus. Echos in excess of

the threshold level are detected by the speech detection hardware.

4.76 Echo cancellation is implemented to detect the presence of outgoing bridged data on the incoming ports which may be reflected back to the NSCX by the telephone network. There are no echos caused by the digital audio bridge unit. Echo cancellation is provided to prevent the echos caused by external sources from entering the bridging circuits.

4.77 The PIC routinely initiates the self-check of each echo cancellation circuit for each idle port. If no errors are detected, the echo cancellation circuit will be enabled. If errors are detected, the corresponding circuit will be disabled. The service status of each echo cancellation circuit is retained by the control program.

Speech Detection (TN661 and TN660)

4.78 The speech detection hardware consists of 17 circuit packs. These circuits provide a dedicated speech detector for each of the 64 ports. Each speech detector monitors the transmit and receive PCM data during its assigned time slot to distinguish between speech (valid voiceband signals) and nonspeech (noise or echo). When speech is detected, the speech level is measured and loaded into a speech-level register. When nonspeech is detected, the register is loaded with a specified nonspeech code. The PIC routinely reads the 64 speech-level registers and changes the level data for each port into control data. The control data is then written into the switching hardware control memory to control the levels of speech, noise, and echo input to the bridge.

4.79 The speech detector compares the modified PCM data from the echo canceler with a varying threshold level to distinguish between speech and noise. The incoming PCM data is also compared with the outgoing data to detect low-level echo passed by the echo canceler. The incoming data is considered as speech when it is above the threshold level and no echo is detected.

4.80 There are four speech detector circuits contained on each TN661 circuit pack. Each detector consists of a digital signal processor, EPROM, parallel-to-serial, and serial-to parallel conversion circuits, and an 8-bit speech-level register. Each circuit also checks parity on the transmit and receive data. A single parity error output lead connects each TN661 circuit pack to a 16-bit error source register in the TN660 circuit pack. A control register on each TN661 circuit pack allows the PIC to control the operation (enable/disable, etc.) of each digital signal processor. Read/write access to this register is provided via the internal data bus. The output data from each speech level register is multiplexed to the internal data bus via the TN660 circuit pack. The TN660 circuit pack also contains a 16-bit cutoff control register. This register allows the PIC to disable the output of speech level data from any of the 16 TN661 circuit packs.

Conference Summation (TN658 and TN659)

4.81 The conference summation hardware consists of two circuit packs. These circuits are also called the switching hardware. The TN658 circuit pack contains the conference control memory, coefficient memory, arithmetic circuits, and memory storage for the voice samples to be summed into the bridge. The TN659 circuit pack contains an input ROM, input multiplier, output multiplier, and an output ROM. The input ROM translates the incoming PCM data from the standard mu-255 compressed format to linear data. The output ROM provides the inverse function.

4.82 The switching hardware sums the input signals for each conference during each frame of 64 time slots. It then transmits the summed conference signals to each conferee. The input signals for any given time slot are subtracted from the summed conference signals transmitted in the corresponding outgoing time slot.

4.83 Automatic level control and noise control are also provided by the switching hardware. The signal levels input to each conference are equalized so that conferees will not detect a significant difference in volume. The speech detectors report the measured levels of each speech/noise sample to the PIC. The PIC determines the amount of modification to be made and transfers a coefficient for each time slot to the switching hardware. The incoming signals are then modified prior to conference summation. The coefficients are also used to control the conference noise level. A conferee may be added as a talker or only as a listener. The PIC has complete control over the gain/loss modification of audio levels by writing a location in the coefficient memory for each time slot.

Network Services Frame (SD-4A139-01, J4A017G-1)

4.84 The J4A017G-1 Network Services Frame houses five units that perform specific NSCX functions. This NSCX frame is used for the DSDC application when using DSD8 or later (Figure 38). The five units are:

- Time slot interchange unit, (SD-4A114-01, J4A017AB-1)
- Processor and N-link terminal unit, (SD-4A140-01, J4A017AL-1)
- Maintenance interface unit, (J4A017AC-1)
- Data storage controller unit, (SD-4A141-01, J4A017AM-1)
- Tone receiver unit, (SD-4A116-01, J4A017AF-1 or J4A017AF-40).

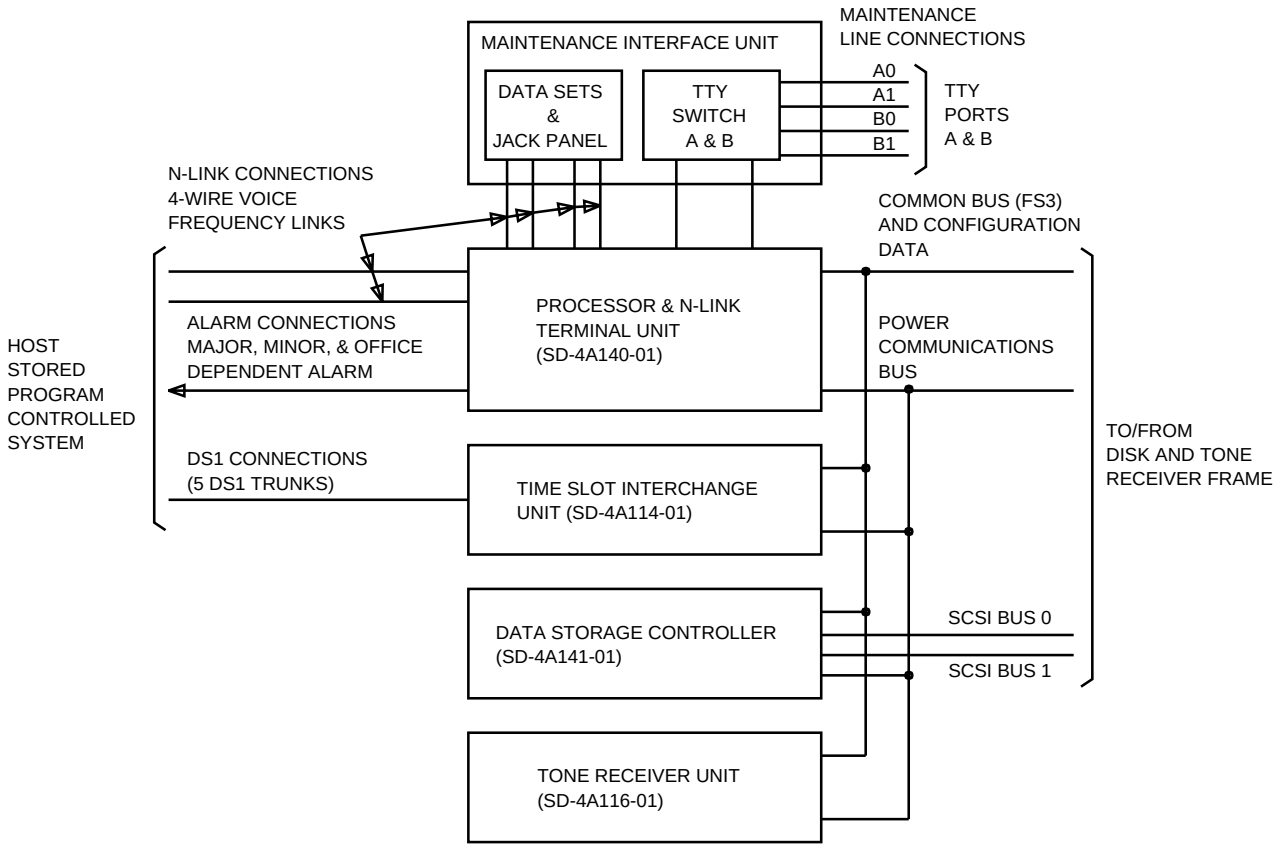


Figure 38. Network Services Frame — Functional Block Diagram - SD4A139-01, J4A017G-1

A. Processor and N-Link Terminal Unit (SD-4A140-01, J4A017AL-1)

General

4.85 The processor and N-link terminal unit provides overall control of the NSCX. It performs call processing, maintenance, fault recovery, diagnostics, and audits for the NSCX. The various modules in the processor and N-link terminal unit are interconnected via a parallel address, data, and control bus called the system bus. The modules are designed with bus master circuitry and/or bus slave circuitry. Modules designed with bus master circuitry may obtain use of the bus and initiate data transfers on it. Modules designed with bus slave circuitry are the object of data transfers only. The main processor, IOP, centralized announcement update processor, and memory refresh controller are the only modules on the system bus designed with bus master circuitry. Modules on the bus designed with slave bus circuitry include the main memory, interrupt controllers, timers, N-link terminal, main memory protection circuit, unit cutoff registers, display drivers, and other maintenance registers. The processor and N-link terminal unit is divided into nine functional areas (Figure 39):

- Main processor (TN637)
- Main memory (TN664)
- Input/output processor (TN1590)
- Centralized announcement update processor (TN654)
- Processor display board (TN678)
- N-Link terminal unit (TN640, two TN638, and TN639)
- Link processor (TN639)
- Serial link interface (TN638)
- Voice frequency link access (TN640).

Main Processor (TN637)

4.86 See paragraphs 4.22, 4.23, and 4.25.

Main Memory (TN664)

4.87 The main memory consists of one or two TN664 circuit packs which reside on the system bus. The system bus address range allows up to 2 MB of memory.

4.88 Each TN664 provides 1 megabyte of dynamic RAM. Each pack has its own refresh circuitry, but one pack refresh controller (pack number one, the leftmost) is active and controls all memory pack refreshes. The full 2 MB of RAM is accessible by the IOP.

4.89 Since the main processor memory is implemented using dynamic RAM, it is protected from memory faults by an error correction scheme. Six additional memory bits for each 2-byte word are used to store an error detection and correction code calculated over each 16-bit word. Uncorrectable errors result in an interrupt of the main processor so that fault recovery programs can be invoked.

4.90 The operating program and data used by the main processor is stored in the main memory. Since this memory is volatile, a loss of power to the unit will destroy the contents of the memory. Therefore, during power-up or bootstrap, the memory must be loaded from disk. This operation is performed by the IOP which contains firmware stored in EPROM. Programs are loaded from disk only during NSCX initialization and fault recovery procedures. Paging from the disk is not done during normal operation.

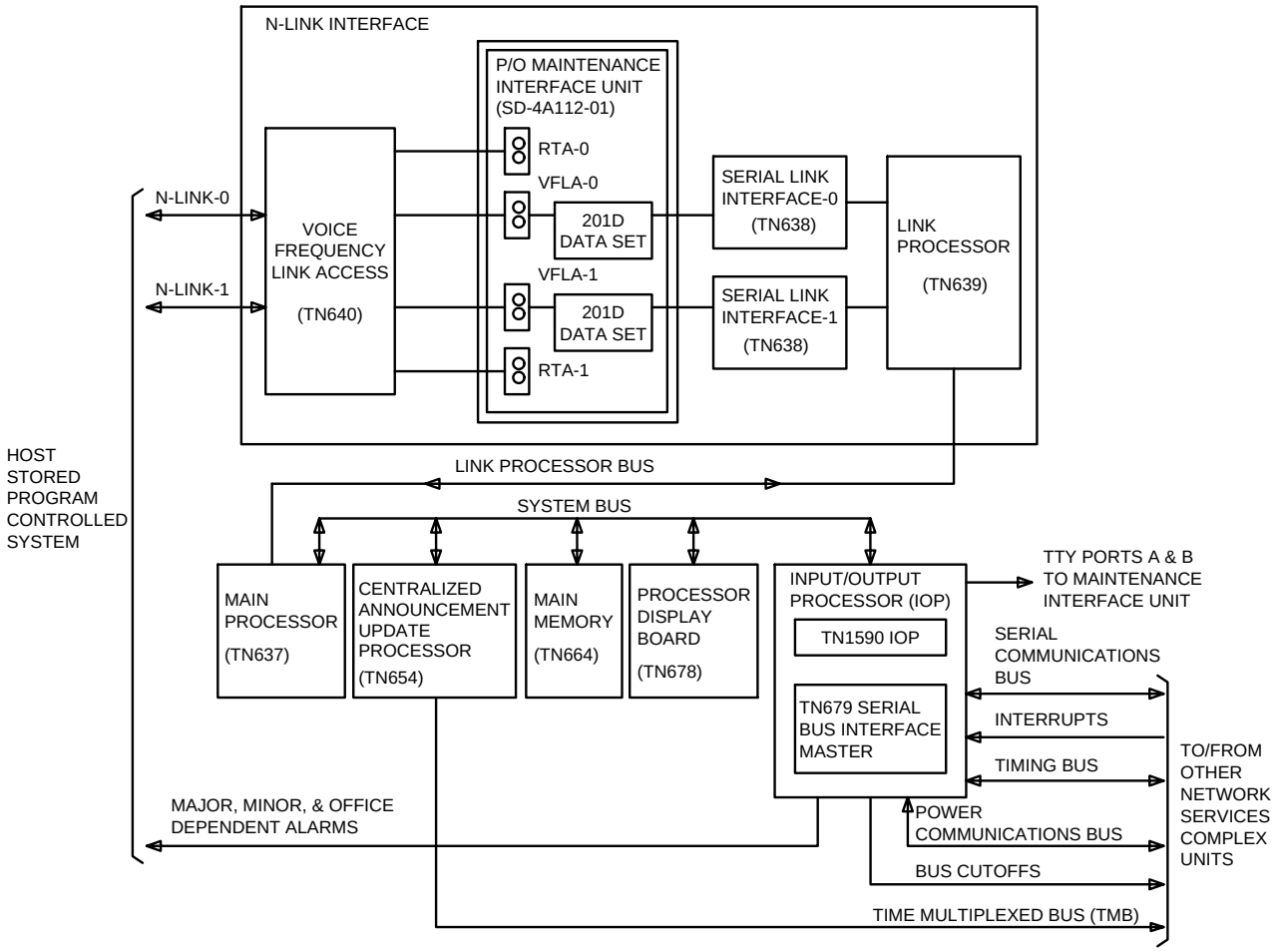


Figure 39. Processor and N-link Terminal Unit - SD4A140-01, J4A017AL-1 — Functional Block Diagram

Input/Output Processor (TN1590 and TN679)

4.91 The IOP consists of two circuit packs (TN1590 and TN679). Circuit pack TN1590 contains the circuitry for IOP functions. Circuit pack TN679 contains the circuitry for the serial bus interface master. The IOP functions mainly as a direct memory access controller for all units and TTY port input/output operations. Since the IOP program is contained in EPROM, the program is also used for bootstrap and other recovery and utility functions. The IOP is a complete processing system using a single 16 bit 8086 microprocessor. The IOP also contains RAM and EPROM, system bus and serial communications bus interfaces, timers, TTY ports, and other miscellaneous hardware.

4.92 The 8086 microprocessor interfaces with the system bus and an internal IOP bus called the resident bus. The resident bus connects all of the local IOP peripheral devices together. These devices include the serial communications bus interface, the IOP memory, and two TTY ports. The IOP controls all serial communications bus activity. The IOP memory consists of 64 KB of EPROM and 8 KB of RAM. The IOP program is contained in the EPROM. Addresses generated by the IOP to this EPROM are mapped from the upper 64 K main memory address spectrum to the IOP resident bus. The RAM serves as a data storage facility for the IOP. The RAM is comprised of static devices which do not require periodic refreshing to maintain the data contents. Addresses generated by the IOP to this RAM are mapped from the lowest 8 K of the main memory address spectrum to the IOP resident bus.

4.93 Two ASCII start-stop TTY ports reside on the IOP resident bus. Each port consists of a UART, RS-232C drivers and receivers for both data and modem control, and baud rate generation hardware. During normal NSCX operation, the two TTY ports are set to operate in the half-duplex mode at 1200 baud. However, TTY port B can be reconfigured by the user to operate at the standard rates of 1200, 2400, 4800, or 9600 baud.

4.94 The two UARTs provide TTY access to the NSCX via two key switches (A and B) and four RS-232C connectors (A0, A1, B0, and B1) located on the maintenance interface unit. Switch A transfers control only between the A0 and A1 connectors. Output data may be simultaneously monitored via both connectors (A0 and A1). Switch B transfers all port functions between connectors B0 and B1. These two TTY ports provide the primary control and display facility for the NSCX. They may be interfaced to a dedicated or shared data terminal arrangement in the host office and to a remote operations, administration, and maintenance facility. The local data terminal equipment may include a keyboard/display terminal, printer, and flexible diskette data storage/playback equipment. When the main processor is in the maintenance mode, only TTY port A is active.

Processor Display Board (TN678)

4.95 See paragraphs 4.32, 4.33, and 4.34.

Centralized Announcement Update Processor (TN654)

4.96 The addition of the TN654 pack to the NSCX complex makes centralized announcement update possible (Figure 40). This pack contains an 80186 microprocessor, an interface to shared system memory, and an interface to the RTMDB/TTMDB into and out of the TSI [2]. The concept of the centralized announcement update is that an NSCX site designated a master can send an announcement stored on its disk in Adaptive Differential Pulse Coded Modulation (ADCPM) format to any or all of up to 24 remote or slave stations. A powerful error correction scheme guarantees that the announcement is transmitted correctly. The announcement ends up stored in ADPCM format on the receiving stations' disks. Transfer is made in real time using dial AS-56 lines. Since ADPCM does not use all the available AS-56 bandwidth, error correction code can be included with the announcement data. The announcement is broken into buffers for transmission, and each buffer is appended with a two-dimensional error correcting code. This code can correct up to 12 ms

of dropout every 299 ms in the presence of a continuous background error rate of 1 in 1000 (ten to the minus third).

4.97 The microprocessor on the TN654 pack communicates with the rest of the system via a mailbox arrangement in shared memory. When it is desired to transfer an announcement, the TN654 pack at the master end is notified to prepare to broadcast. It starts sending a unique test pattern coded with the error correcting code. The slave stations then make AS-56 calls to the master site, and their TN654 packs are notified to prepare to receive. Time slots are selected in the TSI so that the incoming AS-56 calls at the master and outgoing calls at the slave are in slots on the TTMDB and RTMDB buses. Also, connection is made between the Data Storage Controller (DSC) at each end and the TN654 pack. When all the receiving slave stations have completed their calls and have synchronized on the test pattern, a command is entered at the master station [usually from the Centralized Announcement Update (CAU) control system] to start the broadcast. The master immediately switches from test pattern to actual announcement data. The slave stations sense this change and begin decoding the incoming buffers and sending the ADPCM announcement data to the DSC for recording. At the end of the transfer process, byte counts are checked at each end against those requested and with a count sent over the link in a message trailer. If they are correct and if there has been no uncorrectable transmission error, the announcement is made permanent at the receiving site.

4.98 The TN654 pack contains an INTEL* 80186 microprocessor and a four-channel DMA controller along with 128 KB of RAM memory and 64 KB of EPROM memory. The DMA controller acts as an interface between the processor and the RTMB/TTMB bus that communicates with the TSI. All four channels of the controller can be performing independent channel subprograms simultaneously. The first DMA channel transfers bytes from the AS-56 time slot from the TSI into RAM buffers. The second channel feeds data to the error-correction circuits. The third channel receives data back from the error-correction circuits. The fourth channel outputs data to the DSC via another TSI time slot. In addition to this, the microprocessor communicates with the system main processor via a block of shared system memory. Notification is in the form of interrupts.

N-Link Terminal Unit (TN638, TN639, and TN640)

4.99 See paragraphs 4.35 through 4.40.

* Registered trademark of Intel Corporation

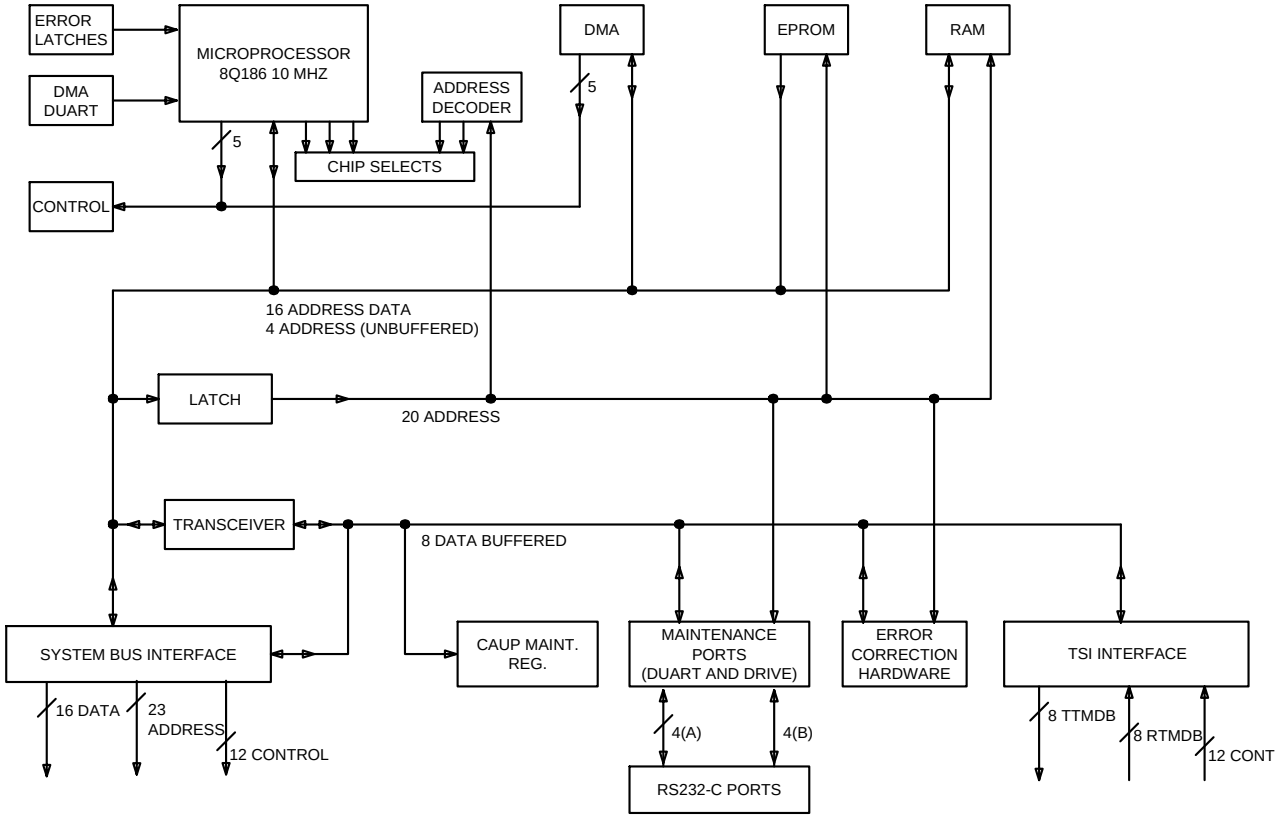


Figure 40. Centralized Announcement Update Processor — Functional Block Diagram

B. Time Slot Interchange Unit (SD-4A114-01, J4A017AB-1)

4.100 See paragraphs 4.41 through 4.45.

C. Data Storage Controller Unit SD-4A141-01, J4A017AM-1)

4.101 The unit, in conjunction with the Disk and Tone Receiver (DTR) Frame), provides disk-based recorded announcements and general data storage for the NSCX. Announcements are output in PCM format over TTMDB time slots assigned for use by the DSC. Up to 72 announcements may be output (played) simultaneously. (Actually the requirements are 72; however, the DSC has the capability to output 120 announcements simultaneously.) Up to 42,000 unique announcements may be cataloged, and up to 32 announcements can be linked into a single playback. Disk storage capacity is 96 half-second announcements, 202 one-second announcements, and 20 MB of data storage. A backup copy of the NSCX operating system is stored on disk in the data storage area. This program is transferred via the serial communications bus to the NSCX main memory during system recovery and initialization.

4.102 The DSC along with the disk and tone receiver frame (SD-4A144-01) are a replacement for the DSU (data storage unit) (SD-4A115-01) and associated 300-megabyte moving head disk frame (SD-4C056-01) for DSDC applications of the NSCX. The data storage controller unit is divided into five different functional areas (Figure 41):

- Unit controller and memory (TN1576, TN1577, and TN1583)
- Disk interface (TN1578)
- Common bus interface (TN649 and UN110B)
- Voice buffer (TN1581 and TN1582)
- Voice control (TN1579 and TN1580).

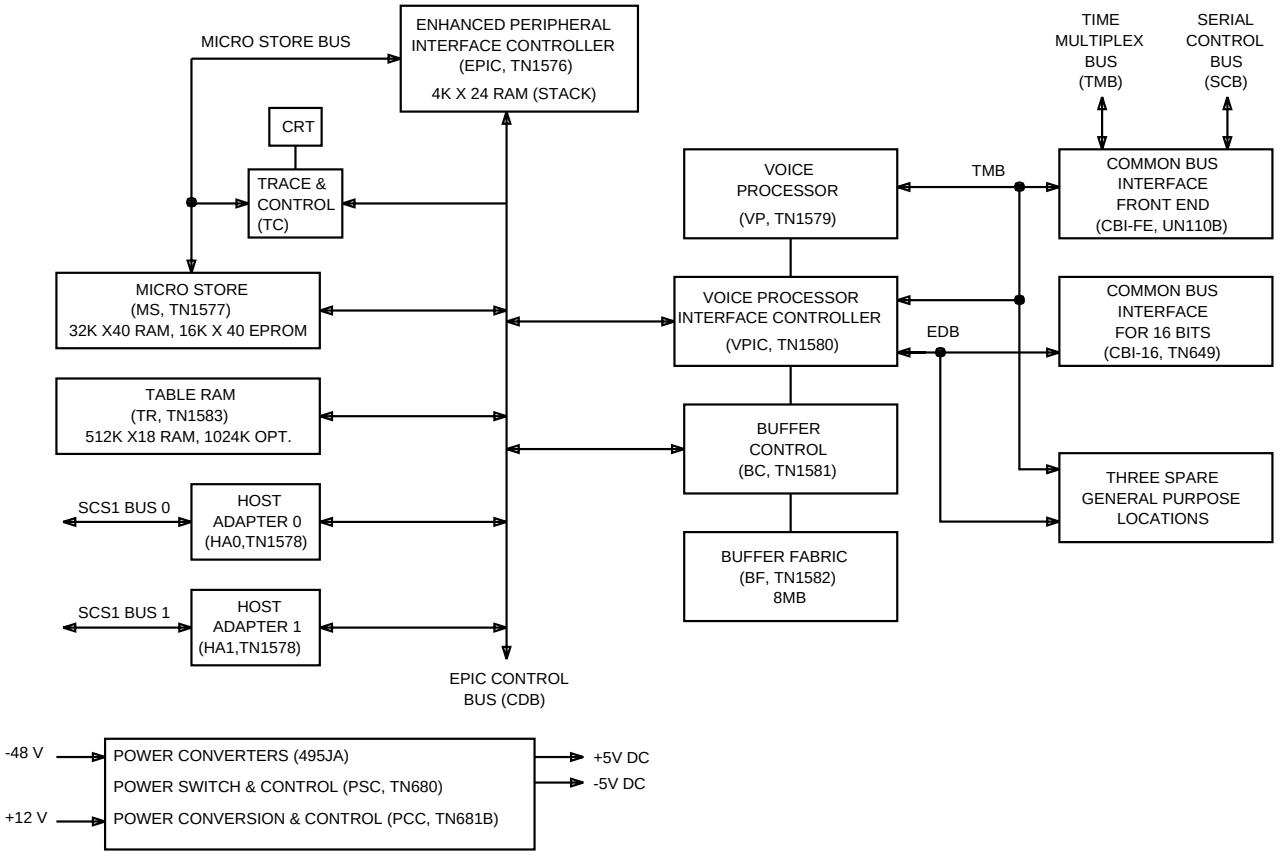


Figure 41. Data Storage Controller Unit SD4A141-01 — Functional Block Diagram

Unit Controller (TN1576)

4.103 The TN1576 Enhanced Peripheral Interface Controller (EPIC) provides central control for the DSC unit and is based on the 2901 bit-slice processor arranged as a 16-bit microprogrammed controller. The EPIC communicates with the other peripheral circuit packs in the DSC by an 18-bit data bus, (16 bits of data and 2 bits of parity). The EPIC executes a microprogram contained in 16 K by 40 of EPROM plus an additional 32 K by 40 of RAM located on the TN1577 MS (micro store), which is loaded during DSC unit initialization. A TN1583 TR (table RAM) circuit pack provides 512 K words of general purpose memory. A second TR can be added to the DSC unit in EQL 04-130 to further increase the amount of table RAM provided.

4.104 To help during development of the DSC unit and during debugging of field problems, a special L-567460 TC (trace and control) circuit can be inserted into a spare circuit pack position (EQL 04-106) next to the EPIC to provide programmer control of the EPIC. With the TC, EPIC microinstructions can be traded, single-stepped, break points set, etc.

Disk Interface (TN1578)

4.105 Two TN1578 Host Adapter (HA) circuit packs provide an interface between the EPIC and the two Small Computer System Interface (SCSI) buses. Each SCSI bus is connected to hard disks used to store announcement and program data for the NSCX. All disks connected to the SCSI buses are located in the disk and tone receiver frame (J4A0017H-1). Two SCSI buses are provided to reduce overall disk seek time for the unit and increase data throughput. The data stored on the disks is the same between SCSI buses. In this way, one disk can seek while the other is transferring data. A single floppy disk is provided on SCSI Bus #0 to allow high speed program downloading.

4.106 The SCSI is the X3T9.2 standard adopted by the American National Standards Institute (ANSI). The SCSI devices are daisy-chained together on a shielded 50-conductor SCSI bus cable. The two ends of the SCSI bus 50-conductor cable are terminated with an impedance of 100 ohms. The SCSI data bus and SCSI control bus are common to all devices, and they are driven differentially (that is, dual lines driven out of phase with each other). This allows up to a 25 meter bus length and helps in meeting Electro-Magnetic Compatibility (EMC) requirements.

Voice Buffer (TN1581 and TN1582)

4.107 A large four-megaword memory array is provided by a TN1582 Buffer Fabric (BF) to buffer announcement data being played or recorded on each channel used on the Time Multiplexed Bus (TMB). The TN1582 also stores half-second and one-second announcements so that they do not have to be moved from disk each time they are needed. Data is written into and read from the TN1582 by the 1581 Buffer Control (BC) which administers control to the memory by interleaving EPIC and voice processor access.

Voice Control (TN1579 and 1580)

4.108 The TN1579 Voice Processor (VP) and TN1580 Voice Processor Interface Controller (VPIC) perform Adaptive Differential Pulse Code Modulation (ADPCM) decoding/encoding of the data to/from the TMB. The ADPCM algorithm provides a two-to-one compression/expansion of PCM data which doubles the voice storage capacity of the disks connected to the DSC unit.

Common Bus Interface (TN694 and UN110B)

4.109 The UN110B Common Bus Interface - Front End (CBI-FE) and the TN649 Common Bus Interface for 16 bits (CBI-16) provide an interface to the TMB and the SCB. The TMB carries PCM data to/from the TSI unit while the SCB carries control messages to/from the PROC unit.

D. Tone Receiver Unit (SD-4A116-01, J4A017AF-1 or J4A017AF-40)

4.110 See paragraphs 4.56 through 4.63.

Disk and Tone Receiver Frame (SD-4A144, J4A017H-1)

4.111 The J4A017H-1 disk and tone receiver frame houses four different type units that perform specific NSCX functions. This frame is used only for the DSDC application. The units are found in Figure 20.

- Tone receiver unit (SD-4A116-01, J4A017AF-1 or J4A017AF-40)
- Floppy disk unit (SD-4A143-01, J4A017HC-1)
- Hard disk unit (J4A024AC-1, SD-4A168-01)
- Fan unit (J5D003BE-1, SD-5D019-01).

Tone Receiver Unit (SD-4A116-01, J4A017AF-1 or J4A017AF-40)

4.112 See paragraphs 4.56 through 4.63.

Floppy Disk Unit (SD-4A143-01, J4A017HC-1)

4.113 The floppy disk unit consists of a 5.25-inch floppy disk drive, a SCSI single-ended to differential-ended converter board, and an SCSI single-ended disk drive controller. The floppy disk drive is 1.2 MB formatted (1.6 MB unformatted) in capacity. The unit is powered by the 131J1 (+12 V) and 131F1 (+5 V) power units located on the fuse panel.

Hard Disk Unit (J4A024AC-1, SD4A168-01)

4.114 The Hard Disk Unit consists of a hardware shelf equipped with two TN1972 Hard Disk circuit packs and two UN356 Power Control circuit packs. It can optionally be equipped with a second pair of TN1972 circuit packs. Each pair of TN1972 circuit packs will provide 1.6 GB of usable space after they have been formatted. This will provide 402,653 seconds of announcement space. The Hard Disk Unit will derive its power from the frame provided –48 V.

Fan Unit (J5D003BE-1)

4.115 The fan unit will provide the necessary cooling for the Hard Disk Unit. Each fan unit will be equipped with three fans. Failure of a fan will cause and alarm indication. A LED will also be provided to indicate which fan has failed.

Automatic Speech Recognition Cabinet (SD-4A200-01, J4A017R-1)

4.116 The Automatic Speech Recognition (ASR) is located in a separate ASR cabinet but is considered a subunit of the TR. It interfaces with the ASR interface in the Tone Receiver. The ASR cabinet contains the ASR units needed to support the speech recognition of up to 3 T1 lines between the NSCX and the Host switch.

A. Automatic Speech Recognition Unit

4.117 The ASR unit provides the NSCX with single digit speech recognition capabilities. Each ASR unit will provide 24 channels of speech recognition capability. Three ASR units are required to provide the speech recognition support of up to 3 T1 lines between the NSCX and the Host switch. The ASR units consist of:

- Passive backplane enclosure
- Power supply
- Single board processor
- Floppy/hard disk interface
- IEEE-488 interface card
- 12 ASR circuit cards (AYC8)
- Bus termination Card (AYC19).

4.118 The passive backplane enclosure contains all the necessary power connections to operate the ASR unit. The passive backplane enclosure consists of power supply, power switch, a passive 20 slot AT computer backplane, and three fans attached to the front face of the enclosure (Figure 28).

4.119 The enclosure houses the single board processor, 12 ASR circuit cards, floppy/hard disk interface, IEEE-488 GPIB (General Purpose Interface Bus) interface card, bus termination card, and power supply.

4.120 The single board processor collects the valid digits collected by the ASR circuit cards and reports the digits back to the TR unit over the IEEE-488 bus. The ASR interface in the TR unit then transmits the data to the TR controller over the intra-unit RS-232 serial bus where it is formatted and sent to the MP over the SCB. The processor resets and enables the speech detector of the ASR channel prior to each instance of speech detection. The processor also performs internal diagnostics, initializes the IEEE-488 bus, loads the ASR circuit card's programs and templates from the hard disk drive located in the ASR Interface unit.

4.121 The Disk Interface accesses the hard disk during initializations and updates. During an initialization the MS-DOS* software, GPIB software, processor operational program, ASR circuit card recognition code and its voice templates are loaded to the ASR unit from the ASR Interface unit's hard disk drive. When the various internal diagnostics are run, the ASR unit informs the TR unit that the initialization completed without error the ASR unit is ready for either additional diagnostic commands or operational commands. It also accesses the floppy drive used for updating the ASR software.

4.122 The IEEE-488 GPIB bus interface card provides the interface control link between the single board processor and the ASR Interface circuit pack (TN1811) located in the TR unit shelf.

4.123 Each of the 12 ASR circuit cards contain 2 independent channels of speech recognition capability to provide a total of 24 channels of recognition per ASR unit. Each ASR channel will have a separate analog input supplied by the TR unit to provide the analog speech path to each ASR channel.

4.124 The bus termination circuit pack provides passive termination for the control, address, and data signals in the 20 slot ASR unit.

B. ASR Interface Unit

4.125 The ASR Interface unit contains the floppy and hard disks used by the ASR unit. The operational software will boot off the hard disk drive while the floppy disk is for software updates only. The hard disk contains the MS-DOS software, GPIB software, processor operational program, ASR circuit card recognition code, and the ASR circuit card voice templates.

* MS-DOS is a registered trademark of Microsoft Corporation in the United States and other countries.

5. Network Services Complex Controls and Indicators

Maintenance Interface Unit Controls

5.01 The primary control and display facility for the NSCX is provided by two TTY IOP ports (A and B) on the maintenance interface unit (Figure 7). These two ports may be interfaced to a dedicated or shared data terminal arrangement in the host office and to a remote operations, administration, and maintenance facility. The data terminal equipment may include a keyboard/display terminal, printer, and flexible diskette data storage/playback equipment. During normal system operation, each port is set to operate at 4800 baud, full-duplex. Port B can be configured by TTY input messages to provide all of the standard baud rates up to 9600 baud.

5.02 Two RS-232C-type connectors are provided for each TTY port, controlled by an associated switch (552A key). The A switch transfers transmit control (only) between the two associated connectors (A0 and A1). Output data may be simultaneously monitored via both connectors A0 and A1. The B switch transfers all port functions between connectors B0 and B1.

TN678 Display Panel Controls and Indicators

5.03 The TN678 circuit pack in the processor and N-link terminal unit (Figure 5) provides some limited control and display functions essential to the bootstrapping of the NSCX. The display section provides a summary of NSCX status and error conditions and an alphanumeric display to indicate a failing test state. The alphanumeric display is also used to indicate the level of initialization taking place. These displays are designed to give an immediate indication of NSCX status and error conditions. Also, the displays aid in repairing the NSCX when the TTY ports are inoperative. Controls and indicators for the TN678 circuit pack are defined in Table A.

TN680 Power Switch Controls and Indicators

5.04 The processor and N-link terminal unit and each NSCX subunit except the the 2 Gbyte Hard Disk Unit contains one TN680 power switch and control circuit pack. The Power Failure (PF) Light-Emitting Diode (LED) is associated with the power monitor and distribution circuits contained in the TN680 circuit pack. These circuits can support up to eight functional circuit packs. Identical power monitor and distribution circuits are provided by the TN681/TN681B circuit pack to support the remaining functional circuit packs (in groups of eight) contained in each NSCX unit. Controls and indicators for the TN680 circuit pack are defined in Table B.

UN356 Power Unit Switch Controls and Indicators

5.05 The J4A024AC-1 Hard Disk Unit contains two UN356 Power Units. The UN356 contains switches to turn the power on and off. It is also equipped with LED type alarms that indicate the status of the unit. Controls and indicators for the UN356 Power Unit are defined in Table C.

Table A. TN678 Display Panel — Controls and Indicators

Name	Type	Function
(None)	Alphanumeric Display	Indicates diagnostic phase number or initialization level number
SVC	LED (Red)	Indicates service is inhibited
TRKS	LED (Yellow)	Indicates trunks are blocked
INH	LED (Yellow)	Indicates interrupts are inhibited
DGN	LED (Green)	Indicates diagnostics is in progress
INIT	LED (Green)	Indicates NSCX initialization is in progress
MU	LED (RED)	Indicates memory is uninitialized
MJ	LED (Red)	Indicates NSCX power alarms or other software-defined major alarm
MN	LED (Yellow)	Indicates software-defined minor alarm
ACO	LED (Yellow)	Indicates NSCX alarms are cut off
ACT	Pushbutton Switch	When both ACT and RES pushbuttons are simultaneously pressed, (1) Initiates a complete NSCX initialization (2) Tests all display lamps
ACO	Rocker Switch	Alarm cutoff switch
RES	Pushbutton Switch	(Same as ACT switch function)

Table B. TN680 Power Switch and Control Circuit Pack — Controls and Indicators

Name	Type	Function
PF	LED (Red)	Indicates power failure of circuits monitored by this pack
ON	Pushbutton Switch	Starts power-up sequence if all alarm conditions have been reset by the off switch
OFF	Pushbutton Switch	Removes power from unit if OS is lighted or if MOR is also pressed. It also resets PF and ALM LEDs if power is removed.
OFF	LED (Red)	Indicates unit power is off
ALM	LED (Red)	Indicates unit power alarm or sequence parity error
OS	LED (Yellow)	Indicates this unit placed out-of-service by main processor
ACK	LED (Green)	Indicates main processor acknowledgement of TTY out-of-service requests
ACO	LED (Green)	Indicates unit alarm cut off
Test	Pushbutton Switch	(1) Performs lamp test of all LEDs except PF (2) If power is up and OS is lighted, initiates manual test of unit power monitor circuits—all PF LEDs in unit should light when switch is pressed, and extinguished when switch is released.
ACO	Rocker Switch	Unit Alarm cutoff switch
MOR	Pushbutton Switch	(Manual override) Unit is powered down when the MOR and OFF pushbuttons are simultaneously pressed, regardless of unit service status

Table C. UN356 Power Unit Circuit Pack — Controls and Indicators

Name	Type	Function
ON	Pushbutton Switch	Starts power-up sequence if all alarm conditions have been reset by the off switch
OFF	Pushbutton Switch	Removes power from unit if OS is lighted or if MOR is also pressed.
OFF	LED (Red)	Indicates unit power is off
PA	LED (Red)	Power Alarm
OS	LED (Yellow)	Indicates this unit is placed out of service by main processor
FA	LED (Red)	Fuse Alarm
LTEST	Pushbutton Switch	Performs lamp test of all LEDs
MOR	Pushbutton Switch	(Manual override) Unit is powered down when MOR and OFF pushbuttons are simultaneously pressed, regardless of unit service status

TN681 Power Failure Indicator

5.06 Each TN681 power control circuit pack contains a single panel-mounted LED labeled PF. When lighted, the PF LED indicates detection of an out-of-range voltage or overcurrent condition, and the associated power unit has been shut down. The TN681 PF LED and power monitor circuits are identical to the TN680 PF LED and power monitor circuits. The power monitor and distribution circuits of either type circuit pack can support up to eight functional circuit packs. One or more TN681 circuit packs (as required) are provided in each NSCX unit to supplement the power monitor and distribution circuits provided by the TN680 circuit pack.

Power Unit Controls and Indicators

5.07 Seven types of power units (495JA, 494G1, 131F1, 131J1, 131N1A, 130D, and 133K) are equipped in the various NSCX units. Each power unit contains an in-rush control circuit and a mechanically interlocked ON/OFF switch. The ON/OFF switch, when in the OFF position, permits the power unit to be safely inserted into a connector with –48 V present. The ON/OFF switch must be in the ON position to enable external power-up and power-down control of the power unit. When fully inserted into a connector, the 495JA and 494G1 power unit ON/OFF switches are automatically placed in the ON position. The ON/OFF switches on the 131F1, 131J1, 131N1A, 130D, and 133K power units must be manually placed in the ON position after the unit is fully inserted into a connector.

5.08 Each power unit contains a red LED which lights to indicate electronic shutdown of the power unit output voltage. The 494G1 and 495JA power unit also contains an LED and a pushbutton switch labeled ST. The LED and ST pushbutton switches are not used in the NSCX application.

Fuse Alarm Indicators

5.09 With the exception of one fuse, all fuses contained in the NSCX fuse panels are equipped with a plastic indicator. The plastic indicator protrudes from the end of the fuse to indicate a blown fuse. Two fuse positions designated TSI-B and TSIBNA in the network services frame fuse panel are wired in parallel to supply +12 V to the time slot interchange unit. The lower amperage TSI-B fuse (alarm-type) serves as a pilot fuse for the higher amperage nonalarm type TSIBNA fuse.

Disk Power Controls and Indicators

5.10 The inverter control unit in the moving head disk frame controls the application of AC voltage to the disk drive. This unit contains an ED-4C194 plug-in control unit which controls power to the moving head disk drive. Table D defines the function of the controls and indicators on the ED-4C194 control unit. A front mounted fuse provides –48 V power to the ED-4C194 control unit. Failure of this fuse results in the removal of AC power from the disk drive.

5.11 A covered ON/OFF switch on the KS-22072 moving head disk drive may be used to start or stop the disk drive for disk pack replacement.

Table D. ED—4C194Control Unit — Controls and Indicators

Name	Type	Function
ON	Pushbutton Switch	Applies power to disk inverter control circuits
OFF	Pushbutton Switch	Removes power to disk inverter circuit if OS is lighted or if MOR is simultaneously pressed.
OFF	LED (Red)	Indicates control unit and disk drive power is off
ALERT	LED (Red)	Indicates failure of cooling fan in disk file inverter
OSS	LED (Orange)	Indicates data storage unit placed out of service by main processor
RQIP	LED (Green)	Not used
ROS	LED (Green)	Not used
ROS/RST	LED (Green)	Not used
ACO/T	Rocker Switch	Unit Alarm cutoff and lamp test switch
MOR	Pushbutton Switch	(Manual Override) Unit is powered down when MOR and OFF pushbutton are simultaneously pressed, regardless of unit service status

6. Power

Introduction

6.01 The majority of NSCX units share a common power design that provides the following major features:

- Power is derived from –48 V using FASTECH power unit circuit packs.
- Power units are automatically shut down for fault protection.
- Each unit (or functional unit group) except the 2 GB Hard Disk Unit has an individual TN680 power switch and control circuit pack.
- Each unit power control circuit communicates power status to the main processor.
- Each unit power control circuit provides clamping outputs to protect the NSCX common bus during unit fault and power cycling intervals.
- Indicators are provided to help localize any detected power fault.

6.02 The following rules must be applied when assigning NSCXs to power distribution frames:

- Each power distribution frame distributes –48 V power from two primary buses (A and B). The even numbered NSCXs must be powered from the A bus, and the odd numbered NSCXs must be powered from the B bus.
- A maximum of eight NSCXs (four on each bus) may be powered from each power distribution frame.
- No more than two NSCXs of the same type or one-half the NSCXs of that type, whichever is less, may be powered from a single bus (A or B) of any power distribution frame.
- The assignment of NSCXs for the same type of service should be spread (as much as possible) over all of the power distribution frames.

NSCX Power Requirements

6.03 Each NSCX frame requires one or two –48 V power feeders from a J86334B-1 or J86334C-1 power distribution frame (Figures 42 and 43). The J86334B-1 power distribution frame is required for use with –48 V battery plants. The J86334C-1 power distribution frame is required for use with +140 V to –48 V converter plants. In addition, the moving head disk frame requires 208 V 60-Hz from the office essential AC source.

6.04 The moving head disk drive requires an uninterrupted source of 208 V AC for proper operation. Disk drive power is normally supplied from the office essential AC power source via the inverter control unit. In the event of essential AC power interruption, undervoltage condition, or 60-Hz frequency deviation, disk drive power is automatically supplied by the –48 V to 208 V AC disk file inverter. The disk drive must be started from the 208 V essential AC source since the –48 V power feeder to the inverter is not fused for this purpose. Disk drive startup is accomplished by removing the –48 V fuse on the disk file inverter and pressing the inverter control unit ON pushbutton. After startup, the –48 V fuse is returned to the fuse holder to enable the inverter.

6.05 Each of the other NSCX frames require two –48 V power feeders from the power distribution frame. The power feeders to each frame are connected to a fuse panel via a filter unit located in the base of the frame. The –48 V is then distributed to the various DC-to-DC power converter units within the frame via alarm-type fuses in the fuse panel. The ASR cabinet requires two –48V DC feeders from the power distribution frame.

6.06 A 131N1A type power unit in the network services frame fuse panel supplies unswitched +24 V to the two data sets in the maintenance interface unit. The 495JA, 494G1, and 131J1 type power units provide switched +5 V, –5.2 V, and +12 V, respectively, to the associated logic circuits.

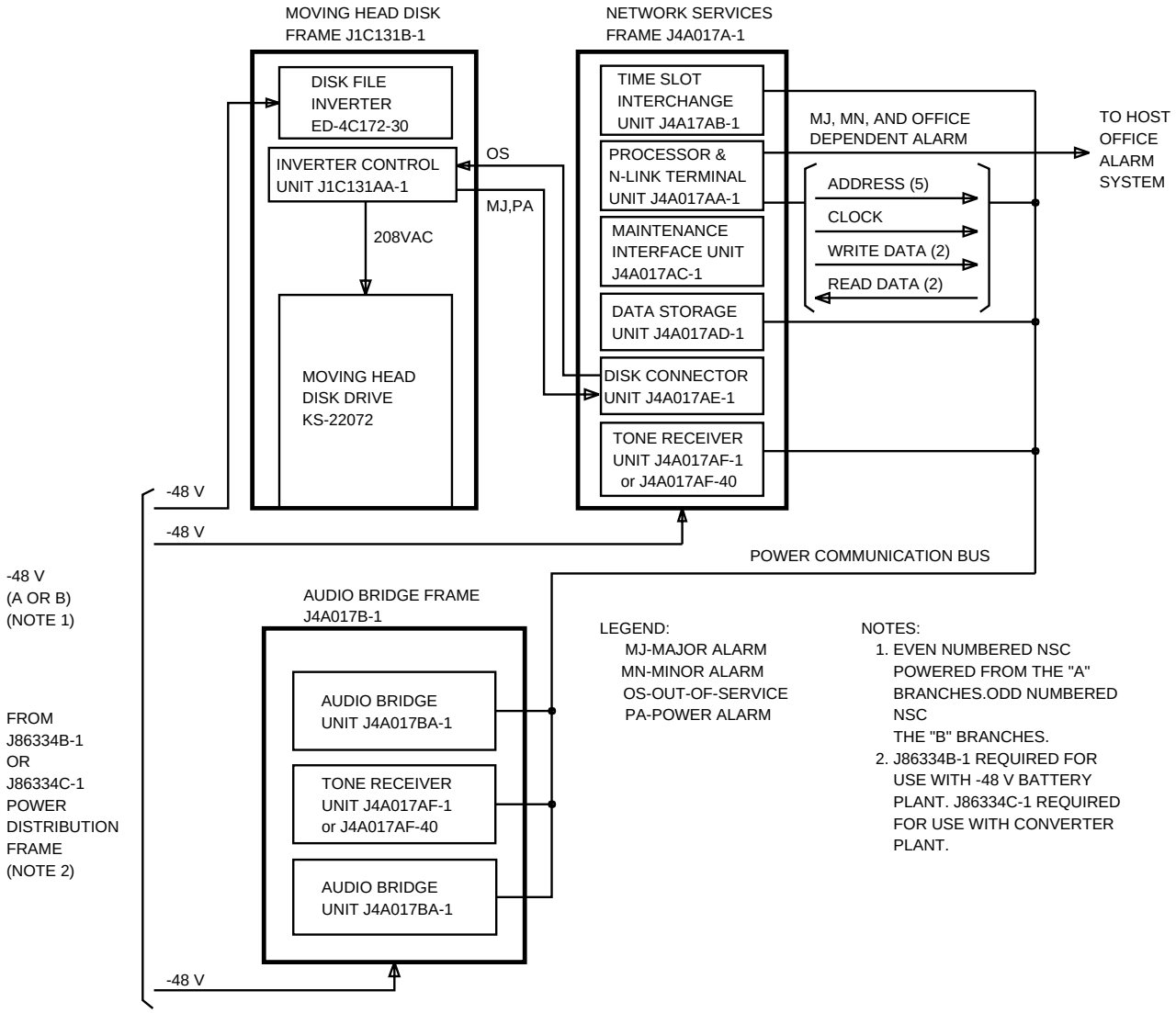


Figure 42. Voice-Only or Voice Analog Graphics Teleconferencing Network Services Complex Power Distribution and Alarms — Functional Block Diagram

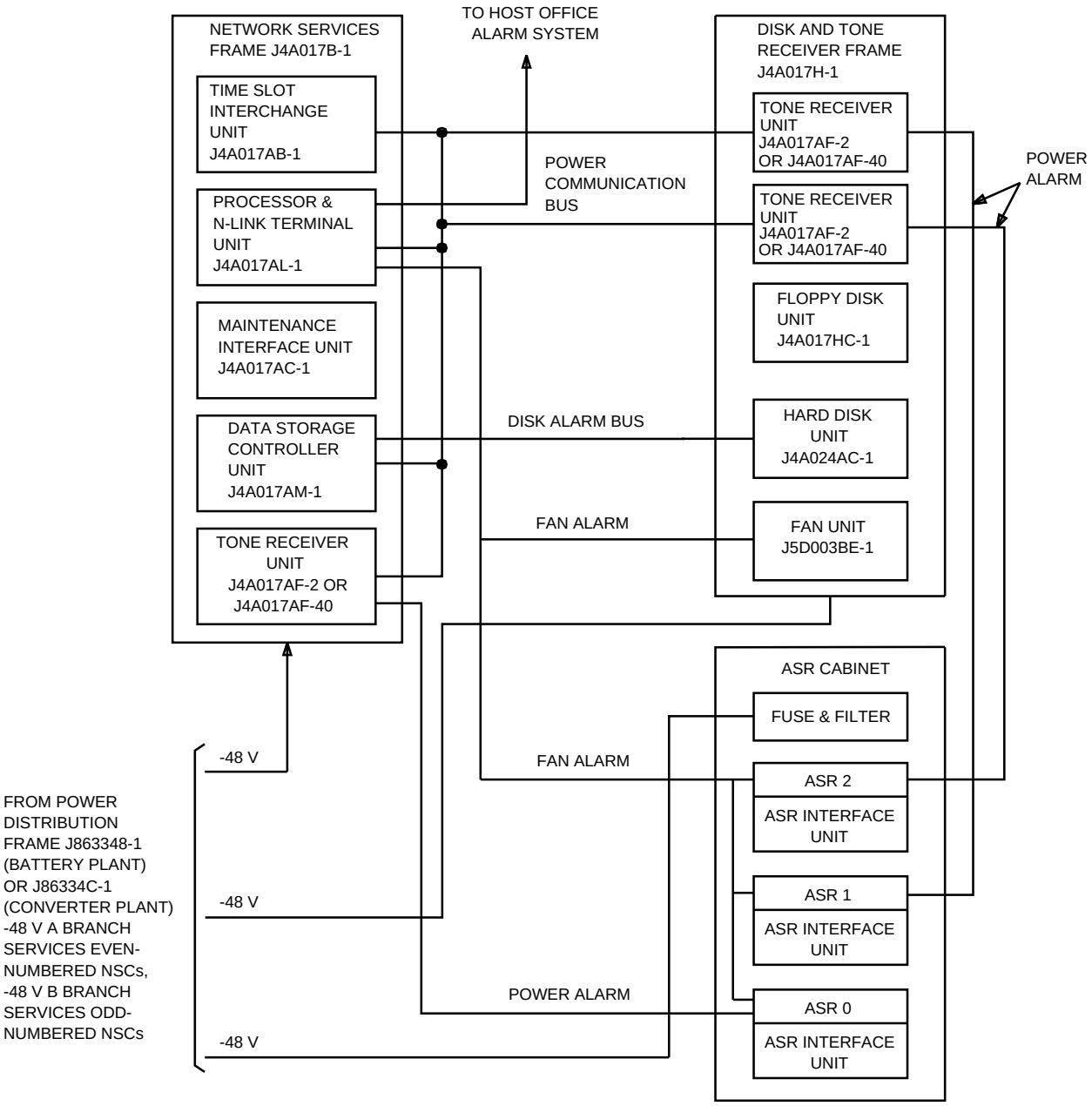


Figure 43. Direct Services Dialing Capability NSCX Power Distribution and Alarms — Functional Block Diagram DSD8 or Later Generic

Power Control and Alarms

6.07 Power to the logic circuits in each NSCX unit is controlled by one TN680 power switch and control circuit pack located in each functional unit except for the 2 Gbyte Hard Disk Unit. Each 2 Gbyte Hard Disk Unit contains two UN356 Power Units. Unswitched operating voltage (+12 V) is supplied to each TN680 circuit pack so that the power switch indicators will operate correctly when the unit is in the power-down condition. The controls and indicators on the TN680 circuit pack are defined in Table B. The controls and indicators on the UN356 Power Units are defined in Table C. A program-controlled sequencer in each TN680 circuit pack controls the manual power-up sequence and manual or automatic power-down sequence of the associated unit. It also monitors the output of the associated Power Failure (PF) voltage and current monitoring circuits contained in both the TN680 and TN681 circuit packs.

6.08 All NSCX TN680 circuit packs and UN356 Power Units are connected to the main processor (processor and N-link terminal unit) via a power communication bus (Figures 42 and 43). This bus allows the main processor to control the Out-Of-Service (OS) and Acknowledge (ACK) lamps on all TN680 circuit packs. It also allows the main processor to run unit power monitor tests and to receive power status and alarm information. The power communication bus consists of five unit address leads, a clock lead, two write data leads (ACK and OS), and two read data leads. The main processor sequentially addresses each unit and reads the power status and/or alarm indications over the two read data leads on a continuous time-shared basis. The ACK and OS write data leads are also used by the main processor to initiate a unit power monitor test. Power monitor test results are reported to the main processor via the two read data leads.

6.09 The major alarm and power alarm outputs from the moving head disk frame are connected to the data storage unit. The data storage unit periodically scans the major alarm output and, when active, registers the major alarm in an Error Source Register (ESR). The power alarm output is monitored only during diagnostics. Alarms registered in the data storage unit ESR are reported to the main processor via the NSCX serial communication bus.

6.10 The ASR power alarms are connected to the corresponding tone receiver unit power control circuit packs. A power alarm on an ASR unit will appear on the tone receiver TN680 and be reported to the NSCX as a tone receiver power failure.

6.11 The main processor in the processor and N-link terminal unit reports NSCX major alarms, minor alarms, and office-dependent alarm conditions to the host office alarm facilities. The NSCX office-dependent alarm output is used to generate the appropriate alarm message in the host office.

Manual Power Monitor Test

6.12 A manual power monitor test may be performed while the unit is in the OOS state. When the unit is in service (OS lamp off), the manual power monitor test is inhibited. The manual power monitor test is initiated by depressing the TEST switch and observing that all PF lamps on the unit light and remain lighted. The sequencer advances through two test states while the TEST switch is depressed. Releasing the TEST switch returns the sequencer to the OOS state and extinguishes the PF lamps.

Programmed Power Monitor Test

6.13 When the unit is in service, the main processor will run a programmed power monitor test by properly sequencing the OS and ACK lamps when DGN Phase 1 is requested on a unit. The sequencer is advanced through several test states by the OS and ACK lamp sequence. The OS lamp is turned on first, followed by the ACK lamp. Both lamps are then turned off to terminate the test and return the sequencer to the in-service state. Test results are monitored via the

two power communications bus read bits (scan 1 and scan 0) during the sequenced test states.

7. Maintenance

Introduction

7.01 The NSCX is designed with simplex units using a modular architecture which is loosely coupled to a host Stored Program-Controlled System (SPCS) office. Many NSCXs are installed nationwide to support each type of service. The NSCXs are connected to the host office using DS1 trunks and two signaling links (N-links). Since the NSCX is loosely coupled, it must rely heavily on self-testing and diagnostics which are independent from the host SPCS.

7.02 The primary system maintenance objective is the maintenance of service during error and/or fault intervals. Since each NSCX consists of simplex units, new service for a faulted NSCX is normally inhibited during fault intervals. Established conferences will be maintained via a faulted NSCX (when possible). Service originations must be routed to other NSCXs of the same type. The service of a faulted NSCX is completely inhibited once the established conferences are terminated. To meet the system maintenance objective, the following items are accomplished in relation to the NSCX:

- Detection of faults and errors
- Alerting operating personnel via TTY error message
- Maintaining established conferences during a fault condition (when possible)
- Inhibiting new service originations
- Isolate faulty equipment and remove it from service via program control
- Diagnose fault by manually-initiated diagnostic programs after NSCX service is inhibited
- List the suspected faulty circuit pack(s) via TTY
- Repair equipment (operating personnel)
- Verify repair by diagnostic and operational test programs
- Return repaired equipment to service.

7.03 Operating personnel are alerted to fault and/or error conditions by office alarms and TTY error messages. Hourly machine service and performance reports may also indicate error conditions of a transient nature.

Maintenance Software

A. NSCX Frame Routine Exercise

7.04 The NSCX unit diagnostics should be run at least once a week. This can be accomplished by removing the frame from service, or it can be done automatically. The diagnostics will catch faults that may develop in the hardware error detection circuitry or catch any faults that may be missed by the in-service Routine Exercises (REX).

7.05 Automatic frame routine exercise can be enabled by typing certain messages when bringing the frame up. When the chosen time arrives, the NSCX software will remove the frame from service, run all diagnostics, run an INIT:LEV 3, and allow service. Before service is allowed, the NSCX clock must be set. This is done under REX control, the 3B APS is requested by the NSCX REX software to send a SET:CLK command. It is done this way so the entire REX function requires no manual intervention if no faults are present. If a fault is found, the NSCX must be restored to service manually. To automate the routine exercise, use the following messages:

- LOAD:REXTIME
- ALW:REXTIME

B. Individual Unit Routine Self-Test

7.06 Individual units in the NSCX may schedule routine self-test exercises internally, work permitting, to detect hardware and software errors. Errors are reported to the main processor via the serial communication bus. Error reports are then provided via the (IOP) TTY ports.

Hardware Errors

7.07 An error report and/or a unit power alarm report is produced when a hardware error is detected. A power alarm report accompanied by a major or minor office alarm is generated whenever the main processor unit power bus hardware detects an NSCX power problem. An error report accompanied by a major or minor office alarm is generated when hardware problems other than power alarms are detected. Hardware errors may cause units to be automatically taken out of service. If some service can still be provided, the NSCX will be left operational. When not enough units remain to continue service, the inhibit service sequence will be started to stop all new originations. If a hardware failure causes total loss of service, a major alarm is generated, and the NSCX will be immediately put in the service-inhibited state (if possible). Manual repair actions are required to restore an NSCX to service when any hardware failure causes a complete loss of service.

Fan Errors

7.08 Initial fan failure in an NSCX complex will report a fan error. Subsequent fan failures will not be reported.

Software Errors

7.09 Software errors such as mutilated data or memory protection problems also result in error report messages. The message contents indicate the nature and severity of the problem. Those problems that do not destroy calls or billing information are accompanied by a minor office alarm. When the number of software errors exceed a specific threshold, the system integrity program will automatically run a level 1 initialization. All critical data structures in memory are audited so that data mutilation errors can be neutralized. Further software errors will cause system integrity to escalate to a level 2 initialization. All data structures associated with transient calls are reinitialized. Stable teleconferencing calls are not affected. However, DSDC calls are not saved because they are of short duration. When a complete loss of NSCX software sanity occurs, manual action is required for repair and restoration to service.

C. Diagnostic Tests

7.10 Diagnostic tests must be manually initiated and can be run only when the NSCX is in the service inhibit state. Frame routine exercise diagnostics are run once each week.

7.11 Diagnostic capabilities include the following features:

- Early termination when a test failure is detected
- Phase repetition for main processor or main processor resident diagnostics
- Output of first five failures of any failing phase (all diagnostic results of every phase may be optionally requested)
- Diagnostic execution may be manually aborted at any time
- TTY request option provided for generation of faulty pack list
- Full NSCX diagnostics run via restore to service TTY request.

D. System Initialization

7.12 Initialization level 1 or level 2 can be invoked automatically due to excessive errors. Initialization level 3 completely initializes an NSCX and can only be triggered by manual action. Any of the three levels can be initiated by the appropriate input message. A level 3 may also be activated by pressing the Reset (RES) and Activate (ACT) pushbuttons on the NSCX control and display panel. The level 3 is designed to reset the entire NSCX regardless of machine state. It is used after

installation of an NSCX and any time the software is to be completely changed.

Routine Measurement Reports

7.13 An Machine Performance Report (MPR) and an Machine Service Report (MSR) are generated hourly by the NSCX if they have been manually allowed. The MPR provides peg counts of machine performance and irregularities. The MSR provides peg counts of NSCX failures relating to the service provided.

Standard Maintenance Functions

A. Configuration

7.14 The service provided by an NSCX may be inhibited or allowed, as indicated by the state of the SVC lamp on the TN678 display panel in the processor and N-link terminal unit. When service is inhibited, no traffic is being handled, and all trunks are blocked. When service is allowed, the trunks are unblocked, and the NSCX can handle calls. A TTY input message is used to allow the NSCX to handle traffic. If the appropriate NSCX units are in-service [Out-of-Service (OS) lamps extinguished] so that some service can be provided, then all trunks are unblocked. This condition is indicated by an output message and the TRKS (trunks) blocked lamp on the TN678 display panel. If no service can be provided, the request to allow service is denied. This condition is indicated by a TTY output message.

7.15 A TTY input message is also used to inhibit NSCX service. The inhibit service action is started immediately by blocking all idle trunks as indicated by the TRKS lamp and a TTY output message. This action has no effect on trunks in the setup or stable state. However, no new conferences can be initiated or set up, but it is possible to add new legs to an existing conference. A TTY message accompanied by a spurt minor alarm is generated when all active calls hang up and NSCX service is inhibited.

7.16 Normal TTY configuration requests (remove and restore) are executed only if service is inhibited. When a normal restore request is typed in, diagnostics are run on the unit, and the unit is restored if the diagnostic test is successful. The restore is denied if the diagnostics fail. An unconditional restore request while service is inhibited results in immediate restoral without diagnostics. An unconditional restore request is denied if service is allowed. A normal remove request places the unit in the out-of-service state where it can be powered down without using the manual override. An unconditional remove request while service is allowed is executed only if the action leaves the NSCX in a state where it can provide service.

B. Control and Display

7.17 The primary NSCX control and display facility is provided by two IOP ports (A and B). Other control and display facilities include:

- Major and minor alarms and office-dependent alarms output to the host office alarm facilities
- TN678 display panel
- TN680 power switch and control circuit packs
- UN356 Power Unit
- Unit PF indicators
- Power unit alarm indicators
- Fuse alarm indicators.

7.18 The function of the unit power switches (TN680 and UN356 circuit packs) is limited to power control, alarm retire, and lamp display of unit power and maintenance status. An interlock is provided to prevent accidental removal of power from an in-service group. The interlock can be overridden when the manual override and power-off pushbuttons are simultaneously pressed.

C. Disk Change and Update

7.19 For all Teleconferencing (TC) NSCXs the NSCX disk pack contains announcements and NSC data storage, including a copy of the NSCX generic program. The announcements provide instructions and information when a particular service is accessed. It is necessary to occasionally add, delete, or modify these announcements. The Operations Network Administration Center (ONAC) is responsible for providing the initial disk pack to each NSCX containing the appropriate service announcements. The ONAC also provides disk packs to each NSCX for large announcement updates and generic software updates. Announcement updates are accomplished via the T1 lines under the control of the NSCX maintenance TTY. For DSD NSCXs with DSCs, the disk packs are not removable. The disks are paired, and if one fails, a copy can be made from the other disk. If both fail, the Advance Feature Service Center (AFSC) will ship new units to the site.

D. Routine Tasks

7.20 The procedure for performing any routine task at the NSCX is provided in the appropriate Task Oriented Practice (TOP).

E. Repair and Replace Tasks

7.21 Repair and replace tasks to be performed at the NSCX are provided in the appropriate TOP or are covered in training.

8. References

8.01 The following listing identifies documents which contain information concerning the NSCX. Refer to the latest AT&T numerical index for document availability.

- AT&T 254-301-210, Moving Head Disk Drive - General Description
- AT&T 256-041-500, Task Oriented Practice - Network Services Complex
- AT&T 592-033-100, 2201D-Type Data Set - Identification
- AT&T 592-040-120, Private Line Data Sets 2024, 2048, and 2096 - Description and Operation
- AT&T 592-040-220, Private Line Data Sets 2024, 2048, and 2096 - Installation and Connections

Abbreviations and Acronyms

This part defines the abbreviations and acronyms used in this practice.

AB	Audio Bridge
ACK	Acknowledge
ACP	Action Control Point
ACT	Activate
ADPCM	Adaptive Differential Pulse Code Modulation
AFSC	Advance Feature Service Center
ANSI	American National Standards Institute
ASCII	American Standard Code for Information Interchange
ASR	Automatic Speech Recognition
BC	Buffer Control
BF	Buffer Fabric
CAU	Centralized Announcement Update
CBI-16	Common Bus Interface for 16 Bits
CBI-FE	Common Bus Interface - Front End
CCIS	Common Channel Interoffice Signaling
CRC	Cyclic Redundancy Check
CSDC	Circuit Switched Digital Capability
DDD	Direct Distance Dialing
DIF	Digital Interface
DMA	Direct Memory Access
DS1	Digital Service 1
DSC	Data Storage Controller
DSD	Direct Services Dialing (Frame)
DSDC	Direct Services Dialing Capability
DSU	Data Storage Unit
DSX	Digital Cross-Connect
DTR	Disk and Tone Receiver (Frame)
EMC	Electro-Magnetic Compatibility
EPIC	Enhanced Peripheral Interface Controller
EPROM	Erasable Programmable Read-Only Memory
ESR	Error Source Register
GPIB	General Purpose Interface Bus
HA	Host Adapter
HDLC	High-Level Data Link Control
IEEE	Institute of Electrical Electronic Engineers
IOP	Input/Output Processor
MPR	Machine Performance Report
MSR	Machine Service Report
NSCX	Network Services Complex
NCP	Network Control Point
NS	Network Services (Frame)
ONAC	Operations Network Administration Center
OS	Out-of-Service
PCM	Pulse Code Modulation
PF	Power Failure
PIC	Peripheral Interface Controller
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
RES	Reset
REX	Routine Exercise
ROM	Read-Only Memory
RTMDB	Receive Time Multiplexed Data Bus
SCB	Serial Communications Bus
SCSI	Small Computer System Interface

SPCS	Stored Program Controlled System
SYU	Synchronization Signal Unit
TMB	Time Multiplex Bus
TOP	Task Oriented Practice
TR	Table RAM
TSC	Time Slot Count
TTMDB	Transmit Time Multiplexed Data Bus
UART	Universal Asynchronous Receive-Transmit
VFL	Voice Frequency Link
VP	Voice Processor
VPIC	Voice Processor Interface Controller

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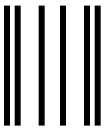

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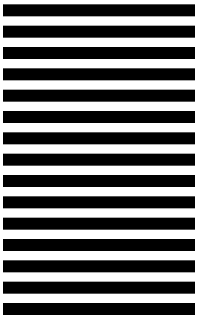

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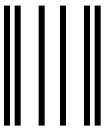

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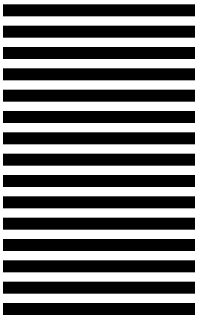

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