SETUP AND OPERATION OF THE ITE-5511 MICROCONTROL TEST SET

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1. GENERAL INFORMATION

1.1 This section provides operating instructions for the various control and display functions available when using the ITE-5511 3ACC Microcontrol Test Set. This information supplements the basic description of test method of operation contained in TMO-5511. The TMO also contains a checkout procedure if the test set is suspected of having a malfunction.

1.2 This test set is designed as an aid in diagnosing hardware and software problems which inhibit both CUs from bootstrapping test tapes into any system using the 3ACC. It provides several useful functions such as compare stop on the MAR, compare stop on an error condition, load the MIR (and execute crosspoints), step the clock or step the program, provides an eight-level transfer facility on the MAR register, or run the CC on the test set (slow) clock. The test set also provides useful displays of the gating bus, clock phases, MAR, MIR, and some control and error flip-flops.

2. TYPICAL CONTROL FUNCTIONS WITH OPERATING INSTRUCTIONS

2.01 Disable all Test Set Outputs to the Control Unit

2.011 Place the MODE switch in the RUN position.

2.012 Place the BLK ERR switch down. BLK ERR lamp should be off.

2.013 Place the RST CKTS switch in the center position. The RST CKTS lamp should be off.

2.014 Place the CONTROL STATE MATCH switch in the STOP position.

2.015 Place the MAR MATCH switch in the STOP position.

2.02 Enable Test Set Outputs to the Control Unit without Affecting System Operation

2.021 To enable the Micro Store Address (MAR) match circuits operate the MAR Match switch to the ENABLE (up) position.

2.022 To enable the Control State Match circuits operate the Control State Match switch to the ENABLE (up) position.

2.023 To enable the test set STEP, CYCLE, and LOAD functions and to enable the test set's internal timing circuits, operate the MODE switch to the TEST (up) position. With the MODE switch in this position the test set clock, 6 usec cycle, is used instead of the system clock, 150 nsec cycle.

2.03 Initialize the Control Unit

2.031 The three-position RST CKTS switch is used to initialize the Control Unit. With the switch in the off (center) position there is no output from the test set. Operating the switch up (on) will provide a constant initialization signal to the Control Unit. The RST CKTS lamp will be on. The down (momentary) position will initialize the Control Unit and allow it to start. To properly initialize the Initialization Sanity Check bits (ISC) in the System Status Register, it may be necessary to operate the RST CKTS switch to the down (momentary position) three times in succession. It may also be necessary to manually zero main store address 40 (octal) from the CC control panel to get the CC to start properly.

2.04 Sync on MAR Address

2.041 To obtain a sync pulse on a particular MAR address, set the MICRO STORE ADDRESS switches to the desired address (center position is "don't care"). Operate the P2 STROBE switch up and P0, P1, and P3 down. When the MAR address in the Control Unit matches the switches a negative sync pulse is produced on the MAR MATCH SYNC jack.

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2.05 Sync on Control State

2.051 To obtain a sync pulse on a particular error condition or on a particular configuration of the control flip-flops set the appropriate Control State switches to either the "0" or "1" position. Other switches should be in the center (don't care) position. Set the Strobe switch up (P0-P3) for the clock phase during which the match is expected to occur. If the clock phase is unknown set all Strobe switches up. A negative sync pulse will now be produced on the Control State Match Sync jack each time the CC flip-flops match the state of the test set match switches during the clock phase or phases indicated by the position of the strobe switches.

2.06 Stepping the Clock

2.061 To advance the clock one-half a clock phase set the MODE switch to TEST and operate the STEP pushbutton. Since the clock is advanced one-half a clock phase for each push of the STEP pushbutton, it will take eight pushes of the STEP pushbutton to advance the clock one full cycle. The Clock lamps (P0-P3) indicate which clock phase is active. There should be only one clock phase active at a time.

2.07 Stepping the Program

2.071 "Stepping the program" is a phrase used to describe the function which allows the CC to advance through its micro program one instruction at a time. In our case we will be advancing the CC one clock cycle at a time and thus step through the program one microinstruction at a time.

2.0711 Disable test set outputs as described in paragraph 2.01.

2.0712 Operate the CYCLE switch to the SNGL position.

2.0713 Operate the LOAD switch to the OFF (down) position.

2.0714 Operate the MODE switch to the TEST position. Note the SNGL lamp is on.

2.072 Each operation of the CYCLE pushbutton will now advance the CC one clock cycle.

2.073 To allow the CC to run continuously operate the CYCLE switch to the CONT position (CONT lamp on) and operate the CYCLE pushbutton.

2.08 Compare Stop on Microstore Address Register (MAR)

2.081 The MAR compare circuits work independently of the MODE switch and may be used with the test set in RUN. To stop the CC when a particular microstore address is reached:

2.0811 Set the desired address in the MICRO STORE ADDRESS switches.

2.0812 Set the TRANSFER TRACE FREEZE switch down (FREEZE lamp off).

2.0813 Operate the CLR pushbutton.

2.0814 Rotate the TRANSFER TRACE rotary switch to the "1" position.

2.0815 Operate the MAR MATCH switch to the ENABLE (up) position (ENABLE lamp on).

2.082 If the machine was not running it can be started using the CYCLE function (paragraph 2.073) if MODE switch is in the TEST position.

When the MAR in the CC matches the information in the test set MAR keys the CC will be stopped and the test set will switch to the TEST mode. The MAR lamps will display the CURRENT microstore address and the previous (TRACE) address.

2.09 Compare Stop on Control State

2.091 A Control State is defined as a combination of control and error flip-flops. To stop the CC on a particular control state:

2.0911 Set the CONTROL STATE match switches to the desired positions (note that the center is a don't care position).

2.0912 Set the STROBE switches up for the clock phase(s) during which the control state is expected.

2.0913 Operate the CONTROL STATE MATCH switch to the ENABLE (up) position.

2.0914 Start the CC using the CYCLE or the RST CKTS function.

2.092 Example: To stop the CC when the CF gets set during clock phase P2 proceed as follows:

2.0921 Set the CF switch to the "1" (up) position and all other switches in this group to the center (don't care) position.

2.0922 Set STROBE switch P2 up and P0, P1, P3 down.

2.0923 Set the MATCH switch up (ENABLE) and start the CC.

2.093 Whenever the CC control and error flip-flops match the information in the control state and STROBE switches the CC will be stopped and the test set will switch to the TEST mode.

2.10 Transfer Trace on the Microstore Address Register

2.101 The test set has the capability of saving the last eight microstore addresses which the CC has accessed. The test set contains a 12-bit, 8-word memory to provide this capability. To trap the last eight microstore addresses accessed by the CC proceed as follows:

2.1011 Perform a "Compare Stop on Microstore Address Register" as described in paragraph 2.08 of this section.

2.1012 When the CC stops the CURRENT lamps on the test set will display the most recent MAR address accessed by the CC. The TRACE lamps will contain a display of the previous microstore address. Rotating the TRANSFER TRACE rotary switch thru positions 2 - 7 will cause the previous microstore addresses to be displayed in the test set lamps.

NOTE: Operating the TRANSFER TRACE FREEZE switch up at any time will prevent the contents of the test sets transfer trace memory from being changed.

2.11 Troubleshoot Stuck Bits on the Bus

2.111 The test set provides a display of the 20-bit (plus parity) bus in the CC. This display is used in conjunction with the start-up procedures for test programs. The CC is set to a condition such that the bus should contain all zeroes. The display will quickly indicate the bits that are stuck to a one condition.

2.112 Since the test set has access to the MIR another method of checking for stuck bits on the bus is available. This second method involves setting up the test set to gate the information in the Next Address (NA) field of the microstore output onto the bus. The procedure follows.

2.1121 Set the MICRO STORE OUTPUT FROM switches to octal 344 (MIRL8).

2.1122 Set the MICRO STORE OUTPUT TO switches to octal 360 (no operation).

2.1123 Set the CB switch down (zero).

2.1124 Set the CA switch up (one).

2.1125 Set the MODE switch to TEST.

2.1126 Set the LOAD switch up.

2.1127 Set the CYCLE switch to CONT.

2.1128 Operate the CYCLE pushbutton. The CC is now gating whatever information is in the test set NA switches onto the low eight bits of the bus. The low eight bits of the bus can now be checked by changing the NA switches and verifying that the bus display lamps (Bits 0 - 7) are an exact duplicate of the NA switches.

2.1129 To check the upper twelve bits of the bus change the information in the FROM switches to octal 341 (MIRH12). The NA field will now be gated to the upper twelve bits (8-19) of the bus.

2.1130 Check the upper twelve bits of the bus as in paragraph 2.1127.

2.12 Execute Crosspoints, Load Registers

2.121 Since the test set can load information into the Microinstruction Register (MIR) the test set has the capability of forcing the microcontrol to execute any command (crosspoint). There are two methods for executing crosspoints. The first method allows one execution of the crosspoint, the other method allows the crosspoint to be executed in a repetitive fashion.

2.122 To execute a crosspoint from microstore:

2.1221 Set the NA switches to the microaddress of the desired crosspoint.

2.1222 Set the CB and CA switches to 00.

2.1223 Set both the TO and the FROM switches to octal 360.

2.1224 Put the test set in TEST mode and step the clock (see paragraph 2.06) to clock phase P2.

2.1225 Put the CYCLE switch to SNGL.

2.1226 Put the LOAD switch up.

2.1227 Operate the CYCLE pushbutton twice to load the MAR.

2.1228 Set the LOAD switch down, set the CYCLE switch to CONT or SNGL.

2.1229 Operating the CYCLE pushbutton will start the CC at the microstore address that was in the NA switches. The CC will either run one cycle or continuously depending on the position of the CYCLE switch.

2.123 To execute a crosspoint from the test set switches:

2.1231 Set the CB and CA switches to 00.

2.1232 Set the NA switches to octal 360.

2.1233 Set the TO and FROM switches to the proper 4/8 codes for the microinstruction to be executed.

2.1234 Put the test set in the TEST mode.

2.1235 Set the LOAD switch up.

2.1236 Set the CYCLE switch to CONT and operate the CYCLE pushbutton.

2.1237 The TO and FROM fields set in the test set switches are now being executed by the CC in a continuous (repetitive) mode.

2.13 Run the CC on the Slow (Test Set) Clock

2.131 Whenever the MODE switch is in the TEST position, clock for the CC is provided from the test sets clock circuit. The basic cycle time of the test set clock is 6 usec. Since the normal CC clock cycle is 150 nsec, running on the test set clock provides a 40 to 1 reduction in the speed of the CC.

2.14 FREEZE The Microstore Address (MAR)

2.141 It is sometimes useful to know what microstore addresses the CC is going through. An example would be if the CC were caught in a tight program loop,we can find what microstore addresses are being used by the CC.

2.1411 To trap the last eight microstore addresses accessed by the CC, operate the TRANSFER TRACE FREEZE switch up. This prevents the test set's transfer trace memory from being changed. The memory will contain whatever was in it when the switch was operated. The CC may now be stopped without losing the MAR information.

2.1412 The contents of the transfer trace memory may be displayed by rotating the transfer trace rotary switch thru positions 0 to 7. Position 0 is the most recent information and position 7 is the eighth most recent information.

ATTACHMENT
Figure 1 on page 5.

→ Arrows indicate new or changed information.

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Reason for Reissue:
Update and improve operating procedures.

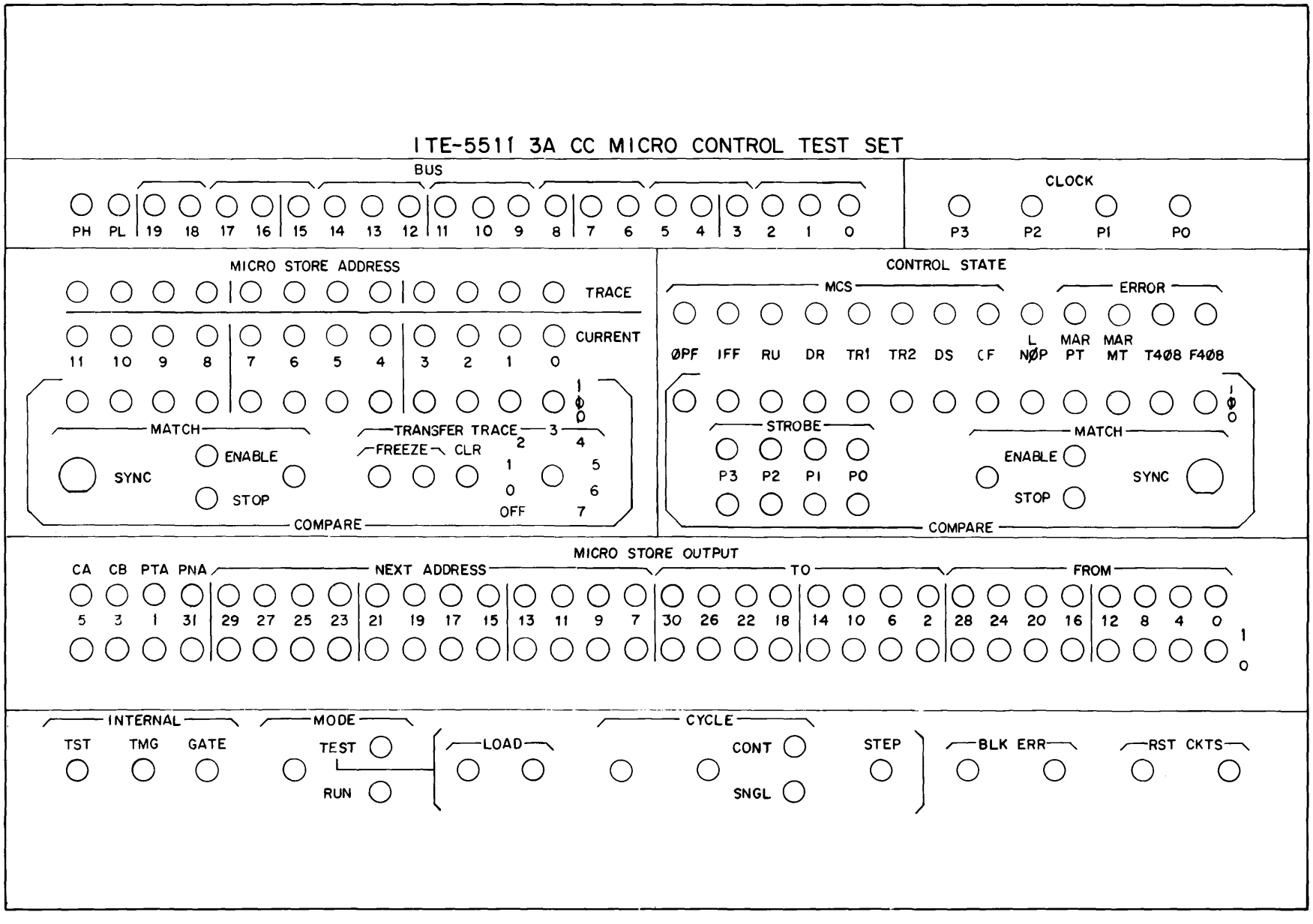

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FIG. 1