

DIMENSION® 600/2000 PBX
PROCESSOR INITIALIZATION CAUSES
(PROC 520)

1. GENERAL

- 1.1 This section is issued in order to make available the information contained in the Administration and Maintenance Manual, 500-497, PROC 520.
- 1.2 The attachment provided can be used to determine the cause(s) of the common control (processor) being initialized.

ATTACHMENT

PROC 520 (7 pages)

Reason for Issue:
Update

Manager, Denver PBX PECC

PRIVATE

THE INFORMATION CONTAINED HEREIN SHOULD NOT BE DISCLOSED TO UNAUTHORIZED PERSONS. IT IS MEANT SOLELY FOR USE BY AUTHORIZED BELL SYSTEM EMPLOYEES.

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PROCEDURE 520 - INITIALIZATION CAUSES

PROC 520

A. DESCRIPTION

Procedure 520 should be used when the NETWORK OTHER-515 and MINOR alarm indicators are turned on.

Procedure 520 is used to:

- Display the failures that caused the common control (processor) to be initialized.
- Clear all maintenance data in memory.

CAUTION

This procedure provides a special feature to clear all maintenance data in memory by entering a 9 into the Initialization Number field and using the CLEAR ENTRY; EXECUTE keys. This removes all failure indications that would normally be investigated with the procedure associated with the fault. Therefore, this procedure should not be used in normal troubleshooting activities.

There is no test selection in this procedure.

USE 'NEXT DATA' TO DISPLAY NEXT HIGHER INIT NO. USE 'NEXT UNIT' TO DISPLAY MORE THAN 2 CAUSES. USE 'CLEAR DATA', 'EXECUTE' TO CLEAR FAILURE HISTORY. CAUTION. SELECT INIT NO=9 AND USE 'CLEAR DATA', 'EXECUTE' TO ZERO ALL MAINTENANCE DATA. 9 IS ONLY VALID INPUT.	INIT CAUSE CODES: 1-SHORT POWER FAIL 2-MICRO PARITY 3-SANITY TIME OUT 4-I/O SANITY TIME OUT 5-MEMORY PARITY 6-BRANCH ALLOW 7-WRITE PROTECT 8-ILLEGAL OP CODE 9-MICRO PARITY PREDICT	10-BIT SWAP 11-ILLEGAL MICRO INSTR 12-DUPL CHAN XMIT 13-DUPL CHAN RCV 14-DUPL WRITE PROTECT 15-DUPL PARITY 17-DUPL ILLEGAL INSTR 21-LONG POWER FAIL 22-MICRO DIAGNOSTIC 9 23-HOLD GET AREA	24-BRANCH TO ZERO 25-INTERRUPT AREA 26-FALSE ID 27=2 PROCS ONLINE 28-PROCESSOR SUICIDE 29=5 SHORT INITS 30-DUPL MEM MATCH 31-PARITY AUDIT 32-XRAY PROCESSOR 33-XRAY MEMORY	34-MICRO DIAGNOSTIC 35-PROCESSOR SWITCH	PROCESSOR HEALTH: 0-PASS 1-BIT SWAP 2-SOFT A 3-LDFT B 4-HARDWARE
ISSUE 5 FLIPCHART	○	○	PROC 520	○	○

FLIPCHART ISSUE 5	○	○	INITIALIZATION CAUSES	○	○	PROC 520						
INIT NO	CAUSE 1	CAUSE 2	ADDRESS WHEN FAILED		FAILURE HISTORY				COUNT TO RELOAD	BIT SWAP BAD MEMORY BLOCK	P R O C E S S O R	
			MEMORY BLOCK	ADDRESS IN MEMORY BLOCK	FAILURES PER HOUR		FAILURE BEGAN (HOURS AGO)	MOST RECENT FAILURE				
1	2	3	4	5	6	7	HOURS AGO	MINUTES AGO	10	11	12	

1.	5.	-	-	7.	1	0	7	7	1.	9.	1.	1.	3	1.	4.	-	-	0.	520
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B. FIELD DEFINITIONS AND CODES

Field	Code	Definition
1		Initialization number:
	0	Summary.
	1-6	Different causes.
	9	Used only to clear all maintenance data (see paragraph A).
2, 3		Initialization causes associated with codes 1 through 6 in field 1:
	1	Short power failure.
	2	Micro memory parity.
	3	Sanity time out.
	4	Input/output time out.
	5	Memory parity.
	6	Branch allow.
	7	Write protect.
	8	Illegal operation code.
	9	Micro parity predict.
	10	Bit swap.
	11	Illegal micro instruction.
	12	Duplication channel transmit.
	13	Duplication channel receive.
	14	Duplication write protect.
15	Duplication parity.	
17	Duplication illegal instruction.	
21	Long power failure.	
22	Microdiagnostic Test 9 executed.	

Field	Code	Definition	
2,3 (Contd)	23	Hold get area overflow or underflow.	
	24	Branch to zero area.	
	25	Interrupt area.	
	26	False identification.	
	27	Two processors on line.	
	28	Processor suicide.	
	29	Five short initializations.	
	30	Duplication memory match failure.	
	31	Parity error during audit.	
	32	X-ray program detected processor failure.	
	33	X-ray program detected memory failure.	
	34	Microdiagnostic detected failure.	
	35	Processor switch.	
	4	0-17	Failed memory block location.
	5	0-17777	Octal address in memory block.
6	0-99	Failure Summary: Sum of approximate number of failures per hour.	
		Failure History: Approximate number of failures per hour.	
7	0-17 (odd numbers only)	Failure Summary: Number of hours since the oldest individual failure started (to the nearest hour).	

B. FIELD DEFINITIONS AND CODES (Contd)

Field	Code	Definition
7 (Cont)		Individual Failure History: Number of hours since the failure started in the displayed block location.
Number of hours plus minutes since: Failure Summary: Most-recent failure of any memory block. Failure History: Most-recent failure of the displayed memory block.		
8	0-136	Hours.
9	0-59	Minutes.
10	0-5	Initialization level, indicating the seriousness of the initialization causes.
11	0-17	Number of the memory block that caused a bit swap.
12		Processor health status:
	0	No failure.
	1	Bit swap.
	2	Software A failure: Minor.
	3	Software B failure: Possibly problem in switching processors.
	4	Hardware failure.

C. TEST PROCEDURE

The following is a description of what the initialization causes procedure does and how it is run follows:

Call in Procedure 520:

PROC NO.; 520; ENTER

A zero is displayed in field 1 and all other fields are dashed. Depressing EXECUTE takes a "snapshot" of the failure history and displays it on the MAAP. If one or more failures have occurred, the following is displayed:

Field	Contents
1	0, indicating initialization causes summary.
6	Total number of failures per hour.
7	Number of hours since any memory block failed.
8,9	Time elapsed since most recent failure.
12	Processor health status.

The failure summary displays all the initialization causes that have occurred.

C. TEST PROCEDURES (Contd)

Depressing the NEXT DATA key displays the most-recent initialization cause. The display includes the following:

Field	Contents
1	1, initialization number.
2,3	Initialization causes.
4,5	Memory block location.*
6	Number of failures per hour for location displayed.
7	Number of hours since failures began.
8,9	Time elapsed since the most-recent failure.
10	Number of initialization causes.
11	Dash.†
12	Processor health status.

* Only certain types of initialization causes display memory block locations. See Table 520-1.

† When an octal location is displayed in field 11, field 2 or 3 will have an encode of 10 and field 12 an encode of 1. Also, the PROCESSOR/MEMORY BIT SWAP indicator will be turned on.

Repeatedly depressing NEXT DATA sequences the display through the initialization numbers, in chronological order, until the last one is displayed. Depressing NEXT DATA again dashes the display. Depressing NEXT DATA once more starts the sequence over with an updated failure summary.

After a cause appears in field 2, depressing NEXT UNIT displays additional causes, if more than two were recorded.

Clear all maintenance data:

CAUTION

Using this operation removes all failure indications that would normally be investigated with the procedure associated with the fault. Therefore, this procedure should not be used in normal troubleshooting activities.

PROC NO.; 520; ENTER; CHANGE FIELD; 1; ENTER; 9; ENTER; CLEAR DATA; EXECUTE

The WAIT indicator turns off when the maintenance memory has been cleared (several seconds after depressing CLEAR DATA; EXECUTE). The MAAP displays a zero in field 1 (initialization number) and a zero in field 6 (failures per hour), indicating that the maintenance data has been cleared.

C. TEST PROCEDURES (Contd)

The only code that can be entered in field 1 is 9. Attempting to enter other codes causes an error code 03 to be displayed.

When Procedure 520 is loaded from tape or initialized by RESET, the special clear data feature can run without first depressing EXECUTE. Procedure 520 will advance to the normal mode of operation, displaying the initialization cause summary without clearing all maintenance memory.

D. REPAIR GUIDE

Initialization causes do not usually point to a faulty circuit pack. However, primary and secondary suspected circuit packs, or other possibilities that should be investigated are listed in Table 520-1.

This procedure affects the following circuit packs:

Circuit Pack	Description
LC28	RAM (random access memory) 8K.
LC128	RAM (16K).
LC346	RAM (64K).
LC35/LC135	RAM-A.
LC36/LC136	RAM data buffer.
LC37/LC137	RAM address and timing (8K).
LC138	RAM address and timing (16K).
LC454	RAM address and timing (64K).
LC133	Input/Output (I/O) and memory decode.
LC132/LC134	I/O buffer and termination.
LC142	Extended microstore.
LC143	201 CC processor.
LC455	201 CC processor w/extended microstore.
LC146	Duplicated control and I/O link.
LC147	Alarm.

D. REPAIR GUIDE (Contd)

Table 520-1. Initialization Cause Repair Procedure

Initialization		Memory Block Address OK	Primary Suspect	Secondary Suspect
Code	Cause			
Detected by Hardware				
1	Short power fail	No	Primary power dropout	
2	Microparity		LC143/LC455	LC142
3	Sanity time-out		LC143/LC455	Software
4	I/O sanity time-out		LC133	Software, LC132/134
5	Memory parity		LC28/LC128/LC346	Software
6	Branch allow		LC28/LC128/LC346	Software
7	Write protect		LC28/LC128/LC346	Software
8	Illegal OP code		Look for other cause	LC143/LC455
9	Microparity predict		LC143/LC455	LC142
10	Bit swap		LC28/LC128/LC346	LC35/LC135, LC36/LC136, LC37/LC137, LC143/LC455
11	Illegal micro Instruction	No	LC146	LC143/LC455, LC142 (off-line)
12	Duplicated Channel transmit	No	LC146	LC143/LC455, LC142 (off-line)
13	Duplicated Channel receive	No	LC146	LC143/LC455, LC142 (off-line)
14	Duplicated write protect	No	LC146	LC143/LC455, LC142 (off-line)
15	Duplicated parity	No	LC146	LC143/LC455, LC142 (off-line)
17	Duplicated illegal instruction	No	LC146	LC143/LC455, LC142 (off-line)
21	Long power Failure	No	Power Outage	Power supply
22	Microdiagnostic 9	No	Reloaded from Micro-diagnostic Test 9	

D. REPAIR GUIDE (Contd)

Table 520-1. Initialization Cause Repair Procedure (Contd)

Initialization		Memory Block Address OK	Primary Suspect	Secondary Suspect
Code	Cause			
Detected by Software				
23	Hold get area	No	Software	LC143/LC455
24	Branch to zero	No	Software	LC143/LC455
25	Interrupt area	No	Software	LC143/LC455
26	False ID	No	Software	LC143/LC455
27	Two Processors on-line	No	LC146, LC132/134	LC147, Alarm panel
28	Processor suicide		Look for other causes*	
29	Five short initializations	No	Look for other causes	
30	Duplicated memory match		LC28/LC128/LC346	LC146, LC143 (patches not in both machines)
31	Parity audit		LC28/LC128/LC346	LC143/LC455
32	X-Ray processor	No	LC143/LC455	LC142
33	X-Ray memory		LC28/LC128/LC346	LC142, LC35/LC135, LC36/LC136, LC37/LC137
34	Microdiagnostic	No	LC143/LC455	LC142
35	Processor switch	No	23-Hour switch	Manual switch, Procedure 521 (Test 3), system I/O failure
<p>* Processor suicide is caused by:</p> <p>Entering long initialization four times, two processors on line, or I/O failure in at least 75 percent of the cabinets.</p>				