DIMENSION® 2000 PBX
MEMORY MATCH TEST
(PROC 522)

1. GENERAL

1.1 This section is issued in order to make available the information contained in the Administration and Maintenance Manual, 500-497, PROC 522.

1.2 The attachment provides test procedures used to compare corresponding memory contents of a dual processor system.

ATTACHMENT

PROC 522 (8 pages)

Reason for Issue:
New Section

Manager, Denver PBX PECC

ISSUE 6 FLIPCHART

PROC 522 WORD 0

FLIPCHART ISSUE 6

MEMORY MATCH TESTS
THIS IS NOT A WORKING PROCEDURE

NOTES:
1. THE MEMORY MATCH TESTS (2-4) COMPARE THE CONTENTS OF CORRESPONDING LOCATIONS IN DUPLICATED COMMON CONTROLS. THE RANGE OF MEMORY TESTED IS RESTRICTED TO THE PROGRAM, PATCH AND TRANSLATION AREAS. TEST 5 IS NOT RESTRICTED AND ALLOWS THE CONTENTS OF MEMORY TO BE READ OVER THE FULL RANGE OF MEMORY.
2. MEMORY ADDRESSES AND CONTENTS ARE DISPLAYED IN OCTAL.

MEMORY AREA CODE (FLD 8):
1=PROGRAM ONLY
2=PATCH ONLY
3=PROGRAM & PATCH
4=TRANSLATION ONLY
5=PROGRAM & TRANSLATION
6=PATCH & TRANSLATION
7=PROGRAM, PATCH, TRANSLATION
8=OTHER (TEST 5 ONLY)

FAILURE CODE (FLD 9):
0=NO FAILURES
1=MEMORY MISMATCHES
2=PARITY ERRORS
4=DUPLICATION CHANNEL ERRORS

PROC 522

TEST 1: DISPLAY A FAILED MEMORY LOCATION. USE 'CLEAR DATA', 'EXECUTE' TO CLEAR FAILURE HISTORY.

TEST 2: TESTS MEMORY LOCATIONS, DISPLAYS SUMMARY AND RANGE OF MEMORY TESTED.

TEST 3: TESTS MEMORY LOCATIONS AND DISPLAYS RANGE OF FAILED BLOCK. DISPLAYS TYPE OF FAILURE AND MEMORY AREA FOR FAILED BLOCK. UPON TEST COMPLETION DISPLAYS TOTAL FAILED WORDS, MEMORY AREAS AND TOTAL FAILED BLOCKS. USE 'NEXT UNIT' TO ADVANCE TO NEXT BLOCK. USE 'NEXT DATA' TO DISPLAY CONTENTS OF FIRST MEMORY LOCATION IN ON-LINE CC, THEN FIRST MEMORY LOCATION IN OFF-LINE CC, THEN ADVANCE TO NEXT MEMORY LOCATION IN ON-LINE CC.

TEST 4: TESTS SPECIFIED RANGE OF MEMORY CONTINUOUSLY. USE 'STOP' TO DISPLAY RESULTS

TEST 5: READ THE CONTENTS OF ANY MEMORY LOCATION OR ANY RANGE OF MEMORY LOCATIONS. USE 'EXECUTE' TO DISPL CONTENTS OF FIRST MEMORY LOCATION IN ON-LINE CC. USE 'NEXT DATA' TO DISPLAY CONTENTS OF FIRST MEMORY LOCATION FOR OFF-LINE CC. SUBSEQUENT 'NEXT DATA' OPERATIONS FUNCTION AS IN TEST 3.

SPECIAL ERROR CODES:
74=COMMON CONTROL NOT DUPLICATED
80=LOCATION OUT OF MEMORY RANGE
81=WAIT UNTIL OFF-LINE CC LOADED
82=USE PROC 520 OR PROC 521 TO CLEAR FAILURE

ISSUE 5 FLIPCHART

PROC 522

FLIPCHART ISSUE 5

MEMORY MATCH TESTS

TEST NO (1)	FIRST MEMORY LOCATION — TESTS 3, 4, & 5: MEMORY BLOCK (2)	FIRST MEMORY LOCATION — TESTS 3, 4, & 5: ADDRESS IN MEMORY BLOCK (3)	LAST MEMORY LOCATION — TESTS 4 & 5: MEMORY BLOCK (4)	LAST MEMORY LOCATION — TESTS 4 & 5: ADDRESS IN MEMORY BLOCK (5)	COMMON CONTROL (6)	TESTS 2 & 3 TOTAL FAILED WORDS / TESTS 3 & 5 CONTENTS OF FIRST MEM LOC (7)	MEMORY AREAS (8)	TESTS 2 & 3 TOTAL FAILED BLOCKS / TESTS 3 & 4 FAILURE CODE (9)	PROC 522
2	0	4062	16	4221	-	21	4	5	522

FIELD 1 2 3 4 5 6 7 8 9

A. PURPOSE

Procedure 522 is used to detect memory mismatches in DIMENSION 2000 duplicated processor systems. This procedure is used when the NETWORK OTHER-515 alarm indicator is lit, when the mismatch flag is set (which lights the MINOR alarm), or to read the contents of a memory location

The mismatch flag is set when any of the following conditions exist:

- The on-line memory comparison test detects a mismatched memory condition.
- A double write operation fails to function correctly.
- The run tape program detects a mismatch.

A mismatch flag displays error code 75 each time a procedure is requested and any time an add, change, or remove operation is successfully completed. The MINOR and OTHER alarms are lit the first time a mismatch flag is set.

Procedure 522 provides the following five tests:

- Test 1 displays and clears a failed memory location detected by the on-line program memory match.
- Test 2 provides a picture of the system's overall memory health.
- Test 3 provides specific groups of unbroken failure blocks and displays the contents of each of the failed memory locations within the failed block for each processor.
- Test 4 allows continuous testing of a specified range of memory locations.
- Test 5 reads the contents of any memory location, or any range of memory locations, for each processor in a duplicated system. Test 5 is the only test in this procedure that can also display the contents of memory locations for an unduplicated system.

The memory match tests (Tests 2 through 4) compare the contents of corresponding locations in duplicated common controls. The range of memory tested is restricted to the program, patch, and translation areas. Test 5 is not restricted and displays the contents of memory to be read over the full range of memory.

Memory address fields (fields 2, 3, 4, and 5) and fields 7 and 9 are displayed in octal.

B. FIELD DEFINITIONS AND CODES

Field	Code	Definition
1	1-5	Test number.
2	00-77	Memory block number (1 block = 8K).
3	0-17777	Starting address within the memory block of field 2.
4	00-77	Memory block number (1 block = 8K).
5	0-17777	Ending address within the memory block of field 4.
6*		Processor memory is being read:
	0	On-line common control.
	1	Off-line common control.
* Does not apply to Test 2 or 4.		

B. FIELD DEFINITIONS AND CODES (Contd)

Field	Code	Definition
7	0-177777	Total number of failed words (Test 2); total number of failed words which displays upon test completion (Test 3).
	0-471150	Contents of memory location in fields 2 and 3 are displayed when NEXT DATA is pressed (Test 3); contents of memory location in fields 2 and 3 are displayed when EXECUTE or NEXT DATA is pressed (Test 5).
8		Memory area code:
	1	Program only.
	2	Patch only.
	3	Program and patch.
	4	Translation only.
	5	Program and translation.
	6	Patch and translation.
	7	Program, patch, and translation.
	8	Other (Test 5 only)
9	0-77	Total failed blocks (Test 2); total failed blocks which are displayed at the completion of the test (Test 3).
		Failure code (complete Test 3, then Test 4):
	0	No failures.
	1	Memory mismatch.
	2	Parity error.
	3	Mismatch and parity.
	4	Duplication channel error.

C. TEST PROCEDURES

NOTE

The following special error codes may be displayed:

Code	Definition
73	If the MAAP is locked up, this indicates the procedure caused a system initialization (INT-A) displayed by Procedure 520.
74	Common control not duplicated (only Test 5 can be executed in an unduplicated system).
80	Location out of memory range, or first location is greater than last location.
81	Wait until off-line CC loaded.
82	May be displayed because of several hardware or software problems. Some of these are: – HALT switch operated in off-line processor. – Both processors appear on-line. – Parity error in off-line processor. Procedures 520 and 521 can be used to correct some of these problems.

Call in Procedure 522:

PROC NO.; 522; ENTER

Test 1 is automatically selected. To select other tests, use the NEXT TEST key.

C. TEST PROCEDURES (Contd)

> **NOTE**
>
> Anytime failure codes 2 or 4 are detected, the test will stop. Procedure 521 should be used to correct duplication channel errors and 520 for parity errors.

Test 1:

Test 1 is used to display and/or clear a failed memory location recorded by the on-line memory match program (this can also be done in Procedure 520).

Depressing the EXECUTE key begins the test. Fields 2 and 3 display the memory block and failed address within that block in octal, respectively. A 1 will be displayed in field 9.

If the on-line program has not detected any memory mismatches, dashes will be displayed in fields 2 and 3 and a zero will be displayed in field 9

To clear the on-line failure history, use CLEAR DATA; EXECUTE. This sequence will dash fields 2 and 3 and display a zero in field 9, indicating the mismatched memory locations failure history has been cleared.

Test 2:

Test 2 is used to test all memory locations and display the total number of failed words. A memory area code display indicates the area of memory where the failures occurred (ie, patch, translation, program, or any combination of these three).

Depressing the EXECUTE key begins the test. Fields 2, 3, 7, 8, and 9 are updated every second. Field 2 displays the block under test, and field 3 the address within that block. Field 7 displays the cumulative number of failed memory locations and field 9 the cumulative number of failed memory blocks. Field 8 displays the area code for the detected failure.

When the test completes, fields 2 and 3 will equal fields 4 and 5. Field 7 displays the total number of failed locations and field 9 the total number of failed blocks. If any failures are detected, field 8 displays the area of memory where the failures were detected.

Depressing STOP stops the test and displays the last memory location tested in fields 4 and 5, and the accumulated failure data in fields 7 and 9.

If all testable memory locations have been tested successfully (no mismatches), the memory mismatch flag is reset and the OTHER and MINOR alarms are retired. The OTHER and MINOR alarms will be lit along with the memory mismatch flag being set if any failures are detected. Only Test 2 can retire alarms and reset the memory mismatch flag. Tests 2, 3, and 4 can turn on the alarms and set the memory mismatch flag.

Depressing EXECUTE again will restart the test from the beginning.

Test 3:

Test 3 is used to test all memory locations from the first memory location to the end of testable memory. The test stops when a contiguous block (a contiguous block may be as small as one location or as large as all of testable memory) of failed memory locations is identified and displays the type of failure detected. The contents of any failed memory location within the failed block is displayed when NEXT DATA is pressed.

C. TEST PROCEDURES (Contd)

Depressing the EXECUTE key begins the test. Fields 2 and 3 are updated every second. Field 2 displays the block under test and field 3 the address within that block. When the first failure is located, fields 2 and 3 freeze, displaying the first location of the failed block. The test continues to run until the end of the failed block has been identified and the stops. Once the failed block has been identified and the test is stopped, depressing NEXT UNIT causes the test to continue from the location displayed in fields 4 and 5 plus one. When stopped, fields 4 and 5 display the last location of the failed block. Field 8 displays the area of memory where the failure occurred and field 9 the type of failure found. When the test completes (fields 2 and 3 equal fields 4 and 5), field 7 displays the total number of failed words, and field 9 the total number of failed memory blocks.

The STOP key stops the test. If the test is stopped in the middle of a failed block of memory locations, fields 4 and 5 will display the last tested failed locations and field 9 will define the type of failure detected. If the test is stopped and no failures were detected, a "0" is displayed in field 9. Fields 4 and 5 display the last testable memory location for this configuration and fields 2 and 3 display the last tested memory location.

Depressing EXECUTE anytime after the first EXECUTE will restart the test from the beginning.

Depressing NEXT UNIT anytime after the test has stopped will cause the test to continue on from where it stopped.

Depressing NEXT DATA after a failed block has been identified displays the contents of the failed memory location within a block of contiguous failures beginning at the memory location of fields 2 and 3. The display will alternate between Processors 0 and 1 and then step to the next memory location. When all of the memory locations have been read, depressing NEXT DATA again displays dashes. Depressing NEXT DATA once more starts the process over again.

Test 4:

Test 4 allows continuous testing of a specified range of memory.

Begin testing at a specific memory location:

> (Starting memory block); ENTER; (Starting address); ENTER; (Ending memory block); ENTER; (Ending address); ENTER; EXECUTE
>
> If starting and ending memory locations are not entered (ie, only EXECUTE is used), the test will start with the last displayed block of failures from Test 3. If no errors were found in Test 3, fields 2 and 3 and fields 4 and 5 display the entire range of testable memory. Fields 2 and 3 flash every 2 seconds indicating that the displayed locations can be used or a new range entered. The test will restart when the last location is reached and continuously run until the STOP key is depressed.
>
> Depressing STOP stops the test. If failures were detected within the specified range, fields 2 and 3 display the lowest failed location within the test range and fields 4 and 5 the highest failed location within the test range. Field 8 displays the area of memory and field 9 the faillure code. If no failures are detected, fields 2 and 3 and 4 and 5 display the original range, field 8 dashes, and field 9, a zero. Fields 8 and 9 are refreshed after every pass through the range specified, and when the STOP key is depressed.

C. TEST PROCEDURES (Contd)

Test 5:

Test 5 is used to read either any single location or range of memory locations. Test 5 can be used with either duplicated or unduplicated systems.

Begin testing at a specified location:

> (Starting memory block); ENTER; (Starting address); ENTER; (Ending memory block); ENTER; (Ending address); ENTER; EXECUTE
>
> When the test is first read in, the display defaults to the last displayed block of failures from Test 3. If no failures were found in Test 3, fields 2 and 3 and 4 and 5 display the same default range as Test 2. However, any range within the entire range of memory may be entered. Fields 2 and 3 also blink indicating that the default locations can be used or another range entered.

EXECUTE starts the test and reads the contents of the first location for processor 0.

Depressing NEXT DATA steps through the memory range displayed in fields 2 and 3 through fields 4 and 5 one at a time alternating between the on-line and off-line common controller as indicated in field 6. When the last memory location is read, depressing NEXT DATA again displays dashes. Depressing NEXT DATA once more restarts the test at the first memory location of the on-line common controller.

If the system is unduplicated, only the on-line controller can be read.

D. REPAIR GUIDE

The repair guide is broken down into two parts; the translation repair guide and the patch program repair guide.

> **NOTE**
>
> Good customer service is defined as follows:
>
> - The most recent changes made to the system are in and working properly.
> - No trouble reports exist (eg, phones not working).
> - Attendant consoles are not malfunctioning.
> - An abnormal number of status memory audit pegs do not exist.
> - There are no initialization problems (see Procedure 520).

TRANSLATION Repair Guide

1. If customer service is good, go to Step 2. If not, go to Step 5.
2. Run tape in on-line processor. Go to Step 3.
3. Load the off-line processor with the on-line tape and run Procedure 522. If the two processors match, go to Step 4. If they mismatch, run Procedure 500 in both processors.
4. Perform a run tape of the off-line tape. Repair procedure complete.
5. Switch service to the off-line processor. If customer service is good, go to Step 2 above. If service is not good, continue.

D. REPAIR GUIDE (Contd)

TRANSLATION Repair Guide (Contd)

6. Reload the off-line processor. Perform a hard switch. This is done by halting the on-line processor (switch the GO/HALT switch to the HALT position). The PBX is automatically switched over to the other processor. If customer service is good, go to Step 3 above. If service is not good, continue.

7. Reload the off-line processor. Perform a hard switch as explained in Step 6. If customer service is good, go to Step 3 above. If service is not good, continue.

8. At this point you have reloaded each processor independently without achieving good service. Start at Step 3 with backup tapes in an attempt to provide good customer service.

PATCH and PROGRAM Repair Guide

NOTE

Customer service must be good before proceeding with this section. Good customer service is defined as follows:

- The most recent changes made to the system are in and working properly.
- No trouble reports exist (eg, phones not working).
- Attendant consoles are not malfunctioning.
- An abnormal number of status memory audit pegs do not exist.
- There are no initialization problems (see Procedure 520).

If customer service is not good, go to the TRANSLATION repair guide first. If the TRANSLATION repair guide fails to provide good service, then go to Step 1 below.

1. Find the total number of patches on each tape using Procedure 490. If the tapes have the same number of patches, go to Step 4. If the two tapes mismatch, continue with Step 2.

2. Add the missing patches to the deficient tape using Procedure 490.

3. Reload the deficient common controller and check for a mismatch. If a mismatch still exists, use Procedure 500 to isolate the problem in the tape or minirecorder area. If there are no mismatches, repair is complete.

4. If the problem is in the PROGRAM memory area only, go to Step 5. If the problem is a PROGRAM memory area and PATCH memory area or PATCH memory area only, go to Step 10.

D. REPAIR GUIDE (Contd)

PATCH and PROGRAM Repair Guide (Contd)

5. Acquire second level maintenance help to determine which processor is in error. Correct the failed common control using Procedure 999. Reload the deficient processor without interrupting service. Check for proper operation using Procedure 522, Test 3. If the two tapes match, go to Step 8. If a mismatch still exists, continue with Step 6.

6. Reload the incorrect common control with the tape from the correct common control and run Procedure 522. If the tapes match, run Procedure 500. If the tapes still mismatch, continue.

7. The first tape is probably defective. Replace the tape and rerun the test again from the beginning.

8. Run Procedure 522, Test 4 on the failed memory locations. If the two tapes match, the error was probably intermittent and the repair is complete. If the two tapes still mismatch, continue.

9. Replace the defective memory board. Reload the tape and rerun Procedure 522, Test 2 to clear the alarms.

10. Run Procedure 522, Test 3 and determine which patch is missing from the defective tape by counting the number of failed locations. Add the deficient patch to the defective common control using Procedure 490.

11. Add the missing patch to the tapes, reload the tapes, and run Procedure 522. If the two tapes match, repair is complete. If the two tapes still mismatch, run Procedure 500 (suspect a defective tape drive).

END