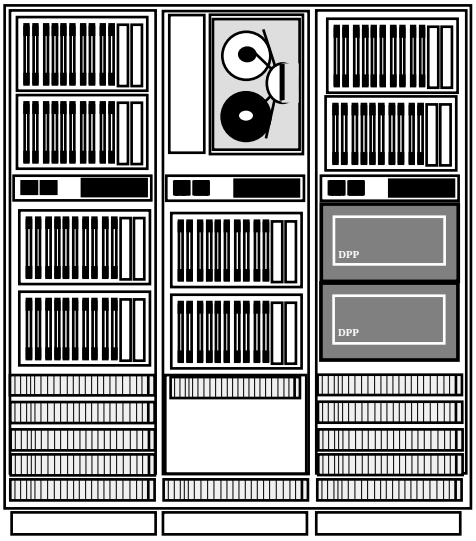
297-1001-536

Distributed Processing Peripheral

Card Replacement Guide

BCS35 and up Standard 01.03 August 1996



northern telecom

DMS-100 Family

Distributed Processing Peripheral

Card Replacement Guide

Publication number: 297-1001-536
Product release: BCS35 and up
Document release: Standard **01.03**
Date: August 1996

Publication history

August 1996

Standard release 01.03 for software release BCS36 and up. This version includes changes to this "Publication history" page.

December 1993

Standard release 01.02 for software release BCS36 and up.

Contents

List of Figures

List of Tables

List of Procedures

About this document

This document describes the card replacement procedures for the Distributed Processing Peripheral (DPP).

Applicability of this document

Northern Telecom (NT) software releases are called batch change supplements (BCS) and are identified by a number, for example, BCS35.

This document applies to DMS–100 Family offices with BCS35. Unless the document is revised, it also applies to offices with software releases greater than BCS35.

How to identify the software in your office

The *Office Feature Record D190* lists your current BCS and its NT feature packages. To view similar information on screen, enter the following command string at a Maintenance Administration Posistion (MAP) terminal.

```
PATCHER;INFORM LIST;LEAVE
```

How the DPP documentation package is organized

This document is part of the DPP documentation package supporting Northern Telecom's DPP products. The DPP documentation package is a subset of the DMS–100 Family library.

Documents in the DPP documentation package

The DMS–100 Family library is structured in numbered layers, each of which is associated with a Northern Telecom product. The DPP documentation package is in the 297–1001 layer.

The list of DPP documents follows.

Document	Title
297–1001–019	*Distributed Processing Peripheral (DPP) Product Guide*
297–1001–543	*DPP Alarm Clearing and Performance Monitoring Guide*
297–1001–536	*DPP Card Replacement Guide*
297–1001–331	*DPP Administration Guide*
297–1001–537	*DPP Recovery and Routine Maintenance Procedures*

How the DPP documents relate to other documents

DPP documents are intended to be used with other documents in the DMS–100 Family library.

To understand the contents of the DPP documents, other documents in these layers may help:

- DMS–100 basic documents in the 297–1001 layer
- DPP documents in the 297–1001 layer

Where to find information

Documents helping you understand this manual, or the tasks it describes, are referenced in the text.

These documents, and other related manuals, follow.

Note: More than one version of these documents may exist. To determine which version of a document applies to the BCS in your office, check the *Northern Telecom Publications Master Index, 297–1001–001*.

Document	Title
297–1001–001	*Master Index of Practices*
GFXINDEX	*General Feature Description Index of Documents*
297–1001–112	*Modular Documentation System (MDS)*
297–1001–128	*AMA – Bellcore Format*
297–1001–310	*Table Editor Reference Manual*
297–1001–821	*DMS Menu Commands Reference* (covers DPP commands)
297–1001–820	*DMS NonMenu Commands Reference*
297–1001–013	*Device Independent Recording Package (DIRP) Product Guide*
297–1001–345	*DIRP Administration Guide*
297–1001–175	*DIRP Planning and Engineering Guide*
297–1001–345	*DIRP Administration Guide*
297–1001–574	*DIRP Recovery Procedures*
297–1001–572	*DIRP Routine Maintenance Guide*
297–1001–356	*DIRP Translation Guide*
297–1001–510	*Log Report Manual*
297–1001–451	*Customer Data Schema* (contains the five DPP translations tables)
297–1001–513	*Input/Output Devices (IOD) Man–Machine Interface Description*

NT and BNR trademarks and the products they represent

The following chart lists all NT and BNR trademarks in this document.

Trademark	Product
DMS	*Digital multiplex system* telephone switching equipment
DMS SuperNode	telecommunications switching equipment
MAP	*Maintenance and administration position* telephone communication equipment

What precautionary messages indicate

Caution, danger and warning messages indicate potential risks, as identified in the following chart.

Message	Significance
CAUTION	Possibility of service interruption or degradation
DANGER	Possibility of personal injury
WARNING	Possibility of equipment damage

Examples of the precautionary messages follow.

CAUTION
Calls are dropped when line group controller is busied.
Manually removing the line group controller from service removes all its subtending peripheral modules from service. All calls in progress are dropped.

DANGER
Risk of electrocution
The inverter contains high voltage lines. Do not open the front panel of the inverter unless fuses F1, F2, and F3 have been removed first. Until these fuses are removed, the high voltage lines inside the inverter are active, and you risk being electrocuted.

WARNING
Backplane connector pins may become damaged.
Use light thumb pressure to align the card with the connectors. Next use the levers to seat the card into the connectors. Failure to align the card first may result in bending of backplane connector pins.

How commands, parameters, and responses are represented

In this document, commands, parameters, and responses are represented according to the following conventions.

Input prompt (>)

An input prompt (>) indicates that the following information is a command.

Type the command that follows the input prompt and press the carriage return key.

Capital letters

Capital letters represent commands, fixed parameters, and responses appearing at a MAP.

Enter the command or fixed parameter exactly as it appears.

Lowercase letters

Lowercase letters represent variables.

For commands and parameters, enter the letters or numbers the variable represents. In most instances, the name for the variable clearly indicates what you must enter. If it does not, further explanations are provided.

In responses (presented in capital letters), lowercase letters represent a range of values.

The following example illustrates the command syntax in this document.

Examples of command syntax in this document

Step	Action
1	Post the card in the inactive unit.
input>	**>POST unit_no card_no state**
parameters>	where unit_no is the number of the inactive unit (0 or 1) card_no is the number of the card you replaced (22–27) state is the state of the unit in which you wish to replace the card (Insv, SysB, ManB or Offl)
Example input>	For example: **>POST 7 1 INSV**
Example output>	`CARD 7 IS POSTED IN UNIT 1 OF MSB16`

Replacing circuit packs

How to use this document

Use the procedures in this document when replacing circuit packs in the DPP. A general description of each circuit pack is first presented, then the replacement procedures are given. Next, information about option settings and circuit pack layout is presented.

General information about circuit pack failures

Circuit pack failure usually causes the DPP to go to an alarm condition and switch system control to the standby processor – away from the processor with the faulty circuit pack. The DPP's response to failure depends on how the Error Map (ERRMAP) is set up.

Level 0 alarm failures do not cause a processor switch. Level 1, 2, and 3 alarm failures do require a processor switch. Level 1 is the least severe, and level 3 is the most severe.

Perform a manual processor switch away from the side with the suspected circuit pack; see Procedure 1–1 . If the DPP is still in PRIME mode, set it to an ONLY mode before replacing the circuit pack. If a card causes a level 2 alarm in the active processor, the DPP will switch processors if the standby processor has a level 1 or level 0 alarm or less.

General Troubleshooting Guidelines

The circuit packs used here are only examples. This troubleshooting procedure is valid for any combination of circuit pack printouts.

Enter the command TEST ACT or TEST STDBY and the following printout may appear:

```
DPP STANDBY/ACTIVE FAULT
ERROR DETECTED ON PROC (A or B)
CPU CARD    /    SLOT:A1  EQPEC=6M62
EPROM PCA   /    SLOT:A2  EQPEC=6M63
MEM EXPN    /    SLOT:A3  EQPEC=6M64
```

Perform Procedure 1–1.

Procedure 1–1
DPP troubleshooting procedure – no specific fault indicator available

Step	Action	Notes
1	Make sure the DPP is in an ONLY processor mode for the processor that does not have the fault.	See Procedure 1–2.
2	Power down the processor in error – this should be the off-line processor. Reseat the circuit packs listed in the printout and wait for 30 seconds. Apply power to the processor and wait for the "S/W LOADED" message to appear.	See Chapter 17 for DPP power supply information.
3	Test the processors with the TEST ACT and TEST STDBY commands. If the tests pass, place the DPP in the PRIME processor mode and let soak for 2 days.	
4	After the soak period, retest both processors with the TEST ACT and TEST STDBY commands.	
5	If the test fails or the problem reappears after the soak time, perform steps 6a through 6b.	
6a	Activate the ONLY mode for the on-line processor. Power down the off-line processor.	
6b	Replace the NT6M62xx circuit pack with a spare and apply power to the processor.	The NT6M62xx card is the CPU card in Slot 1.
6c	Test the processors with the TEST ACT or TEST STDBY command.	
6d	If the test passes, place the DPP in the PRIME processor mode and let it soak for 2 days.	

(continued)

Procedure 1–1
DPP troubleshooting procedure – no specific fault indicator available
(continued)

Step	Action	Notes
6e	If the test immediately fails or the error reoccurs during the soak time, repeat Step 6a, replacing NT6M63xx in Step 6b. If after replacing NT6M62xx and NT6M63xx, the problem reappears, repeat from Step 6a, replacing NT6M64xx in Step 6b.	NT6M63xx: EPROM card, slot 2. NT6M64xx: DRAM card, slot 3.
6d	If the test passes, place the DPP in the PRIME processor mode and let it soak for 2 days.	
6	If trouble continues, contact next level of support.	
	End	

Note:

Reseating the circuit packs listed in the TEST ACT or TEST STDBY command clears the problem in some cases. If the error does not reoccur during the soak time after reseating the circuit packs, then the reseating will have cleared the problem.

Changing processor modes

If preparing to change a circuit pack and you need to change mode, use the following procedure.

Procedure 1–2
DPP circuit packs replacement – changing processor modes

Step	Action	Notes
1	Press the processor A/B Select Switch to the position (A or B) that matches the active processor.	
2	Press the O/P Mode Switch to the ONLY position.	
3	Turn the Mode Switch.	Turn to the right and release.
4	Observe that the active processor unit ONLY status lamp lights. Wait for the log message, "Processor force selected – nonredundant." Go to one of the procedures referenced in step 6, as required.	DPP will go into alarm.
5	Go to the appropriate chapters in this document for replacement procedures for the circuit packs. The document is organized according to circuit pack.	

Central Processor Unit (CPU)

General description

The CPU circuit pack is located in slot 1 of the A and B chassis. The CPU, which has direct memory access, organizes data flow throughout the DPP. Its operations can be classified according to the functions of its four major Integrated Circuits (ICs):

- Z80 IC
- DMA IC
- CTC IC
- PIO IC

The 8–bit microprocessor Z80 IC is responsible for operational, statistical, and maintenance functions. Some of its activities include communication, statistics, and log messages. The Z80 microprocessor is driven by the crystal clock (on the same circuit pack) through the various program steps.

The Direct Memory Access (DMA) IC is a Z80–compatible device, responsible for data transfer to and from Random Access Memory (RAM) and the DSI circuit packs.

The Counter Timer Circuit (CTC) IC handles interrupts from various devices within the DPP that request access to the bus for data transfer. AC power (the 60 Hz signal supplied from the external ac transformer, if equipped) is supplied to the P/A Comm circuit pack. Here it is converted to 60 Hz pulses and supplied to the CTC so it can generate the interrupt. The CTC recognizes the priority of the devices interrupting the normal idle state of the Z80 microprocessor and directs the Z80 to grant access to the bus according to the importance of the device making the request.

The Parallel Input/Output (PIO) Circuit IC is used for all interprocessor communications.

The clock signal used to drive the Z80 microprocessor originates from a crystal on the CPU circuit pack.

Central processor unit LED display

The CPU circuit pack contains a seven–segment display Light Emitting Diode (LED) that provides a visual display of error control status. Five hardware status lines are decoded to display CPU fault conditions. The display also contains a decimal point feature that provides a visual display of the CPU clock. See Table 2–1.

Output to the display must occur within 0.5 seconds for the display to remain valid. This time frame is compatible with the 0.5 second status request time interval of the error control circuit pack. The data byte and hardware status lines are decoded by an Erasable Programmable Read Only Memory (EPROM). Output conditions may appear as shown in Table 2–1.

There are various option settings on this circuit pack. See Table 2–1. Figure 2–2 shows the option locations and circuit pack layout.

Replacing CPU circuit pack

To replace the CPU circuit pack, use the following procedure.

Procedure 2–1
Replacing CPU circuit pack – slot 1

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty CPU is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis using the +8 V dc red rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "S/W Loaded" to print.
8	At the maintenance terminal, enter: **>RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.

(continued)

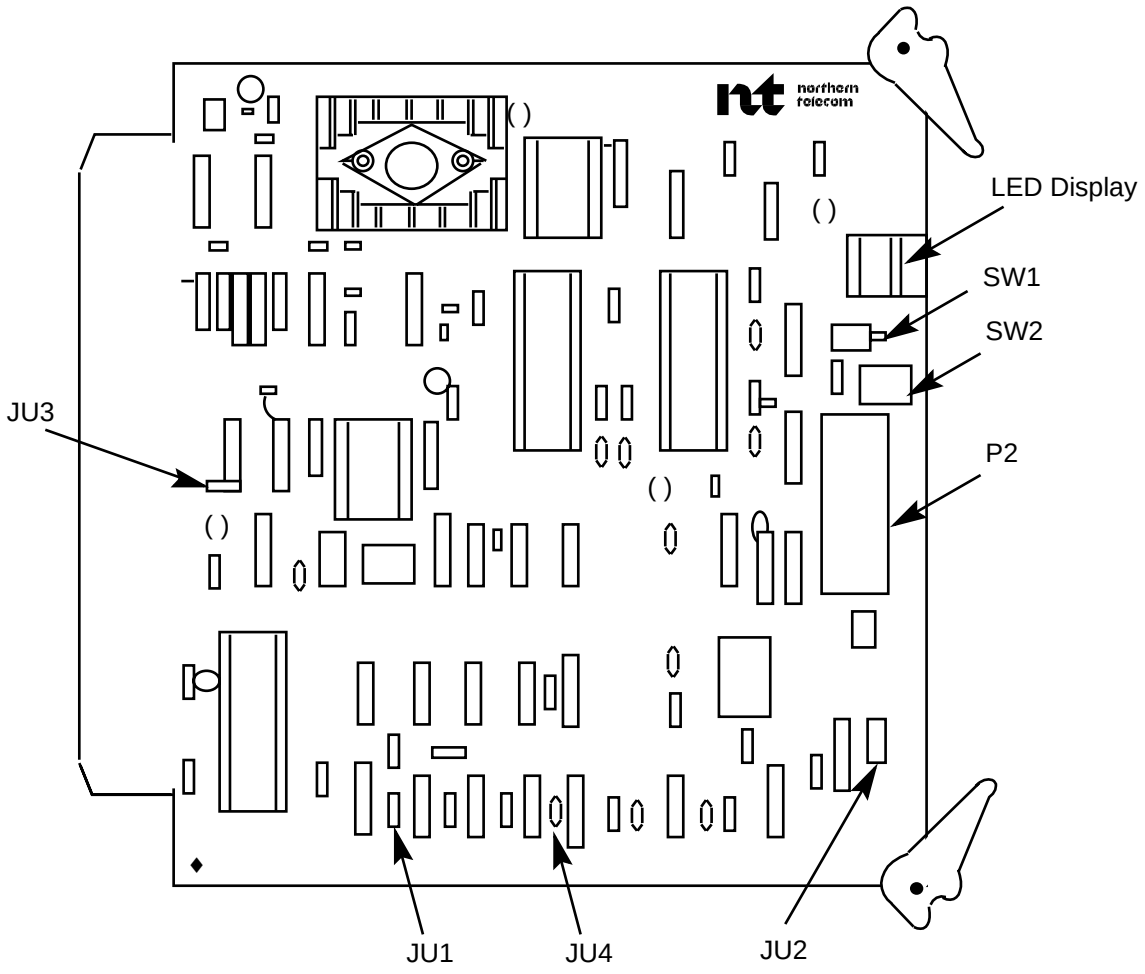
Procedure 2–1
Replacing CPU circuit pack – slot 1 (continued)

Step	Description	Notes
9	At the maintenance terminal, enter: **>TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **>RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Notes:
Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Figure 2–1
CPU with DMA (A1 and B1) circuit pack (NT6M62BA) options



Note: Switch SW2 is a four–position right angle dip switch at the edge of the CPU circuit pack.

Table 2–1
ECAC alarm reporting priority sequence – LED display codes

LED	Level	Category	Response	Notes
E.		Major	Invalid CPU Response	
d.	3	Critical	Critical Level 3	Processor switch occurs.
C.	2	Critical	Critical Level 2	Processor switch occurs.
b.	1	Critical	Critical Level 1	Processor switch occurs.
A.	0	Critical	Critical Level 0	Level 0 alarms are alarms only, with no accompanying processor switch.
9.	3	Major	Major Level 3	Processor switch occurs.
8.	2	Major	Major Level 2	Processor switch occurs.
7.	1	Major	Major Level 1	Processor switch occurs.
6.	0	Major	Major Level 0	Level 0 alarms are alarms only, with no accompanying processor switch.
5.	3	Minor	Minor Level 3	Processor switch occurs.
4.	2	Minor	Minor Level 2	Processor switch occurs.
3.	1	Minor	Minor Level 1	Processor switch occurs.
2.	0	Minor	Minor Level 0	Level 0 alarms are alarms only, with no accompanying processor switch.
1.		None		Planned processor switch.
Ξ.		None		All systems operational.

End

Table 2–2
CPU display control functions

Mode	SW2–3	SW2–4	Description
Monitor Error Control Port	on	off	Standard setting: data written to the error control port I/01 (88–8B; hex) is decoded, along with processor signals WAIT, HALT, RESET, BUSAK, and CLK
Independent Port	off	on	Data must be written to I/06 (9C–9F; Hex). This is included for future use. Display codes must be modified by changing the decoder firmware.
Both Ports (invalid)	on	on	This is an invalid condition since data written to either port may be displayed.
Neither Port (invalid)	off	off	No data is written to the display circuit, causing an error condition display = E.

Table 2–3
CPU with DMA circuit pack (A1 and B1) options – part number: NT6M62BA

Device type number	Position/setting	Function	Setting	Factory On–site
Jumper (J3)[1]	PINS: 2–3 8 KHz clock from DMS–100 enabled. 1–2: 60 Hz clock from AC adapter, if present.	Determines whether the DPP uses 8 KHz from the DMS–100 or the optional ac clock.		1–2 pin 1 is closest to gold finger contacts.
Jumper (JU1)[1]	In: Enable 8KHz clock receiver. Out: Disable 8KHz clock receiver.	Control operation of 8KHz clock receiver.		In
Jumper (JU2)	All: Enable additional wait states. Disable additional wait states.	Enable the addition of wait states (up to 5) on the ABCD inputs of the counter chip.		Configured for 1 wait state in the copper tracings
Jumper (JU3 &JU4)	Out: Connects the internal 8KHz to pin 85 of the backplane connector.	Attachment of peripherals; not defined at this time.		Out (Currently unused)
Strap	None used			
DIP Switch (SW2–1)	On: Outputs = Inputs Off: Output = Tristated	Control Logic Analyzer Port.		1 = Off
DIP Switch (SW2–2)	On: +5V output enabled Off: +5V output disabled	Provide +5 V dc to Analyzer Port connector (pin 21) for powering certain types of external testers. (Limited to 250ma.)		2 = Off
DIP Switch (SW2–3) (SW2–4)	Display Mode 3 4 Err Cont Port On Off I/O 6 Port Off On (Invalid) On On (Invalid) Off Off	Monitors Error Control. Monitors data written to I/O 6 Port.		3 = On 4 = Off
Rotary Switch	None used			

Table 2–3
CPU with DMA circuit pack (A1 and B1) options – part number: NT6M62BA (continued)

Device type number	Position/setting	Function	Setting	Factory On–site
Switch SW1	Momentary Pushbutton (red)	Processor Reset.		

CAUTION
Do not press SW1 unless instructed to do so; activation may cause billing data loss if done on the active processor.

Notes:
1. Although these options are on the CPU card, they are not active in any DPP application.

End

EPROM circuit pack

General description

This circuit pack, in slot 2 of the A and B chassis, stores the main program for DPP operation. It contains 16 Kilobytes (Kbytes) of EPROM and 48 Kbytes of RAM. At power up, the EPROM Boot and Monitor programs automatically download the main program from disk to RAM.

A power regulator IC on this circuit pack reduces the nominal +8.5 V dc provided by the power supply to a regulated +5 V dc for circuit assembly operation.

There are jumper settings on the EPROM. See Tables 3–1, 3–2, and 3–3. Figure 3–1 shows the jumper locations and circuit pack layout.

Replacing EPROM integrated circuits

The DPP contains Erasable Programmable Read Only Memory (EPROM) firmware routines. EPROM Integrated Circuits (ICs) contain operational programming for some DPP system functions. The EPROM's fixed memory is factory programmed with necessary control instructions. After installation in the DPP, the EPROM always responds in the same manner.

You may replace an EPROM IC with another EPROM IC having the same set of programmed instructions, for example when an EPROM malfunctions or fails. However, to change the way the DPP functions, install an EPROM IC with different programmed instructions.

See Procedure 3–1 for removal, installation, and handling precautions when changing DPP EPROM ICs. There are two methods for changing EPROM ICs. One method is to replace the EPROM ICs and the PEC/rel label on the circuit pack. Another method is to replace the entire circuit pack.

> ***Note: 1*** If replacing EPROM ICs, check the reference number on the circuit pack diagram to make sure the right EPROM type is being used.

EPROM IC precautions

Follow these precautions when installing new or replacement EPROM ICs:

- Handle all ICs by the plastic or ceramic package, not by their metal pins.
- Do not expose the ICs to excessive force (dropping) or to large fields of electrical or magnetic energy (power transformers, static discharge). This maltreatment can cause partial or total EPROM memory loss.
- Make sure the UV window is completely covered.
- Work on a surface with a good electrical ground and do not wear clothes or footwear with a high degree of synthetic materials, especially nylon. To prevent IC damage, control or eliminate static electricity.
- The IC is designed for easy socket insertion and removal. Use only minimum pressure since excessive force can bend or break the pins. Also, use the specific tools for extracting and inserting ICs to avoid damaging them.
- Use caution when handling the ICs and the circuit packs. Excessive force can bend or break pins or cause hairline cracks in the copper foils.
- Make sure the notch on the EPROM matches the notch on the socket.

Procedure 3–1
EPROM IC installation procedure

CAUTION

Since all DPP circuit packs are static sensitive, be careful when handling them. [1]

Step	Description	Notes
1	Locate the two EPROM ICs on the circuit pack.[2]	This IC is labeled with a coded number for identification.
2	Gently pry the EPROM IC from its socket and set it aside. Use a gentle rocking motion, alternately lifting each end a little at a time to avoid bending the pins.	Use an IC extractor tool or a small blade regular screwdriver. Do not throw the EPROM away; return it to NT.
3	Remove the new EPROM IC from its packing material and place it on a smooth flat surface so the pins are facing down and the coded identification label can be read from the top.	Use this protective package to store the old EPROM IC until verifying the new one.
4	Position the marked end of the new IC over the marked end of the notch and carefully insert the pins into the socket.	Notches or dots identify the location of pin 1 on both ICs and IC sockets.
5	Apply firm, even downward pressure on the EPROM IC until it is fully seated in the socket.	The new IC may be supplied with 24 or 28 pins. If the IC has 24 pins, install it to the rear of the 28–pin socket. IC–pin 1 lines up over socket–pin 3.
6	Do not remove the coded label from the IC.	

(continued)

Procedure 3–1
EPROM IC installation procedure

Step	Description	Notes
7	Update the label every time an EPROM is changed on that circuit pack.[3]	Each circuit pack with an EPROM chip (or chips) has a firmware ID label. The data for the label is on the EPROM label. The firmware id is the last number on the label.

Notes:
Note 1: Perform this entire procedure on the standby processor with the system locked in ONLY processor mode. After replacement and testing on the standby side with the new firmware, perform an ONLY to ONLY processor switch and change the firmware on the now standby side.
Note 2: If none of the ICs on the circuit packs has a printed label, see Table 3–1 for the index of tables and figures for the circuit pack options. Locate the correct table and figure for the circuit pack.
Note 3: Changing the EPROM on a circuit pack may change the circuit pack's PEC/REL level. The change kit provides the new labels. Also update any spare parts and office records .

End

Replacing the EPROM circuit pack

To replace the EPROM circuit pack, perform the steps in the following procedure.

Procedure 3–2
Replacing EPROM circuit pack

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty pack is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc red rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.

(continued)

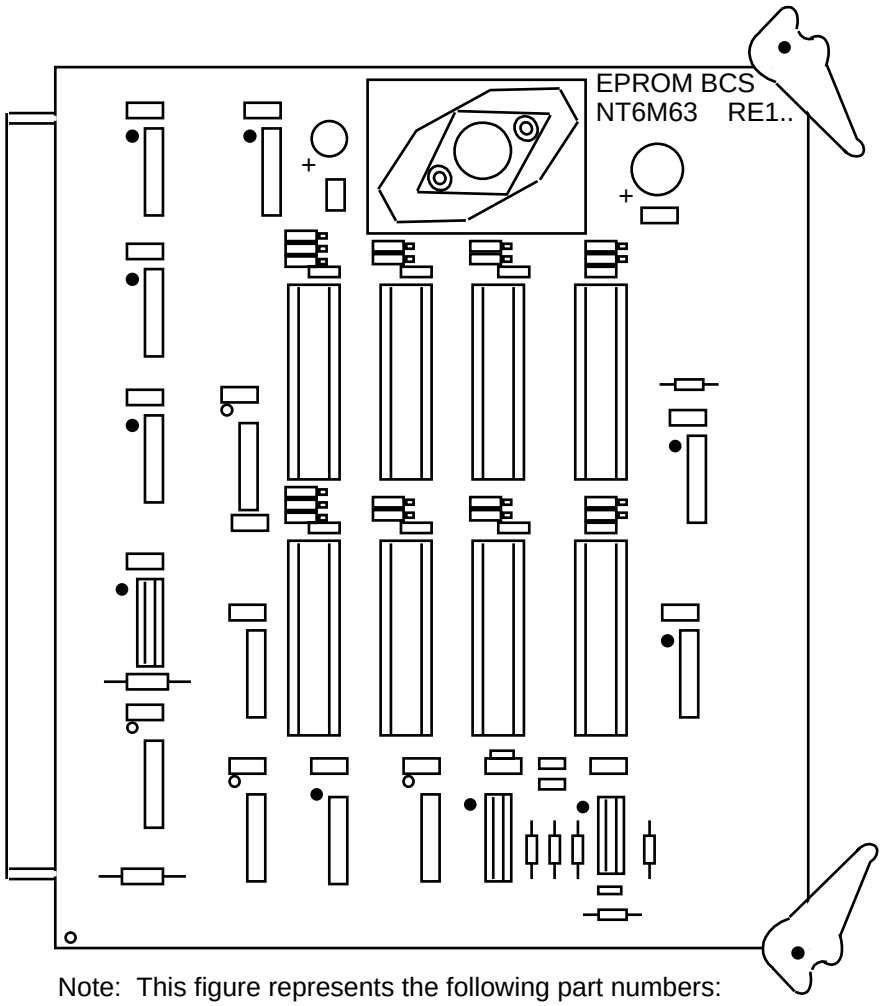
Procedure 3–2
Replacing EPROM circuit pack

Step	Description	Notes
8	At the maintenance terminal, enter: **>RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.
9	At the maintenance terminal, enter: **>TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **>RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Notes:
Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Figure 3–1
EPROM (A2 and B2; see note) circuit pack options



Note: This figure represents the following part numbers:

NT6M63BF (BCS21–24 DPP systems)
NT6M63CF (BCS21–24 DPP systems)
NT6M63CH (DPP systems w/o 56K polling)
NT6M63CJ (DPP systems w/56K polling)
NT6M63CL (DPP systems w/56K polling; nonturbo)

Table 3–1
EPROM circuit pack (A2 and B2) options part number: NT6M63BF, NT6M63CL, NT6M63CH, NT6M63CF; BCS21–up DPP w/o 56K polling

Device type (number)	Position/setting				Function	Setting	
						Factory	On–site
Jumper (P2)	In Out				No DRAM circuit pack Use with DRAM circuit pack		Out
Jumper	Type	P3	P4	P5	(U5)	Configuration set–up for	
(P3)		P6	P7	P8	(U6)	devices U5 and U6.	1–2
(P4)							1–2
(P5)	2016	1–2	1–2	2–3			1–2
(P6)	2782	1–2	1–2	1–2			1–2
(P7)	2764	1–2	1–2	1–2			1–2
(P8)	6264	2–3	1–2	1–2			1–2
	27128	1–2	2–3	1–2			
Jumper	Type	P–9	P–10		(U7)	Configuration set–up for	
(P9)		P–11	P–12		(U8)	devices U7 thru U12.	1–2
(P10)		P–13	P–14		(U9)		2–3
(P11)		P–15	P–16		(U10)		1–2
(P12)		P–17	P–18		(U11)		2–3
(P13)		P–19	P–20		(U12)		1–2
(P14)	2016	2–3	1–2				2–3
(P15)	2732	1–2	1–2				1–2
(P16)	2764	1–2	1–2				2–3
(P17)	6264	1–2	2–3				1–2
(P18)							2–3
(P19)							1–2
(P20)							2–3
Jumper	Type	P23	P22	P21	Adrs	Enable address decoding –	
(P21)	(8)2732	In	In	In	0000	for unpaged memory	Out
(P22)	(8)2764	In	In	Out	0000		In
(P23)	(8)2016	In	Out	In	4000		In
	(8)2016	In	Out	Out	8000		
	(8)2016	Out	In	In	C000		
	(7)2732	Out	In	Out	0000		
	(2)2016	Out	Out	In	7000		
		Out	Out	Out			
Jumper (P24)	1–2 2–3				Paging disabled. Paging enabled.		1–2
Strap	None Used						
DIP Switch	None Used						
Rotary Switch	None Used						

(continued)

Table 3–1
EPROM circuit pack (A2 and B2) options part number: NT6M63BF, NT6M63CL, NT6M63CH, NT6M63CF; BCS21–up DPP w/o 56K polling

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Switch	None Used			

Notes:
Note 1: See Figure 3–1.
Note 2: There are no customer–definable options on this circuit pack. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

End

Table 3–2
EPROM circuit pack (A2 and B2) options – part number: NT6M63CJ; DPP w/ 56K polling

Device type (number)	Position/setting					Function	Setting Factory On–site
Jumper (P2)		In Out				No DRAM circuit pack Use with DRAM circuit pack	 Out
Jumper	Type	P3	P4	P5	(U5)	Configuration set–up for	
(P3)		P6	P7	P8	(U6)	devices U5 and U6.	1–2
(P4)	2016	1–2	1–2	2–3			1–2
(P5)	2782	1–2	1–2	1–2			1–2
(P6)	2764	1–2	1–2	1–2			1–2
(P7)	6264	2–3	1–2	1–2			1–2
(P8)	27128	1–2	2–3	1–2			1–2
Jumper	Type	P–9	P–10		(U7)	Configuration set–up for	
(P9)		P–11	P–12		(U8)	devices U7 thru U12.	1–2
(P10)		P–13	P–14		(U9)		2–3
(P11)		P–15	P–16		(U10)		1–2
(P12)		P–17	P–18		(U11)		2–3
(P13)		P–19	P–20		(U12)		1–2
(P14)	2016	2–3	1–2				2–3
(P15)	2732	1–2	1–2				1–2
(P16)	2764	1–2	1–2				2–3
(P17)	6264	1–2	2–3				1–2
(P18)							2–3
(P19)							1–2
(P20)							2–3
Jumper	Type	P23	P22	P21	Adrs	Enable address decoding –	
(P21)	(8)2732	In	In	In	0000	for unpaged memory	Out
(P22)	(8)2764	In	In	Out	0000		In
(P23)	(8)2016	In	Out	In	4000		In
	(8)2016	In	Out	Out	8000		
	(8)2016	Out	In	In	C000		
	(7)2732	Out	In	Out	0000		
	(7)2016	Out	Out	In	7000		
		Out	Out	Out			
Jumper (P24)		1–2 2–3				Paging disabled. Paging enabled.	1–2
Strap		None Used					
DIP Switch		None Used					

(continued)

Table 3–2
EPROM circuit pack (A2 and B2) options – part number: NT6M63CJ; DPP w/ 56K polling

Device type (number)	Position/setting	Function	Setting Factory On–site
Rotary Switch	None Used		
Switch	None Used		
	End		

Memory expansion circuit pack

General description

The Expanded Memory circuit pack in slot 3 of the A and B chassis provides Dynamic Random Access Memory (DRAM) for temporarily storing various data in the DPP. DRAM is refreshed periodically by the CPU to maintain its programmed state. Each expanded memory circuit pack contains up to 256 Kbytes (262,144 bytes) of DRAM. On the system level, DRAM provides storage of temporary data, such as system calculations, and updating of statistics.

See Table 4–1 for the jumper option settings on this circuit pack (these are standard, not user–defined). Figure 4–1 shows jumper location and circuit pack layout.

Replacing the Memory Expansion circuit pack

To replace the Memory Expansion circuit pack, use the following procedure.

Procedure 4–1
Replacing the Memory Expansion circuit pack

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty DRAM is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc red rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.

(continued)

Procedure 4–1
Replacing the Memory Expansion circuit pack (continued)

Step	Description	Notes
8	At the maintenance terminal, enter: **>RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.
9	At the maintenance terminal, enter: **>TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **>RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

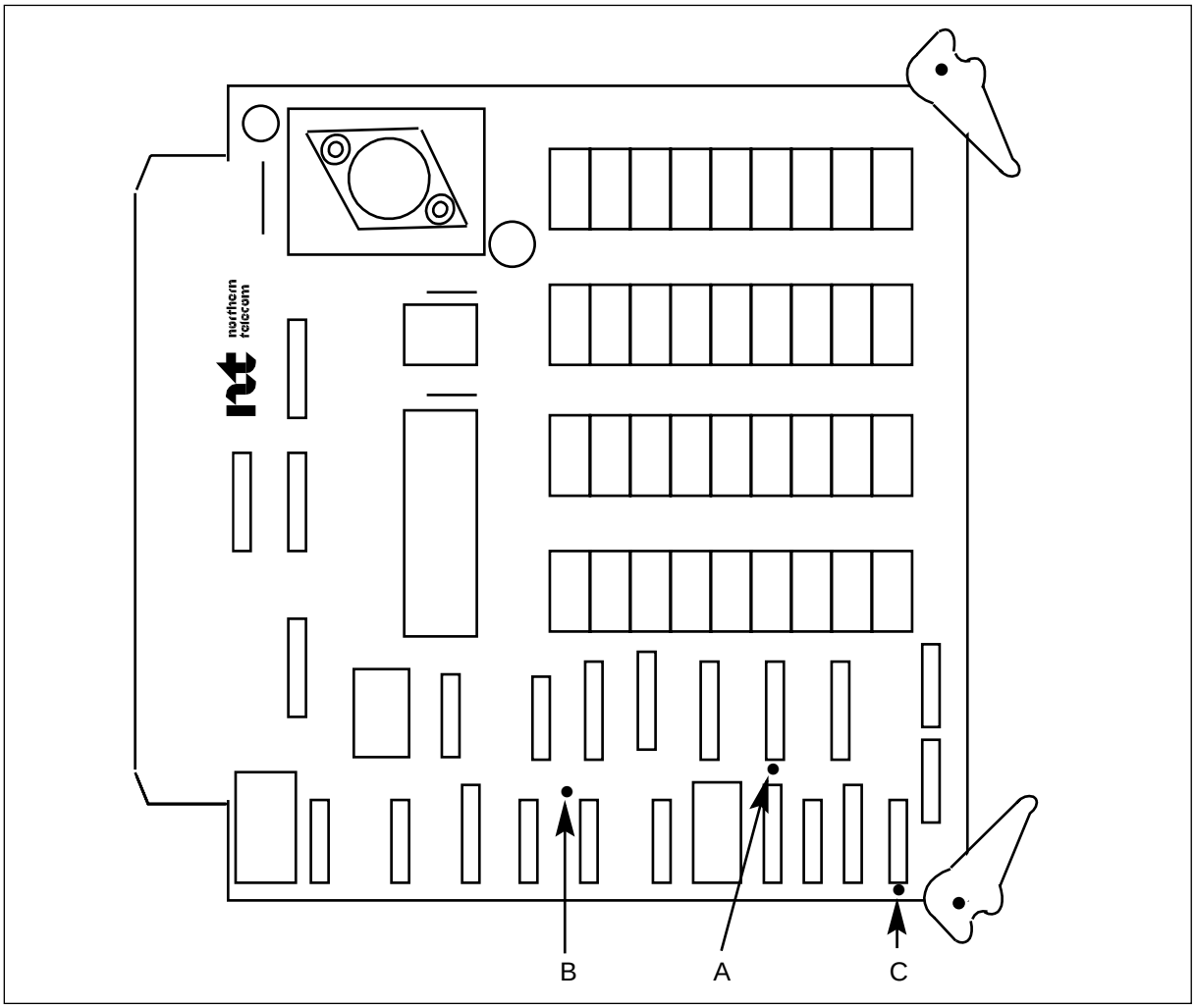
End

Table 4–1
Memory Expansion circuit pack (A3 and B3) options – part number: NT6M64AA

Device type (number)	Position/setting			Function	Setting	
					Factory	On–site
Jumper	A	B	C		B (card 1 in A3) In (All others out)	Must be the same as the factory setting.
	Out	In	Out	Card 1		
	In	In	Out	Card 2		
	Out	Out	In	Card 1 (64K only)		
	In	Out	In	Card 2 (64K only)		
Strap	None Used					
DIP Switch	None Used					
Rotary Switch	None Used					
Switch	None Used					

Notes:
Note 1: See Figure 4–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

Figure 4–1
Memory Expansion circuit pack (A3 and B3) circuit pack (NT6M64AA) options



Error Control II and Error Control II Jumper circuit packs

General description

The Error Control II circuit pack is located in slot 5 of the A chassis, and the Error Control II Jumper circuit pack is in slot 5 of the B chassis.

The Error Control II circuit pack constantly checks the system to verify satisfactory operation and to immediately sense and react to a fault. The Error Control II Jumper circuit pack contains a loop to feed data from the B processor bus to the Error Control II circuit pack in the A chassis. This jumper also has a switch to bypass the Error Control II circuit pack if it needs replacing.

On the system level, the Error Control II circuit pack regulates the status lamps, alarms, and the Processor A Select (ASEL) line directing which processor (A or B) currently controls the DPP.

This circuit pack contains no customer–selectable option settings. See Table 5–1 and Figure 5–1 for the circuit pack layout.

Error control II circuit pack LED

This LED on the front edge of the circuit pack indicates that the self–tests performed by the Error Control II circuits have failed. If this occurs, processor (A and B) status is "frozen." This requires immediate attention to prevent possible data loss if the PRIME status processor develops a fault. Without the Error Control II circuit pack circuits fully operational, the processors probably cannot "switch" if a malfunction occurs.

If there is a minor problem during the test, the LED lights and immediately dims. However, if the LED stays lit, check the MAP output for failure indications. See *DPP Alarm Clearing and Performance Monitoring Procedures* (297–1001–543) for repair procedures.

Error control II circuit pack jumper LED

The LED on the Error Control II Jumper circuit pack (slot 5; B chassis) lights to indicate the toggle switch on the circuit pack has been activated, up position. This toggle switch is activated during replacement of the Error Control II circuit pack (slot 5; A chassis). See Table 5–1.

CAUTION
Do not activate the toggle switch unless performing maintenance activity (replacing Error Control II circuit pack) and the Error Control II circuit pack replacement circuit pack is immediately available.

Replacement procedures

When replacing the Error Control II circuit pack in slot A5 (A chassis), use the following procedure.

Procedure 5–1
Replacing Error control II circuit pack (A5)

CAUTION

Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of the grounding strap.

Step	Description	Notes
1	Remove both front panels (A and B) of the DPP.	Loosen the four captive screws on the left and right hand sides of the chassis. See Figure 5–1.
2	Pull the front panels free of the chassis.	Put the panels in a safe place to avoid scratching and bending.
3	Make sure the DPP is in B ONLY processor mode.	Make the A/B select switch indicate the B processor. Set the O/P select switch to O. Turn mode insert key and release.
4	On the Error Control II Jumper circuit pack in the B chassis (B5), pull the toggle switch outward and lift the switch to the up position.[1]	Switch serves a dual function. First, remove the B chassis power–feed from the Error Control II circuit pack in the A chassis. The toggle locks the error control functions to the B chassis.
5	Power down the A chassis by pressing down the red rocker switch to 0.	
6	Replace the Error Control II circuit pack in the A chassis.	Slot 5.

(continued)

Procedure 5–1
Replacing Error control II circuit pack (A5) (continued)

Step	Description	Notes
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them.	
7	Return power to the A chassis using the rocker switch on the power supply.	Wait for power–up activity to end and the message "S/W Loaded" to print.
8	Return the toggle switch on the Error Control II Jumper circuit pack in B5 to the down (LED off) position.	This unlocks the Error Control functions. The B processor may print out this message: `EC–IC–ALM` (this is normal)
9	At the maintenance terminal, enter: **RSERR ACT 00 (cr)** then, **RSERR STDBY 00 (cr)**	To clear any alarms on the active and standby chassis. Perform any necessary activities to respond to any alarms or error messages.

(continued)

Procedure 5–1
Replacing Error control II circuit pack (A5) (continued)

Step	Description	Notes
10	At the front panel: Set the A/B switch to B Set the O/P switch to P Turn the key switch.	Set the processor status to B PRIME.
11	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	
12	Put the front panels back on the DPP. Position them on the chassis and tighten the four captive screws on the left and right hand sides of each chassis.	Do not overtighten the screws.

Notes:
Note 1: LED display on the CPU (slot A1) may be invalid at this point; ignore the display, proceed.

End

Replacement procedures

When replacing the Error Control II Jumper circuit pack, use the following procedure.

Procedure 5–2
Replacing Error control II Jumper circuit pack

CAUTION

Since all DPP circuit packs are static sensitive, observe all precautionary measures.

CAUTION

Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of the grounding strap.

Step	Description	Notes
1	Make sure the DPP is in A ONLY processor mode.	Press A/B to A. Press O/P to O. Turn mode insert key and release.
2	Remove power from the B chassis by pressing the red rocker switch to 0.	
3	Replace the Error Control II Jumper circuit pack in the B chassis.	Slot 5.
4	Return power to the B chassis using the rocker switch on the power supply.	Wait for power–up activity to end and the message "S/W Loaded" to print.
5	Key to AP processor mode.	Press O/P to P and key.

(continued)

Procedure 5–2
Replacing Error control II Jumper circuit pack (continued)

Step	Description	Notes
6	At the maintenance terminal, enter: **RSERR ACT 00 (cr)** then, **RSERR STDBY 00 (cr)**	To clear any alarms on the active and standby chassis. Perform any necessary activities to respond to any alarms or error messages.
7	At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	
	End	

Table 5–1
Error control II circuit pack (A5) options – part number: NT6M65AA

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	None Used			
Strap	None Used			
DIP Switch	None Used			
Rotary Switch	None Used			
Switch	None Used			

Notes:
Note 1: See Figure 5–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

End

Table 5–2
Error control II jumper circuit pack (B5) options – part number: NTM609AB

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	None Used			
Strap	None Used			
DIP Switch	None Used			
Rotary Switch	None Used			
Switch toggle (SW1)	On = up position = power cut to Error Control II circuit pack in A5 is off.[3]	Error control functions transferred to this circuit pack.	Used only during corrective maintenance on the Error Control II circuit pack (A5): see 297–1001–543 for more information.	
	Off = down position = power feed to Error Control II circuit pack in A5 is on.	Error control functions operate normally.		

Notes:
Note 1: See Figure 5–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.
Note 3: The LED (DS1) lights when toggle switch (SW1) is moved to the (up) On position.

Figure 5–1
Error control II (A5) circuit pack (NT6M65AA) options

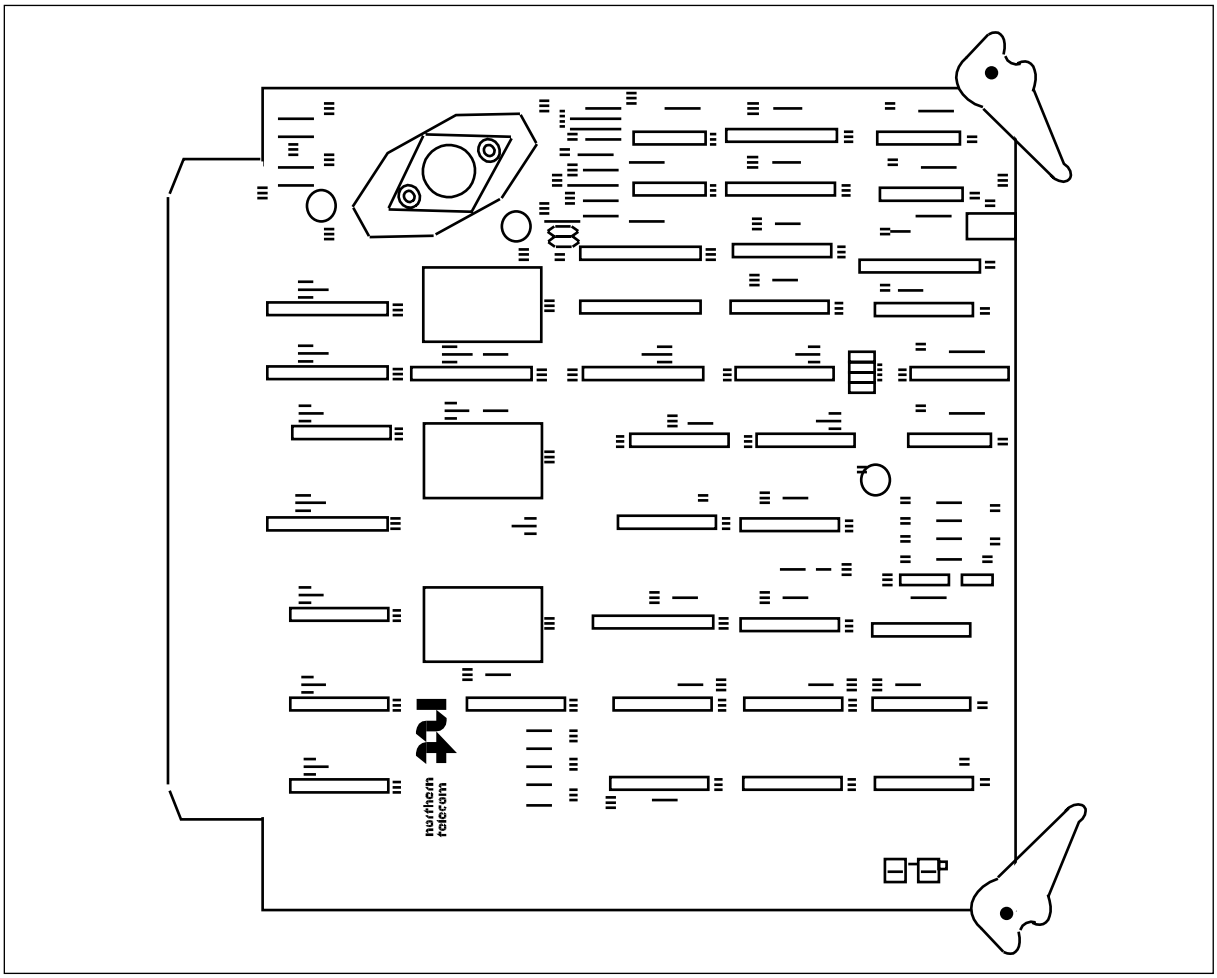
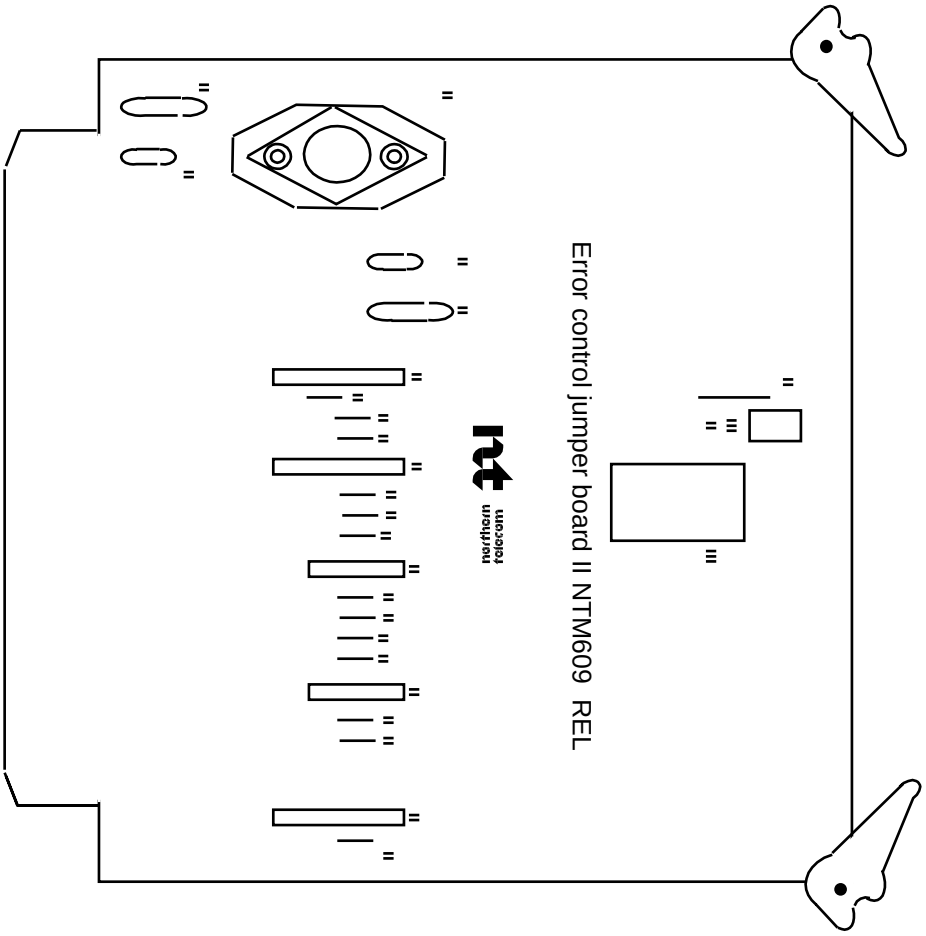


Figure 5–2
Error control II jumper (B5) circuit pack (NTM609AB) options



Note: LED (DS1) lights when toggle switch (SW1) is moved to the (up) On position.

QSIO circuit pack

General description

Located in slot 6 of each chassis, the Quad Serial input/output (QSIO) has one port for maintenance terminal communications, one port for polling call record data if 56K polling feature is unequipped, and two ports for the I/O controllers for serial communication with the DMS–100 (MAP). Each port maintains an independent, selectable baud rate for the transmit and receive functions. On later release QSIOs the transmit clock may be generated externally or internally. On the NT6M60AA QSIO, the receive clock can be set for internal only. On the NT6M60BA QSIO, the receive clock can be set for internal or external. See Table 6–1.

The QSIO circuit pack is a peripheral I/O device to the DPP on–line processor. It provides an interface to system data, addresses, and control signals. The eight–bit data bus is powered by a tristate octal bus transceiver circuit under the active processor's control. The eight address lines are also driven by the active processor, four of them buffered by a tristate octal buffer. Another tristate octal buffer circuit buffers the ten control lines used by the processor.

The QSIO circuit pack reports internal faults to the active processor by generating signal interrupts. To minimize the signal's propagation delay through the circuit pack, a bypass circuit is used in the Programmable Array Logic (PAL). The interrupt output (–INT) is buffered by a quad z–input positive NAND buffer chip to connect to the system interrupt line.

The QSIO circuit pack includes two dual baud rate circuits, plus circuitry to select the clocking source. Each channel of the SIO chips requires two separate clocks: one for transmit and one for receive. Either clock may be generated internally on the circuit pack or externally. For externally generated clocks, the SIO chips are fed by the two identical baud rate circuits, each supporting a single SIO chip. Each circuit generates two baud rate clocks. As a result, if internally generated clocks are selected, the transmit and receive clocks for that channel must operate at the same rate, since only one baud rate clock may be produced for each channel.

The settings on each SIO channel baud rate selector switch correspond to different baud rates. These rates differ for synchronous and asynchronous

ports. Since the SIO channels have both synchronous and asynchronous ports, the baud rates corresponding to the switch settings are not the same for all SIO baud switches.

Note: Enter the baud rate set command BAUD to establish software control of the QSIO channel. See 297–1001–543 *DPP Alarm Clearing and Performance Monitoring* for further information.

Replacing QSIO circuit pack

Use the following procedure when replacing this circuit pack.

Procedure 6–1
Replacing the QSIO circuit pack

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty QSIO is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.

(continued)

Procedure 6–1
Replacing the QSIO circuit pack (continued)

Step	Description	Notes
8	At the maintenance terminal, enter: **>RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.
9	At the maintenance terminal, enter: **>TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **>RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Table 6–1
QSIO circuit pack (A6 and B6) options – part number: NT6M60AA

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (A)	In	+12 V dc, if BR1941 chip is used.	In	Must be the same as the factory setting.
	Out	No +12 V dc if WD1943 chip is used.		
Strap	None used			
DIP Switch (S2)	S2–1 Baud A to RXCA S2–2 RCA to RXCA S2–3 Baud B to RXCB S2–4 RCB to RXCB	DIP switches S2 and S3 are used to select synchronous or asynchronous mode for the four channels of the QSIO. The baud rate selection and mode of operation at rotary switches S4, S5, S6, and S7 is controlled by S2 and S3 according to the following chart.	Off On On Off	Must be the same as the factory setting.
DIP Switch (S3)	S3–1 Baud C to RXCA S3–2 RCC to RXCA S3–3 Baud D to RXCB S3–4 RCD to RXCB		On Off On Off	

Note: This PCB will *only* allow external timing to be set in the modem.

DIP switch	Controls the operation of	Select synchronous	Select asynchronous
S2–1 S2–2	S4	Off On	On Off
S2–3 S2–4	S5	Off On	On Off
S3–1 S3–2	S7	Off On	On Off
S3–3 S3–4	S6	Off On	On Off

(continued)

Table 6–1
QSIO circuit pack (A6 and B6) options – part number: NT6M60AA (continued)

Device type (number)	Position/setting			Function	Setting	
					Factory	**On–site**
DIP Switch (S1)	Position 0 1 2 3 4	= 5 6 7 8 9	Address A B C D E F	Select the logical address of the SIO circuits.	A	Must be the same as the factory setting.

Note: Baud rate selection for the four DPP channels is made at the four rotary switches (S4, S5, S6, and S7) on the front of the circuit pack. The baud rate selected can be set for synchronous or asynchronous operation at S2 and S3. The chart shows conversion for asynchronous to synchronous baud rates and rotary switch position for the applicable selection.

Switch position	Asynch rate	Synch rate	Switch position	Asynch rate	Synch rate
0	50	800	8	1800	N/A
1	75	1200	9	2000	N/A
2	110	1760	A	2400	N/A
3	134.5	2152	B	3600	N/A
4	150	2400	C	4800	N/A
5	300	4800	D	7200	N/A
6	600	9600	E	9600	N/A
7	1200	19200[6]	F	19200[6]	N/A

Rotary Switch (S4)	0 1 2 3 4 5 6 7	50 75/1200 110 134.5 150/2400 300/4800 600/9600 1200	8 9 A B C D E F	1800 2000 2400 3600 4800 7200 9600 19200[6]	BX.25 Polling Link (Synchronous channel; 2400 baud) Channel A baud rate select. (Odd numbers appear as dashes on the face of the rotary switch.)	5 (4800 baud) (This switch is inactive for DPP systems with 56K polling.)	May be 4, 5, or 6, depending on the polling speed.

(continued)

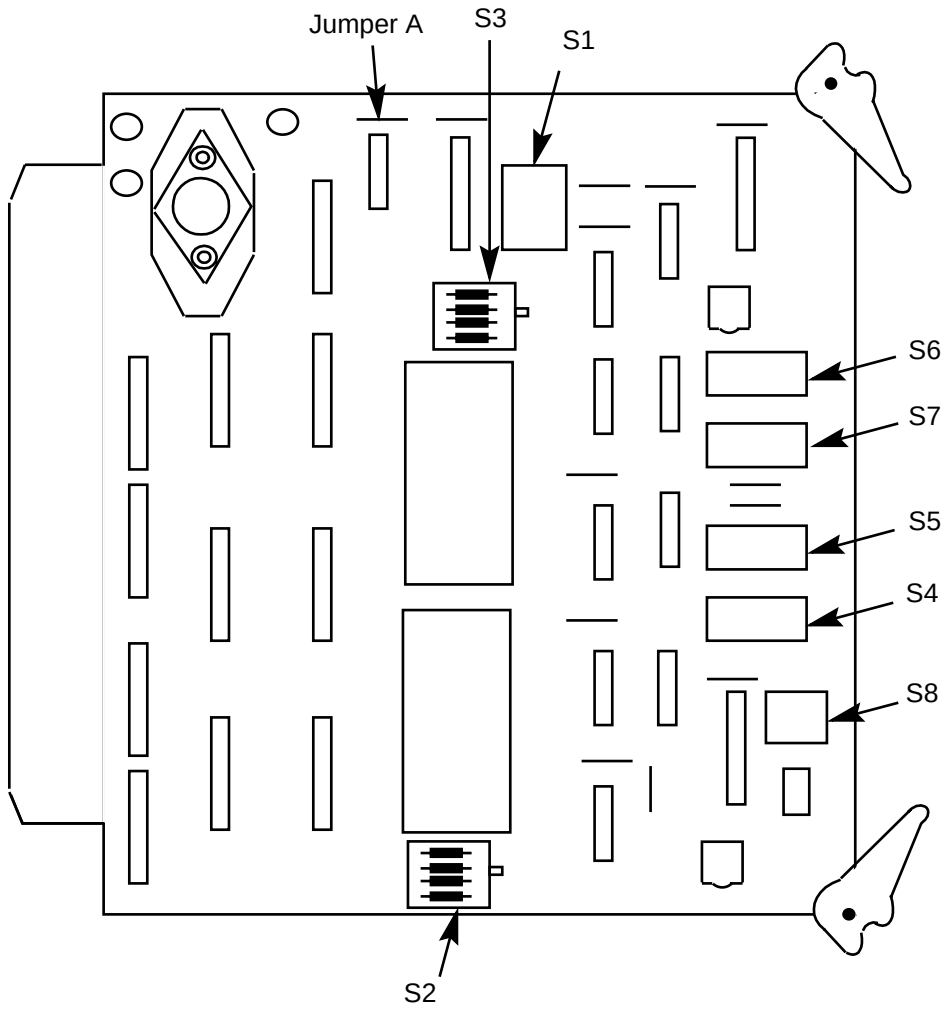
Table 6–1
QSIO circuit pack (A6 and B6) options – part number: NT6M60AA (continued)

Device type (number)	Position/setting				Function	Setting	
						Factory	On–site
Rotary Switch (S5)	0 1 2 3 4 5 6 7	50 75/1200 110 134.5 150/2400 300/4800 600/9600 1200	8 9 A B C D E F	1800 2000 2400 3600 4800 7200 9600 19200[3]	IOC Link (MMI Link to DMS–100) (Asynchronous channel; 2400 baud) Channel B baud rate select. (Odd numbers appear as dashes on the face of the rotary switch.)	A (2400 baud)	
Rotary Switch (S7)	0 1 2 3 4 5 6 7	50 75/1200 110 134.5 150/2400 300/4800 600/9600 1200	8 9 A B C D E F	1800 2000 2400 3600 4800 7200 9600 19200[4]	IOC Link (MMI Link to DMS–100) (Asynchronous channel; 2400 baud) Channel C baud rate select. (Odd numbers appear as dashes on the face of the rotary switch.)	A (2400 baud)	
Rotary Switch (S6)	0 1 2 3 4 5 6 7	50 75/1200 110 134.5 150/2400 300/4800 600/9600 1200	8 9 A B C D E F	1800 2000 2400 3600 4800 7200 9600 19200[5]	Local Printer – (Asynchronous channel; 2400 baud) Channel D baud rate select. (Odd numbers appear as dashes on the face of the rotary switch.)	A (2400 baud) (Rover terminal; typically not used)	
Switch	None used						

Notes:
Note 1: See Figure 6–1.
Note 2: This circuit pack does not support polling on digital data lines; use for an analog network only.
Note 3: The MMI Link (DPP to DMS–100 two–way communication channel connected to connector J2 is MMI Link 1.
Note 4: The MMI Link (DPP to DMS–100 two–way communication channel connected to connector J3 is MMI Link 2.
Note 5: Listed for reference only; not supported in software.

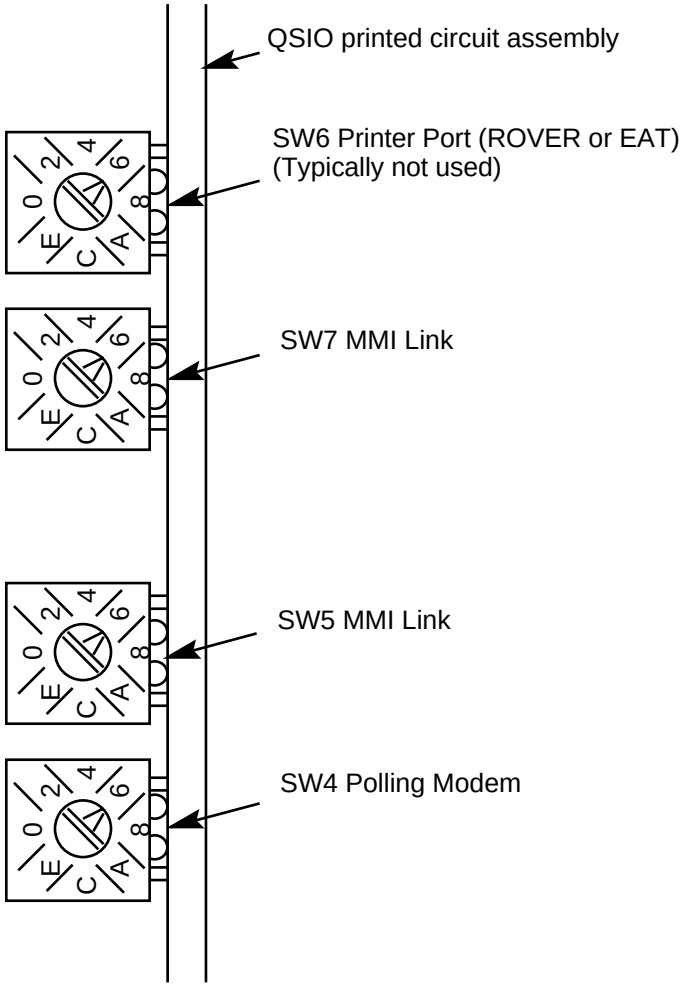
End

Figure 6–1
QSIO (A6 and B6) circuit pack (NT6M60AA) options



Note: This circuit pack does not support polling on digital data lines; use for an analog network only .

Figure 6–2
QSIO (A6 and B6) circuit pack (NT6M60AA) baud rate selector switches



Note: SW4 (polling modem) is inactive if 56K polling is used.

Table 6–2
QSIO circuit pack (A6 and B6) options – part number: NT6M60BA

Device type (number)		Position/setting	Function	Setting	
				Factory	On–site
Jumper (J2)	1–2 2–3	Transmit internal Transmit external	Channel A transmit clock	1–2	
Jumper (J3)	1–2 2–3	ASYNC SYNC	Channel A receive clock	2–3	

Table 6–2
QSIO circuit pack (A6 and B6) options – part number: NT6M60BA (continued)

Device type (number)		Position/setting	Function	Setting	
				Factory	**On–site**
Jumper (J4)	1–2 2–3	Transmit internal Transmit external	Channel B transmit clock	1–2	
Jumper (J5)	1–2 2–3	ASYNC SYNC	Channel B receive clock	1–2	
Jumper (J6)	1–2 2–3	Transmit internal Transmit external	Channel C transmit clock	1–2	
Jumper (J7)	1–2 2–3	ASYNC SYNC	Channel C receive clock	1–2	
Jumper (J8)	1–2 2–3	Transmit internal Transmit external	Channel D transmit clock	1–2	
Jumper (J9)	1–2 2–3	ASYNC SYNC	Channel D receive clock	1–2	
Jumper (J10)	In Out	Select internal timing source (DPP). Select external timing source (Modem).	Select internal or external source for channel A transmit clock	In	
Jumper (J11)	In Out	Select internal timing source (DPP). Select external timing source (Modem).	Select internal or external source for channel B transmit clock	In	
Jumper (J12)	In Out	Select internal timing source (DPP). Select external timing source (Modem).	Select internal or external source for channel C transmit clock	In	
Jumper (J13)	In Out	Select internal timing source (DPP). Select external timing source (Modem).	Select internal or external source for channel D transmit clock	In	
Strap		None used			

(continued)

Table 6–2
QSIO circuit pack (A6 and B6) options – part number: NT6M60BA (continued)

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
DIP Switch (S6)	1 On channel A select Off (normal setting)	NOT USED.	Off	
	2 On channel B select Off (normal setting)		Off	
	3 On channel C select Off (normal setting)		Off	
	4 On channel D select Off (normal setting)		Off	

Note: Baud rate selection for the four DPP channels is made at the four rotary switches (S2, S3, S4, and S5) on the front of the circuit pack. The baud rate selected can be for a synchronous channel or an asynchronous channel. The following chart provides the conversion for asynchronous to synchronous baud rates and the rotary switch position for the applicable selection.

Switch position	Asynch rate	Synch rate	Switch position	Asynch rate	Synch rate
0	50	800	8	1800	N/A
1	75	1200	9	2000	N/A
2	110	1760	A	2400	N/A
3	134.5	2152	B	3600	N/A
4	150	2400	C	4800	N/A
5	300	4800	D	7200	N/A
6	600	9600	E	9600	N/A
7	1200	19200[7]	F	19200[7]	N/A

Rotary Switch (S2)	0	50	8	1800	BX.25 Polling Link (Synchronous channel; 2400 baud) Channel A baud rate select.	4 (2400 baud) (This switch is inactive for DPP systems with 56K polling.)
	1	75/1200	9	2000		
	2	110	A	2400		
	3	134.5	B	3600		
	4	150/2400	C	4800		
	5	300/4800	D	7200		
	6	600/9600	E	9600		
	7	1200	F	19200[7]		
Rotary Switch (S3)	0	50	8	1800	MMI Link (Asynchronous channel; 2400 baud) Channel B baud rate select.	A (2400 baud)
	1	75/1200	9	2000		
	2	110	A	2400		
	3	134.5	B	3600		
	4	150/2400	C	4800		
	5	300/4800	D	7200		
	6	600/9600	E	9600		
	7	1200	F	19200[7]		

(continued)

Table 6–2
QSIO circuit pack (A6 and B6) options – part number: NT6M60BA (continued)

Device type (number)	Position/setting				Function	Setting	
						Factory	On–site
Rotary Switch (S4)	0	50	8	1800	MMI Link (Asynchronous channel; 2400 baud) Channel C baud rate select.	A (2400 baud)	
	1	75/1200	9	2000			
	2	110	A	2400			
	3	134.5	B	3600			
	4	150/2400	C	4800			
	5	300/4800	D	7200			
	6	600/9600	E	9600			
	7	1200	F	19200[7]			
Rotary Switch (S5)	0	50	8	1800	Local Printer – (Rover terminal; typically not used) (Asynchronous channel; 2400 baud) Channel D baud rate select.	A (2400 baud)	
	1	75/1200	9	2000			
	2	110	A	2400			
	3	134.5	B	3600			
	4	150/2400	C	4800			
	5	300/4800	D	7200			
	6	600/9600	E	9600			
	7	1200	F	19200[7]			

(continued)

Table 6–2
QSIO circuit pack (A6 and B6) options – part number: NT6M60BA (continued)

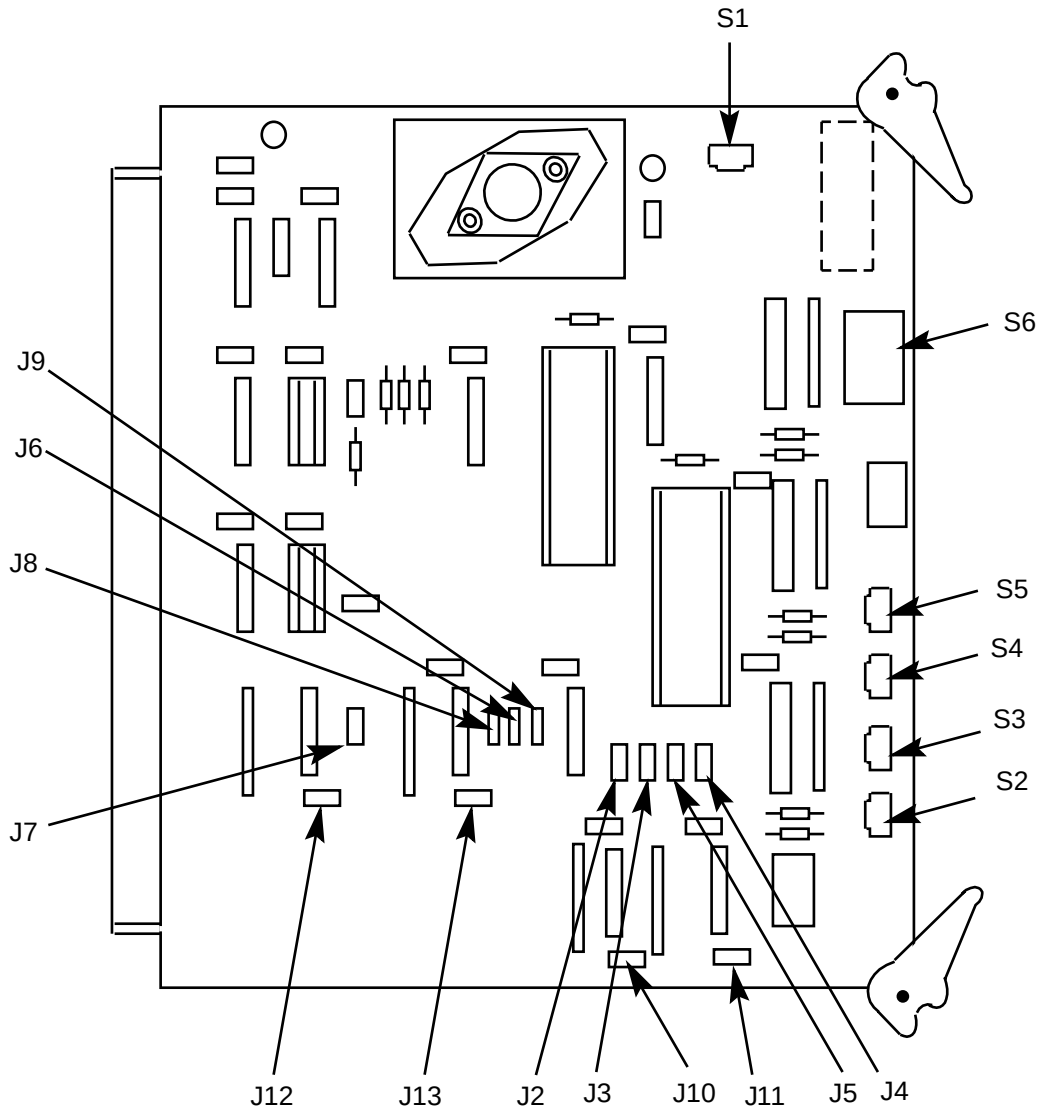
Device type (number)	Position/setting			Function	Setting	
					Factory	On–site
DIP Switch (S1)	Position 0 1 2 3 4	= 5 6 7 8 9	Address A B C D E F	Select the logical address of the SIO circuits.	A	Must be the same as the factory setting.

Notes:
Note 1: See Figure 6–1.
Note 2: This circuit pack supports polling on digital data lines or on analog network. For digital data lines check that:
a. the P/A Comm circuit pack at A16 is part number NT6M84BA
b. the Four Channel COMM circuit pack at A17 is release 03 or later
c. the Collector supports the digital data line feature.
Note 3: Factory settings shown are for an analog network.
Note 4: The internal transmit timing source is generated on the QSIO circuit pack. The external transmit timing source is brought in from a source outside the DPP, usually associated with a modem generated timing source from a digital data line.
Note 5: The MMI Link (DPP to DMS–100 two–way communication channel) connected to connector J2 is MMI Link 1.
Note 6: The MMI Link (DPP to DMS–100 two–way communication channel) connected to connector J3 is MMI Link 2.
Note 7: Listed for reference only; not supported in software.

Usage Notes:
Note 1: Use the following guidelines to determine the on–site settings for J2 through J13:
If BX.25 polling is being done over a digital data line:
a. J2 2–3 external transmit clock timing for channel A.
b. J10 Out external transmit clock timing for channel A.
c. Verify that the settings on QSIO J2–J13 agree with the settings on the P/A Comm (A16) circuit pack when working with digital data lines.
Note 2: SW4 (BX.25 polling baud rate) (for DPP w/o 56K polling)
4 for 2400 baud
5 for 4800 baud
6 for 9600 baud
Note 3: SW5 (local printer speed) 7 for 1200 baud

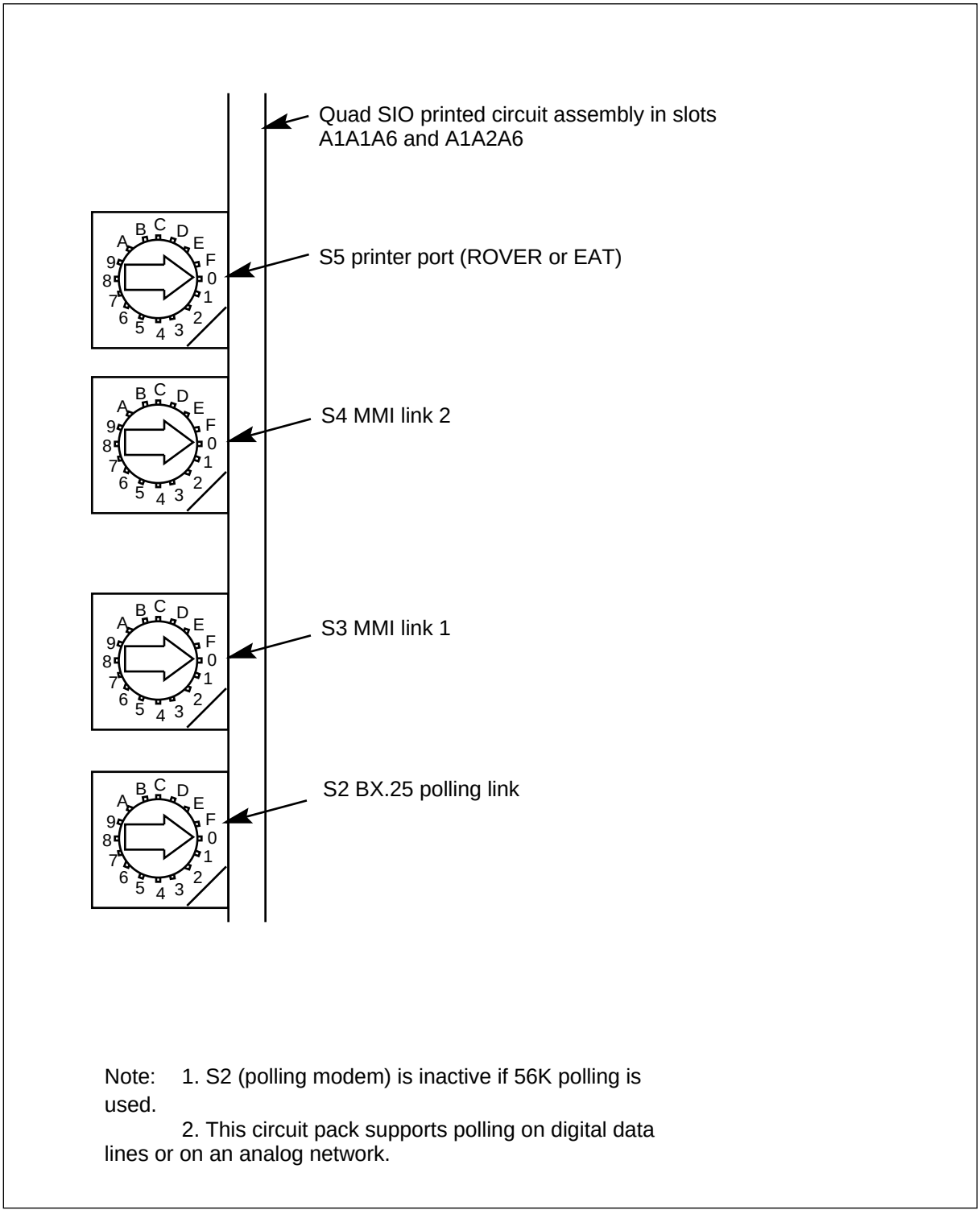
End

Figure 6–3
Quad SIO (A6 and B6) circuit pack (NT6M60BA) options



Note: This circuit pack supports polling on digital data lines or on an analog network.

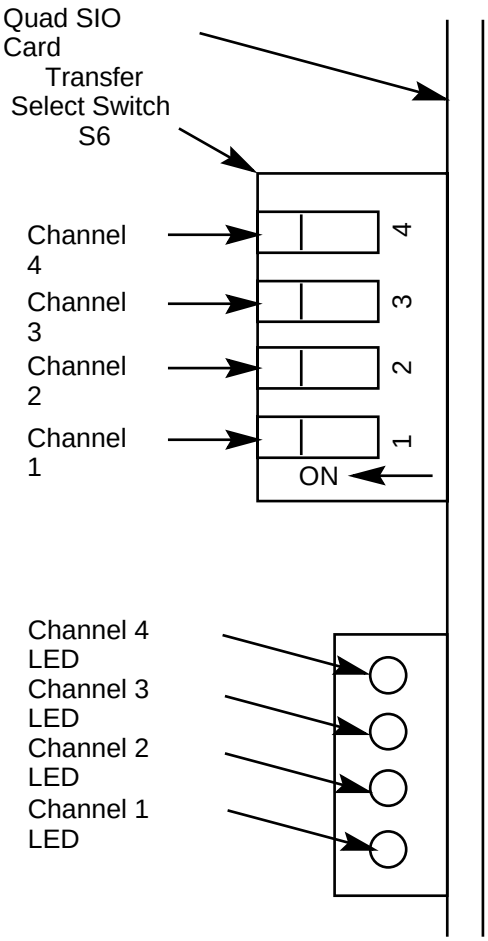
Figure 6–4
Quad SIO (A6 and B6) circuit pack (NT6M60BA) baud rate selector switches



Note: 1. S2 (polling modem) is inactive if 56K polling is used.

2. This circuit pack supports polling on digital data lines or on an analog network.

Figure 6–5
Quad SIO (A6 and B6) circuit pack (NT6M60BA) peripheral switches and indicators



SWITCH S8 CHANNEL POSITIONS

FUNCTION	POSITION	LED
NORMAL	OFF	OFF
FORCED STAND–BY	ON	ON

Notes:
1. This circuit pack supports polling on digital data lines or on an analog network.

2. Do not set these switches (S6–1, S6–2, S6–3, and S6–4) to the On position. This switch and LED are not active in this configuration; all S8 switch settings (1 through 4) must be off.

56K Interface circuit pack – Turbo only

General description

The 56K Interface circuit pack in slot 7 provides a dual serial communication interface function for the DPP. This circuit pack uses a Serial Communication Controller (SCC) chip which lets the DPP transmit and receive serial data at various standard software selectable programmed rates from 1200–9600 bps on channel A and 56K bps on channel B.

56K Interface circuit pack communication with the Main processor (slot 1) is based on a polling strategy as opposed to an interrupt scheme. Two FIFO (First In–First Out) buffers provide a bidirectional path between the 56K Interface circuit pack and Main processor.

The SCC port consists of an SCC chip (at U36) along with a bus interface section and CPU interface section. The SCC has a 9.8304 MHz clock from which it derives timing for SCC bus activity and SIO baud rates. A separate clock is used because the clock available on the circuit pack (12 MHz) exceeds chip capability. The 6MHz (12 MHz divided by two) provided by the CPU is too slow for adequate SCC response.

Table 7–1 shows the five option jumpers on the circuit pack. Figure 7–1 shows jumper locations and circuit pack layout.

The 56K Interface circuit pack requires +5 V dc +/– 0.25 volts. This is accomplished by the 5 volt regulator on the circuit pack which uses the +8.5 V dc supply from the backplane.

The 56K Interface circuit pack capabilities and functions include:

- Interface between DPP system backplane and 56K XOVR circuit pack.
- 512 bytes of bidirectional FIFO RAM for data passing to/from main CPU.
- Noninterrupt driven (polled) data and command port implementation allowing installation in any DPP COM (A7 and B7 used) slot without any additional backplane wiring and capable of virtually simultaneous access from either port without using WAIT states.
- Host (main CPU side) interface to support fully asynchronous access based on 4 mHz timing of standard Z80 bus cycle without wait states.

- Uses 64180 Z80 compatible CPU running at 6Mhz processor clock.
- Industry standard two channel SCC chip running at 9.8304 Mhz. With DMA interface, yields baud rates greater than 56K bps.
- 32K bytes of data RAM with plug–in sockets for up to an additional 512K bytes.
- 32K bytes to 64K bytes of boot PROM.
- Support for V.35, 56Kbps/RS–232 (1200–9600 bps) selection on the SCC ports.
- Single error detection parity guard on entire static memory.
- 50 pin access port for logic analyzer, emulator and/or test support (factory use only).
- RS–232 compatible port for local diagnostics.

The SCC has two channels of high–speed–communication–designated COM channel A and COM channel B. Under software control, it provides all necessary control, status, and data functions for both the V.35 and RS–232 interfaces supported by the 56K XOVR circuit pack. Interface to the 56K XOVR circuit pack is through the backplane via two 20 pin ribbon cables: one 40–pin cable with two 20–pin connectors.

Replacing the 56K Interface circuit pack

Use the following procedure to replace this circuit pack.

Procedure 7–1
Replacing the 56K Interface circuit pack (A7, B7)

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.[1]

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty 56K Interface pack is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.

(continued)

Procedure 7–1
Replacing the 56K Interface circuit pack (A7, B7)

Step	Description	Notes
8	At the maintenance terminal, enter: **RSERR STDBY 00** **(cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.
9	At the maintenance terminal, enter: **TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Table 7–1
56K interface circuit pack (A7 and B7) options – part number: NT6M94AA

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (P2)	Out = select card 1 In = select card 2	Card 1 or 2 address selection	Out	
Jumper (P4)	Out = 256K (27C256) In = 512K (27C512)	256K/512K EPROM enable	Out	
Jumper (P5)	Out = disable watch dog timer In = enable watch dog timer	Watch Dog enable	Out	
Jumper (P8)	Out = disable CPU clock In = enable CPU clock	CPU clock enable	In	
Jumper (P9)	Out = disable SCC clock In = enable SCC clock	SCC clock enable	In	
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Notes:
Note 1: See Figure 7–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only. This data is to be used for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set–up the same as the circuit pack being replaced.

End

High Performance DISK Interface circuit pack

General description

The High Performance (H.P.) Disk Interface circuit pack, in slot 11 of the A and B chassis, is a smart circuit assembly, with its own Z80 microprocessor, EPROM, local RAM, and dual–ported RAM. It is a peripheral of the microprocessor on the main CPU at slot 1.

The H.P. Disk Interface circuit pack is the link to the disk drive and transfers data to and from the bus used for recording on or reading from the disk. The stored program on the H.P. Disk Interface circuit pack provides the write and read commands to the disk drive.

System interface is via the 100–pin edge connector.

See Table 8–1 for the two option jumpers on the circuit pack. Figure 8–1 shows jumper locations and circuit pack layout.

Replacing the H.P. Disk Interface circuit pack

Use the following procedure to replace this circuit pack.

Procedure 8–1
Replacing the H.P. Disk Interface circuit pack (A11, B11)

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty pack is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.

(continued)

Procedure 8–1
Replacing the H.P. Disk Interface circuit pack (A11, B11) (continued)

Step	Description	Notes
8	At the maintenance terminal, enter: **RSERR STDBY 00** **(cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.
9	At the maintenance terminal, enter: **TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Table 8–1
Disk interface circuit pack (A11 and B11) options – part number: NT6M66AC and/or NT6M66AL; 72–Mbyte and 140–Mbyte disk drives

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	None used			
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Note: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

Table 8–2
Disk interface circuit pack (A11 and B11) options – part number: NT6M66AH; 380–Mbyte disk drives, DPP systems w/o 56K polling

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (A)	In = Enable disk Port interrupt Out = Disable disk Port interrupt		Same as factory.	
Jumper (R)	Watchdog timer reset		Same as factory.	
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Notes:
Note 1: See Figure 8–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only.
Note 3: Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

Figure 8–1
Disk interface (A11 and B11) circuit pack (NT6M66AH; 380–Mbyte disk drives) options

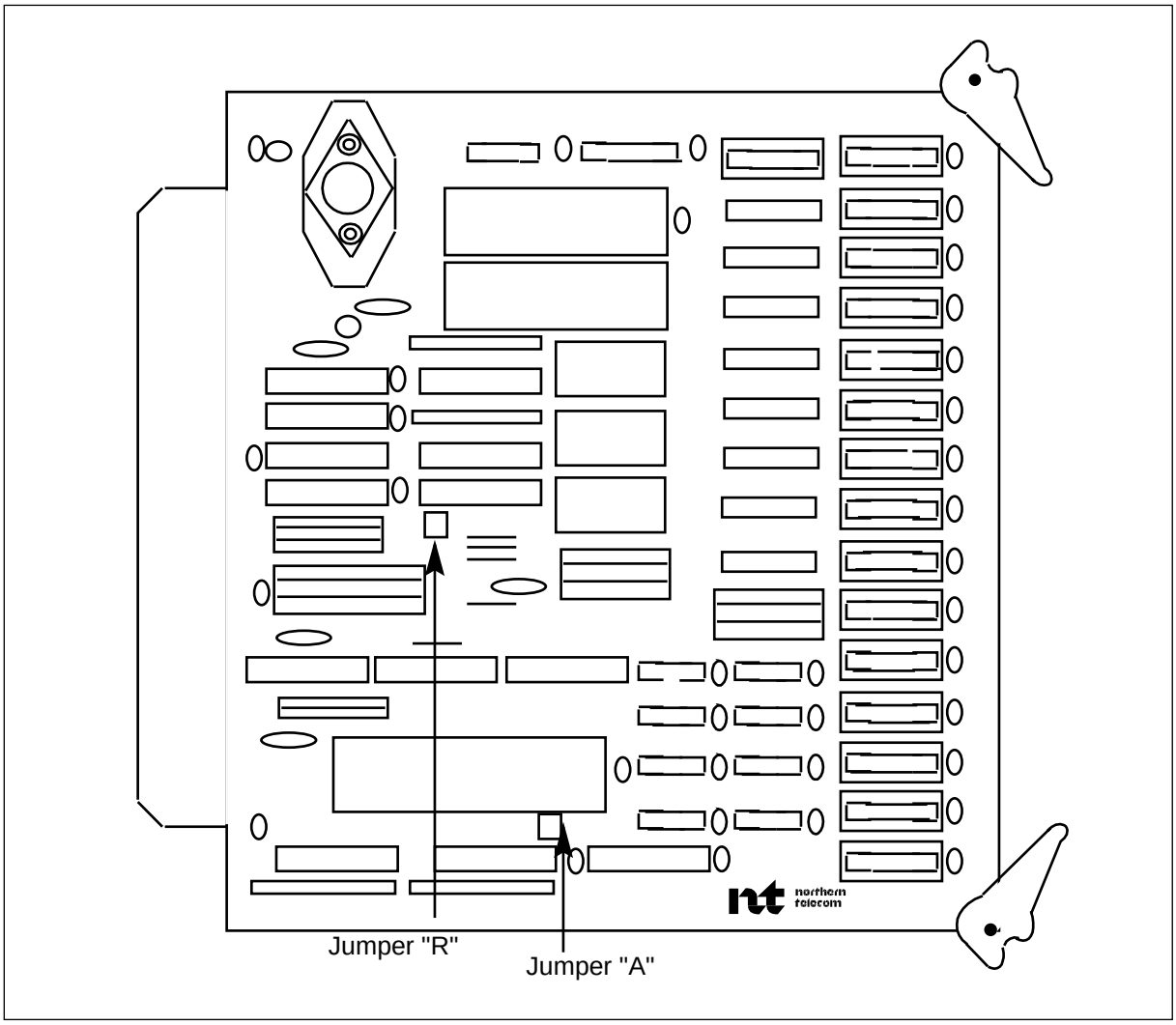


Figure 8–2
Disk interface (A11 and B11) circuit pack (NT6M66AC and NT6M66AL; 72–Mbyte and 140–Mbyte disk drives) options

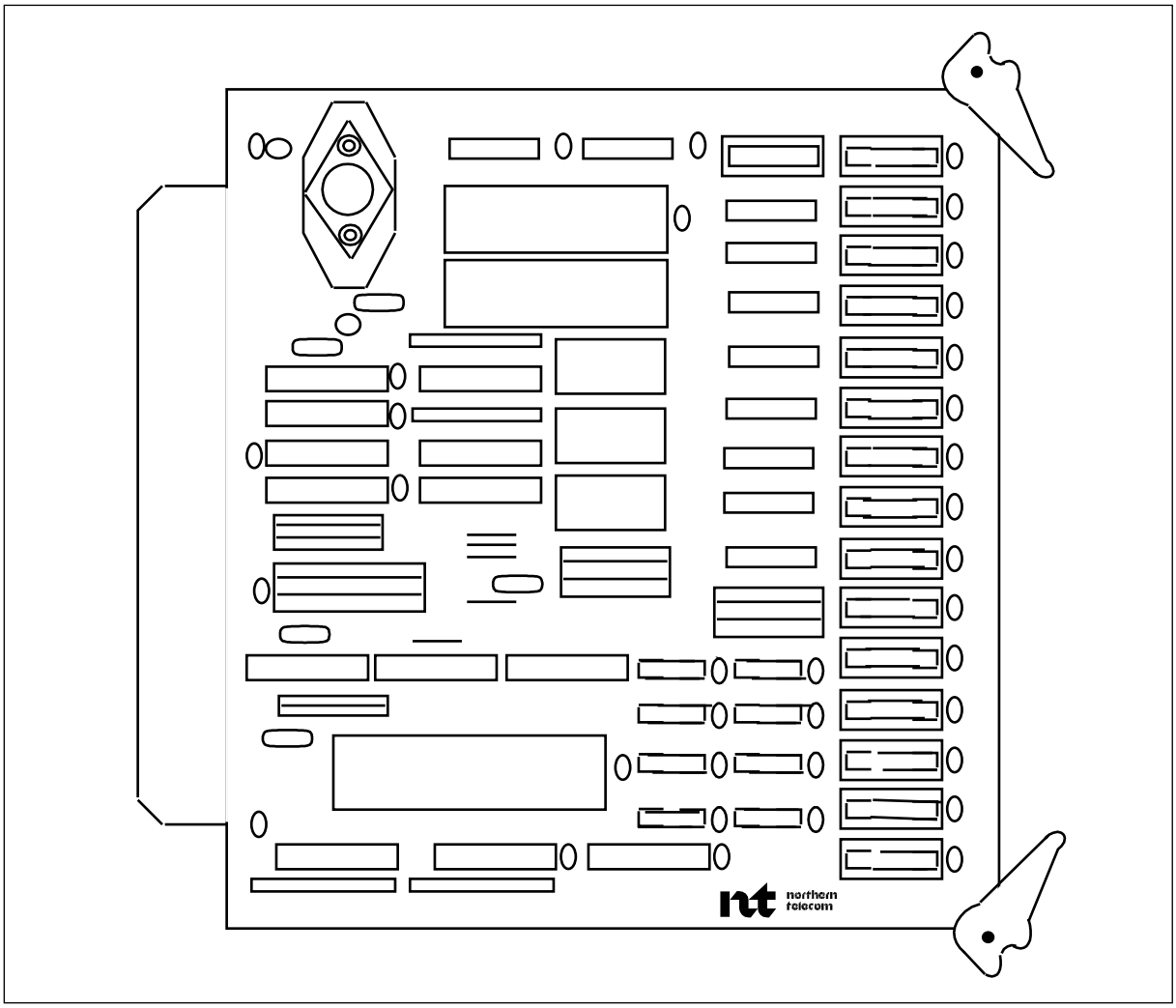


Table 8–3
Disk interface PCA (A11 and B11) options – part number: NT6M66AH; 380–Mbyte,

Device	Setting	Device	Setting
Jumper (A)	Enable disk Port Interrupt In	Jumper (R)	Watchdog timer reset In
Strap	None used	DIP Switch	None Used
Rotary Switch	None Used	Switch	None Used

Table 8–4
Disk interface PCA (A11 and B11) option references – part number: NT6M66AL; 72–Mbyte and 140–Mbyte, w/o 56K polling

Device	Setting	Device	Setting
Jumper (A)	Enable disk Port Interrupt In	Jumper (R)	Watchdog timer reset In
Strap	None used	DIP Switch	None Used
Rotary Switch	None Used	Switch	None Used

SCSI circuit pack – turbo only

General description

The Small Computer System Interface (SCSI) circuit pack, in slot 11 of the A and B chassis of the turbo DPP, is a smart circuit assembly with its own Z80 microprocessor, EPROM, local RAM, and dual–ported RAM. It is considered a peripheral of the microprocessor on the main CPU (A1).

The SCSI circuit pack is the link to the disk drive. It transfers data from and to the bus used for recording on or reading from the disk. The stored program on the SCSI circuit pack provides read and write commands to the disk drive.

This circuit pack performs a SCSI Host Adapter function and resembles an Initiator of Priority 7 to the SCSI bus. Target operation is not provided due to the complexity of an external Y type crossover network which supports redundant storage elements. 32 Kbytes of DPR are used as interface and control for commands and data to and from the Main CP at slot 1. The SCSI circuit pack provides the following capabilities:

- Interface to implement 380–Mbyte disk drives with the 56K polling feature; must be equipped when 760–Mbyte disk drives are used.
- Interface between DPP system backplane and SCSI hard disk drives.
- 32 KBytes of parity protected DPR for command and data passing to and from the Main CPU at slot 1.
- Fully transparent DPR implementation allowing virtually simultaneous access from either port without using wait states.
- Host port of DPR (Main CPU side; slot 1) designed to support fully asynchronous access based on 4 mHz timing of standard Z80 bus cycle without WAIT states.
- 6 MHz processor clock with DPR synchronized and running alternate half clock cycles. (Host cycles occur during the first half of every T state when the clock is high, while SCSI side accesses occur during the second half of each T state when the clock is low).
- NCR 5386 SCSI Bus Controller running at 10 mHz. Cycle–Steal DMA yields approximately 0.4 MBytes per second across the SCSI bus.

- 32 KBytes of data RAM with plug–in slots for up to an additional 256 Kbytes.
- Up to 64 KBytes of program PROM.
- Support for disconnect/reconnect operation on the SCSI bus.
- Single error detection parity guard on DPR memory.
- 50 pin access port for logic analyzer, emulator and test support (factory use only).
- RS–232 compatible port for local diagnostics.

System interface is via the 100–pin edge connector.

The EPROM at U3 is a 27C512 type. Removing jumper P1 and making the appropriate changes to the decode PAL at U23 allows a 27C256 type to be used.

See Table 9–1 for option settings on this circuit pack. Figure 9–1 shows the jumper locations and circuit packs' layout.

Replacing the SCSI circuit pack

Use the following procedure to replace this circuit pack.

Procedure 9–1
Replacing the SCSI circuit pack – slot 11

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.[1]

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty SCSI pack is in the standby processor.	Verify that any applicable firmware for the circuit pack is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	Check the revision level and option settings, if present, before installation.
7	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.

(continued)

Procedure 9–1
Replacing the SCSI circuit pack – slot 11 (continued)

Step	Description	Notes
8	At the maintenance terminal, enter: **RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no faults.
9	At the maintenance terminal, enter: **TEST STDBY 00 (cr)**	After RSERR, alarms may reappear. TEST forces diagnostics which confirm if the fault were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	At the maintenance terminal, enter: **RSERR ACT 00 (cr)**	To clear all alarms on the active processor. Alarms will clear if there are no faults.
12	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Figure 9–1
SCSI circuit pack (A11 and B11) NT6M66BA; 380–Mbyte Disk Drives with 56K polling and 760–Mbyte Disk Drives, and NT6M66BD; 1700–Mbyte disk drives, options

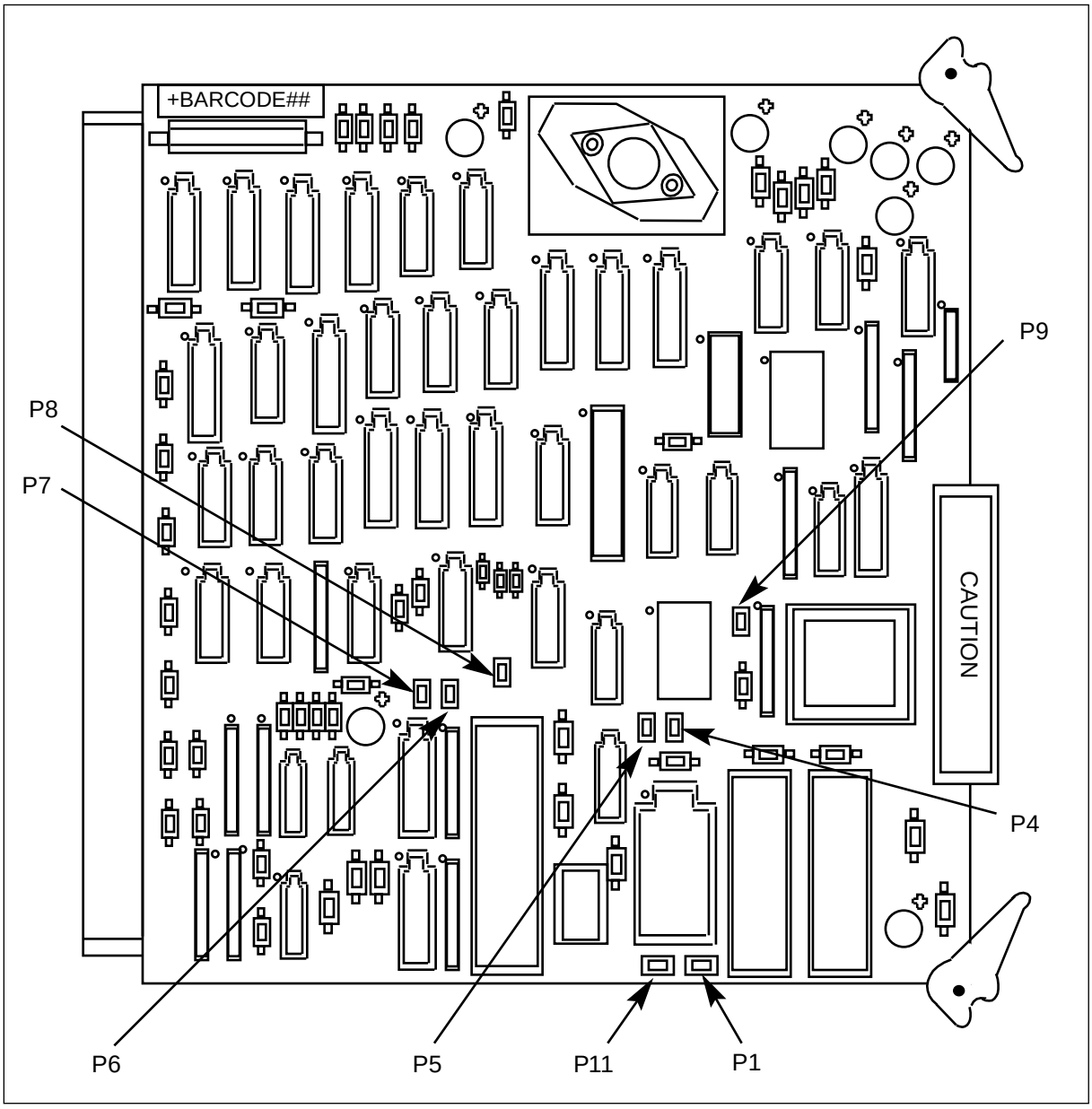


Table 9–1
SCSI circuit pack (A11 and B11) options – part number: NT6M66BA; 380–Mbyte disk drives with 56K polling and 760–Mbyte Disk Drives, and, NT6M66BD; 1700–Mbyte disk drives

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper P1	Out = 256K (27C256) In = 512K (27C512)	256K/512K EPROM enable	In	
P4	Out = NMI disable In = NMI enable	NMI control	In	
P5	Out = Watchdog disable In = Watchdog enable	Watchdog timer control	In	
P6	Out = Normal Arbitration In = Arbitration gated with BUSY	Arbitration – In position is compatible with existing disk (BCS25–28) crossover PCAs	Out	
P7	Out = BSYIN/BSYOUT separate In = BSYIN/BSYOUT tie together	In position is compatible with existing disk (BCS25–28) crossover PCAs	Out	
P8	Out = A select In = Select disk crossover A	Out position is compatible with existing disk (BCS25–28) crossover PCAs	In	
P9	Out = CPU clock disable In = CPU clock enable	CPU clock control	In	
P11	Out = SCCI clock disable In = SCCI clock enable	CPU clock control	In	

Note: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or pack replacement to make sure the replacement pack is set up the same as the pack being replaced.

Data Stream Interface circuit pack

General description

The DPP application eliminates the Magnetic Tape Devices (MTDs) used with the DMS–100 to collect AMA. Data Stream Interface (DSI) circuit packs (slots 12 and 13 in the A and B chassis) in the DPP replace the MTDs.

The DSI packs are smart circuit assemblies, each with its own Z80 microprocessors, EPROM resident software programs, and RAM. Since MTD emulation requires the DPP to maintain redundant communication with the DMS–100 Mag Tape Ports, the DSI circuit packs are active devices. The DSI software program receives and processes commands the DMS–100 normally sends to the MTD. This software also responds with the status and strobe signals the MTDs normally return to the DMS–100. Furthermore, these packs handle the call record data from the DMS–100.

Primary function

The DSI circuit packs' main function is to receive call record AMA data blocks from the DMS–100, to process those records (where required), and to make this data available for transfer to the correct buffer in the main CPU.

Output signals from the DMS–100 MTD ports come through the interface box ribbon cables and adapters and arrive at the DSI circuit packs' input ports.

Cable adapter assemblies

The MTD data path from the DMS–100 to DPP is through DSI cable adapter assemblies in interface boxes installed near the DPP. These assemblies duplicate the connections for the cables that normally interface the DMS–100 to the MTDs. The DMS–100 MTD ports plug into an interface box that provides connectors for the control and status, read, and write leads from the DMS–100. System signals are passed through the interface boxes to J connectors on the DPP. From the J connectors, the signals are routed internally to the DPP DSI circuit packs.

See Table 10–1 for option settings on this circuit pack. Figure 10–1 shows the jumper locations and circuit packs' layout.

Procedure 10–1
Replacing DSI circuit packs (A12,A13,B12,B13)

CAUTION
Since all DPP circuit packs are static sensitive, be careful handling them.

Wear a wrist grounding strap when working with the DPP. There are jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) to accept the banana plug connection on the end of a grounding strap.[1]

Step	Description	Notes
1	Get the replacement circuit pack from the spares kit.	
2	Remove the protective electrostatic bag and place it on a suitable, grounded surface.	
3	Make sure the replacement circuit pack matches the faulty circuit pack's part number and has the correct revision level. Also, make sure the suspected faulty DSI is in the standby processor.	Verify that any applicable firmware for the circuit packs is correct.
4	Remove power from the standby DPP chassis by operation of the +8 V dc rocker switch on the power supply.	A or B, the one with the suspected fault.
5	Remove the suspected circuit pack.	Put it in the empty electrostatic bag.
6	Check the revision level and option settings for the spare circuit pack. Ensure that the options on the spare circuit pack match the options on the removed circuit pack.	Refer to Figures 10–1 and 10–2 and Tables 10–1, 10–2, 10–3, and 10–4 for the correct option setting.
7	Insert the spare circuit pack in the vacated card slot, making sure it is fully seated.	

(continued)

Procedure 10–1
Replacing DSI circuit packs (A12,A13,B12,B13) (continued)

Step	Description	Notes
8	Apply power to the DPP chassis by resetting the rocker switch in step 4 above.	Wait for start–up activity to end and the message, "Software Loaded" to print.
9	At the maintenance terminal, enter: **>TEST STDBY 00 (cr)**	TEST forces diagnostics which confirm if the faults were corrected.
10	Place the active processor unit in PRIME mode. At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor. b. Make the O/P Mode Select Switch P. c. Turn the Mode Switch to the right.	 Make the active processor the PRIME processor. Turn it 45 degrees to the right and release.
11	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	

Note: Make sure any circuit pack option settings are correct before replacing any cards. Incorrect settings can cause improper performance and produce faultlike symptoms in the DPP.

End

Table 10–1
Data stream interface (DSI) circuit packs (A12 and B12) options – part number: NT6M70AA and NT6M70CF

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Strap	None used			
DIP Switch (S1)			@S1 1 = On 6 = On 8 = On 10 = On 2 = Off 3 = Off 4 = Off 5 = Off 7 = Off 9 = Off	Must be the same as the factory setting.
DIP Switch (S2)			@S2 1 = On 4 = On 2 = Off 3 = Off	Must be the same as the factory setting.
Rotary Switch	None used			
Switch	None used			
Jumper	None used			

Figure 10–1
Data stream interface (A12, B12, A13, and B13) circuit packs (NT6M70AA and NT6M70CF) options

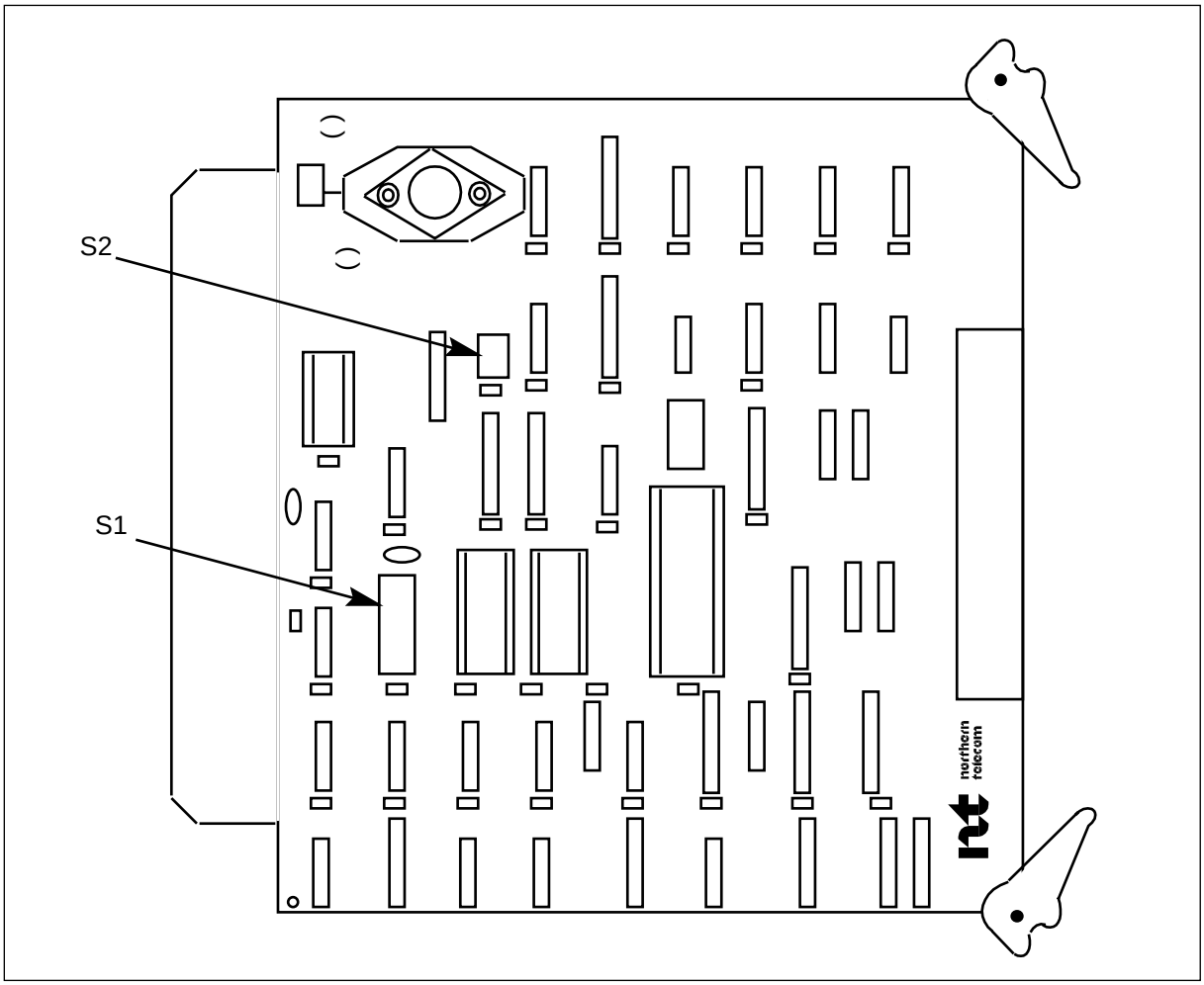


Table 10–2
Data stream interface (DSI) circuit packs (A12 and B12) options – part number: NT6M70AC

Device type (number)	Position/setting	Function	Setting: Factory	Setting: On–site
U42 EPROM SIZE	2764	Straps: B, D	In (Typical)	Note:
	2732A	Straps: F	In	PIN 1 is
	27128	Straps: B, E, D	In	shown as
	27256	Straps: B, E, C	In	white dot
	27512	Straps: A, E, C	In	on PCB.
				1=A,D,G
U41 RAM SIZE[2]		SW1 position: 8	On (Typical)	
	8K x 8	9	Off	
		SW1 position: 9	On (Alternate RAM)	
	32K x 8	8	Off	
U52 RAM SIZE[2]	8K x 8	Straps: G	In (Typical)	
	32K x 8	Straps: H	In	
DIP Switch (S1)	(X = On) 1 2 3 4 5 6 7 8 9	Select:	@S1	Must be the same as
	1 and 2 Off	DSI1	2 = On	the factory
	X	DSI2	3 = On	setting.
	X	DSI3	7 = On	
	X X	DSI4	8 = On	
	X	32K x 8 RAM1 U41[3]	1 = Off	
	X	8K x 8 RAM1 U41[3]	4 = Off	
	X	12.5 ips	5 = Off	
	X	25/37.5 ips	6 = Off	
	X	45 ips		
	X	0.4 to 0.8 MS	9 = Off	
	X	0.6 to 1.6 MS		
		ms = microsecond		
DIP Switch (S2)			@S2	
			1 = On	Must be the
			4 = On	same as the factory
			2 = Off	setting.
			3 = Off	
Rotary Switch	None used			

Table 10–2
Data stream interface (DSI) circuit packs (A12 and B12) options – part number: NT6M70AC

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	All out			
Switch	None used			

Notes:
Note 1: There are no customer–definable options on this circuit packs. Information is for reference only. Use this data for verification during initial DPP system installation and/or circuit packs replacement to make sure the replacement circuit packs are set up the same as the circuit packs being replaced.
Note 2: U52 is typically not equipped. Strapping is shown for reference only. Factory settings for staps S1–8 and S1–9 is subject to change based on availability of EPROM and RAM. Check the manufacturer's identification of U52, U41, and U42 to verify these settings. See the following chart for factory option settings for U41, U42, and U52.

End

Figure 10–2
Data stream interface (A12, B12, A13, and B13) circuit packs (NT6M70AC) options

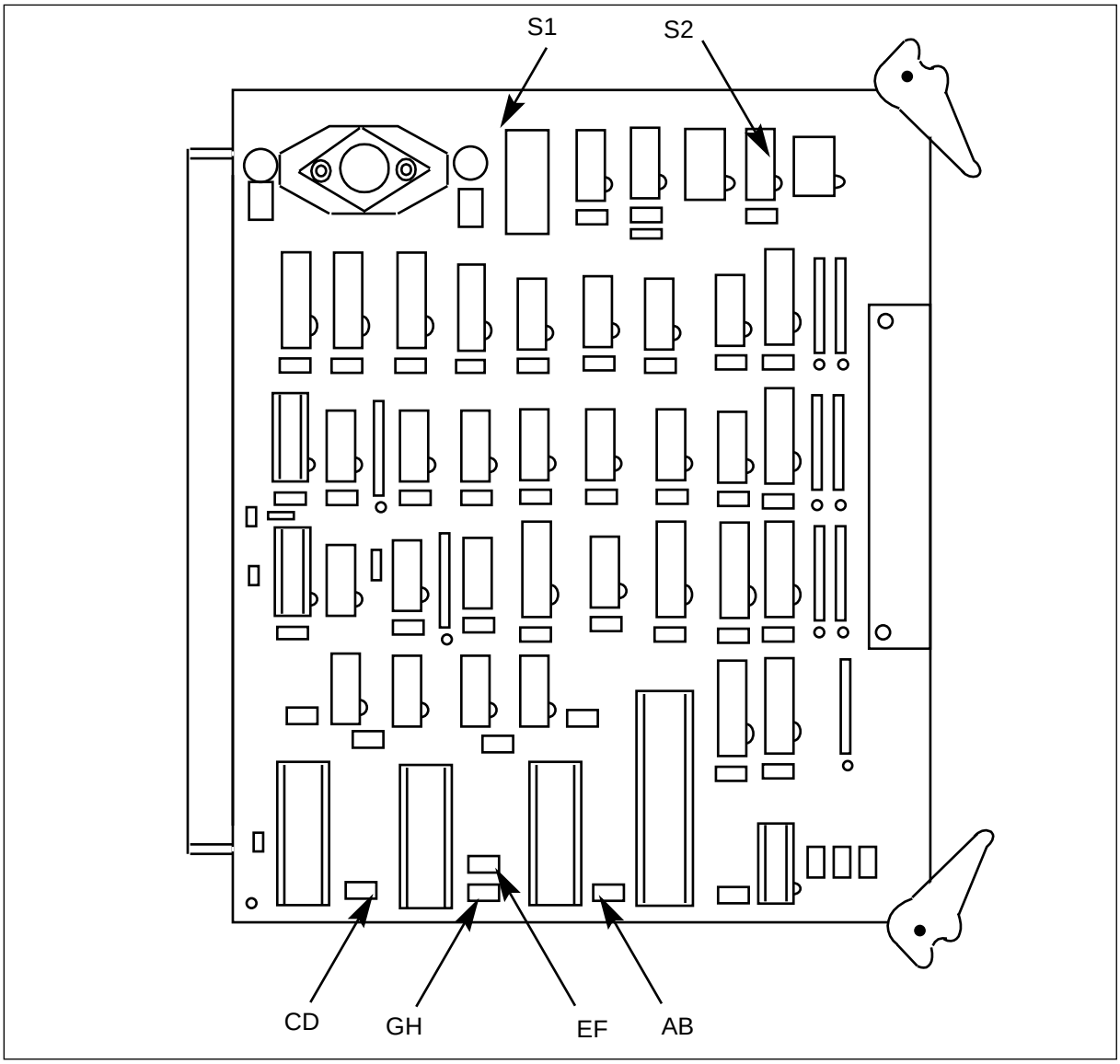


Table 10–3
Data stream interface (DSI) circuit packs (A13 and B13) options – part number: NT6M70AA and NT6M70CF

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Strap	None used			
DIP Switch (S1)			@S1 6 = On 8 = On 10 = On 1 = Off 2 = Off 3 = Off 4 = Off 5 = Off 7 = Off 9 = Off	Must be the same as the factory setting.
DIP Switch (S2)			@S2 1 = On 4 = On 2 = Off 3 = Off	
Rotary Switch	None used			
Switch	None used			
Jumper	None used			

Notes:
Note: See Figure 10–1.
Note: There are no customer–definable options on this circuit packs. Information is shown for reference purposes only. This data is to be used for verification during initial DPP system installation and/or circuit packs replacement to make certain that the replacement circuit packs is set–up the same as the circuit packs being replaced.

Table 10–4
Data stream interface (DSI) circuit packs (A13 and B13) options – part number: NT6M70AC

Device type (number)	Position/setting	Function	Setting: Factory	Setting: On–site
Strap	x = strap to center post A B C D E F G H X X X X X X X X X X X X X X	U42 and U41 Chip type; strap to use with: 2732A U42 2764 U42 27128 U42 27256 U42 27512 U42 8K x 8 RAM2 U52[3] 32K x 8 RAM2 U52[3]	 B, D G	 Must be the same as the factory setting.
U42 EPROM SIZE	2764 2732A 27128 27256 27512	Straps: B, D Straps: F Straps: B, E, D Straps: B, E, C Straps: A, E, C	In (Typical) In In In In	Note: PIN 1 is shown as white dot on PCB. 1=A,D,G
U41 RAM SIZE[2]	8K x 8 32K x 8	SW1 position: 8 9 SW1 position: 9 8	On (Typical) Off On (Alternate RAM) Off	
U52 RAM SIZE[2]	8K x 8 32K x 8	Straps: G Straps: H	In (Typical) In	
DIP Switch (S1)	(X = On) 1 2 3 4 5 6 7 8 9 1 and 2 Off X X X X X X X X X	Select: DSI1 DSI2 DSI3 DSI4 32K x 8 RAM1 U41[3] 8K x 8 RAM1 U41[3] 12.5 ips 25/37.5 ips 45 ips 0.4 to 0.8 MS 0.8 to 1.6 MS ms = microsecond	@S1 3 = On 7 = On 8 = On 1 = Off 2 = Off 4 = Off 5 = Off 6 = Off 9 = Off	Must be the same as the factory setting.

—continued—

Table 10–4
Data stream interface (DSI) circuit packs (A13 and B13) options – part number: NT6M70AC

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
DIP Switch (S2)	(X = On)		@S2 1 = On 4 = On 2 = Off 3 = Off	Must be the same as the factory setting.
Rotary Switch	None used			
Switch	None used			
Jumper	All out			

Notes:
Note 1: There are no customer–definable options on this circuit packs. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit packs replacement to make sure the replacement circuit packs are set up the same as the circuit packs being replaced.
Note 2: U52 is typically not equipped. Strapping is shown for reference only. Factory settings for straps S1–8 and S1–9 subject to change based on availability of EPROM and RAM. Check the manufacturer's identification of U52, U41, and U42 to verify these settings.

End

Bus terminator circuit pack

General description

The bus terminator circuit pack, in slot 14 of the A and B chassis, contains a power regulator. This regulator provides circuitry to terminate the end of the bus which prevents ringing (oscillation) of signals on the bus.

See Table 11–1 for the option settings on this circuit pack. Figure 11–1 shows the circuit pack layout.

Replacing Bus terminator circuit pack

First identify the failing circuit pack to determine which processor (A or B) is off–line. See the following procedure for replacing this pack.

Procedure 11–1
Replacing bus terminator circuit pack – model numbers G12 or earlier (D09 or E12 for example)

Step	Description	Notes
1	First get the DPP's model number from the DPP nameplate, A chassis, rear panel.	**WARNING:** Perform during low traffic.
2	Remove the front cover of the DPP chassis.	
3	Set the status of the active processor to ONLY.	Press the O/P Mode Switch to the ONLY position for the active processor.
4	Press the processor A/B Select Switch to the position (A or B) that matches the active processor.	
5	Turn the Mode Switch.	Turn to the right and release.
6	Make sure the active processor unit ONLY status lamp lights.	
7	Power down the standby chassis.	
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them. [1]	
8	Remove the cables from the front of the circuit packs at positions 12 and 13.	Cable on left goes to position A12; cable on right goes to position A13**.**
9	Remove the DSI circuit packs (slots 12 & 13) and the Disk Interface circuit pack (slot 11).	This is to make room. Identify the DSI circuit packs to know which slot to return them.
10	Remove the two screws from the ribbon cable shield.	Remove and save the screws and shield.
11	Hold the cables out of the way. Remove the suspected bus terminator circuit pack by inserting a finger in the hole in the circuit pack.	Apply firm, even pressure to remove the circuit pack.

(continued)

Procedure 11–1
Replacing bus terminator circuit pack – model numbers G12 or earlier (D09 or E12 for example)

Step	Description	Notes
12	Insert the replacement bus terminator circuit pack.	This pack requires high insertion force for proper seating. Use a thimble or other mechanical aid.
13	Fold the DSI cables back into position along the outer wall of the chassis.	
14	Remount the ribbon cable shield over the DSI cables.	If it does not fit properly, check the folding of the DSI cables. Do not crimp these cables.
15	Insert the two screws to hold the cable shield in place.	Do not overtighten.
16	Reinsert the DSI circuit packs in slots 12 and 13 and the Disk Interface circuit pack in slot 11.	Return the DSI circuit packs to the appropriate locations.
17	Reattach the DSI cables.	
18	Apply power to the chassis.	
20	Wait for startup activity to end and the message "S/W loaded." Set the DPP ONLY processor to PRIME mode.	Set the O/P selector switch to P. Turn the mode insert key 45^{o} to the right and release.
20	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	
21	Reinstall the front panel on the DPP.	
	End	

Procedure 11–2
Replacing bus terminator circuit pack – models H01 and later
(H02 or I01, for example),

Step	Description	Notes
1	First get the DPP's model number from the DPP nameplate, A chassis, rear panel. Two people must reinstall the ribbon cable shield with a 2–1/2–inch No. 2 flat–blade screwdriver.	**WARNING:** Perform during low traffic.
2	Remove the front cover of the DPP chassis.	
3	Set the status of the active processor to ONLY.	Press the O/P Mode Switch to the ONLY position for the active processor.
4	Press the processor A/B Select Switch to the position (A or B) that matches the active processor.	
5	Turn the Mode Switch.	Turn to the right and release.
6	Make sure the active processor unit ONLY status lamp lights.	
7	Power down the standby chassis.	
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them. [1]	
8	Remove the cables from the front of the circuit packs at positions 12 and 13.	Cable on left goes to position A12; cable on right goes to position A13**.**
9	Remove the DSI circuit packs (slots 12 & 13) and the Disk Interface circuit pack (slot 11).	This is to make room. Identify the DSI circuit packs to know which slot to return them.

(continued)

Procedure 11–2
Replacing bus terminator circuit pack – models H01 and later
(H02 or I01, for example), (continued)

Step	Description	Notes
10	From the rear of the IOE frame, insert a sheet of cardboard (approximately 12" x 12" x 1/16") under the left side of the DPP.	The cardboard prevents losing the screws to be removed.
11	From the rear of the IOE frame, use a 2–1/2–inch No. 2 flat–blade screw–driver to remove the two screws holding the ribbon cable shield.	The screws are approximately 2–inches to the rear of the DPP mounting bracket. If the DPP shipping bracket is still attached, remove it for access to the ribbon cable shield screws. Do not reinstall the shipping bracket or its screws. Store them with the other DPP shipping items.
12	Hold the cables out of the way. Remove the suspected bus terminator circuit pack by inserting a finger in the hole provided in the circuit pack.	Apply firm, even pressure to remove the circuit pack.
13	Insert the replacement bus terminator circuit pack.	Use high insertion force for proper seating. Use a thimble or other mechanical aid for proper seating.
14	Fold the DSI cables back into position along the outer wall of the chassis.	
15	Remount the ribbon cable shield over the DSI cables.	If it does not fit properly, check the folding of the DSI cables. Do not crimp the cables.
16	Insert the two screws to hold the cable shield in place. Remove the cardboard sheet after this step.	This requires one person at the rear of the IOE frame . Do not overtighten. Another person at the front of the IOE frame should hold the ribbon cable shield in place.
17	Reinsert the DSI circuit packs in slots 12 and 13 and the Disk Interface circuit pack in slot 11.	Return the DSI circuit packs to the appropriate locations.

(continued)

Procedure 11–2
Replacing bus terminator circuit pack – models H01 and later
(H02 or I01, for example),

Step	Description	Notes
18	Reattach the DSI cables.	
19	Apply power to the chassis.	
20	Wait for start–up activity to end and the message "S/W loaded." Set the DPP ONLY processor to PRIME mode.	Set the O/P selector switch to P. Turn the mode insert key 45^{o} to the right and release.
21	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	
22	Reinstall the front chassis on the DPP.	
	End	

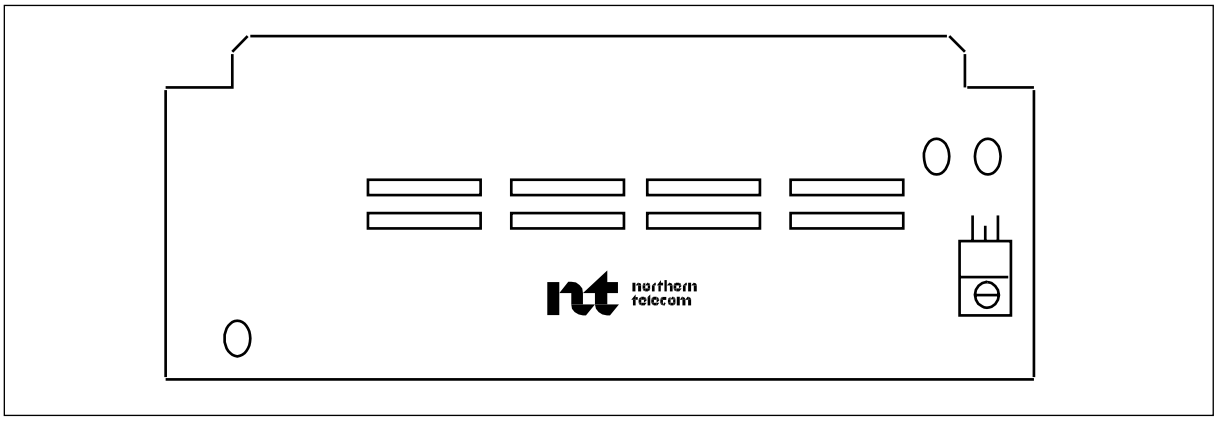
Table 11–1
Bus terminator circuit pack (A14 and B14) options – part number: NT6M68AA

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	None used			
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Note 1: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make certain that the replacement circuit pack is set–up the same as the circuit pack being replaced.

End

Figure 11–1
Bus terminator (A14 and B14) circuit pack (NT6M68AA) options



Power and alarm communications circuit pack

The Power and alarm communications (P/A Comm) circuit pack, located at the rear of the A chassis in position 16, performs a multipurpose function. It provides communications between the Quad SIO circuit pack and various peripherals. Its circuitry responds to switching signals from the error control II circuit pack or keyboard–entered commands. Furthermore, it provides power detection, alarm generation, and ac clock circuitry.

The P/A Comm circuitry detects the loss of output voltages from the DPP power supplies. Six optoisolators are connected in a series string, insuring that any voltage loss interrupts the string and deenergizes the power alarm relay (K7). This causes a form C relay to change state, signalling an alarm condition.

This circuitry also provides operating power for the circuit pack. The +12 V dc, –12 V dc, +8 V dc, and +5 V dc supplies are all monitored and connected to guarantee power to the circuit pack as long as at least DPP power supply is operational. The +8 V dc passes through a regulator to provide +5 V dc power for the logic circuits.

The P/A Comm circuitry also generates external alarms using signals from the error control II circuit pack. Three relays on this pack signal alarm conditions to devices outside the DPP. The circuits which drive these relays are also on the circuit pack. The three relays follow:

- K1 – Minor Alarm
- K2 – Major Alarm
- K3 – Critical Alarm

The ac clock circuit generates timing pulses from a 19 V ac, 60 Hz external source, if equipped. Two such circuits can be provided, one for each DPP chassis. In the circuit, a 60 Hz input is fed to an ac optocoupler to prevent ground noise. The optocoupler produces a 120 Hz signal, divided by two to produce a 60 Hz signal. This signal drives a transistor, providing extra drive capability for sending to the CTC on the CPU circuit pack.

The P/A Comm pack contains up to eight serial channels; only four are used. These four are configured as a 1–input, 1–output switch. The input is connected to the Quad SIO circuit packs in the DPP card racks. The input interface consists of eight signal lines (plus ground) for each channel. These lines are connected to a tristatable octal buffer integrated circuit. The –ASEL signal from the Error Control II circuit pack determines the input–to–output connection.

The P/A Comm circuit pack may use either internal or external transmit clocks for all eight channels. Select the clock source by switches S1 and S2, located as shown in Figure 12–2. Externally transmitted clock signals from the eight outputs are connected to clock lines on the Quad SIO circuit pack. See Table 12–1, Table 12–2, and Table 12–3.

Replacing P/A COMM circuit pack

Use the following procedure to replace the P/A Comm circuit pack.

Procedure 12–1
Replacing the P/A Comm circuit pack

Step	Description	Notes
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them. Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of a grounding strap.	
	 **WARNING** Since the DPP is powered up during this procedure, observe all safety procedures for operations on live equipment.[1]	
1	Wait for a low traffic period, if possible.	Make sure no polling is occurring.
2	Notify technical assistance personnel of the temporary loss of MMI and polling links.	Polling link for DPP systems without 56K polling is routed through the P/A Comm circuit pack. DPP systems with 56K polling use a path through the 56K Xovr to the 56K Connector circuit pack.
3	Remove the slotted screws that fasten the outer edges of the rear panel assembly to the cabinet.	
4	Remove the rear panel of the A chassis.	
5	Pull the rear panel away from the cabinet. Remove the front panel of the A chassis to improve cooling, if necessary.	Put the two panels in a safe place to prevent bending and scratching.

(continued)

Procedure 12–1
Replacing the P/A Comm circuit pack

Step	Description	Notes
6	Remove the cable (P11) connected to the P/A Comm circuit pack.[2, 3] Remove the other cables.	CO alarms activate due to loss of MMI links. Other alarms may also activate and the DPP will change to an "Only" processor mode. This is normal. Silence the alarm at the DMS–100 and go to step 7.
7	Remove the screws that fasten the P/A Comm circuit pack.	Gently remove the circuit pack from its mounting position.
8	Mount the replacement assembly in the vacated position.	
9	Reattach any cables removed in step 6 in reverse order.	Office alarms cease as the MMI links reactivate.
10	Properly reroute all cables.	Make sure all wires and cables are routed so they are not pinched or in contact with the arc of the fan blades.
11	At the maintenance terminal, enter: **>RSERR ACT 00 (cr)**	To clear any alarms on the active processor. Alarms will clear if there are no fault conditions.
12	At the maintenance terminal, enter: **>RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor. Alarms will clear if there are no fault conditions.
13	At the Switch and Status Panel:	If all alarms clear, place the active processor unit in PRIME mode.
	a. Press the A/B Select Switch to match the active processor.	
	b. Make the O/P Mode Switch Prime.	Make the active processor the PRIME processor.

(continued)

Procedure 12–1
Replacing the P/A Comm circuit pack

Step	Description	Notes
	c. Turn the Mode Switch to the right.	Turn it 45 degrees to the right and release.
14	If alarm status shows active alarms, resolve all alarm conditions.	
15	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)**	
16	Test the peripheral port to see if it is still failing.	
17	Seat the rear panel in its fully seated position and reinstall the slotted pan head screws previously removed.[4]	From step 3.
18	Reattach the front panel of the chassis.	If removed.

Notes:
Note 1: Make sure any circuit pack option settings are correct before replacement. Improper performance can be caused by incorrect settings, and produce faultlike symptoms in the DPP.
Note 2: Verify the cable markings (identification) or attach labels to the cables when removing them to facilitate replacement in the correct positions.
Note 3: Make sure the jumpers/straps are set the same as the ones on the circuit pack to be replaced.
Note 4: When replacing the screws, align carefully before tightening to avoid stripping. Tighten the screws, alternating until all are equally tight. Do not "cinch down" any one screw until all are properly aligned; no binding or force needed to turn.

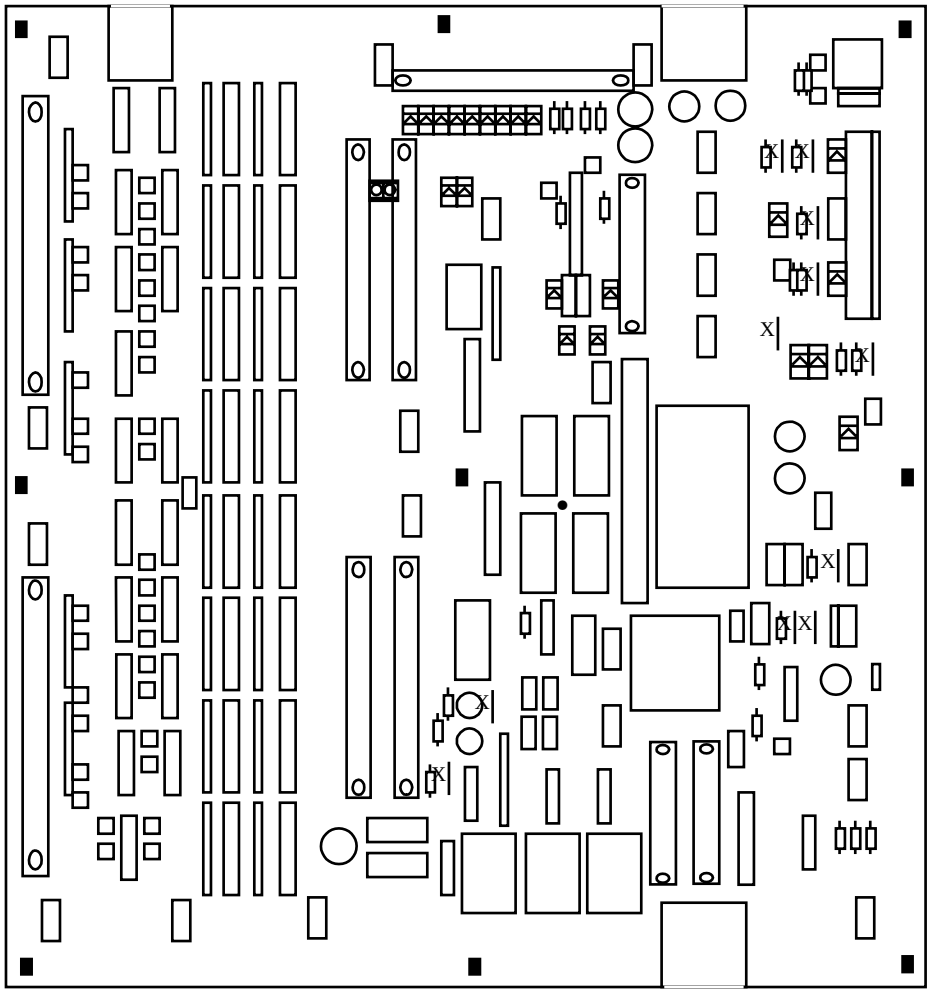
End

Table 12–1
P/A Comm circuit pack (A16) options – part number: NT6M84AA (release 01–06)

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	None used			
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Notes:
Note 1: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.
Note 2: This circuit pack does not support polling on digital data lines; use for an analog network only.

Figure 12–1
P/A Comm circuit pack (A16) – part number: (NT6M84AA; release 01–06) options



Notes:
1. This circuit pack does not support polling on digital data lines; use for an analog network only.
2. There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

Table 12–2
Power and alarm communications circuit pack (A16) options – part number: NT6M84AA (release 07)

Device type (number)	Position/setting		Function	Setting	
				Factory	On–site
Jumper (J14)	1–2	ASEL Control	Crossover Control Select – Control the leads from the Error Control II circuit pack to determine which CPU has control of the Crossover circuitry.	1–2	Must be the same as the factory setting.
	2–3	CPUSEL Control			
Jumper (J15)	1–2	Rover terminal jack enabled.	Rover terminal select control.	1–2	Must be the same as the factory setting.
	2–3	Rover terminal jack disabled.			
Jumper (J16)	1–2	channel 4 on the Quad SIO controlled by the Quad SIO and the setting of J14.	Channel 4 control select – Four position switch, S6, of the Quad SIO; controls the use of the manual transfer switches for the maintenance terminal. (Under control of software only.)	2–3	Must be the same as the factory setting.
	2–3	channel 4 on the Quad SIO controlled by the setting of J14 only.			
Jumper (J17)	1–2	channel 4 on the Quad SIO controlled by the Quad SIO and the setting of J14.	Channel 4 control select – Four position switch, S6, of the Quad SIO; controls the use of the manual transfer switches for the maintenance terminal. (Under control of software only.)	2–3	Must be the same as the factory setting.
	2–3	channel 4 on the Quad SIO controlled by the setting of J14 only.			
Strap	None used				

(continued)

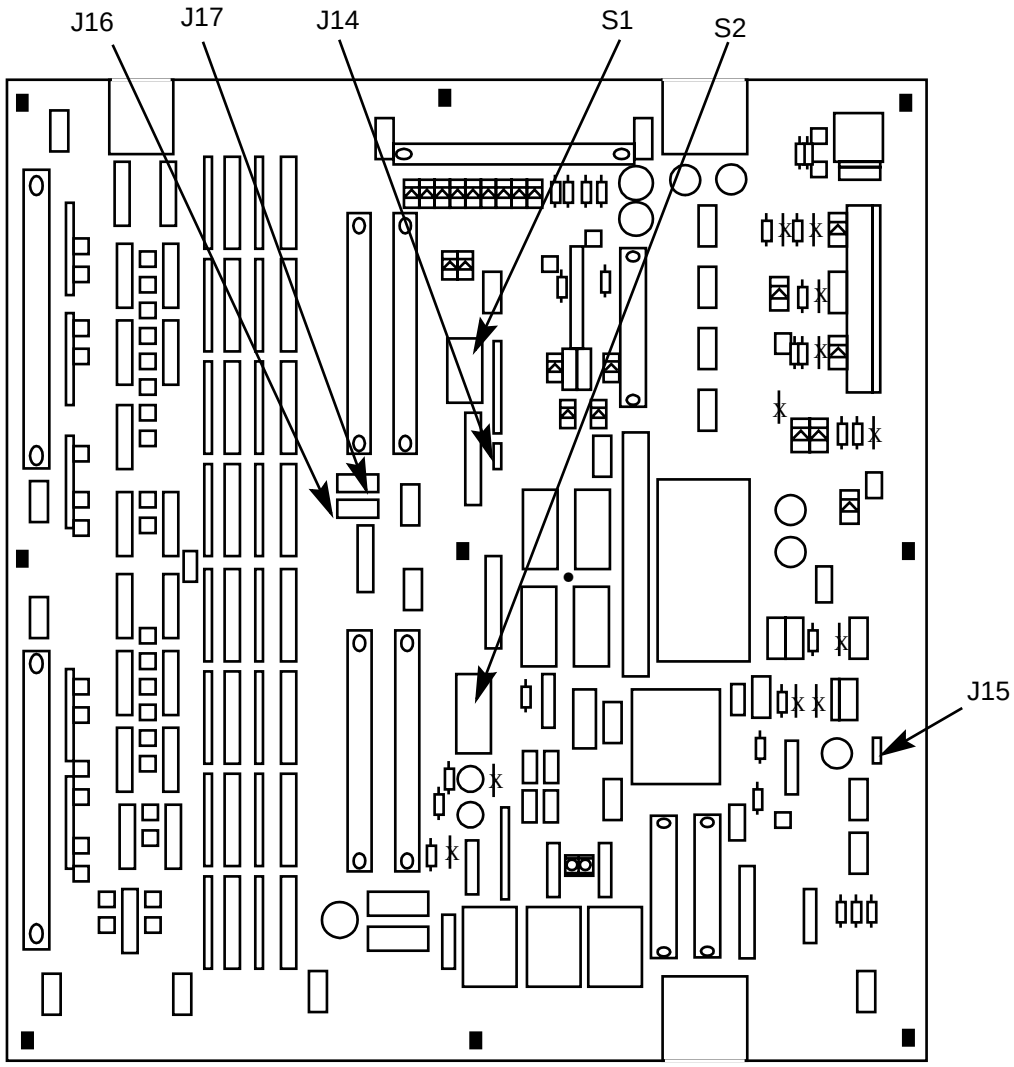
Table 12–2
Power and alarm communications circuit pack (A16) options – part number: NT6M84AA (release 07) (continued)

Device type (number)	Position/setting			Function	Setting	
					Factory	On–site
DIP Switch (S1)[4]	Chan. No.	Int/ Ext	SW1–SW2 Setting			
	1	Int	SW1–1, 5 Off	With SW2, transmit clock selection, (internal or external)	Off	
		Ext	SW1–1, 5 On			
	2	Int	SW1–2, 6 Off		Off	
		Ext	SW1–2, 6 On	With SW1, transmit clock selection,		
	3	Int	SW1–3, 7 Off	(internal or external)	Off	
		Ext	SW1–3, 7 On			
	4	Int	SW1–4, 8 Off		Off	
		Ext	SW1–4, 8 On	(Internal clock is from the Quad SIO in slot A1AxA6.)		
Rotary Switch	None used					
Switch	None used					

Notes:
Note 1: See Figure 12–1.
Note 2: This circuit pack does not support polling on digital data lines; use for an analog network only.
Note 3: Do not set these switches (S–1 and S–2) to the On position; doing so disables the communication path through the associated channel.
Note 4: S1 and S2 settings are customer–definable based on whether communications are over digital or analog lines. See the following chart for digital guidelines. Use these guidelines for to determine the site settings for SW1 and SW2.
a. If channel A, J1 (BX.25 Polling for BCS25–35 DPP systems w/o 56K polling) is done over a digital line:
SW1 positions 1 and 5 ON
all others Off

End

Figure 12–2
Power and alarm communications (A16) circuit pack (NT6M84AA; release 07 and NT6M84BA) options



Notes: 1. The NT6M84AA, release 07, does not support polling on digital data lines; use for an analog network only.

2. The NT6M84BA supports polling on digital data lines and analog networks.

Table 12–3
Power and alarm communications circuit pack (A16) options – part number: NT6M84BA

Device type (number)	Position/setting		Function	Setting	
				Factory	On–site
Jumper (J14)	1–2	ASEL Control	Crossover Control Select – Control the leads from the Error Control II circuit pack to determine which CPU has control of the Crossover circuitry.	1–2	Must be the same as the factory setting.
	2–3	CPUSEL Control			
Jumper (J15)	1–2	Rover terminal jack enabled.	Rover terminal select control.	1–2	Must be the same as the factory setting.
	2–3	Rover terminal jack disabled.			
Jumper (J16)	1–2	channel 4 on the Quad SIO controlled by the Quad SIO and the setting of J14.	Channel 4 control select – Four position switch, S6, of the Quad SIO; controls the use of the manual transfer switches for the maintenance terminal. (Under control of software only.)	2–3	Must be the same as the factory setting.
	2–3	channel 4 on the Quad SIO controlled by the setting of J14 only.			
Jumper (J17)	1–2	channel 4 on the Quad SIO controlled by the Quad SIO and the setting of J14.	Channel 4 control select – Four position switch, S6, of the Quad SIO; controls the use of the manual transfer switches for the maintenance terminal. (Under control of software only.)	2–3	Must be the same as the factory setting.
	2–3	channel 4 on the Quad SIO controlled by the setting of J14 only.			
Strap	None used				

(continued)

Table 12–3
Power and alarm communications circuit pack (A16) options – part number: NT6M84BA
(continued)

Device type (number)	Position/setting			Function	Setting	
					Factory	On–site
DIP Switch (S1)[4]	Chan. No.	Int/ Ext	S1–S2 Setting			
	1	Int	S1–1, 5 Off	With S2, transmit clock selection, (internal or external)	Off	
		Ext	S1–1, 5 On			
	2	Int	S1–2, 6 Off		Off	
		Ext	S1–2, 6 On	With S1, transmit clock selection, (internal or external)		
	3	Int	S1–3, 7 Off		Off	
		Ext	S1–3, 7 On			
	4	Int	S1–4, 8 Off	(Internal clock is from the Quad SIO in slot A1AxA6.)	Off	
		Ext	S1–4, 8 On			
DIP Switch (S2)[4]	Chan. No.	Int/ Ext	S1–S2 Setting			
	5	Int	S2–1, 5 Off	(External clock is derived by looping around the TCIn signals.)	Off	
		Ext	S2–1, 5 On			
	6	Int	S2–2, 6 Off		Off	
		Ext	S2–2, 6 On			
	7	Int	S2–3, 7 Off		Off	
		Ext	S2–3, 7 On			
	8	Int	S2–4, 8 Off		Off	
		Ext	S2–4, 8 On			
Rotary Switch	None used					
Switch	None used					

Notes:
Note 1: See Figure 12–1.
Note 2: This circuit pack supports polling on digital data lines or on an analog network. For use with digital lines check that:
a. DPP systems is BCS25–35
b. Quad SIO circuit pack at A6 and B6 is part number NT6M60BA
c. Four Channel Comm circuit pack at A17 is release 03, or later
d. Collector supports the digital data line feature.
Note 3: Factory settings shown are for an analog network only.
Note 4: S1 and S2 settings are customer–definable based on whether communications use analog or digital data lines. See the following chart for the digital application to determine the on–site settings for SW1 and SW2:
a. If channel A, J1 (BX.25 Polling for BCS25–35 DPP systems w/o 56K polling) is done over a digital data line:
SW1 positions 1 and 5 On
All other Off
Note 5: Make sure the settings for internal and external transmit receive clocks agree with the settings on the QSIO circuit packs in A6 and B6 before working with digital data lines.

End

Disk Crossover and Controller circuit packs

General description

These circuit packs provide the data and control paths between the Disk Interface circuit pack in the card rack and the disk drives: 72 – 380 Mbyte w/o 56K or compression polling. For 380 Mbyte, 760 Mbyte, or 1.7 Gbyte disk drives w/56Kpolling or compression polling, see Section 14: SCSI Crossover pack.

The Disk Crossover (Xovr) circuit pack is on the inside of the hinged panel, A15 and B15, at the rear of each DPP chassis. This pack provides a crossover data path between the processors and the disk. The program in the active processing unit controls this pack which simultaneously routes data from the active Disk Interface circuit pack to both disk drives.

For 380– and 760–Mbyte disk drives, the Disk Controller circuit pack is inside the disk drive. For the 72– and 140–Mbyte drives, the Disk Controller circuit pack is on the top of the disk assembly. This circuit pack is in the data path between the Disk Xovr circuit pack and the disk drive. The Disk Controller circuit pack is a smart circuit assembly, containing a processor, RAM, EPROM, and additional control circuitry. Control signals (status commands, write signals, and read signals) are passed through this pack, which initiates the appropriate operation in the disk drive.

See Table 13–1 for the jumper option setting on the Disk II Crossover circuit pack. Figure 13–1 shows the jumper location and circuit pack layout. The Disk Controller options are described in Table 13–2.

Replacing Disk Controller circuit pack

Use the following procedure when replacing the Disk Crossover circuit pack.

Procedure 13–1
Replacing Disk XOVR circuit pack

Step	Description	Notes
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them. Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of a grounding strap.	
	 **WARNING** Since the DPP is powered up during this procedure, observe all safety procedures for operations on live equipment.[1]	
1	Wait for a low traffic period, if possible.	Make sure no polling is taking place.

2	Locate the failing Disk XOVR circuit pack and change the disk mode to the other disk ONLY mode, if necessary.
	
	Enter: (at the terminal)
	
	>DISK MODE xx (cr)
	
	where:
	xx = disk mode = AO = A ONLY
	= BO = B ONLY
		The other disk is the one not in the same chassis as the suspected Disk XOVR circuit pack.
		
		Proper response =
		
		`DISK MODE: AO`
		or
		`DISK MODE: BO`

3	Loosen the slotted screws which fasten the outer edges of the rear panel assembly to the cabinet.	
4	Remove the appropriate rear panel.	Wait for the disk mode change to complete.

(continued)

Procedure 13–1
Replacing Disk XOVR circuit pack

Step	Description	Notes
5	Pull the rear panel away from the cabinet. Remove the front panel of the chassis to improve cooling, if necessary.	Put the two panels in a safe place to prevent bending and scratching.
6	Loosen the 2 screws at the top of the hinged card panel and the screw at the bottom of the hinged card panel.[2]	Let it swing slowly down from the top until it rests.
7	First remove power cable (J4), then any cables and screws connected to the suspected circuit pack.[3,4]	Gently pull the suspect assembly loose from its mounting position.

8	Mount the replacement assembly in the vacated position and reconnect any cables removed in step 7 in reverse order. Verify the repair by switching disk modes back to PRIME.[5]
	
	Enter: (at the terminal)
	
	>DISK MODE xx (cr)
	
	where:
	xx = disk mode = AP = A PRIME
	= BP = B PRIME
	
	Proper response =
	
	`DISK MODE: AP`
	`or`
	`DISK MODE: BP`
		If the replacement XOVR circuit pack solves the problem, the DPP will begin a disk copy that may take several hours, depending on how much data and how large the disks are.
		
		(from disk mode AO)
		(from disk mode BO)

9	Lift the hinged circuit assembly gate back to its vertical position and tighten the (3) screws loosened in step 4.[6]	Remove the insulating material, if used.
10	Route all wires and cables to avoid pinching or crimping when the rear panel is reinstalled.	

(continued)

Procedure 13–1
Replacing Disk XOVR circuit pack

Step	Description	Notes
11	Seat the rear panel. Reinstall the slotted pan head screws previously removed.	From step 1. See the note about screw tightening.
12	Enter: (at the terminal) **>TEST ACT (cr)** Proper response = `DISK TEST PASSED`	This is one message that may appear; see Table 13–1 for further information. For any other response, see the procedure sheet for that message and perform activities listed there.
13	Reattach the front panel of the chassis, if removed.	Replace rear panels for proper convection cooling.

Notes:
Note 1: Make sure any circuit pack option settings are correct before replacement. Improper performance can be caused by incorrect settings, and produce faultlike symptoms in the DPP.
Note 2: If the circuit pack at A15 is being replaced, use a Styrofoam block or another insulating material, about 1" x 1" x .5", to insulate the pins of the 16–pin cable on the P/A Comm circuit pack to prevent accidental shorting against the chassis.
Note 3: Verify the cable markings (identification) or attach labels to the cables when removing to facilitate replacement in the correct positions.
Note 4: If the circuit pack has option jumpers or straps that must be set before installation, make sure the jumpers/straps are set exactly the same as the ones on the circuit pack to be replaced.
Note 5: Make sure the cable(s) are connected properly (pin 1 in the correct position) to prevent data loss.
Note 6: When replacing the screws, align carefully before tightening to avoid stripping. Tighten the screws, alternating until all are equally tight. Do not "cinch down" any one screw until all are properly aligned; no binding or force needed to turn.

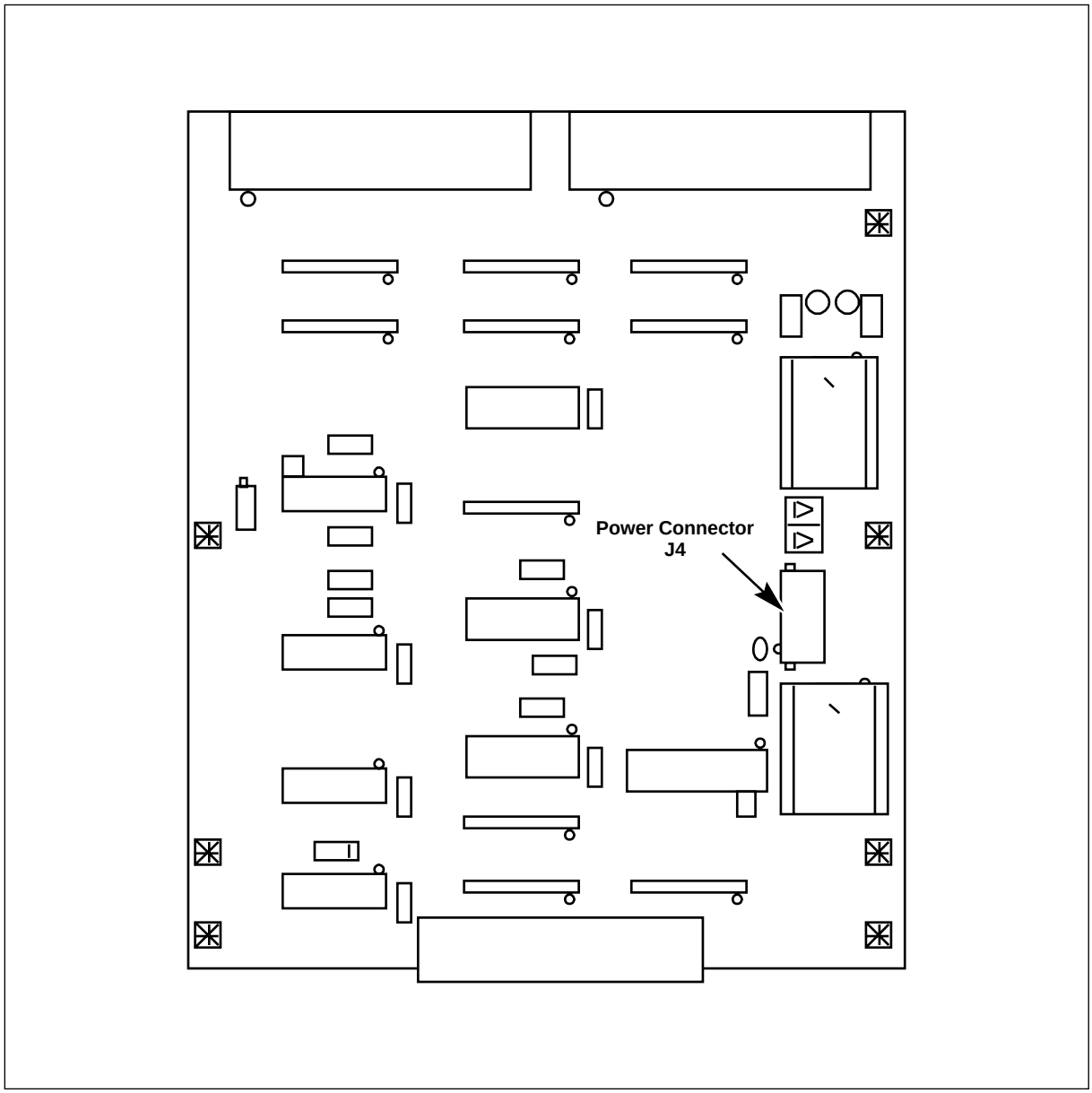
End

Table 13–1
Disk II crossover circuit pack (A15 and B15) options – part number: NT6M72AC, (72–Mbyte and 140–Mbyte disk drives); NT6M72AD, (72–Mbyte and 140–Mbyte disk drives); NT6M72AE, (required for 380–Mbyte disk drives w/o 56k polling, DPP systems w/o 56K polling, compatible with 72–and 140–Mbyte disk drives)

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (J5)	Center pin to A pin Center pin to B pin	Processor A select Processor B select	A/B	
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Notes:
Note 1: Make sure any circuit pack option settings are correct before replacement. Improper performance can be caused by incorrect settings, and produce faultlike symptoms in the DPP.
Note 2: See Figure 13–1.
Note 3: For circuit packs at A15, make sure jumper J5 is set for selection of the disk drive in the A chassis.
Note 4: For circuit packs at B15, make sure jumper J5 is set for selection of the disk drive in the B chassis.

Figure 13–1
Disk II crossover (A15 and B15) circuit pack (NT6M72AC, NT6M72AD, and NT6M72AE; 72– thru 380–Mbyte disk drives w/o 56K or compression polling options



Disk controller circuit pack

Located directly on top of the 72–Mbyte and 140–Mbyte disk drives, this circuit pack provides data management and data control for Winchester–type disk drives. The disk controller circuit pack uses as its host interface the industry standard 8–bit, parallel, bidirectional SCSI bus.

See Table 13–2 for the option settings on this circuit pack. Figure 13–2 shows option locations and circuit pack layout.

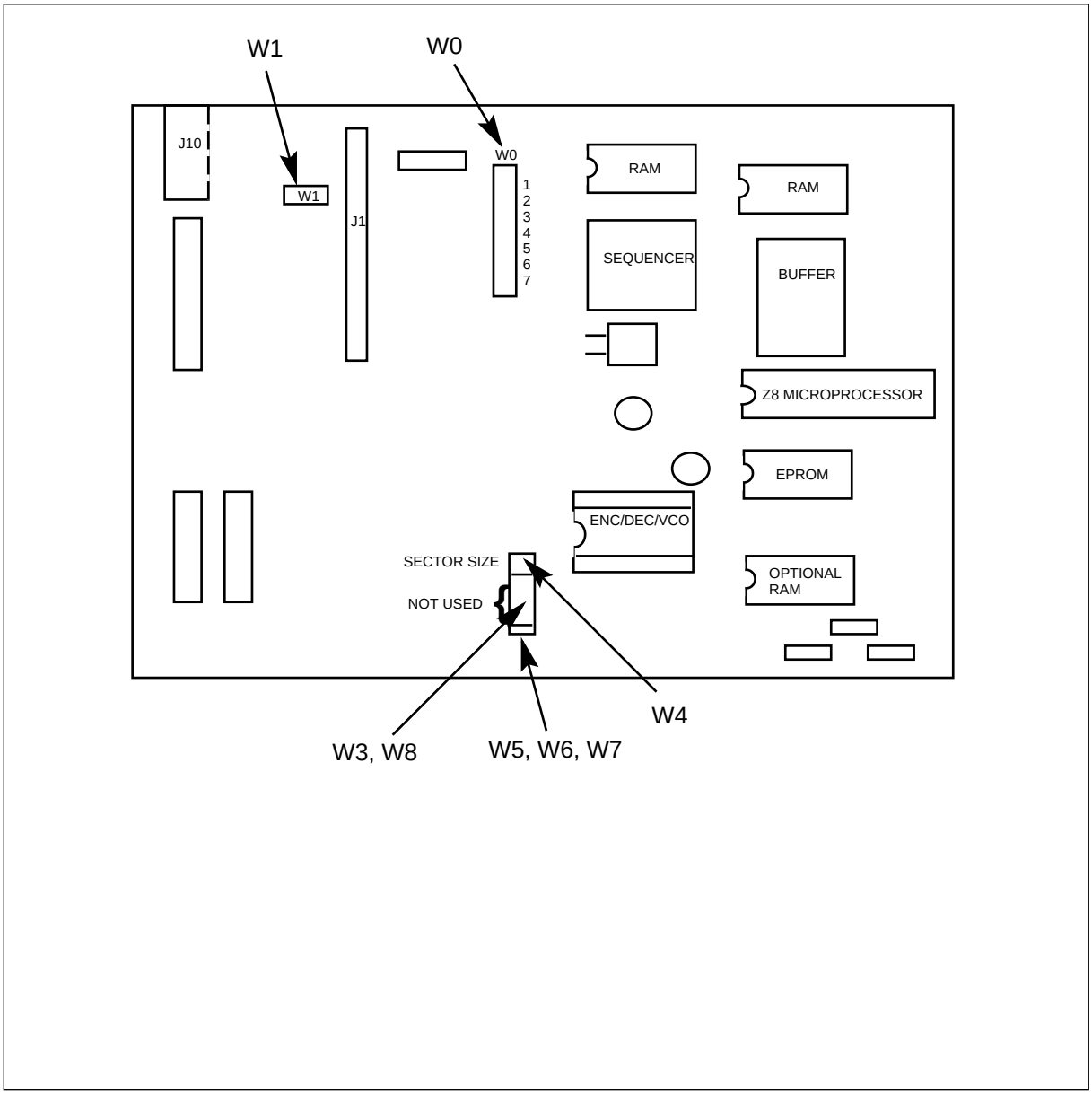
Note: This pack is not field changeable.

Table 13–2
Disk controller circuit pack (A21A1) options – part number: 680–9143

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (W0)	State Pri. 0 shorted; I.D. = 0 1 shorted; I.D. = 1 2 shorted; I.D. = 2 3 shorted; I.D. = 3 4 shorted; I.D. = 4 5 shorted; I.D. = 5 6 shorted; I.D. = 6 7 shorted; I.D. = 7	SCSI Controller ID. Defines the SCSI device priority. ID 7 is the highest priority in a multi–controller configuration.	0	Must be the same as the factory setting.
Jumper (W1)	1 – 2 = parity enabled 2 – 3 = parity disabled	Host Parity	1–2	Must be the same as the factory setting.
Jumper (W2)	Not used			
Jumper (W3) (W4)	W3 W4 Bytes Per Sector open open 128 short open 256 open short 512 short short 1024	Select disk drive Sector Size	W3 open W4 short	Must be the same as the factory setting.
Jumper (W5) (W6) (W7) (W8)	Function established in the copper tracings; do not modify	Logical Unit Number Assignment.	Out Out Out Out	Must be the same as the factory setting.
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Note:
Note 1: There are no customer–definable options on this circuit pack. Information is for reference only.
Note 2: Only present on the 72–Mbyte and 140–Mbyte disk drives.

Figure 13–2
Disk controller (A21A1 and B21A1) circuit pack (680–9143) options



Disk controller circuit pack

Located directly on top of the 72–Mbyte and 140–Mbyte disk drives, this circuit pack provides data management and data control for Winchester–type disk drives. The disk controller circuit pack uses as its host interface the industry standard 8–bit, parallel, bidirectional SCSI bus.

See Table 13–2 for the option settings on this circuit pack. Figure 13–2 shows option locations and circuit pack layout.

Note: This pack is not field changeable.

There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

Figure 13–3
Disk II crossover (A15 and B15) circuit pack (NT6M72AC, NT6M72AD, and NT6M72AE; 72– thru 380–Mbyte disk drives, BCS25–28 DPP systems) options

Table 13–3
Disk controller PCA (A21A1) option references – part number: 680–9143

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (W0)	State Pri. 0 shorted; I.D. = 0 1 shorted; I.D. = 1 2 shorted; I.D. = 2 3 shorted; I.D. = 3 4 shorted; I.D. = 4 5 shorted; I.D. = 5 6 shorted; I.D. = 6 7 shorted; I.D. = 7	SCSI Controller ID. Defines the SCSI device priority. ID 7 is the highest priority in a multi–controller configuration.	0	Must be the same as the factory setting.
Jumper (W1)	1 – 2 = parity enabled 2 – 3 = parity disabled	Host Parity	1–2	Must be the same as the factory setting.
Jumper (W2)	Not used			
Jumper (W3) (W4)	W3 W4 Bytes Per Sector open open 128 short open 256 open short 512 short short 1024	Select disk drive Sector Size	W3 open W4 short	Must be the same as the factory setting.
Jumper (W5) (W6) (W7) (W8)	Function established in the copper tracings; do not modify	Logical Unit Number Assignment.	Out Out Out Out	Must be the same as the factory setting.
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Table 13–3
Disk controller PCA (A21A1) option references – part number: 680–9143 (continued)

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site

Note:
Note 1: See Figure 13–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only.
Note 3: Only present on the 72–Mbyte and 140–Mbyte disk drives.

Notes:
Note 1: Refer to information earlier in this document.
Note 2: There are no customer–definable options on this PCA. Information is shown for reference purposes only. This data is to be used for verification during initial DPP system installation and/or PCA replacement to make certain that the replacement PCA is set–up the same as the PCA being replaced.
Note 3: Only present on the 72–Mbyte and 140–Mbyte disk drives.

Figure 13–4
Disk controller (A21A1 and B21A1) PCA (680–9143) options

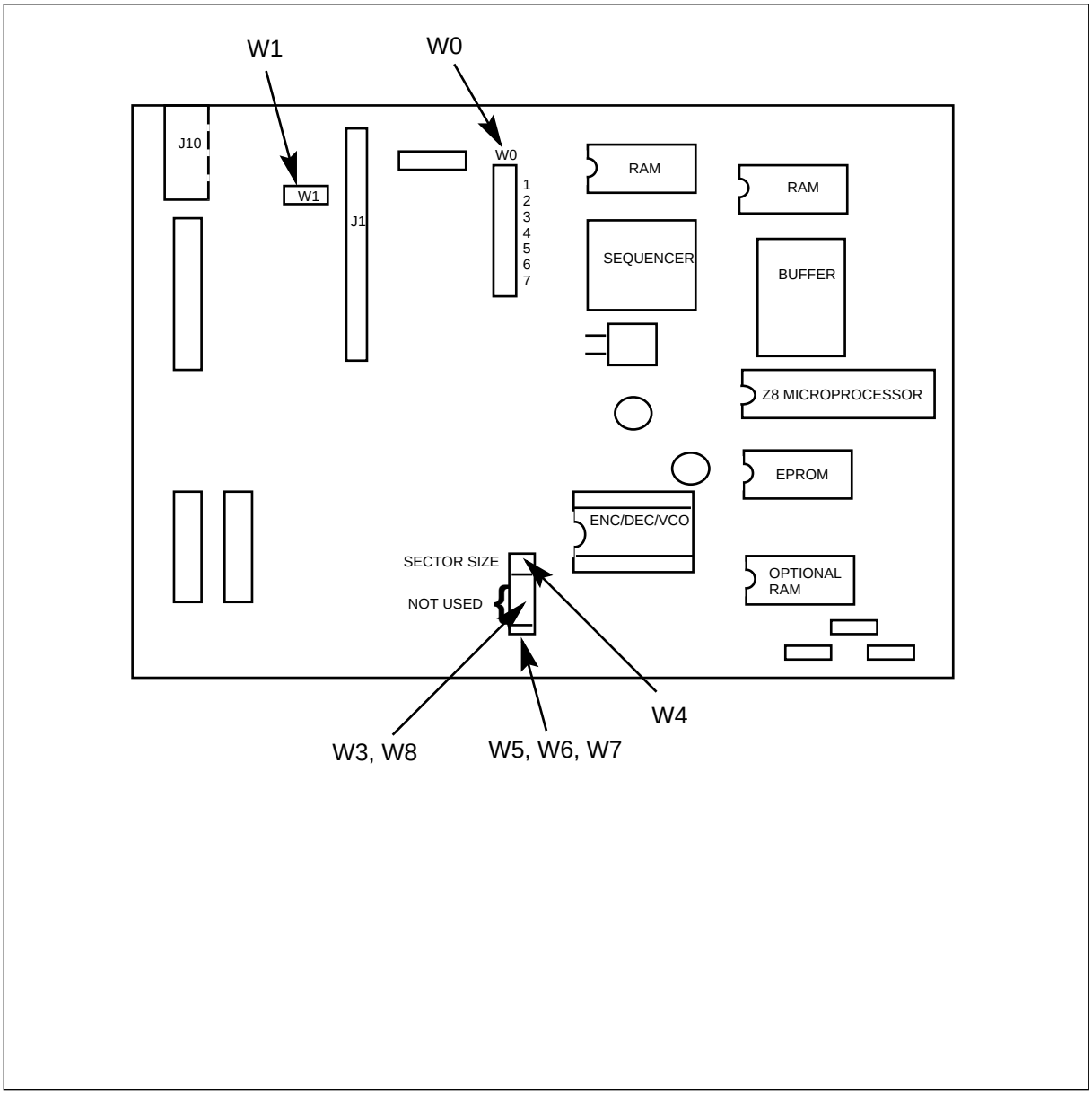


Table 13–4
Disk controller PCA (B21A1) option references – part number: 680–9143

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (W0)	State Pri. 0 shorted; I.D. = 0 1 shorted; I.D. = 1 2 shorted; I.D. = 2 3 shorted; I.D. = 3 4 shorted; I.D. = 4 5 shorted; I.D. = 5 6 shorted; I.D. = 6 7 shorted; I.D. = 7	SCSI Controller ID. Defines the SCSI device priority. ID 7 is the highest priority in a multi–controller configuration.	0	Must be the same as the factory setting.
Jumper (W1)	1 – 2 = parity enabled 2 – 3 = parity disabled	Host Parity	1–2	Must be the same as the factory setting.
Jumper (W2)	Not used			
Jumper (W3) (W4)	W3 W4 Bytes Per Sector open open 128 short open 256 open short 512 short short 1024	Select disk drive Sector Size	W3 Open W4 Short	Must be the same as the factory setting.
Jumper (W5) (W6) (W7) (W8)	Function established in the copper tracings.	Logical Unit Number Assignment.	Out Out Out Out	Must be the same as the factory setting.
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Table 13–5
Disk controller circuit pack (B21A1) options – part number: 680–9143

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (W0)	State Pri. 0 shorted; I.D. = 0 1 shorted; I.D. = 1 2 shorted; I.D. = 2 3 shorted; I.D. = 3 4 shorted; I.D. = 4 5 shorted; I.D. = 5 6 shorted; I.D. = 6 7 shorted; I.D. = 7	SCSI Controller ID. Defines the SCSI device priority. ID 7 is the highest priority in a multi–controller configuration.	0	Must be the same as the factory setting.
Jumper (W1)	1 – 2 = parity enabled 2 – 3 = parity disabled	Host Parity	1–2	Must be the same as the factory setting.
Jumper (W2)	Not used			
Jumper (W3) (W4)	W3 W4 Bytes Per Sector open open 128 short open 256 open short 512 short short 1024	Select disk drive Sector Size	W3 Open W4 Short	Must be the same as the factory setting.
Jumper (W5) (W6) (W7) (W8)	Function established in the copper tracings.	Logical Unit Number Assignment.	Out Out Out Out	Must be the same as the factory setting.
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

SCSI Crossover circuit pack – turbo only

General Description

The SCSI Crossover (Xovr) circuit packs are located at positions A15 and B15 on the inner portion of the hinged card panel at the rear of the A and B chassis. They are connected between both SCSI Interface circuit packs in the DPP (A side and B side) and both SCSI Disk Drive assemblies (Disk 1, disk A at A21; Disk 2, disk B at B21).

The system interface ports of the SCSI Xovr circuit packs (40–pin connectors Jl & J2) consist of 8 data lines with parity and 12 control lines. One port is provided for each of the two SCSI Interface cards. The SCSI port provides the system interface to the SCSI disk drives.

Power from both A and B chassis is provided at this connector in a diode OR'ed arrangement for redundancy purposes.

The SCSI XOVR circuit packs provide the following functions:

- Interface between DPP system backplane (SCSI Interface circuit pack) and SCSI Disk Drives.
- Support for crossover and disk selections for the SCSI Interface circuit pack.
- Support for disconnect/reconnect feature.
- Full hardware implementation; no software required.
- Two 40–Pin access ports; one for each SCSI Interface circuit pack.
- 50–pin access port for the disk drive.
- 4–pin power connector identical to current crossover card.
- Either disk drive tristatable off the SCSI bus in case of a fault.

See Table 14–1 for the jumper setting on this circuit pack. Figure 14–1 shows the circuit pack layout.

Replacing the SCSI circuit pack

To replace the SCSI circuit pack, use the following procedure.

Procedure 14–1
SCSI XOVR circuit pack replacement

Step	Description	Notes
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling these materials. Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of a grounding strap.	
	 **WARNING** Since the DPP is powered up during this procedure, observe all safety procedures for operations on live equipment.[1]	
1	Wait for a low traffic period, if possible.	Make sure no polling is taking place.

2	Locate the failing SCSI/XOVR circuit pack and change the disk mode to the other disk ONLY mode, if necessary.
	
	Enter: (at the terminal)
	
	>DISK MODE xx (cr)
	
	where:
	xx = disk mode = AO = A ONLY
	= BO = B ONLY
		The other disk is the one not in the same chassis as the suspected SCSI/XOVR circuit pack.
		
		Proper response =
		
		`DISK MODE: AO`
		or
		`DISK MODE: BO`

3	Loosen the slotted screws which fasten the outer edges of the rear panel assembly to the cabinet.	
4	Remove the appropriate rear panel.	Wait for the disk mode changed to complete.

(continued)

Procedure 14–1
SCSI XOVR circuit pack replacement (continued)

Step	Description	Notes
5	Pull the rear panel away from the cabinet. Remove the front panel of the chassis to improve convection cooling, if necessary.	Put the two panels in a safe place to prevent bending and scratching.
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them.	
6	Loosen the 2 screws at the top of the hinged card panel and the screw at the bottom of the hinged card panel.[2]	Let it swing slowly down from the top until it rests.
7	First remove power cable (J4), then any cables and screws connected to the suspected circuit pack.[3,4]	Gently pull the suspect assembly loose from its mounting position.

8	Set the A/B jumper. Then mount the replacement assembly in the vacated position and reconnect any cables removed in step 7 in reverse order. Verify the repair by switching disk modes back to PRIME.[5]
	
	Enter: (at the terminal)
	
	>DISK MODE xx (cr)
	
	where:
	xx = disk mode = AP = A PRIME
	= BP = B PRIME
	
	Proper response =
	
	`DISK MODE: AP`
	`or`
	`DISK MODE: BP`
		(from disk mode AO)
		from disk mode BO)
		
		(If the replacement XOVR circuit pack solves the problem, the DPP will begin a disk copy that may take several hours, depending on the data on the PRIME disk.

9	Lift the hinged circuit assembly gate back to its vertical position and tighten the (3) screws loosened in step 4.[6]	Remove the insulating material, if used.

(continued)

Procedure 14–1
SCSI XOVR circuit pack replacement

Step	Description	Notes
10	Route all wires and cables to avoid pinching or crimping when the rear panel is reinstalled.	
11	Seat the rear panel. Reinstall the slotted pan head screws previously removed.	From step 1. See the note about screw tightening.
12	Enter: (at the terminal) **>TEST ACT (cr)** Proper response = `DISK TEST PASSED`	This is one message that may appear; see Table 14–1 for further information. For any other response, see the procedure sheet for that message and perform activities listed there.
13	Reattach the front panel of the chassis, if removed.	Replace rear panels for proper convection cooling.

Notes:
Note 1: Make sure any circuit pack option settings are correct before replacement. Improper performance can be caused by incorrect settings, and produce faultlike symptoms in the DPP.
Note 2: If replacing the circuit pack at A15 i, use a Styrofoam block or another insulating material, about 1" x 1" x .5", to insulate the pins of the 16–pin cable on the P/A Comm circuit pack to prevent accidental shorting against the chassis.
Note 3: Verify the cable markings (identification) or attach labels to the cables when removing to facilitate replacement in the correct positions.
Note 4: If the circuit pack has option jumpers or straps that must be set before installation, make sure the jumpers/straps are set exactly the same as the ones on the circuit pack to be replaced.
Note 5: Make sure the cable(s) are connected properly (pin 1 in the correct position) to prevent data loss.
Note 6: When replacing the screws, align carefully before tightening to avoid stripping. Tighten the screws, alternating until all are equally tight. Do not "cinch down" any one screw until all are properly aligned; no binding or force needed to turn.

End

Table 14–1
SCSI crossover circuit pack (A15 and B15) options – part number: NT6M93AA; 380–Mbyte disk drives with 56K polling; 760–Mbyte, 1.7 GB disk drives, all instances

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (J5)	1 – 2 disk A 2 – 3 disk B	Disk A select Disk B select	A/B (refer to notes 3 and 4)	
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Notes:
Note 1: See Figure 14–1.
Note 2: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement pack is set–up the same as the pack being replaced.
Note 3: For the SCSI Crossover circuit pack at position A15, make sure jumper J5 is set for selecting the disk drive in the A chassis.
Note 4: For the SCSI Crossover circuit pack at position B15, make sure jumper J5 is set for selecting the disk drive in the B chassis.

Figure 14–1
SCSI crossover (A15 and B15) circuit pack (NT6M93AA; 380–Mbyte disk drives with 56K polling; 760–/1700–Mbyte disk drives; options

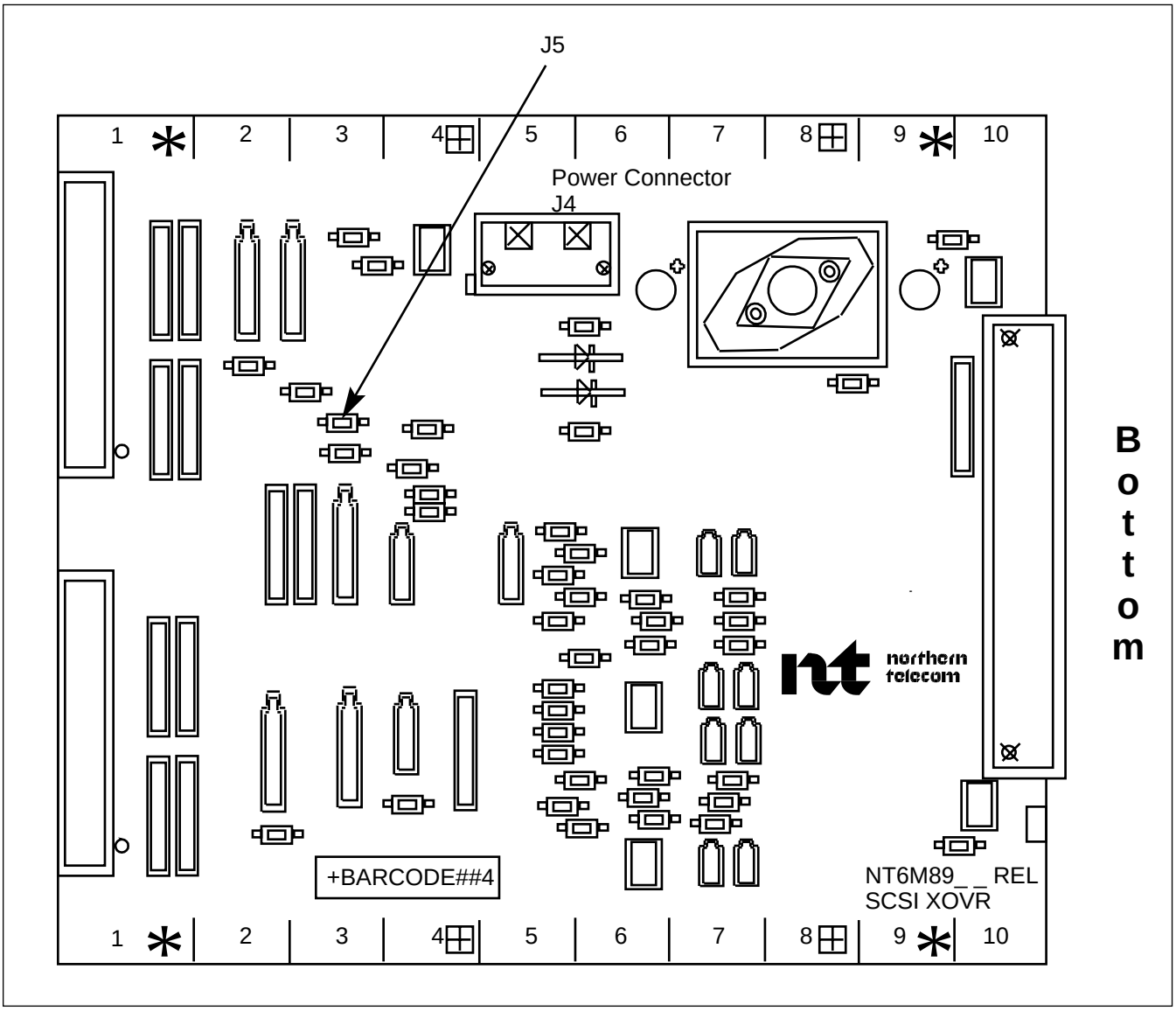
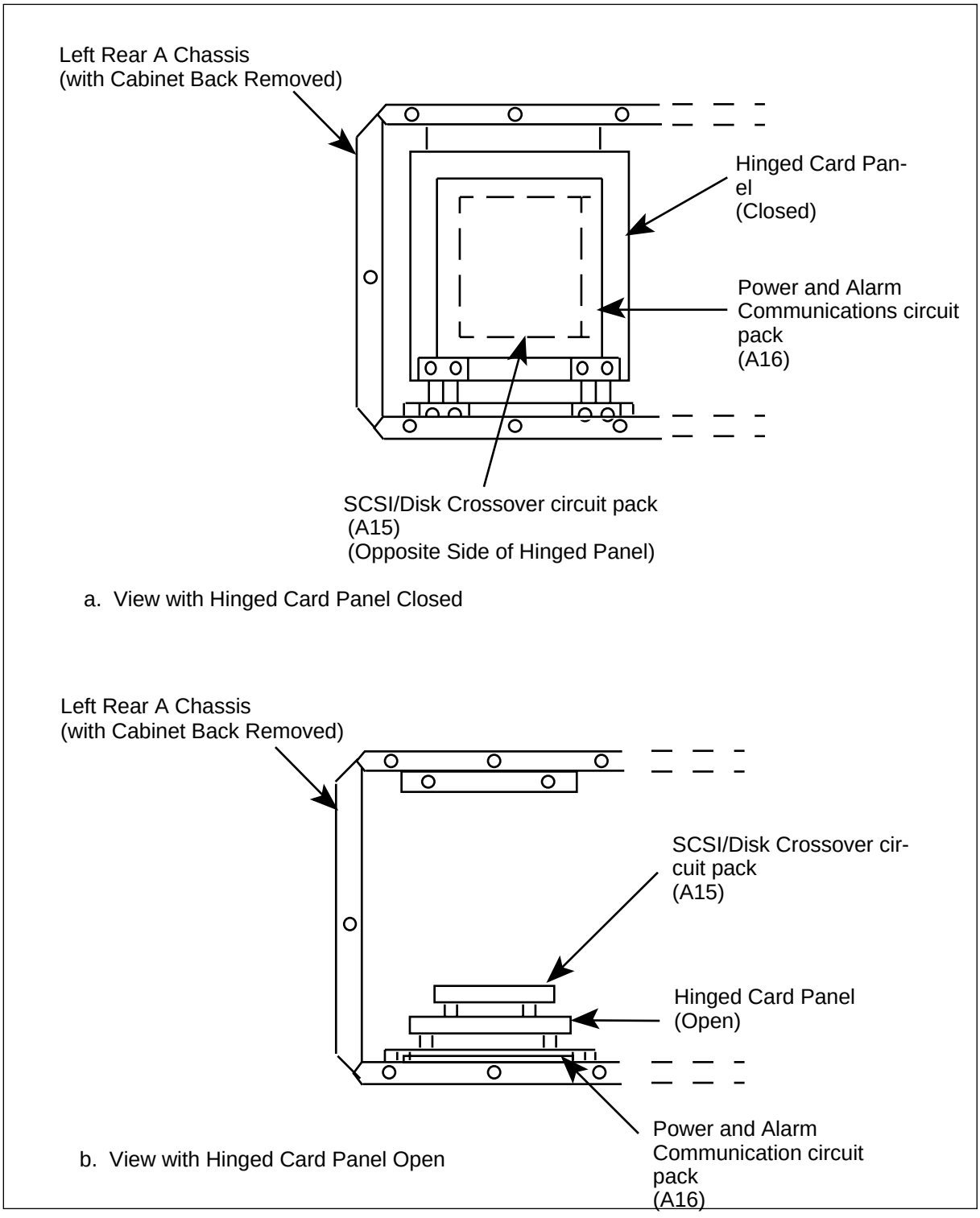


Figure 14–2
Opening hinged panel at the rear of the DPP chassis



56K Crossover circuit pack – turbo only

General Description

The 56K Crossover (XOVR) circuit pack provides the following capabilities:

- Interface between the DPP system backplane (56K Interface circuit pack at A7 and B7) and 56K Connector circuit pack.
- Support for XOVR and interface selections for the Serial Communication Controller (SCC) ports.
- Support for V.35 and RS–232 interface for the SCC ports.
- Full hardware implementation; no software required.
- Two 40–pin access ports; one for each of the 56K Interface circuit packs.
- A 60–pin access for the 56K Connector circuit pack.
- 12–pin power connector like the one on the P/A Comm circuit pack.

56K XOVR circuit pack layout is shown in Figure 15–2. Table 15–1 provides option setting information.

Replacing 56K Xovr circuit pack

To replace this circuit pack, use the following procedure.

Procedure 15–1
56K XOVR circuit pack replacement

Step	Description	Notes
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling these materials. Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of a grounding strap.	
	 **WARNING** Since the DPP is powered up during this procedure, observe all safety procedures for operations on live equipment.[1]	
1	Wait for a low traffic period, if possible.	Make sure no polling is taking place.
2	Notify technical assistance personnel of the temporary loss of the polling links.	DPP systems with 56K polling use a path through the 56K Xovr to the 56K Connector circuit pack for polling link.
3	Remove the slotted screws which fasten the outer edges of the rear panel assembly to the cabinet.	
4	Remove the rear panel of the B chassis.	
5	Pull the rear panel away from the cabinet. Remove the front panel of the B chassis to improve cooling, if necessary.	Put the two panels in a safe place to prevent bending and scratching. The DPP will change to an "Only" processor mode.
6	First remove the power cable (J1) then the cables connected to the 56K Xovr circuit pack.[1, 2]	Various alarms may also activate. This is normal. Silence the alarm at the DMS–100 and proceed to step 7.
7	Remove the screws that fasten the 56K Xovr circuit pack.	Gently remove the circuit pack from its mounting position.

(continued)

Procedure 15–1
56K XOVR circuit pack replacement (continued)

Step	Description	Notes
8	Mount the replacement assembly in the vacated position.	
9	Reattach any cables removed in step 6 in reverse order.	Office alarms cease.
10	Properly reroute all cables.	Make sure all wires and cables are routed so they are not pinched or in contact with the arc of the fan blades.
11	If alarm status shows active alarms, troubleshoot all alarm conditions . At the maintenance terminal, enter: **TEST ACT (cr)** **TEST STDBY (cr)** Test the polling function.	
12	If alarm status shows active alarms, resolve all alarm conditions present.	
13	Seat the rear panel in its fully seated position and reinstall the slotted pan head screws previously removed.[3]	From step 3.
14	Reattach the front panel of the chassis.	If removed.
15	At the maintenance terminal, enter: **>RSERR ACT 00 (cr)**	To clear any alarms on the active processor.
16	At the maintenance terminal, enter: **>RSERR STDBY 00 (cr)**	To clear any alarms on the standby processor.
17	At the Switch and Status Panel: a. Press the A/B Select Switch to match the active processor.	If all alarms clear, place the active processor unit in PRIME mode.

(continued)

Procedure 15–1
56K XOVR circuit pack replacement (continued)

Step	Description	Notes
	b. Make the O/P Mode Select Switch P.	Make the active processor the PRIME processor.
	c. Turn the Mode Switch to the right.	Turn it 45 degrees to the right and release.
18	Test the polling link(s) see if they are still failing.	

Notes:
Note 1: Verify the cable markings (identification) or attach labels to the cables as they are removed to facilitate replacement in the correct positions.
Note 2: Make sure the jumpers/straps are set the same as the ones on the circuit assembly to be replaced.
Note 3: When replacing the screws, align carefully before tightening to avoid stripping. Tighten the screws, alternating until all are equally tight. Do not "cinch down" any one screw until all are properly aligned; no binding or force needed to turn.

End

Figure 15–1
Opening hinged panel at the rear of the DPP chassis

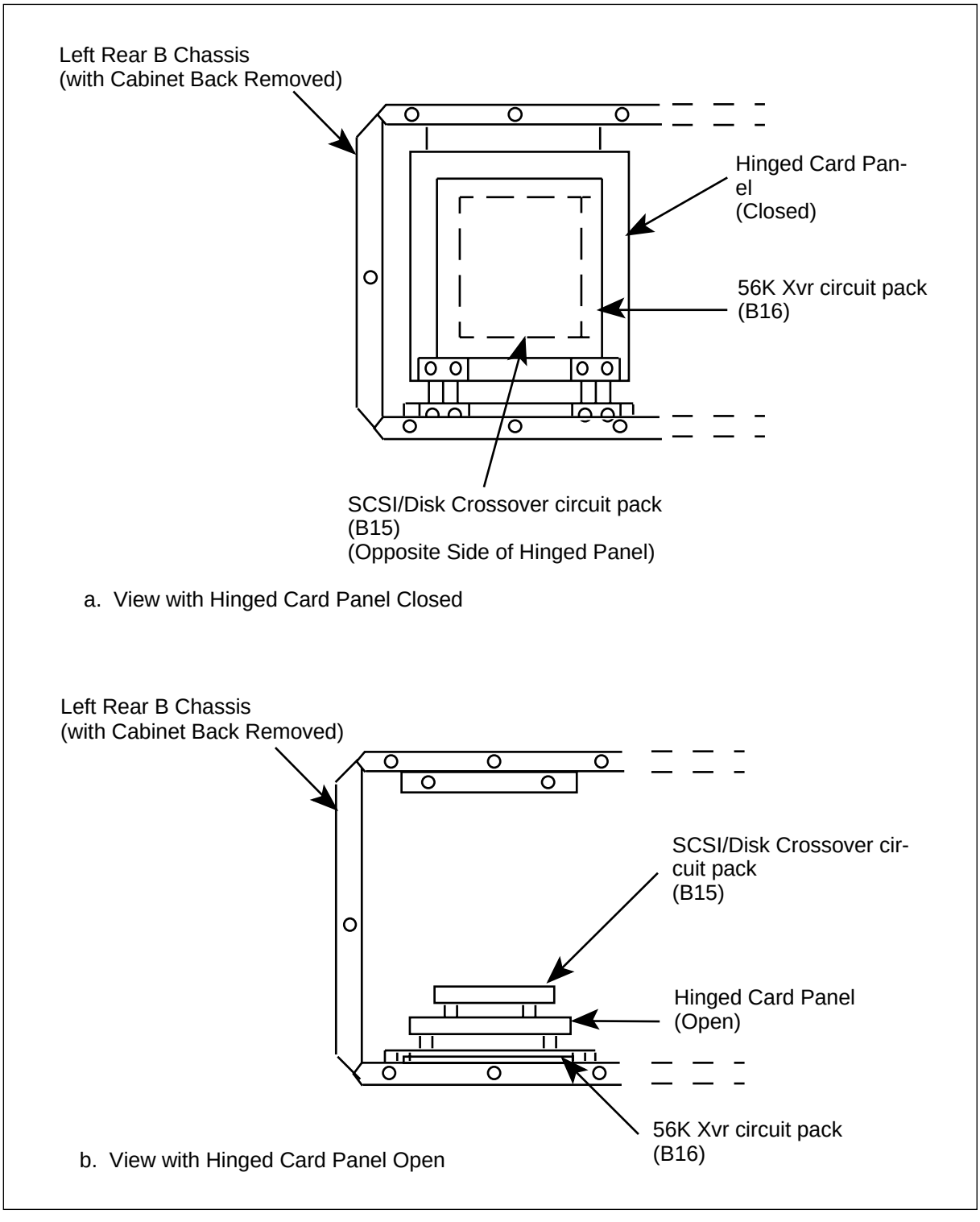
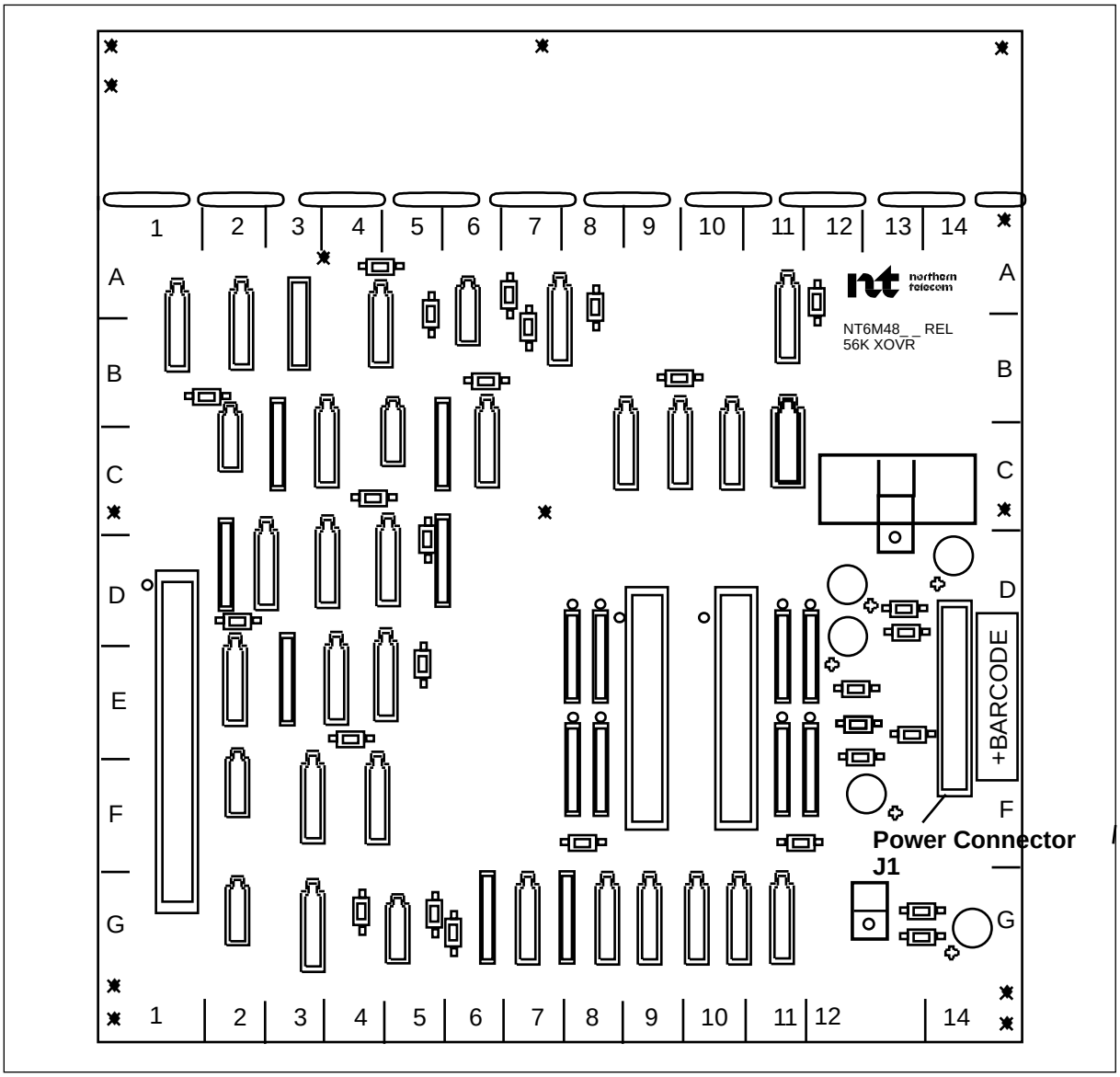


Table 15–1
56K crossover circuit pack (B16) options – part number: NT6M48AA

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper	None used			
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

Notes:
Note 1: There are no customer–definable options on this circuit pack. Information is shown for reference only. Use this data for verification during initial DPP system installation and/or circuit pack replacement to make sure the replacement circuit pack is set up the same as the circuit pack being replaced.

Figure 15–2
56K Crossover (B16) circuit pack (NT6M48AA) Options



Four–channel communication circuit pack

General Description

The Four–Channel Communication (Comm) circuit pack provides the physical interface between the DPP's serial communication channels and external devices. It is located on the Connector Mounting panel on the right side of the upper chassis, as viewed from the front.

Connector panel

This panel is simply called the Connector panel for the nonturbo DPP (A Chassis). Required for 56K polling, it is called the 56KConnector panel for the turbo DPP (B Chassis). The 56K Connector Panel is used with the Turbo feature. This feature can support the 56K polling feature and with 760–Mbyte disk drives. It may also have 380–Mbyte disks.

This panel supports four serial channels. It provides pin–out connection between a single 50–pin ribbon cable and four DB–25 connectors. It is totally passive, containing connectors only, no active circuitry. It supports all EIA interface leads for synchronous operation.

The panel provides the following functions:

- up to four channels of EIA RS–232 compatible serial interface (DTE interface); system architecture allows only one active interface at a time.
- physical interface between the serial channels and the 56K XOVR panel.

Interface between this panel and the 56 XOVR circuit pack is via a 50–pin ribbon cable. Signals carried by the cable are

- nine EIA RS–232 leads for each of the four channels
- multiple logic ground lines.

Four–Channel Comm circuit pack

This pack supports four serial channels. It provides pin–out connection between a single 50–pin ribbon cable and four DB–25 connectors. The circuit pack is totally passive, containing connectors only and no active circuitry. All EIA interface leads are supported, whether for synchronous or asynchronous operation.

The Four–channel circuit pack provides the following functions:

- up to four channels of EIA RS–232 compatible serial interface (DTE interface)
- two channels, jumper–selectable, between Automatic Dial–up Unit interface (unused) to modem/telephone line and serial channels
- physical interface serial channels and the P/A Comm circuit pack.

Interface between this circuit pack and the P/A Comm circuit pack is via a 50–pin ribbon cable. Signals carried by the cable are

- nine EIA RS–232 leads for each of the four channels
- multiple logic ground lines.

Figure 16–1 shows the jumper locations and circuit pack layout. See Table 16–1 for the jumper settings.

Replacing the Four–channel comm pack

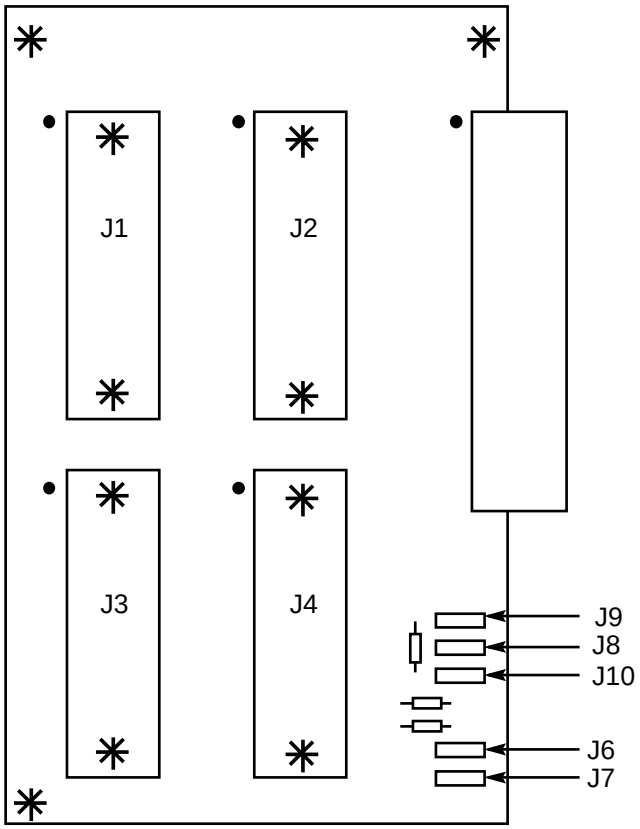
Use the following procedure to replace this pack.

Procedure 16–1
Four–Channel Comm circuit pack replacement

Step	Description	Notes
	 **CAUTION** Since all DPP circuit packs are static sensitive, be careful when handling them. Wear a wrist grounding strap when working with the DPP. Jacks at the lower right of the Rover Interface panel (B chassis) and the lower right of the Switch and Status Panel (A chassis) are provided to accept the banana plug connection on the end of a grounding strap.	
	 **WARNING** Since the DPP is powered up during this procedure, observe all safety procedures for operations on live equipment.	
1	Wait for a low traffic period, if possible.	Make sure no polling is occurring.
2	Notify technical assistance personnel of the temporary loss of MMI and polling links.	Polling link for DPP systems without 56K polling is routed through the P/A Comm circuit pack. DPP systems with 56K polling use a path through the 56K Xovr to the 56K Connector circuit pack.
3	Remove the slotted screws on the outer edges of the rear panel assembly to the cabinet.	
4	Remove the rear panel of the A chassis.	
5	Pull the rear panel away from the cabinet. Remove the front panel of the A chassis to improve convection cooling, if necessary.	Put the two panels in a safe place to prevent bending and scratching.

6	Remove the MMI cable.	J2 and J3 on "A" chassis.
7	Remove the hex–head screws attaching the four–channel communication circuit pack.	Use an offset ratchet driver for limited clearance.
8	Remove the four–channel comm circuit pack. Verify the options on the pack.	Gently remove the pack from its position.
9	Insert the replacement pack in the vacated position.	
10	Reattach any cables removed in step 6.	Office alarms cease as the polling links reactivate.
11	Properly route all cables.	Make sure all wires and cables are routed so they are not pinched or in contact with the arc of the fan blades.
12	Replace the hex–head screws removed in step 7..	
13	Seat the rear panel in its fully seated position and reinstall the slotted pan head screws previously removed.[3]	
14	Replace the rear panel of the A chassis.	
End		

Figure 16–1
Four–channel communications (A17) circuit pack (NT6M85AA) options



Notes: 1. When used with digital data lines, make sure this pack is release 03 or later.
2. Jumpers J6, J7, J8, J9, and J10 may be on the reverse side of some printed circuit assemblies.

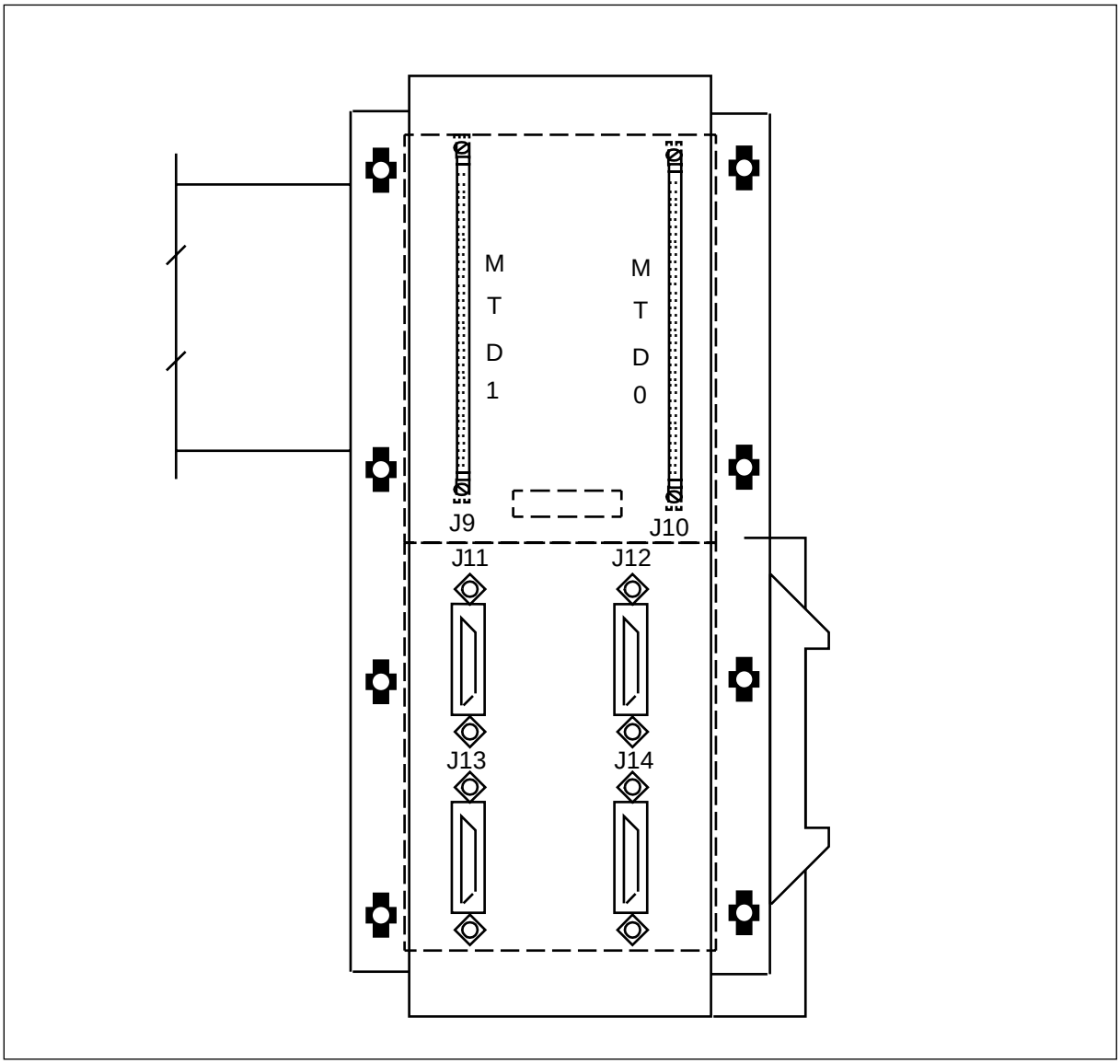
Table 16–1
Four–channel communications circuit pack (A17) options – part number: NT6M85AA

Device type (number)	Position/setting	Function	Setting	
			Factory	On–site
Jumper (J6)	2–3	ADU Operation*	1–2	Must be same as factory setting.
	1–2	No ADU operation (EIA on chan 1 &2)		
Jumper (J7)	2–3	ADU Operation*	1–2	Must be same as factory setting.
	1–2	No ADU operation (EIA on chan 1 &2)		
Jumper (J8)	2–3	ADU Operation*	1–2	Must be same as factory setting.
	1–2	No ADU operation (EIA on chan 1 &2)		
Jumper (J9)	2–3	ADU Operation*	1–2	Must be same as factory setting.
	1–2	No ADU operation (EIA on chan 1 &2)		
Jumper (J10)	2–3	ADU Operation*	1–2	Must be same as factory setting.
	1–2	No ADU operation (EIA on chan 1 &2)		
Strap	None used			
DIP Switch	None used			
Rotary Switch	None used			
Switch	None used			

End

***Note:** ADU operation is not used on the DPP .

Figure 16–2
56K connector panel assembly (B26) panel (NT6M65AA) options



Power supplies

Powering down DPP for maintenance

Powering down the DPP for maintenance is divided into two categories:

- +8.5 V dc power down
- –48 V dc power down

+8.5 V dc power down, removal, or maintenance of circuit packs requires removing the +8.5 V dc output from the DPP power supply. The circuit breaker is a push ON (1), push OFF (O) rocker switch. Press the rocker switch to the OFF (O) position to manually open the +8.5 V dc line. To reset an automatically tripped circuit breaker, first push the OFF (O) side of the circuit breaker, then push the ON (1) side.

–48 V dc Power Down. Power down the –48 V dc C.O. input power for maintenance on the following:

- Power supply
- Cooling fan (except for brief periods of time, i.e. when the required spare parts are near at hand).

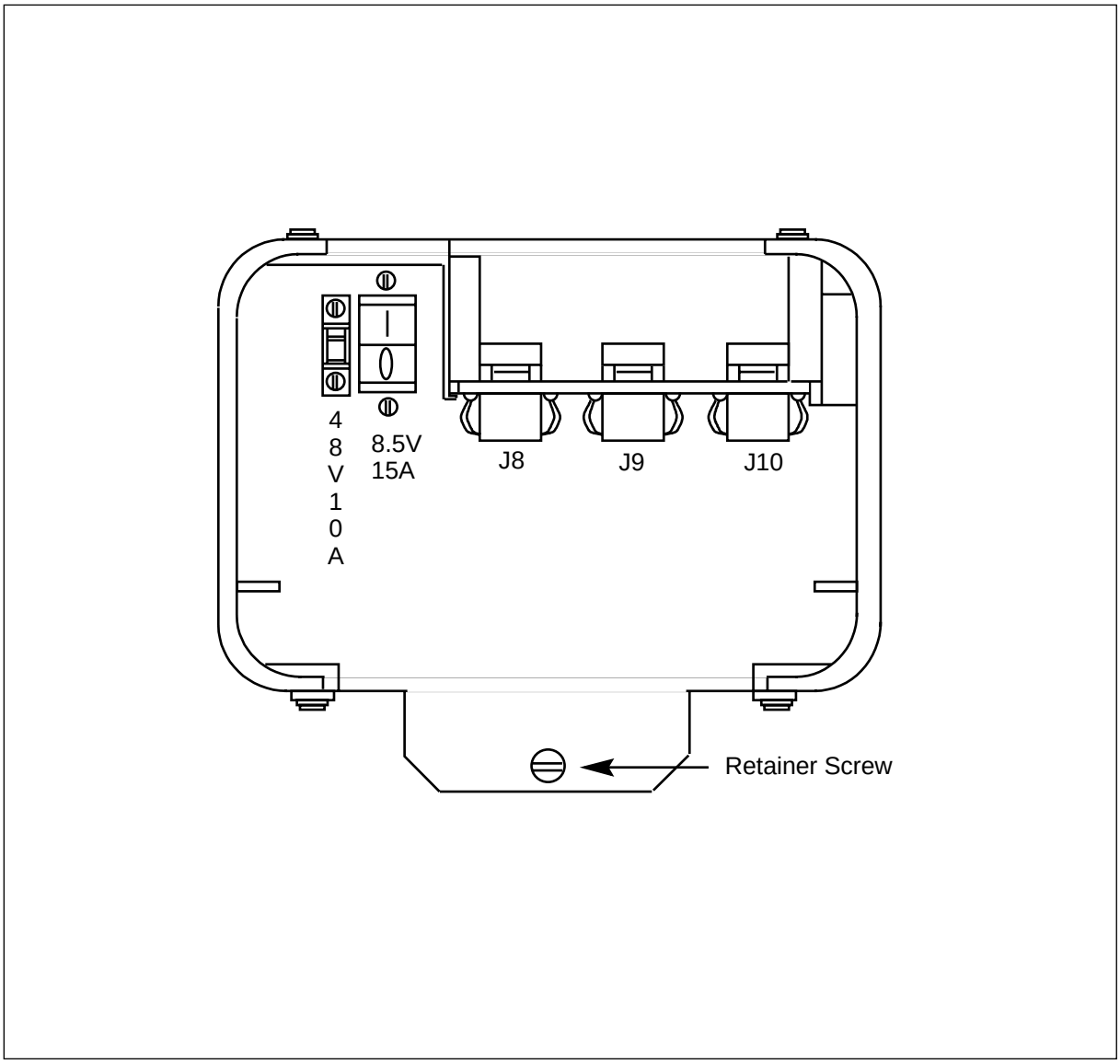
Since the processor and disk in the chassis are powered down, make sure the processor mode and the disk mode are ONLY (toward the other chassis and disk) before the power is removed.

When performing any type of maintenance on the fan (fan not running), open the front cover of the DPP to improve convection cooling. Perform the necessary functions. Power down the –48 V dc when the fan is inoperable for extended periods of time to prevent damage from overheating.

For maintenance, power down the –48 V dc at the external circuit breakers (or other disconnects) for power distribution control. Note the location of the disconnects before removing any equipment in case of an emergency. Only remove the –48 V dc fuse from the power supply to power down the DPP in an emergency.

Leave the disk drives untouched for at least 30 seconds after power down since vibration during power down may damage the disk drive.

Figure 17–1
DPP power supply assembly



DPP system fuses

DPP fuses are located on the front panel of the DPP power supply.

The power supply has the –48 V dc circuit fused. A GMT–type fuse is used. These fuses have a spring–loaded colored flag which opens when the fuse is blown. To replace, pull the blown fuse straight out from the fuse holder and insert the new fuse of the same type and rating.

A clear fuse cover is furnished for covering the fuse as a safety precaution. After performing fuse replacement, remember to install the cover.

The power supply has a circuit breaker to protect the +8.5 V dc line.

Figure 17–1 shows the location of the fuses and Table 17–1 gives fuse replacement information.

Table 17–1
Fuse replacement information

Fuse function	Fuse function	Amperes (color)	Fuse type and replacement part number
Power Supply	–48 V dc from CO	10 (Grn)	10 ampere fuse: Buss GMT–10 NT part No: A0108995
Fan Filter PCA Assembly[1]	–48 V dc from CO	.5	.5 ampere fuse NT part No: A0109762

Replacing power supply for maintenance

If removing a power supply, follow Procedure 17–1. The only tool needed is a small flat–blade screwdriver. If necessary, have replacement fuses on hand.

Procedure 17–1
Power supply replacement

Step	Description	Notes
1	Remove the front panel of the DPP. Put it in a safe place to avoid damage. Remove only the top panel if you are changing the A power supply.	Loosen the four captive screws on the left and right sides of the front panel; carefully remove the front panel.
	Remove both the A and B front panels if changing the B power supply.	This allows access to the Switch and Status Panel.
2	Make sure the other CPU is in the ONLY mode of operation, and the other disk is in the ONLY mode of operation. First put the disks to an ONLY mode.	Press the A/B rocker switch to match the processor with the good power supply. Press the O/P switch to 0 and turn the key switch 45∂ clockwise.
3	Power down the faulty power supply. See Figure 17–1.	
	Remove the –48 V dc C.O. power.	Remove the –48 V dc source for the processor chassis at the DMS–100 fuse panel; disk drive in this chassis is now disabled
4	Remove the three connector plugs from the front of the power supply.	Pull down gently; fold the cables back out of the way.
5	Loosen the slotted–head captive screw at the bottom of the power supply.	
6	Gently pull the power supply out of the chassis.	Make sure the three connectors (and cables) are out of the way during removal of the power supply unit.
7	To install the replacement power supply, make sure all cables and connectors are out of the way of the insertion path.	Make sure the proper fuses are installed in the replacement power supply. See Table 17–1 and Figure 17–1.
8	Gently slide the power supply into position until it is fully seated.	If any resistance, remove the power supply and check for obstructions. Remove the obstructions and reinsert the power supply.

(continued)

Procedure 17–1
Power supply replacement (continued)

Step	Description	Notes
9	Reconnect the three connectors removed in step 4 during the removal phase.	Connect as follows: Pwr Sup Plug — Conn. (Pwr Sup) a. J8 to P8 b. J9 to P9 c. J10 to P10
10	Tighten the slotted captive screw until snugly in place; do not bear down.	
11	Apply power to the unit. Restore the 8.5 V dc power. Wait for start–up activity to end and the message "S/W loaded" to print.	Restore the –48 V dc power source at the DMS–100 fuse panel. Press the I portion of the red circuit breaker in the upper left corner of the power supply until it clicks into place.
12	Make the processor system redundant.	Press the A/B rocker switch on the status panel to match the active processor. See step 2. Press the O/P switch to P and turn keyswitch clockwise.
13	Make the disk system redundant.	Type: DISK MODE x P where x = A or B, depending on whether the disk mode is A0 or B0.
14	Reinstall the front panel of the DPP.	Tighten the four captive screws on the left and right hand sides of the front panel. Do not bear down to tighten.

Notes:
Note 1: If both sides of the DPP are powered down, the DPP must be powered up according to the Switch and Status Panel switch settings or the Switch and Status Panel switch settings must be changed to match the side being powered up. Otherwise, the power fail circuit of the Error Control II causes an instant switch away from the powered down (selected) processor. If both processors are powered down and the Switch and Status Panel switches are set to the A processor, do not power up the B chassis. This causes the Error Control II to ignore other switch commands. If this power up condition occurs, it is cleared by setting the Switch and Status Panel switches to the selected side (processor) and turning the mode insert switch on the Switch and Status Panel. This condition does not exist when both processors are powered up together.

End

List of terms

AMA

Automatic Message Accounting

An automatic recording system which documents all of the necessary billing data of subscriber–dialed long distance.

AMATPS

AMA Teleprocessing System

An AMA data management system in the DMS–100 designed for use with BELLCORE AMA data. AMATPS consists of the DMS–100 Device Independent Recording Package (DIRP), the DPP, and a remote data collection center. The DMS–100 DIRP manages the flow of AMA data from the DMS–100 to the DPP. The DPP functions as the AMA data formatter (BCS25–26) and collector, and as the AMA transmitter. The remote polling center acts as the AMA data polling system.

BELLCORE

Bell Communications Research

A group responsible for coordinating Bell Operating Company projects and setting guidelines for DMS–100s.

BPS

Bits per second

CO

Central Office

A switching office arranged for terminating subscriber lines and provided with equipment and trunks for establishing connections to and from other switching offices.

CC

Central Control Complex

Comprises all Central Control functions of the DMS–100. It consists of the Central Message Controller, CPU, and Data Store.

CPU

Central Processor Unit

CTC

Counter Timer Circuit

A circuit on the DPP CPU circuit pack that handles vectored interrupts from various devices within the DPP that request access to the data bus for data transfer.

DIRP

Device Independent Recording Package

Software which automatically directs data from the various administrative and maintenance facilities to the appropriate recording devices.

DMA

Direct Memory Access

The use of special hardware for transferring data to and from memory to reduce the number of interrupts required for program data transfers.

DPP

Distributed Processing Peripheral

A peripheral device of the DMS–100 that functions as an AMA data collector and an AMA transmitter in the AMATPS of the DMS–100. The DPP collects AMA data from the DIRP, formats the data (BCS25–26), stores the data on its own internal disk, and transmits the data to a data collection center when polled by the collection center. The DPP performs the AMAT functions independently of the DMS–100, thereby off–loading the AMAT functions from the DMS–100 CC.

DRAM

Dynamic Random Access Memory

A Random Access Memory system that employs transistor capacitor storage cells. The logic state is stored in the capacitor and buffered by the transistor. The capacitive charge is only held for a short duration and must be refreshed at a periodic rate to maintain its programmed state.

DSI

Data Stream Interface

A DPP circuit that accepts AMA data from the DMS–100 MTD–driven circuit packs or equivalents. The DSI emulates a Magnetic Tape Drive on DMS–100 MTD Ports, duplicating all communications signals normally exchanged between the DMS–100 and an MTD.

DTR

Data Terminal Ready

A signal sent from a terminal device indicating to the host device its readiness to communicate.

EAI

Emergency Administrative Interface

A terminal port at the DPP to support the Emergency Administrative Terminal.

EAT

Emergency Administrative Terminal

A maintenance terminal connected directly to the DPP that is used for performing various maintenance functions on the DPP. The EAT connects to the DPP emergency administrative interface.

EIA

Electronic Industries Association

EMI

Electromagnetic Interference

Emissions given off by all electronic devices which may interfere with TV, radio, police radio, and other forms of electronic communication if emitting devices are not properly shielded.

EOT

End of Tape

A signal sent from an MTD to its host indicating that no more data should be recorded on the currently loaded tape.

EPROM

Erasable Programmable Read Only Memory

A read–only memory in which stored data can be erased by ultraviolet light and reprogrammed.

ESD

Electro–Static Discharge

The passing of electrical energy from a statically charged body to a discharged body or ground. Statically charged bodies may store several thousand volts, which has potential to severely damage or even destroy static sensitive electronic components such as Metal Oxide Semiconductor devices.

HOC

Host Office Collector

An AMA data collection center that polls Central Offices in its region on a prescheduled basis and compiles the collected data onto a magnetic tape. The tape is used by the Revenue Accounting Office for computing customer billing.

IC

Integrated Circuit

A series of interconnected active and passive electronic devices integrated into a single semi–conductor substrate (typically silicone) or deposited on a single substrate, and capable of performing one or more complete electronic functions.

IOC

Input/Output Controller

An equipment shelf which provides an interface between up to 36 Input/Output devices and the Central Message Controller. The IOC contains a Peripheral processor which independently performs local tasks, thus relieving the load on the CPU.

MAP

Maintenance and Administrative Position

A group of components which provide a Man–Machine Interface between OTC personnel and the DMS–100 Family. A MAP consists of Visual Display Unit, voice communications module, testing facilities, and MAP furniture.

MODEM

MOdulator/DEModulator

A device which modulates and demodulates signals for transmission and reception, respectively, over communication facilities. A modem allows digital signals to be sent over analog lines.

PIO

Port Input/Output

A device on the DPP CPU circuit pack that controls a communications bus between the DPP processors.

RAM

Random Access Memory

A static, read/write memory system in which information is stored in discrete, individually addressable locations such that access time is independent of location.

SIO

Serial Input/Output

Circuitry in the DPP that passes data from the DPP to external devices. The DPP employs four such circuits in its serial I/O circuit pack that provides communications paths between the DPP and DMS–100/DPP maintenance interface, the DPP EAT, and the remote polling center link (BCS25–26).

DMS-100 Family

Distributed Processing Peripheral

Card Replacement Guide

Publication number: 297-1001-536
Product release: BCS35 and up
Document release: Standard 01.03
Date: August 1996

Printed in Canada and printed in the United States of America.

northern telecom