DIGITAL SWITCHING SYSTEMS

DMS-100*

LINE MODULE DESCRIPTION

CONTENTS

FIGURES

1. INTRODUCTION

GENERAL

1.01   This practice describes the function, organization, struc-
ture, and operation of the Line Module (LM). The LM operation
section is supported by descriptions of the Line Module Control-
ler (LMC), and of the various interface and maintenance circuits
within the LM.

REASON FOR REISSUE

1.02   This practice is reissued for the following reasons: to
add a description   of the new type   NT2X19AC Line Drawer
(non-metallic, moulded structure), and to expand the description
of ringing generator operation in the "takeover" state.

PURPOSE OF A LINE MODULE

1.03   The LM is a type of Peripheral Module (PM) which is used,
in the DMS-100 (Local) and DMS-100/200 (Local/Toll) digital
switching systems, to provide an interface between analog sub-
scriber lines and the digital speech links to the switching net-
work.

1.04   The purpose of a LM with respect to the hierarchy of hard-
ware modules in the DMS-100 Family of digital switching systems
is described in Section 297-1001-100. The general characteristics
of PM, and the function and operations of the various types of
PM, are described in Section 297-1001-103.

REFERENCES

1.05   References listed as Prerequisites are essential for an
understanding of this practice. Those listed as Information con-
tain detailed information concerning other items mentioned in
this practice, but are not essential.   All references are
inserted at the appropriate place in the text.

     (a) Prerequisites

DOCUMENT
NUMBER   TITLE

297-1001-100   DMS-100 Family System Description
297-1001-103   DMS-100 Family Peripheral Module
297-1001-104   DMS-100 Family I/O Message System

(b) Information

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DOCUMENT
NUMBER          TITLE

297-1001-102    Network Description
297-1001-106    Maintenance System
297-1001-110    Maintenance and Administrative Position
297-1001-111    Power Distribution Center
297-1001-120    Equipment Labelling, Numbering, and Referencing.
297-1001-510    Output Report Manual
297-1001-515    PM Man-Machine Interface Description
297-2101-116    Line Testing
297-2101-121    Automatic Line Testing
297-2101-516    Lines Subsystem MMI Description
GS2X05          +24V Converter and Programmable Ringing Generator
GS2X17          Line Card, Type A
GS2X18          Line Card, Type B
GS0X29          Frame Supervisory Panel, LM
GS2X70          Multi-Output Power Converter
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2. FUNCTIONS OF LM

2.01 The LM performs the following functions as routine tasks assigned to it by the Central Control (CC). LM functions are performed by PP programs (execs) contained in an exective store area of the LM. Each exec is identified by a sequence number which is sent to the PP from the CC. Receipt of the sequence number causes the associated program to be executed. By performing these tasks within the LM, the PP function relieves the load on the Central Processing Unit (CPU) in the CC, enabling it to concentrate on higher-level activities.

    a. <u>With Type A or B Line Circuit Cards (see Part 6)</u>.

* Scanning of subscriber loops for off-hook (origination), on-hook, or hook flashes.

* Connection of subscribers to speech channels via the network connections.

* Generation and application of digitally-simulated call progress tones to subscribers lines (dial tone, audible ringing, busy tone), or idle code.

* Collection of dial pulses.

* Accepts DIGITONE* dialling.

* Generation and application of selected types of ringing waveforms to called-party subscribers terminated on them.

* Supervision for off-hook during ringing (ringing trip).

* Maintenance of LM hardware.

* Performance of loop and subscriber apparatus tests.

* Automatic Number Identification (ANI).

b. <u>With Type B Line Cards only (see Part 6)</u>.

   *   Generation and application of various coin   box
       control voltages.

   *   Detection of various subscriber apparatus and loop
       conditions, such as ground-start, coin present.

   *   DIGITONE* disabling for coin boxes.

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* DIGITONE is a trademark of Northern Telecom Limited

3. ORGANIZATION AND HARDWARE STRUCTURE OF LM

ORGANIZATION

3.01   Refer to Fig. 1. The digital side of the LM is connected
to the digital switching network via two, three or four 4-wire
duplicated speech links, each carrying 30, 2-way, Pulse-Code Mod-
ulated (PCM) speech channels, and two internal message channels.
On the analog side, the LM accommodates up to 640, 2-wire sub-
scriber line circuits. The number of speech links used to the
network depends on traffic requirements.   The LM has an inherent
concentration of 640 lines onto 60, 90 or 120 speech link chan-
nels, which is performed, as in other PM, by a   peripheral
processor (PP) function. In the LM, the PP function is performed
by a master processor and three subordinate processors, located
in the Line Module Controller (LMC) shelf. The LMC and the pro-
cessors are described in detail in part 5.

3.02   To improve reliability, LM are organized so as to operate
in pairs in a double-bay Line Module Equipment (LME) frame. Each
LM of the pair interfaces with its own set of 640 line circuits,
but the LMC in each LM supports the other via secondary bus
interfaces and busses (dashed lines) in the event of failure in
either LMC. Traffic and call-handling capabilities are reduced
while one LMC is out of service, because the in-service LMC is
handling up to 1280 line circuits, but both sets of 640 line cir-
cuits can continue to operate while the failed LMC is out of
service.

3.03   The line interface circuits of an LM are organized into
four shelves of Line Drawers (LD), each shelf containing five LD,
for a total of 20 (0 – 19) LD per LM. Each LD contains 32 (0 –
31) Line Circuit (LC) cards, each LC containing one interface
circuit to a subscriber's line. The LC are connected to sub-
scriber's lines via connectorized cables to the Distribution
Frame (DF). One line card position out of the 640 positions in
an LM is assigned for test purposes, and although cabled to the
(DF), the test card is not connected to a subscriber's line. The
actual capability of an LM in terms of subscriber's connections
is therefore 639 lines. The applicable test procedures are
described in 297-2101-116 and 297-2101-516. LC types are select-
able to match the requirements of the subscriber's service (see
Part 6).

3.04   The LD also contains a Ringing Multiplexer function which
distributes ringing voltages to the 32 LC on command from the
LMC, and two Bus Interface (BI) functions. One BI (designated
'Primary') multiplexes the LD to one of 20 terminal digroups on
its own LMC, while the other BI (designated 'secondary') multi-
plexes to a corresponding digroup on the mate LMC. Each LD has a
similar arrangement for the other 19 digroups.

HARDWARE STRUCTURE

3.05   LME Double-Bay Frame.   Refer to Fig. 2.   Viewed from the
front, the two LM in a double-bay LME frame are identified by -0
(left LM) and -1 (right LM). The twenty LD in each LM are num-
bered from 00 (bottom left) to 19 (top right). Since each LD con-
tains 32 LC, each of the 1280 lines associated with each LC in
either half of the double-bay frame can be uniquely identified as
follows:

```
LME           Bay
ID NO.    Left/Right  LD  LC

  ##           0      00  00 (Test LC)
  ##           0      19  31
  ##           1      00  00
  ##           1      19  31
```

Further details of the identification scheme are contained in
297-1001-120.

3.06   Each LM also contains a Frame Supervisory Panel (FSP),
which handles office battery power feeds to the LM and also con-
tains power control and alarm circuitry. The FSP is described in
GS0X29.

3.07   Structure of Line Drawers. The structure of the shelf
housing the Line Drawers is illustrated in Figs. 3 and 4. Each
LD can be withdrawn, but not removed, from the shelf (e.g.:
LD-00) for maintenance purposes and still remain operative
because all electrical connections between the LD and its shelf
are carried in flexible cables.

3.08   LD are available in two configurations, performing the
same functions, but having different hardware structures. The
two types of LD are identified by Northern Telecom (NT) product
codes, as follows:

    a. Line Drawer NT2X19AA.   This type of LD is of all-mental
        frame construction, with card sockets arranged as illus-
        trated in Fig. 3. There are 35 card positions (00-34),
        of which positions 00 to 31 are assigned to LC cards.
        Position 32 is assigned to the ringing bus multiplexer
        card, and positions 33 and 34 to the bus interface (BI)
        cards. Position 34 accommodates the primary BI to the
        "own" RLC, while position 33 is for the secondary BI to
        the mate RLC.

    b. Line Drawer NT2X19AC. The frame of this type of LD is
        moulded from non-metallic material, and has card socket
        arrangements as illustrated in Fig. 4.   There are 33 card
        positions (00-32), of which 32 positions are assigned to

LC cards. The functions of ringing bus multiplexer, pri-
mary BI, and secondary BI are performed by the Line
Drawer Interface (LDI) card. The LDI card is located in
position 32 at the front of   the LD.   In Part 4
(OPERATION), the references to the functions of primary
and secondary BI, and ringing bus MUX are equally appli-
cable when these functions are contained in the LDI card.

3.09   In both types of LD, as a provisionable option, when the
DIGITONE disabling feature is applied to an NT2X18AD line
circuit, card position 31 is assigned to an NT2X03AA + 48V Power
Converter card instead of a line circuit.   The number of line
circuits for that LD is then reduced by one. DIGITONE disable is
only required for tip-only coin control. See GS2X18 for details
of the NT2X18AD line circuit.

4. OPERATION

GENERAL

4.01   This part describes the various operations which occur
within the LM by following the paths of speech and control sig-
nals passing from the switching network to the line circuits (re-
ceive) and from the line circuits to the network (transmit). Also
described are internal activities of the processors, maintenance
circuits and ringing system. Fig. 5 illustrates the LMC func-
tions, while   Fig. 6 illustrates   the LD   functions.   The
description is applicable to both types of LD.

NETWORK INTERFACE

4.02   Up to four speech links (0 - 3) from the network (receive)
enter the LM at the Network Interface card. In this card, signals
on the speech links are converted from diphase serial format to
unipolar serial data, and the clock and frame pulses are
extracted. The contents of the message channel to the Central
Control (channel 0, speech link 0) are directed to the CC Message
Processor. This processor extracts CC messages, inserts reports
to be sent to the CC and implements the CC message protocol (ref.
Section 297-1001-104).

4.03   The Network Interface card outputs four network digroups
to the Receive Multiplexer (R - MUX). First, the 'Receive' Chan-
nel Supervision Messages (CSM), coded in bit-1 of connected
speech channels, are collected by the PP Message Processor. (Ref.
Section 297-1001-103). This processor also checks the parity
bit-0 on incoming speech channels, to ensure that odd parity is
present. The four network digroups are then applied to the inputs
of the R-MUX. From this point on, speech signals are treated
differently from control signals.

SPEECH SIGNAL PATHS

4.04   In addition to the inputs from the four network digroups,
other service and control signals are also input to the Receive
MUX. The service signals comprise standard audible tones in dig-
ital form from the tone generator (dial tone, audible ring, busy
tone), or idle code. The control signals from the Signalling
Processor are addressed to specific line cards to operate their
ringing relays.

4.05 'Receive' Path. Under control of the Connection Memory, four of the "receive" network digroup inputs are selected every channel time, and connected to four of the 20 terminal receive digroups (TRD 0 through 19). The Receive MUX has an additional maintenance digroup output which can be connected to the Transmit MUX maintenance digroup input for looparound purposes. On these terminal digroups the channels selected are carried to the Bus Interfaces (BI) in the associated Line Drawers. The remaining unselected terminal receive digroups carry no intelligence and remain in a fixed logical state until selected at the appropriate channel time. Which line circuits in the selected LD will receive these four signals is determined by the Connection Memory, acting via the Terminal Address card. The PCM speech samples pass through the BI in the line drawer (e.g. LD-0), which sends them to the appropriate line circuit, using terminal address information (TA-0 through TA-19) obtained from the Terminal Address Interface. On each line card that receives speech samples, the samples are decoded from PCM into analog form and output to the subscriber's line.

4.06 'Transmit' Path. At the same time, as the 'receive' path events, the analog speech coming from the subscriber's line to the line circuit is encoded into PCM, and output from the line circuit together with supervision status information. The outputs from the line circuits are collected by the Primary BI in each LD (e.g. LD-0) where they are switched, under control of the connection memory and terminal address interface, onto terminal transmit digroups (TTD). The selected terminal transmit digroup carries the signal to the input of the Transmit MUX.

4.07 In addition to the 20 terminal transmit digroups, a maintenance input (looparound) from the Receive MUX, and tone generator input, are also applied to the input of the Transmit MUX. Four of these input signals are connected at any channel time, under Connection Memory control, to four "transmit" network digroups.

4.08 At the CSM times (bit 1 of each speech channel), the PP Message Processor inserts "transmit" CSM into the four selected "transmit" network digroups. The CSM were loaded into the PP Message Processor by the Master Processor.

4.09 The four "transmit" network digroups then enter the Network Interface card. There, outgoing messages for the CC (reports), which the CC Message Processor outputs, are inserted into the CC message channel. Parity bits are generated and inserted, and the signals on the four network digroups are converted from unipolar serial data to diphase format. The converted network digroup signals are then output to cables carrying the speech links to the switching network.

4.10   The supervision status of active lines (those line cir-
cuits that are connected to a channel on a network digroup) is
automatically collected by the Signalling Processor through its
interface to the network digroups.

CONTROL SIGNAL PATHS

4.11   Control channel -0, digroup -0 is assigned to CC messages.
In the receive direction (from CC), the contents of this channel
are extracted in the Network Interface card and sent to the CC
Message Processor. In the transmit direction (to CC), the output
of the CC Message Processor is inserted into the same channel of
the Network Interface card. The remaining control channels in
digroups 1 through 3 carry no information to or from the Network,
and pass through the Network Interface card in both directions
without effect.

4.12   Within the LM, the control channel time slots are used to
pass control words to, and responses from, the line circuits and
ringing multiplexers. Control words are output by, and responses
are stored in, the Signalling Processor.

4.13   On "receive", 10-bit control words are output by the Sig-
naling Processor and brought to the input of the Receive MUX.
During control channel times, this input is connected (under con-
trol of the Signaling Processor) to a terminal receive digroup.
The control word then passes through the same units and paths as
the PCM speech samples. The control word is carried on a terminal
receive digroup to a Bus Interface, and then to a selected line
circuit. The address which selects the line circuit originates
in the Signaling Processor, and is converted in the Terminal
Address Interface card to an instruction (TA-0 through TA-19),
telling the Bus Interface which line circuit to select. The
addressed line circuit responds with 10 bits of data (8 bits of
response to the control word, 1 bit spare, and 1 supervision
bit). This response travels back through the Bus Interface, the
corresponding terminal transmit digroup, and is connected in the
transmit MUX to a transmit network digroup. The response, as well
as the supervision status of the line circuit accessed, are col-
lected by the Signaling Processor and stored in its memory.

INTERPROCESSOR COMMUNICATION

4.14   The LM Master Processor communicates with its subordinate processors,   and   with   the   Connection   Memory,   through mutually-accessible sections of memory located on each subordinate card. Some control signals:- reset, interrupt, and interrupt clear, are also exchanged between the Master Processor and its subordinate units. The processors, their subordinate units, the Receive MUX and Transmit MUX, and other cards are located in the Line Module Controller (LMC) shelf, which is described in part 5 of this practice.

LM MAINTENANCE

4.15   The functioning of the LM and its units is periodically monitored. If a fault is detected, it is verified, and depending on the severity of the fault, the LM may notify the Central Control and continue in service, or the CC may transfer control of its lines to the mate LMC.

4.16   The LM hardware is monitored in several ways as follows:

   a. <u>Activity Circuit.</u>   The activity circuit contains a 200 msec 'sanity' timer which is normally prevented from timing-out by periodic reset signals from the SP.   The activity line broadcasts the 'sane' status of the timer, and thus of the LMC, to the bus interface (BI) cards in the LD as long as no timeout occurs.

       If a fault of sufficient severity occurs in the LMC, the reset signal is not given by the SP, sanity timeout occurs, and an 'Inoperative' signal appears on the activity line to the LD. Locking logic in the activity circuit prevents accidental random resetting of the sanity timer by requiring a specific sequence of accesses before reset can occur. The busses from the secondary BI in each LD are connected to the corresponding terminal receive and transmit digroups in the mate LMC. Each LMC continuously monitors the activity line of its mate via its secondary BI. If an 'Inoperative' signal appears on the activity line, the mate notifies CC of the failure. The CC then issues a 'takeover' command to the mate LMC to start servicing all the lines connected to failed LM as well as its own. This command deactivates the primary BI in the LD of the failing LM and activates its secondary BI to the mate LM. Also, one of the Programmable Ringing Generators (RG-0, RG-1) in the failing LMC is placed under control of the mate Ringing Generator Interface (RGI).

Calls in progress and calls in process of set-up are dropped whenever the takeover action occurs. When the failed LM bay is serviceable, the SP applies the proper sequence of accesses to the activity circuit and the sanity timer is reset. The CC is notified of the readiness for service, via the mate activity line. Since the transfer back to normal operation (each LMC serving its own LM) also causes calls to be dropped, this action does not occur automatically. The transfer is performed manually at a low-traffic time by using the return-to-service (RTS) command. Refer to 297-1001-515 for details.

b.   The network side of the LM (i.e: Network Interface, Master Processor, CC Message Processor, and PP Message Processor is monitored by other components of the DMS-100 switching system, mainly the CC and other PM.

c.   Digital components in the line circuits of the LM are monitored within the LM, using various diagnostic paths (such as looparound) provided by the LM hardware. Diagnostic tests are supervised by the Signaling Processor.

d.   Analog units and components (such as the Programmable Ringing Generators, Ringing MUX, and the analog parts of line circuits) are monitored within the LM, by tests such as ringer continuity, stuck ringing relay test, etc.

e.   See Fig. 6 Other analog components in the line circuit (LC) cards are periodically checked via the two test access (TA) busses in the LM, which provide metallic test connections to the tip and ring leads of any one of the 640 line circuits. One of the TA busses connects to the 320 LC in LD-0 through LD-9, while the other bus connects to the 320 LC in LD-10 through LD-19. The TA busses in each LM are connected to a TA switching matrix which forms part of the line testing equipment for the DMS-100 or DMS-100/200 system. Refer to 297-2101-116 for details of the line testing equipment and procedures.

4.17   <u>Maintenance Status.</u> The maintenance status of the LM, up
to the   line circuits, is reported to the   DMS-100 maintenance
system,   which displays   the state   of   the LM circuits ('In
Service', 'System Busy', or 'Man Busy') under the 'PM' header on
the Visual Display Unit (VDU).   The LM performs various tests on
itself when instructed to do so by the CC.   If test results show
faults of sufficient severity, the CC would declare the LM 'Sys-
tem Busy', and 'takeover' by the mate LM would occur.   The
various types of LM faults which can occur are reported to the
log system, and appear as output reports. Refer to 297-1001-510
for details of output reports. See 297-1001-106 for details of
the maintenance system, and 297-1001-110 for details of the Main-
tenance and Administrative Position (MAP), of which the VDU is a
part.   The commands and responses required to obtain status
information on an LM via the MAP are described in detail in
297-1001-515.

4.18   The status of the subscriber's loop and of the line card
circuit connected to the loop is displayed under the "Lns" header
of the maintenance system, using the Line Test Position (LTP)
described in 297-2101-116.

4.19   Some of the "PM" and "Lns" reports to the maintenance sys-
tem are associated with alarm conditions ranging in severity from
"minor" to "critical". The association of LM status to alarm
conditions is described in 297-1001-515.

RINGING

4.20   Refer to Fig. 7. Ringing in the LM is generated and
applied separately from speech and control signals. In each LM,
there are two programmable generators, which can output a variety
of ringing waveforms on receipt of a suitable drive signal. When
ringing is to be applied to a subscriber's loop, the Signaling
Processor loads the appropriate code for the desired ringing
waveform into the Ringing Generator Interface (RGI) card. This
card drives the Programmable Ringing Generators to output the
selected ringing waveform. The Ringing Multiplexer in the Line
Drawer where the line circuit to the called subscriber is
located, is instructed to connect the drawer's internal ringing
bus to the output of one of the Programmable Ringing Generators.
The ringing relay on the line circuit that serves the called sub-
scriber is then operated via the bi-directional bus from the BI.
Commands that control the ringing relays on the line circuits and
ringing multiplexers originate in the Master Processor and are
output by the Signaling Processor, via the Receive MUX and Bus
Interface.

4.21   The type of ringing scheme which is output by the RG is
controlled by entries in the Ring Table in the customer data
schema (see 297-2101-451, section 1/115).   Also, a suitable type

of RGI card is selected to match the ringing scheme, and is installed in the LMC. The following RGI card types are available:

RGI Type   Ringing Scheme

NT2X27AA   20 Hz Bell.
NT2X27AB   Decimonic MF.
NT2X27AC   Harmonic MF.
NT2X27AD   Synchronomic 16 Hz.
NT2X27AE   Synchronomic MF.

4.22   At the end of the ringing phase (when the called subscriber goes off-hook), the ringing relay is released by another command. The programmable ringing generator can now be be re-programmed to output another type of waveform (e.g. coin control voltage) if required. Since the ringing load is shared between the two Programmable Ringing Generators, on the next command the ringing multiplexer may be instructed to connect to the output of the other generator.

4.23   Refer to Fig 8. State 1 shows the normal operation of ringing circuits, as just described, with the LMC of each bay controlling its own RGI and RG, via its own SP. The RGI card in each bay contains two RGI circuits (RGI-0, RGI-1), which provide interfaces between RG-0 and RG-1 respectively.

4.24   States 2 and 3 show a situation where, due to a fault in Bay 1, the LMC in Bay-0 has received a takeover command from the CC. RG-0 and RG-1 in Bay-1 are still operable, because they contain their own power supplies, but control signals via the SP and RGI card in Bay-1 are not available. The SP in Bay-0 selects at random, one or the other of its RGI circuits (RGI-0 or RGI-1) to control one of the RG in Bay 1.

4.25   State 2 shows the condition where Bay-0 is using its RGI-1 to control RG-1 in Bay-1, and RGI-0 to control its own RG-0. State 3 shows the opposite condition with Bay-0 using RGI-0 to control RG-0 in Bay-1, and RGI-1 to control its own RG-1.

4.26   A similar pair of situations occurs oppositely if Bay-1 takes over Bay-0. In all takeover situations, only two out of the four RG in the two RLM bays are operable as long as the takeover is in effect. All the possible RG and RGI states are tabulated and described in detail from the maintenance point of view in 297-1001-515.

4.27   Each programmable ringing generator card also contains a sensor and protection circuits which send status signals back to the Ringing Generator Interface card. The status signals are

available to the Signaling Processor for action or information,
as necessary. The sensor circuit is used for the ANI test, the
coin-present test, and the loop-to-ground resistance test. The
protection circuits monitor current and voltage on the ringing
busses, and will turn the ringing generator off if either becomes
excessive. This condition is designated as the 'shutback' mode
of the ringing generator, and causes a fault report and minor
alarm to appear under the 'PM' header of the MAP (see Maintenance
Status).

5. LINE MODULE CONTROLLER (LMC) DESCRIPTION

LMC SHELF LAYOUT

5.01   Refer to Fig. 9. The following LM functions described in
OPERATION are located in the LMC shelf as plug-in printed circuit
cards. The hardware identities of the cards closely parallel
their functions, except that some cards contain additional cir-
cuits and perform functions not yet mentioned. From left to right
(front view) the LMC shelf card assignments are:

 a. +24V Converter and Ringing Generator (NT2X05AA) (qty 2).
      In addition to performing the functions of Programmable
      Ringing Generators -0 and -1, these cards each contain a
      power converter section. The power converter circuits
      receive the office battery input from the Power Distrib-
      ution Center (PDC) and convert it to +24V for relays and
      other circuits in the LM. Power Distribution to the LM
      from the PDC is described in 297-1001-111. The ringing
      generator section is capable of any output in the range
      of 0 to [1] 240V, dc to 60 Hz, as directed by commands from
      the signaling processor via the ringing generator inter-
      face. Details of this card are contained in GS2X05.

 b. Ringing Generator Interface (NT2X27AA-AE) Function is as
      described in OPERATION.

 c. Signaling Processor (NT2X24AB) Function is as described
      in OPERATION and in LMC PROCESSOR HIERARCHY.

 d. Signaling Processor Interface (NT2X25AB) Provides an
      interface between the Signaling Processor, the Receive
      and Transmit MUX and the Connection Memory. Handles the
      insertion and extraction of signalling information into
      and from the terminal digroups.

 e. Extension Memory (Optional). Provides extra memory capa-
      bility for the Master Processor if required.

 f. Master Processor (NT2X26AA). Function is as described in
      OPERATION and in LMC PROCESSOR HIERARCHY.

 g. CC Message Processor(NT2X33AA), PP Message Processor
      (NT2X34AA). See OPERATION and LMC PROCESSOR HIERARCHY.

 h. Connection Memory and Transmit MUX (NT2X22AA). These two
      functions are contained in one hardware unit. Functions
      are as described in OPERATION.

 i. Receive MUX (NT2X23AA). The Receive MUX (R-MUX) func-
      tions as described in OPERATION.

j. <u>Network Interface (NT2X36AA).</u> See OPERATION.

k. <u>Terminal Address Interface and Tone Generator (NT2X21AA)</u>.
Combined on one hardware unit, but operate independently.
The Terminal Address Interface functions as described in
OPERATION. The Tone Generator section contains the audi-
ble tones encoded digitally in a ROM. Tones are applied
as required via the R-MUX, under control of the Signaling
Processor.

l. <u>Power Converter (NT2X70AA).</u> Provides multi-purpose DC
voltages (^{1}12V, ^{1}5V) from an office battery feed from the
PDC (See 297-1001-111). Refer to GS2X70 for details of
this card.

LMC PROCESSOR HIERARCHY

5.02   Refer to Fig.10.   The four processors in the LMC operate
as a hierarchy with the Master Processor being at the highest
level,   and   the   three   other   processors operating   under
instructions from the Master Processor. The three subordinate
processors each issue subsidiary instructions to control those
functions within their own fields of activity.

MASTER PROCESSOR

5.03   The Master Processor is the only processor in the LMC
which communicates directly with the CC. This processor contains
the instruction set composed of "execs." which implement the task
assigned to the LM by   the CC software. (See part 1. PURPOSE).
The Master Processor carries out, under instructions from the CC,
all high level tasks. It executes routines that control the proc-
essing and supervision of a call. It sends instructions to
subordinate units to control hardware, and it receives reports
about messages received or events observed in the hardware. It
controls maintenance and traffic measurement activities.

5.04   The Master Processor is a microprocessor unit with 48
Kbytes of dynamic Random Access Memory (RAM) and 2 Kbytes of
Erasable Programmable Read-Only Memory (EPROM). Its memory can be
expanded, if required, by adding the Memory Extension card con-
taining 64 kbytes of memory capability.

5.05   Directly subordinate to the Master Processor are the CC
Message Processor (CCMP), the PP Message Processor (PPMP), the
Signalling Processor (SP) and the Connection Memory (CM).

CC MESSAGE PROCESSOR (CCMP)

5.06   The CCMP is the interface between the Master Processor and
the message channel to the CC. The CCMP contains a microprocessor
unit with up to 2 kbyte of RAM and 4 kbytes of EPROM. Currently,
1 kbyte of RAM and 2 kybtes of EPROM are unused and are avail-
able for expansion. Communication between the Master Processor
and the CCMP occurs via a mutually-accessible 1 kbyte block of
the RAM. The CCMP can interrupt the Master Processor, or reset
it, on receiving the appropriate message from the CC.

5.07   Communication with the CC takes place over the message
channel (channel -0, network link numbered 0 in the LM). The CCMP
receives messages sent to the LM from the CC over this channel,
and transmits to CC messages that the Master Processor generates.
(The term "report" is used for a message going to the CC). The
exchange of messages is governed by the protocol described in
297-1001-104 (I/O Message System).

5.08   The CCMP is reset every frame (125 usec) and scans the
byte received on the message channel. If a message is present, it
is copied into the memory   area accessible to the Master
Processor. If a report is to be sent to the CC, the next byte of
the report is copied into the network interface output register
for the message channel. The contents of the output register are
then transmitted on the message channel in the next frame.

5.09   If no messages are to be sent or received, the CCMP
exchanges IDLE codes. If messages are present, the "May-I-Send"
(MIS), "Send" sequence is used, also the "PACK" or "NACK" activ-
ities subsequent to message exchange, as specified by the message
protocol.

PP MESSAGE PROCESSOR (PPMP)

5.10   The PPMP does not communicate with the CC, but with
hierarchically equal units (i.e: the PP in other peripheral mod-
ules). The PPMP communicates with the Master Processor through a
1.5 kbyte section of RAM, an interrupt line, and a first-in,
first-out (FIFO) memory which stores causes of interrupts.

5.11   PP to PP messages take place over bit 1 of the 10-bit PCM format, on connected speech channels only. A complete message, referred to as the Channel Supervision Message (CSM), consists of 40 bits transmitted at a rate of 1bit per frame (5 msec duration). The first 24 bits are used for synchronization, and the remaining 16 bits carry PP to PP mesages. The meaning of individual parts of the CSM is explained in Section 297-1001-103.

5.12   The PPMP supervises activity on the CSM in the speech channels. On the transmit path the PPMP repeatedly transmits CSM whose contents are determined by the Master Processor. On the receive path, the PPMP collects CSM from connected PP in other PM and compares the contents of the CSM to patterns given by the Master Processor. When enabled, the PPMP interrupts the Master Processor to indicate a match or mismatch, storing the cause of the interrupt in the FIFO memory. The received CSM are stored in the network interface memory, where they can be examined by the Master Processor.

5.13   Another function of the PPMP is the checking of parity on speech channels. Bit-0 of the 10-bit PCM format is the parity bit. The PPMP checks each channel for odd parity, and when ena-bled, interrupts the Master Processor if a parity violation is detected. The cause of interrupt is stored in the FIFO memory.

SIGNALING PROCESSOR (SP)

5.14   The SP is the interface between the Master Processor and the control circuits in the line side of the LM. Through the SP, the line circuits, ringing multiplexers, programmable ringing generators and the activity circuit are controlled, and their status is reported.

5.15   The SP consists of a microprocessor with 2 kbytes of EPROM, 5 kbytes of private RAM and 1 kbyte of RAM as an interface to the Master Processor. The SP can interrupt the Master Process-or and can be reset by it. To control the subordinate hardware, the SP operates in three functional areas:

    a. Line circuit control. Via the SP Interface and Bus
        Interface cards.

    b. Programmable Ringing Generator Control. Via the Ringing
        Generator Interface.

    c. Activity Control. Via the activity circuit.

6. LINE CIRCUIT CARDS

GENERAL

6.01   The Line Circuit (LC) card is the final interface between
the subscriber's line and the LM digital circuitry. The location
of the LC in the Line Drawer is illustrated in Figs. 3, or 4, and
the functional relationship of the LC to the LM is illustrated in
Fig. 6.

6.02   Through the LC, office battery and control voltages, ring-
ing and tones are applied to the loop; loop status is supervised;
outgoing speech samples are converted to analog waveforms (and
vice versa) and test access is realized. Loop loss control is
exercised by remote selection of loss pads in the digital/analog
(receive) speech path (range 0 to 7dB in 1dB steps). Loop bal-
ance is achieved by selecting an appropriate balance network to
match the cable type.

LINE CIRCUIT TYPES

6.03   Two types of line circuits are available for use in the
LD. Card types are interchangeable and can be mixed in any LD to
meet the office provisioning requirements. The most typical LC is
the Type A line circuit, which is covered in simplified form in
the following description. The Type B line circuit operates simi-
larly, but has additional circuitry to enable it to operate with
more   sophisticated   subscriber   equipment,   such   as
ground-start/loop-start coin-operated apparatus and PABX. Refer
to GS2X17 for details of the features and characteristics of the
Type A line circuit, and to GS2X18 for the Type B line circuit.

TYPICAL LINE CIRCUIT

6.04   Refer to Fig. 11. The subscriber's loop is connected to
the Tip and Ring terminals of the line circuit analog side. The
digital side of the line circuit interfaces with the Line Drawer
bi-directional bus to the bus interface cards. The other Line
Drawer connections are to office battery and ringing bus MUX.
The metallic test access points, for bridged monitor or test-out,
are connected to the TA busses as described in part 4. Bridged
monitor enables test access to the VF transformer and subscriber
loop leads. Test-out enables the subscriber's loop only to be
accessed.

6.05   The LM communicates with its line circuits over the
bi-directional bus. The line circuit access chip is normally in
the "receive" state. Data is sent to a line circuit via the bus
interface in the associated line drawer. The data consists of 10
bits, of which the first bit is 0 and serves as the "start" bit.
The second bit is the "mode" bit, which indicates whether the
next 8 bits are to be interpreted as PCM speech (mode = 0) or as
control (mode = 1). In speech mode, these 8 data bits are
directed by the access chip to the codec and filter for transfor-
mation into analog speech signals. In the control mode, the 8
bits are divided into two groups of four bits. The most signif-
icant four bits are an address which selects the group of
commands, and the least significant four bits select one command
out of the group specified in the address.

6.06   The control codes are latched into registers in the access
chip, and output command signals to components within the LC. In
the following examples of typical control codes, the 8-bit code
is expressed as a two-digit hexadecimal (HEX) number, where the
left digit represents the most significant four bits (group
address), and the right digit the least significant four bits
(command selection).

HEX. CODE

ADDRESS	COMMAND	GROUP	OPERATION
2	6 ⌐	Receive speech	⌐ Select 0 dB loss
2	E │	path, loop loss	Select 1 dB loss
2	2 │	control.	Select 2 dB loss
2	A >	Selection of loss	< Select 3 dB loss
2	4 │	pads, range 0 to	Select 4 dB loss
2	C │	7 dB in 1 dB	Select 5 dB loss
2	0 │	steps.	Select 6 dB loss
2	8 ⌐		⌐ Select 7 dB loss
7	8	BALANCE NETWORK	Select balance network for loaded subscriber loop. When code 78 is not present the non-loaded balance network is selected.
3	8	RELAY CONTROL	Arm ring relay.
3	4	RELAY CONTROL	Operate test access relay for bridged monitor connection.
3	2	RELAY CONTROL	Operate cut-off relay to disconnect subscriber's loop.

6.07   Control codes such as the above are generated automat-
ically by the signaling processor whenever the appropriate mes-
sage is received from the CC.   The above control codes are
typical examples only, and are not a complete list. Actual codes
may differ from those listed.

6.08   When the 10th bit has been received, the bi-directional
bus goes to the "transmit" state. The line circuit responds by an
output of 10 bits of data from the access chip registers. If the
incoming data was PCM speech, the first 8 bits transmitted are
also a PCM speech sample. If the incoming data was a control
code, the first 8 bits transmitted are a response from the access
chip data register. The 9th bit is not used and the 10th bit
indicates the status (off-hook, on-hook) of the subscriber's line
connected to the line circuit.

7. ABBREVIATIONS

ANI   Automatic Number Identification
BI   Bus Interface
CC   Central Control
CM   Connection Memory
CSM   Channel Supervision Message
CCMP   CC Message Processor
CPU   Central Processing Unit
DMS   Digital Multiplex Switching
DF   Distribution Frame
EPROM   Erasable Programmable Read-Only Memory
FIFO   First In First Out
FSP   Frame Supervisory Panel
HEX   Hexadecimal
I/O   Input/Output
LC   Line Circuit
LD   Line Drawer
LM   Line Module (bay)
LME   Line Module Equipment (frame)
LMC   Line Module Controller
LTP   Line Test Position
MAP   Maintenance and Administrative Position
MIS   May-I-Send
MP   Master Processor
MMI   Man-Machine Interface
MUX   Multiplexer
PCM   Pulse Code Modulation
PDC   Power Distribution Center
RAM   Random Access Memory
PM   Peripheral Module
PP   Peripheral Processor
PPMP   PP Message Processor
R-MUX   Receive Multiplexer
RTS   Return To Service
SP   Signalling Processor
TA   Test Access
TA-0   Terminal Address-0
TA-19   Terminal Address-19
T-MUX   Transmit Multiplexer
TRD   Terminal Receive Digroup
TTD   Terminal Transmit Digroup
VDU   Visual Display Unit
VF   Voice Frequency