297-8991-511

DMS-100

XA-Core

Maintenance Guide

CSP15 Standard 05.01 April 2001

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DMS-100

XA-Core

Maintenance Guide

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- In the chapters titled “Introduction” and “Cards and packlets”, added information about the PE configurations supported in CSP15: 2+1, 3+1, and 5+1.

March 2001

Standard Release 04.04

- Corrections to minor errors in Release 04.03.

March 2001

Standard Release 04.03

- In the chapter titled “Capacity monitoring tools in an XA-Core”, added notes stating that when multiple PEs are out of service, the values displayed in certain fields on the Capacity MAP screen are incorrect and invalid.

October 2000

Standard Release 04.02

- Content maintenance and revisions

August 2000

Standard Release 04.01

- Added 3+1 configuration for PE cards, and the capability to provision up to 10 SM cards.

- Replaced “How to problem solve a store allocation error of a MemLim alarm” with the chapter titled “How to problem solve a MemLim alarm”.

- Added the Ethernet interface packlet and ETHR MAP display and commands required for trials of Succession Network IP solutions. Ethernet packlet is not scheduled for general availability until CSP15.

- Added the chapter titled “Capacity monitoring tools in an XA-Core”.

May 2000

Standard Release 03.02

- Added AMDI MAP level commands

March 2000

Standard release 03.01

- Updated processor element (PE) and shared memory configurations (SM)

November 1999

Standard release 02.02

- Add NTLX02CA processor element.

August 1999

Standard release 02.01

- Updates and format cleanup.

June 1999

Standard release 01.01

- First release of this document.

Contents

Maintenance Guide

About this document

This document helps maintenance personnel find and clear faults in the XA-Core. This document applies to the DMS SuperNode and the DMS SuperNode SE switches.

How to check the version and issue of this document

This document uses numbers, for example 01.01, to indicate the version and issue of the document.

The first two digits indicate the version. The version number increases with each update to support a new software release. For example, the first release of a document is 01.01. In the next software release cycle, the first release of the same document is 02.01.

The second two digits indicate the issue. The issue number increases with each revision when the document is released again in the same software release cycle. For example, the second release of a document in the same software release cycle is 01.02.

Determine which version of this document applies to the software you have and determine the order of this document.

References in this document

This document refers to the following documents:

- *Switch Performance Monitoring System Application Guide*, 297-1001-330
- *Digital Switching Systems DMS-100 Family Maintenance Managers Morning Report*, 297-1001-535
- *DMS Family Commands Reference Manual*, 297-1001-822
- *XA-Core Maintenance Manual*, 297-8991-510
- *XA-Core Reference Manual*, 297-8991-810

1 Introduction

This chapter provides a summary of the DMS SuperNode and SuperNode SE switches and the architecture of the eXtended Architecture Core (XA-Core).

This chapter includes the following sections:

- System architecture of DMS SuperNode and SuperNode SE switches
- Cabinet layouts of DMS SuperNode and SuperNode SE switches
- XA-Core architecture in DMS SuperNode and SuperNode SE switches
- XA-Core configurations in DMS SuperNode and SuperNode SE switches

System architecture of DMS SuperNode and SuperNode SE switches

The DMS SuperNode and SuperNode SE switches share the following common components:

- DMS-core
- DMS-bus
- DMS-link

The DMS-core provides computing and data storage resources. The DMS-core can have one of two types. One type of the DMS-core is a computing module (CM) and the second type is an XA-Core. This document describes the XA-Core type of DMS-core and not the CM type. The XA-Core type of DMS-core has three main modules of shared memory (SM), processing element (PE), and input/output processor (IOP).

The DMS-bus processes and sends messages to nodes in the SuperNode and SuperNode SE switches. The DMS-bus has two load-sharing message switches (MS).

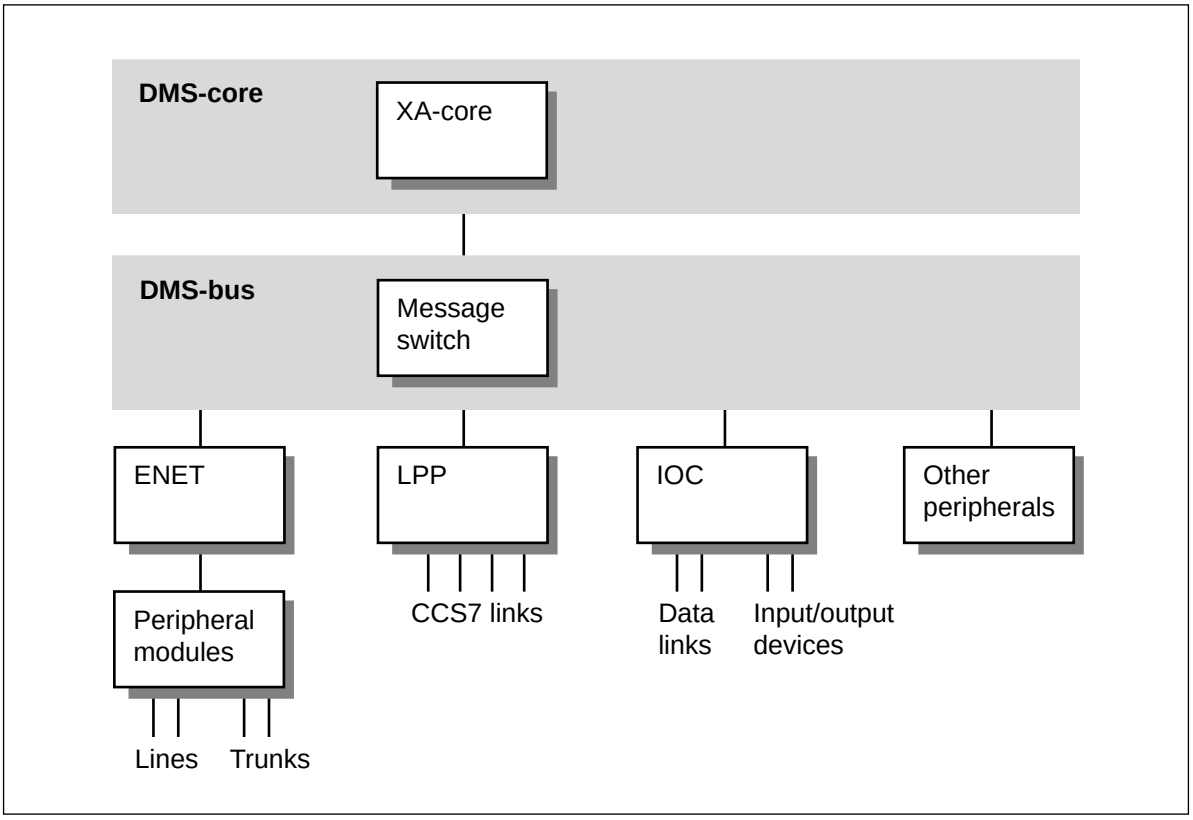
The DMS-link allows the DMS-core and DMS-bus to communicate in the SuperNode and SuperNode SE switches. The DMS-link is the software structure which does signaling standards for the public network.

Other modules the DMS SuperNode and SuperNode SE switches can have are:

- Enhanced network (ENET)
- Link peripheral processor (LPP)
- Input/output controller (IOC)
- CCS7 link interface unit (LIU7)
- Peripheral modules (PM)
- Other peripherals

Figure 1-1 on page 1-2 shows the system architecture of the XA-Core in a DMS SuperNode switch.

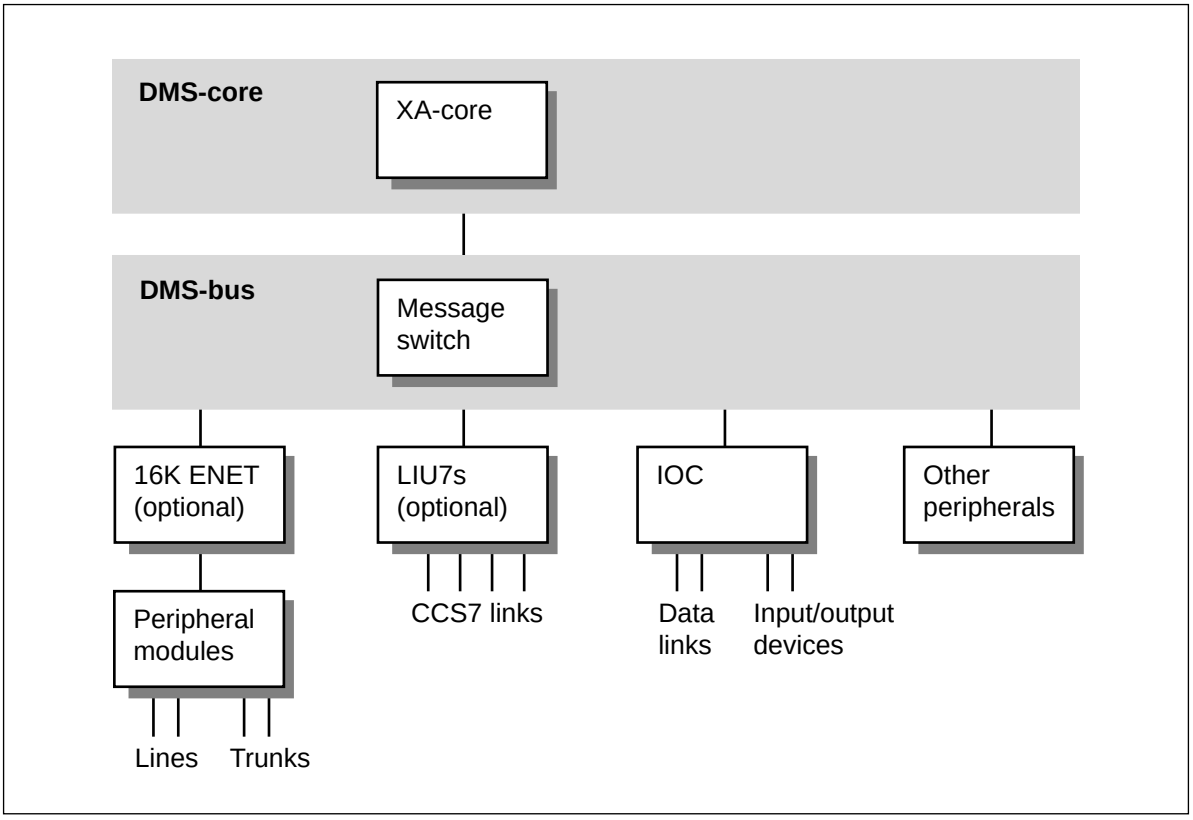
Figure 1-1 XA-Core in the architecture of the DMS SuperNode switch



The DMS SuperNode SE can also have a 16K ENET and LIU7s. The 16K ENET provides voice and data signal switching for nodes in the DMS SuperNode SE switch. The 16K ENET also provides message routes to the MS. The LIU7 provides CCS7 message processing.

Figure 1-2 on page 1-3 shows the system architecture of the XA-Core in a DMS SuperNode SE switch.

Figure 1-2 XA-Core in the architecture of the DMS SuperNode SE switch



Cabinet layouts of DMS SuperNode and SuperNode SE switches

The XA-Core hardware is on an XA-Core shelf in a cabinet. The following list shows three types of cabinets that can have an XA-Core shelf.

- NTLX01AA dual plane combined XA-Core cabinet (DPCX)
- NTLX01BA SuperNode XA-Core cabinet (SNXA)
- NTLX01CA extension XA-Core cabinet (EXTX)

Figure 1-3 on page 1-4 shows the NTLX01AA DPCX cabinet layout for XA-Core in a DMS SuperNode switch.

Figure 1-3 XA-Core in the SuperNode cabinet layout

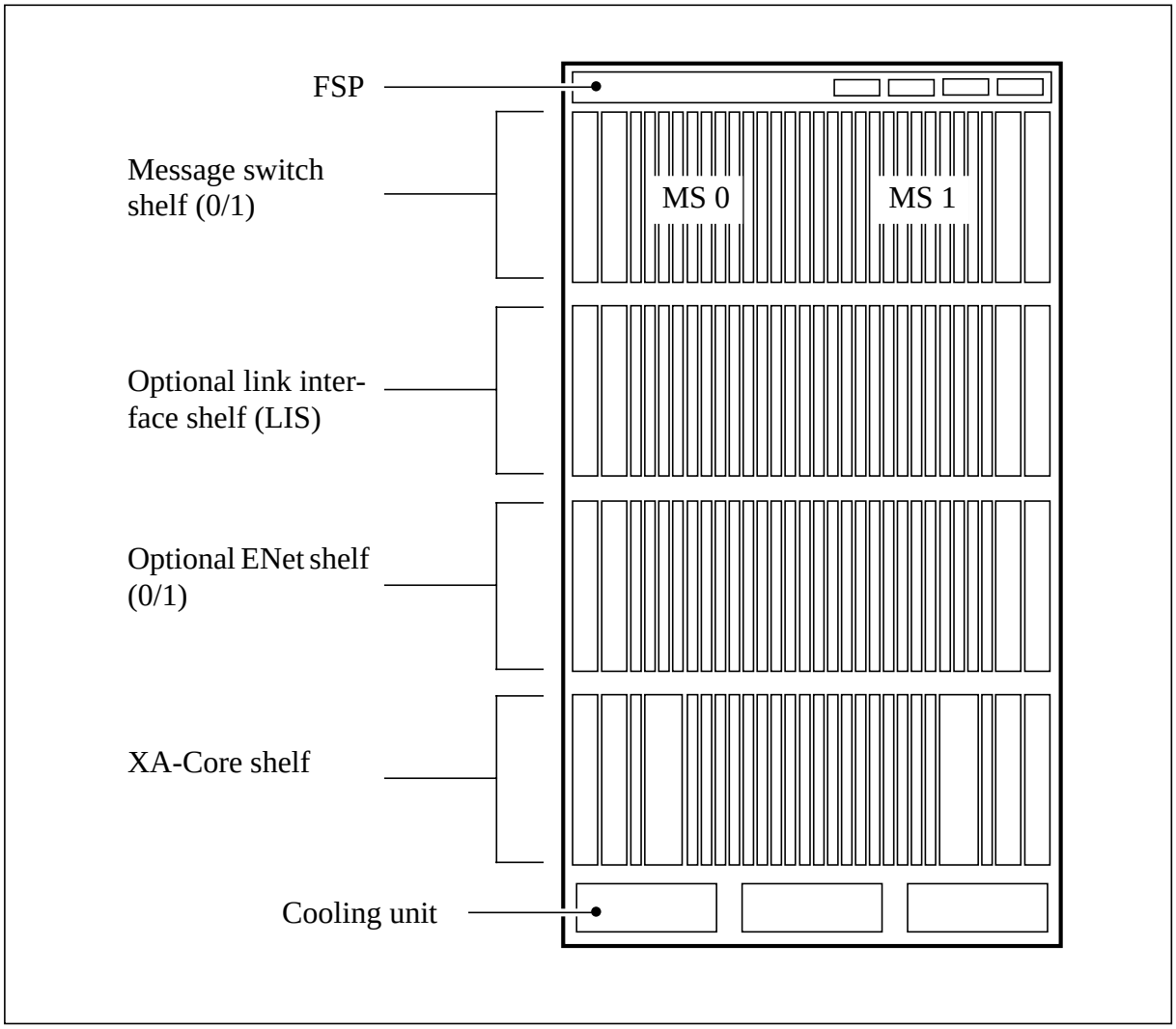


Figure 1-4 on page 1-5 shows the NTLX01BA SNXA cabinet layout for XA-Core for XA-Core in a DMS SuperNode SE switch.

Figure 1-4 XA-Core in the SuperNode SE cabinet layout

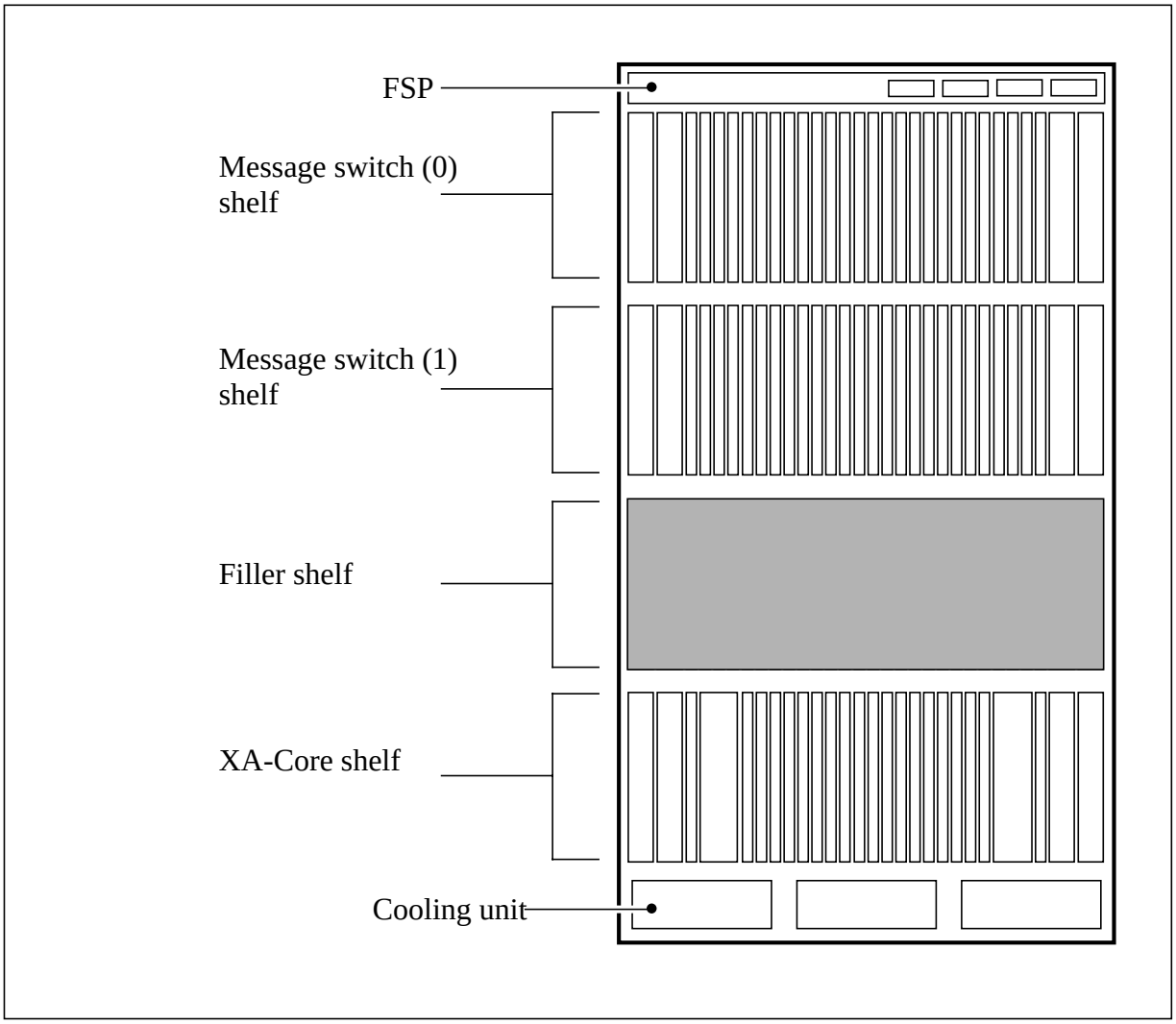
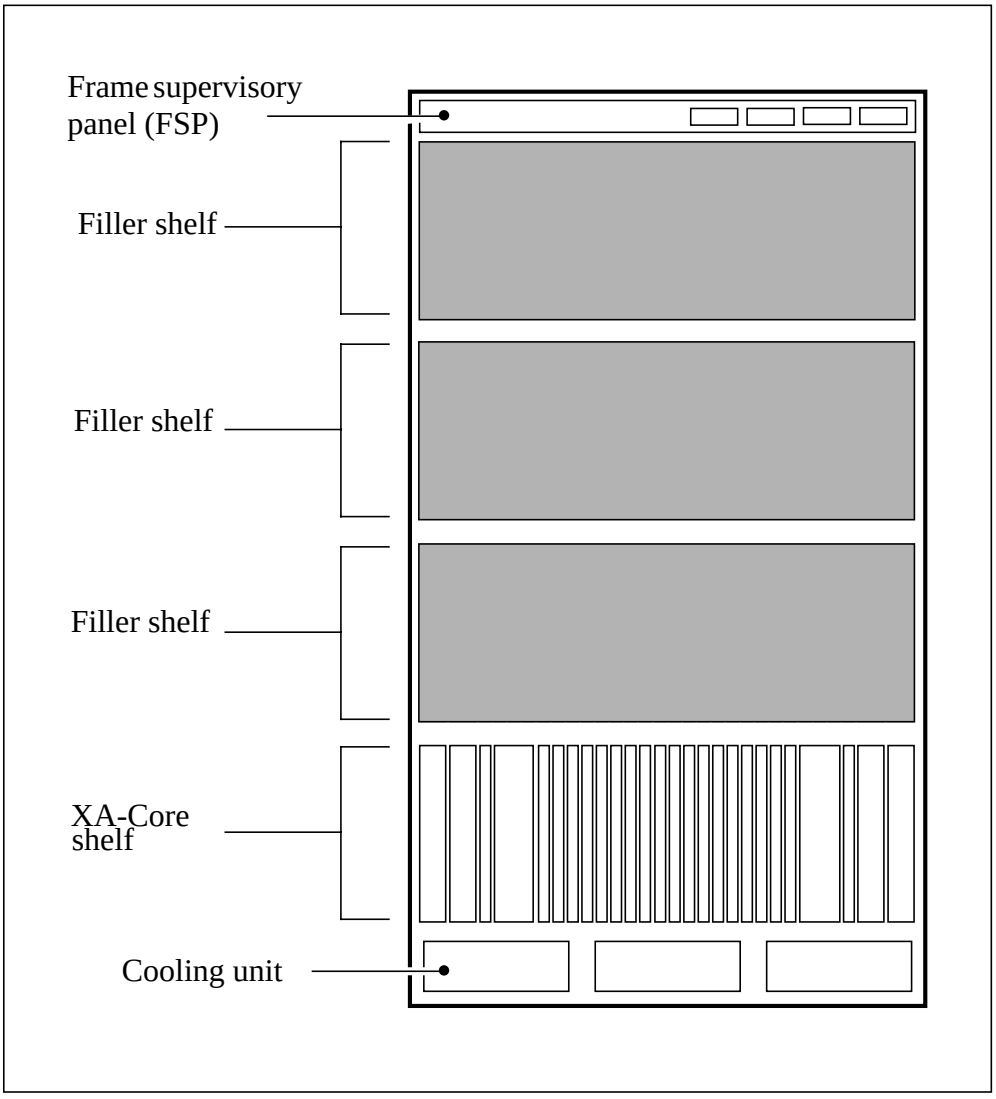


Figure 1-5 on page 1-6 shows the NTLX01CA EXTX extension cabinet layout for XA-Core in a DMS SuperNode and DMS SuperNode SE switch.

Figure 1-5 XA-Core in the extension cabinet layout



XA-Core architecture in DMS SuperNode and SuperNode SE switches

The XA-Core architecture is the same for SuperNode and SuperNode SE switches. The XA-Core contains the following components:

- processor and memory
- interfaces
- reset control
- bus termination
- time of day (TOD) clocks
- point-of-use power supply (PUPS)

Processor and memory

The processor and memory controls call processing, configuration, and maintenance of the switch. The processor and memory include the following circuit packs.

- processor element (PE) circuit packs (NTLX02)
- input/output processor (IOP) circuit packs (NTLX03)
- shared memory (SM) circuit packs (NTLX14)

File system

The XA-Core has a logical file system (LFS) and a fault tolerant file system (FTFS). The LFS does not depend on the device type. An LFS-to-FTFS interface gives the LFS access to the FTFS volumes. The interface transfers LFS operation requests into FTFS operation requests. The FTFS provides the following to XA-Core.

- volume directories and the capability for directories in a hierarchy structure with path names
- a configuration for disk cache
- extent-based system for disk files
- application registration for file system event notification

In-service spares

All installed spares in XA-Core are in an in-service mode. XA-Core automatically places the spares into replacement use for other equipment that goes out of service. Replacement of equipment that goes out of service requires no manual maintenance action. XA-Core has hot insertion and removal of circuit packs and packlets.

Reset control

The reset control provides a utility for a local or remote reset of the XA-Core. The reset control displays the status of total XA-Core processing. The reset control also has command interpreter (CI) capability but no display of menu-type levels of the maintenance and administration position (MAP). The reset terminal interface (RTIF) is an interface to a display terminal for reset control. The RTIF can be a local or a remote terminal. A remote RTIF terminal can connect through a modem to the XA-Core. The RTIF interface protocol for the XA-Core are as follows.

- RS-232 (local or remote)
- RS-422 (remote)
- current loop (local)

The RS-232/RS-422 serial interface packlet (NTLX08) contains the reset capability in an XA-Core shelf. An XA-Core shelf has two NTLX08 packlets for reset control (one packlet is a backup for the other packlet).

XA-Core status information of the reset control display indicates the following:

- heartbeat on operation of the switch
- status during a boot or reset
- information on RTIF hardware
- results of diagnostics and tests when power applied
- node name of RTIF

Bus termination

The single slot circuit pack filler (NTLX20BA) is the terminator circuit pack for the XA-Core midplane. The terminator circuit pack is in XA-Core slots of the PE, SM, and IOP that are not in use.

Time of day clocks

The time of day (TOD) clocks provide link synchronization of the XA-Core to the clock subsystem of the MS. The two CMIC packlets (NTLX05) of the XA-Core contain the TOD clocks. A TOD update message from the MS maintains TOD accuracy.

Power supply

The power supply provides power for the XA-Core shelf. The power distribution center (PDC) provides power on three power feeds for each of the A and B battery power feeds. Two shelf interface module (SIM) circuit packs (NTLX12) provide power interconnection for A and B battery power feeds. Each SIM circuit pack provides three power feeds for either the A or B battery for a DMS SuperNode switch. A DMS SuperNode SE switch has two power feeds connected for each of the A and B battery power feeds. DMS SuperNode SE has no use for the third power feeds of both the A and B battery power feeds. The power feeds connect to the point-of-use power supplies (PUPS) on the hardware modules. A dc to dc converter in the PUPS supplies local power to the hardware modules.

Interfaces

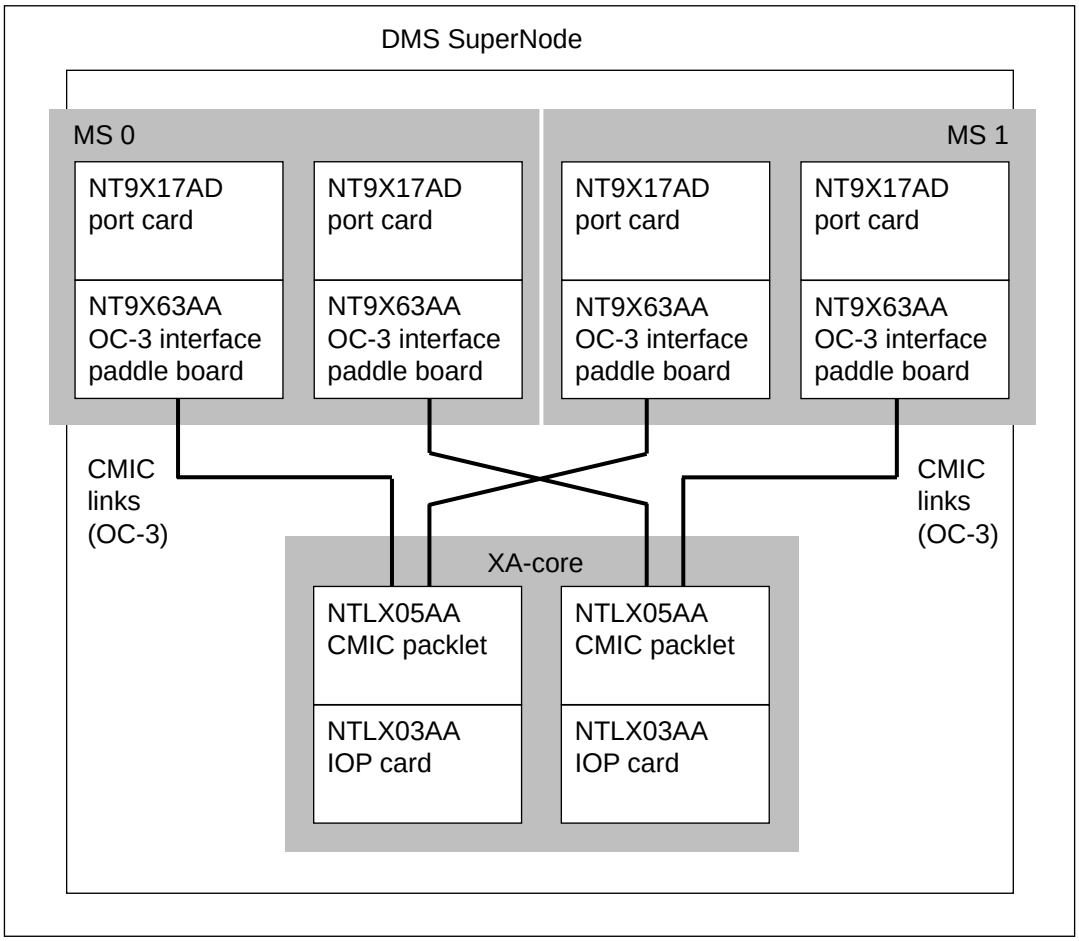
The interfaces allow XA-Core to communicate with other nodes in the switch and with storage devices. The interfaces with other nodes in the switch are through the MS. Communication between the XA-Core and the MS is over core-MS interconnect (CMIC) links. CMIC links use the octal carrier level 3 (OC-3) rate. The interfaces with storage devices support the storage of billing records, logs, load images, and other file system records. A direct memory access (DMA) device connects the XA-Core directly with the MS and storage

devices. The interfaces include the following circuit pack, packlets, and paddle board.

- OC-3 two-port interface packlet (NTLX05) for CMIC links
- disk drive packlet (NTLX06)
- digital audio tape (DAT) tape drive packlet (NTLX07)
- RS-232/RS-422 serial interface packlet (NTLX08) for RTIF terminals

Figure 1-6 on page 1-9 shows the CMIC links for DMS SuperNode.

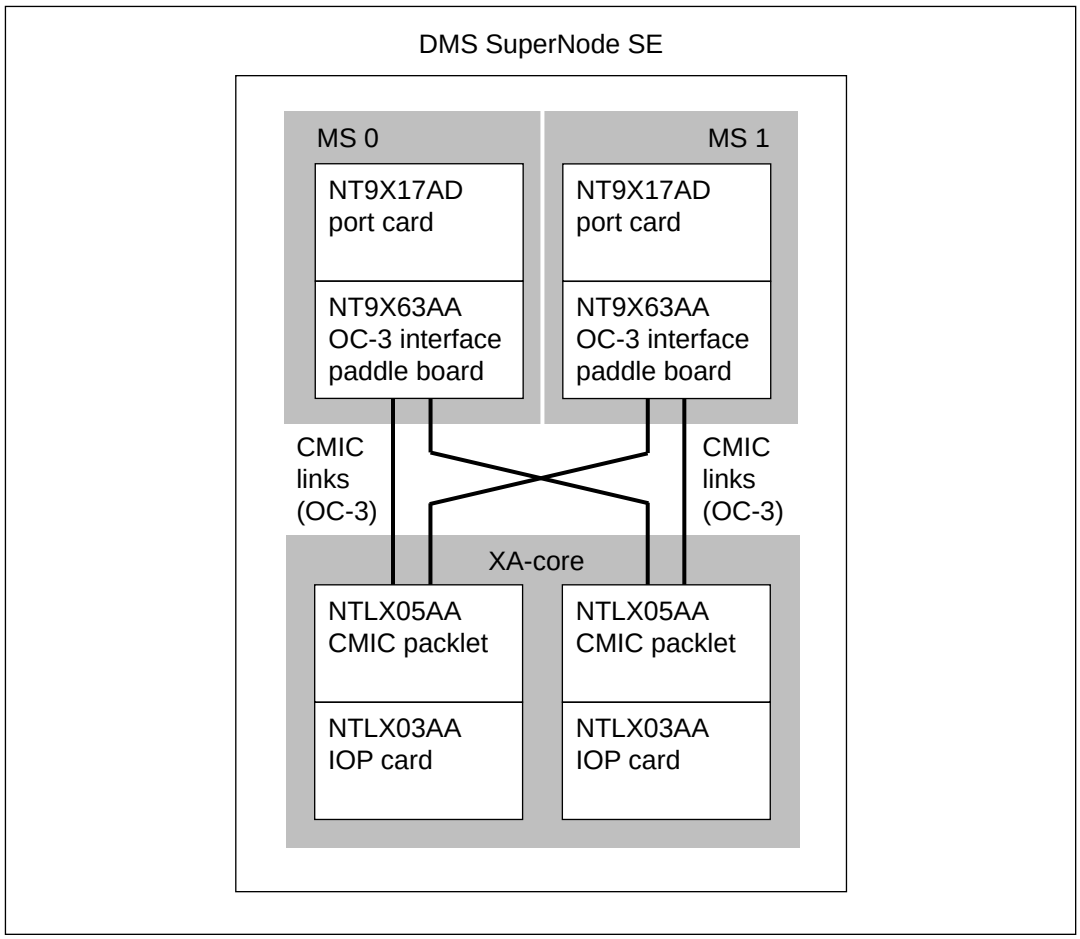
Figure 1-6 XA-Core to MS port connections for DMS SuperNode



Note: This figure provides an example of the card and packlet PEC codes that can be equipped. Other PECs with different PEC suffixes have been developed but are not shown here.

Figure 1-7 on page 1-10 shows the CMIC links for DMS SuperNode SE.

Figure 1-7 XA-Core to MS port connections for DMS SuperNode SE



Note: This figure provides an example of the card and packlet PEC codes that can be equipped. Other PECs with different PEC suffixes have been developed but are not shown here.

MS support for XA-Core

Octal carrier level 3 (OC-3) links provide XA-Core communication with the DMS message switch (MS). The Core-MS interconnect (CMIC) packlets (NTLX05) terminate the OC-3 links on the XA-Core. The MS needs OC-3 interface paddle boards (NT9X63) to terminate the CMIC links. The MS also needs central processing unit (CPU) circuit packs (NT9X13) and port circuit packs (NT9X17) that support XA-Core.

Table 1-1 on page 1-11 lists the circuit packs and paddle boards that the MS needs to support the XA-Core. The MS needs the listed circuit packs and paddle boards in an XA-Core configuration that is different from the computing module (CM) configuration. The MS needs the listed circuit packs

and paddle boards plus other hardware in an MS shelf of the SuperNode and SuperNode SE cabinets.

Table 1-1 MS circuit packs and paddle boards to support XA-Core

PEC	Version	Name	Description
NT9X13	DG	CPU circuit pack	16-MHz/16-Mbyte CPU in a first-time installation of a SuperNode cabinet or to upgrade from an NT9X13DD CPU circuit pack in a SuperNode cabinet
NT9X13	NB	CPU circuit pack	16-MHz/16-Mbyte CPU in a first-time installation of a SuperNode SE cabinet or to upgrade from an NT9X13NA CPU in a SuperNode SE cabinet
NT9X17	AD	Four-port circuit pack	Four-port circuit pack
NT9X63	AA/AB	OC-3 interface paddle board	OC-3 interface paddle board

XA-Core configurations in DMS SuperNode and SuperNode SE switches

XA-Core has circuit packs and packlets located on an XA-Core shelf. An input/output (IOP) circuit pack of one or two slot size contains the packlets.

XA-Core circuit packs and packlets

Table 1-2 on page 1-11 lists the circuit packs and packlets of the XA-Core shelf. The table indicates the product engineering code (PEC) of each type of circuit packs and packlet.

Table 1-2 XA-Core circuit packs and packlets (Sheet 1 of 2)

PEC	Version	Name	Description
NTLX02	AA/ CA	Processor element (PE) circuit pack	256-Mbytes processor element (PE)
NTLX03	AA/AB	Input/output processor (IOP) circuit pack	One-slot IOP for CMIC and RTIF
NTLX03	BA/BB	Input/output processor (IOP) circuit pack	Two-slot IOP for disk and tape
NTLX05	AA/AB	OC-3 two-port interface packlet	Core-MS interconnect (CMIC) interface for XA-Core to message switch (MS) communication
NTLX05	BA	OC-3 two-port AMDI interface packlet	Core-ATM interconnect

Table 1-2 XA-Core circuit packs and packlets (Continued) (Sheet 2 of 2)

PEC	Version	Name	Description
NTLX06	AA/AB	Disk drive packlet	4- or 8-Gbyte disk drive for data storage
NTLX07	AA	Digital audio tape (DAT) tape drive packlet	1.3-Gbyte DAT tape drive for data storage
NTLX08	AA/AB	RS232/ serial interface packlet	Remote terminal interface (RTIF)
NTLX09	AA	Ethernet single-port interface packlet	Connection to the LAN hub and the IP network
NTLX12	AA	Shelf interface module (SIM) circuit pack	Power supply/power conditioner
NTLX14	CA	Shared memory (SM) circuit pack	384-MBytes shared memory (SM)
NTLX20	AA	Filler circuit pack	Regulates air flow in the cabinet
NTLX20	BA	Terminating filler circuit pack	Terminating circuit pack for one slot not used in shelf

Visual indicators on circuit pack

Each XA-Core circuit pack and packlet has visual indicators on the faceplate. The visual indicators are light-emitting diodes (LED). These LEDs are indicators of the status of the circuit pack or packlet for removal. All the LEDs on all circuit packs and packlets of the XA-Core shelf illuminate in response to a MAP level command INDICAT with parameter TESTALL. The parameter TESTALL checks the LEDs for correct illumination. The status indicators are:

- Red LED illuminated indicates you can remove the circuit pack or packlet safely (circuit pack is not in service). The red LED can also wink instead of illuminate. The red LED winks in response to a MAP level command INDICAT activated for a circuit pack or packlet.
- Green LED illuminated indicates you cannot remove the circuit pack or packlet safely (circuit pack is in service).
- Amber LED illuminated indicates a loss of primary feed or link signal to the circuit pack or packlet. The amber LED is only on the SIM circuit packs and the CMIC/RTIF packlets. The amber LED is on the SIM circuit pack for loss of one or more power feeds to the SIM circuit pack. The amber LED is on the CMIC/RTIF packlets for loss of one or more link signals.

Live-inserted circuit pack

Maintenance activities can insert and remove XA-Core circuit packs from a live slot of an XA-Core shelf. The design of a non-contact midplane permits the live insertion and removal of XA-Core circuit packs. A non-contact midplane has electrical connections completed by the effect of electric and

magnetic field coupling in the circuit path. An exception to the live insertion and removal of circuit packs is the NTLX12AA shelf interface module (SIM) circuit pack. Remove power from the SIM circuit pack only before the insertion or removal of the SIM circuit pack. To remove power from the SIM circuit pack, turn off all three circuit breakers on the faceplate of the SIM circuit pack. XA-Core also permits the live insertion and removal of packlets.

XA-Core shelf design

SuperNode shelf layout

This section describes CP and packlet placement in an XA-Core shelf in a SuperNode.

In CSP15, the XA-Core shelf supports the following PE configurations: 2+1, 3+1, and 5+1.

- In the 2+1 configuration, there are PE circuit packs in slots 4 front, 5 front, and 16 front. All three PE circuit packs operate in a load sharing mode.
- In the 3+1 configuration, there are PE circuit packs in slots 4 front, 5 front, 13 front, and 16 front. All four PE circuit packs operate in a load sharing mode.
- In the 5+1 configuration, there are PE circuit packs in slots 4 front, 5 front, 6 front, 12 front, 13 front, and 16 front. All six PE circuit packs operate in a load sharing mode.

  Note: In each PE configuration, the spare processing power is the equivalent of one PE unit. A PE unit is the processing power of a PE circuit pack that uses PowerPC 604 processors. The NTLX02AA and the NTLX02CA use such processors.

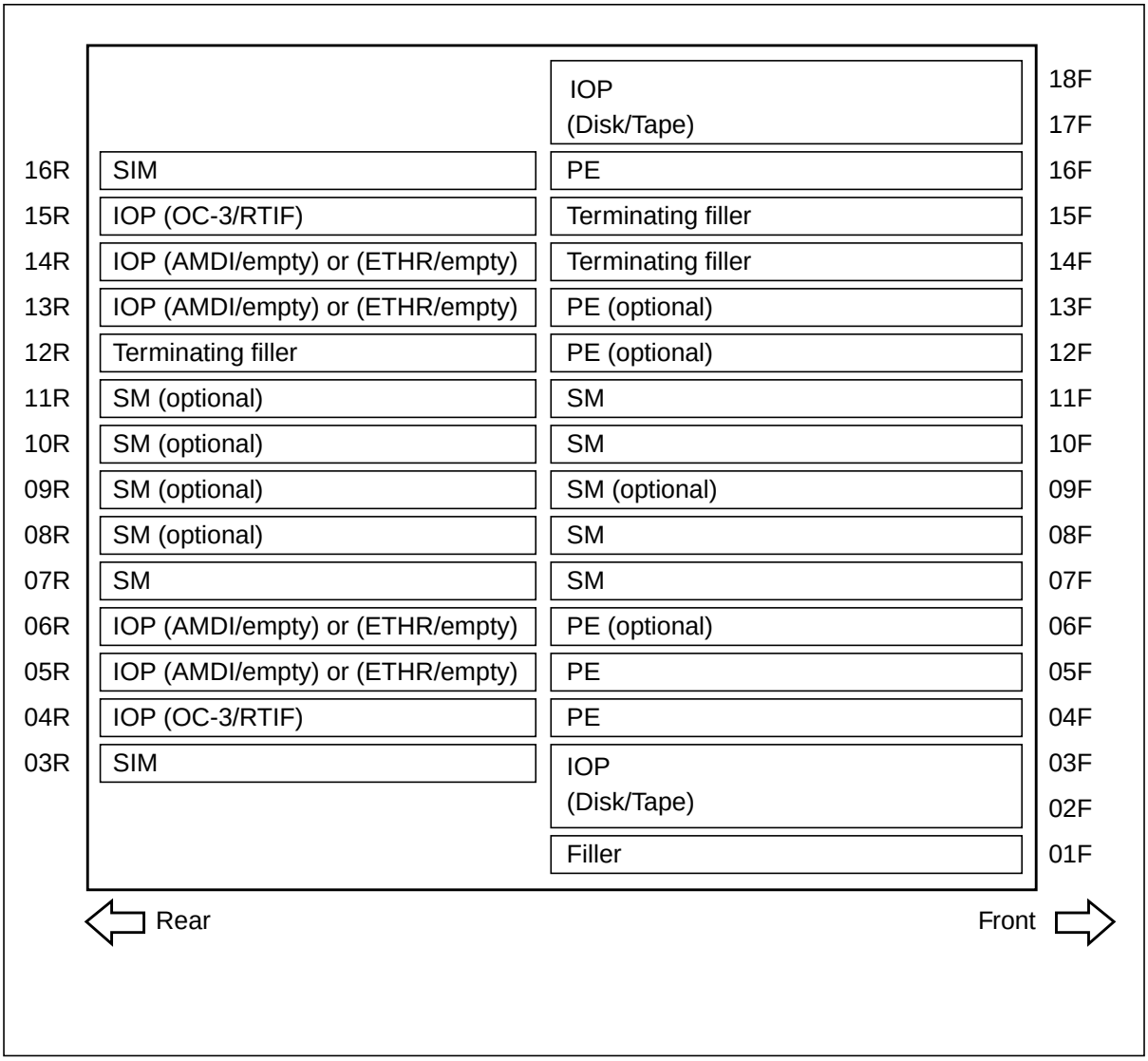
The minimum configuration requires that five SM cards be present in slots 7 front, 7 rear, 8 front, 10 front, and 11 front. Other supported configurations are

- seven SM cards (slots 7 front, 7 rear, 8 front, 10 front, 11 front, 10 rear, and 9 rear)
- ten SM cards (slots 7 front, 7 rear, 8 front, 10 front, 11 front, 10 rear, 9 rear, 8 rear, 9 front, and 11 rear)

The IOP cards in slots 5R, 6R, 13R, and 14R are optional.

Figure 1-8 on page 1-14 shows the shelf layout for an XA-Core shelf in a SuperNode.

Figure 1-8 Example of XA-Core shelf layout in SuperNode



SuperNode SE (SNSE) shelf layout

This section describes the shelf layout for an XA-Core shelf in a SuperNode SE (SNSE). In this scenario, the XA-Core is in the SNSE cabinet; it is not in an extension cabinet.

In CSP15, the XA-Core shelf supports the following PE configurations: 2+1, 3+1, and 5+1.

- In the 2+1 configuration, there are PE circuit packs in slots 4 front, 5 front, and 16 front. All three PE circuit packs operate in a load sharing mode.
- In the 3+1 configuration, there are PE circuit packs in slots 4 front, 5 front, 13 front, and 16 front. All four PE circuit packs operate in a load sharing mode.
- In the 5+1 configuration, there are PE circuit packs in slots 4 front, 5 front, 13 front, 14 front, 16 front, and 12 rear. All six PE circuit packs operate in a load sharing mode.

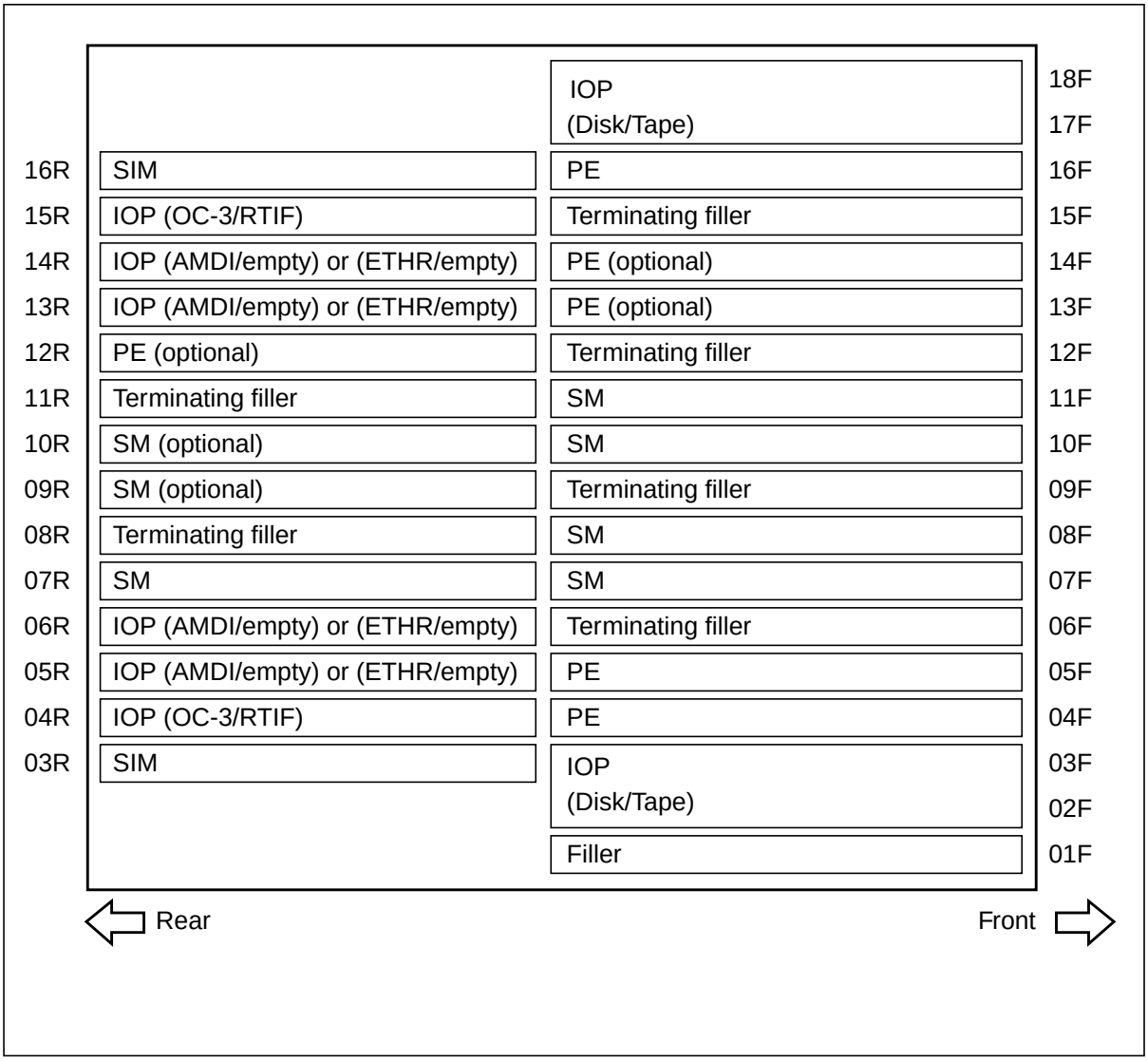
  Note: In each PE configuration, the spare processing power is the equivalent of one PE unit. A PE unit is the processing power of a PE circuit pack that uses PowerPC 604 processors. The NTLX02AA and the NTLX02CA use such processors.

The minimum configuration requires that five SM cards be present in slots 7 front, 7 rear, 8 front, 10 front, and 11 front. An additional supported configuration is seven SM cards (slots 7 front, 7 rear, 8 front, 10 front, 11 front, 10 rear, and 9 rear). The SNSE supports a maximum of seven SM cards.

The IOP cards in slots 5R, 6R, 13R, and 14R are optional.

Figure 1-9 on page 1-16 shows the shelf layout for an XA-Core shelf in the main cabinet in a SuperNode SE.

Figure 1-9 Example of XA-Core shelf layout in SuperNode SE



2 Preventive maintenance methods

This chapter describes preventive maintenance methods for the eXtended Architecture Core (XA-Core) in the DMS SuperNode and DMS SuperNode SE switches. This chapter lists the preventive maintenance procedures for routine maintenance that operating company personnel can perform. This chapter also describes the automatic maintenance performed on the XA-Core by the support operating system (SOS) of the switch.

This chapter includes the following sections:

- Routine maintenance procedures list the preventive maintenance procedures in the *XA-Core Maintenance Manual*, 297-8991-510.
- Automatic maintenance describes the system-run processes that detect, repair, and report problems.
- System recovery controller (SRC) describes the control of recovery activities by the SRC.
- Split mode of XA-Core describes the split mode of XA-Core into two sides.

Routine maintenance procedures

Routine procedures if performed according to a schedule, prevent faults in both the hardware and the software of the switch. Refer to the *XA-Core Maintenance Manual*, 897-8991-510, to find the procedures.

The XA-Core preventive maintenance procedures include the following:

- How to allocate test volumes on XA-Core disk drives
- How to allocate test volumes on XA-Core digital audio tape (DAT) drive packlets
- How to change XA-Core routine exercise (REx) intensity
- How to check and adjust the time of day (TOD) clock of XA-Core
- How to clean the XA-Core digital audio tape (DAT) drive
- How to copy an office image from XA-Core disk to tape

- How to perform light-emitting diode (LED) maintenance
- How to replace XA-Core cooling unit filters
- How to restore an office image from XA-Core tape to disk
- How to return an XA-Core circuit pack, packlet, or assembly to Nortel Networks
- How to schedule automatic image taking for XA-Core
- How to schedule digital audio tape (DAT) drive maintenance in XA-Core
- How to test wrist-strap grounding cords in XA-Core

Automatic maintenance

The XA-Core provides automatic maintenance through the following activities:

- processor bus matcher
- Audits
- Routine exercise (REx) tests
- System recovery controller (SRC)

Processor bus matcher

The processor bus matcher is in the RHINO processor which is an enhanced version of the high-speed instruction prefetcher path optimizer (Hippo) containing 512 Kilobytes of on board SRAM.

Audits

Audits are background processes that the switch runs to monitor the state of the XA-Core. Audits of software provide background processes that check the accuracy of applications and of resource data. Audits of hardware provide diagnostic tests of hardware. Audits run for both in-service and out-of-service conditions of hardware. The in-service diagnostics of audits prevent isolation of the circuit pack or packlet under test. An in-service diagnostic checks hardware except when the hardware is under normal operation of the software. The out-of-service diagnostics of audits are complete tests of a circuit packs or packlets. Separate diagnostic tests of hardware are in the audits or in the routine exercise (REx) tests but normally not both.

Routine exercise (REx) tests

Routine exercise (REx) tests are maintenance tests that the switch runs to check the state of the XA-Core. REx tests of software check the accuracy of software applications and of resource data. REx tests of hardware identify hardware failures before an outage or performance degradation occurs. The correction of hardware failures that REx tests identify prevents an outage or performance degradation. The system REx (SREx) test controller has software

that runs the REx tests for automatic execution at time intervals. The SREx tests run on the complete switch. SREx tests run when the CPU occupancy for CallP + Maintenance is less than 40%. Software table REXSCHED defines the time intervals for SREx tests. Table REXSCHED also provides the ability to enable or disable separate REx tests. A REXTST command at the MAP terminal can request a manual REx test on part of the XA-Core when required. A RExTst indication appears on the MAP display when the switch executes a REx test.

REx diagnostic tests

The REx tests perform diagnostic tests of hardware under two conditions. REx tests perform diagnostic tests on hardware that is in service and out of service. The in-service diagnostic tests of REx tests check all XA-Core functions and hardware that the XA-Core audits have not checked. The in-service diagnostics of REx tests prevent isolation of the circuit pack or packlet under test. The out-of-service diagnostic tests of REx checks fault detection of XA-Core hardware through error insertion. Error insertion for an out-of-service diagnostic on hardware requires the circuit pack or packlet to be in isolation. The out-of-service diagnostic of a REx test is not a complete test like the out-of-service diagnostic of an audit. An out-of-service diagnostic of a REx test checks hardware except when the hardware is under normal operation of the software.

REx tests have no check of the IDPROM of a circuit pack against software table PECINV. A check of the IDPROM occurs automatically in XA-Core during the addition of the circuit pack to the shelf.

The SREx tests run automatically each night, normally at the default time of 1:30 a.m. Normally on Wednesday, the full SREx test runs. On all other nights of the week, the base SREx test normally runs. Entries in software tables can modify the schedule for SREx tests. The entries for REx schedule are in table REXSCHED and office parameter NODEREXCONTROL of table OFCVAR. Refer to the procedure, “How to change XA-Core REx intensity” in this document.

Before the REx test begins, the switch automatically checks the dedicated stability threshold counters. The stability threshold counters perform a monitor of parity fault counts of the static random access memory (SRAM). If there are too many SRAM parity faults in a determined time before the request for a REx test, the switch responds as follows:

- The MAP displays a warning and confirmation prompt when a manual request for a REx test is not good. The manual REx test can abort or can execute.
- The switch aborts the beginning an automatic REx test at the planned time and generates a log report. The log indicate the reason for no REx test.

When two automatic REx tests that follow one another cancel in one day, a RExSch minor alarm occurs.

A monitor of the switch stability continues during a REx test. The switch aborts the REx test when a mismatch, trap, link closure, or restart occurs during a REx test.

REx test classes

REx tests are available in groups called classes. The classes of REx test are as follows:

- PE
- SM
- IO
- BASE
- ALL
- FULL

The classes of REx tests have the following differences:

- PE class of REx test is:
  - — A REx test on a processor element (PE) circuit pack of an XA-Core that is a different PE circuit pack for each REx test performed.
  - — The REx tests are out-of-service tests.
- SM class of REx test is:
  - — A REx test on a shared memory (SM) circuit pack of an XA-Core that is a different SM circuit pack for each REx test performed.
  - — The REx tests are out-of-service tests.
- IO class of REx test is:
  - — A REx test on an input/output processor (IOP) circuit pack and related packlets of an XA-Core. The REx test is on a different IOP circuit pack and related packlets for each REx test performed.
  - — The REx tests are out-of-service tests.
- BASE class of REx test is:
  - — A REx test while in service on all PE circuit packs, SM circuit packs, IOP circuit packs, and related packlets of an XA-Core.
  - — An image test performed.
  - — By default, BASE REx tests run each day of the week except Thursday.

- ALL class of REx test is:
  - — A REx test while in service on all PE circuit packs, SM circuit packs, IOP circuit packs, and related packlets of an XA-Core.
  - — A REx test while out of service on a different PE circuit pack, a different SM circuit pack, and a different IOP circuit pack (with related packlets) of an XA-Core. The circuit packs and packlets are different for each REx test.
- FULL class of REx test is:
  - — A REx test while in service on all PE circuit packs, SM circuit packs, IOP circuit packs, and related packlets of an XA-Core.
  - — A REx test while out of service on a different PE circuit pack, a different SM circuit pack, and a different IOP circuit pack (with related packlets) of an XA-Core. The circuit packs and packlets are different for each REx test.
  - — An image test performed.
  - — By default, FULL REx tests run each Thursday of the week.

REx test results report

When there is a REx test, the switch generates log report XAC415 to indicate a pass or failure of the REx test. The switch issues a RExTst minor alarm under the XAC header of the alarm banner when the REx test fails. Log report XAC415 reports on a REx test failure to indicate the following:

- reason for REx test failure
- category
- list of hardware detected for possible problem

When a system REx test cannot complete, the switch generates a failure reason. The following conditions of the switch prevent the system REx test from completing:

- can not interrupt another maintenance activity in process
- system resources not available to run the REx test (recommend REx test occur during low traffic periods)

When a REx test fails, another REx test that passes is the only way to clear the RExTst minor alarm. For the detailed instructions to clear the RExTst minor alarm, refer to the chapter, refer to the chapter, “Understanding the alarm system” in the *XA-Core Maintenance Manual*, 297-8991-510.

When a system REx test cannot start on two daily attempts that follow one another, the switch issues a RExSch minor alarm. The RExSch minor alarm appears under the XAC header of the alarm banner. A system REx test cancels

because faults exceed the thresholds monitored by the switch. The switch monitors thresholds for stability faults to identify repeating problems. Entries in software tables list the values of the thresholds.

Indications of automatic test results

The following indicators warn operating company personnel of the results of automatic maintenance tests.

- alarms
- logs
- operational measurements (OM)

Operating company personnel can monitor the indicators for directions and patterns. When monitored, operating company personnel can detect and correct small problems before the small problems become larger problems.

For detail information about clearing alarms, refer to the chapter, "Problem isolation and correction" of this document. Also, refer to the chapter, "Understanding the alarm system" in the *XA-Core Maintenance Manual*, 297-8991-510.

For additional information about logs, refer to the chapter, "Logs" of this document. Also, refer to the chapter, "Understanding XA-Core log reports" in the *XA-Core Reference Manual*, 297-8991-810.

For additional information about OMs, refer to the chapter, "Operational measurements" of this document. Also, refer to the chapter, "XA-Core operational measurements" in the *XA-Core Reference Manual*, 297-8991-810.

System recovery controller (SRC)

The system recovery controller (SRC) controls recovery activities in the switch. The SRC arranges the recovery of switch nodes in the correct sequence. The SRC recovers a node after recovery of other nodes that the node requires for correct recovery. The SRC plans the recovery activities to reduce the period of the outage.

The SRC makes several recovery attempts when a node cannot recover. The SRC makes more detail analysis with each recovery attempt. If needed, the SRC reloads a node's software and return the node to service. This reload of a node's software occurs when required because the node is out of service during the reload.

The SRC also controls recovery activities on switch nodes outside of the XA-Core module.

The SRC performs the following functions:

- SRC dependency manager controls the correct sequence of recovery of the switch nodes
- SRC group manager arranges switch nodes together in groups for broadcast loading when required
- SRC concurrent activity manager balances the amount of recovery work with other switch activities
- SRC starts recovery applications and monitors each step of the applications for quick completion

SRC activation

The following events make active the SRC to query and when needed, begin the recovery activities:

- warm restart of the XA-Core
- cold restart of the XA-Core
- reload restart of the XA-Core
- loss of software load in a peripheral module (PM)
- manual RESTART SWACT, ABORT SWACT, or NORESTART SWACT of the XA-Core

A restart restores the software of the support operating system (SOS) of the switch to a state that has stability. The reset terminal interface (RTIF) indicates the completion of a restart. The shape of the cursor on the RTIF display changes every second to indicate a completion of the restart. This change of the cursor shape for each second indicates basic operation of the SOS.

Split Mode of XA-Core

The XA-Core splits into two sides during an image test. The image test checks the sanity of the switch's software within the shared memory (SM) circuit packs of the XA-Core. The split XA-Core has an active side and an inactive side. The image test cannot start and split the XA-Core if one SM circuit pack only is available to the active side. The active side needs a minimum of two SM circuit packs for the XA-Core to split. Each side of the split XA-Core has one copy of the software image. The image test occurs on the image copy of the inactive side. Each side of the split XA-Core has one processor element (PE) circuit pack. The XA-Core has an ImgTst minor alarm displayed on the MAP during the image test. The image test runs manually by the Image command at the XACMtc level of the MAP. The image test also runs automatically for the base and full REx tests.

The split mode of XA-Core also can occur when the XA-Core is in an upgrade operation. The XA-Core has an Upgrade minor alarm displayed on the MAP during the upgrade operation.

3 Logs

This chapter describes the log reports for the eXtended Architecture Core (XA-Core) of the DMS SuperNode and DMS SuperNode SE switches.

Log reports are a primary source of information to monitor the components of the XA-Core. XA-Core log reports

- identify faults on XA-Core components
- provide information on system tests
- identify possible actions for correcting alarm conditions
- generate to indicate when an alarm condition clears

DMS SuperNode and SuperNode SE XA-Core related logs

The following types of logs are XA-Core related:

- XA-Core logs (XAC)
- lost logs (LOST)
- footprint logs (FPRT)
- input/output audit logs (IOAU)

Detailed information for analyzing the root cause of difficult log reports is in the chapter, “Problem isolation and correction” of this document. For additional information on logs of XA-Core, refer to the *XA-Core Reference Manual*, 297-8991-810.

XA-Core logs

XA-Core log reports identify information from XA-Core cards, subsystem clocks, imaging, routine exercise (REx) tests, and link tests.

The following list identifies all XA-Core log reports and their triggers.

Table 3-1 XA-Core log reports (Sheet 1 of 4)

Log	Title	Trigger
XAC300	LowSM	Low shared memory (SM) because of a fault on the indicated SM card.
XAC302	LowPE	Low processor element (PE) because of a fault on the indicated PE card.
XAC303	MScomm (Mesaage Switch Communication)	Problem of communication with the message switch (MS) because of a fault on cards, packlets, ports, or links.
XAC304	TOD (Time of Day Clock)	Problem with the Time of day (TOD) clock.
XAC305	RTIF (Reset Terminal Interface)	Problem with the reset terminal interface (RTIF) because of a fault on cards, packlets, or devices.
XAC306	Disk	Problem with a disk because of a fault on cards, packlets, or devices.
XAC307	Tape	Problem with a tape because of a fault on cards, packlets, or devices.
XAC308	Image Test Report	Failed an image test.
XAC309	AMDI	Loss of AMDI link redundancy.
XAC312	IOP	Problem with the input/output processor (IOP).
XAC320	Cardlist Report	XA-Core card list
XAC321	WgSlot (Shelf Audit Failure - Card Configuration)	A software audit has detected a card in the wrong XA-Core shelf slot.
XAC322	PETrbl	ISTb state of PE card.
XAC323	SMTrbl	ISTb state of SMcard.
XAC324	IOTrbl	ISTb state of IOP card or of a packlet.
XAC325	RIBKEY Detected	Retrofit inactive boot key (RIBKEY) tool installed in local ports of reset terminal interfaces (RTIF).

Table 3-1 XA-Core log reports (Sheet 2 of 4)

Log	Title	Trigger
XAC326	MS Link Configuration Mismatch	Mismatch detected between the expected message switch (MS) link configuration and the actual configuration.
XAC327	WgSlot (Card Inserted into Wrong slot)	XA-Core Card or packlet in wrong shelf slot.
XAC329	Ethernet	Problem of communication with XA-Core because of link failure or loss of ethernet link redundancy.
XAC330	Firmware Mismatch	Firmware version of the field replaceable unit does not match the version recorded in the data schema.
XAC333	Firmware Loading Failure	Firmware-loading process failure.
XAC335	OC-3 Packlet Fault	Informs user that table XAMDILNK must be datafilled.
XAC400	XA-Core Summary Report	XA-Core summary report.
XAC413	RExSch (REx Schedule Failure)	Routine exercise (REx) test cancelled two times in a row in one day.
XAC415	Routine Exercise (REx) Report	Report on routine exercise (REx) test.
XAC600	LowSM Condition Cleared	Cleared fault of low shared memory (SM).
XAC601	MemLim Condition Cleared	Cleared fault of memory limit
XAC602	LowPE Condition Cleared	Cleared fault of low processor element (PE).
XAC603	MScomm Alarm Cleared	Cleared fault of message switch (MS) communication.
XAC604	TOD Alarm Cleared	Cleared fault of time of day (TOD) clock.
XAC605	RTIF Alarm Cleared	Cleared fault of reset terminal interface (RTIF).
XAC606	Disk Alarm Cleared	Cleared fault of disk.
XAC607	Tape Alarm Cleared	Cleared fault of tape.

Table 3-1 XA-Core log reports (Sheet 3 of 4)

Log	Title	Trigger
XAC608	Image Alarm Cleared	Cleared fault of image.
XAC609	AMDI Link Condition Cleared	AMDI links are returned to service.
XAC610	Card Returned To Service	Card returned to service (RTS).
XAC612	IOP Alarm Cleared	Cleared input/output processor (IOP) alarm.
XAC613	RExSch Alarm Cleared	Cleared fault of routine exercise (REx) schedule.
XAC614	XATrap Alarm Cleared	Cleared fault of software trap in XA-Core.
XAC615	REx Started	Started routine exercise (REx) test.
XAC618	Split (Split Mode Entered)	XA-Core has entered split mode.
XAC619	Split Mode Exited	XA-Core has exited split mode.
XAC622	PETrbl Alarm Cleared	Cleared PETrbl alarm.
XAC623	SMTrbl Alarm Cleared	Cleared SMTrbl alarm.
XAC624	IOTrbl Alarm Cleared	Cleared IOTrbl alarm.
XAC625	RIBKEY Removed	Retrofit inactive boot key (RIBKEY) tool removed from local ports of reset terminal interface (RTIF) packlet.
XAC626	MS Link Configuration Restored	Message switch (MS) link configuration restored.
XAC627	WgSlot Cleared (Card Removed)	Card or packlet removed from wrong XA-Core shelf slot.
XAC628	Provisioning/Depro-visioning Information Log	Log output when provisioning or deprovisioning.
XAC629	Ethernet cleared	Cleared ETHR alarm.
XAC630	Firmware Mismatch Cleared	Cleared firmware mismatch.
XAC631	Firmware Soaking Started	Firmware-soaking process begins.
XAC632	Firmware Soaking completed	Firmware-soaking process ends.

Table 3-1 XA-Core log reports (Sheet 4 of 4)

Log	Title	Trigger
XAC633	Firmware Loading started	Firmware-loading process begins.
XAC634	Firmware Loading Completed	Firmwarer-loading process ends successfully.
XAC635	Firmware Loading in Progress	A restart has occurred and a field replaceable unit is in the soaking state.
XAC640	Manual Test Report	Manual test on a selected XA-Core card, packlet, or link to determine if it is in service or out of service.
XAC801	MemLim (Memory Limit)	Memory allocation to the operating system reaches 90 percent of the limit.
XAC814	XATrap	Number of software traps exceeds the alarm threshold.

Lost logs

The switch generates lost (LOST) log reports for lost messages or for message errors.

The following list identifies lost log reports and their triggers.

Table 3-2 Lost log reports

Log	Title	Trigger
LOST110	MSG TOSSED	Message tossed.
LOST111	INPUT HANDLER ERROR	Input handler error.
LOST116	SEND ERROR	Send error.

Footprint logs

The switch generates footprint (FPRT) log reports after a switch restart. The footprint log report contains snapshot data on the XA-Core.

The following list identifies footprint logs and their triggers.

Table 3-3 Footprint logs

Log	Title	Trigger
FPRT105	Successful Footprint	Snapshot data reported on XA-Core footprint after a switch restart.
FPRT106	Footprint Not Collected	Footprint not collected for XA-Core after a switch restart.

Input/output audit logs

The switch generates input/output audit (IOAU) log reports that provide information related to input/output (I/O) audits.

The following list identifies the input/output audit log reports and their triggers.

Table 3-4 Input/output audit logs

Log	Title	Trigger
IOAU112	REX Scheduler Notice	Scheduler notice for routine exercise (REx) test.

4 Operational measurements

This chapter describes the operational measurements (OM) for the eXtended Architecture Core (XA-Core) of the DMS SuperNode and SuperNode SE switches.

DMS SuperNode and SuperNode SE XA-Core related OMs

OMs provide load and performance information. The OM system controls collection, display, and generation of OM data for the operating company. For additional information on OMs of XA-Core, refer to the chapter, "XA-Core operational measurements" in the *XA-Core Reference Manual*, 297-8991-810.

OM group XACORE

OM group XACORE provides performance information about the XA-Core. For detailed information on the registers of OM group XACORE, refer to the chapter, "XA-Core operational measurements" in the *XA-Core Reference Manual*, 297-8991-810. For lists of logs and alarms related to individual OM registers, see Table 7-1 on page 7-5 in this document.

The following table lists the registers in OM group XACORE for Release 1.

Table 4-1 OM group XACORE registers for Release 1 (Sheet 1 of 2)

Register	Peg reason or usage description
XAPE	Processing element (PE) fault
XAPEMAJU	Period of PE major alarm
XAPECRIU	Period of low processing capacity
XARXPE	Failure of routine exercise (REx) test for class PE
XASM	Critical Shared memory (SM) fault
XASSMPXU	Period of simplex SM operation caused by system action of switch
XAMSMPXU	Period of simplex SM operation caused by manual action on switch

Table 4-1 OM group XACORE registers for Release 1 (Sheet 2 of 2)

Register	Peg reason or usage description
XARSMPXU	Period of simplex SM operation caused by REx test
XASMCRIU	Period of low shared memory critical alarm
XARXSM	Failure of routine exercise (REx) test for class SM
XAIOP	Critical Input/output processor (IOP) fault
XARXIO	Failure of routine exercise (REx) test for class IO
XADISK	Disk fault
XATAPE	Tape fault
XARTIF	Reset terminal interface (RTIF) packlet fault
XALOCP	Critical fault on the local port of the reset terminal interface (RTIF) packlet
XAREMP	Critical faults on the remote port of the reset terminal interface (RTIF)
XACMIC	Computing module interface connector (CMIC) fault
XASWINI	Warm restart caused by system action of switch
XAMWINI	Warm restart caused by manual action on switch
XASCINI	Cold restart caused by system action of switch
XAMCINI	Cold restart caused by manual action
XATRAP	XA-Core trap interrupt
XARXABRT	System routine exercise (REx) test aborted
XARXBASE	Failure of routine exercise (REx) test for class BASE
XARXFULL	Failure of routine exercise (REx) test for class FULL
XARXALL	Failure of routine exercise (REx) test for class ALL
XALKMAJU	Period of MScomm major alarm
XAMDI	Number of critical AMDI packlet faults
XAMDILNK	Number of critical AMDI link faults
XAMDMAJU	Period of AMDI major alarm
XAMDCRIU	Period of AMDI critical alarm

The following table lists the registers in OM group XACORE for Release 2.

Table 4-2 OM group XACORE registers for Release 2

Register	Peg reason or usage description
XAPE	Processing element (PE) fault
XARXPE	Failure of routine exercise (REx) test for class PE
XASM	Critical Shared memory (SM) fault
XARXSM	Failure of routine exercise (REx) test for class SM
XAIOP	Critical Input/output processor (IOP) fault
XARXIO	Failure of routine exercise (REx) test for class IO
XADISK	Disk fault
XATAPE	Tape fault
XARTIF	Reset terminal interface (RTIF) packlet fault
XALOCP	Critical fault on the local port of the reset terminal interface (RTIF) packlet
XAREMP	Critical faults on the remote port of the reset terminal interface (RTIF)
XACMIC	Computing module interface connector (CMIC) fault
XARXABRT	System routine exercise (REx) test aborted
XARXBASE	Failure of routine exercise (REx) test for class BASE
XARXFULL	Failure of routine exercise (REx) test for class FULL
XARXALL	Failure of routine exercise (REx) test for class ALL
XAMDI	Number of critical AMDI packlet faults
XAMDILNK	Number of critical AMDI link faults
XETHR	Number of critical ethernet packlet faults
XETHRPRT	Number of critical ethernet port faults
XETHRLNK	Number of critical ethernet link faults

OM group XACPOM

OM group XACPOM includes the CPBASE OMs for XA-Core. For detailed information on the registers of OM group XACPOM, refer to the chapter, "XA-Core operational measurements" in the *XA-Core Reference Manual*, 297-8991-810.

Table 4-3 OM group XACPOM registers for Release 2

Register	Peg reason or usage description
ENCAPSZ	Encapsulators requested and retrieved
ENCAPSZ2	Number of times ENCAPSZ has wrapped around maximum value of 65536
ENCPOVFL	Period of low processing capacity
CPOVFL	Failure of routine exercise (REx) test for class PE
ENMSSZ	Critical Shared memory (SM) fault
ENMSOVFL	Period of simplex SM operation caused by system action of switch

OM group XACSRVC

OM group XACSRVC contains 11 usage registers, which record the lengths of time that fault or alarm conditions exist, and five peg registers, which record the number of fault conditions on the XA-Core. For detailed information on the registers of OM group XACSRVC, refer to the chapter, "XA-Core operational measurements" in the *XA-Core Reference Manual*, 297-8991-810.

Table 4-4 OM group XACSRVC registers for Release 2 (Sheet 1 of 2)

Register	Peg reason or usage description
XAPEMAJU	Period of PE major alarm
XAPECRIU	Period of low processing capacity
XASSMPXU	Period of simplex SM operation caused by system action of switch
XAMSMPXU	Period of simplex SM operation caused by manual action on switch
XARSMPXU	Period of simplex SM operation caused by REx test
XASMCRIU	Period of low shared memory critical alarm

Table 4-4 OM group XACSRVC registers for Release 2 (Sheet 2 of 2)

Register	Peg reason or usage description
XASWINI	Warm restart caused by system action of switch
XAMWINI	Warm restart caused by manual action on switch
XASCINI	Cold restart caused by system action of switch
XAMCINI	Cold restart caused by manual action
XATRAP	XA-Core trap interrupt
XALKMAJU	Period of MScomm major alarm
XAMDMAJU	Period of AMDI major alarm
XAMDCRIU	Period of AMDI critical alarm
XETHRMJU	Period of ETHR major alarm
XETHRCRU	Period of ETHR critical alarm

OM group XASTAT

OM group XASTAT measures central processing unit (CPU) usage and call processing on the XA-Core. For detailed information on the registers of OM group XASTAT, refer to the chapter, "XA-Core operational measurements" in the *XA-Core Reference Manual*, 297-8991-810.

Table 4-5 OM group XASTAT registers for Release 2 (Sheet 1 of 2)

Register	Peg reason or usage description
XASUTIL	Percentage of call processing capacity used
XASPUTIL	Peak call processing usage
XASCMPLX	Indicates ratio of complexity of observed call mix compared to standard office
XASSCHED	Indicates ratio of scheduling overhead compared to expected capacity
XASFORE	Indicates ratio of operating system overhead compared to overhead allocated at capacity
XASMAINT	Indicates ratio of maintenance usage compared to allocation

Table 4-5 OM group XASTAT registers for Release 2 (Sheet 2 of 2)

Register	Peg reason or usage description
XASDNC	Indicates ratio of NOSFT usage compared to allocation
XASOM	Indicates ratio of OM usage compared to allocation
XASGTERM	Indicates ratio of GTerm usage compared to GUARANTEED_TERMINAL_CPU_SHARE office parameter
XASBKG	Indicates ratio of background class usage compared to allocation
XASAUXCP	Indicates ratio of AUXCP usage compared to AUXCP_CPU_SHARE office parameter
XASNETM	Indicates ratio of NETMTC usage compared to allocation
XASSNIP	Indicates ratio of SNIP usage compared to allocation
XASPESC	Number of one-minute intervals during PE state change transfer period
XASNXFR	Number of transfer periods
XASOVER	Number of transfer periods while system usage was greater than 100%
XASOTHLD	Number of one-minute intervals while system utilization exceeded office parameter CC_ENGLEVEL_WARNING_THRESHOLD

5 User interface and commands

This chapter describes the maintenance and administration position (MAP) displays of the XA-Core. This chapter also provides information about the non-menu hidden commands for the MAP levels of the XA-Core. In this chapter are examples of MAP displays and descriptions of the status field indicators of the MAP display. This chapter also has information about the reset terminal interface (RTIF) of the MAP display.

This chapter describes the following:

- XA-Core MAP levels and non-menu hidden commands

  This section describes the non-menu hidden commands that are available at each MAP level of the XA-Core. This section provides examples of MAP displays and a table of all possible values in the fields of the MAP display.

- Reset terminal interface commands

  This section describes the commands available for the reset terminal interface (RTIF) of the MAP display.

XA-Core MAP levels and nonmenu commands

XA-Core has MAP levels that display interactive information about a MAP terminal. The XA-Core MAP levels display XA-Core information. The XA-Core MAP levels also provide command entry from both a menu and from no menu (or non-menu) selections. Information about the menu commands is in the *XA-Core Reference Manual*, 29708991-810. This chapter describes the XA-Core MAP levels and the non-menu commands that are available at the XA-Core MAP levels.

XA-Core MAP levels

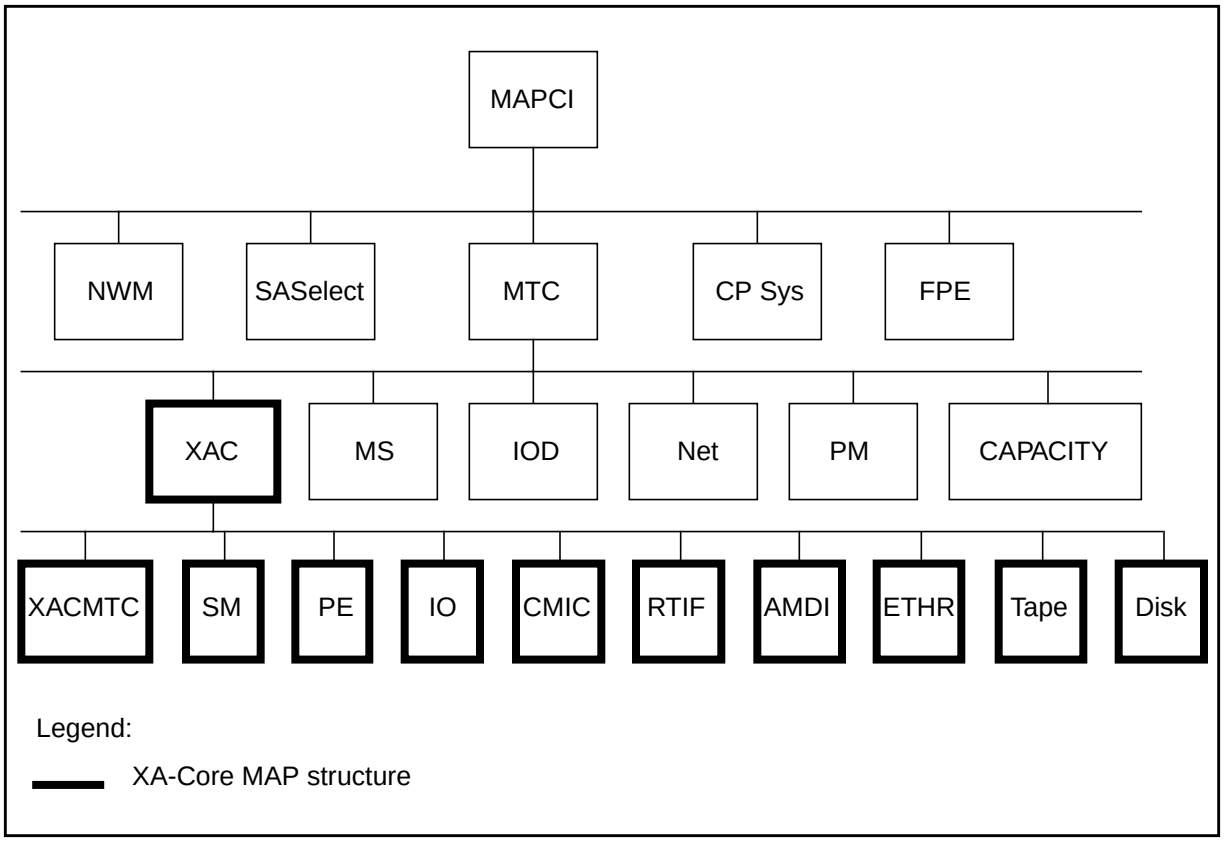
Access to the XA-Core MAP levels starts from the command interpreter (CI) of the MAP display through the MAPCI and MTC levels. A list of XA-Core Map levels is as follows.

- XAC level
- XACMtc level

- SM level
- PE level
- IO level
- CMIC level
- RTIF level
- AMDI level
- ETHR level
- Tape level
- Disk level

Figure 5-1 describes the hierarchy of the MAP display levels of XA-Core.

Figure 5-1 MAP hierarchy

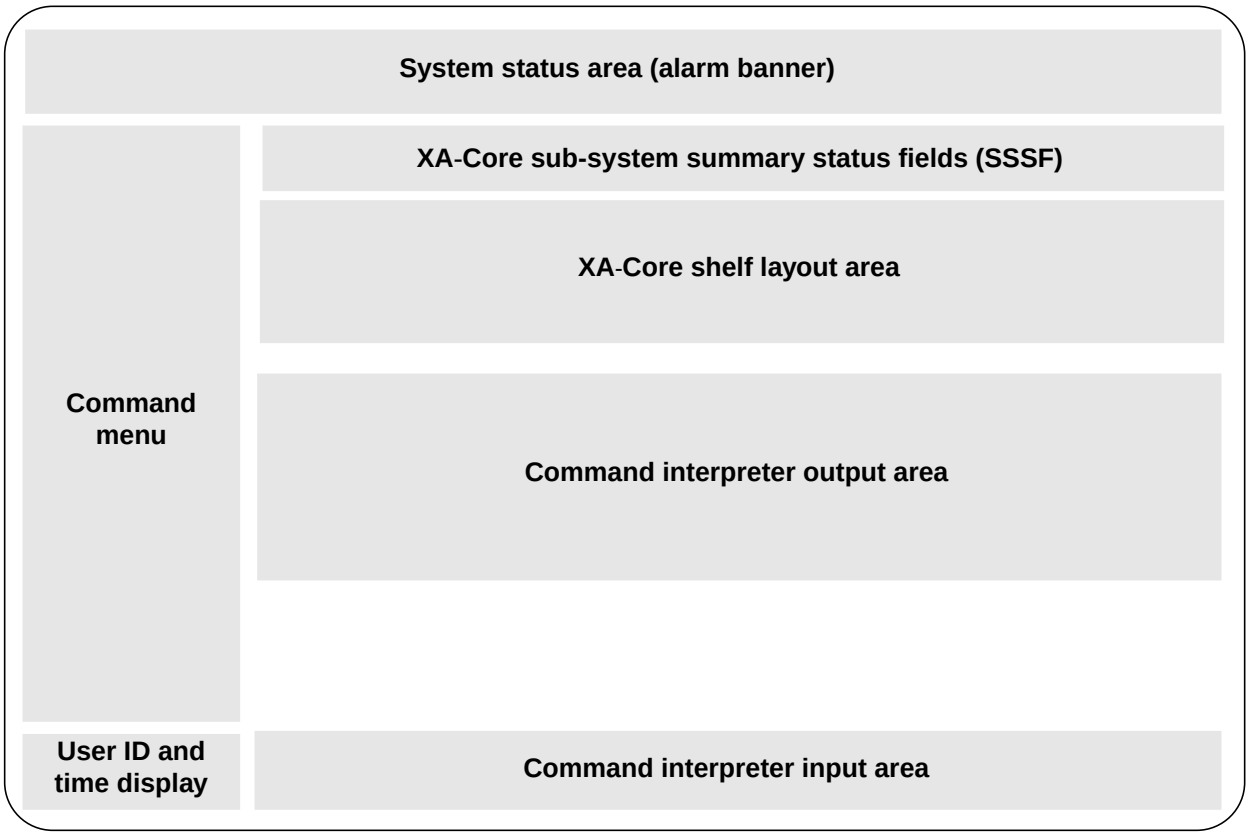


Note: This document contains information on the CAPACITY MAP level, which is accessed through the MAPCI and MTC levels. For information on the CAPACITY MAP level, see the chapter, “Capacity-monitoring tools in an XA-Core”.

XA-Core MAP display

The XA-Core MAP display is a user interface to the switch. The MAP display has real-time information about the switch. Entry of commands to the switch can originate at the MAP display. Refer to the *XA-Core Reference Manual*, 297-8991-810, for a description of the XA-Core MAP layout. Figure 5-2 shows the layout of an XA-Core MAP display.

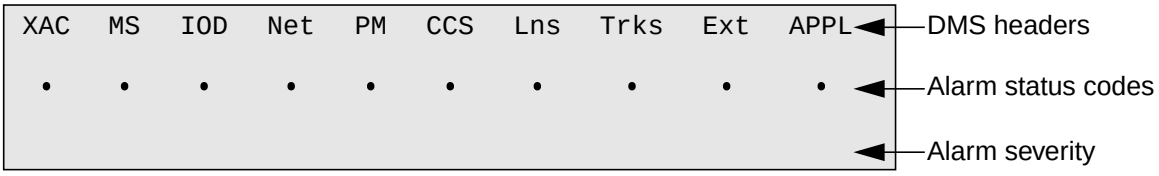
Figure 5-2 Layout of an XA-Core MAP display



System status area (alarm banner)

The system status area of the MAP display shows system alarms of the switch under an alarm banner. The alarm banner has XA-Core system alarms under the header XAC. Figure 5-3 shows the system status area (alarm banner) on an XA-Core MAP display.

Figure 5-3 System status area (alarm banner) on an XA-Core MAP display



XA-Core shelf layout area

Figure 5-4 shows an XA-Core shelf layout area on a MAP display. The physical side (front/rear) field displays the position of the CPs or packlets in the physical shelf. A single or two-digit number indicates the physical slot positions on the physical side. The CPs and packlets of the shelf layout area of XA-Core have status field indicators. The XA-Core MAP levels display the status of CPs and packlets in fields identified as Sta (status) and Dep (dependency). A field identified as Typ (type) displays an asterisk (*) to show the slots that the current MAP can process a command on.

Figure 5-4 XA-Core shelf layout area on a MAP display

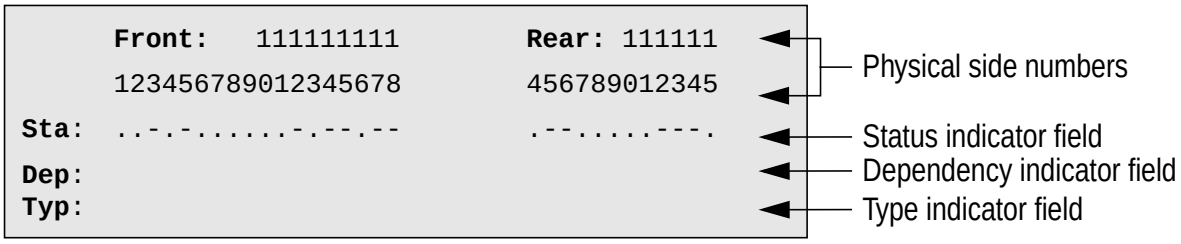


Table 5-1 describes the status field indicators at XA-Core levels of the MAP.

Table 5-1 Status field indicators at XA-Core levels of the MAP (Sheet 1 of 2)

Field	Indicator	Description
Sta	(blank)	Slot not used
	. (dot)	Circuit pack (CP) and/or packlet in slot is in service (**InSv**)
	-	No equipment in slot
	C	CP and/or packlet in slot is central side busy (CBsy)
	I	CP and/or packlet in slot is in service trouble (**ISTb**)
	M	CP and/or packlet in slot are manual busy (**ManB**)
	S	CP and/or packlet in slot are system busy (**SysB**)
	X	CP and packlets in slot are in the split mode
Dep	(blank)	A blank indicates no dependency.

Table 5-1 Status field indicators at XA-Core levels of the MAP (Sheet 2 of 2)

Field	Indicator	Description
	T	A "T" indicates an under test dependency. The under test dependency means that the CP in the matching physical side number field is under test. The field displays a blank after the test is complete.The test (T) dependency has priority over the fault (F) dependency.
	F	An "F" indicates a fault dependency. The fault dependency means that a packlet in the matching physical side number field has a fault or is out of service (OOS).
Typ	(blank)	A blank in the type status indicates the slots that commands of the current MAP level cannot process a command on.
	* (asterisk)	An asterisk in the type status indicates the slots that the current MAP level can process a command on.

Subsystem status summary field (SSSF) at XA-Core levels of the MAP

The subsystem status summary field (SSSF) displays the working status of the equipment. Figure 5-5 shows the XA-Core SSSF on a MAP display. The SSSF includes three rows that display the following information.

1. **Subsystem headers**: A permanently displayed set of titles that describe the different XA-Core subsystems. The headers match the subsystems for the CP types (SM, PE, IO) and the packlet (PKLT).
2. **Equipment alarm codes**: The equipment alarm field shows equipment alarms for each subsystem type. If there are multiple faults in a single card/packlet type, the equipment alarm field displays the most important.
3. **OOS FRU count**: The out-of-service (OOS) field replaceable unit (FRU) count field displays the total number of out-of-service CPs or packlets in each of the subsystems. The count can increase for each critical fault condition. The count does not increase for not-critical device faults and trouble conditions.

Figure 5-5 XA-Core subsystem status summary field (SSSF) on a MAP display

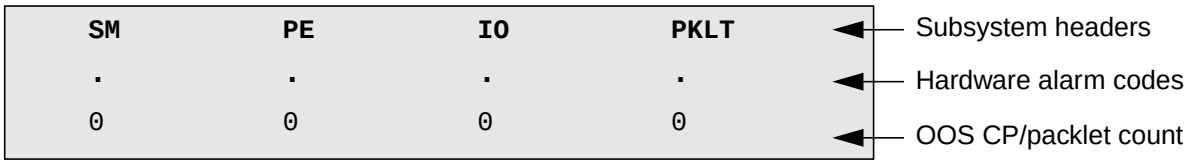


Table 5-2 shows the SSSF equipment alarms of CPs. The equipment alarms of CPs are under the headers PE, SM, and IO in the SSSF of the MAP display. A CP is an FRU that has a product engineering code (PEC). The table shows a fault/state description for each SSSF equipment alarm.

Table 5-2 Equipment alarms of cards in SSSF fields SM/PE/IO of XA-Core levels of the MAP

Fault/State Description	SM	PE	IO
Critical fault	SMfl	PEfl	IOPfl
Cannot detect FRU	noCard	noCard	noCard
Inactive FRU	split	split	split
REx Test	RExTst	RExTst	RExTst
ManB FRU	SM M	PE M	IOP M
FRU trouble	SMtb	PEtb	IOPtb
Slot not provisioned	badPEC	badPEC	badPEC
Unknown fault	SM ?	PE ?	IOP ?
Firmware fault	SMfw	PEfw	IOPfw

Tables 5-3 and 5-4 show the SSSF equipment alarms of packlets. The equipment alarms are under the header PKLT in the SSSF of the MAP display. The tables show the equipment alarms for different types of packlets. The table also shows a fault/state description for each SSSF equipment alarm.

Table 5-3 Equipment alarms of packlets in SSSF field PKLT of XA-Core levels of the MAP

Fault/State Description	PKLT					
	CMIC	**TOD**	**MS link**	**RTIF**	**Local RTIF**	**Remote RTIF**
Cannot correct fault	CMICfl	TODfl	LINKfl	RTIFfl	LocPfl	RemPfl
Inactive FRU	split	split	split	split	split	split
REx test	RExTst	RExTst	RExTst	RExTst	RExTst	RExTst
RIB key not removed				RIBkey	RIBkey	RIBkey
CMIC isolation	XAisol					
TOD isolation		TODflt				
MS TOD fault		MSTOD				
ManB FRU	CMIC M			RTIF M	LocP M	RemP M
Dependency busy FRU	CMIC C	TOD C	LINK C	RTIF C	LocP C	RemP C
FRU trouble	CMICtb	TODtb	LINKtb	RTIFtb	LocPtb	RemPtb
Slot not provisioned	badPEC			badPEC		
Unknown fault	CMIC ?	TOD ?	LINK ?	RTIF ?	LocP ?	RemP ?

Table 5-4 Equipment alarms of packlets in SSSF field PKLT of XA-Core levels of the MAP

Fault/State Description	PKLT			
	Disk	**Tape**	**AMDI**	**ETHR**
Cannot correct fault	DISKfl	TAPEfl	AMDIfl	ETHRfl
Inactive FRU	split	split	split	split
REx test	RExTst	RExTst	RexTst	RexTst
RIB key not removed				
CMIC isolation				
TOD isolation				
MS TOD fault				
ManB FRU	DISK M	TAPE M	AMDI M	ETHR M
Dependency busy FRU	DISK C	TAPE C	AMDI C	ETHR C
FRU trouble	DISKtb	TAPEtb	AMDItb	ETHRtb
Slot not provisioned	badPEC	badPEC	badPEC	badPEC
Unknown fault	DISK ?	TAPE ?	AMDI ?	ETHR ?

Common hidden menu commands

The following commands are hidden menu commands that are common for all XA-Core MAP levels. Perform these commands at the XAC, XACMtc, SM, PE, IO, CMIC, RTIF, Tape, and Disk levels of the MAP.

ABORT

The abort (ABORT) command aborts another command before the other command enters to task. Use the ABORT command when the command that you abort has not started a task.

ABTK

The abort task (ABTK) command aborts a task that is active. Use the ABTK command when the command that you abort has started a task.

XAC level hidden menu commands

Perform the common hidden menu commands of XA-Core at the XAC MAP level.

Figure 5-6 is an example of an XAC MAP level.

Figure 5-6 XAC MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

XAC                    Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit                 123456789012345678   456789012345   .    .    .    .
 2 Card_          Sta:  -. .--..-.-----..    .--.--------.   0    0    0    0
 3 XACMtc         Dep:
 4 SM              MTC:
 5 PE              XAC:
 6 IO
 7 CMIC
 8 RTIF
 9 Disk
10 Tape
11 AMDI
12
13
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

XACMtc level hidden menu commands

Perform the common hidden menu commands of XA-Core at the XACMtc MAP level.

Figure 5-7 is an example of an XACMtc MAP level.

Figure 5-7 XACMtc MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

XACMtc          Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit         123456789012345678   456789012345   .    .    .    .
 2              Sta:  -. .--..-..----..    .--.-------.   0    0    0    0
 3              Dep:
 4              Traps:        Per Minute  =    0          Total =   1
 5              Last Image run at:      00:00:00
 6                        restart type = warm
 7              Last XARExTst run at:  10:07:28
 8              Last XARExTst Type:    base
 9               XACMtc:
10
11 Image
12 RExTst_
13 RExInt_
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

SM level hidden menu commands

Perform the common hidden menu commands of XA-Core at the SM MAP level.

Figure 5-8 is an example of an SM MAP level.

Figure 5-8 SM MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

SM                    Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit               123456789012345678   456789012345   .    .    .    .
 2                Sta: -. .--..-..----..    .--.-------.   0    0    0    0
 3                Dep:
 4                Typ:        ** **             *
 5                  Physical: 1920         Useable: 1920        Available: 960
 6 Tst_             SYNC State: triplex
 7 Bsy_
 8 RTS_           XAC:
 9                SM:
10
11
12 Uneq_
13
14 Alarm_
15
16 Trnsl_
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

PE level hidden menu commands

Perform the common hidden menu commands of XA-Core at the SM MAP level.

Figure 5-9 is an example of a PE MAP level.

Figure 5-9 PE MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

PE                    Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit               123456789012345678   456789012345   .    .    .    .
 2                Sta: -. .--..-..----..    .--.-------.   0    0    0    0
 3                Dep:
 4                Typ:     *           *
 5                 XAC:
 6 Tst_            PE:
 7 Bsy_
 8 RTS_
 9
10 LoadFW_
11
12 Uneq_
13
14 Alarm_
15
16 Trnsl_
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

IO level hidden menu commands

Perform the common hidden menu commands of XA-Core at the IO MAP level.

Figure 5-10 is an example of an IO MAP level.

Figure 5-10 IO MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

IO                    Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit              123456789012345678  456789012345   .    .    .    .
 2                  Sta: -.-.-.-.-.-.-.-.-.  ..-.-.-.-..   0   0    0    0
 3                  Dep:
 4                  Typ:  *              *   **        **
 5                  Slot: Side: Status:  Packlets-Upper:         Lower:
 6 Tst_               2   Front    .              Tape  .        Disk .
 7 Bsy_              17   Front    .              Tape  .        Disk .
 8 RTS_               4   Rear     .              RTIF  .        CMIC .
 9                   15   Rear     .                            AMDI .
10 LoadFW_           14   Rear     .                            AMDI .
11 Uneq_             15   Rear     .              RTIF  .        CMIC .
12                  XAC:
13                   IO:
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

CMIC level unlisted menu commands

Perform the common hidden menu commands of XA-Core at the CMIC MAP level.

Figure 5-11 is an example of a CMIC MAP level.

Figure 5-11 CMIC MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

CMIC                 Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit              123456789012345678   456789012345   .    .    .    .
 2                Sta: -. .--..-.-----..    .--.-------.   0    0    0    0
 3                Dep:
 4                Typ:                        *          *
 5                Slot:  Side: Packlet:  Status: Link0: Link1:  TOD:
 6 Tst_              4   Rear  lower     .       .      .       .
 7 Bsy_             15   Rear  lower     .       .      .       .
 8 RTS_           XAC:
 9                CMIC:
10 LoadFW_
11
12 Cntrs_
13 Route_
14 Alarm_
15
16 Trnsl_
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

RTIF level hidden menu commands

Perform the common hidden menu commands of XA-Core at the RTIF MAP level.

Figure 5-12 is an example of an RTIF MAP level.

Figure 5-12 RTIF MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

RTIF                 Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit              123456789012345678   456789012345   .    .    .    .
 2                Sta: -. .--..-..----..    .--.-------.   0    0    0    0
 3                Dep:
 4                Typ:                        *          *
 5                Slot: Side: Packlet:  Status:  Local Port:  Remote Port:
 6 Tst_             4   Rear  upper     .        .            .
 7 Bsy_            15   Rear  upper     .        .            .
 8 RTS_            XAC:
 9                 RTIF:
10
11
12 Cntrs_
13
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

AMDI level hidden menu commands

Perform the common hidden menu commands of XA-Core at the AMDI MAP level.

Figure 5-13 is an example of an AMDI MAP level.

Figure 5-13 AMDI MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

AMDI                    Front:    111111111   Rear:  111111  SM   PE   IO PKLT
 0 Quit                 123456789012345678   456789012345  .    .    .    .
 2                  Sta: -.-.--.-.-.-.--.-.   ...-...---.  0    0    0    0
 3                  Dep:
 4                  Typ:                        *         *
 5                  Slot: Side: Packlet:  Status:  Link0:  Link1:
 6                   05   Rear  lower     .        .        -
 7 Tst_              06   Rear  lower     .        .        -
 8 Bsy_              13   Rear  lower     .        .        -
 9 RTS_              14   Rear  lower     .        .        -
10 LoadFW_
11 Uneq_            AMDI:
12
13
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

ETHR level hidden menu commands

Perform the common hidden menu commands of XA-Core at the ETHR MAP level.

Figure 5-14 is an example of an ETHR MAP level.

Figure 5-14 ETHR MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

AMDI                  Front:    111111111   Rear:  111111  SM   PE   IO PKLT
 0 Quit               123456789012345678   456789012345  .    .    . ETHR M
 2                Sta: -.-.--.-.-.-.--.-.   ...-...---.  0    0    0    0
 3                Dep:
 4                Typ:                        *         *
 5                Slot: Side: Packlet:  Status:  Link0:  Link1:
 6                 05   Rear  lower     .        .        -
 7 Tst_            06   Rear  lower     .        .        -
 8 Bsy_            13   Rear  lower     .        .        -
 9 RTS_            14   Rear  lower     .        .        -
10 LoadFW_
11 Uneq_          ETHR:
12
13
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

Tape level hidden menu commands

Perform the common hidden menu commands of XA-Core at the Tape MAP level.

Figure 5-15 is an example of a Tape MAP level.

Figure 5-15 Tape MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

Tape                 Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit              123456789012345678   456789012345   .    .    .    .
 2                Sta: -. .--..-..----..    .--.-------.  0    0    0    0
 3                Dep:
 4                Typ:   *              *
 5                Slot:  Side:   Packlet: Status:  User Name:  Drive:
 6 Tst_              2   Front   Upper    .        SYSTEM      mounted
 7 Bsy_             17   Front   Upper    .                    idle
 8 RTS_           XAC:
 9                Tape:
10
11
12 Cntrs_
13
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

Disk level hidden menu commands

Perform the common hidden menu commands of XA-Core at the Disk MAP level.

Figure 5-16 is an example of a Disk MAP level.

Figure 5-16 Disk MAP level

```
XAC     MS     IOD     Net     PM     CCS     Lns     Trks     Ext     APPL
 .      .       .      .       .       .      .        .       .        .

Disk                    Front:   111111111   Rear: 111111   SM   PE   IO  PKLT
 0 Quit                 123456789012345678   456789012345   .    .    .    .
 2                  Sta: -. .--..-.-----..    .--.--------.  0    0    0    0
 3                  Dep:
 4                  Typ:   *              *
 5                  Slot: Side:  Packlet:  Status:
 6 Tst_               2   Front  Lower     .
 7 Bsy_              17   Front  Lower     .
 8 RTS_
 9
10                   XAC:
11 Format_           Disk:
12
13
14 Alarm_
15
16
17 Indicat_
18 Query_
  XMAP0
 Time  14:12
```

Reset terminal interface (RTIF) commands

Operating company personnel use the reset terminal interface (RTIF) as an interface to the DMS SuperNode or DMS SuperNode SE switch. The RTIF display for a switch with XA-Core provides two types of interfaces as follows.

- an interface to start resets and restarts on the switch
- an interface to the serial input/output (IO) resource of the switch

The RTIF can be an interface to start resets and restarts on the switch. The RTIF display can have command entries that start boots, cold restarts, reload restarts, and warm restarts on the switch.

The RTIF can be an interface to the serial input/output (IO) resource of the switch. The RTIF display can have single-line command entries to a MAP

display. The single-line command entry can access the command interpreter (CI) and each MAP level of the XA-Core. The RTIF display cannot view the complete MAP level display. The RTIF display has a single-line command entry to the MAP levels of XA-Core.

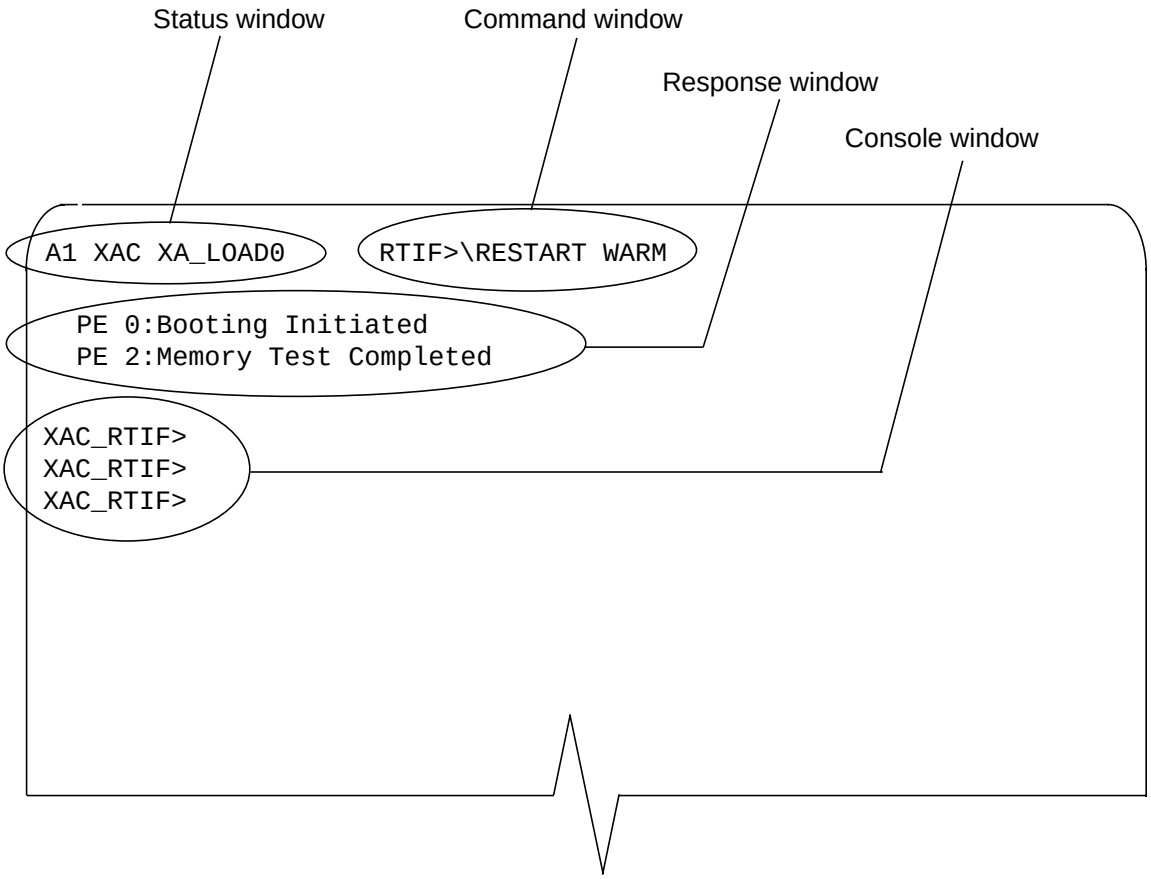
The commands and maintenance activities of the RTIF are for operating company personnel with experience. Wrong use of RTIF commands can interrupt subscriber service.

The RTIF display for XA-Core has four windows as follows.

- status window
- command window
- response window
- console window

Figure 5-17 shows an example of a display of an RTIF screen for XA-Core.

Figure 5-17 Example of an RTIF display for XA-Core



The status window shows the following.

- status of the operational state of the switch (displays a flashing event code)
- identity of the RTIF for XA-Core (displays XAC)
- name of the software load that runs on the XA-Core

The command window and the response window are for the last entered command. The command window echoes the last entered command from the console window. The response window displays the switch response to the last entered command.

The console window displays console data sent by the firmware and the software. The console window has no data related to an RTIF command. When operating company personnel enter an RTIF command in the console window, the command text moves to the command window. The console window changes to a full screen window when operating company personnel enter an RTIF command \STATUS.

This section describes the RTIF commands for XA-Core. RTIF commands begin with a \ (*back slash*) character. Perform the following commands at an RTIF terminal.

\ (Backslash)

The \ (back slash) command allows operating company personnel to check for RTIF activity. The operating company personnel enters the \ (back slash) with no other text or data to check for RTIF activity. This command also enables the status window, command window, and the response window of the RTIF screen display after use of the \STATUS command.

\BOOT

This command forces a reset which loads an image from a specified small computer system interface (SCSI) device.

Table 5-5 shows the \BOOT command parameters.

Table 5-5 \BOOT command parameters (Sheet 1 of 2)

Parameter	Description
<slot_number>	Boots from a packlet in the IOP card of the indicated slot number of the XA-Core shelf.
<front_or_rear>	Boots from a packlet in the IOP card on the front or rear side of the XA-Core shelf.
<upper_or_lower>	Boots from a packlet in the upper or lower slot of the IOP card.

Table 5-5 \BOOT command parameters (Sheet 2 of 2)

Parameter	Description
default	Automatic boot when no parameters used.

\CLEAR

This command clears the display screen.

\ENABLE

This command enables specified functions of the RTIF.

\GET

This command removes the RTIF console from the processor element (PE) or low level maintenance (LLM) user. This command instructs the RTIF console to run the input output processor (IOP) firmware command interpreter (FWCI).

\HELP

This command displays information to use an RTIF command or a list of RTIF commands.

Table 5-6 \HELP command parameters

Parameter	Description
<rtif_command>	Displays information to use the RTIF command.

Note: The default parameter displays a list of RTIF commands.

\LOCBAUD

This command sets the baud rate of the local port of the RTIF packlet.

Table 5-7 \LOCBAUD command parameters

Parameter	Description
<baud_rate>	Sets baud rate of the local port of the RTIF packlet.

\NO

This command provides negative acknowledgment to an approval prompt for a reset command.

\OVERIDE

This command indicates the beginning of a reset command.

\PUT

This command passes the RTIF console back to the original user. The original user is either for the processor element (PE) or the low level maintenance (LLM).

\QUERY

This command queries the RTIF parameters.

\REMBAUD

This command sets the baud rate of the remote port of a RTIF packlet.

Table 5-8 \REMBAUD command parameters

Parameter	Description
<baud_rate>	Sets baud rate of the remote port of a RTIF packlet.

\RESET

This command begins a reset for XA-Core.

Table 5-9 \RESET command parameters

Parameter	Description
<RESTART>	Begins a reset with a restart.
<FWCI>	Begins a reset from the firmware command interpreter (FWCI).
default	Default is a restart.

\RESTART

This command begins a restart for XA-Core.

Table 5-10 \RESTART command parameters (Sheet 1 of 2)

Parameter	Description
<WARM>	One-to-one calls in process remain in process and temporary data store clears.
<COLD>	Calls in process remain in process until the peripherals start again. When peripherals start again, the switch lets go of calls in process. Temporary data store clears.

Table 5-10 \RESTART command parameters (Sheet 2 of 2)

Parameter	Description
<RELOAD>	Calls in process remain in process until the peripherals start again. When peripherals start again, the switch lets go of calls in process. Temporary and permanent data store clears. Data store RAM clears and deallocates.
<RTIF>	Restores firmware of RTIF. XA-Core not changed.

Note: The default parameter is a warm restart.

\SELF TEST

This command displays the results of background tests that run continuously on the RTIF.

\STATUS

This command disables the status window, command window, and the response window of the RTIF screen display. This command changes the console window to full screen. The command \ (back slash) enables the status window, command window, and the response window of the RTIF screen display.

\YES

This command provides positive acknowledgment to an approval prompt for a reset command.

6 Cards and packlets

This chapter describes the cards and packlets for the eXtended Architecture Core (XA-Core) of the DMS SuperNode and DMS SuperNode SE switches. This chapter describes the cards and packlets in numeric order. Refer to the *XA-Core Reference Manual*, 297-8991-810, for additional information on XA-Core cards and packlets.

DMS SuperNode and SuperNode SE XA-Core card and packlets descriptions

The XA-Core shelf has cards and packlets located in front and back slots of the XA-Core shelf. The cards and packlets are field replaceable units (FRU). Each of the cards and packlets has a product engineering code (PEC) for an identifier.

A card is a circuit pack that inserts into a slot on the XA-Core shelf. XA-Core has three basic types of cards:

- memory cards
- processor cards
- power interface cards

The communication link between the cards is the extended architecture interconnect (XAI). The XAI is a network of links found in the midplane. The midplane is a printed circuit board (PCB) that is like a backplane. The XA-Core shelf has the midplane located in the center of the shelf between the front and back slots for cards and packlets. The midplane is a non-contact midplane. A non-contact midplane has electromagnetic field couplers and connector pins for card connections to the midplane. These couplers connect through the effect of an electromagnetic field from one pair of circuit tracks to another pair. A voltage on a transmit pair of circuit tracks induces a small voltage pulse on a receive side of another track pair. Each coupler has a small transmitter and antenna embedded in the midplane circuit tracks. The non-contact midplane allows card insertion and removal in a live state of electrical power.

A packlet is a circuit pack that inserts into a slot on the input/output processor (IOP) card. XA-Core has two basic types of packlets:

- mass storage packlets
- external communication packlets.

The communication link between a packlet and the IOP card that contains the packlet, is a peripheral component interconnect (PCI) bus.

Table 6-1 lists the XA-Core cards and packlets.

Table 6-1 XA-Core cards and packlets (Sheet 1 of 2)

PEC	Title	SN	SNSE
NTLX02AA	256-Mbyte processor element (PE) card	Y	Y
NTLX02CA	256-Mbyte processor element (PE) card	Y	Y
NTLX03AA	One-slot Input/output processor (IOP) card	Y	Y
NTLX03AB	One-slot Input/output processor (IOP) card	Y	Y
NTLX03BA	Two-slot Input/output processor (IOP) card	Y	Y
NTLX03BB	Two-slot Input/output processor (IOP) card	Y	Y
NTLX05AA	OC-3 two-port interface packlet	Y	Y
NTLX05AB	OC-3 two-port interface packlet	Y	Y
NTLX05BA	OC-3 AMDI two-port interface packlet	Y	Y
NTLX06AA	4-Gbyte disk drive packlet	Y	Y
NTLX06AB	8-Gbyte disk drive packlet	Y	Y
NTLX07AA	Digital audio tape (DAT) tape drive packlet	Y	Y
NTLX08AA	RS232 serial interface packlet	Y	Y
NTLX09AA	Ethernet interface packlet	Y	Y
NTLX12AA	Shelf interface module (SIM) card	Y	Y
NTLX14CA	384-Mbyte shared memory (SM) card	Y	Y

Table 6-1 XA-Core cards and packlets (Continued) (Sheet 2 of 2)

PEC	Title	SN	SNSE
NTLX20AA	Slot filler card	Y	Y
NTLX20BA	Terminating filler card	Y	Y

NTLX02 processor element (PE) card

The NTLX02 processor element (PE) card provides the XA-Core with a computing device that has fault detection and a spare. XA-Core capability to process is scalable.

A reduced instruction set computing (RISC) PowerPC (PPC) 604 processor is the base for PE design. The PPC 604 operates at 166.67 MHz. The PPC bus operates at 66 MHz.

The number of PE cards depends on the processing power required. In CSP15, the XA-Core shelf supports the following PE configurations: 2+1, 3+1, and 5+1.

- In the 2+1 configuration, there are three PE circuit packs. All three PE circuit packs operate in a load sharing mode.
- In the 3+1 configuration, there are four PE circuit packs. All four PE circuit packs operate in a load sharing mode.
- In the 5+1 configuration, there are six PE circuit packs. All six PE circuit packs operate in a load sharing mode.

> ***Note:*** In each PE configuration, the spare processing power is the equivalent of one PE unit. A PE unit is the processing power of a PE circuit pack that uses PowerPC 604 processors. The NTLX02AA and the NTLX02CA use such processors.

Each PE card operates in the XA-Core in the simplex state. The PE card maintains a state of service separate from other PE cards. Operating company personnel can remove and replace any PE card for upgrade or repair when required. Removal of a PE card requires the switch to keep enough resources to process. If the switch keeps enough resources, removal of a PE card can not cause an outage or interruption in the switch.

The NTLX02 card provides the following functions:

- PPC 604 RISC processor
- 32-Kbyte instruction and data caches

- 256-Mbyte local synchronous dynamic random access memory (SDRAM) for program store
- electrically-erasable programmable read-only memory (EEPROM)

NTLX02AA PE card

The NTLX02AA PE card provides computing capacity and fault detection for shared memory (SM) and the extended architecture interconnect (XAI).

Description of functions

Two 166.67-MHz, PPC 604 superscalar RISC processors provide the computing capacity.

The two PPC 604 buses can operate in three different modes:

- duplex
- simplex
- inactive

The duplex mode is the normal operation. During normal operation, identical tasks and transactions operate on both buses at the same time. This duplex mode provides fault detection capability. If a bus signal mismatch occurs, the PE card separates from the remainder of the system.

The simplex mode is for diagnostic purposes only.

The inactive mode is for when the system has detected a fault. The processors cannot access the buses. The processors remain in the inactive mode until the PE module resets. The inactive mode prevents errors from entering and transmitting through the XA-Core module.

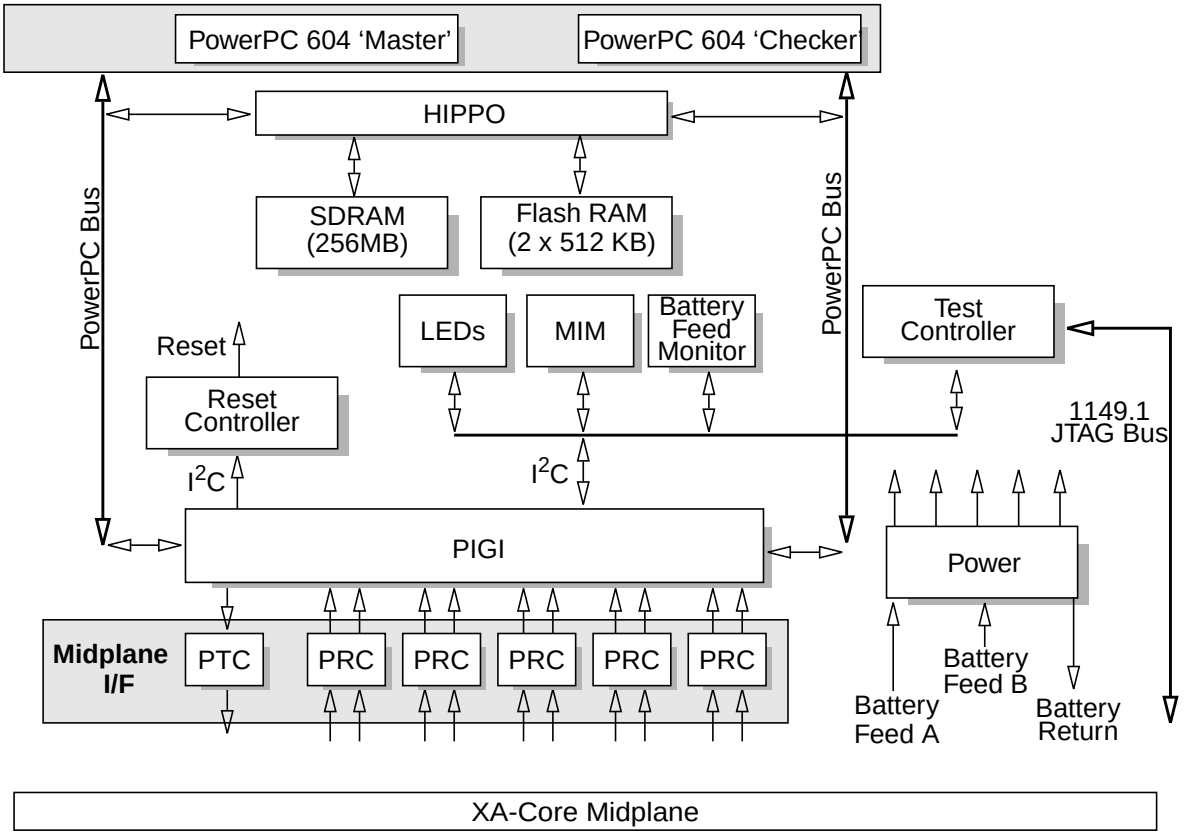
Circuits by function

The NTLX02AA has circuits for functions as follows:

- processor circuit
- test circuit
- power circuit
- XAI interface (XAI I/F) circuit

Figure 6-1 on page 6-5 shows a block diagram of the NTLX02AA card.

Figure 6-1 NTLX02AA block diagram



Processor circuit

Two PPC 604ev processors provide computing capability for the PE. The processors operate using a master/monitor design to provide fault detection. Both processors receive identical data and their output responses match to make sure that both processors operate correctly. The HIPPO, an enhanced high-speed instruction prefetcher path optimizer, monitors the operation of the two CPUs. The HIPPO is an application specific integrated circuit (ASIC).

The processors support a 64-bit external data bus with single-pulse and burst transfer. A 32-bit address bus allows for an address pipeline. Synchronous dynamic random access memory (SDRAM) has 256 Mbytes.

Test circuit

The test circuit manages structure tests for the PE card. Primary functions of the test circuit include:

- control IEEE 1149.1 test buses to perform interconnect tests, logic built-in self test (BIST), array BIST and seed-and-signature tests
- allow software or firmware to start structure tests through a hard reset at the hardware level
- pass control over structure tests to an external test master on the IEEE 1149.5 bus
- allow communication to the reset master for reset requests that originate from the IEEE 1149.5 module test and maintenance (MTM) bus
- control of light emitting diodes (LED)
- allow an external test master on the IEE 1149.5 bus to read the intelligent test master (ITM) slot
- configure again the scan chain on the PE to bypass the PTC/PRCs
- find the PPC IEEE 1149.1 port from the scan chain for common on-chip processor (COP) access
- access the module information memory (MIM) for module fault logs

Power circuit

The power circuit includes the following components:

- peripheral functionality module (PFM)
- local filter circuit
- decoupling capacitors
- point of use power supply (PUPS)

The PFM gathers the two battery input feeds to the power supply into an OR logic diode circuit. This OR logic diode circuit provides connection redundancy and protects the PE against total power failure that originates from the input rails. Power feed detection circuits report any power interruptions to software.

The PFM also provides local differential and common mode filtering to suppress noise that originates from the power feeds. The PFM also filters noise which can originate from a PE that has faults.

Decoupling capacitors limit current surges related to power-up.

Three PUPS provide power to the low noise analog circuit, to the PPC core logic and to all other card circuits. A +3.3-V, 33-W PUPS supplies power to the low noise analog circuit. A +2.5-V, 25-W PUPS supplies power to the PPC

core logic. A +3.3-V, 50-W PUPS supplies power to all other card circuits. Analog output requires a filter so that voltage noise reduces to 10 mV peak-to-peak. The PE without the PUPS dissipates about 66 W.

XAI interface (XAI/IF) circuit

A controller makes the midplane clear to the core PE logic and determines read/write access to shared memory (SM). The midplane interface uses five pulse receiver chips (PRC) and one pulse transmitter chip (PTC). The PRC and PTC allow communication with the non-contact midplane.

Each PRC provides two dedicated receive links to two of the shared memory slots. Each of the two PRC links receive a 4-Gbit/s data stream from a SM card by the XAI. The PRC then demultiplexes and relays the data stream to the PE interface to Gigabit interconnect (PIGI). The PIGI is an ASIC.

The PE transmits a 2-Gbit/s data stream over a 250-MHz bus to the PTC. The signal multiplexes and relays to the XAI over a 500-MHz bus. The PTC has a 1-GHz reference clock frequency.

NTLX02CA PE card

The NTLX02CA is the only version of the PE card supported in releases after CSP13. It provides computing capacity and fault detection for shared memory (SM) and the extended architecture interconnect (XAI).

Description of functions

Two 166.67-MHz, PPC 604 superscalar RISC processors provide the computing capacity.

The two PPC 604 buses can operate in three different modes:

- duplex
- simplex
- inactive

The duplex mode is the normal operation. During normal operation, identical tasks and transactions operate on both buses at the same time. This duplex mode provides fault detection capability. If a bus signal mismatch occurs, the PE card separates from the remainder of the system.

The simplex mode is for diagnostic purposes only.

The inactive mode is for when the system has detected a fault. The processors cannot access the buses. The processors remain in the inactive mode until the PE module resets. The inactive mode prevents errors from entering and transmitting through the XA-Core module.

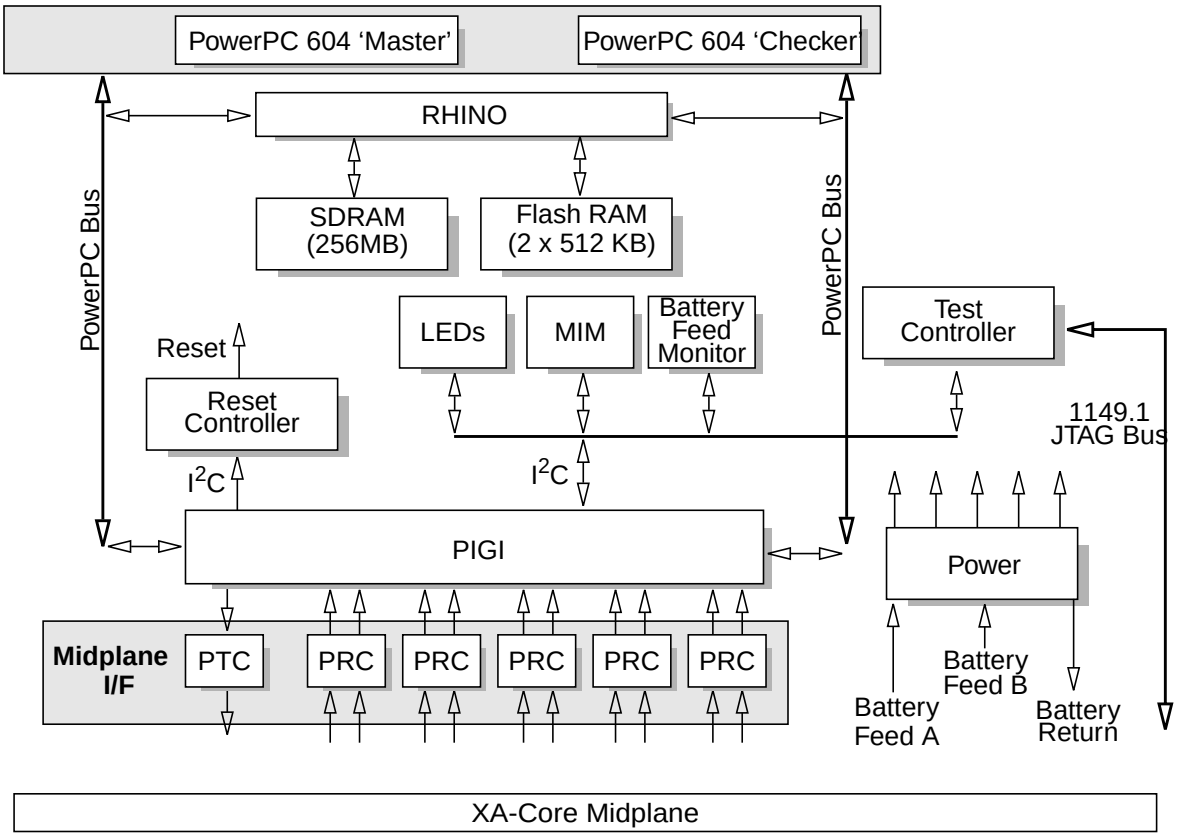
Circuits by function

The NTLX02CA has circuits for functions as follows:

- processor circuit
- test circuit
- power circuit
- XAI interface (XAI I/F) circuit

Figure 6-2 on page 6-8 shows a block diagram of the NTLX02CA card.

Figure 6-2 NTLX02CA block diagram



Processor circuit

Two PPC 604ev processors provide computing capability for the PE. The processors operate using a master/monitor design to provide fault detection. Both processors receive identical data and their output responses match to make sure that both processors operate correctly. The RAM-on-chip HIppo New Optimizations (RHINO), an enhanced high-speed instruction prefetcher

path optimizer (HIPPO), monitors the operation of the two CPUs. The RHINO is an application specific integrated circuit (ASIC).

The processors support a 64-bit external data bus with single-pulse and burst transfer. A 32-bit address bus allows for an address pipeline. Synchronous dynamic random access memory (SDRAM) has 256 Mbytes.

Test circuit

The test circuit manages structure tests for the PE card. Primary functions of the test circuit include:

- control IEEE 1149.1 test buses to perform interconnect tests, logic built-in self test (BIST), array BIST and seed-and-signature tests
- allow software or firmware to start structure tests through a hard reset at the hardware level
- pass control over structure tests to an external test master on the IEEE 1149.5 bus
- allow communication to the reset master for reset requests that originate from the IEEE 1149.5 module test and maintenance (MTM) bus
- control of light emitting diodes (LED)
- allow an external test master on the IEE 1149.5 bus to read the intelligent test master (ITM) slot
- configure again the scan chain on the PE to bypass the PTC/PRCs
- find the PPC IEEE 1149.1 port from the scan chain for common on-chip processor (COP) access
- access the module information memory (MIM) for module fault logs

Power circuit

The power circuit includes the following components:

- peripheral functionality module (PFM)
- local filter circuit
- decoupling capacitors
- point of use power supply (PUPS)

The PFM gathers the two battery input feeds to the power supply into an OR logic diode circuit. This OR logic diode circuit provides connection redundancy and protects the PE against total power failure that originates from the input rails. Power feed detection circuits report any power interruptions to software.

The PFM also provides local differential and common mode filtering to suppress noise that originates from the power feeds. The PFM also filters noise which can originate from a PE that has faults.

Decoupling capacitors limit current surges related to power-up.

Three PUPS provide power to the low noise analog circuit, to the PPC core logic and to all other card circuits. A +3.3-V, 33-W PUPS supplies power to the low noise analog circuit. A +2.5-V, 25-W PUPS supplies power to the PPC core logic. A +3.3-V, 50-W PUPS supplies power to all other card circuits. Analog output requires a filter so that voltage noise reduces to 10 mV peak-to-peak. The PE without the PUPS dissipates about 66 W.

XAI interface (XAI/IF) circuit

A controller makes the midplane clear to the core PE logic and determines read/write access to shared memory (SM). The midplane interface uses five pulse receiver chips (PRC) and one pulse transmitter chip (PTC). The PRC and PTC allow communication with the non-contact midplane.

Each PRC provides two dedicated receive links to two of the shared memory slots. Each of the two PRC links receive a 4-Gbit/s data stream from a SM card by the XAI. The PRC then demultiplexes and relays the data stream to the PE interface to Gigabit interconnect (PIGI). The PIGI is an ASIC.

The PE transmits a 2-Gbit/s data stream over a 250-MHz bus to the PTC. The signal multiplexes and relays to the XAI over a 500-MHz bus. The PTC has a 1-GHz reference clock frequency.

NTLX03 input/output processor (IOP) circuit pack

The NTLX03 input/output Processor (IOP) card supports large data storage and communication in the XA-Core.

IOP cards works with circuit packs called packlets that plug into the IOP cards. XA-Core packlets are for two basic types of services as follows:

- communication service
- large data storage service

Communication service is on the following packlet types:

- core-MS interconnect (CMIC) packlets

  - NTLX05AA/AB OC-3 two-port interface packlet

- remote terminal interface (RTIF) packlets

  - NTLX08AA RS232 serial interface packlet

  - NTLX08AB RS232 serial interface packlet

Network service is on the following packlet types:

- core-ATM interconnect (AMDI) packlet
  - NTLX05BA OC-3 two-port AMDI interface packlet
- core-LAN hub/IP network interconnect (ETHR) packlet
  - NTLX09AA Ethernet interface single-port packlet

Large data storage service is on the following packlet types:

- tape packlets
  - NTLX07AA digital audio tape (DAT) drive packlet
- disk drive packlets
  - NTLX06AA 4-Gbyte disk drive packlet
  - NTLX06AB 8-Gbyte disk drive packlet

There are four types of IOP cards as follows:

- NTLX03AA single-width IOP card
- NTLX03AB single-width IOP card that allows for hot insertion of packlets
- NTLX03BA double-width IOP card
- NTLX03BB double-width IOP card that allows for hot insertion of packlets

The NTLX03AA/AB is a single-width IOP card that installs in a single slot on the back side of the XA-Core shelf. The NTLX03AA accepts only the following:

- CMIC packlets
  - NTLX05AA OC-3 two-port interface packlet
  - NTLX05AB OC-3 two-port interface packlet, capable of firmware downloading
- RTIF packlets
  - NTLX08AA RS232 serial interface packlet
- AMDI packlets
  - NTLX05BA OC-3 two-port interface packlet
- ETHR packlets
  - NTLX09AA Ethernet interface single-port packlet

The NTLX03BA is a double-width IOP card that installs in two slots on the front side of the XA-Core shelf. The NTLX03BA accepts only the following:

- tape packlets
  - NTLX07AA digital audio tape (DAT) drive packlet
- disk packlets
  - NTLX06AA 4-Gbyte disk drive packlet
  - NTLX06AB 8-Gbyte disk drive packlet

NTLX03AA/AB single-width IOP card

The NTLX03AA/AB single-width IOP card supports communication services. The NTLX03AA/AB card inserts into a single XA-Core shelf slot. The NTLX03AA/AB card uses CMIC, RTIF, AMDI, or ETHR packlets.

Description of functions

The NTLX03AA/AB uses five pulse receiver chips (PRC) and one pulse transmitter chip (PTC) to link with the shared memory (SM) cards. The PRC and the PTC link with the SM cards over the XA-Core midplane.

From the midplane, each PRC receives two 4-Gbit/s links from two SM cards. Each PRC also receives a 500-MHz differential clock link. Each of the 4-Gbit/s links includes four 1-Gbit/s differential pairs. For each 4-Gbit/s link, data demultiplexes to eight 500-Mbit/s differential pairs. The demultiplexed data transmits at differential-PECL compatible levels, with a 500-Mbit/s differential frame signal and a 250-MHz differential clock signal.

The one PTC transmits over the midplane to all of the SM cards. The PTC can transmit to 10 SM cards. The PTC multiplexes four 500-Mbits/s differential pairs. The PTC transmits two 1-Gbits/s differential pairs and a 500-MHz differential clock signal.

From the midplane, each PRC receives two 4-Gbit/s links from two SM cards. Each of the 4-Gbit/s links include four 1-Gbit/s differential pairs added to a 500-MHz differential clock signal. For each 4-Gbit/s link, data demultiplexes to eight 500-Mbit/s differential pairs. These differential pairs transmit at compatible levels of positive emitter-coupled logic (PECL). that is differential. The differential pairs also transmit with a 500-Mbit/s differential frame signal and a 250-MHz differential clock.

The input/output signals transmit over a 33-MHz internal bus of the IOP card. Local logic provides low-level control and monitoring to filter the internal IOP interrupts and increase performance.

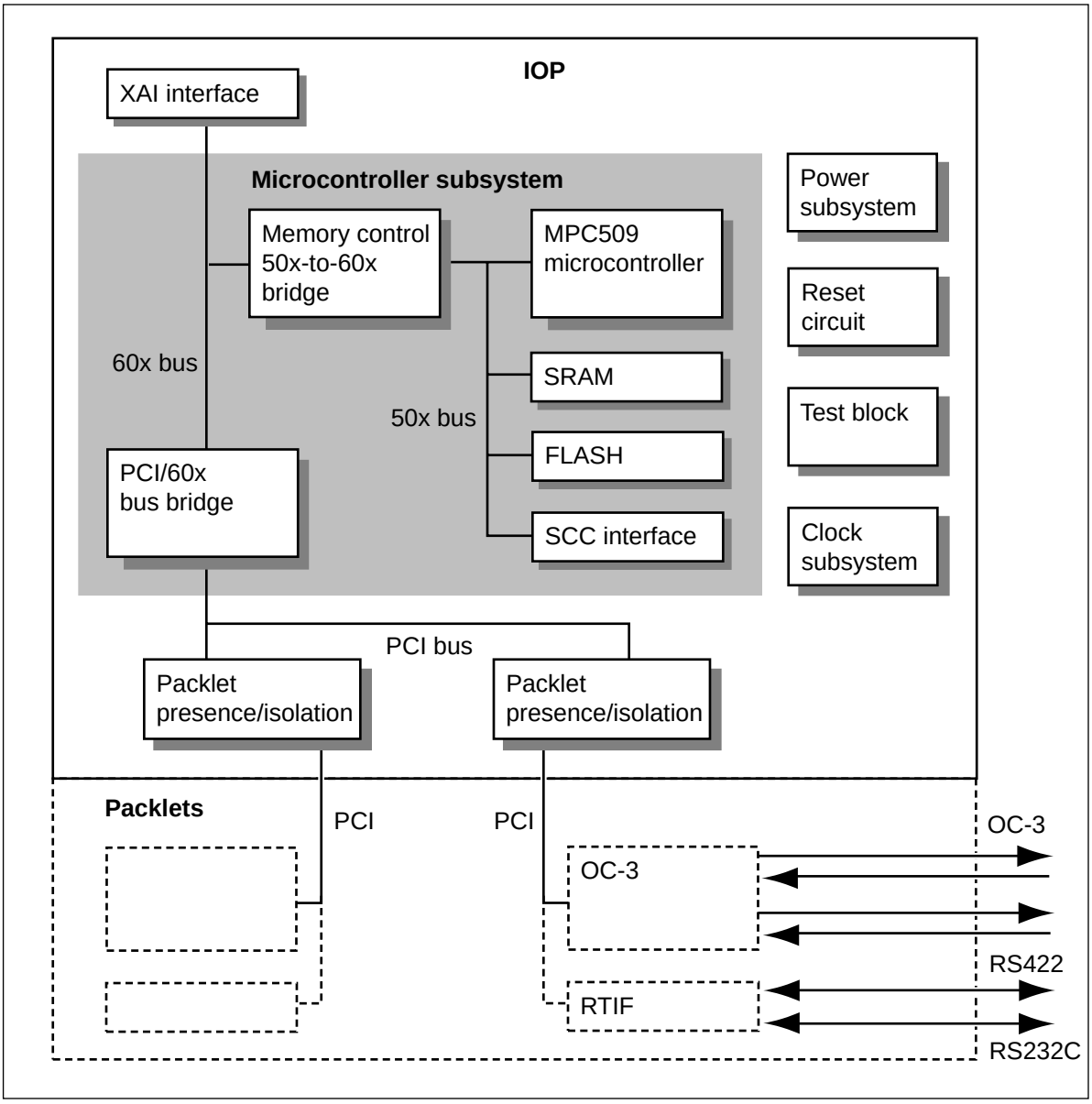
Circuits by function

The NTLX03AA/AB includes function circuits as follows:

- XAI interface (XAI I/F) circuit
- micro-controller circuit
- reset circuit
- clock circuit
- test circuit
- power circuit
- packlet presence/isolation circuit
- packlets

Figure 6-3 on page 6-14 shows a block diagram of the NTLX03AA/AB card.

Figure 6-3 NTLX03AA/AB block diagram



XAI interface (XAI I/F) circuit

The extended architecture interface (XAI) circuit is a controller to the midplane. The XAI circuit uses an application specific integrated circuit (ASIC) called a PE interface to Gigabit interconnect (PIGI). A controller makes the midplane clear to the core IOP logic and determines read/write access to the shared memory (SM). The midplane interface uses five pulse receiver chips (PRC) and one pulse transmitter chip (PTC) to communicate with the non-contact midplane.

Micro-controller circuit

The micro-controller circuit provides local control and monitor of IOP hardware. The micro-controller circuit is an MPC509 ASIC. The micro-controller circuit filters interrupts that originate from the packlets to improve performance. The micro-controller circuit also performs low-level initialization and maintenance for the IOP and some packlet types.

Other circuits found in the micro-controller circuit are as follows.

- Memory control 509-to-604 bridge circuit is an ASIC called the roadrunner. The roadrunner connects the MPC509 micro-controller to the PCI /604 bus bridge.
- PCI/604 bus bridge circuit is an ASIC called the coyote. The coyote connects the 32-bit wide PCI bus to the 64-bit wide PPC 604 bus.
- Static random access memory (SRAM) memory is for data store and for memory copied from the flash memory.
- Flash memory provides memory space for the MPC509 micro-controller. Flash memory also provides memory for in-service firmware upgrade from another card (PE card).
- Serial communication controller (SCC) interface circuit is for serial communications of firmware debug and development activities. The SCC interface circuit connects from the roadrunner to an SCC add-on card.

Reset circuit

The reset circuit captures and analyzes reset requests from both local and remote sources. The circuit responds by an action to ignore the request or to issue a hard or soft reset to the packlets. A soft reset causes a packlet to start again and to continue the activity before reset. A hard reset causes a re-initialization of IOP memory and packlet processes.

Clock circuit

The clock circuit provides steady clock signals for the IOP and packlets. The clock circuit uses the following:

- an MPC946 complementary metal oxide semiconductor(CMOS) clock driver for low voltage
- a 33-MHz crystal oscillator that is external

The 33-MHz signal transmits to the following:

- the micro-controller circuit
- the PE interface to Gigabit interconnect (PIGI)
- the peripheral component interconnect (PCI) components/packlets

The 33-MHz signal also divides down to 16.67 MHz to provide a clock to:

- the intelligent test controller (ITC)
- the reset circuit

Test circuit

The test circuit manages structure tests on the IOP. The test circuit provides a link to the Institute of Electrical and Electronics Engineers (IEEE) 1149.5 test bus. The IEEE 1149.5 test bus is part of the XA-Core. The test circuit generates IEEE 1149.1 scan chains to test the IOP. Two ways to control the test circuit are:

- When the IOP is out of service, a test device on the IEEE 1149.5 test bus can send test commands. The test commands start IEEE 1149.1 scan tests of the complete IOP.
- During office operation, the test circuit performs a scan test on a part of the IOP logic. The scan test helps identify and separate IOP components that have faults.

The test circuit also accesses the module information memory (MIM) located on the IOP, packlets, processing element (PE) and SM. The hardware stores fault information in the MIM.. The test circuit, the printed circuit pack (PCP) firmware, and the system software share MIM control.

Power circuit

The power circuit provides power to the IOP. Two point-of-use power supplies (PUPS) have an input voltage range of 36-75 V dc. The PUPS generate 25-W, 3.3-V digital and analog outputs from battery backplane feeds. The analog output uses a filter to reduce voltage noise to 10 mV peak-to-peak. The location of the PUPS is on the IOP mezzanine card.

The battery input feeds to the power supply connect by an OR logic diode circuit. This OR logic diode circuit provides connection redundancy and protects the IOP against total power failure that originates from the input rails. Power feed detection circuits report any power interruptions to software. Power to the packlets comes from the same battery feeds. Each packlet receives a battery feed and has a PUPS that regulates the packlet's voltage and power requirements.

Packlet presence/isolation circuit

The packlet presence/isolation circuit provides event notification, such as packlet removal and insertion, to the micro-controller circuit. The presence/isolation circuit also separates a packlet's PCI bus from the other circuits of the IOP. This separation allows hot insertion or removal of the packlet from the IOP.

Field effect transistor (FET) switches, connected in series with the packlet PCI bus, provide the packlet isolation mechanism. The switches are normally in a turned-on state, limiting their effect to that of a 6-12 ohm resistor. When the switches are in a turned-off state, the packlet appears to be a high impedance (infinite resistance) load to the IOP. This high impedance load to the IOP separates the packlet. FET switches are in a turned-off state in the event of packlet failure.

Packlets

The various types of packlets that install in NTLX03AA/AB IOP cards provide CMIC services, RTIF communication services, ATM services, or IP services.

The CMIC packlet provides a duplex OC-3 link and activates the asynchronous transfer mode (ATM) physical layer. CMIC packlets can be installed in IOP cards in shelf positions 4R and 15R.

The RTIF packlet provides a remote terminal port to monitor XA-Core processes from an operations, administration, and maintenance (OAM) point of view. RTIF packlets can be installed in IOP cards in shelf positions 4R and 15R.

The AMDI packlet provides an interface to the ATM edge switch. AMDI packlets can be installed in IOP cards in shelf positions 5R, 6R, 13R, and 14R.

The ETHR packlet provides the connection between the XA-Core shelf and the LAN hub IP network. ETHR packlets can be installed in IOP cards in shelf positions 5R, 6R, 13R, and 14R.

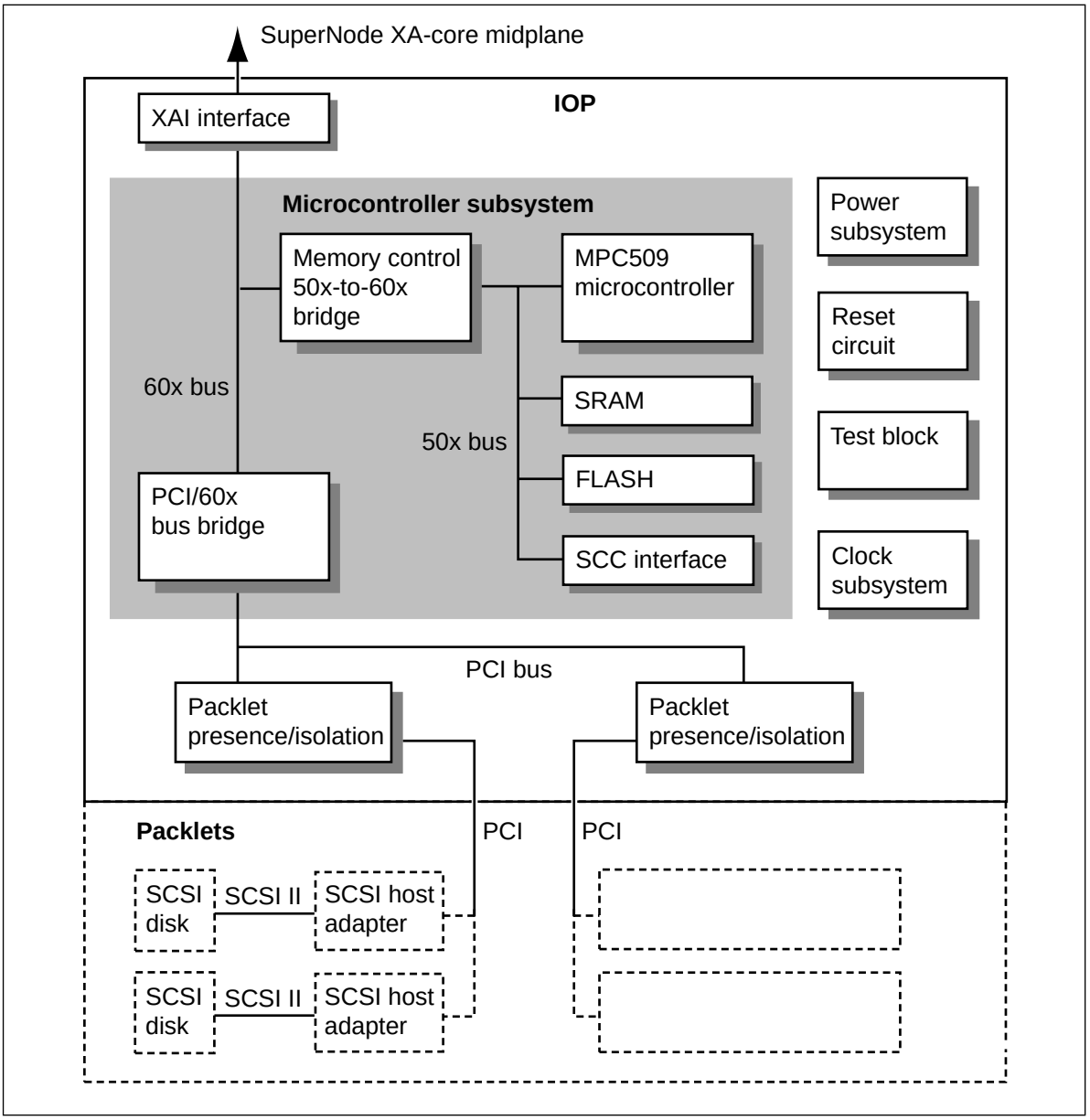
NTLX03BA/BB double-width IOP card

The NTLX03BA/BB double-width IOP card is like the NTLX03AA/AB except for the following:

- An NTLX03BA/BB card inserts into two slots on the front of the XA-Core shelf. The two slots for an NTLX03BA/BB card are side by side. An NTLX03AA/AB card inserts into a single slot on the back (or rear) of the XA-Core shelf.
- NTLX03BA/BB cards accommodate a DAT tape drive packlets or disk drive packlets, rather than CMIC, RTIF, AMDI, or ETHR packlets.

Figure 6-4 on page 6-18 shows a block diagram of the NTLX03BA/BB card.

Figure 6-4 NTLX03BA/BB block diagram



Packlets

The packlet pairs of the NTLX03BA/BB IOP card provide disk and tape storage services.

The XA-Core shelf has a minimum of two DAT tape drive packlets. The two DAT tape drive packlets provide storage capacity that ranges between 1-4 Gigabytes. File processor (FP) applications use the DAT drives.

The XA-Core shelf has a minimum of two disk drive packlets. The disk drives provide 4 or 8 Gigabytes of storage capacity. Software can operate the disks in simplex mode or as shadowed sets to support fault tolerance. Normally the disks operate in shadowed sets. The disks are a 8.89 cm x 14.61 cm (3.5 in. x 5.75 in.), 2.54-cm (one in.) high form component. The disk data path is 16-bits wide. The disk data path has a repeated data transfer rate of 8 MBytes/s. The disk data path has a peak data transfer rate of 20 MBytes/s.

NTLX05 OC-3 two-port interface packlet

The NTLX05 OC-3 two-port interface packlet provides core MS interconnect (CMIC) service through an optical carrier level 3 (OC-3) signal. The CMIC service is on an asynchronous transfer mode (ATM) link. The service provided by the NTLX05 is a CMIC link between the XA-Core and the message switch (MS). At the MS, the CMIC link connects to an NT9X63AA/AB OC-3 ATM paddle board.

The NTLX05 packlet inserts into an NTLX03AA/AB IOP card. The location of the NTLX05 packlet and the NTLX03AA/AB IOP card, is in a back slot of the XA-Core shelf. The NTLX05AA/AB packlet has a mezzanine card included in the packlet assembly to make a small packlet assembly.

NTLX05AA/AB OC-3 two-port interface packlet

The NTLX05AA/AB OC-3 two-port interface packlet is the XA-Core interface for a CMIC link. Another name for the NTLX05AA/AB is the CMIC packlet. This CMIC packlet provides a duplex OC-3 link at 155.52 Mbits/s between the XA-Core and the MS.

The NTLX05AA/AB CMIC packlet connects to the IOP card through a peripheral component interconnect (PCI) bus. The PCI bus is a 32-bit multiplexed path for data transfer.

The NTLX05AB is identical to the NTLX05AA packlet except it has the added capability to have its firmware downloaded and changed by the DMS-100.

Description of functions

The NTLX05AA/AB provides the following functions:

- termination of duplex OC-3 links of the synchronous optical network (SONET)
- optical to electrical conversion of OC-3 to synchronous transport signal 3 (STS-3)
- termination of the ATM layer (cell transmission and reception)
- termination of the AAL5 segmentation and re-assembly sublayer (AAL5-SAR)

- termination of the AAL5 common part convergence sublayer (AAL5-CPCS)
- reception of a dedicated virtual channel that contains time of day (TOD) information derived from the DMS bus links of the MS
- provide a 32-bit multiplexed PCI bus to connect to an IOP card
- transfer to the MS the out-of-band (OOB) messages such as reset

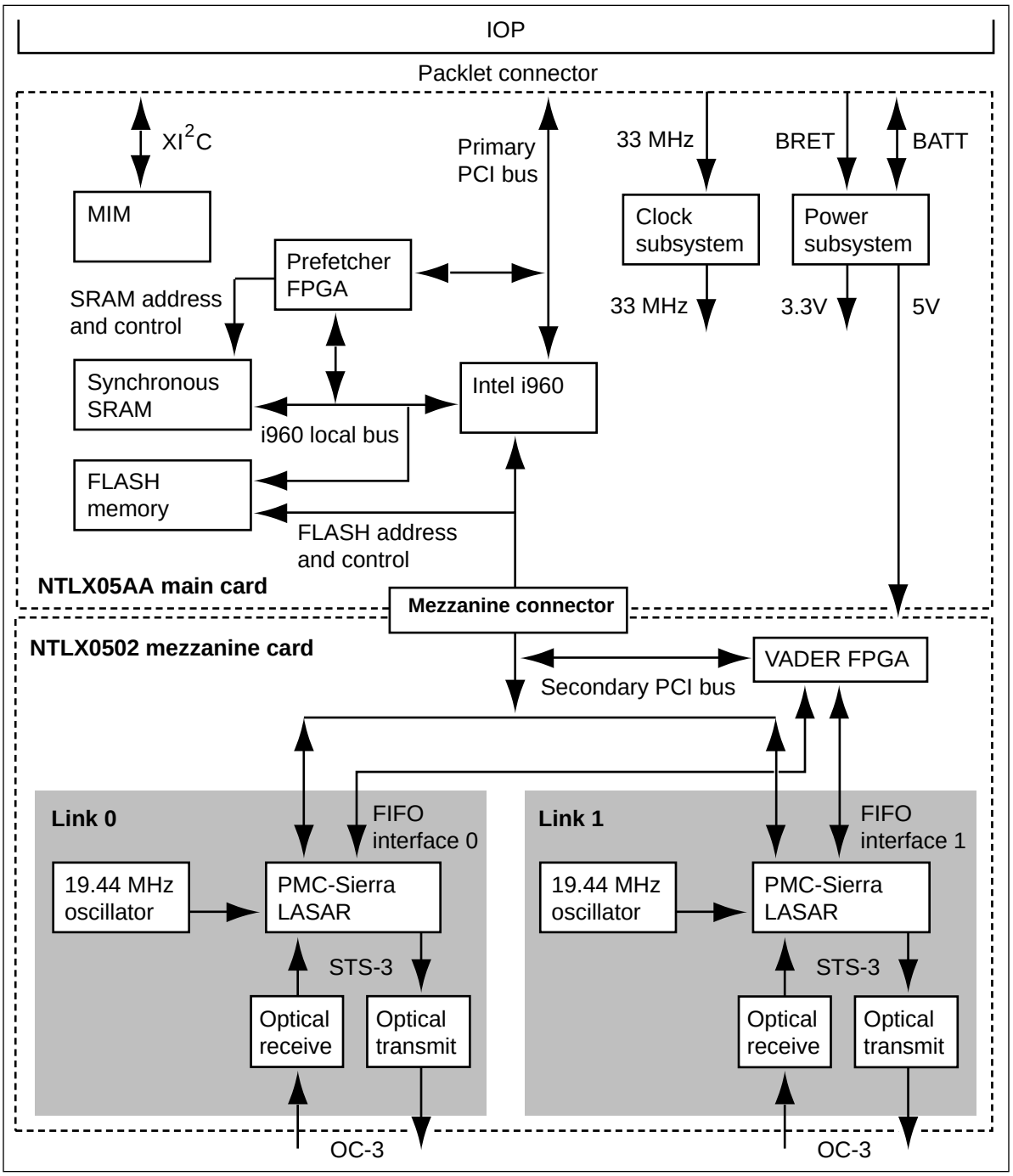
Circuits by function

The NTLX05AA includes the following circuits by function:

- optical transceiver (transmitter-receiver) circuits
- ATM adapter circuits for peripheral component interconnect (PCI)
- microprocessor circuit
- time of day (TOD) field programmable gate array (FPGA) circuit
- time of day (TOD) circuit
- out of band (OOB) circuit
- module information memory (MIM) circuit
- point-of-use power supply (PUPS) circuit

Figure 6-5 on page 6-21 shows a block diagram of the NTLX05AA/AB CMIC packlet.

Figure 6-5 NTLX05AA/AB block diagram



Optical transceiver circuits

The optical interface on the NTLX05AA/AB packlet is a 155.52-Mb/s multimode fiber transceiver. The NTLX05AA/AB packlet has two optical transceivers for links 0 and 1. The transceiver provides a SONET OC-3 link

for distances up to 2000 m with 62.5/125-mm multimode fiber-optic cables. The SONET OC-3 link of fiber-optic cable between the XA-Core and the MS is shorter than the 2000 m capability. The maximum distance of fiber-optic cable between the XA-Core packlet and MS paddle board is 100 m. The circuit includes a duplex subscriber connector (SC) interface.

The transceiver is a short reach (SR) class of SONET optical interface. The wide application classes of SONET optical interfaces include the following:

- short reach (SR) are normally for connections between sites with interconnection distances up to 2 km
- intermediate reach (IR) are normally for connections between sites with interconnection distances up to 15 km
- long reach (LR) are normally for connections between sites with interconnection distances up to 40 km

The optical transmit sections use the differential signals of the positive emitter-coupled logic (PECL) to drive light-emitting diodes (LED).

The optical receive sections use photodiodes to produce differential logic and signal detect outputs. The differential logic and signal detect outputs are positive emitter-coupled logic (PECL) compatible.

ATM adapter circuits for peripheral component interconnect (PCI)

The ATM adapter circuit for peripheral component interconnect (PCI) is a semi-conductor chip. The NTLX05AA/AB has two of these chips for the two links 0 and 1. These chips put into operation the following:

- ATM physical layer processor for SONET STS-3 (155.52 Mb/s) interface (includes clock recovery and clock reassembly)
- ATM layer for SONET STS-3 ATM user network interface (UNI)
- ATM adaptation layer type 5 (AAL5) segmentation and reassembly sublayer (SAR) processor for 128 ATM virtual circuits (transmit and receive)
- direct memory access (DMA) controller for PCI manages the transfer of packets between the SAR and the static random access memory (SRAM)

The ATM adapter circuit for peripheral component interconnect (PCI) chip has another name. The other name for this chip is a local ATM segmentation and reassembly and physical layer interface (LASAR).

The ATM adapter circuits for peripheral component interconnect (PCI) have the following features:

- support of ATM network interface that uses framing for signaling digital hierarchy (SDH) and SONET at 155.52 Mbps
- implementation of the ATM physical layer according to the UNI specification of the ATM forum and ITU-T recommendation I.432
- implementation of the ATM adaptation layer type 5 (AAL5) for broadband integrated services digital network (ISDN) according to ITU-T recommendation I.363
- direct interface for optical fiber (multimode or single mode)
- Saturn compliant interface for physical layer devices (SCI-PHY) for connection to external physical layer devices (SCI-PHY is from the UTOPIA specification of the ATM forum submission 93-940)
- simultaneous operation of the segmentation and reassembly (SAR) layer for 128 virtual circuits (VC)
- peak rate control of message transfer based per virtual circuit (VC)
- standard five signal P1149.1 JTAG test port to limit scan during test
- low power, 0.6-micron, +5-V complementary metal oxide semiconductor (CMOS) technology
- 208 pin, plastic quad flat pack (PQFP) package
- 19.44-Mhz oscillators to generate STS-3 and OC-3 signals

Microprocessor circuit

The microprocessor circuit has a high-performance processor core to program the PCI interface. Peripherals are around the processor core to complete the programmed microprocessor circuit.

The microprocessor circuit contains the following:

- three PCI buses
- processor local bus
- synchronous static random access memory (SRAM) controller
- advanced programmable interrupt controller (APIC) bus
- FLASH memory device
- synchronous static random access memory (SRAM) device

A prefetch field programmable gate array (FPGA) device provides memory control to access the SRAM and generate parity.

Time of day (TOD) field programmable gate array (FPGA) circuit

The TOD FPGA has two main functional units, the cell processor (CP) unit and the prefetch processor unit for data cells. The CP unit operates at the ATM cell level and performs the following functions:

- generate time of day (TOD) information used by XA Core
- forward out-of-band (OOB) information to the NT9X63AA/AB OC-3 paddle board
- receive TOD binary information from the MS
- receive information of the peripheral identification from the MS
- send information about the core identification to the MS
- send information about the firmware side band channel (FWSBC) to the NT9X63AA/AB OC-3 paddle board

The TOD FPGA circuit has another name.

Time of day (TOD) circuit

XA-Core depends on the time of day (TOD) to generate billing data and to control the time of internal events. The TOD circuits are in the DMS bus and the XA-Core.

The cell processor FPGA of the DMS bus has a TOD counter that uses the 16.384 MHz clock of the backplane. This clock has a long-term drift rate equal to a Stratum 1 clock source as an accurate link clock source.

The XA-Core controls the time of the TOD counter in the TOD FPGA with a 19.440-MHz crystal oscillator.

The TOD of the XA-Core remains synchronized to the TOD of the DMS bus because of a generated ATM cell. The generation of the ATM cell is at a constant rate. The DMS bus generates the ATM cell that contains the frozen digital time as read from the TOD counter of the DMS bus. The DMS bus sends the ATM cell to the ATM adapter circuit for PCI. The ATM adapter circuit for PCI sends the ATM cell through the UTOPIA interface to the TOD FPGA circuit. The TOD counters of the TOD FPGA are in a free-run state until the TOD counters require an update. The update comes from the drift error rate between the rates of the frozen digital time of the ATM cell and the 19.440-MHz crystal oscillator. The update to the TOD counter of the TOD FPGA circuit synchronizes TOD rates for the XA-Core and DMS bus.

Out of band (OOB) circuit

The NTLX05AA transmits out of band (OOB) information to the NT9X63AA/AB paddle board of the DMS bus. OOB messages enter the IOP on the XA-Core from the midplane. The PCI bus passes the OOB messages from the IOP to the NTLX05AA/AB packlet. The OOB information register

of the TOD FPGA circuit in the NTLX05AA/AB packlet stores the OOB messages. The NTLX05AA packlet sends the OOB messages in an ATM cell to the TOD FPGA circuit of the NT9X63AA/AB paddle board in the DMS bus. When the DMS bus receives the OOB messages from XA-Core without errors, the DMS bus passes on the OOB messages. The DMS bus passes the OOB messages to the MS reset terminal interface (RTIF).

Module information memory (MIM)

Each packlet in the XA-Core has a module information memory (MIM). The MIM stores fault log information generated by the integrated test master (ITM) on the NTLX03AA input/output processor (IOP) card. The ITM communicates with the MIM over the XA-Core inter-integrated circuit (XI2C) bus. The MIM circuit stores the following types of information:

- module identification storage
- storage for applications related to production of the packlet
- storage for applications related to performance of the packlet
- module fault log storage
- module test vector storage

Power requirements

Power for the NTLX05AA/AB packlet requires two power supplies for distribution of two voltages. The main assembly of the NTLX05AA/AB packlet uses a 3.3-V point-of-use power supply (PUPS). The mezzanine card of the NTLX05AA/AB packlet uses a 5-V PUPS. Current-limit protection is available when the 3.3-V PUPS is not available after a failure.

NTLX05BA XA-Core OC-3 two-port interface

The NTLX05BA XA-Core OC-3 (Optical Carrier) two-port interface packlet is the ATM Multi-mode Data Interface (AMDI) to the ATM edge switch.

The packlet installs on the NTLX03AA/AB input/output processor (IOP) card and connects through fiber optic cable directly to the ATM edge switch over ports supporting STM-1 single-mode (155.52 Mbit/s) signaling.

The packlet provides a pair of ATM (asynchronous transfer mode) ports with SONET OC-3 links, to the ATM edge switch. These links use the following protocols:

- the ATM physical layer according to the ATM Forum User Network Interface Specification and ITU-T Recommendation I.432
- the ATM Adaptation Layer Type 5 (AAL-5) for Broadband ISDN according to ITU-T Recommendation I.363
- a subset of the lower half of the Service Specific Convergence Sublayer - the Reliable Data Exchange Protocol (RDEP) as described by the ITU-T document Q.2110

The features of the NTLX05BA packlet are as follows:

- termination of a pair of SONET OC-3 links
- optical to electrical signal conversion (OC-3 to STS-3C)
- termination of the ATM< layer
- termination of the AAL5 Segmentation and Reassembly Sublayer
- termination of the lower half of a subset of the Service Specific Convergence Sublayer
- reception of a dedicated channel that contains the time of day (TOD) synchronization information
- transmission of out of band (OOB) messages
- built in self test (BIST) fault detection, isolation, and reporting
- provisi0on of a 32-bit multiplexed peripheral component interconnect (PCI) bus for connectivity to the IOP card
- capability to have firmware changed and downloaded from the DMS switch

Location

The packlet installs in the lower packlet position of a single-width NTLX03AA/AB input/output processor (IOP) card. The IOP card installs in one of the following slots on the rear side of the XA-Core midplane assembly: 5R, 6R, 13R, and 15R. As an alternative, a spare IOP card can install in slot 12R.

NTLX06 disk drive circuit packlet

The NTLX06 disk drive packlet provides fixed large storage for the XA-Core. The NTLX06 packlet is a packlet located in the NTLX03BA double-width IOP card. The NTLX03BA double-width IOP card is in two slots on the front of an XA-Core shelf.

NTLX06AA disk drive packlet

The NTLX06AA disk drive packlet provides 4.0-Gbytes of fixed large storage for the XA-Core. The NTLX06AA disk drive packlet supports SCSI-2 fast and wide modes.

Description of functions

A minimum of two NTLX06AA packlets are in an XA-Core shelf. The NTLX06AA packlet provides the following functions:

- It provides four Gbytes of fixed large storage for the SuperNode or the SuperNode SE switch with an XA-Core.
- It performs PCI to SCSI and SCSI to PCI transactions through a PCI to SCSI bus controller.
- It does auto power-up and disk spin-up to minimize system recovery time.

The NTLX06AA uses a SCSI-2 Fast and Wide hard disk drive. This disk packaging supports the industry standard of 8.9 cm x 14.6 cm x 2.5 cm size.

The American National Standards Institute (ANSI) standard SCSI-2 fast and wide bus provides a high-speed burst data transfer rate of 20-MByte/s peak, burst and a wide data path (16-bit). The fast data transfer rate from the disk reduces system loading time.

Software can operate the disks in either simplex mode or shadowed set mode. When operating in shadowed set mode, all data records on two disk drives. In the event of a fault, the failed disk goes out of service. The operation continues with the other disk from the set in a simplex mode when the failed disk goes out of service.

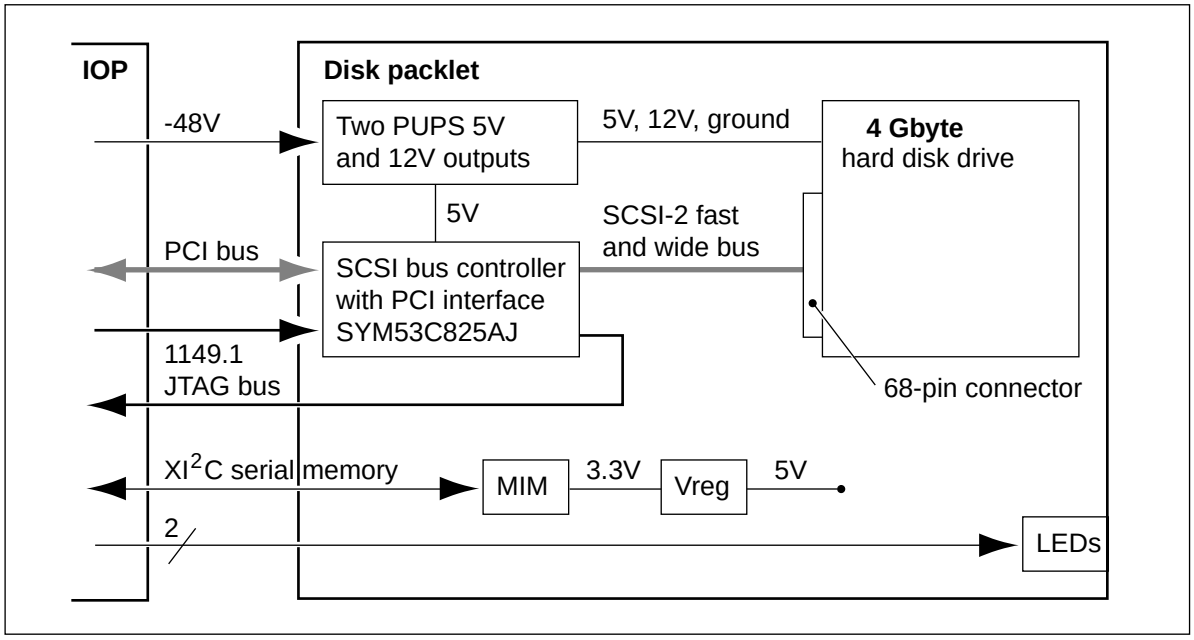
Circuits by function

The NTLX06AA disk drive packlet includes function circuits as follows:

- hard disk drive circuit
- PCI to SCSI bus controller circuit
- clocks circuit
- hardware reset circuit
- SCSI-2 fast and wide bus circuit
- point-of-use power supply (PUPS) circuit
- presence/isolation circuit
- light emitting diodes (LEDs) circuit
- module information memory (MIM) circuit

Figure 6-6 on page 6-28 shows a block diagram of the NTLX06AA disk drive packlet.

Figure 6-6 NTLX06AA block diagram



Hard disk drive circuit

The main component of the disk packlet is the 4-GByte hard disk drive. The hard disk drive has a SCSI-2 fast & wide (F&W) bus interface. The hard disk drive fits within a 8.9 cm x 14.6 cm x 2.5 cm size package. The hard disk drive is separate from the printed circuit board (PCB). The hard disk drive connects to the PCB by a SCSI cable and a power cable.

The IOP card detects an inserted NTLX06AA packlet. The IOP card starts control of the LEDs of the packlet and the field effect transistor (FET) switches on the PCI bus. The hard disk drive automatically spins up the disk with a power application. The spin-up process can last up to 30 seconds to complete. During the spin-up time the disk drive performs self tests. When the disk drive has finished its initialization, firmware or software can control disk turn up or spin down. The firmware or software control the disk spin by a start or stop unit SCSI command.

PCI to SCSI bus controller circuit

The PCI to SCSI bus controller connects the PCI bus of the IOP card to the SCSI device. The PCI to SCSI bus controller is identical to the SCSI host adapter. The PCI to SCSI bus controller is the primary interface of the NTLX06AA packlet to the IOP. The PCI to SCSI bus controller performs all

transactions between the disk drive and the IOP. All the transactions between the disk drive and the IOP are through the PCI bus.

The controller supports SCSI-2 specifications. SCSI-2 is an 8-bit bus that transmits at 10 Mbytes/s peak. SCSI-2 fast and wide is a 16-bit bus that transmits at 20 Mbytes/s peak. The PCI part of the chip supports a peak of 132 Mbytes/s.

A joint test access group (JTAG) bus connects between the PCI to SCSI bus controller of the NTLX07AA packlet and the IOP card. The JTAG bus provides testing capability.

Clocks circuit

The NTLX06AA has two clocks. One clock is for the PCI interface and the other clock is for the SCSI interface. The PCI bus clock operates at 33 MHz. The PCI bus clock feeds into the SYM53C825AJ CLK input. The SCSI interface uses a 40-MHz clock to do the SCSI-2 fast & wide protocol. The SCSI interface clock comes from a 40-MHz crystal oscillator stored in a buffer connected to the SYM53C825AJ SCLK input.

Hardware reset circuit

The PCI to SCSI bus controller and the SCSI bus are the only devices on the NTLX06AA packlet that requires a reset.

A reset of the PCI to SCSI bus controller is from a reset signal of the supply voltage supervisor. The supply voltage supervisor is on the NTLX06AA packlet. The reset signal goes to the IOP card. The IOP card responds to the reset signal and sends a reset signal to the NTLX06AA packlet. The reset signal goes to the PCI to SCSI bus controller of the NTLX06AA packlet. The reset signal from the IOP card performs a hardware reset of the PCI to SCSI bus controller. Software reset of the PCI to SCSI bus controller requires a software write to bit 6 of the ISTAT register. The ISTAT register is in the PCI to SCSI bus controller. A hardware reset clears the configuration registers while a software reset does not clear the configuration registers.

A reset of the SCSI Bus is only possible under software control. The reset routine of software writes to bit 3 of the SCNTL1 register in the PCI to SCSI bus controller.

SCSI-2 fast and wide bus circuit

The NTLX06AA packlet uses a SCSI-2 fast and wide bus. The SCSI-2 fast and wide bus is 16-bits wide with a 20-Mbyte/s transfer rate. The SCSI-2 fast and wide bus has one disk drive connected and no other devices. The NTLX06AA packlet uses a SCSI-2 fast and wide bus that is single ended.

Point-of-use power supply (PUPS) circuit

The point-of-use power supply (PUPS) provides local power conversion for the power requirements of the NTLX06AA packlet. The NTLX06AA packlet has two PUPS that generate outputs of +5 V and +12 V. The outputs voltages of the NTLX06AA packlet originate from a single power feed of -48 V from the IOP card.

Presence/isolation circuit

The presence/isolation circuit starts an event notification to the IOP card. The event notification is for insertion and removal of the NTLX06AA packlet from the IOP card.

Light emitting diodes (LEDs) circuit

The NTLX06AA packlet has two light emitting diodes (LEDs) on its face plate. The two LEDs are for the common alarm plan used by the XA-Core. The integrated test bus master (ITM) on the IOP card controls the two LEDs.

Module information memory (MIM) circuit

Each packlet in the XA-Core has a module information memory (MIM). The MIM stores fault log information generated by the integrated test master (ITM) on the NTLX03AA input/output processor (IOP) card. The ITM communicates with the MIM over the XA-Core inter-integrated circuit (XI2C) bus. The MIM circuit stores the following types of information:

- module identification storage
- storage for applications related to production of the packlet
- storage for applications related to performance of the packlet
- module fault log storage
- module test vector storage

Power requirements

The PUPS have an input voltage range of -36 V to -75 V. The PUPS generates 25-W, 3.3-V digital and analog outputs from battery backplane feeds. Table 6-2 on page 6-30 shows the NTLX06AA power requirements.

Table 6-2 NTLX06AA power requirements

Parameter	Minimum	Nominal	Maximum	Power
Supply voltage	-36 V	-48 V	-75 V	
Supply current	2.94 A	2.15 A	1.37 A	
IOP + 1 tape + 1 disk	1.46 A	1.09 A	0.70 A	75 W

NTLX06AB disk drive packlet

The NTLX06AB disk drive packlet provides 8.4-Gbytes of fixed large storage for the XA-Core. The NTLX06AB disk drive packlet supports the SCSI-2 fast and wide protocol.

Description of functions

A minimum of two NTLX06AB packlets are in an XA-Core shelf. The NTLX06AB packlet provides the following functions:

- It provides 8.4 Gbytes of fixed large storage for the SuperNode or the SuperNode SE switch with an XA-Core.
- It performs PCI to SCSI and SCSI to PCI transactions through a PCI to SCSI bus controller.
- It does auto power-up and disk spin-up to minimize system recovery time.

The NTLX06AB uses a SCSI-2 Fast and Wide hard disk drive. This disk packaging supports the industry standard of 8.9 cm x 14.6 cm x 2.5 cm size.

The American National Standards Institute (ANSI) standard SCSI-2 fast and wide bus provides a high-speed burst data transfer rate of 20-MByte/s peak, burst and a wide data path (16-bit). The fast data transfer rate from the disk reduces system loading time.

Software can operate the disks in either simplex mode or shadowed set mode. When operating in shadowed set mode, all data records on two disk drives. In the event of a fault, the failed disk goes out of service. The operation continues with the other disk from the set in a simplex mode when the failed disk goes out of service.

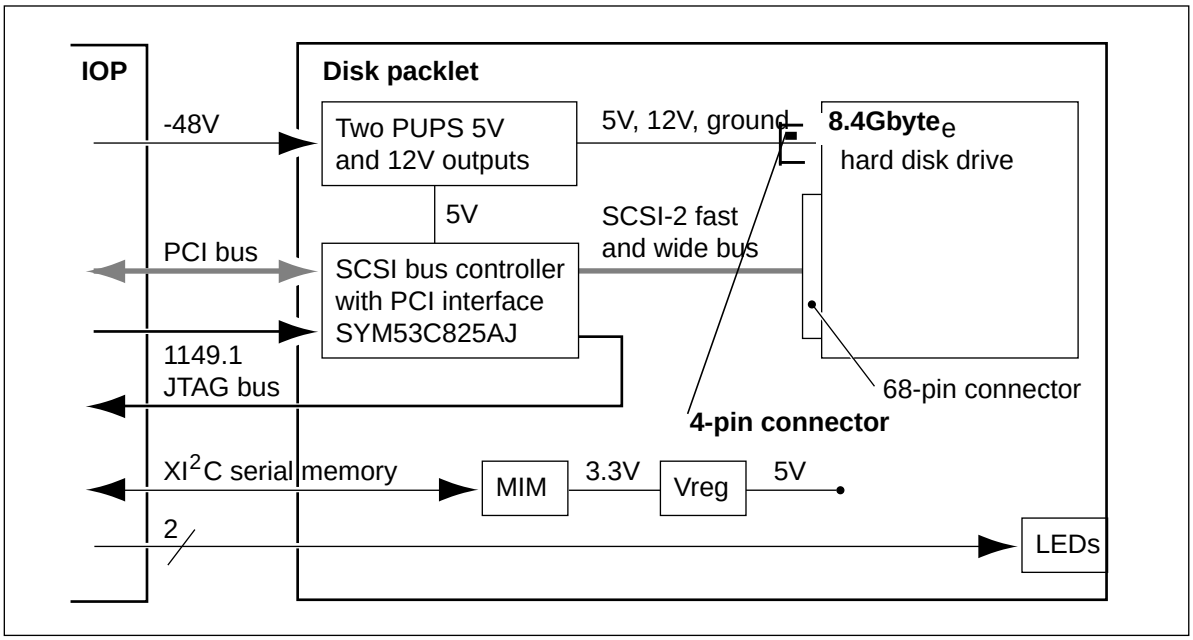
Circuits by function

The NTLX06AB disk drive packlet includes function circuits as follows:

- hard disk drive circuit
- PCI to SCSI bus controller circuit
- clocks circuit
- hardware reset circuit
- SCSI-2 fast and wide bus circuit
- point-of-use power supply (PUPS) circuit
- presence/isolation circuit
- light emitting diodes (LEDs) circuit
- module information memory (MIM) circuit

Figure 6-7 on page 6-32 shows a block diagram of the NTLX06AB disk drive packlet.

Figure 6-7 NTLX06AB block diagram



Hard disk drive circuit

The main component of the disk packlet is the 8.4-GByte hard disk drive. The hard disk drive has a SCSI-2 fast & wide (F&W) bus interface. The hard disk drive fits within a 8.9 cm x 14.6 cm x 2.5 cm size package. The hard disk drive is separate from the printed circuit board (PCB). The hard disk drive connects to the PCB by a SCSI cable and a power cable.

The IOP card detects an inserted NTLX06AB packlet and enables the field effect transistor (FET) switches on the PCI bus. The IOP card also controls the packlet LEDs. The hard disk drive automatically spins up the disk with a power application. The spin-up process can last up to 30 seconds. During the spin-up time the disk drive performs self tests. When the disk drive has finished its initialization, firmware or software can control disk spinup or spin down. Firmware or software controls the disk spin by a start or stop unit SCSI command.

PCI to SCSI bus controller circuit

The PCI to SCSI bus controller connects the PCI bus of the IOP card to the SCSI device. The PCI to SCSI bus controller is another name for the SCSI host adapter. The PCI to SCSI bus controller is the primary interface of the NTLX06AB packlet to the IOP. The PCI to SCSI bus controller performs all

transactions between the disk drive and the IOP. All the transactions between the disk drive and the IOP are through the PCI bus.

The controller supports SCSI-2 and SCSI-2 fast and wide specifications. SCSI-2 is an 8-bit bus that transmits at 10 Mbytes/s peak. SCSI-2 fast and wide is a 16-bit bus that transmits at 20 Mbytes/s peak. The PCI part of the chip supports a peak of 132 Mbytes/s.

A joint test access group (JTAG) bus connects between the PCI to SCSI bus controller of the NTLX06AB packlet and the IOP card. The JTAG bus provides testing capability.

Clock circuit

The NTLX06AB has two clocks. One clock is for the PCI interface and the other clock is for the SCSI interface. The PCI bus clock operates at 33 MHz and originates from the IOP. The PCI bus clock feeds into the SYM53C825AJ CLK input. The SCSI interface uses a 40-MHz clock to do the SCSI-2 fast & wide protocol. The SCSI interface clock comes from a 40-MHz crystal oscillator connected to the SYM53C825AJ SCLK input.

Hardware reset circuit

The PCI to SCSI bus controller and the SCSI bus are the only devices on the NTLX06AB packlet that requires a reset.

The NTLX06AB has an onboard supply voltage supervisor. If 5 V on the packlet drops below a specified voltage, the supervisor activates a reset a reset signal. The reset signal goes to the IOP card. The IOP card responds to the reset signal and sends a separate reset signal back to the NTLX06AB packlet. The reset signal goes to the PCI to SCSI bus controller of the NTLX06AB packlet. The reset signal from the IOP card performs a hardware reset of the PCI to SCSI bus controller. Software reset of the PCI to SCSI bus controller requires a software write to bit 6 of the ISTAT register. The ISTAT register is in the PCI to SCSI bus controller. A hardware reset clears the configuration registers while a software reset does not clear the configuration registers.

A reset of the SCSI Bus is only possible under software control. The reset routine of software writes to bit 3 of the SCNTL1 register in the PCI to SCSI bus controller.

SCSI-2 fast and wide bus circuit

The NTLX06AA packlet uses a SCSI-2 fast and wide bus. The SCSI-2 fast and wide bus is 16-bits wide with a 20-Mbyte/s transfer rate. The SCSI-2 fast and wide bus has one disk drive connected and no other devices. The NTLX06AB packlet uses a SCSI-2 fast and wide bus that is single ended.

Point-of-use power supply (PUPS) circuit

The point-of-use power supply (PUPS) provides local power conversion for the power requirements of the NTLX06AB packlet. The NTLX06AB packlet has two PUPS that generate outputs of +5 V and +12 V. The outputs voltages of the NTLX06AB packlet originate from a single power feed of -48 V from the IOP card.

Presence/isolation circuit

The presence/isolation circuit starts an event notification to the IOP card. The event notification is for insertion and removal of the NTLX06AB packlet from the IOP card.

Light emitting diodes (LEDs) circuit

The NTLX06AB packlet has two light emitting diodes (LEDs) on its face plate. The two LEDs are for the common alarm plan used by the XA-Core. The integrated test bus master (ITM) on the IOP card controls the two LEDs.

Module information memory (MIM) circuit

Each packlet in the XA-Core has a module information memory (MIM). The MIM stores fault log information generated by the integrated test master (ITM) on the NTLX03BA input/output processor (IOP) card. The ITM communicates with the MIM over the XA-Core inter-integrated circuit (XI2C) bus. The MIM circuit stores the following types of information:

- module identification storage
- storage for applications related to production of the packlet
- storage for applications related to performance of the packlet
- module fault log storage
- module test vector storage

Power requirements

The PUPS have an input voltage range of -36 V to -75 V. The PUPS generates 5-V, 25-W and 12-V, 50-W outputs from battery backplane feeds. Table 6-3 on page 6-34 shows the NTLX06AB power requirements.

Table 6-3 NTLX06AB power requirements

Parameter	Minimum	Nominal	Maximum	Power
Supply voltage	-36 V	-48 V	-75 V	
Supply current	0.43 A	0.68 A	1.45 A	
IOP + 1 tape + 1 disk	1.46 A	1.09 A	0.70 A	75 W
Note: The maximum rating occurs at disk spin-up.				

NTLX07 digital audio tape (DAT) drive circuit packlet

The NTLX07 digital audio tape (DAT) drive packlet provides fixed large storage for the XA-Core. The NTLX07 packlet is a packlet located in the NTLX03BA double-width IOP card. The NTLX03BA double-width IOP card is in two slots on the front of an XA-Core shelf.

NTLX07AA digital audio tape (DAT) drive packlet

The NTLX07AA digital audio tape (DAT) drive packlet provides 1-4 Gigabyte of transportable large storage for the XA-Core. The NTLX07AA packlet uses a SCSI-2 DAT drive.

Description of functions

Two NTLX07AA packlets are in the SuperNode or the SuperNode SE configuration of the DMS-100 family of switches. The NTLX07AA packlet provides the following functions:

- 1-4 GigaByte of transportable large storage for the SuperNode or the SuperNode SE switch with an XA-Core.
- Perform PCI to SCSI and SCSI to PCI transactions through a PCI to SCSI bus controller.

The NTLX07AA packlet uses a SCSI-2 DAT drive. This DAT packaging supports the industry standard 10.2 cm x 15.0 cm x 4.1 cm size.

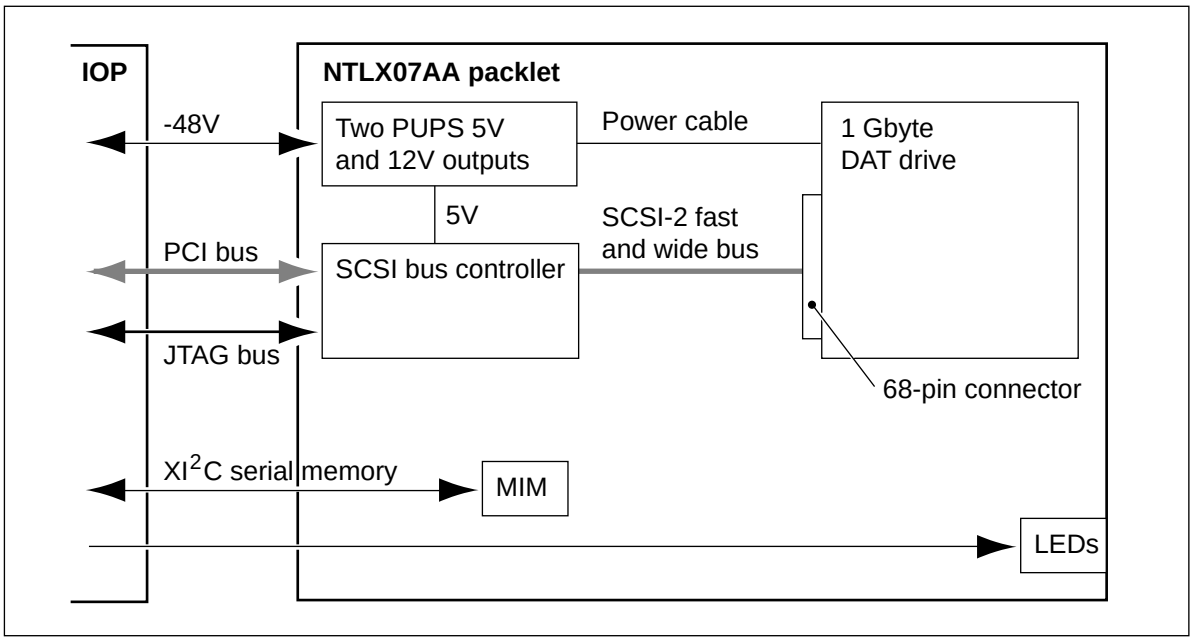
Circuits by function

The NTLX07AA packlet includes function circuits as follows:

- DAT drive circuit
- PCI to SCSI bus controller circuit
- clocks circuit
- hardware reset circuit
- SCSI-2 fast and wide bus circuit
- point-of-use power supply (PUPS) circuit
- presence/isolation circuit
- light emitting diodes (LEDs) circuit
- module information memory (MIM) circuit

Figure 6-8 on page 6-36 shows a block diagram of the NTLX07AA DAT drive packlet.

Figure 6-8 NTLX07AA block diagram



DAT drive circuit

The main component of the NTLX07AA packlet is the DAT drive. The DAT drive has a capacity from 1.0 Gbytes for a 60-m tape to 4.0 Gbytes for a 120-m tape. A 90-m tape has a DAT drive capacity of 2.0 Gbytes. The NTLX07AA packlet has a SCSI-2 interface. The NTLX07AA packlet follows the 10.2 cm x 15.0 cm x 4.1 cm size.

The DAT drive attaches to supports on the PCB of the NTLX07AA packlet. The DAT drive connects to the PCB of the NTLX07AA packlet by a SCSI cable and a Power cable. The DAT drive operates in simplex mode.

The IOP card detects an inserted NTLX07AA packlet. The IOP card starts control of the LEDs of the packlet and the field effect transistor (FET) switches on the PCI bus. The DAT drive automatically applies power with an inserted NTLX07AA packlet.

The EJECT button controls the ejection of the DAT tape from the NTLX07AA packlet. Access to the EJECT button is through the door of NTLX07AA face plate. Complete removal of the DAT tape is possible when the DAT tape is partially outside the door of the NTLX07AA packlet.

PCI to SCSI bus controller circuit

The PCI to SCSI bus controller connects the PCI bus of the IOP card to the SCSI device. The PCI to SCSI bus controller is identical to the SCSI host adapter. The PCI to SCSI bus controller is the primary interface of the

NTLX07AA packlet to the IOP. The PCI to SCSI bus controller performs all transactions between the DAT drive and the IOP. All the transactions between the DAT drive and the IOP are through the PCI bus.

The controller supports SCSI-2 and SCSI-2 fast and wide specifications. SCSI-2 is an 8-bit bus that transmits at 10 Mbytes/s peak. SCSI-2 fast and wide is a 16-bit bus that transmits at 20 Mbytes/s peak. The PCI part of the chip supports a peak of 132 Mbytes/s.

A joint test access group (JTAG) bus connects between the PCI to SCSI bus controller of the NTLX07AA packlet and the IOP card. The JTAG bus provides testing capability.

Clocks circuit

The NTLX07AA has two clocks: one for the PCI interface and one for the SCSI interface. The PCI bus clock operates at 33 Mhz. The clock signal feeds directly into the SYM53C825AJ clock input. The SCSI interface uses a 40-Mhz clock to do the SCSI-2 Fast & Wide protocol. The SCSI interface clock comes from a 40-Mhz crystal oscillator stored in a buffer connected to the SYM53C825AJ SCLK input.

Hardware reset circuit

The PCI to SCSI bus controller and the SCSI bus are the only devices on the NTLX07AA packlet that requires a reset.

A reset of the PCI to SCSI bus controller is from a reset signal of the supply voltage supervisor. The supply voltage supervisor is on the NTLX07AA packlet. The reset signal goes to the IOP card. The IOP card responds to the reset signal and sends a reset signal to the NTLX07AA packlet. The reset signal goes to the PCI to SCSI bus controller of the NTLX07AA packlet. The reset signal from the IOP card performs a hardware reset of the PCI to SCSI bus controller. Software reset of the PCI to SCSI bus controller requires a software write to bit 6 of the ISTAT register. The ISTAT register is in the PCI to SCSI bus controller. A hardware reset clears the configuration registers while a software reset does not clear the configuration registers.

A reset of the SCSI Bus is only possible under software control. The reset routine of software writes to bit 3 of the SCNTL1 register in the PCI to SCSI bus controller.

SCSI-2 fast and wide bus circuit

The NTLX07AA packlet uses a SCSI-2 fast and wide bus. The SCSI-2 fast and wide bus is 16-bits wide with a 20-Mbyte/s transfer rate. The SCSI-2 fast and wide bus has one DAT drive connected and no other devices. The NTLX07AA packlet uses a SCSI-2 fast and wide bus that is single ended.

Presence/isolation circuit

The presence/isolation circuit starts an event notification to the IOP card. The event notification is for insertion and removal of the NTLX07AA packlet from the IOP card.

Light emitting diodes (LEDs)

The NTLX07AA packlet has two light emitting diodes (LEDs) on its face plate. The two LEDs are for the common alarm plan used by the XA-Core. The integrated test bus master (ITM) on the IOP card controls the two LEDs.

Module information memory (MIM)

Each packlet in the XA-Core has a module information memory (MIM). The MIM stores fault log information generated by the integrated test master (ITM) on the NTLX03AA input/output processor (IOP) card. The ITM communicates with the MIM over the XA-Core inter-integrated circuit (XI2C) bus. The MIM circuit stores the following types of information:

- module identification storage
- storage for applications related to production of the packlet
- storage for applications related to performance of the packlet
- module fault log storage
- module test vector storage

Point-of-use power supply (PUPS) circuit

The point-of-use power supply (PUPS) provides local power conversion for the power requirements of the NTLX07AA packlet. The NTLX07AA packlet has two PUPS that generate outputs of +5 V and +12 V. The outputs voltages of the NTLX07AA packlet originate from a single power feed of -48 V from the IOP card.

Power requirements

The PUPS have an input voltage range of -36 V to -75 V. The PUPS generates 25-W, 3.3-V digital and analog outputs from battery backplane feeds. Table 6-4 on page 6-38 shows the NTLX07AA power requirements.

Table 6-4 NTLX07AA power requirements

Parameter	Minimum	Nominal	Maximum	Power
Supply voltage	-36 V	-48 V	-75 V	
Supply current	2.94 A	2.15 A	1.37 A	
IOP + 1 tape + 1 disk	1.46 A	1.09 A	0.70 A	75 W

NTLX08 RS232 serial interface circuit packlet

The NTLX08 RS232 serial interface packlet provides an interface for a serial RS-232 input/output service. A reset terminal interface (RTIF) is a serial RS-232 input/output service. The NTLX08 RS232 serial interface packlet also supports current loop (CL) data communications. The NTLX08 packlet is a packlet located in the NTLX03AA/AB single-width IOP card. The NTLX03AA/AB single-width IOP card is in one slot of the XA-Core shelf. The location of the NTLX03AA/AB card with an NTLX08 packlet is in a back slot of the XA-Core shelf.

NTLX08AA RS232 serial interface packlet

The NTLX08AA RS232 serial interface packlet provides service for a reset terminal interface (RTIF).

The NTLX08AA packlet provides a reset system. The reset system reboots and monitors the SuperNode and SuperNode SE switches that have an XA-Core. The RTIF has E1A RS232C links to maintenance terminals. The NTLX08AA packlet also supports current loop (CL) data communications. The NTLX08AA is in a single-width IOP unit (NTLX03AA) which is in a single XA-Core shelf slot.

Description of functions

The NTLX08AA packlet provides an interface to XA-Core with the following functions:

- reset the state of the XA-Core with no consideration to the switch state
- monitor and control functions during commissioning and emergency recovery
- provide switch status

The above functions of the NTLX08AA packlet also include the following functions:

- fault information
- status reports during boot activity
- switch sanity
- provide RS232C and current loop (CL) interface protocol
- provide human-machine interface for local and remote access
- act as a serial port resource for both firmware and software interpreters

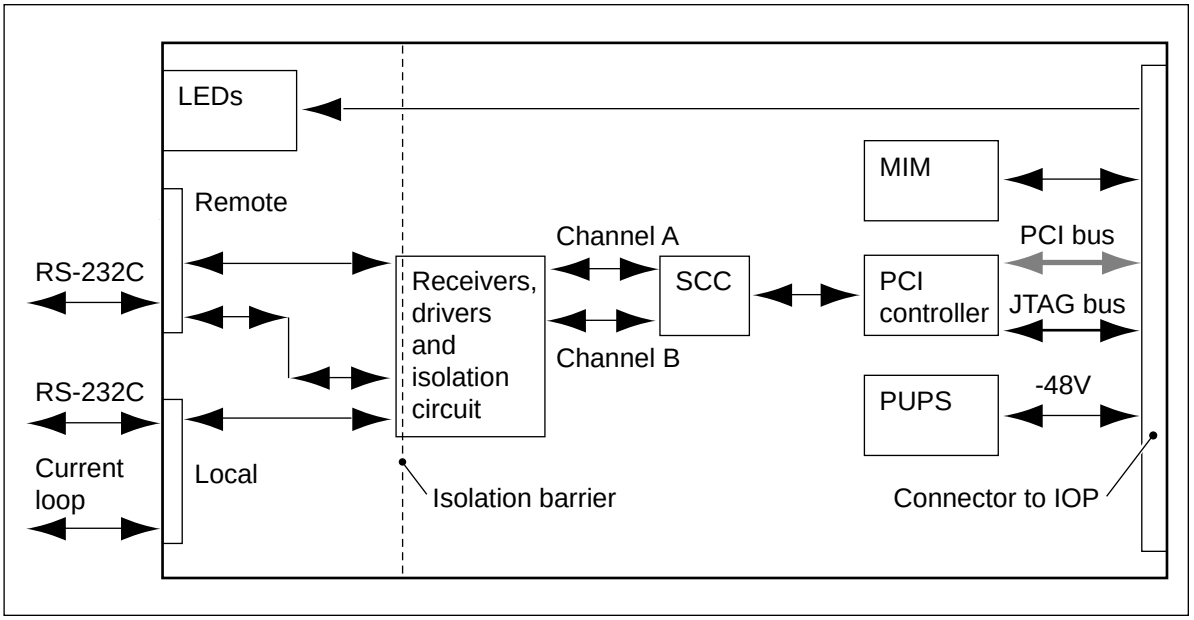
Circuits by function

The NTLX08AA includes function circuits as follows:

- peripheral component interconnect (PCI) controller circuit
- serial communication controller (SCC) circuit
- universal asynchronous receiver transmitter (UART) and isolated system ground (ISG) circuits
- light emitting diodes (LEDs) circuit
- module information memory (MIM) circuit
- point-of-use power supply (PUPS) circuit

Figure 6-9 on page 6-40 shows a block diagram of the NTLX08AA RS232 serial interface packlet.

Figure 6-9 NTLX08AA block diagram



PCI controller circuit

The peripheral component interconnect (PCI) controller circuit is a field programmable gate array (FPGA) device. The PCI controller provides an interface between the IOP's PCI Bus and the SCC.

Some of the functions of the PCI controller are the following:

- identify the PCI agent
- joint test access (JTAG) limit scanning capability
- decode address and pass through to the SCC

- eight bit data and command pass through to the SCC
- interrupt request and acknowledge pass through between PCI bus and SCC
- automatic configuration when power turned on from a programmable read only memory (PROM) that has the configuration
- optional device configuration through the limit scan port

SCC circuit

The serial communication controller (SCC) is a two-channel interface between the UART and the PCI controller. The two channels are channel A and channel B. The SCC has the following features:

- two full-duplex channels that are each self-sufficient:
- separate baud rate generator
- separate digital phase-locked loop for clock recovery
- local loopback and auto echo modes.

UART and ISG circuits

The two universal asynchronous receiver transmitter (UART) circuits converts the SCC's channels A and B serial data to RS-232C and current-loop (CL) interfaces. The conversion is necessary so that external terminal equipment can connect to the RTIF interface. The transceiver devices require a single (+5 V) power source.

The isolated system ground (ISG) circuit provides isolation of the external interfaces from the XA-core power and ground. The isolation is ISG compliant for the RTIF interface.

Channels A and B of the SCC are available to the user. Channels A and B have two high-density connectors DB26 and DB15 located on the face-plate of the packlet. Channel A creates the interface to the local terminal or serial communication equipment through either an RS-232C or current loop (CL) interface. Channel B uses the RS-232C interface for remote interface connections.

Light emitting diodes (LEDs) circuit

Control of the three LEDs on the NTLX08AA packlet is by three signals from a register. The register is the intelligent test master (ITM) general purpose input/output (GPIO). The control follows the alarm plan for XA-Core.

Module information memory (MIM) circuit

Each packlet in the XA-Core has a module information memory (MIM). The MIM stores fault log information generated by the integrated test master (ITM) on the NTLX03AA input/output processor (IOP) card. The ITM

communicates with the MIM over the XA-Core inter-integrated circuit (XI2C) bus. The MIM circuit stores the following types of information:

- module identification storage
- storage for applications related to production of the packlet
- storage for applications related to performance of the packlet
- module fault log storage
- module test vector storage

Point-of-use power supply (PUPS) circuit

The point-of-use power supply (PUPS) provides local power conversion from the -48 V source. The PUPS also provides power-up reset for about 0.1 s after the +5V reaches the working level.

The PUPS circuit also provides for detection of an NTLX08AA packlet insertion in a slot of the XA-Core shelf.

Power requirements

The PUPS has an input voltage range of 36 V to 75 V. The PUPS generates 25-W, 3.3-V digital and analog outputs from battery backplane feeds. Table 6-5 on page 6-42 shows the NTLX008AA power requirements.

Table 6-5 NTLX08AA power requirements

Parameter	Minimum	Nominal	Maximum	Power
Supply voltage	-36 V	-48 V	-75 V	
Supply current	2.94 A	2.15 A	1.37 A	
IOP + 1 RTIF + 1 CMIC	1.46 A	1.09 A	0.70 A	52.5 W

NTLX08AB RS232 serial interface packlet

The NTLX08AB RS232 serial interface packlet provides service for a reset terminal interface (RTIF).

The NTLX08AB packlet provides a reset system. The reset system reboots and monitors the SuperNode and SuperNode SE switches that have an XA-Core. The RTIF has EIA RS232C links to maintenance terminals. The NTLX08AB packlet also supports current loop (CL) data communications. The NTLX08AB is in a single-width IOP unit (NTLX03AA) which is in a single XA-Core shelf slot.

Description of functions

The NTLX08AB packlet provides an interface to XA-Core with the following functions:

- reset the state of the XA-Core with no consideration to the switch state
- monitor and control functions during commissioning and emergency recovery
- provide switch status

The above functions of the NTLX08AB packlet also include the following functions:

- fault information
- status reports during boot activity
- switch sanity
- provide RS232C and current loop (CL) interface protocol
- provide human-machine interface for local and remote access
- act as a serial port resource for both firmware and software interpreters

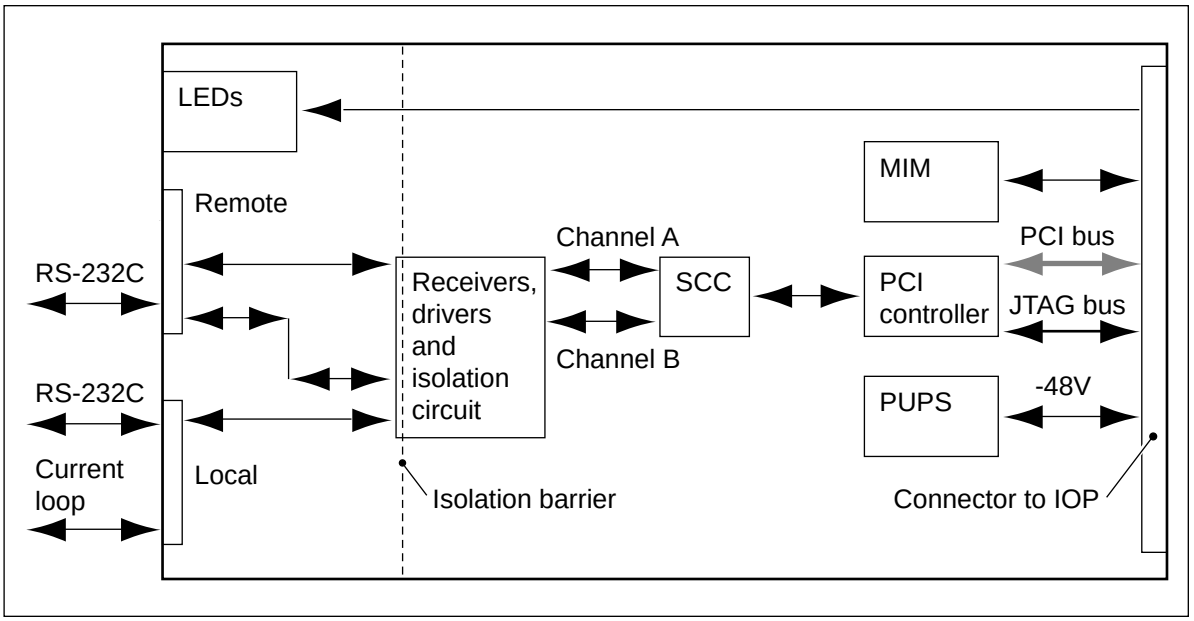
Circuits by function

The NTLX08AB includes function circuits as follows:

- peripheral component interconnect (PCI) controller circuit
- serial communication controller (SCC)
- universal asynchronous receiver transmitter (UART) and isolated system ground (ISG) circuits
- light emitting diodes (LEDs) circuit
- module information memory (MIM) circuit
- point-of-use power supply (PUPS) circuit

Figure 6-10 on page 6-44 shows a block diagram of the NTLX08AB RS232 serial interface packlet.

Figure 6-10 NTLX08AB block diagram



PCI controller circuit

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Some of the functions of the PCI controller are the following:

- identify the PCI agent
- joint test access (JTAG) limit scanning capability
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SCC circuit

The serial communication controller (SCC) is a two-channel interface between the UART and the PCI controller. The two channels are channel A and channel B. The SCC has the following features:

- two full-duplex channels that are each self-sufficient
- separate baud rate generator

- separate digital phase-locked loop for clock recovery
- local loopback and auto echo modes.

UART and ISG circuits

The two universal asynchronous receiver transmitter (UART) circuits converts the SCC's channels A and B serial data to RS-232C and current-loop (CL) interfaces. The conversion is necessary so that external terminal equipment can connect to the RTIF interface. The transceiver devices require a single (+5 V) power source.

The isolated system ground (ISG) design provides isolation of the external interfaces from the XA-core power and ground. The isolation is ISG compliant for the RTIF interface.

Channels A and B of the SCC are available to the user. Channels A and B have two high-density connectors DB15 and DB26 located on the face-plate of the packlet. Channel A creates the interface to the local terminal or serial communication equipment through either an RS-232C or current loop (CL) interface. Channel B uses the RS-232C interface for remote interface connections.

Light emitting diodes (LEDs) circuit

Control of the three LEDs on the NTLX08AB packlet is by three signals from a register. The register is the intelligent test master (ITM) general purpose input/output (GPIO). The control follows the alarm plan for XA-Core.

Module information memory (MIM) circuit

Each packlet in the XA-Core has a module information memory (MIM). The MIM stores fault log information generated by the integrated test master (ITM) on the NTLX03AA input/output processor (IOP) card. The ITM communicates with the MIM over the XA-Core inter-integrated circuit (XI2C) bus. The MIM circuit stores the following types of information:

- module identification storage
- storage for applications related to production of the packlet
- storage for applications related to performance of the packlet
- module fault log storage
- module test vector storage

Point-of-use power supply (PUPS) circuit

The point-of-use power supply (PUPS) provides local power conversion from the -48 V source. The PUPS also provides power-up reset for about 0.1 s after the +5V reaches the working level.

Power requirements

The PUPS has an input voltage range of 36 V to 75 V. The PUPS generates 20-W, 5.0-V output from battery backplane feeds. Table 6-6 on page 6-46 shows the NTLX08AB power requirements.

Table 6-6 NTLX08AB power requirements

Parameter	Minimum	Nominal	Maximum	Power
Supply voltage	-36 V	-48 V	-75 V	11 W
Supply current (48Vdc)	0.150 A (idle)	0.230 A (active)	1.0 A (hot insertion)	

NTLX09AA XA-Core Ethernet single port interface packlet

The NTLX09AA XA-Core Ethernet single port interface packlet provides the connection between the XA-Core shelf and the LAN hub and IP network.

The packlet installs on the NTLX03AA/AB input/output processor (IOP) card and connects to the LAN through a twisted-pair copper wire and the single Ethernet 10.100BaseT RJ45 Teladapt connector mounted on the face panel of the packlet.

The Category 5 Ethernet cable has a length restriction of 100 meters.

The packlet supports IEEE 802.3 framing. Multiproduct encapsulation procedures are implemented according to ANSI T1.617 Annex F and RFC 1490. Protocols can be encapsulated using direct Network Layer Protocol Identifiers (NLPID), Subnetwork Access Protocol (SNAP), or NLPID for ITU-T Q.933.

The Ethernet packlet contains a full implementation of the UDP-TCP/IP standard, enabling the card to act as a router. The packlet supports the following protocols and applications:

- Internet protocol (IP) v4, defined in RFC 791
- the Internet Control Message Protocol (ICMP), defined in RFC 792, which provides communication control functions
- Simple Network Management Protocol (SNMP), defined in RFC 1213 and RFC 1315
- Routing Information Protocol (RIP) v1, defined in RFC 1058, which supports the variable length subnet mask and classes interdomain routing features from RIP v2
- Address Resolution Protocol (ARP), defined in RFC 826, which supports classic IP addressing extended to include recognition of subnet zero. Broadcast forwarding in a configurable capability.

- Transport Control Protocol (TCP), defined in RFC 793, which enables connection-oriented transport services
- User Datagram Protocol (UDP), which provides connectionless transport services
- Path determination for routing is supported by dynamic routing (RIP), and by configurable static and default routes.

The features of the NTLX09AA packlet are as follows:

- termination of a 10/100BaseT physical (PHY) link
- full duplex support at both 10 and 100 Mbit/s
- IEEE 802.3u auto0negotiation support
- 32-bit multiplexed peripheral component interface (PCI) bus for connectivity to the IOP card
- ITAG test interfaces of all devices except the physical link to PCI bus converter (82559 device) and the S-SRAM used as buffer memory

Location

The packlet installs in the lower packlet position of a single-width NTLX03AA/AB input/output processor (IOP) card. The IOP card installs in one of the following slots on the rear side of the XA-Core midplane assembly: 5R, 6R, 13R, and 15R. As an alternative, a spare IOP card can install in slot 12R.

NTLX12 shelf interface module (SIM) circuit pack

The NTLX12 shelf interface module (SIM) card provides the power interface for the XA-Core shelf. The interface is between the power input of the power distribution center (PDC), and the XA-Core shelf. Each XA-Core shelf has two NTLX12 SIM cards located in slots on the back side.

NTLX12AA SIM card

The NTLX12AA SIM card is the power interface for the XA-Core shelf. All of the input and output interfaces are through connectors.

Description of functions

Each NTLX12AA SIM card receives three, -48 V / -60 V, 30-A input feeds from the PDC. The NTLX12AA SIM card provides:

- a low frequency filter for each of the three input feeds
- a slow-charge circuit prevents high current spikes to not enter the filter capacitors at system power-up
- load stability

- current limit of a maximum 20 A for each of three outputs through three 20-A circuit breakers
- test access
- alarm reports to the frame supervisory panel (FSP)

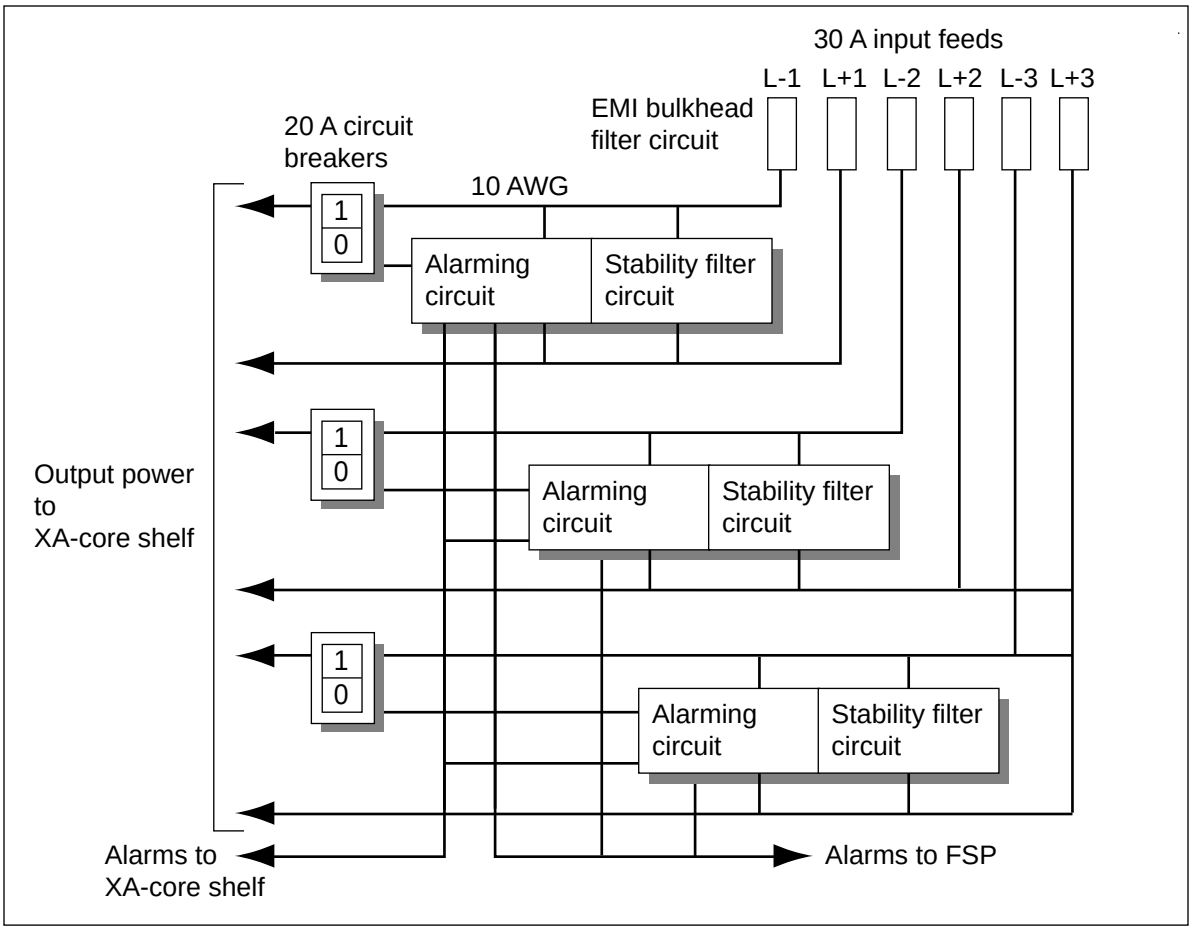
Circuits by function

The NTLX12AA SIM card has circuits for functions as follows:

- electromagnetic interference (EMI) bulkhead filter circuit
- 20-A circuit breakers
- alarm circuits
- stability filter circuits

Figure 6-11 on page 6-48 shows a block diagram of the NTLX12AA SIM card.

Figure 6-11 NTLX12AA block diagram



EMI bulkhead filter circuit

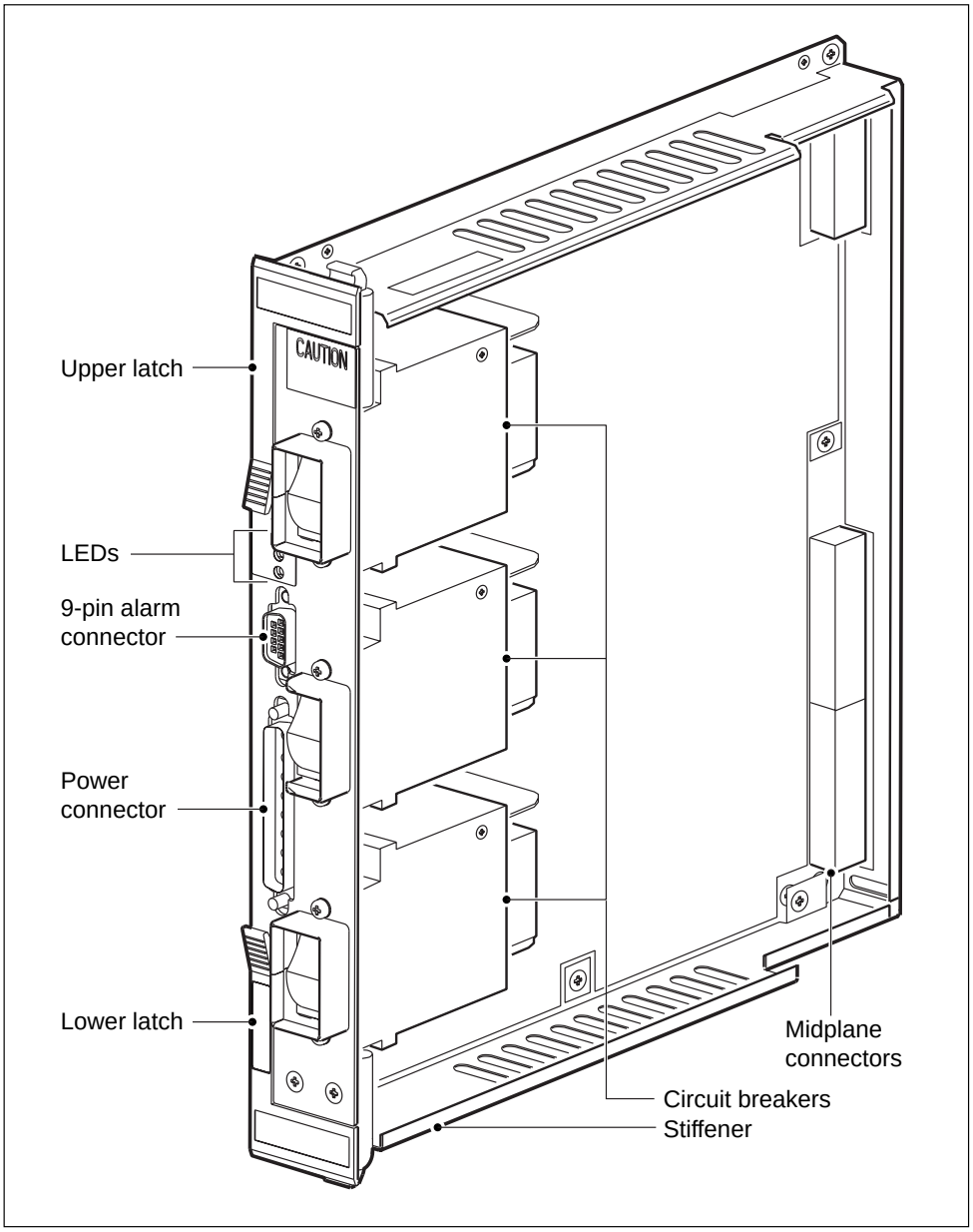
Electromagnetic interference (EMI) filters are in the EMI bulkhead filter circuit. This circuit filters out EMI for all signals through the midplane connector (or bulkhead) of the NTLX12AA SIM card.

20A circuit breakers

There are three 20-A circuit breakers on the power output to the XA-Core shelf. Each of the three circuit breakers is in line with one of the three 30-A input feeds. The circuit breakers protect the midplane and allow for maintenance activity.

Figure 6-12 on page 6-50 shows a view of the circuit breakers on the NTLX12AA SIM card.

Figure 6-12 Circuit breakers of the NTLX12AA SIM card



Alarm circuits

The alarm circuits generate alarms if a circuit breaker trips or if fuses blow within the circuits of the NTLX12AA SIM card. The generated alarms go to the frame supervisory panel (FSP) and to the XA-Core shelf. A generated

alarm also makes the amber LED light on the faceplate of the NTLX12AA SIM card. The amber LED lights to indicate one of the three power feeds at the input has lost power. When all input power feeds have no power, the red LED lights on the faceplate of the NTLX12AA SIM card.

Stability filter circuits

The stability filter circuits provide low frequency filters and load stability functions for the power to the output.

Power requirements

The NTLX12AA SIM card accepts three 30-A input feeds. The input voltage capability is for -48 V or for -60 V. The input voltage range is -38 V to -75 V. In figure 6-11, the L1, L2, and L3 represent the leads of the three input feeds. The "-" and "+" for L1, L2, and L3 represents the negative (-) and positive (+) leads of the input feeds.

Light emitting diode (LED) strategy

The NTLX12AA SIM card has three visual indicators on the faceplate. The three visual indicators are light emitting diodes (LED) that have different colors. The colors of the three LEDs are green, amber, and red. These LEDs provide a visual indication of the status of the NTLX12AA SIM card. The status indicates when there is safe removal of the NTLX12AA SIM card from a slot of the XA-Core shelf. Table 6-7 on page 6-51 shows LED indications, reasons, and actions.

Table 6-7 LED indications, reasons, and actions (Sheet 1 of 2)

Green LED	Amber LED	Red LED	Reason	Action
Off	Off	Off	Card has no power, a LED control failure, or no connection to midplane	Do not remove the card before further investigation - service not affected if card removed
On	Off	Off	Card operates correctly	Do not remove the card - removal of card can result in loss of service

Table 6-7 LED indications, reasons, and actions (Sheet 2 of 2)

Green LED	Amber LED	Red LED	Reason	Action
On	On	Off	Alarm state failure of card, input feed, or circuit breaker	Do not remove the card before additional analysis
Off	On	On	All input feeds have no power	Can remove card safely

NTLX14 shared memory (SM) circuit pack

The NTLX14 shared memory (SM) card provides the XA-Core with a memory device for data store. All data store is in the shared memory that any PE card can access.

The SM card design supports the following services.

- data ownership
- shared memory for data store
- requests for separate ownership or shared read ownership
- access restriction to prevent other switch failures by IOP or PE cards
- 32-byte memory ownership
- XAI transactions except for access to 64-byte read/write memory
- retransmit XAI frames between PE and IOP cards (pass-through mode)
- 32-Mbyte memory modules that can program to other 32-Mbyte logical address limit
- reset control by XAI register access
- 16 XAI receive ports and one (dual) XAI transmit port

The SM cards support fault tolerance for switch reliability. The SM cards support fault tolerance by a design of checkpoints and rollback. The checkpoint represents a successful completion of a software task. Rollback is a return of the software state to the last completed checkpoint when the current software task cannot complete by a planned time. A rollback from a fault condition allows the SM card retry to complete the software task.

NTLX14CA 384-Mbyte shared memory (SM) card

The NTLX14CA 384-Mbyte shared memory (SM) card provides 384 Mbytes of logical memory (768 Mbytes of physical memory). The physical memory

includes six main memory hybrids that use synchronous dynamic random access memory (SDRAM) design of 64 Mbytes.

Functional description

Each SM card communicates with all the PE and IOP cards. An SM card has no communication with the other SM cards. The SM card has two copies of main memory and a single ownership memory. An application specific integrated circuit (ASIC) device called the shared memory ownership and access controller (SMOAC) supports most of the SM card functions. The SM card has extended architecture interconnect (XAI) logic to interface between the SMOAC device and the XAI midplane.

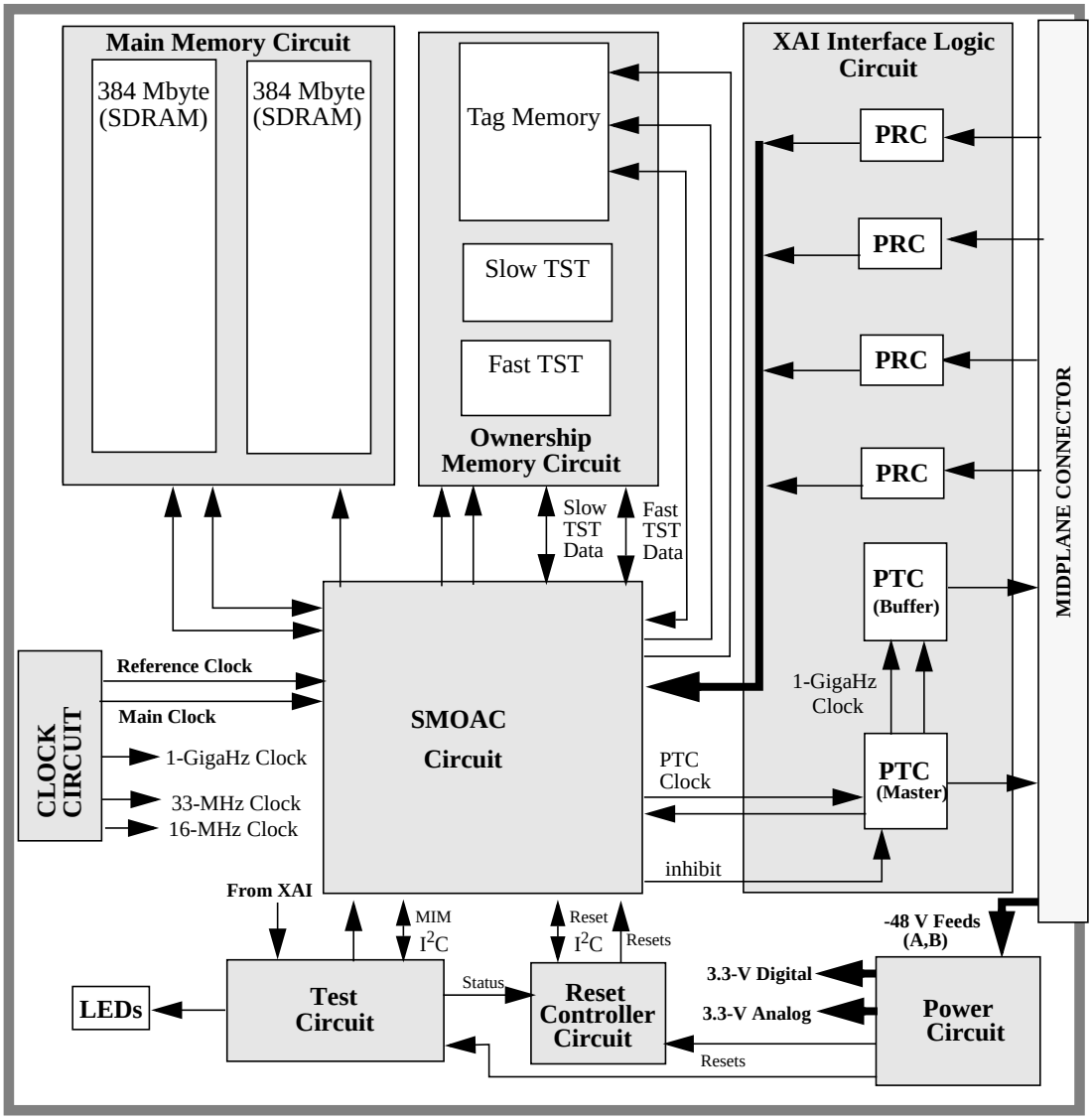
Circuits by function

The NTLX14CA SM card has circuits for functions as follows:

- main memory circuit
- ownership memory circuit
- shared memory ownership and access controller (SMOAC) circuit
- extended architecture interconnect (XAI) interface logic circuit
- power circuit
- test circuit
- reset controller circuit
- timer circuit
- clock circuit

Figure 6-13 on page 6-54 shows a block diagram of the NTLX14CA card.

Figure 6-13 NTLX14CA block diagram



Main memory circuit

The main memory circuit provides 384 Mbytes of logical memory to support data ownership and rollbacks. The logical memory has two physical 384-Mbyte memories that support two copies (A and B). The two copies in physical memory are transparent to the XA-Core software.

Ownership memory circuit

The ownership memory stores information required to perform ownership transactions. Three components of the ownership memory circuit are as follows:

- tag memory to store tag information of the memory array
- fast static random access memory (SRAM) to store task identification number (TIN) state table (TST) of the memory array
- slow SRAM to store TST information of the memory array

Shared memory ownership and access controller (SMOAC) circuit

The shared memory ownership and access controller (SMOAC) circuit is an ASIC device. The SMOAC circuit has the following main features:

- supports 40-bit logical address procedures
- provides access protection for programmed segments of memory
- does physical access translation that can program to each port
- provides interface to main memory
- provides interface to ownership memory
- provides interface to XAI midplane through the XAI interface logic
- provides dedicated output of internal faults to intelligent test controller/intelligent test master (ITC/ITM)
- provides global sanity timer for the SM card
- provides built-in self-test (BIST)
- provides interface to the ITC through serial inter-integrated circuit (I2C) port
- supports operation modes of shared memory as follows:
  - — simplex
  - — duplex
  - — triplex
  - — update
- provides diagnostic multiplex port for debug requirements
- provides statistics counters for higher system level needs
- contains and provides access to register set for SM card

Extended architecture interconnect (XAI) interface logic circuit

The extended architecture interconnect (XAI) logic circuit communicates with PE and IOP cards. The XAI logic circuit has 16 pulse receive chip (PRC) ports

on four PRC devices. The XAI logic circuit has two pulse transmitter chip (PTC) ports on two PTC devices.

The 16 PRC ports includes four receive ports for each of four PRC devices. The PRC ports receive signals from the XAI midplane and transfer data to the SMOAC device. Each PRC port receives two differential 1-Gigabit/s data stream and a 500-MHz differential clock from the XAI midplane. Data transfers to the SMOAC device as follows:

- four differential data pairs at 500 Mbits/s
- one differential frame signal
- one differential quadrature clock of 250 MHz

The two PTC ports have one port in a master mode and the second port in a buffer mode. Both of the two PTC ports have the same XAI data that goes from the SMOAC device to each side of the XAI midplane. The master PTC device receives eight signals of differential data pairs. The master PTC device also receives a 250-MHz differential clock from the SMOAC device.The with effect data rate per pair is 500 Mbytes/s for a throughput of 4 Gigabytes/s. The two ports of the PTC device can drive the midplane. The master PTC port can transmit an inhibit signal received from the SMOAC device over a dedicated status line.

Power circuit

The power circuit includes the following components:

- discrete power circuits
- local filter circuits
- de-coupling circuits
- point-of-use power supplies (PUPS) for the following:
  - 3.3-V, 25-W PUPS for the low noise analog circuits
  - 3.3-V, 50-W PUPS for all other digital circuits

Test circuit

The test circuit has the following components:

- integrated test master (ITM)
- module information memory (MIM)
- intelligent test controller (ITC)
- light-emitting diode (LED) indicators for SM card status
- access to monitor status of voltage feeds

The ITC and ITM control all SM structure tests except for BIST tests of the main memory and ownership memory. The SMOAC device controls the BIST tests of the main memory and ownership memory. The ITC and ITM automatically performs tests on power-up resets or hard resets. Faults found by The ITC and ITM tests identifies the components that have faults. The ITC and ITM log the fault information with the MIM. Fault information goes to the MIM through the interface of the inter-integrated circuit (I2C) bus on the ITM.

The joint test access group (JTAG) has test access port JTAG (TAPJ) ports available on circuits. TAPJ ports are on the ITM, ITC, SMOAC, PTC, and PRC devices. TAPJ ports are compatible with the Institute of Electrical and Electronics Engineers (IEEE) 1149.1 standard.

Reset controller circuit

The reset controller circuit controls the following:

- reset of main components on the SM card
- beginning of structure tests on the SM card
- maintain reset software for all levels of reset

The levels of reset are as follows:

- power-up reset
- hard reset that can start from
  - timeout of global sanity timer
  - reset control register RSTCLR for SMOAC
  - parity error/protocol error
  - timeout of ITC monitor
- soft reset that can start from
  - timeout of global sanity timer
  - reset control register RSTCLR for SMOAC

A hard or soft reset can start from same sources. The same sources are a timeout of the global sanity timer or the reset control register RSTCLR for SMOAC. The hard or soft reset selection depends on the values of SOFTIT and RSTPROG bits in the SMOAC.

Timer circuit

The timer circuit includes the following:

- global sanity timer in the SMOAC circuit
- ITC monitor timer in the test circuit

Clock circuit

The clock circuit has clock frequencies as follows:

- 66-MHz clock to SMOAC, main memory, ownership memory, and ownership latches by the main clock generator and the reset controller
- 66-MHz reference clock to the SMOAC by reference clock generator
- 16-MHz clock to ITC by clock generator of the test circuit
- 33-MHz clock to ITM bt clock generator of the test circuit
- 1-GigaHz clock to the master PTC from the resonator that is on the NTLX14CA SM card - the PTC converts 1-GigaHz clock to 250-MHz clock

Power requirements

The power requirements of the NTLX14CA SM card are as follows:

- input voltage range of -36 V to -75 V (nominal voltages of - 48 V and -60 V)
- output voltage of 3.3 V
- total input power of 66 W
- low voltage turn off of power
- over voltage protection
- in-rush current limit
- two battery feeds (A and B) of -48 V each
- monitor circuit for voltage feed
- electromagnetic interference (EMI) filter
- simultaneous turn off of both PUPS

NTLX20AA slot filler circuit pack

The NTLX20AA slot filler card regulates air flow from the cooling unit through the cabinet.

The NTLX20AA slot filler card has the following features:

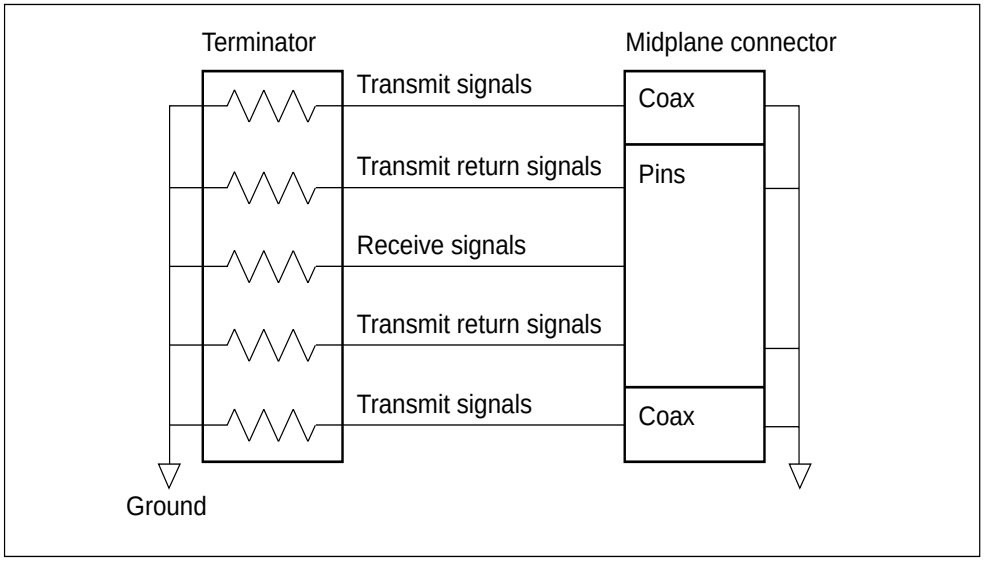
- no midplane pin or power connections
- no internal circuits
- electro-magnetic interference (EMI) shielding
- installs in slot 1F of the XA-Core shelf

NTLX20BA terminating filler circuit pack

The NTLX20BA terminating filler card provides termination for an unprovisioned slot on an XA-Core shelf. The termination is for all receive couplers and transmit paths of the unprovisioned slot. The termination reduces the effects of noise and cross talk on communication channels with PE, IOP, and SM cards. The NTLX20BA terminating filler card has a series of resistors to terminate the unprovisioned slot.

Figure 6-14 on page 6-59 shows a block diagram of the NTLX20BA terminating filler card.

Figure 6-14 NTLX20BA block diagram



7 Problem isolation and correction

This chapter describes the resident tools used to problem solve fault conditions on the eXtended Architecture Core (XA-Core). The XA-Core is on the DMS SuperNode and SuperNode SE switches. For information on nonresident tools, refer to the *Technical Assistance Manuals*.

Diagnostic tools

This chapter describes the following diagnostic tools:

- alarms
- DMS monitoring (DMSMON) tool
- log reports
- maintenance manager's morning report (AMREPORT)
- operational measurements (OM)
- OM-log-alarm cross-reference table (Table 7-1 on page 7-5)
- Sherlock
- switch performance monitoring system (SPMS)
- TRAPINFO

Alarms

Alarms are the main indicators of problems with the system. Alarms provide information about the following types of problems:

- equipment failure
- equipment that operates at a performance degrade
- equipment reached defined capacity level of the operating company
- full or partial system sanity
- software errors
- automatic recovery attempt that is unsuccessful
- reboot that is not authorized

- auto transfer to standby
- inability to transfer from a fault condition to standby
- loss of communication between entities or subsystems
- loss of ability to store operational information (*data exceeds threshold*)
- failure of inter-node transmission
- loss of communication with operation support systems
- power distribution failure
- security violations
- fire and intrusion

Three levels of severity divide the alarms:

- minor
- major
- critical

A minor alarm means a problem that does not cause a loss of service.. Examples of minor alarm conditions include the following:

- conditions that may lead to a major alarm if not corrected
- one piece of a pool of equipment that has been busied
- service degradation that has fallen below a threshold of an operating company

A major alarm means that one-half of a duplicated system is out of service. The major alarm may cause a loss of service. There is no backup if another fault occurs on the active system. A switch generates a major alarm when service degrades below a threshold of an operating company.

A critical alarm means a problem that causes a loss of service. Examples of critical alarm conditions include the following:

- loss of call processing capability (*dead system*)
- partial or full loss of system sanity
- service degradation that has fallen below a threshold of an operating company

Each alarm has a log report for reference. The log report give more detailed information about the problem than the alarm.

XA-Core system alarms appear under the XAC header of the MTC level of the MAP. For more information on alarms, refer to the chapter, “Understanding the alarm system” in the *XA-Core Maintenance Manual*, 297-8991-510.

DMSMON

DMSMON monitors changes in operation when operating company personnel change a release load. DMSMON formats the information into a report for manual or automatic generation.The type of information in the report includes the following:

- counts of internal events (*e.g. warm and cold restarts*) and downtime information
- system trap information
- counts of log reports
- hardware counts (*configuration information*)

For additional information about the DMSMON tool, refer to the *DMS Family Commands Reference Manual*, 297-1001-822.

Log reports

Log reports are a primary source of information about the components of the XA-Core. Some logs can isolate a problem to a single component. Other logs help to identify problems attributed to more than one component.

Log reports include the following information:

- severity of the log report (represented by the number of asterisks)
- type of log
- time and day
- suspected problem
- list of suspected cards

For information about the XA-Core related logs, refer to the “Logs” chapter of this document.

Maintenance manager’s morning report

AMREPORT provides a 24-h summary of performance, administrative, and maintenance information. The AMREPORT information helps maintenance

programs for correction and prevention of problems. The switch produces AMREPORT as a log report that includes the following information:

- switch performance information
  - — SPMS indicators
  - — call processing performance
  - — processor element (PE) occupancy
  - — network integrity
  - — peripheral module (PM) switch of activity (SWACT) information
  - — software performance: trap and SWER counts
  - — footprint (FP) and OM log counts
  - — information on SWACT of XMS-based peripheral module (XPM)
- scheduled test results
  - — automatic line test (ALT)
  - — automatic trunk test (ATT)
- switch operations
  - — image dump results
  - — patch summary
  - — outage indicators
  - — integrity check of table data
  - — unscheduled XPM REx test

For additional information about AMREPORT, refer to the *Digital Switching Systems DMS-100 Family Maintenance Managers Morning Report*, 297-1001-535.

Operational measurements

Operational measurements (OMs) provide load and performance information. The OM system controls collection, display, and report generation of OM data for the operating company.

For additional information about XA-Core related OMs, refer to the chapter, “Operational measurements” of this document.

Alarm, log, and OM relationship

The following table contains cross-references to alarms, logs and OMs.

Table 7-1 Alarms and related logs and operational measurement registers (Sheet 1 of 2)

Alarms	Related logs	Related OM registers
RExTst	XAC415, XAC615	XARXPE, XARXIO, XARXSM, XARXBASE, XARXFULL, XARXABRT, XARXALL
FWvers	XAC330, XAC630	none
FWsoak	XAC 631, XAC635, XAC632	none
ImgTst	XAC308, XAC608	none
Split	XAC618, XAC619	XAPEMAJU, XAMSMPXU, XARSMPXU, XASSMPXU
MemLim	XAC601, XAC801	XASM, XASMCRIU
LowPE	XAC302, XAC602	XAPE, XAPECRIU, XAPEMAJU, XARXPE
LowSM	XAC300, XAC600	XASM, XAMSMPXU, XARSMPXU, XASSMPXU
AMDI	XAC309, XAC335, XAC609	XAMDI, XAMDILNK, XAMDMAJU, XAMDCRIU
ETHR	XAC329, XAC629	XETHRMJU, XETHRCRU, XETHR, XETHRPRT, XETHRLNK
MScomm	XAC303, XAC603	XACMIC, XAIOP, XARXIO, XALKMAJU
Image	XAC308, XAC608	XARXBASE, XARXFULL
TOD	XAC304, XAC604	XAIOP, XACMIC
XATrap	XAC614, XAC814	XATRAP
Disk	XAC306, XAC606	XADISK
RTIF	XAC305, XAC605	XARTIF, XAIOP, XALOCP, XAREMP
RExSch	XAC413, XAC613	none
Tape	XAC307, XAC607	XATAPE, XAIOP
PEtbl	XAC322, XAC622	none

Table 7-1 Alarms and related logs and operational measurement registers (Sheet 2 of 2)

Alarms	Related logs	Related OM registers
IOtrbl	XAC324, XAC624	none
IOflt	XAC312, XAC612	none
SMtbl	XAC323, XAC623	none
RiBkey	XAC325, XAC625	none
WgSlot	XAC321, XAC327, XAC627	none

Sherlock

Sherlock is a data collection tool for immediate use after a service outage. Sherlock automatically collects the data required to analyze the cause of the failure. Only one person can use Sherlock at a time.

Sherlock initiates a set of parallel processes that collect all the data available for the specified type of service failure. Sherlock sends the data to a series of temporary files. A person cannot access or control the data except if the person stops the Sherlock process before data collection completes.

Once data collection completes, Sherlock creates data and console files on a specified storage device. Sherlock also erases the temporary files. The data file name is SHRKyyyymmddhhmmss(Z). The Z means the file is a compressed file. The name of the console file is SHERLOCK$OUT. The console file contains all the messages and responses sent to the terminal. The console file also contains some additional messages (e.g. time stamps).

For additional information about how to use Sherlock, refer to the *DMS Family Commands Reference Manual*, 297-1001-822.

Switch performance monitoring system

The switch performance monitoring system (SPMS) monitors all areas of switch operation and outputs regular reports on performance. The reports show different points of view.

The base for SPMS reports is the index values of OMs that the switch generates. The time covered in the SPMS report ranges from 0.5 h to one month. This range of time provides a monitor of day-to-day events and of a longer period of switch performance.

Plans for the switch performance index use SPMS results for administration purposes. The operating company can use the overall office performance index, any section of lower-level indexes, or both.

SPMS consists of three sections as follows:

- service section
- maintenance performance section
- provided resources section

For additional information about SPMS, refer to *Switch Performance Monitoring System Application Guide*, 297-1001-330.

TRAPINFO

TRAPINFO displays information about software traps. TRAPINFO gets information from the log utility and displays the information in one of several formats.

For additional information about how the TRAPINFO tool, refer to the *DMS Family Commands Reference Manual*, 297-1001-822.

8 How to problem solve a MemLim alarm

Background

Some commonly used terms

In this document, the following definitions are used.

Table 8-1 Definitions of commonly used terms (Sheet 1 of 2)

Term	Definition
memory-module	This is the basic unit of memory managed by the maintenance software. A module is 32 megabytes in size. Maintenance transfers store to the operating system's store-allocator when requested by the store-allocator. The amount transferred is one memory-module (32 megabytes) at a time. Any given module that has been transferred may only be used as data-store or program-store, never both types within the same module.
vast-area	This is the basic unit of memory managed by the operating system's store-allocator. A vast-area is 64 kilobytes is size.
spare-memory	This is memory that has not been transferred to the store-allocator. It is wholly owned by Maintenance. It always exists as a integral number of memory-modules.
available-memory	This is memory that is owned by the store-allocator but that has not been allocated to any application software. This is always an integral number of vast-areas.
used-memory	This is memory that is owned by the store-allocator that has been partially or completely allocated to application software. It is always an integral number of vast-areas.

Table 8-1 Definitions of commonly used terms (Sheet 2 of 2)

Term	Definition
free-memory	This is memory that is owned by the store-allocator and that has been assigned a particular store-type but that has not yet been allocated to any application software. It consists of the fragments of used vast-areas (see above), that are not allocated.
addressable-memory	This is the total amount of memory that can be addressed in the system. This number depends on the number of shared-memory cards in the SM-configuration. For example, a 5-card system has 768 megabytes of addressable-memory and a 10-card system has 1728 megabytes of addressable-memory.
physical-memory	This is the total amount of memory installed in the XA-Core shelf. Currently, the only memory card supported for XA-Core has 12 modules of 32 megabytes each, for a per-card total of 384 megabytes.
data-store	This is memory that can be used for storing data. There are several types of data-store (DS), such as temporary data-store (DSTEMP), protected data-store (DSPROT), etc.
program-store	This is memory that can be used for storing program instructions. There are several types of program-store, such as protected program store (PSPROT) and fast program store (PSRAM).
software-image	This is the total memory that is occupied by the software's instructions, rounded to the nearest 32 megabyte boundary, plus the total memory that is occupied by the software's data, also rounded to the nearest 32 megabyte boundary.

Addressable memory

Memory on an XA-Core is arranged such that the addressable memory range is in duplex (meaning that there are two copies of this data), and, in addition, one shared-memory card's worth of the addressable memory range is in triplex (meaning three copies). The amount of addressable memory (abbreviated here as AM) is defined by the following formula:

$$AM = \left(\frac{N-1}{2}\right) \times 384$$

where N is the number of cards, and the result is given in megabytes. The value 384 is the number of megabytes on one SM card. For example, a five-card system (N=5) has a addressable memory range of 768M. The following table, lists the addressable memory ranges against the number of shared-memory cards for systems of various sizes (note that not all of these sizes are supported in all CSPs).

Table 8-2 Configured address space against the number of shared-memory cards

Number of SM cards (N)	Addressable memory (AM)
5	768
6	960
7	1152
8	1344
9	1536
10	1728

The software image

The term image used here is defined to be the total memory that is occupied by the software's instructions, rounded to the nearest 32 megabyte boundary, plus the total memory that is occupied by the data of the software, also rounded to the nearest 32 megabyte boundary.

The image is loaded into the addressable memory on boot and it may then grow (or possibly shrink) dynamically over time. As applications request store from the support operating system (SOS), the memory resources owned by SOS are depleted. When these memory resources shrink below a certain threshold, SOS requests store to be transferred from the unused portion of the addressable memory range into the image, thereby increasing the size of the image.

One way to calculate the size of the image on a given switch running a given software load is using the value for the spare memory displayed by the store all usage command. This spare memory is the total number of kilobytes in the

unused portion of the addressable memory range, i.e. the part of the addressable memory range that does not belong to the image. The image then is all the memory that is not spare. For a 5-card system, for example, there could be 262144 kilobytes of spare reported by store all usage out of the total addressable memory range of 768 megabytes. We calculate the image by subtracting this from the total addressable memory as follows (note that kilobytes are converted to megabytes by dividing by 1024).

$$I = AM - \frac{(SPARE)}{1024} = 768 - \left(\frac{262144}{1024}\right) = 512$$

Memory limits for XA-Core

Limits imposed by software

The XA-Core memory configuration gives different upper bounds on the amounts of PS and DS for different software releases. The following table indicates these amounts.

Table 8-3 Upper bounds of PS and DS

CSP	Start of PS	End of PS	Delta
10.4	#30000000	#4FFFFFFF	512M
12, 13, 14	#30000000	#3FFFFFFF	256M

The following table defines the memory limitations for data store (DS) for the various releases of the XA-Core software. These limits are the ones imposed by the layout of the memory configuration.

Table 8-4 Memory limitations for data store

CSP	Start of PS	End of PS	Delta
10.4	#50000000	#7FFFFFFF	768M
12	#40000000	#7FFFFFFF	1024M
13, 14	#40000000	#AFFFFFFF	1792M

Limits imposed by hardware

The above tables show the limits on the amounts of PS and DS as determined by the XA-Core memory configurations imposed by software. These limits are further constrained by hardware limitations and configurations.

The limit on the amount of shared-memory PS that may be used currently depends on the amount of local PS available on the PE. There are eight 32M modules on a PE. One of these modules is reserved. That leaves seven 32M modules or 224MB. It does not matter whether the memory configuration limits PS at address 3FFFFFFF or address 4FFFFFFF since the maximum amount of shared-memory PS is 224MB which corresponds to a maximum address of #3e000000.

Both PS and DS are limited by the number of shared-memory cards installed in the XA-Core. The maximum number of cards permitted is dependent on the particular software release. The following table gives the numbers of cards and resulting amounts of physical and addressable memory.

Table 8-5 Number of SM cards and physical and addressable memory

Number of SM cards	Physical memory	Addressable memory
5	1920M	768M
7	2688M	1152M
10	3840M	1728M

Each SM card has twelve 32M modules on it for a total of 384MB. The physical memory is then just the number of cards times 384MB. The amount of addressable memory takes into consideration that one card is a spare card and hence is not counted and also that each memory module has a copy (is in duplex), as discussed above.

Since shared memory includes both PS and DS, the addressable memory maximums in the above table refer to PS plus DS. Therefore, the maximum amounts of DS that can be used will depend on the amount of PS used and vice versa. The following table gives the maximum amounts of DS possible for two example loads -- one in which the maximum amount of PS is used and one in which a typical amount of PS is used, 128MB.

Table 8-6 Maximum amount of data store for two example loads

	Max PS configuration		Max DS configuration	
Addressable Memory	Used PS	Max DS Available	Used PS	Max DS Available
768M	224M	544M	128M	640M
1152M	224M	928M	128M	1024M
1728M	224M	1504M	128M	1600M

Store allocation

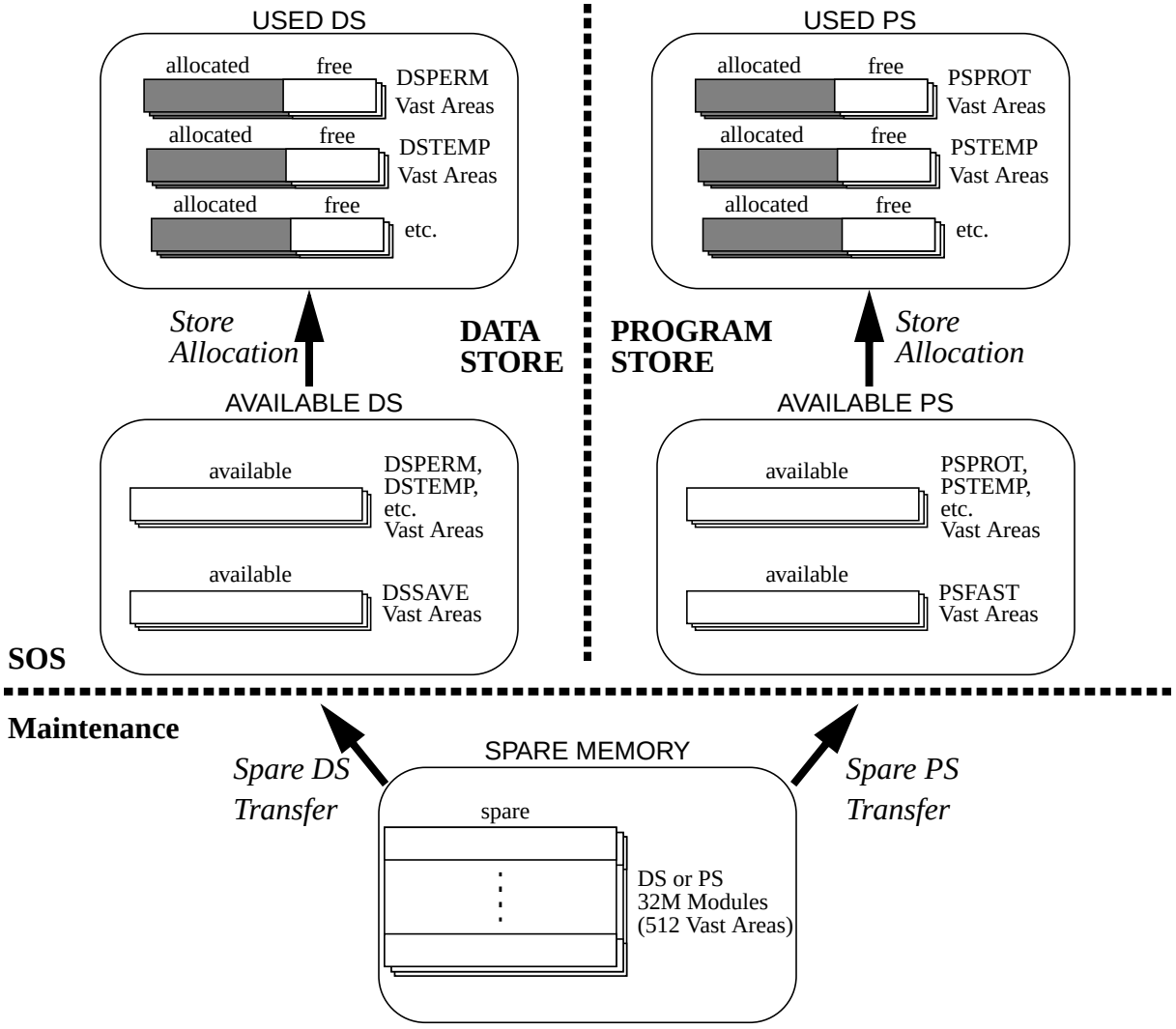
The support operating system (SOS) has a store-allocator, the purpose of which is to allocate memory to applications. Figure 8-1 shows the various pools of memory maintained by SOS and Maintenance and shows the interactions between these pools.

It can be seen from the upper two-thirds of the figure, that SOS maintains separate pools for data-store (DS) and program-store (PS) and that within these categories, there is a further subdivision between available store (DS and PS) and used store (DS and PS). Within the category of used store, the store-allocator recognizes separate pools of vast-areas of specific store-types. For example. the figure lists DSPERM and DSTEMP vast-areas for DS and PSPROT and PSTEMP vast-areas for PS. There are many other store-types not shown. These used vast-areas are partially or completely allocated to application software. The parts, or blocks, of a vast-area allocated to one or more applications are collectively labeled as allocated, while the remaining fragments, or blocks, not allocated, are labeled as free.

The store allocator also keeps separate pools of vast-areas in the available store categories (DS and PS). However, unlike the used store, the pools of vast-areas in the available store categories are flexible in that, typically, vast-areas from these pools may be allocated to one of several possible store-types. The figure shows a pool of available vast-areas that may be assigned to DSPERM and DSTEMP, among others not shown. A second pool of available vast-areas is applicable to the DSSAVE store-type. On the PS side, a pool of available vast-areas is listed that may be assigned to PSPROT and PSTEMP, among others not shown. A second pool of available PS is shown that may be applied to the PSFAST store-type.

The lower portion of the figure shows the spare memory maintained by Maintenance. This memory is handled in blocks of 32 megabytes called modules. One 32M module contains 512 vast-areas. These modules do not have any store-type associated with them while they are managed by Maintenance.

Figure 8-1 Memory pools and store allocation from spare to available to used memory pools.



When an application makes a request for a specific amount of a specific type of store, say 10 kilobytes of DSTEMP, the store-allocator first looks through its pool used vast-areas of the requested type, in this case DSTEMP, looking for a free block large enough to accommodate the request, in this case, 10 kilobytes. If such a block is found, then this block is allocated to the application.

If, however, no such block exists in the list of used vast-areas, then the store-allocator goes to the appropriate pool of available vast-areas from which a new vast-area of the requested type may be obtained. If an available vast-area exists in the appropriate pool, in this example this is the pool from which DSPERM, DSTEMP, etc., are allocated, then this vast-area is permanently

assigned the requested store-type, DSTEMP. The 10 kilobyte block is given to the application and the now-used vast-area is added to the list of used vast-areas.

If the appropriate pool of available memory is empty, the store-allocator requests a new module from the Maintenance system. Maintenance then transfers a new module to the store allocator for use as either data-store or program-store, as required. In this example, if the pool of available memory from which DSTEMP is allocated was depleted, Maintenance would transfer a module to be used as data-store. The store-allocator would replenish the pool from which DSTEMP is allocated and proceed to assign the DSTEMP store-type to a new vast-area and then allocate the requested 10K block, as discussed above. The process of transferring a module from Maintenance to the store-allocator is called store-transfer or sometimes spare-transfer (since the pool of modules owned by Maintenance is referred to as the spare-memory).

MemLim algorithm

Available-memory and store types

In order to operate properly, an XA-Core requires available resources of both data-store and program-store. There are many sub-types of memory within these two broad categories that each must be available if the switch is to be fully functional.

Program-store and data-store are allocated from a common pool of memory-modules. As discussed above, once a module has been allocated to DS or PS, the whole module must be used for this one type (DS or PS).

Not all of the DS store-types or PS store-types are allocated from a common pool of DS or PS. For example, the memory used for DSSAVE is reserved for DSSAVE alone. Similarly, DSSCRATCH is also not allocated from the common pool of available-memory for DS. Therefore, although there may be plenty of memory left for, say, DSSAVE, there may be none left for DSSTACK or DSTEMP. In this situation, the switch would not function properly, A similar argument is applicable to PS.

This is illustrated by an example. Suppose that a particular switch is configured to have five shared-memory cards, or 768 megabytes of addressable-memory. Suppose that the software load running on the switch requires 98 megabytes of program-store. The number of modules needed for PS in this case would be four, or 128 megabytes. However, of this 128 megabytes, only 100 megabytes is used, leaving 30 megabytes available.

Subtracting 128 megabytes from 768 megabytes gives 640 megabytes, the remaining memory that can be used for DS. Suppose the software requires 632 megabytes of DS. This leaves 8 megabytes of available-memory for DS.

The total available-memory is then 30 megabytes of PS plus 8 megabytes of DS, or 38 megabytes in total. However, of the 8 megabytes of available DS, a certain portion will be for DSSAVE only, say two vast-areas or 128 kilobytes, and a certain portion will be for DSSCRATCH only, say 125 vast-areas or 8000 kilobytes. Since 8 megabytes is 128 vast-areas, this leaves 128 minus 125, minus 2, or just one vast-area of 64 kilobytes for DSTEMP, DSPROT, DSPERM, etc.

It can be seen from this example then, that in raising the MemLim alarm, it is important to treat PS and DS separately and to examine the availability of the store-types within the DS and PS categories.

Determining the MemLim alarm level

The MemLim alarm algorithm treats the program-store and data-store store-types separately. The minor alarm is based on the total available DS or PS memory. The major alarm pays attention to the availability of a critical set of DS types and a critical set of PS types.

The following is the algorithm for determining the MemLim alarm level based on the usage of data-store.

1. Determine if a DS store-transfer is possible.
    a. Determine if there is any spare-memory. If there is none, a store-transfer is not possible. Otherwise, proceed to step 1b).
    b. If there is some spare-memory then determine if the address-space for DS will be exceeded by a store-transfer. If yes, then a store-transfer is not possible.
    c. If a store-transfer is possible, then there is no alarm situation. Otherwise proceed to step 2.
2. Determine the amount of available DS reported by SOS.
    a. If the available DS for the critical subset of DS store types is eight vast-areas or less, then the system raises the MemLim MAJOR alarm.
    b. Otherwise, if the total available DS is less than 32 megabytes, then the system raises the MemLim MINOR alarm.

    Now look at the algorithm for raising the MemLim alarm based on the usage of program store.

3. Determine if a PS store-transfer is possible.

   a. Determine if there is any spare-memory. If there is none, a store-transfer is not possible. Otherwise, proceed to step 3b).

   b. If there is some spare-memory, then determine if the address-space for PS will be exceeded by a store-transfer or if the PE cards have exhausted their local spare-memory. If yes, then a store-transfer is not possible.

   If a store-transfer is possible, then there is no alarm situation. Otherwise proceed to step 4.

4. Determine the amount of available PS reported by SOS.

   a. If the available PS for the critical subset of PS store types is one vast-area or less, then the system raises the MemLim MAJOR alarm.

   b. Otherwise, if the total available PS is less than eight megabytes, then the system raises the MemLim MINOR alarm.

5. These independent DS and PS alarm results are combined so that the highest applicable alarm level is reported on the MAP and in the logs. The following “truth table” defines how the DS and PS alarms are combined.

Table 8-7 Truth table for combining DS and PS alarms

DS Alarm Test Result	PS Alarm Test Result	MemLim Alarm Status
none	none	none
Minor	none	Minor
Major	none	Major
none	Minor	Minor
Minor	Minor	Minor
Major	Minor	Major
none	Major	Major
Minor	Major	Major
Major	Major	Major

Memory fragmentation

As indicated in the background section, used-memory refers to vast-areas that are at least partially allocated. The remaining parts that are not allocated are referred to as free. These free areas can be of any size. When an application needs memory, if it is looking for a small block, it the store allocator might be

able to find a vast-area of the right store-type that has a free block on it large enough to satisfy the application's request. However, if no used vast-areas of the right type have a block of sufficient size, a new available vast-area will need to be used.

The MemLim algorithm does not consider the free blocks as being available. The reason for this is that it is necessary to be sure that future requests for any store-type and of any size can be satisfied, not just smaller requests or requests for certain store-types.

XSMEMLIM diagnostic tools

XSMEMLIM command

There is a need for the ability to display the numerical data used in calculating the MemLim alarm status. The XSMEMLIM command is designed to provide this data.

Table 8-8 The XSMEMLIM command

SYNTAX	XSMEMLIM
DESCRIPTION	Displays information about the memory limits and related alarm status.
EXAMPLE	xsmemlim

In order to display this information, use the XSMEMLIM command as follows:

Command input:

```
>xsmemlim
```

The following is an example MAP response display:

```
Memory Limits Statistics

Total addressable memory:  786432 Kbytes
Spare memory:                   0 Kbytes

Store     Available   Available   Major       Minor       Transfers
Alarm Type
          Memory Crt  Memory Any  Limit       Limit       Okay
Status
          (Kbytes)    (Kbytes)    (Kbytes)    (Kbytes)
 DS           576        8704       512       32768       NO
minor
 PS         23552       27712        64        8192       NO
no alarm
 TOTAL      24128       36416

MemLim Alarm Status: minor
```

In the DS row there are 576 kilobytes of available store in the critical set of store-types and there are 8704 kilobytes of available store in total. The limits for the major and minor alarms are 512 kilobytes and 32768, respectively. Since 8704 is less than 32768, and 576 is greater than 512, the MemLim minor is asserted. There are more than 27 megabytes of available PS.

Suppose that another vast-area of DSTEMP was allocated on a switch in the state shown in the above XSMEMLIM sample output. The the XSMEMLIM command, if run again, would show the following:

Command input:

```
>xsmemlim
```

The following is an example MAP response display:

```
Memory Limits Statistics

Total addressable memory:  786432 Kbytes
Spare memory:                   0 Kbytes

Store     Available   Available   Major       Minor       Transfers
Alarm Type
          Memory Crt  Memory Any  Limit       Limit       Okay
Status
          (Kbytes)    (Kbytes)    (Kbytes)    (Kbytes)
 DS           512        8640       512       32768       NO
major
 PS         23552       27712        64        8192       NO
no alarm
 TOTAL      24064       36352

MemLim Alarm Status: major
```

The number of kilobytes of available-memory in the critical set of store-types is now 512 and equal to the major limit. For this reason, the MemLim major is raised.

STORE command

The SOS store-allocator provides a command that may be used to investigate many aspects of store-allocation. Information is available on:

- amounts of allocated and free store for each store type
- amounts of available DS and PS
- amount of spare memory
- which applications are using which type of store, and how much
- many others

A brief overview of the STORE command follows.

The syntax of the STORE command is of the form

```
store <store-type> <parameter> [<option>...]
```

The <store-type> argument may be any of the store-types listed in Table 8-9, or ALL, to perform the store command on all store-types; or DS, to perform the command on all data-store types; or PS to perform the command on all program-store types; or DUMPDS, to perform the command on all types of DS that are dumped; or DUMPPS, to perform the command on all types of PS that

are dumped; or VALIDDS, to perform the command on all valid DS types; or VALIDPS, to perform the command on all valid PS types.

The <parameter> argument may be any one of the parameters listed in Table 8-10 on page 8-17. Depending on the selected parameter, there may be one or more options specified.

Table 8-9 List of store-types for the STORE command. (Sheet 1 of 3)

Store-type	Description
dstemp_blocking	Temporary data store
dsram_blocking	Permanent protected data store
dsperm_blocking	Permanent unprotected data store
pstemp_write_blocking	Temporary program store
dssave_blocking	Permanent data store saved over reboots.
psprot_write_blocking	Permanent program store
dssram_blocking	Fastest DSTEMP (68k)
pssram_write_blocking	Fastest PSPROT (68k)
dsipl_write_blocking	DS used by genimage for IPLUNLOAD modules
psipl_write_blocking	PS used by genimage for IPLUNLOAD modules
dsfprot_write_blocking	Fast DSPROT (68k)
dsfperm_blocking	Fast DSPERM (68k)
dsdbunprot_blocking	Unprotected DABM store similar to DSUNPROT
psfast_write_blocking	Fastest PSPROT unused by GENIMAGE.
dspperm_blocking	Permanent data store saved over reloads
dsdbtemp_blocking	Temporary DABM data store.
dsdbperm_blocking	Permanent DABM data store saved over restarts.
dsdbprot_write_blocking	Protected DABM data store saved over restarts.
psalien_write_blocking	XS store used by SOS to boot unix
dsxprot_write_blocking	XS store shared by Unix and SOS
dsxperm_blocking	XS store shared by Unix and SOS
dsxtemp_blocking	XS store shared by Unix and SOS
psxshare_write_blocking	XS shared program store (SOS/VM)
dsstack_blocking	Process Stacks and Private Segments
dssos_blocking	O.S. Private Info (PCBs, PSTs, Pool headers.)
dssosprot_write_blocking	O.S. Protected Private Info (Robust Queues).
dsunprot_blocking	Unprotected store saved over all restarts except reboot
dsscratch	Scratch memory, Similar to DSFPERM but contents not guaranteed to survive a context switch. On XA-Core this is local memory.
dsstor_blocking	Reserved for those additional storetypes needed on both the old and new store allocator.

Table 8-9 List of store-types for the STORE command. (Sheet 2 of 3)

Store-type	Description
dsstorprot_write_blocking	Reserved for those additional storetypes needed on both the old and new store allocator.
dstemp_write_blocking	Temporary data store
dsram_write_blocking	Fastest DSPERM
dsprot_blocking	Permanent protected data store
dsperm_write_blocking	Permanent unprotected data store
pstemp_blocking	Temporary program store
dssave_write_blocking	Permanent data store saved over reboots.
psprot_blocking	Permanent program store
dssram_write_blocking	Fastest DSTEMP (68k)
pssram_blocking	Fastest PSPROT (68k)
dsipl_blocking	DS used by genimage for IPLUNLOAD modules
psipl_blocking	PS used by genimage for IPLUNLOAD modules
dsfprot_blocking	Fast DSPROT (68k)
dsfperm_write_blocking	Fast DSPERM (68k)
dsdbunprot_write_blocking	Unprotected DABM store similar to DSUNPROT
psfast_blocking	Fastest PSPROT unused by GENIMAGE.
dspperm_write_blocking	Permanent data store saved over reloads
dsdbtemp_write_blocking	Temporary DABM data store.
dsdbperm_write_blocking	Permanent DABM data store saved over restarts.
dsdbprot_blocking	Protected DABM data store saved over restarts.
psalien_blocking	XS store used by SOS to boot unix
dsxprot_blocking	XS store shared by Unix and SOS
dsxperm_write_blocking	XS store shared by Unix and SOS
dsxtemp_write_blocking	XS store shared by Unix and SOS
psxshare_blocking	XS shared program store (SOS/VM)
dsstack_write_blocking	Process Stacks and Private Segments
dsstack_write_blocking	Process Stacks and Private Segments
dssos_write_blocking	O.S. Private Info (PCBs, PSTs, Pool headers.)
dsfprot_blocking	O.S. Protected Private Info (Robust Queues).
dsunprot_write_blocking	Unprotected store saved over all restarts except reboot
dsstor_write_blocking	Reserved for those additional storetypes needed on both the old and new store allocator.
dsstorprot_blocking	Reserved for those additional storetypes needed on both the old and new store allocator.
dstemp_mixed_blocking	Temporary data store

Table 8-9 List of store-types for the STORE command. (Sheet 3 of 3)

Store-type	Description
dsram_mixed_blocking	Fastest DSPERM
dsprot_mixed_blocking	Permanent protected data store
dsperm_mixed_blocking	Permanent unprotected data store
pstemp_mixed_blocking	Temporary program store
dssave_mixed_blocking	Permanent data store saved over reboots.
psprot_mixed_blocking	Permanent program store
dssram_mixed_blocking	Fastest DSTEMP (68k)
pssram_mixed_blocking	Fastest PSPROT (68k)
dsipl_mixed_blocking	DS used by genimage for IPLUNLOAD modules
psipl_mixed_blocking	PS used by genimage for IPLUNLOAD modules
dsfprot_mixed_blocking	Fast DSPROT (68k)
dsfperm_mixed_blocking	Fast DSPERM (68k)
dsdbunprot_mixed_blocking	Unprotected DABM store similar to DSUNPROT
psfast_mixed_blocking	Fastest PSPROT unused by GENIMAGE.
psfast_mixed_blocking	Fastest PSPROT unused by GENIMAGE.
dspperm_mixed_blocking	Permanent data store saved over reloads
dsdbtemp_mixed_blocking	Temporary DABM data store.
dsdbperm_mixed_blocking	Permanent DABM data store saved over restarts.
dsdbprot_mixed_blocking	Protected DABM data store saved over restarts.
psalien_mixed_blocking	XS store used by SOS to boot unix
dsxprot_mixed_blocking	XS store shared by Unix and SOS
dsxperm_mixed_blocking	XS store shared by Unix and SOS
dsxtemp_mixed_blocking	XS store shared by Unix and SOS
psxshare_mixed_blocking	XS shared program store (SOS/VM)
dsstack_mixed_blocking	Process Stacks and Private Segments
dssos_mixed_blocking	O.S. Private Info (PCBs, PSTs, Pool headers.)
dsfprot_mixed_blocking	O.S. Protected Private Info (Robust Queues).
dsunprot_mixed_blocking	Unprotected store saved over all restarts except reboot
dsstor_mixed_blocking	Reserved for those additional storetypes needed on both the old and new store allocator.
dsstorprot_mixed_blocking	Reserved for those additional storetypes needed on both the old and new store allocator.

Table 8-10 STORE command parameter options

Parameter	Description
SCAN	Print information about specific blocks of store.
OWNERS	Print information about store sorted by owner.
SUMMARY	Print a summary of information about each specified store-type.
USAGE	Print information about the usage of the specified store-types.
AREAS	Print information about each specified store area.
FRAGMENTATION	Print statistics about the current levels of fragmentation.
INFO	Print miscellaneous information about the specified store-types.
BLOCKADDR	Print information about the block of store at a specific address.
PROBE	Probe for memory hardware configuration information at the specified address.
ATTRIBUTES	Print the memory attributes (blocking, write_blocking, etc.) for the store at the specified address.

Forms of the STORE SCAN command

The following tables show the available forms of the STORE SCAN command

Table 8-11 The STORE SCAN BLOCKS command

SYNTAX	STORE <store-type> SCAN BLOCKS <from> <to> [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays information about all the blocks of store that lie between the <from> address and the <to> address. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan blocks #4012366a #4012ffff

Table 8-12 The STORE SCAN RANGE command

SYNTAX	STORE <store-type> SCAN RANGE <from> <to> [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays a summary of information about each store-type represented in the set of blocks that lie between the address <from> and the address <to>. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan range #4012366a #4012ffff

Table 8-13 The STORE SCAN BLKSIZE command

SYNTAX	STORE <store-type> SCAN BLKSIZE [<from>] [<to>] [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays information about blocks that have a size within the specified bounds <from> bytes up to <to> bytes. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan blksize #00000010 #00000050

Table 8-14 The STORE SCAN MODULE command

SYNTAX	STORE <store-type> SCAN MODULE <name> [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays information about the blocks owned by the specified module. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan module ‘willtrap’

Table 8-15 The STORE SCAN PROCESS command

SYNTAX	STORE <store-type> SCAN PROCESS <name> [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays information about the blocks owned by the specified process. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan process ‘daddy’

Table 8-16 The STORE SCAN USER command

SYNTAX	STORE <store-type> SCAN USER <name> [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays information about the blocks of store owned by the specified user. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan user ‘someuser’

Table 8-17 The STORE SCAN ID command

SYNTAX	STORE <store-type> SCAN ID <id1> <id2> [VERBOSE]
DESCRIPTION	This form of the STORE SCAN command displays information about the blocks of store owned by the specified numeric owner ID. The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ds scan id #030B #0000

Table 8-18 The STORE SCAN ALL command

SYNTAX	STORE <store-type> SCAN ALL [VERBOSE]
DESCRIPTION	This version of the STORE SCAN command displays information about all of the blocks of the specified store-type.The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ps scan all

Table 8-19 The STORE SCAN FREE command

SYNTAX	STORE <store-type> SCAN FREE [VERBOSE]
DESCRIPTION	This version of the STORE SCAN command displays information about all of the free blocks of the specified store-type.The optional flag VERBOSE may be specified to display more information.
EXAMPLE	store ps scan free

STORE OWNERS command

The STORE OWNERS command displays information about blocks of memory where the block information is listed in sorted-order to that the owners with the most store can be easily determined.

Table 8-20 The STORE OWNERS command

SYNTAX	STORE <store-type> OWNERS [<n>] [<min>] [<max>]
DESCRIPTION	This commands displays the information about blocks of store sorted in decreasing order of total store allocated by owner. The option <n> may be used to limit the display to n owners. The options <min> and <max> may be used to select only owners of blocks of size ranging from <min> bytes to <max> bytes.
EXAMPLE	store dstemp owners 10

STORE SUMMARY command

The STORE SUMMARY command displays summary information about all the blocks the blocks of the specified store-types. The summary data includes information on free and allocated blocks in terms of their maximum, minimum, and total sizes.

Table 8-21 The STORE SUMMARY command

SYNTAX	STORE <store-type> SUMMARY
DESCRIPTION	Display a summary of information on all the blocks of the specified store-type.
EXAMPLE	store dstemp_blocking summary

STORE USAGE command

The STORE USAGE command displays information about the current usage of the specified store-types. This information includes the numbers of allocated and free kilobytes for each store-type.

Table 8-22 The STORE USAGE command

SYNTAX	STORE <store-type> USAGE
DESCRIPTION	Displays information about the usage of the specified store-types.
EXAMPLE	store dstemp_blocking usage

STORE AREAS command

The STORE AREAS command displays information about all the vast-areas of the specified store-types. Note that this can be a very large display that might take many minutes to display on a MAP terminal. There are options to this command that can filter the output to display only those areas of interest.

Table 8-23 The STORE AREAS command

SYNTAX	STORE <store-type> AREAS [<from>] [<to>] [<status>]
DESCRIPTION	Displays information about all the vast-areas of the specified store-types. The option starting and ending address <from> and <to> may be specified to narrow the set of areas displayed. The optional status selector may be any one of avail, beingformed, inuse, or corrupted.
EXAMPLE	store pstemp areas inuse

STORE FRAGMENTATION command

The STORE FRAGMENTATION command displays statistics about the fragmentation present in the memory-system.

Table 8-24 The STORE FRAGMENTATION command

SYNTAX	STORE <store-type> FRAGMENTATION
DESCRIPTION	Displays the fragmentation statistics.
EXAMPLE	store all fragmentation

STORE INFO command

The STORE INFO command displays information about each specified store-type.

Table 8-25 The STORE INFO command

SYNTAX	STORE <store-type> INFO [VERBOSE]
DESCRIPTION	Displays information about the specified store-types.
EXAMPLE	store dstemp info verbose

STORE BLOCKADDR command

The STORE BLOCKADDR command display information about the block of memory at the specified address.

Table 8-26 The STORE BLOCKADDR command

SYNTAX	STORE <store-type> BLOCKADDR <address>
DESCRIPTION	Displays information about the block of memory at the given address.
EXAMPLE	store ds blockaddr #4489FC00

STORE PROBE command

The STORE PROBE command displays memory hardware related information for the specified address.

Table 8-27 The STORE PROBE command

SYNTAX	STORE <store-type> PROBE <address>
DESCRIPTION	Displays memory hardware information about the specified address.
EXAMPLE	store ds probe #4489E000

STORE ATTRIBUTES command

The STORE ATTRIBUTES command displays the memory attribute for the memory-line at the specified address. Use this command to determine the memory at the specified address is write blocking, or blocking, etc.

Table 8-28 The STORE ATTRIBUTES command

SYNTAX	STORE <store-type> ATTRIBUTES <address>
DESCRIPTION	Displays the attribute for the memory line at the given address.
EXAMPLE	store ds attributes #419D0000

Using the STORE command

The following are some examples showing how the STORE command can be used to display information about memory.

To display information about store usage across all store-types, use the STORE command as follows:

Command input:

```
>store all usage
```

The following is an example MAP response display:

```
Info based on inuse DS areas
Storetype       Used      Free     Total   % Used
DSTEMP_B       14525Kb      66Kb   14591Kb    99%
DSPROT_W       17114Kb     165Kb   17279Kb    99%
DSPERM_B       70159Kb      48Kb   70207Kb    99%
DSSAVE_B        1306Kb      37Kb    1343Kb    97%
DSFPROT_W         26Kb      38Kb      64Kb    40%
DSPPERM_B          2Kb      61Kb      63Kb     3%
DSSTACK_B       5076Kb     108Kb    5184Kb    97%
DSSOS_B          525Kb      50Kb     575Kb    91%
DSUNPROT_B     10701Kb      50Kb   10751Kb    99%
DSSCRATCH         55Kb       8Kb      63Kb    87%
DSSTOR_B        1005Kb      82Kb    1087Kb    92%
DSSTORPROT_W    3406Kb     113Kb    3519Kb    96%
DSTEMP_W          55Kb       8Kb      63Kb    87%
DSPROT_B           6Kb      57Kb      63Kb     9%
DSPERM_W        2868Kb      11Kb    2879Kb    99%
DSSOS_W          460Kb      51Kb     511Kb    90%
DSUNPROT_W         1Kb      62Kb      63Kb     1%
DSTEMP_M         183Kb       8Kb     191Kb    95%
DSPROT_M           8Kb      55Kb      63Kb    12%
DSPERM_M         225Kb      30Kb     255Kb    88%
DSSOS_M           35Kb      28Kb      63Kb    55%
TOTAL DS      127750Kb    1136Kb  128886Kb    99%

TOTAL BASED ON ALL DS AREAS
TOTAL DS: USED = 127750Kb  AVAIL =  11385Kb  TOTAL = 139135Kb
%USED = 91%

Info based on inuse PS areas
Storetype       Used      Free     Total   % Used
PSPROT_W        5344Kb      95Kb    5439Kb    98%
PSSRAM_W         445Kb       2Kb     447Kb    99%
PSFAST_W       27643Kb     516Kb   28159Kb    98%
FIRMWARE_DLL    4160Kb       0Kb    4160Kb   100%
TOTAL PS       37593Kb     613Kb   38206Kb    87%

TOTAL BASED ON ALL PS AREAS
TOTAL PS: USED =  37593Kb  AVAIL =  27942Kb  TOTAL =  65535Kb
%USED = 51%
```

To display the top ten users of DSTEMP_BLOCKING store. use the STORE command as follows:

Command input:

```
>store dstemp_blocking owners 10
```

The following is an example MAP response display:

```
Collecting DSTEMP_B owner information... please wait...

Statistics for owners of DSTEMP_B, ordered by total size
Blocks  TotalSize Min       Max       OwnerId     Process  Module
User
    845 #006E39A0 #00000060 #00006020 #017A,#0000          MPBMSUI
   1212 #0012D780 #000000E0 #0000F020 #6000,#5002
   1051 #00121A80 #00000040 #00005940 #0180,#0000          MTSKERN
      7 #0004C0E0 #00002020 #0000E020 #03D6,#0000          SSCIDEBG
    136 #00045100 #00000820 #00000820 #0BDA,#0000
BLKMONUI
     34 #00044580 #000000C0 #00004020 #03DA,#0000
XLTRSMUI
      3 #0002FA60 #0000FE20 #0000FE20 #04F8,#0000          VMCTCT
      9 #0002F200 #00000040 #000080A0 #0746,#0000          DKCACHUI
     66 #0002BF60 #000000E0 #00010000 #0107,#0000
XLFIDBUI
    173 #000296A0 #00000040 #00003E00 #018D,#0000
SIPDATPI
```

To display information about blocks of memory in a particular address range, use the STORE SCAN command as follows:

Command Input:

```
>store all scan blocks #40000000 #40010000
```

The following is an example MAP response display:

The following is an example MAP response display:

```
Store block data for: DSSAVE_B
Start     Size      Storetype    OwnerId     Process  Module   User
#40000000 #000005A0 DSSAVE_B     #00A3,#0000          STOR
.
.
.
#4000E0E0 #00001000 DSSAVE_B     #00BA,#0000          TRAPDEFS

Storetype    Ttl     Ttl       Min       Max       Avail
             Blks    Size      Blk       Blk       64k
             Free    Free      Free      Free      Pages
DSSAVE_B           1 #00000F20 #00000F20 #00000F20       0

Totals:            1 #00000F20                          0

Storetype    Ttl     Ttl       Min       Max       Inuse
             Blks    Size      Blk       Blk       64k
             Allcd   Allcd     Allcd     Allcd     Pages
DSSAVE_B          16 #0000F0E0 #00001000 #000052E0       2

Totals:           16 #0000F0E0                          2
```

To display information about memory owned by a particular module, use the STORE command as follows:

Command input:

```
>store psprot_write_blocking scan module stor
```

The following is an example MAP response display:

```
store dsperm scan module willtrap

Storetype    Ttl   Ttl       Min       Max
             Blks  Size      Blk       Blk
             Owned Owned     Owned     Owned
DSPERM_B           1 #000000C0 #000000C0 #000000C0

Totals:            1 #000000C0
```

Diagnosing a MemLim alarm

When a MemLim alarm (major or minor) appears on the shared-memory level of the maintenance map, or when a MemLim log appears in the XAC log stream, the following actions may be taken to determine the cause of the alarm.

The first step is to use the XSMEMLIM command. The output of this command directly shows whether the alarm is due to a shortage of available program store or a shortage of available data store.

If there is a shortage of program store indicated by XSMEMLIM then it may be that the maximum physical limit of 224 megabytes of program store is near to being reached. Or it may be that there is no spare memory and the remaining available memory to SOS is less than the MemLim threshold.

If the XSMEMLIM tool shows that the alarm is due to a shortage of data store, then it may be that the spare memory has been all used up and the remaining available data store is less than a MemLim threshold.

The STORE command can be used to determine how store is being used and if there is an errant process or module that is allocating too much memory.

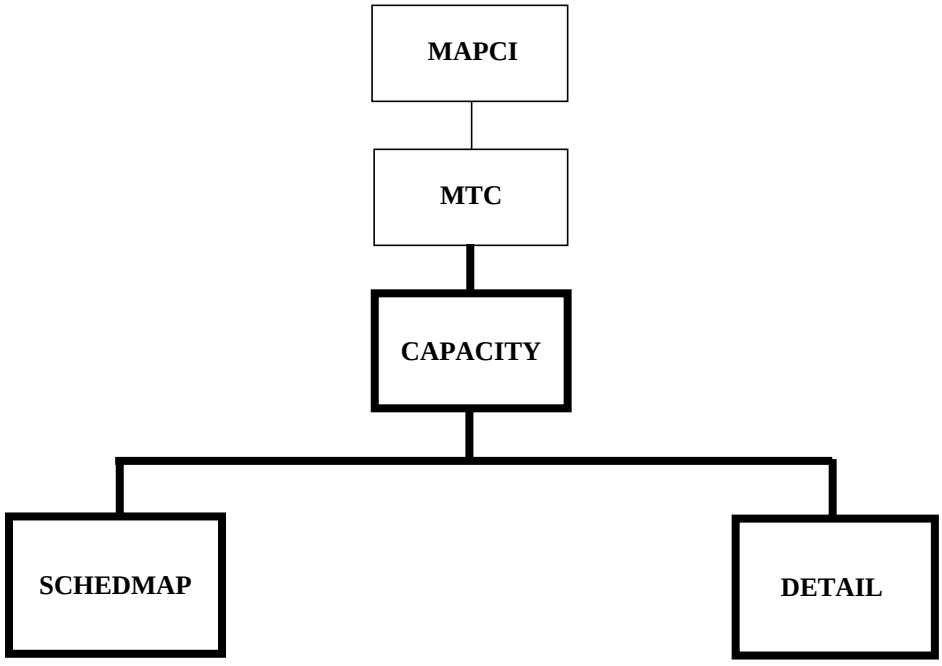
9 Capacity-monitoring tools in an XA-Core

Overview

The capacity-monitoring tools for an XA-Core are based on the CPSTATUS/CPSTAT and ACTIVITY monitoring tools used by the DMS SuperNode to monitor CM capacity.

The Capacity MAP and CAPCI interface have replaced CPSTATUS/CPSTAT and ACTIVITY. The Capacity MAP level supports two MAP sub-levels, SCHEDMAP and DETAIL.

Figure 9-1 Capacity MAP hierarchy



The capacity-monitoring tools introduce a set of logs to provide capacity information for future analysis, as well as an operational measurement (OM)

group to measure central processing unit (CPU) usage on an XA-Core. New office parameters CAP_MAX_DUR and RATED_POWER have also been added.

The following table contains an overview of the capacity measurements provided in an XA-Core.

Table 9-1 Overview of capacity measurements in an XA-Core (Sheet 1 of 4)

		New for XA-Core		
Measurement	**UNIT**	**Y**	**N**	**Description**
CATMP/HR	Number		X	Call attempts per hour.
UTIL	Percent		X	Current call attempts as a percentage of Engineered Call Attempts.
ENGCATMP	Number		X	Projected engineered call attempts per hour at which all grade of service specifications are met. This value is based on the Rated Power of the office, and does not take the processing power of the spare PE into account.
MAXCATMP	Number	X		Projected maximum call attempts per hour at which all grade of service specifications are met. This value includes all PEs, including those provisioned for reliability.
COMPLEX	Percent		X	Ratio of the relative complexity of the call mix running on a switch. This is useful for comparing call mix complexity between different switches.
ENGLEVEL	ABOVE/ BELOW		X	Current utilization is above or below office parm CC_ENGLEVEL_WARNING_THRESHOLD. This parm has a default value of 100.
CCOVRLD	ON/OFF		X	Status of Central Control Overload controls in the last minute.
PESC	YES/NO	X		PE State Change indicator. ‘YES’ indicates a PE state change occurred during the last minute.
SCHED	Percent		X	Observed scheduler overhead utilization relative to the expected overhead occupancy at capacity (Expected occupancy or OCCexp = 8%).
FORE	Percent		X	Observed operating system utilization relative to the expected occupancy at capacity. Foreground includes SYSTEMCLASS, SYSTOOLCLASS, INITCLASS (OCCexp = 1%).
MAINT	Percent		X	Observed MAINTCLASS utilization relative to the expected occupancy at capacity (OCCalloc = 8%).

Table 9-1 Overview of capacity measurements in an XA-Core (Sheet 2 of 4)

Measurement	UNIT	New for XA-Core Y	New for XA-Core N	Description
DNC	Percent		X	Observed NOSFTCLASS utilization relative to the expected occupancy allocated at capacity. DNC includes NOSFT class (OCCalloc = 3%).
AUXCP	Percent		X	Observed AUXCPCLASS utilization relative to the expected occupancy at capacity. This value can be altered via the office parm AUXCP_CPU_SHARE (OCCalloc = 1% to 25%).
OM	Percent		X	Observed OM utilization relative to the expected occupancy at capacity. OM includes GOMCLASS and NGOMCLASS (OCCalloc = 3%).
GTERM	Percent		X	Observed GTERMCLASS utilization relative to the expected occupancy at capacity. This value can be altered via the office parm GUARANTEED_TERMINAL_CPU_SHARE (OCCalloc = 2% to 16%).
BKG	Percent		X	Observed background classes utilization relative to the expected occupancy at capacity. Background includes BKGCLASS and AUDITCLASS (OCCalloc = 3%).
NETM	Percent		X	Observed NETMTCCLASS utilization relative to the expected occupancy allocated at capacity (OCCalloc = 0%).
SNIP	Percent		X	Observed SNIPCLASS utilization relative to the expected occupancy at capacity (OCCalloc = 1%).
OAvgDel	Number		X	Weighted average waiting time on the CCB originating queue.
95%OLim	Number		X	This represents the 95% high water mark for the CCB originating queue.
PAvgDel	Number		X	Weighted average waiting time on the CCB progress queue.
95%PLim	Number		X	This represents the 95% high water mark for the CCB progress queue.
BAvgDel	Number		X	Weighted average waiting time on the Background (BKGCLASS) ready queue.
95%BLim	Number		X	This represents the 95% high water mark for the Background ready queue.

Table 9-1 Overview of capacity measurements in an XA-Core (Sheet 3 of 4)

Measurement	UNIT	New for XA-Core Y	New for XA-Core N	Description
MAvgDel	Number	X		Weighted average waiting time on the Maintenance (MAINTCLASS) ready queue.
95%MLim	Number	X		This represents the 95% high water mark for the Maintenance ready queue.
OrigDeny	Number		X	OM field in OM group CP. Origination denial counts the number of originations that are ignored because they were not serviced within 3s of arrival.
InefDeny	Number		X	OM field in OM group CP2. Ineffective Deny counts the origination/abandon pairs that are ignored because they were not serviced within 0.5s from the time the origination arrived.
LCMdtsr	Percent		X	LCM dial tone speed recording.
LMdtsr	Percent		X	LM dial tone speed recording.
XASUTIL	Percent		X	Current Payload Utilization. Provides average over transfer period (%).
XASPUTIL	Percent	X		Provides Peak Payload Utilization value over the transfer period (%).
XASCMPLX	Percent		X	Call Complexity Ratio.
XASSCHED	Percent		X	Scheduler Overhead percent utilization.
XASFORE	Percent		X	Foreground percent utilization.
XASMAINT	Percent		X	Maintenance Class percent utilization.
XASDNC	Percent		X	NOSFT Class percent utilization.
XASOM	Percent		X	OM percent utilization.
XASGTERM	Percent		X	GTerm Class percent utilization.
XASBKG	Percent		X	Background percent utilization.
XASAUXCP	Percent		X	AUXCP Class percent utilization.
XASNETM	Percent		X	NETM Class percent utilization.
XASSNIP	Percent		X	SNIP Class percent utilization.
XASPESC	Number	X		Number of one minute intervals in the transfer period during which a PE state change occurred.

Table 9-1 Overview of capacity measurements in an XA-Core (Sheet 4 of 4)

Measurement	UNIT	New for XA-Core Y	New for XA-Core N	Description
XASNXFR	Number	X		Number of transfer periods accumulated in this OM report. If there is one transfer period accumulated in this report, this OM will output 1.
XASOVER	Number	X		Number of one minute intervals in the transfer period during which system utilization was greater than 100%.
XASOTHLD	Number	X		Number of one minute intervals in the transfer period during which system utilization exceeded the CC_ENGLEVEL_WARNING_THRESHOLD.

Capacity MAP level

The Capacity MAP levels provide the user with information necessary to manage XA-Core capacity. Select the CAPACITY option from the MTC MAP level to access the Capacity MAP level.

The Capacity MAP level provides high level information on office capacity. Measurements update every minute. The SCHEDMAP and DETAIL sub-levels provide the user with more detail on XA-Core capacity.

Figure 9-2 Capacity MAP level

```
 XACM      MS     IOD     Net      PM     CCS     Lns    Trks    Ext     APPL
  .        .       .       .       .       .       .       .       .       .

CAPACITY
 0 Quit     CATMP/HR UTIL ENGCATMP MAXCATMP COMPLEX ENGLEVEL CCOVRLD PESC
 2 Parms      120000   75   160000   200000     120    BELOW     OFF   NO
 3 SchedMap
 4 Detail
 5
 6
 7
 8
 9
10
11
12
13
14
15
16
17 StrtLog
18 StopLog
 XMAP0
Time  14:12   >
```

CAPACITY MAP field definitions

The following section describes the information presented in CAPACITY MAP level to the user.

Note: When multiple PEs are out of service, the information displayed in the following fields is incorrect and invalid: UTIL, ENGCATMP, MAXCATMP, COMPLEX, and ENGLEVEL.

CATMP/HR

This field defines the current call attempts per hour.

The call attempts data is obtained from registers in the OFZ and OTS Operational measurement (OM) groups. Table 9-2 provides additional information on the specific registers used from these OM groups.

Table 9-2 OM registers used to determine Call Rate

OM Field	OM Group	Description
NIN	OFZ	Number of incoming calls.
NIN2	OFZ	Extension register for NIN.
NORIG	OFZ	Number of originating calls.
NORIG2	OFZ	Extension register for NORIG.
NINC	OTS	Number of incoming call attempts.
NINC2	OTS	Extension register for NINC.
NORG	OTS	Number of originating call attempts.
NORG2	OTS	Extension register for NORG.

Note: OMs OCINI, OCCMS and RONATT are used in TOPS offices.

UTIL

This field defines the current utilization of the call processing capacity.

Call processing capacity utilization reports in a manner similar to BRISC. However the XA-Core performance curve is non-linear. This non-linearity is a result of the parallel processing nature of XA-Core. CPU time is necessary to ensure the integrity of shared data. This time is not constant and is a function of the current call rate, call mix and the amount of non-payload work performed. It is included in the calculation of utilization.

Calculate utilization as a ratio of the current call processing activity to the projected engineered call processing activity for the current call mix. ENGCATMP defines the engineered call rate.

$$\text{Utilization} = \frac{\text{CATMP/HR}}{\text{ENGCATMP}} \times 100$$

For example, if ENGCATMP is projected to be 1,000,000 calls/hour and the current call rate is 600,000 calls/hour, the utilization is reported as 60%.

Utilization reports a dash (‘-’) if the value is less than 20%, with the actual percentage subject to further study under traffic conditions. The capacity prediction algorithm needs a sufficient traffic level to report accurate results.

Note: When multiple PEs are out of service, the information displayed in the UTIL field is incorrect and invalid.

ENGCATMP

The engineered call attempts per hour field Indicates the projected engineered calls per hour for the current call mix at capacity.

The engineered call capacity is based on the rated power of the office. The spare processing power is not included in the calculation. Since most offices will normally be provisioned with one spare PE, a single PE fault will not have an affect on ENGCATMP. If a PE failure reduces the available processing power to a value less than the rated power of the office, then the ENGCATMP value will decrease. The ENGCATMP value will then be based on the processing power currently provided by all in-service PEs.

The value of ENGCATMP also changes according to the current call mix and the CPUtime guaranteed to non-CallP scheduler classes. Feature rich calls require more CPUtime. As the call mix becomes more complex, the ENGCATMP value decreases. Increasing the office parameter settings for AUXCP_CPU_SHARE or GUARANTEED_TERMINAL_CPU_SHARE decreases the amount of time available to do call processing work. This lowers the value of ENGCATMP. Changing the allocated percentages for SNIP, NOSFT, or other engineerable classes also affects the value of ENGCATMP. Utilization has an inverse relation to ENGCATMP, and therefore any decreases in the engineered call attempts value leads to an increase in utilization.

Utilization reports a dash (‘-’) if the value is less than 20%, with the actual percentage subject to further study under traffic conditions. The capacity prediction algorithm needs a sufficient traffic level to report accurate results.

Note: When multiple PEs are out of service, the information displayed in the ENGCATMP field is incorrect and invalid.

MAXCATMP

This field indicates the maximum call attempts per hour for the current call mix at capacity, including all in-service and spare PEs.

Unlike BRISC, this value also takes GOS specifications into account. The delta between MAXCATMP and ENGCATMP (when all PEs are in-service) provides an indication of the call capacity of the spare PEs.

Unlike ENGCATMP, MAXCATMP changes when the spare PE fails and will report a value identical to ENGCATMP. MAXCATMP is also affected by call mix and CPUtime guaranteed to non-CallP scheduler classes similar to ENGCATMP.

Utilization reports a dash ('-') if the value is less than 20%, with the actual percentage subject to further study under traffic conditions. The capacity prediction algorithm needs a sufficient traffic level to report accurate results.

Note: When multiple PEs are out of service, the information displayed in the MAXCATMP field is incorrect and invalid.

COMPLEX

This field represents the relative complexity of the call mix running on a switch and is useful for comparing the call complexity between different switches without influence from other measurements. ENGCATMP does not allow this. COMPLEX is identical to the measurement reported in BRISC offices.

Complexity varies with CPU capacity required to process a call type. Feature rich real-time intensive call types increase the complexity reported by the switch. The higher the call complexity, the lower the call mix.

Call complexity is reported as a percentage of the standard model. A call complexity ratio of 100% indicates that the complexity of the call mix of the switch matches the complexity of the call mix of the standard. A switch reporting a call complexity percentage of less than 100 is running a less complex call mix and can be expected to achieve a higher call rate than the standard model. A call complexity of more than 100 indicates a switch that will achieve a lower maximum call rate due to the increased complexity of its call mix. Call complexity is updated every minute using the following formula.

$$\text{Complexity} = \frac{\text{Standard office call rate}}{\text{Standardized ENGCATMP}}$$

Complexity calculates using a standardized ENGCATMP so switches that use different office parameter settings can still be compared based on the following scheduler share settings.

Table 9-3 Scheduler share settings (Sheet 1 of 2)

Parameter	Utilization
GTERM:	2%

Table 9-3 Scheduler share settings (Sheet 2 of 2)

Parameter	Utilization
AUXCP:	1%
NETMTC:	0%
NOSFT:	0%

Unless the office parameter settings are identical to the standard office, the standardized ENGCATMP value used in complexity will be different from the ENGCATMP value displayed at the Capacity MAP level.

Utilization reports a dash (‘-’) if the value is less than 20%, with the actual percentage subject to further study under traffic conditions. The capacity prediction algorithm needs a sufficient traffic level to report accurate results.

Note: When multiple PEs are out of service, the information displayed in the COMPLEX field is incorrect and invalid.

ENGLEVEL

This field reports ABOVE if the current utilization is greater than, or BELOW if the current utilization is less than the office parameter CC_ENGLEVEL_WARNING_THRESHOLD. This parameter has a default value of 100.

Note: When multiple PEs are out of service, the information displayed in the ENGLEVEL field is incorrect and invalid.

CCOVRLD

The call processing overload field reports ON or OFF depending on the state of the call processing overload controls in the previous minute.

PESC

The processor element state change indicator field reports YES if a PE state change occurred during the last minute. Otherwise, the PESC field reports NO.

Capacity menu commands

Menu commands appear on the MAP command menu. Non-menu commands do not appear on the MAP menu list. Enter both menu and non-menu commands in the command interpreter input area.

Table 9-4 contains a summary description Capacity MAP level commands.

Table 9-4 Summary of Capacity MAP commands

Command	Menu #	Type	Function
Detail	4	Nav	Display the Detail MAP sub-level.
Parms	2	Info	Display the current settings for office parameters and other engineerable settings.
Quit	0	Nav	Exit from the MAP level and display the MTC MAP level.
SchedMap	3	Nav	Display the SchedMap sub-level.
StopLog_	17	Op	Stops a log of Capacity MAP information.
StrtLog_	18	Op	Starts a log of Capacity MAP information.

Detail

The Detail command is a menu command. The Detail command instructs the XA-Core system to display the Detail MAP level.

Menu selection number
4

Type
Navigational

Parameters
There are no command parameters.

Options
There are no command options.

Command format examples
Example use of the Detail command is shown in Table 9-5. The Detail command syntax is shown in the example below:

COMMAND

Table 9-5 Detail command examples

Command example	Command description
>Detail	Exit from the current MAP session and display the DETAIL MAP level.

Parms

The Parms command displays the current setting for office parameters and other engineerable settings that affect call processing capacity. The following information displays:

GUARANTEED_TERMINAL_CPU_SHARE: Displays the current setting for this office parameter in table OFCENG. This value determines the expected occupancy for GTERM at capacity and determines the ratio shown in the GTERM field on the SchedMAP sub-level.

AUXCP_CPU_SHARE: Displays the current setting for this office parameter in table OFCENG. This value determines the expected occupancy for AUXCP at capacity and determines the ratio shown in the AUXCP field on the SchedMAP sub-level.

CC_ENGLEVEL_WARNING_THRESHOLD: Displays the current setting for this office parameter in table OFCENG (default value of 100). This value triggers the display for the ENGLEVEL field at the Capacity MAP level and uses the value ABOVE or BELOW.

NETM Share setting: Time allocated to NETMTC class. This value determines the expected occupancy for NETM at capacity and determines the ratio shown in the NETM field on the SchedMAP sub-level.

DNC Share setting: Time allocated to NOSFT class. This value determines the expected occupancy for NOSFT at capacity and determines the ratio shown in the DNC field on the SchedMAP sub-level.

SNIP Share setting: Time allocated to SNIP class. This value determines the expected occupancy for SNIP at capacity and determines the ratio shown in the SNIP field on the SchedMAP sub-level.

1% CPU Allocation: Relates the drop or increase in the engineered call attempts per hour expected based on a one percent change in the total CPU time guaranteed to a non-callp scheduler class.

Menu selection number

2

Type

Informational

Parameters

There are no command parameters.

Options
There are no command options.

Command format examples
Example use of the Parms command is shown in Table 9-6. The Parms command syntax is shown in the example below:

COMMAND

Table 9-6 Parms command examples

Command example	Command description
>Parms	Provides information on the current setting of office parameters and other engineerable settings.

Quit

The Quit command is a common menu command. The Quit command instructs the XA-Core system to exit from the current MAP session. You can exit to any MAP level that is higher in the MAP level hierarchy.

Note: The XA-Core system continues to execute any previous commands entered.

Menu selection number
0

Type
Navigational

Parameters
The Quit command parameters are optional.

All
Use the <all> parameter to terminate all XA-Core MAP sessions and display the CI prompt.

Incrname
Use the <incrname> parameter to end the current MAP session and display a MAP level higher in the MAP system hierarchy. Enter a MAP level name. The XA-Core system displays the MAP level that is one level higher in the MAP system hierarchy than the <incrname> (increment name) value.

Nlevel
Use the <nlevel> parameter to end the current MAP session and display a MAP level higher in the MAP system hierarchy. Enter a number value to

represent the number of DMS MAP levels to step back in the MAP system hierarchy.

Options
There are no command options.

Command format examples
Example use of the Quit command is shown in Table 9-7. The Quit command syntax is shown in the example below:

COMMAND <parameter>

Table 9-7 Quit command examples

Command example	Command description
>QUIT	Use the Quit command with no parameters to exit from the current MAP session. Display a MAP level that is one level above the current MAP session level.
>QUIT mtc	QUIT <incrname>: Exit the current MAP session. Display the MAP level that is one level above the indicated MAP level name.
>QUIT 2	QUIT <nlevel>: Exit the current MAP session. Display the MAP level that is two levels above the current MAP session in the MAP hierarchy.
>QUIT all	QUIT <all>: Exit from all MAP sessions and display the CI prompt.

SchedMAP
The SchedMAP command is a menu command. The SchedMAP command instructs the XA-Core system to display the SChedMAP MAP level.

Menu selection number
3

Type
Navigational

Parameters
There are no command parameters.

Options
There are no command options.

Command format examples
Example use of the SchedMAP command is shown in Table 9-8. The SchedMAP command syntax is shown in the example below:

COMMAND

Table 9-8 SchedMAP command examples

Command example	Command description
>SchedMAP	Exit from the current MAP session and display the SchedMAP MAP level.

StopLog_
The StopLog_ command is a menu command. The StopLog_ command instructs the log system to begin a log of Capacity MAP information.

Note: The StopLog_ command will stop all capacity logs, not just those started by the user who entered the command.

Menu selection number
17

Type
Operational

Parameters
The StopLog_ command requires command parameters. If the user does not enter any parameters or enters invalid parameters, the MAP terminal displays an error message. The MAP terminal prompts the user to enter a correct parameter value.

All
Stops all logs.

Capacity
Stops CAP100 and CAP101 logs.

Detail
Stops CAP100, CAP101 and CAP103 logs.

SchedMAP
Stops CAP100, CAP101 and CAP102 logs.

Options
There are no command options

Command format examples
Example use of the StopLog command is shown in Table 9-9. The StopLog command syntax is shown in the example below:

COMMAND <parameter>

Table 9-9 StopLog command examples

Command example	Command description
>StopLog all	Stop all capacity logs currently running.
>StopLog capacity	Stop CAP100, CAP101 and CAP102 logs.
>StopLog detail	Stop CAP103 logs.
>Stoplog schedmap	Stop Cap100, CAP101 and CAP102 logs.

StrtLog_
The StrtLog_ command is a menu command. The StrtLog_ command instructs the log system to begin a log of Capacity MAP information.

Note: The CAP103 log uses additional CPU time. The user will receive a warning message when starting this log.

Menu selection number
18

Type
Operational

Parameters
The StrtLog_ command requires command parameters. If the user does not enter any parameters or enters invalid parameters, the MAP terminal displays an error message. The MAP terminal prompts the user to enter a correct parameter value.

All
Starts all logs.

Brief
Starts all logs except CAP103.

Capacity
Starts CAP100 and CAP101 logs.

Detail
Starts CAP100, CAP101 and CAP103 logs.

Duration
An integer value from 16 to 255 that specifies how long the log should be left running. The maximum of 255 is a default value that can be changed in office parameter CAP_MAX_DURATION.

Forever
If this parameter is entered, logs will continue to run until the StopLog command is entered.

SchedMAP
Starts CAP100, CAP101 and CAP102 logs.

Options
There are no command options.

Command format examples
Example use of the StrtLog command is shown in Table 9-10. The StrtLog command syntax is shown in the example below:

COMMAND <parameter>

Table 9-10 StrtLog command examples

Command example	Command description
>StrtLog all 16	Starts all capacity logs currently running for 16 minutes.
>StrtLog brief 16	Starts all logs except CAP103 for 16 minutes.
>StrtLog capacity 16	Starts CAP100, CAP101, CAP102 logs for 16 minutes.
>StrtLog detail 16	Starts CAP103 logs for 16 minutes.
>Strtlog schedmap forever	Starts Cap100, CAP101 and CAP102 logs until the user enters the StopLog command.

SchedMAP MAP level

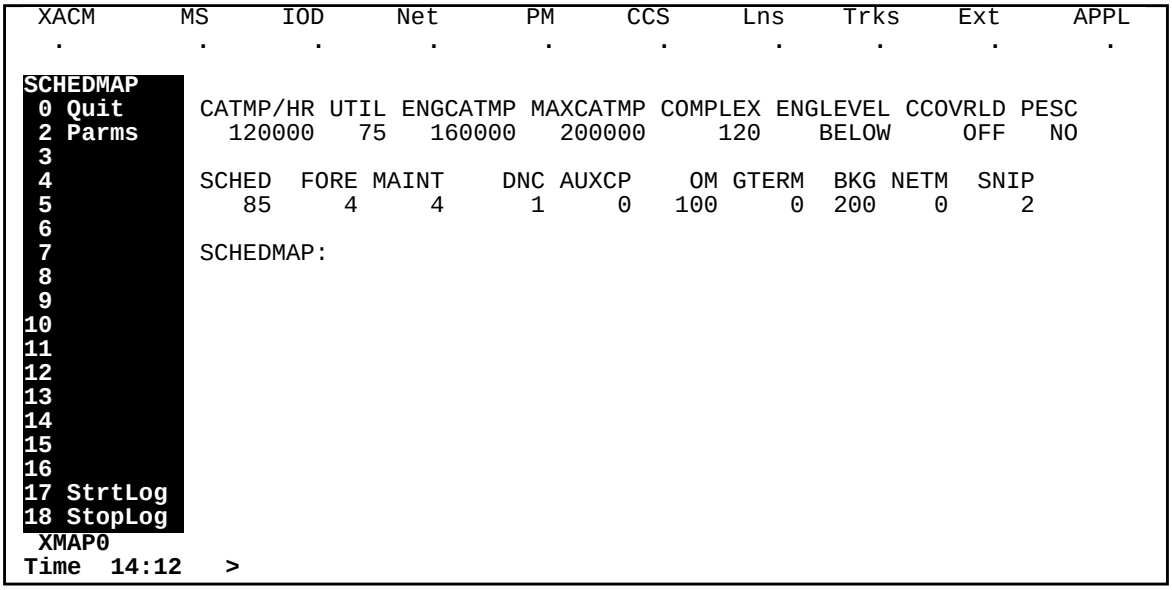
The SchedMAP MAP level provides information on the Scheduler system, displaying utilization values. The class or class group utilization calculates as follows

Class Utilization= Current time used by class X 100
Time allocated or guaranteed for class

When a switch is running at capacity, most of the scheduler class fields are at or below 100. However, spare processing power reserved to handle PE faults is distributed evenly to all in-service PEs. Time not being used by CallP may be used by other classes. This occurs even at capacity. Therefore, a BKG utilization greater than a 100 can occur at capacity. Similarly, when a switch is not at capacity, some of the scheduler fields can show high values. This occurs because time not being used for call processing can be used by other classes.

Office parameters AUXCP and GTERM settings can be changed in table OFCENG. Changing these parameters will alter the amount of time that is available for call processing and change the reported call capacity utilization and ENGCATMP values. They will also impact the AUXCP and GTERM utilizations reported at the SchedMap sub-level.

Figure 9-3 SchedMAP level



SchedMAP MAP field definitions

The following section describes the information presented in SchedMAP MAP level.

> ***Note:*** The expected occupancy (OOC_{exp}) and allocated occupancy (OCC_{alloc}) values are default values as of NA007.

AUXCP

This field contains the observed AUXCPCLASS utilization relative to the expected occupancy at capacity. This value is variable since it can be altered via the office parm AUXCP_CPU_SHARE (OCC_{alloc} = 1% to 25%).

BKG

The field contains background class utilization relative to the expected occupancy at capacity. Background includes BKGCLASS and AUDITCLASS (OCC_{alloc} = 3%).

DNC

The DNC field contains the observed NOSFTCLASS utilization relative to the expected occupancy allocated at capacity. DNC includes NOSFT class (OCC_{alloc} = 3%). This value is variable since it can be altered through packaging.

FORE

The foreground field contains operating system utilization relative to the expected occupancy at capacity. Foreground includes SYSTEMCLASS, SYSTOOLCLASS and INITCLASS (OCC_{exp} = 1%).

GTERM

This contains the observed GTERMCLASS utilization relative to the expected occupancy at capacity. This value is variable since it can be altered via the office parm GUARANTEED_TERMINAL_CPU_SHARE. Default value set to 2% (OCC_{alloc} = 2% to 16%).

MAINT

This field contains the observed MAINTCLASS utilization relative to the expected occupancy at capacity (OCC_{alloc} = 8%).

NETM

This field contains the NETMTCCLASS utilization relative to the expected occupancy allocated at capacity (OCC_{alloc} = 0%). This value is variable since it can be altered via packaging.

OM

The OM field contains the observed OM utilization relative to the expected occupancy at capacity. OM includes GOMCLASS and NGOMCLASS (OCC_{alloc} = 3%).

SCHED

This field contains the observed scheduler overhead utilization relative to the expected overhead occupancy at capacity (OCC_{exp} = 8%).

SNIP

This field contains the observed SNIPCLASS utilization relative to the expected occupancy at capacity (OCC_{alloc} = 1%).

SchedMAP menu commands

Menu commands appear on the MAP command menu. Non-menu commands do not appear on the MAP menu list. Enter both menu and non-menu commands in the command interpreter input area.

Table 9-11 contains a summary description SchedMAP MAP level commands.

Table 9-11 Summary of SchedMAP MAP commands

Command	Menu #	Type	Function
Parms	2	Info	Display the current settings for office parameters and other engineerable settings.
Quit	0	Nav	Exit from the MAP level and display the MTC MAP level.
StopLog_	17	Op	Stops a log of Capacity MAP information.
StrtLog_	18	Op	Starts a log of Capacity MAP information.

Parms

The Parms command displays the current setting for office parameters and other engineerable settings that affect call processing capacity. The following information displays:

GUARANTEED_TERMINAL_CPU_SHARE: Displays the current setting for this office parameter in table OFCENG. This value determines the expected occupancy for GTERM at capacity and determines the ratio shown in the GTERM field on the SchedMAP sub-level.

AUXCP_CPU_SHARE: Displays the current setting for this office parameter in table OFCENG. This value determines the expected occupancy for AUXCP

at capacity and determines the ratio shown in the AUXCP field on the SchedMAP sub-level.

CC_ENGLEVEL_WARNING_THRESHOLD: Displays the current setting for this office parameter in table OFCENG (default value of 100). This value triggers the display for the ENGLEVEL field at the Capacity MAP level and uses the value ABOVE or BELOW.

NETM Share setting: Time allocated to NETMTC class. This value determines the expected occupancy for NETM at capacity and determines the ratio shown in the NETM field on the SchedMAP sub-level.

DNC Share setting: Time allocated to NOSFT class. This value determines the expected occupancy for NOSFT at capacity and determines the ratio shown in the DNC field on the SchedMAP sub-level.

SNIP Share setting: Time allocated to SNIP class. This value determines the expected occupancy for SNIP at capacity and determines the ratio shown in the SNIP field on the SchedMAP sub-level.

1% CPU Allocation: Relates the drop or increase in the engineered call attempts per hour expected based on a one percent change in the total CPU time guaranteed to a non-callp scheduler class.

Menu selection number
2

Type
Informational

Parameters
There are no command parameters.

Options
There are no command options.

Command format examples
Example use of the Parms command is shown in Table 9-12. The Parms command syntax is shown in the example below:

COMMAND

Table 9-12 Parms command examples

Command example	Command description
>Parms	Provides information on the current setting of office parameters and other engineerable settings.

Quit

The Quit command is a common command. The Quit command instructs the XA-Core system to exit from the current MAP session. You can exit to any MAP level that is higher in the MAP level hierarchy.

Note: The XA-Core system continues to execute any previous commands entered.

Menu selection number
0

Type
Navigational

Parameters
The Quit command parameters are optional.

All
Use the <all> parameter to terminate all XA-Core MAP sessions and display the CI prompt.

Incrname
Use the <incrname> parameter to end the current MAP session and display a MAP level higher in the MAP system hierarchy. Enter a MAP level name. The XA-Core system displays the MAP level that is one level higher in the MAP system hierarchy than the <incrname> (increment name) value.

Nlevel
Use the <nlevel> parameter to end the current MAP session and display a MAP level higher in the MAP system hierarchy. Enter a number value to represent the number of DMS MAP levels to step back in the MAP system hierarchy.

Options
There are no command options.

Command format examples

Example use of the Quit command is shown in Table 9-13. The Quit command syntax is shown in the example below:

COMMAND <parameter>

Table 9-13 Quit command examples

Command example	Command description
>QUIT	Use the Quit command with no parameters to exit from the current MAP session. Display a MAP level that is one level above the current MAP session level.
>QUIT mtc	QUIT <incrname>: Exit the current MAP session. Display the MAP level that is one level above the indicated MAP level name.
>QUIT 2	QUIT <nlevel>: Exit the current MAP session. Display the MAP level that is two levels above the current MAP session in the MAP hierarchy.
>QUIT all	QUIT <all>: Exit from all MAP sessions and display the CI prompt.

StopLog_

The StopLog_ command is a menu command. The StopLog_ command instructs the log system to begin a log of Capacity MAP information.

Note: The StopLog_ command will stop all capacity logs, not just those started by the user who entered the command.

Menu selection number

17

Type

Operational

Parameters

The StopLog_ command requires command parameters. If the user does not enter any parameters or enters invalid parameters, the MAP terminal displays an error message. The MAP terminal prompts the user to enter a correct parameter value.

All
Stops all logs.

Capacity
Stops CAP100 and CAP101 logs.

Detail
Stops CAP100, CAP101 and CAP103 logs.

SchedMAP
Stops CAP100, CAP101 and CAP102 logs.

Options
There are no command options.

Command format examples
Example use of the StopLog command is shown in Table 9-14. The StopLog command syntax is shown in the example below:

COMMAND <parameter>

Table 9-14 StopLog command examples

Command example	Command description
>StopLog all	Stop all capacity logs currently running.
>StopLog capacity	Stop CAP100, CAP101, and CAP120 logs.
>StopLog detail	Stop CAP103 logs.
>Stoplog schedmap	Stop Cap100, CAP101 and CAP102 logs.

StrtLog_
The StrtLog_ command is a menu command. The StrtLog_ command instructs the log system to begin a log of Capacity MAP information.

Note: The CAP103 log uses additional CPU time. The user will receive a warning message when starting this log.

Menu selection number
18

Type
Operational

Parameters
The StrtLog_ command requires command parameters. If the user does not enter any parameters or enters invalid parameters, the MAP terminal displays an error message. The MAP terminal prompts the user to enter a correct parameter value.

All
Starts all logs.

Brief
Starts all logs except CAP103.

Capacity
Starts CAP100 and CAP101 logs.

Detail
Starts CAP100, CAP101 and CAP103 logs.

Duration
An integer value from 16 to 255 that specifies how long the log should be left running. The maximum of 255 is a default value that can be changed in office parameter CAP_MAX_DURATION.

Forever
If this parameter is entered, logs will continue to run until the StopLog command is entered.

SchedMAP
Starts CAP100, CAP101 and CAP102 logs.

Options
There are no command options.

Command format examples
Example use of the StrtLog command is shown in Table 9-15. The StrtLog command syntax is shown in the example below:

COMMAND <parameter>

Table 9-15 StrtLog command examples (Sheet 1 of 2)

Command example	Command description
>StrtLog all 16	Starts all capacity logs currently running for 16 minutes.
>StrtLog brief 16	Starts all logs except CAP103 for 16 minutes.

Table 9-15 StrtLog command examples (Sheet 2 of 2)

Command example	Command description
>StrtLog capacity 16	Starts CAP100, CAP101 and CAP102 logs for 16 minutes.
>StrtLog detail 16	Starts CAP103 log for 16 minutes.
>Strtlog schedmap forever	Starts Cap100, CAP101 and CAP102 logs until the user enters the StopLog command.

Detail MAP level

The Detail MAP sub-level provides information on call processing utilization and scheduler queues.

> ***Note:*** Accessing this sub-level causes an increase in utilization as collecting and reporting the information requires additional CPU time. The user will receive a warning message when accessing this sub-level.

The Detail sub-level uses a timer to stop monitoring and collecting data to prevent unnecessary increases in utilization. Office parameter CAP_MAX_DURATION in table OFCENG sets the value of the timer. The default value for the timer is 255 minutes. Each user who enters the Detail sub-level will reset the timer for all users. Monitoring and collection of information will end when the user exits the MAP sub-level, or the timer expires.

Figure 9-4 Detail MAP level

```
 XACM      MS     IOD     Net      PM     CCS     Lns    Trks    Ext     APPL
  .        .       .       .       .       .       .       .       .       .

DETAIL
 0 Quit     CATMP/HR UTIL ENGCATMP MAXCATMP COMPLEX ENGLEVEL CCOVRLD PESC
 2 Parms      120000   75   160000   200000     120    BELOW     OFF   NO
 3
 4          OAvgDel 95%OLim PAvgDel 95%PLim BAvgDel 95%BLim           TIMER
 5             17ms    45ms    13ms    25ms    13ms    25ms        03:30:45
 6
 7          MavgDel 95%MLim OrigDeny InefDeny LCMdtsr LMdtsr
 8             12ms    25ms      --       --      --     --
 9
10          Detail:
11
12          WARNING:
13           Please be advised that accessing this sub-level utilizes
14           additional CPU time.
15
16
17 StrtLog
18 StopLog
 XMAP0
Time  14:12   >
```

Detail MAP field definitions

The following section describes the information presented in SchedMAP MAP level.

95%BLim

The 95% background limit field is the same as 95% originating limit field but using the background priority queue (RDYBW) figures.This field represents the 95% high water mark for the background ready queue.

95%MLim

The 95% maintenance limit field represents the 95% high water mark for the maintenance ready queue.

95%OLim

The 95% originating limit field represents the 95% high water mark for the CCB originating queue.

95%PLim

The 95% progress limit field is the same as 95% originating limit field but using data on the CCB progress queue as opposed to the CCB originating queue. This field represents the 95% high water mark for the CCB progress queue.

BAvgDel

The background average delay field contains the weighted average waiting time on the background (BKGCLASS) ready queue.

InefDeny

The Ineffective Deny field is found in OM group CP2. The register counts origination/abandon pairs that are ignored because they were not serviced within 0.5s from the time the origination arrived.

LCMdtsr

The LCM dial tone speed recording field is the ratio of the number of calls delayed by more than 3s on LCMs, over the total number of calls processed by LCMs.

LMdtsr

The LM dial tone speed recording field is the ratio of the number of test calls delayed by more than 3s on LMs, over the total number of test calls processed by the LMs.

MAvgDel

The maintenance average delay field contains the weighted average waiting time on the maintenance (MAINTCLASS) ready queue.

OAvgDel

The originating average delay field contains the weighted average waiting time on the CCB originating queue.

OrigDeny

The origination denial field is found in OM group CP. The register counts originations that are ignored because they were not serviced within 3s of arrival.

PAvgDel

The progress average delay field is the same as the originating average delay field, but using data on the CCB progress queue as opposed to the CCB originating queue.

TIMER

This field indicates how much time is remaining until the data monitoring system is automatically shut off. The timer initializes to the value of CAP_MAX_DURATION and updates once every minute. Each time the seconds portion of the timer reaches 00, the MAP display updates. The timer resets to the value of CAP_MAX_DURATION if another user enters the Detail MAP level, or the Detail logs begin.

SchedMAP menu commands

Menu commands appear on the MAP command menu. Non-menu commands do not appear on the MAP menu list. Enter both menu and non-menu commands in the command interpreter input area.

Table 9-16 contains a summary description SchedMAP MAP level commands.

Table 9-16 Summary of SchedMAP MAP commands

Command	Menu #	Type	Function
Parms	2	Info	Display the current settings for office parameters and other engineerable settings.
Quit	0	Nav	Exit from the MAP level and display the MTC MAP level.
StopLog_	17	Op	Stops a log of Capacity MAP information.
StrtLog_	18	Op	Starts a log of Capacity MAP information.

Parms

The Parms command displays the current setting for office parameters and other engineerable settings that affect call processing capacity. The following information displays:

GUARANTEED_TERMINAL_CPU_SHARE: Displays the current setting for this office parameter in table OFCENG. This value determines the expected occupancy for GTERM at capacity and determines the ratio shown in the GTERM field on the SchedMAP sub-level.

AUXCP_CPU_SHARE: Displays the current setting for this office parameter in table OFCENG. This value determines the expected occupancy for AUXCP at capacity and determines the ratio shown in the AUXCP field on the SchedMAP sub-level.

CC_ENGLEVEL_WARNING_THRESHOLD: Displays the current setting for this office parameter in table OFCENG (default value of 100). This value triggers the display for the ENGLEVEL field at the Capacity MAP level and uses the value ABOVE or BELOW.

NETM Share setting: Time allocated to NETMTC class. This value determines the expected occupancy for NETM at capacity and determines the ratio shown in the NETM field on the SchedMAP sub-level.

DNC Share setting: Time allocated to NOSFT class. This value determines the expected occupancy for NOSFT at capacity and determines the ratio shown in the DNC field on the SchedMAP sub-level.

SNIP Share setting: Time allocated to SNIP class. This value determines the expected occupancy for SNIP at capacity and determines the ratio shown in the SNIP field on the SchedMAP sub-level.

1% CPU Allocation: Relates the drop or increase in the engineered call attempts per hour expected based on a one percent change in the total CPU time guaranteed to a non-callp scheduler class.

Menu selection number

2

Type

Informational

Parameters

There are no command parameters.

Options
There are no command options.

Command format examples
Example use of the Parms command is shown in Table 9-17. The Parms command syntax is shown in the example below:

COMMAND

Table 9-17 Parms command examples

Command example	Command description
>Parms	Provides information on the current setting of office parameters and other engineerable settings.

Quit

The Quit command is a common menu command. The Quit command instructs the XA-Core system to exit from the current MAP session. You can exit to any MAP level that is higher in the MAP level hierarchy.

Note: The XA-Core system continues to execute any previous commands entered.

Menu selection number
0

Type
Navigational

Parameters
The Quit command parameters are optional.

All
Use the <all> parameter to terminate all XA-Core MAP sessions and display the CI prompt.

Incrname
Use the <incrname> parameter to end the current MAP session and display a MAP level higher in the MAP system hierarchy. Enter a MAP level name. The XA-Core system displays the MAP level that is one level higher in the MAP system hierarchy than the <incrname> (increment name) value.

Nlevel
Use the <nlevel> parameter to end the current MAP session and display a MAP level higher in the MAP system hierarchy. Enter a number value to

represent the number of DMS MAP levels to step back in the MAP system hierarchy.

Options
There are no command options.

Command format examples
Example use of the Quit command is shown in Table 9-18. The Quit command syntax is shown in the example below:

COMMAND <parameter>

Table 9-18 Quit command examples

Command example	Command description
>QUIT	Use the Quit command with no parameters to exit from the current MAP session. Display a MAP level that is one level above the current MAP session level.
>QUIT mtc	QUIT <incrname>: Exit the current MAP session. Display the MAP level that is one level above the indicated MAP level name.
>QUIT 2	QUIT <nlevel>: Exit the current MAP session. Display the MAP level that is two levels above the current MAP session in the MAP hierarchy.
>QUIT all	QUIT <all>: Exit from all MAP sessions and display the CI prompt.

StopLog_
The StopLog_ command is a menu command. The StopLog_ command instructs the log system to begin a log of Capacity MAP information.

Note: The StopLog_ command will stop all capacity logs, not just those started by the user who entered the command.

Menu selection number
17

Type
Operational

Parameters
The StopLog_ command requires command parameters. If the user does not enter any parameters or enters invalid parameters, the MAP terminal displays an error message. The MAP terminal prompts the user to enter a correct parameter value.

All
Stops all logs.

Capacity
Stops CAP100 and CAP101 logs.

Detail
Stops CAP100, CAP101 and CAP103 logs.

SchedMAP
Stops CAP100, CAP101 and CAP102 logs.

Options
There are no command options.

Command format examples
Example use of the StopLog command is shown in Table 9-19. The StopLog command syntax is shown in the example below:

COMMAND <parameter>

Table 9-19 StopLog command examples

Command example	Command description
>StopLog all	Stop all capacity logs currently running.
>StopLog capacity	Stop CAP100, CAP101 and CAP102 logs.
>StopLog detail	Stop CAP103 log.
>Stoplog schedmap	Stop Cap100, CAP101 and CAP102 logs.

StrtLog_
The StrtLog_ command is a menu command. The StrtLog_ command instructs the log system to begin a log of Capacity MAP information.

Note: The CAP103 log uses additional CPU time. The user will receive a warning message when starting this log.

Menu selection number
18

Type
Operational

Parameters
The StrtLog_ command requires command parameters. If the user does not enter any parameters or enters invalid parameters, the MAP terminal displays an error message. The MAP terminal prompts the user to enter a correct parameter value.

All
Starts all logs.

Brief
Starts all logs except CAP103.

Capacity
Starts CAP100 and CAP101 logs.

Detail
Starts CAP100, CAP101 and CAP103 logs.

Duration
An integer value from 16 to 255 that specifies how long the log should be left running. The maximum of 255 is a default value that can be changed in office parameter CAP_MAX_DURATION.

Forever
If this parameter is entered, logs will continue to run until the StopLog command is entered.

SchedMAP
Starts CAP100, CAP101 and CAP102 logs.

Options
There are no command options.

Command format examples
Example use of the StrtLog command is shown in Table 9-20. The StrtLog command syntax is shown in the example below:

COMMAND <parameter>

Table 9-20 StrtLog command examples

Command example	Command description
>StrtLog all 16	Starts all capacity logs currently running for 16 minutes.
>StrtLog brief 16	Starts all logs except CAP103 for 16 minutes.
>StrtLog capacity 16	Starts CAP100, CAP101, and CAP102 logs for 16 minutes.
>StrtLog detail 16	Starts CAP103 log for 16 minutes.
>Strtlog schedmap forever	Starts Cap100, CAP101 and CAP102 logs until the user enters the StopLog command.

Capacity CI level

The CAPCI command provides identical information to the Capacity and SchedMAP MAP levels. Field definitions are identical, and the user may also enter the PARMS command.

The following is an example of CAPCI command syntax.

Figure 9-5 CAPCI commands

```
> help CAPCI
  CAPCI -- Display information on system capacity
   Parms: [<option>   {PARMS,
                       SCHEDMAP,
                       ALL}]

> CAPCI
  CATMP/HR UTIL ENGCATMP MAXCATMP COMPLEX  ENGLEVEL CCOVRLD  PESC
    120000   75   160000   200000     120    BELOW     OFF    NO

> CAPCI ALL
  CATMP/HR UTIL ENGCATMP MAXCATMP COMPLEX  ENGLEVEL CCOVRLD  PESC
    120000   75   160000   200000     120    BELOW     OFF    NO

  SCHED  FORE MAINT    DNC AUXCP    OM GTERM  BKG NETM  SNIP
     85    75    80     66   100    95    50  300    0    20


  Guaranteed_Terminal_CPU_Share = 2%
  AUXCP_CPU_Share               = 1%
  CC_Englevel_Warning_Threshold = 100%
  NETM Share setting            = 0%
  DNC Share setting             = 3%
  SNIP Share setting            = 1%
  1% CPU allocation             = 2142 CATMP/HR
```

Capacity operational measurements

The capacity-monitoring tools introduce OM Group XASTAT. Active operational measurements are updated once every minute.The XASTAT OM group measures central processing unit (CPU) usage and call processing on an XA-Core. Also use OM group XASTAT to provision an XA-Core.

NTP 297-8991-810 contains a complete description of OM Group XASTAT and the associated registers.

Capacity logs

The capacity-monitoring tools introduce four logs for logging capacity information for future analysis by the user. The system sends one line of output to the log buffer every minute while the logs are active. This contains measurements from the previous minute. Logs are provided every 15 minutes, as well as a summary log for the numerical data recorded at the Capacity MAP level over the 15 minute sample period.

NTP 297-8991-810 contains complete descriptions of logs CAP100, CAP101, CAP102 and CAP103.

DMS-100

XA-Core

Maintenance Guide

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