

405-TYPE DATA SYSTEM DESCRIPTION

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1. GENERAL

1.01 This section provides descriptive information for a 405-type data system. Information concerning the data terminal equipment or related services is not included in this section. The 405-type data system is primarily used in central offices.

1.02 This section is reissued to add data set 405-type field conversion information and to update the reference part. Since this is a general revision of the section, change arrows ordinarily used to indicate changes have been omitted.

1.03 A basic 405-type system consists of a data set 405A transmitter and a data set 405B receiver. This arrangement will be used for discussion in this section.

1.04 As shown in Fig. 1, each data set is located in a central office. Data is transmitted and received from the remote data location via an interface which is designed to accommodate the type of data to be transmitted. This system will accommodate 8, 20, or 32 parallel data inputs. Data is transmitted serially by time division multiplexing (TDM) and frequency-shift keying (FSK) at optionally selected maximum rates of 700, 880, 1400, or 1760 bits per second using a private line, voiceband channel. The system provides no voice or telephone signaling capability.

1.05 Table A shows the orderable codes for data sets, D-specification kits, and data units (DUs). The data set concept permits building out the data system to accept maximums of 8, 20, or 32 input/output signals. The D-specification kit contains the data unit, necessary hardware, and instructions for a field conversion of an 8-bit input/output system to a 20- or 32-bit input/output system. The data unit may also be ordered and used as maintenance spares for the list 2 or 3 portion of the 405-type data sets.

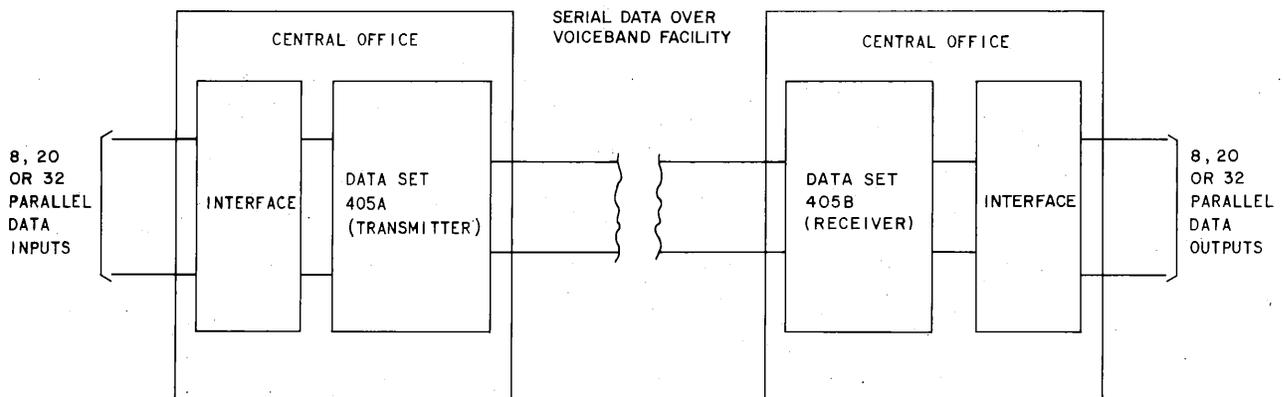


Fig. 1—405-Type Data System

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Note: Transmitter and receiver must be the same list number (8, 20, or 32 input/output signals) and have the same bit rate option installed.

1.06 The purpose of the 405 system is to monitor, transmit, and provide remote indications for the binary state of the data inputs. This is accomplished by transmitter scan or sampling of the data appearing at the data set interface. All the input data states are sampled simultaneously prior to the transmission of each word. The sampling rates for the 405A data sets operating in the continuous-scan mode are shown in Table B.

1.07 Transmission may be either continuous or start-stop as follows:

- Continuous transmission causes data words to be transmitted one after another.
- Start-stop transmission enables the customer to start transmission of a data word at any time by initiating a start command. A new word cannot be started until the transmission of the previous word has been completed.

1.08 Scanning permits the parallel data to be stored as binary information in the transmitter

TABLE A
ORDERABLE CODES

CODES	INPUTS	OUTPUTS	NOTES
DS 405A-L1A	8		1
DS 405A-L1/2	20		2
DS 405A-L1/3	32		3
DS 405B-L1A		8	4
DS 405B-L1/2		20	5
DS 405B-L1/3		32	6
D-180539 KIT	12		7
D-180540 KIT	24		8
D-180541 KIT		12	9
D-180542 KIT		24	10
DU 45A1	12		11
DU 45C1	24		12
DU 45B1		12	13
DU 45D1		24	14

Notes:

1. 8-bit transmitter
2. 405A-L1A and additional 12-bit input buffer and shift register (list 2)
3. 405A-L1A and additional 24-bit input buffer and shift register (list 3)
4. 8-bit receiver
5. 405B-L1A and additional 12-bit shift register with output buffer (list 2)
6. 405B-L1A and additional 24-bit shift register with output buffer (list 3)
7. For expansion from 8- to 20-bit transmitter
8. For expansion from 8- to 32-bit transmitter
9. For expansion from 8- to 20-bit receiver
10. For expansion from 8- to 32-bit receiver
11. The list 2 portion of 405A-L1/2
12. The list 3 portion of 405A-L1/3
13. The list 2 portion of 405B-L1/2
14. The list 3 portion of 405B-L1/3.

TABLE B
SAMPLING RATES
(CONTINUOUS – SCAN OPERATION)

TRANSMITTING BIT RATE (bps)	SAMPLING INTERVAL/INPUT (ms)		
	8 INPUT	20 INPUT	32 INPUT
700	15.714	32.857	50.000
880	12.500	26.136	39.773
1400*	7.857	16.429	25.000
1760†	6.250	13.068	19.886

* Requires C1 line conditioning.

† Requires C2 line conditioning.

shift register. Timing pulses and internal data set logic causes the data to be shifted out one bit at a time to generate a serialized data word. Logic circuits cause each word to be preceded by a 3-bit alternating prefix code which is used by the receiver for sync detection.

1.09 The serialized data word is used to frequency-shift key an oscillator which produces frequency-modulated (fm) voiceband signals corresponding to the binary input. This fm output is factory adjusted and transformer matched at 0 dBm into 600 ohms to meet private line requirements. Transmission is in one direction only to an associated receiver via a private line data channel. Because transmission is in one direction, only one-half of the 4-wire data channel is connected to data set 405-type.

1.10 The 405B receiver functions to demodulate the voiceband serial data word and to regenerate a parallel data output corresponding to the transmitted word.

1.11 Input to the receiver is transformer matched to a filtering circuit which eliminates spurious noise and unwanted frequency components. Receiver demodulator and slicer circuits convert the fm signal into a pulse train. Each pulse has a magnitude of 0 volts or +4.5 volts depending on the frequency of the signal at the input to data set 405B. These pulses are demultiplexed and shifted into a register where they are clocked, as parallel data, into an output buffer. The buffer provides data set isolation and parallel data drive to the user interface.

2. PHYSICAL DESCRIPTION

2.01 Data sets 405A-L1A and 405B-L1A shown in Fig. 2 and 3 are integrated modular units using solid state circuit packs and integrated circuit substrates. The units are mounted in wire frame racks which are adjustable to fit either a 23- or 25-inch-wide central office frame. Location of the various circuit packs are shown in Fig. 2 and 3.

2.02 Central office connections are provided by wire wrap connections that terminate in a panel or interface circuit that may mount above or below the data set. This panel (not furnished as part of the data set) provides power and audible/visual alarm connections which indicate trouble in the data system.

2.03 Interface connections to L1A (P1) units are made with a KS-19087-L2 connector. The L1/2 and L1/3 units require a KS-19088-L2 connector when connecting to the interface. Interconnections between L1/2 or L1/3 and L1A are made with an M15F cord, furnished with the unit.

2.04 Data sets 405A and 405B will operate in a central office environment over an ambient temperature range of 35 to 120°F within a relative humidity of 20 to 80 percent. All circuits are powered from -48 volt central office battery and ground. Actual voltage working limits are between -48 and -54 dc volts. Normal current drains from the -48 volt supply are shown in Table C for data sets and data units.

2.05 The size and weight of the orderable data set codes are shown in Table D. Table E shows the size and weight for the D-specification kits.

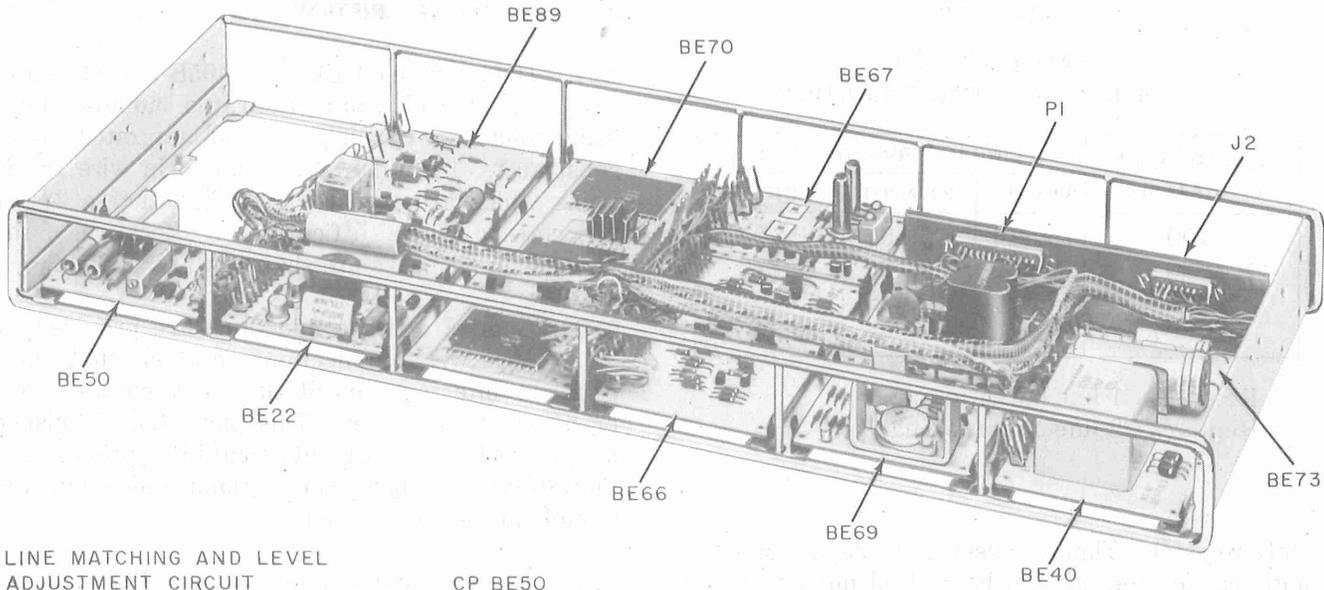
3. FUNCTIONAL DESCRIPTION

3.01 The following text provides a block diagram analysis of data sets 405A- and 405B-type based on circuit pack functions. BE 40, BE 67, and BE 69 circuit packs, which are used in both data sets, will be described under 405A- and 405B-type headings for completeness.

A. Data Set 405A-Type Transmitter

3.02 The data set performs five essential functions:

- Accepts parallel input data



LINE MATCHING AND LEVEL ADJUSTMENT CIRCUIT	CP BE50
8-BIT INPUT BUFFER	CP BE66
CRYSTAL OSCILLATOR	CP BE67
-48V TO +4.5V CONVERTER	CP BE69
8-BIT TRANSMITTER MULTIPLEXER	CP BE70
CONVERTER FILTER	CP BE73
TRANSMITTER ALARM	CP BE89
SERIAL MODULATOR	CP BE22
TRANSFORMER	CP BE40
15-PIN CONNECTOR	J2
25-PIN CONNECTOR	PI

Fig. 2—Data Set 405A-L1A Transmitter

- Generates sync pattern
- Performs parallel-to-serial conversion
- Transmits either continuously or in a start-stop mode
- Provides an alarm indication of any system abnormality.

3.03 Since the essential transmitter functions are similar for 8, 20, or 32 input data bits, an explanation of an 8-input data set will be provided in this section. Figure 4 is a block diagram which is used in explaining the overall function.

8-Bit Input Buffer (BE 66)

3.04 This module contains eight individual transistorized buffer stages which accept a

maximum of eight parallel data signals from the customer-provided interface. The buffer outputs are suitable for application to the data set diode transistor logic (DTL) circuits.

3.05 When more than eight inputs are required, additional input buffers may be employed by ordering data sets or D-specification kits as shown in Table A.

3.06 Each input signal indicates the binary state (on or off condition) of the data to be transmitted. An interface signal of -48 dc volts or an open circuit is buffered to $+4.5$ dc volts. A ground signal on the interface results in a low-impedance, zero volt (ground output) from the buffer. The parallel buffer outputs and the timing signal from the crystal oscillator are applied to the transmitter multiplexer.

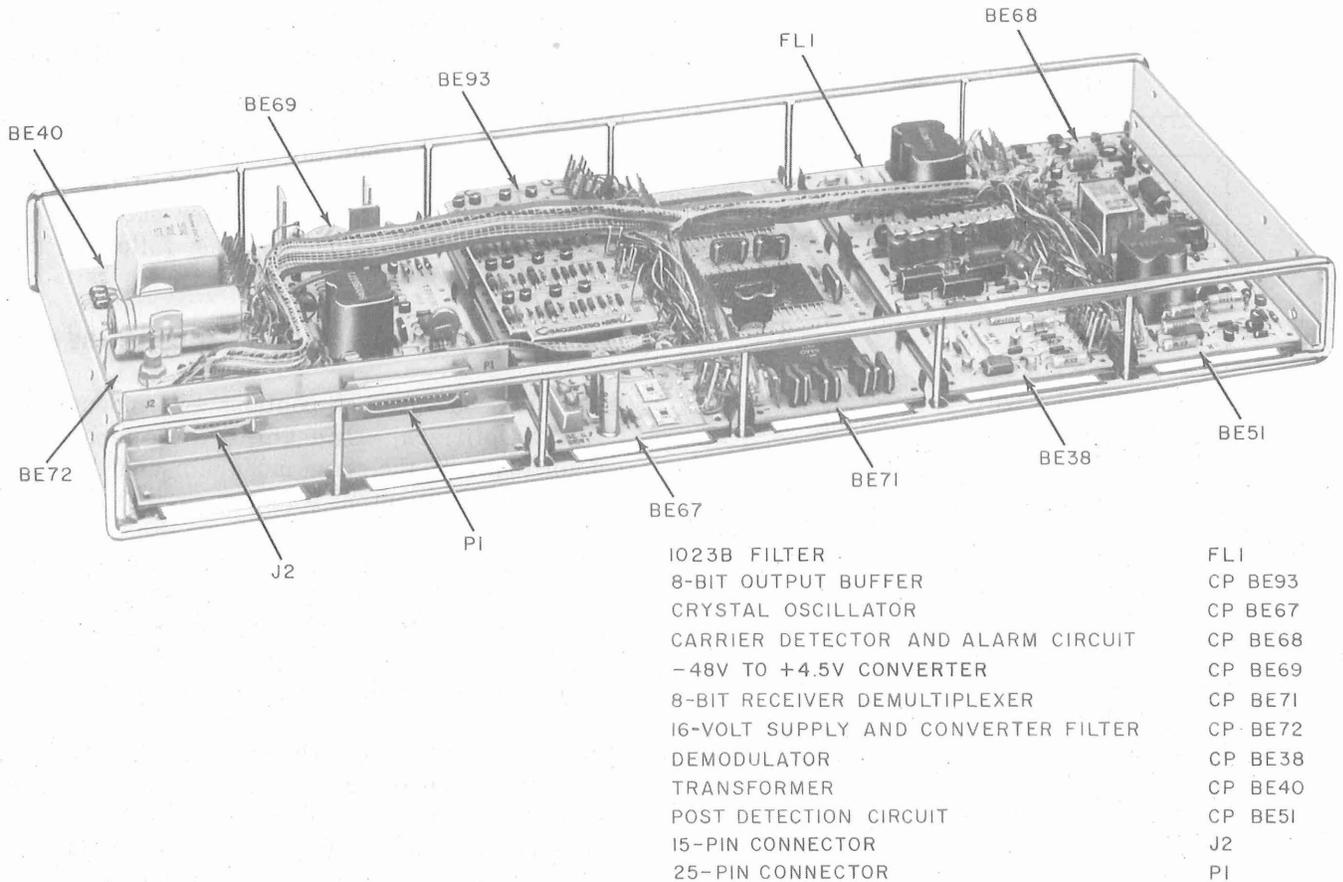


Fig. 3—Data Set 405B-L1A Receiver

Crystal Oscillator (BE 67)

3.07 This module is the data set clock. It generates a stable timing signal which produces synchronization and drive for the data set DTL circuits.

3.08 A crystal-controlled oscillator produces frequencies of either 179.2 kHz (700 or 1400 bps) or 225.28 kHz (880 or 1760 bps) as determined by optional screw switch settings. Oscillator output is amplified, divided, and shaped to a corresponding square wave of 44.8 kHz, 56.32 kHz, 89.6 kHz, or 112.64 kHz. This is the clock signal which is applied to a countdown circuit in the transmitter multiplexer to be divided further for establishing the serial data rate.

8-Bit Transmitter Multiplexer (BE 70)

3.09 This module consists of three interconnected hybrid integrated circuits (HICs) which

perform the major data set logic functions. The HIC designated CM1 is a 4/8 bit serializer, CM2 is the countdown circuit, and CM3 is the transmitter serializer.

3.10 Parallel data inputs from the input buffer are applied to CM1 and are stored in a shift register which is set to indicate the state of each input. The clock signal from the crystal oscillator is applied to CM2 which divides the frequency by a factor of 64. This division results in a square wave output signal which determines the speed at which the data will be transmitted. The output of CM2 causes CM1 to shift out a data bit, for each input state, on every positive transition of the clock signal. The serialized data from CM1 is applied to CM3 which performs the logic functions to produce a data word containing all information necessary for a valid transmission.

3.11 Integrated circuit CM3 produces an alternating three-pulse prefix (101 or 010) which is

TABLE C
CURRENT DRAINS

DATA SET	mA
405A-L1A	140
405A-L1/2 or 405A-L1A with 45A1 DU	180
405A-L1/3 or 405A-L1A with 45C1 DU	220
405B-L1A	210*
405B-L1/2 or 405B-L1A with 45B1 DU	310*
405B-L1/3 or 405B-L1A with 45D1 DU	410*

* Does not include current into circuits connected to the receiver outputs

introduced at the start of each word. This code provides a sync detection pattern for the data system receiver. CM3 may be optionally conditioned to cause the data set to operate in the continuous-scan or the start-stop mode (in which transmission of each data word is under the control of the user). When operating start-stop, the user may give the start command (G-1) at any time following the end-of-word (EOW) indication.

Line Matching and Level Adjustment Circuit (BE 50)

3.12 This circuit pack contains two independent amplifiers. One amplifier operates in conjunction with the serial modulator and the other with the data set output transformer.

3.13 A level shifting amplifier receives the output from CM3 and converts a +4.5 volt and ground signal into a corresponding bi-polar signal of -8 or +4.5 volts, respectively. This signal ensures positive keying of the serial modulator.

3.14 The output from the serial modulator is an fm signal (explained in 3.16) and is applied to the other amplifier which functions as a linear amplifier. The output of this amplifier is adjustable over a 30-dB range and is matched to the input impedance of the data set output transformer.

TABLE D
DATA SET
PHYSICAL CHARACTERISTICS

DATA SET	HEIGHT (INCHES)	WIDTH (INCHES)	DEPTH (INCHES)	WEIGHT (POUNDS)
405A-L1A	1.92	23/25	8.15	6-1/2
405A-L1/2	3.92	23/25	8.15	10-3/4
405A-L1/3	3.92	23/25	8.15	11-1/2
405B-L1A	1.92	23/25	8.15	6-3/4
405B-L1/2	3.92	23/25	8.15	11
405B-L1/3	3.92	23/25	8.15	11-3/4

TABLE E
D-SPECIFICATION KIT
PHYSICAL CHARACTERISTICS

KIT	HEIGHT (INCHES)	WIDTH (INCHES)	DEPTH (INCHES)	WEIGHT (POUNDS)
D-180539	3.9	23/25	8.15	5-1/2
D-180540	3.9	23/25	8.15	6-1/3
D-180541	3.9	23/25	8.15	5-1/2
D-180542	3.9	23/25	8.15	6-1/3

Serial Modulator (BE 22)

3.15 This module consists of an oscillator which is keyed between two frequencies depending upon the binary state of the input data.

3.16 The signal from the line matching and level adjustment circuit is a pulse train in which a +4.5 volt amplitude signal indicates a mark (caused by -48V or an open circuit connected to the corresponding data input at P1) and a -8 volt signal represents a space (caused by a ground being connected to the corresponding data input at P1). As the signal is applied to the modulator, the amplitude differences cause the oscillator to be alternately keyed to generate either 2100 Hz (mark) or 1300 Hz (space). The resulting output is the voiceband fm data word.

Transformer (BE 40)

3.17 This module is comprised of a transformer-varistor network which couples the data set output signal to the transmission facility. In addition to providing the proper 600-ohm impedance, the circuit provides isolation and protection to the data set from foreign potentials.

-48 to +4.5 Volt Converter (BE 69)

3.18 The converter furnishes the +4.5 and -48 dc volt potentials required to power the data set. Central office battery and ground are used as a reliable source of input power for the converter.

3.19 The +4.5 volt output is regulated to ± 0.03 volts to ensure reliable operation of the

DTL circuits. Protection from overvoltage conditions is provided by a circuit which de-energizes the converter if the output exceeds +6.0 volts.

3.20 The -48 dc volt output is a quiet voltage derived by filtering the central office battery voltage. It is used to supply power for sensitive data set circuits requiring -48 volt power.

Converter Filter (BE 73)

3.21 This unit consists of two capacitors which provide filtering of the +4.5 and -48 dc volt converter outputs.

Transmitter Alarm (BE 89)

3.22 This module monitors three vital data set functions carrier, EOW signal (in the continuous scan mode only), and power supply voltage as an indication of normal operation. Loss of any one of these functions produces audible and visual alarms in the central office.

3.23 The serial modulator output signal is sampled for an indication of acceptable carrier. When the amplitude falls below an acceptable value, an alarm condition is activated.

3.24 When the data set is operating in the continuous scan mode, an improper EOW signal (+4.5 volts for about 7 msec) from the transmitter multiplexer is used as an indication of data set trouble.

3.25 The loss of voltage (-48 or +4.5) or out-of-tolerance +4.5 volt level immediately

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disables the data set and causes an alarm to be indicated.

3.26 A timing circuit provides a one-second delay interval which guards against activating an alarm caused by momentary troubles. When a trouble has been corrected, the timing circuit provides an additional two seconds before turning the alarm off. A fault lead is provided for customer and telephone company use which may be used to drive a traffic register for evaluating system performance.

B. Data Set 405B-Type Receiver

3.27 The data set performs five essential functions:

- Demodulates the line signal
- Establishes bit and word synchronization
- Performs serial-to-parallel conversion
- Presents a parallel data output to the interface
- Provides an alarm indication of any system abnormality.

3.28 Since the essential receiver functions are similar for 8-, 20-, or 32-output bit data sets, an explanation of the 8-output data set is provided in this section. Figure 5 is a block diagram which is used in explaining the overall function.

3.29 The incoming data signal, which is demodulated by the receiver, is produced by an associated data set 405A-type transmitter. The signal is a time division multiplexed (TDM) data word which is frequency modulated between 2100 Hz (mark) and 1300 Hz (space). A prefix code (alternately 101 and 010) is transmitted at the start of each word to provide the receiver with a sync detection pattern. Data transmission mode may be either continuous scan or start-stop, depending upon customer requirements.

Transformer (BE 40)

3.30 This module consists of a transformer, varistor network which couples the line signal from the transmission facility to the data set. In addition to providing coupling and impedance

matching, the module furnishes protection to the data set from foreign potentials.

Filter (FL1)

3.31 The signal from the transformer is applied to this unit which functions as a bandpass filter. The circuit is tuned to pass the fm signal transmitted from data set 405A. Spurious noise and oscillations outside this bandwidth are rejected, resulting in a clean input signal to the demodulator.

Demodulator (BE 38)

3.32 Demodulation of the frequency-modulated signal and an Electronic Industries Association (EIA) driver circuit are furnished by this module.

3.33 The demodulation produces a pulse of fixed amplitude and width for every zero crossing in the input signal. The demodulated signal appears as a series of pulses in which pulses derived from 2100 Hz indicate a mark, and the pulses derived from 1300 Hz indicate a space. This signal is amplified and applied to the post detection circuit.

3.34 After being shaped by the post detection circuit, the signal is reapplied to an amplifier circuit in this module, which provides an EIA input to the data set logic driver located on the carrier detector and the alarm circuit module.

Post Detection Circuit (BE 51)

3.35 The circuit consists of a low-pass filter and trigger-type slicer used to shape the demodulated signal. A carrier loss indication is also derived from the unit and applied to the carrier detector and alarm circuit.

3.36 The series of pulses from the demodulator circuit is fed to a low-pass filter. The output of the filter is a dc level that is proportional to the frequency of the received data signal. This signal is coupled to a slicer which squares up the signal for application to the EIA drives in the demodulator module.

3.37 A signal for providing loss-of-carrier indication is produced if the incoming signal level drops below -48 dBm (demodulator output becomes zero).

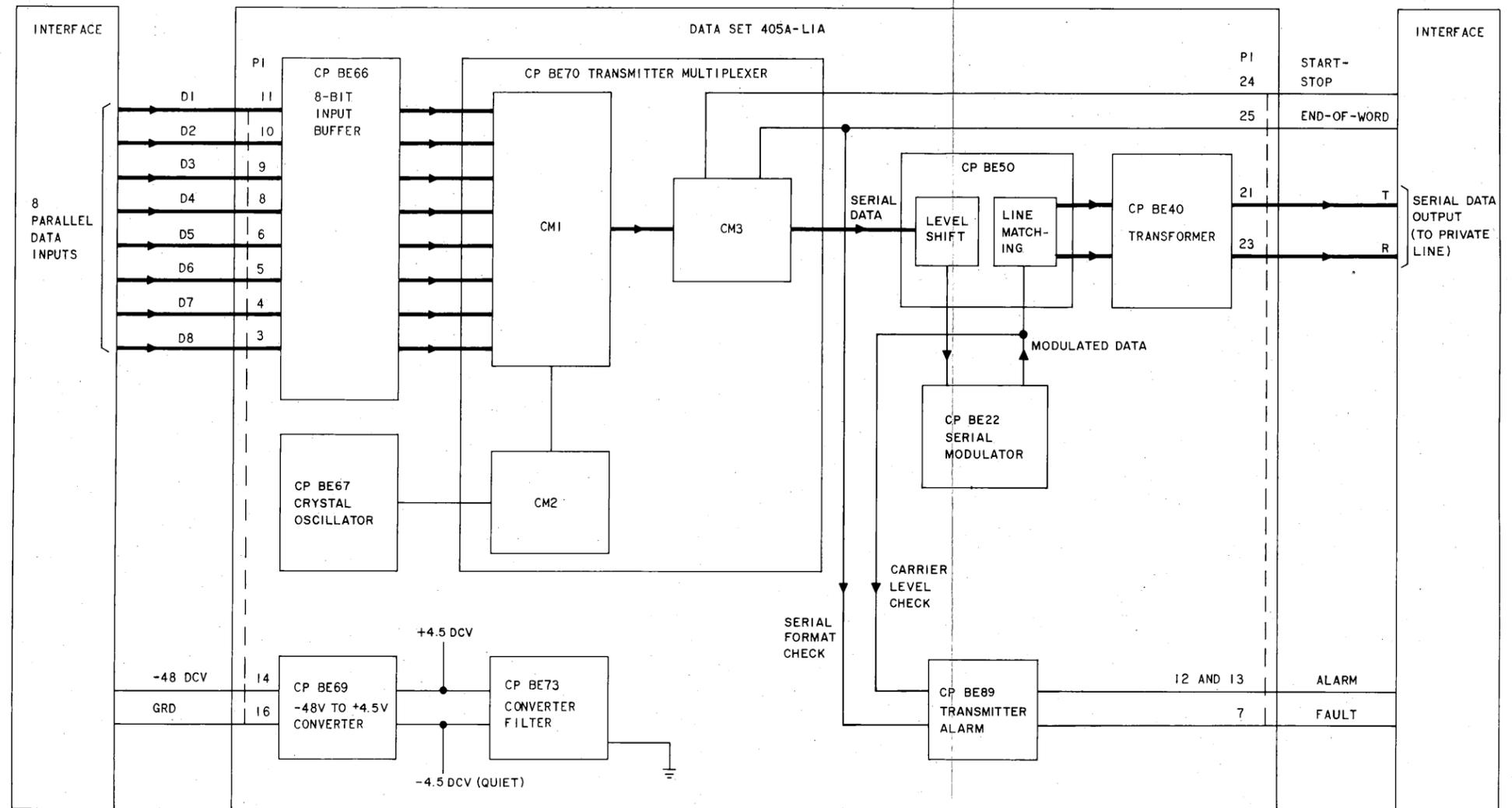


Fig. 4—Data Set 405A-L1A Block Diagram

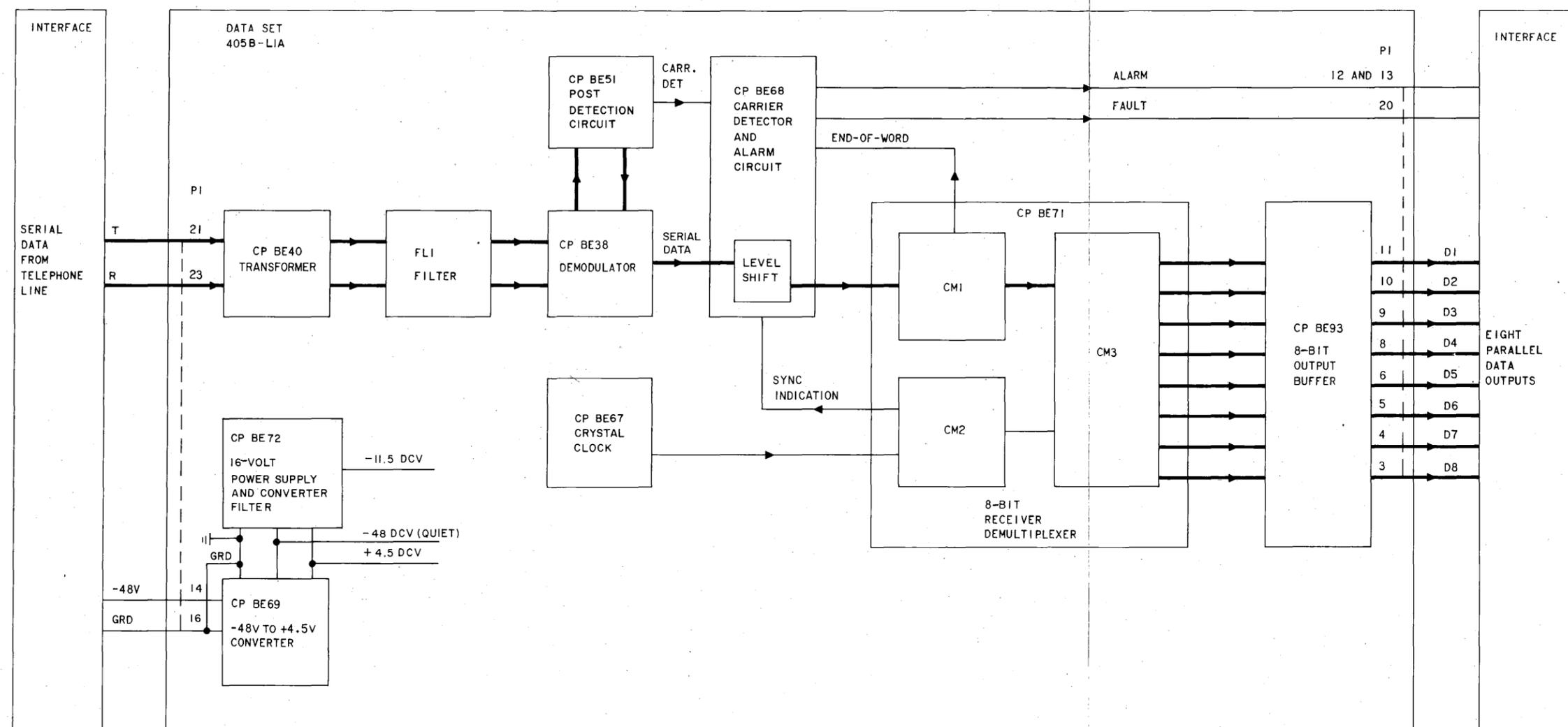


Fig. 5—Data Set 405B-L1A Block Diagram

Carrier Detector and Alarm Circuit (BE 68)

3.38 This module monitors four vital data set functions as an indication of normal operation. Loss of any one of these functions for approximately one second causes an audible and visual alarm at the central office. A buffer amplifier is also incorporated in this module to provide drive for the receiver demultiplexer.

3.39 Voltage levels which correspond to acceptable carrier requirements are derived and applied to this circuit from the post detection circuit and the demodulator. When carrier is lost, an alarm condition is activated.

3.40 When the data set is operating in the continuous scan mode, an optional signal indicating improper end-of-word is available from the receiver demultiplexer, and is used as an indication of data set trouble. The receiver demultiplexer also furnishes a voltage which changes level in the event that synchronization is lost, causing an alarm to be activated. The voltage continues to indicate loss of sync until three consecutive words are in sync. Loss of voltage ($-48V$) or an out-of-tolerance voltage ($+4.5V$) disables the data set, causing an alarm to be activated.

3.41 Timing circuits provide a 1-second interval which guards against transmitting alarms caused by momentary troubles. When an alarm condition has been corrected, the timing circuit provides an additional two seconds before turning the alarm off. A fault lead is provided for customer or telephone company use which may be used to activate a traffic register for evaluating system performance.

3.42 The serial data word from the demodulator is applied to a buffer amplifier in this module. The amplifier performs a level shifting function which changes the EIA input from the demodulator into corresponding $+4.5$ volt and ground signals suitable for application to HICs in the receiver demultiplexer.

Receiver Demultiplexer (BE 71)

3.43 This circuit pack consists of three interconnected HICs which perform the function of establishing word and bit synchronization, serial-to-parallel conversion, and buffer storage. The HIC designated

CM1 is a sync detector, CM2 is a countdown circuit, and CM3 is a 4/8 bit output register.

3.44 The serial data word from the buffer amplifier is applied to CM1, which searches for the proper prefix code (101 or 010). When a valid prefix is recognized, a sync pulse is generated, sync is established, and the information (data) portion of the word is passed to CM3. In the event sync is lost, a sync pulse counter on CM2 prohibits passing any new data to the storage buffers until synchronization of three consecutive data words has occurred.

3.45 Serial data from CM1 is applied to a shift register in CM3. If synchronization and correct end-of-word are established, the clock input causes the register to shift the data to the storage buffers. When the mark- or space-hold option has been incorporated, an alarm condition causes all the data outputs to change to 1s (space hold) or 0s (mark hold). Space hold causes all relays or message register connected to the data outputs at P1 to be operated during an alarm condition. Mark hold causes the message registers to be released.

3.46 When more than eight parallel data outputs are required, additional shift registers and buffer storage stages may be added by installing data sets or D-specification kits as shown in Table A.

Crystal Oscillator (BE 67)

3.47 This module is the data set clock. It generates a stable timing signal which provides synchronization and drive for data set internal logic.

3.48 A crystal-controlled oscillator produces frequencies of either 179.2 or 225.28 kHz as determined by optional screw switch settings. The oscillator output is amplified, divided, and shaped to a square wave of 44.8, 56.32, 89.6, or 112.64 kHz. This signal is applied to the countdown circuit in the receiver demultiplexer to be divided further into a signal used for driving the shift register circuits.

8-Bit Output Buffer (BE 93)

3.49 This module consists of eight identical buffer stages, each capable of providing a data signal to the interface. Parallel data input levels

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from the storage buffers on BE 71 are either at +4.5 volts dc or ground.

3.50 Each output is capable of driving a relay circuit having a coil connected to a negative potential of -48 volts dc nominal.



The connected output circuit should not be allowed to draw more than 90 mA. No internal dc current limiting is provided. Consequently, at least 600 Ω must be provided between each data output and the -48 volt supply. The output circuits do, however, contain protection against inductive surges so that no external contact protection is required.

3.51 A maximum of 32 parallel data outputs is available by installing data sets or D-specification kits as shown in Table A.

-48 to +4.5 Volt Converter (BE 69)

3.52 The converter furnishes the +4.5 and -48 dc volt potentials used to power the data set. Central office battery and ground are used as a source of input power for the converter.

3.53 The +4.5 dc volt output is regulated to ± 0.03 volts to ensure reliable operation of the logic circuits. Protection from overvoltage conditions is provided by a circuit which de-energizes the converter if the output exceeds +6.0 volts.

3.54 The -48 dc volt output is a quiet voltage derived by filtering the central office battery voltage. It is used to supply power for sensitive data set circuits requiring -48 volt power.

16-Volt Power Supply and Converter Filter (BE 72)

3.55 This module furnishes the capacitors needed to filter the -48 and +4.5 dc volt output of the converter. A zener diode circuit is included to produce a -11.5 dc volt supply required by the demodulator and the post detection circuit.

4. REFERENCES

4.01 For additional information relating to the 405-type data system, refer to the following documents:

- CD- & SD-1D203-01 Data Set 405A-Type
- CD- & SD-1D204-01 Data Set 405B-Type
- CD- & SD-1C451-01 Interface Circuit for 405-Type Data Sets

SECTION	TITLE
252-140-101	Interface Circuit for Use Between 405-Type Data Sets and Message Registers in Remote Registers Operation (SD-1C451-01), Description
252-140-501	Interface Circuit for Use Between 405-Type Data Sets and Message Registers in Remote Register Operation (SD-1C451-01), Verification Procedure
312-809-150	405-Type Data System — Supplementary Information
312-809-180	405-Type Data System — Summarizing Specification
312-809-200	405-Type Data System — Installation and Connections
312-809-300	405-Type Data System—Maintenance
312-809-500	405-Type Data System—Test Procedures
594-029-100	405-Type Data System—Identification.