DATA SET 201D-TYPE

DESCRIPTION

CONTENTS PAGE

1. GENERAL

1.01 This section contains the physical and functional descriptions, test features, and the maintenance policy for data set (DS) 201D-L1A. The DS is used for transmission of data at 2400 bits per second (bps) in various Bell System applications and normally operates under control of a separate stored program processor. The processor monitors system performance and detects and isolates faulty units in the system. Information pertaining to the stored program processor (also referred to as an automatic terminal controller) is not included in this section.

1.02 This section has been reissued to incorporate changes required by the addition of a second option switch to the DS 201D. Change arrows have been used to indicate revised paragraphs.

1.03 DS 201D (Fig. 1) uses a 4-level phase shift keying (PSK) modulation scheme to transmit and receive serial binary data synchronously at the rate of 2400 bps over a 3002-type, 4-wire private line (PL) channel with or without C2 conditioning.

1.04 DS 201D is intended for internal Bell System use in an environment of a central office (CO) in such systems as the Traffic Service Position System (TSPS) and the Common Channel Interoffice Signaling (CCIS) system. CCIS is similar to the International CCITT No. 6 signaling system.

1.05 The significant features of DS 201D are its high reliability, operation controlled by a stored program processor, and CO compatibility. DS 201D is designed to be powered from a 24-volt, CO battery, and meets the environmental requirements for CO equipment in terms of ambient temperature, ambient humidity, shock, and vibration.

1.06 A typical DS 201D configuration requires two 4-wire, 3002-type lines or equivalent voice frequency lines. The primary line, line B, is connected to the remote DS, but connections for line A may vary depending on DS system configuration. Figures 2 and 3 show the basic configurations for CCIS and TSPS. In TSPS, line A and line B are connected to the remote DS where a spare line (A) is shared between two data sets.

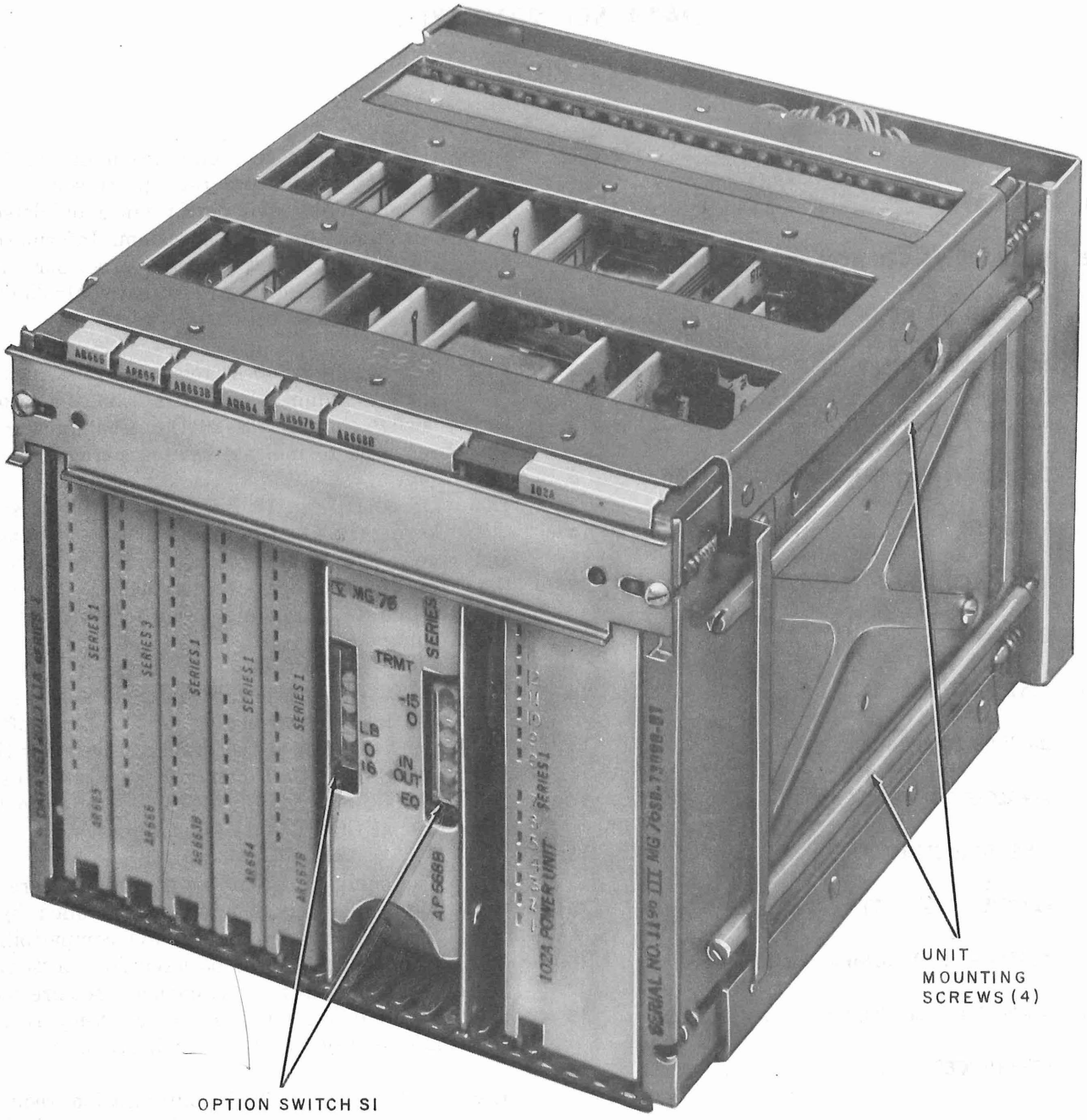


Fig. 1—DS 201D-L1A (Front View)

In CCIS, the DS is connected to two voice-frequency links (VFL) either through a VFL access circuit or the switching network depending upon the type of office. In some cases, only one VFL (normally VFLB) will be provided between the offices.

1.07 The DS (under automatic terminal control) can operate in eight functional states. Each state is determined by the control signals LC, DL, AL, LT, and FT. Five most significant states are listed below:

- Normal operation (transmit and receive on line B)
- Transmit and receive on line A (line transfer)

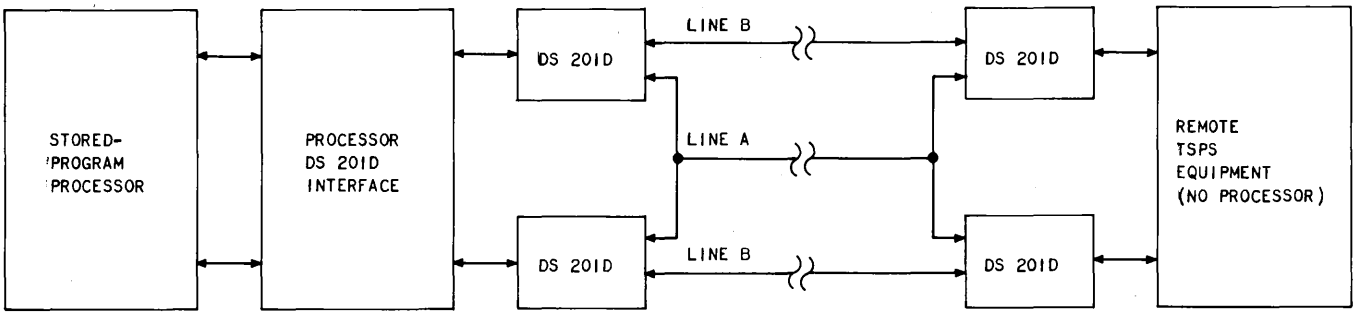


Fig. 2—Basic TSPS Configuration Using DS 201D

- Line A or B disconnected for facility test while other line remains in use.
- Digital loop
- Analog loop.

2. PHYSICAL DESCRIPTION

2.01 DS 201D consists of six AR-type circuit packs (CPs), a 102A power unit, a 58B apparatus mounting, and a mounting bracket. The DS weighs approximately 13 pounds and the dimensions are given in Fig. 4. The required 24V dc power is approximately 18 watts (0.75 ampere). DS 201D will operate in an ambient temperature range of 0° to 58°C with an ambient relative humidity of 20 to 95 percent.

2.02 A male 50-pin interface connector (KS-16671-L1) is located at the rear of the DS and provides all connections including the power leads, two 4-wire PLs, and the leads to the controller.

2.03 Plug KS-16671-L1 mates with the recommended connectors KS-16786-L51 and KS-16672-L17 for use in TSPS and CCIS applications, respectively. Other equivalent connectors may be used as determined in KS specification of the plug.

2.04 The four mounting screws provide easy removal and replacement of the DS from the frame during trouble location and correction.

3. FUNCTIONAL DESCRIPTION

3.01 This part will describe the functional circuitry and interface leads of DS 201D. The DS is divided into four sections to simplify understanding and description (Fig. 5). The four sections are 102A power unit, transmitter, common and interface circuitry, and receiver. Each functional block has an AR number listed vertically on the right side. This number indicates that the majority of the functional circuitry is on the specified CP. The exceptions to this notation are the 102A power unit, which is an entire CP, and the common and interface circuitry, where all components without the AR number are physically located on the interface AR668B CP (which contains two printed wiring boards).

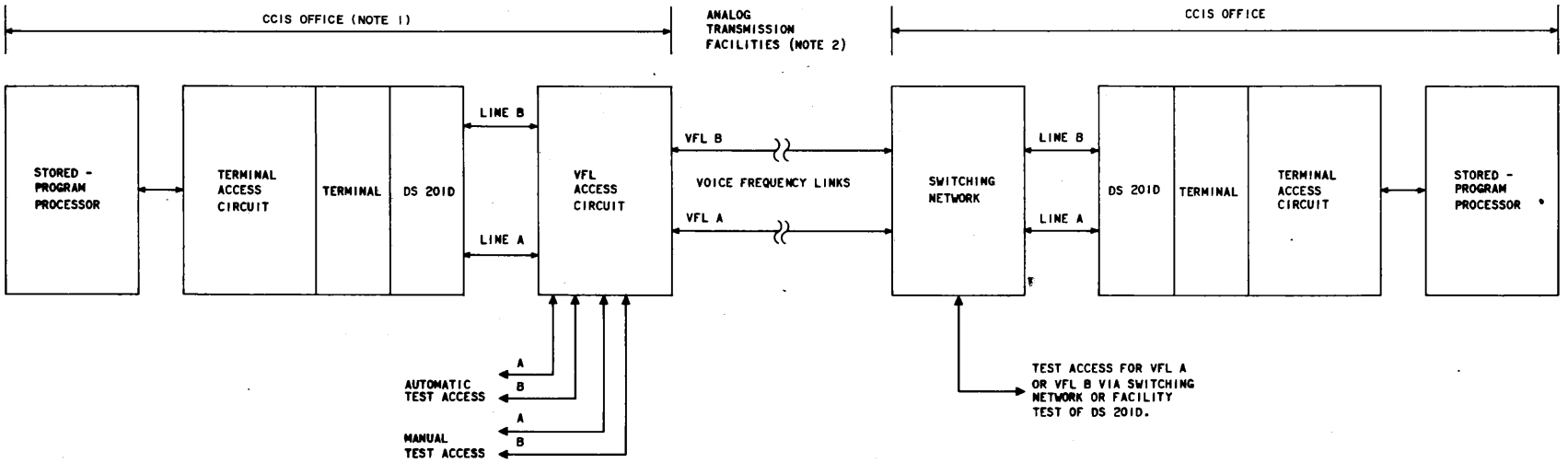
102A POWER UNIT

3.02 The 102A power unit provides dc-to-dc conversion. Input values of 24V dc are converted to output values of +5, +12, and -12V dc. Table A lists the voltage values that appear at specified pins on the CPs and on connector P7.

TRANSMITTER

3.03 The transmitter accepts serial binary data from the customer interface and encodes that data for transmission over a voiceband frequency telephone channel.

3.04 The customer sends serial data over the send data (SD) lead to the serial-to-parallel converter. The SD signal is synchronized by the phase-locking circuits with a 2400-Hz clock signal. The clock signal is provided by either the DS internally or by the customer terminal equipment on lead SCTE (serial clock transmit, externally). Serial clock transmit (SCT) is sent to the customer for timing purposes.



NOTES:
(1) IN SOME SYSTEMS BOTH OFFICES WILL BE OF THIS TYPE
(2) IN SOME SYSTEMS ONLY ONE VFL (NORMALLY B) WILL BE PROVIDED BETWEEN OFFICES

Fig. 3—Basic CCIS Configuration Using DS 201D

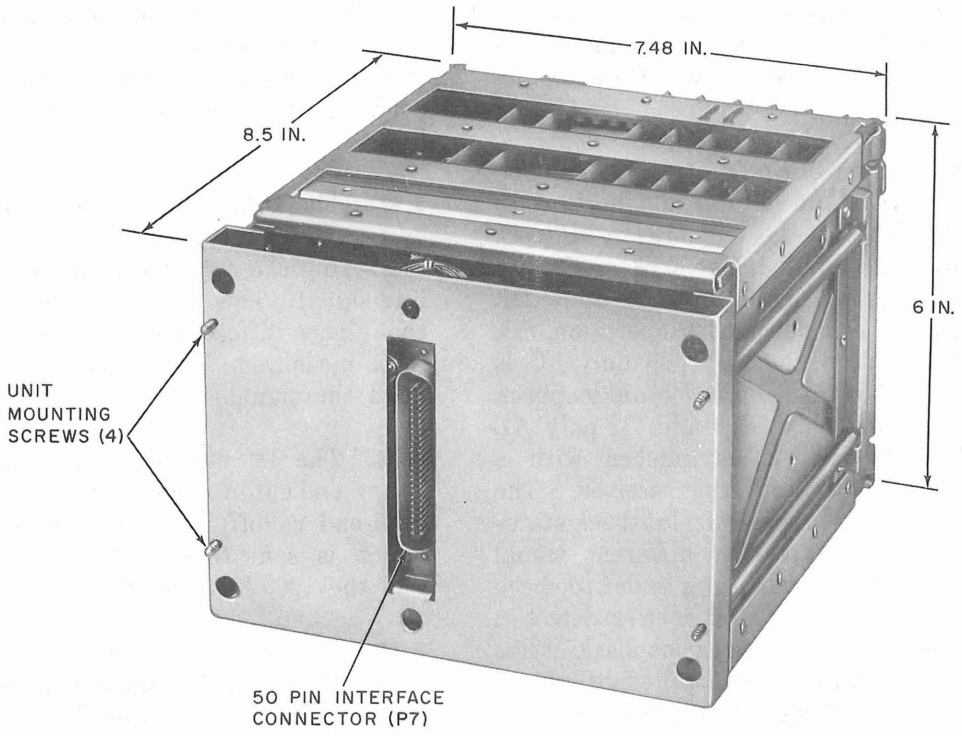


Fig. 4—DS 201D-L1A (Rear View)

3.05 The data is grouped into pairs of adjacent bits (dibits) by the serial-to-parallel converter. Each dibit or symbol occurs at the rate of 1200 symbols per second.

3.06 The symbols are sent to phase and envelope modulators which encode the data as discrete phase changes of the 1800-Hz carrier. Four phase changes are possible since each symbol represents two bits of data (refer to Table B).

3.07 The outputs of the phase and envelope modulators are sent to a digital-to-analog converter where the signal is converted to a discrete level analog signal. This signal contains high-frequency components which are removed by the low-pass filter, resulting in a line signal spectrum from 600 to 3000 Hz. The line signal is optioned to either pass through the compromise equalizer or to bypass it. The line signal is again optioned to provide a power level of 0 dBm or -15 dBm, depending on system application. Then the signal is amplified and sent to the transmit line B, leads BT1 and BR1.

3.08 The countdown and phase-lock circuits provide synchronization for the transmitter from the common countdown. Thus, synchronization allows the customer to transmit data using his own 2400-Hz clock signal which the customer may provide to the DS on SCTE.

COMMON AND INTERFACE CIRCUITRY

3.09 This part describes the line interface and circuitry that is common to the transmitter and receiver. Most of the functional components are physically located on the interface AR668B CP.

3.10 The line interface is between the data set and line A and line B, which are two separate 4-wire PLs. The transmitter output and receiver input are connected to line B or line A under control of lead LT (line transfer). Line B is utilized when a low level on LT exists. Line A is utilized when LT is high. Normally, line B is utilized.

3.11 ▶With LT low, a low level on FT (facility test) causes line B to be connected to the DS and line A is terminated into 600 ohms. With LT low and FT high, line B is connected to the

DS and line A is looped back through the amplifier. With LT high and FT high, line A is connected to the DS and line B is looped back through the amplifier.◀

3.12 The combinations of line control (LC), analog loopback (AL), and digital loopback (DL) provide eight possible states, as indicated in Table C. These input controls establish loopback conditions for the analog or digital signals by RAL and RDL relays, respectively. For normal DS operation, LC, DL, and AL must all be low. When only LC is high, the transmitter is turned off. Digital loopback is achieved by making only DL high. If only AL is high, analog loopback is established with a nominal -15 dBm signal into the receiver. The remaining four states are the analog loopback states (total of five analog states) at different signal levels which permit the terminal controller to check the operation of the receiver and carrier detector. Switching between the five analog loopback states is accomplished by a transistor-controlled attenuator with a response time of less than one millisecond and, thus, is fast enough to test carrier off reliable (COR) response time, synchronization time, and holdover time.

3.13 The DSR logic produces a high on lead DSR (data set ready) when DL, AL, LC, LT, FT, and IE are all low.

3.14 The 460.8 kHz and 1.0368 MHz are square wave (clock) signals which are derived by common countdown from the 8.2944-MHz crystal oscillator. These clock signals are for use in the TSPS terminal equipment.

RECEIVER

3.15 The purpose of the receiver is to reconstruct customer digital data from the phase-modulated line signal and to provide the customer with a timing signal SCR (serial clock receive). SCR notifies the customer when each bit is to be sampled at the receiver output on lead RD (received data). The receiver also gives the customer an indication on the COV lead (carrier on voltmeter) whenever carrier energy is present at the receiver input.

3.16 The received line signal enters the receiver normally from line B of the telephone interface. The signal is amplified by 15.4 dB during normal receiver operations, then sent to the shaping filter and the guard band filter (refer to 3.23). The shaping filter removes out-of-band energy, thus eliminating some noise which may exist at the receiver input. This allows the DS to perform better in the presence of noise on the line.

3.17 The balanced modulator shifts the received data up to the IF frequency band, thus increasing the occurrences of zero crossings of the line signal. This allows the time delays, and thus the phase differences, between adjacent symbols to be measured. This reconstructs the digital data from the signal.

3.18 The IF bandpass filter has a sharp low-end cutoff below 14.4 kHz and a more gradual high-end rolloff. This selects the upper sideband which is sent to the IF slicer, carrier detector, and the 1200-Hz tank filter.

3.19 The IF slicer converts the signal to TTL (transistor-transistor logic) levels for processing by the digital demodulator. The demodulator detects the positive and negative transitions at the zero crossings to determine the differential phase changes between two symbols. The output of the demodulator is a coded dibit symbol which is sent to a parallel-to-serial converter. After conversion, the received data is sent on lead RD to the customer interface. However, received data is inhibited in the interface unless line signal carrier is detected (carrier on delayed [COD] is high).

3.20 The carrier detector circuitry also receives the IF bandpass filter output. The detector generates signals COV and COD. A high level on COV indicates that energy at tip and ring on the line interface is above -26 dBm in the 600- to 3000-Hz band. A low level indicates that energy is below -30 dBm. COD will make low-to-high transitions coincidental with COV but will be delayed with respect to that of COV by slightly more than one second for high-to-low transitions.

3.21 The output of the IF bandpass filter also enters the 1200-Hz tank filter which produces a 1200-Hz signal that is sent to a slicer and results in a square wave. The square wave from the timing recovery is sent to the add-delete circuitry where the phase-locking method generates stable dibit and serial bit clock pulses for the receiver circuitry.

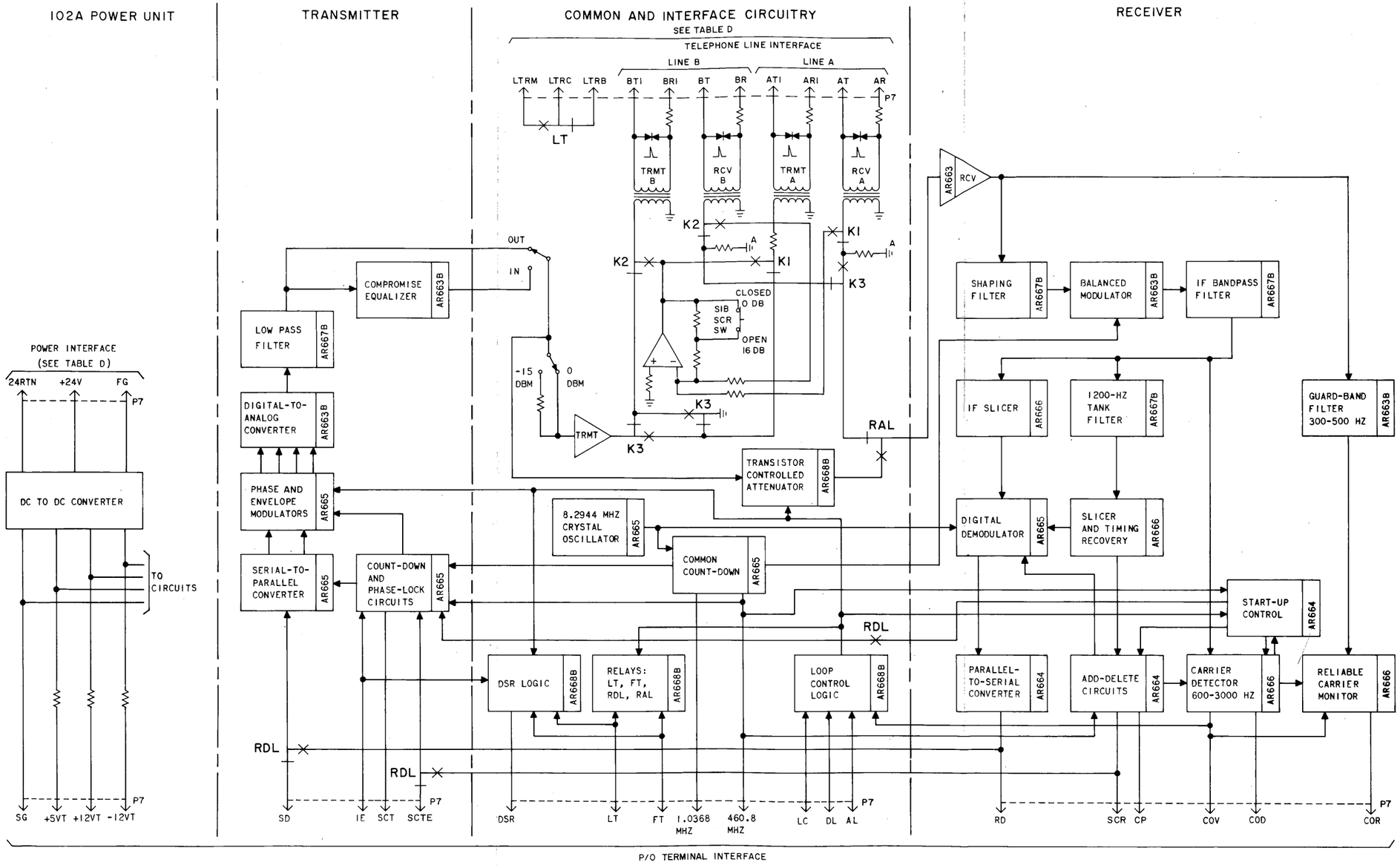


Fig. 5—Simplified Functional Schematic of DS 201D

TABLE A

VOLTAGE REQUIREMENTS AT PIN TERMINALS

CP	VOLTAGES				
	+12V*	—12V*	+5V*	—6V*	+24V†
AR663B	2	20	21	13	—
AR664	—	—	21	—	—
AR665	—	—	21	—	—
AR666	2	20	21	13	—
AR667B	2	20	—	—	—
AR668B	2	20	21	—	—
102A	10,11	13,14	1,2,3	—	19,20
Connector-P7	13	9	11	—	5,7

*Relative to signal ground

† Relative to 24 RTN.

TABLE B

SYMBOLS ENCODED AS CARRIER PHASE CHANGES

SYMBOL ON SD LEAD		PHASE CHANGES OF CARRIER RELATIVE TO PREVIOUS DIGIT INTERVAL
BIT 1	BIT 2	
0	0	+ 45°
0	1	+135°
1	0	— 45°
1	1	—135°

Note: PSK modulation using positive logic where high level equals 1 and a low level equals 0.

3.22 The purpose of the start-up control circuitry is to generate an initializing pulse and, when in a digital loop, a different pulse called GIP. The GIP pulse aligns the programmable countdown chain for the transmitter. The start-up circuitry also controls the one-second holdover circuits and when carrier is lost, resets the add and delete circuitry. If carrier is present, the one-second holdover counter is disabled.

3.23 The guard-band filter rejects frequencies in the received line signal which are not in the frequency band of 300 to 500 Hz. The filter output is sent to the reliable carrier monitor where it is used in conjunction with the energy in the data band (600 to 3000 Hz) to distinguish a valid data signal from noise. This signal is presented on the COR lead and is the logical NAND of COV and the output of a guard-band filter.

INTERFACE LEADS

3.24 This part introduces the terminal interface leads which appear at the interface connector P7. Since some of the following leads are not used and others are self explanatory, all leads in Table D will not be described.

TABLE C

CONTROL INPUTS DETERMINE STATE OF DS

CONTROL INPUTS*			STATE OF DS
LC	DL	AL	
0	0	0	1 Normal on-line
1	0	0	2 Line signal power off (on-line)
0	1	0	3 DL (DS regenerator)
0	0	1	4 AL —15 dBm nominal receive level
0	1	1	5 AL —26 dBm low receive level
1	1	0	6 AL —5.5 dBm high receive level
1	1	1	7 AL —30 dBm receive level COR test
1	0	1	8 AL line signal power off, less than —40 dBm receive level

*1 = high level, 0 = low level
LC = Line Control
DL = Digital Loopback
AL = Analog Loopback

CLOCK 460.8 kHz and 1.0368 MHz — These are square wave outputs provided by the data set for use in the TSPS terminal equipment. They are both derived by fixed countdown from the same 8.2944-MHz crystal oscillator and are accurate to ±.005 percent.

SCT — Serial Clock, Transmitter. A 2400-Hz square wave output is normally derived by fixed countdown from the crystal oscillator. The terminal provides every bit of data on SD at the positive transition of SCT and the DS will sample SD at the negative transition of SCT. When external timing is used, SCT is phase-locked to SCTE. In the digital loopback mode, SCT is phase-locked to SCR.

SD — Send Data. A 2400-bps serial stream of binary data to be presented to the DS synchronously under control of SCT (or SCTE when IE is high). Information on SD is ignored in the digital loopback state.

SCR — Serial Clock, Receiver. A 2400-Hz square wave output is normally phase-locked to the clock of the remote transmitter. The terminal uses SCR to determine when to sample received data (RD). The DS will provide each bit of received data on the positive transition of SCR; the terminal should sample RD on the negative transition of SCR. In the analog loopback states, SCR is phase-locked to the local SCT through the same circuits used normally. When carrier failure is indicated by the low state of COV, SCR is derived by fixed countdown from the crystal.

RD — Received Data. A 2400-bps serial stream of binary data is presented by the DS to the terminal in synchronism with SCR. When

TABLE D

INTERFACE CONNECTOR — (P7)

TERMINAL*	DESIGNATION	TERMINAL*	DESIGNATION
25	Clock — 460.8K	50	Data Set Ready — DSR
24	AR	49	Signal Ground — SG
23	Not Used	48	Digital Loopback — DL
22	AR1	47	TP13
21	Clock — 1.0368M	46	Line Control — LC
20	AT	45	TP12
19	Carrier On Voltmeter — COV	44	Line Transfer — LT
18	AT1	43	TP11
17	Carrier On Delay — COD	42	Facility Test — FT
16	BR	41	TP10
15	Clear Pulse	40	Internal, External — IE
14	BR1	39	TP9
13	+12VT	38	Analog Loopback — AL
12	BT	37	TP8
11	+5VT	36	Carrier On Reliable — COR
10	BT1	35	TP7
9	−12VT	34	Serial Clock Transmit, External — SCTE
8	LTRM	33	Not Used
7	+24V	32	Receiver Data — RD
6	LTRB	31	Not Used
5	+24V	30	Serial Clock Receive — SCR
4	LTRC	29	Not Used
3	24 RTN	28	Serial Clock Transmit — SCT
2	Frame Ground — FG	27	Signal Ground — SG
1	24 RTN	26	Send Data — SD

*The order of the terminals coincide with corresponding location when looking into the plug end (P7).

the received line signal has been lost, as indicated by the low state of COV, RD remains connected to the receiver for approximately one second. When interface lead COD is low, RD is clamped in the high state.

COV Carrier On, Voltmeter. A high level on this lead indicates that energy at T-R of the line interface is above -26 dBm in the 600- to 3000-Hz band. A low level indicates that energy at T-R is below -30 dBm in the 600- to 3000-Hz band. COV will make a transition from low to high within 7 milliseconds of the appearance of energy above -26 dBm at T-R. A high-to-low transition will occur within 10 milliseconds of the fall of line energy at T-R below -30 dBm.

COD Carrier On, Delayed. COD will make a low-to-high transition coincident with that of the COV lead, but the high-to-low transition will be delayed by 1.07 seconds with respect to COV. During this delay interval when COV is low and COD is high, the receiver is in a ***holdover*** condition. During this condition, the line signal has dropped to such a low level that SCR must be derived from the local crystal oscillator. The crystal oscillator has high stability which limits SCR drift. This drift is a small fraction of a clock period from the phase formerly derived from the remote transmitter clock. If the remote signal is reestablished within the holdover period, error-free reception will resume at once.

COR Carrier Off, Reliable. COR represents a signal that is the logical NAND of COV and the output of a guard-band circuit within the DS. The guard-band circuit compares the energy in 300- to 500-Hz band at the receiver input with the energy in the 600- to 3000-Hz band. A low level on COR indicates that COV is high and that the energy in the 600- to 3000-Hz band is significantly greater than the energy in the 300- to 500-Hz band (signal quality good). A high level indicates that COV is low or that the energy in the 300- to 500-Hz band is comparable to the energy in the 600- to 3000-Hz band (signal quality poor). Loss of carrier will be indicated within 10 milliseconds by a low-to-high transition of COR, even in the presence of noise.

IE Internal-External. A high level on lead IE enables the phase-lock circuits to synchronize the transmitter clock (SCT) to the external 2400-Hz clock on SCTE. To ensure proper operation of both the transmitter and receiver timing circuits, SCTE must be accurate to ±6 Hz, and to guarantee holdover for one second, SCTE must be held to ±0.1 Hz. A low level on IE causes the transmitter to derive SCT from the 8.2944-MHz oscillator.

DSR Data Set Ready. A high level occurs on this lead only when all six control inputs (LC, DL, AL, LT, FT, and IE) are low. This is the normal condition with the DS connected to line B. DSR is low if any one or more of these six inputs is high. However, DS 201D may continue transmitting and receiving data when DSR is low; for example, when LT and/or IE are high.

SCTE Serial Clock, Transmitter (External). Externally provided transmitter bit rate clock (generated by the terminal) is used to clock data on SD when IE is high. SCTE is connected internally to SCR when DL is high and AL and LC are both low (digital loopback mode).

LC Line Control. A high signal level on LC with DL low turns the transmitter off; that is, no output signal appears on either transmit line (line A or line B). A high-to-low transition on this lead (with DL low) causes the transmitter to turn on and, assuming LC remains high, the transmitter will process data appearing on the SD lead.

DL Digital Loopback. In this mode the DS acts like a regenerator. The signal on the local SD lead is ignored. A high level on DL with LC and AL both low causes the reconstructed data from the distant DS to be connected to the input of the local transmitter, internal to the DS. Also, the transmit line signal is normal (-15 dBm) if COV equals 1 and is off if COV equals 0. This permits the distant DS to turn off the transmitter of the digitally looped local DS. At the interface, DSR is made low. In addition, SCTE is internally connected to SCR and the SCT add-delete circuits are enabled, causing SCT to be phase-locked to SCR within the DS. A low level on DL with LC and AL both low gives

the normal functions of LC, RD, COV, SD, SCR, and SCT.

AL Analog Loopback. A high level on AL with DL and LC both low causes the receiver input to be disconnected from the line interface, and causes the transmitter output and receiver input to be connected together inside the DS. Hence, the local terminal receives on RD what it sends on SD through most of the circuitry in the local DS for verification of proper DS operation. About an 8- or 9-bit delay (four or five symbols) can be expected between RD and SD through the DS. In the analog loopback mode, the SCT add-delete circuits are disabled (if IE is low) and the SCR circuits are enabled. Thus, SCR may have a jitter of several microseconds about the stable SCT waveform. A low level on AL, DL, and LC causes the normal connection of the receiver input to the line interface.

LT Line Transfer. A high level on LT (with FT low) causes the transmitter output and receiver input of the DS to be connected to line A and disconnected from line B. A low level on LT (with FT low) causes the transmitter output and receiver input to be connected to line B and disconnected from line A. This is the normal condition.

FT ▶A high level on FT (with LT low) causes the transmitter and receiver to be connected to line B and the line A receive pair to be connected through the amplifier to the line A transmit pair. A high level on FT (with LT high) causes the transmitter and receiver to be connected to line A and the line B receive pair to be connected through the amplifier to the line B transmit pair. The amplifier may be optioned for 0 dB of gain for CCIS installations or 16 dB of gain for TSPS installations.◀

SG Signal Ground is the circuit reference in the DS. SG provides voltage reference for other circuits. It is internally isolated from the 24 RTN lead and from the DS housing (FG).

FG Frame Ground. Connector pin electrically connected to 58B housing.

+12VT Test voltages. These outputs are buffered
-12VT voltages with accuracies of ±10 percent
+5VT to provide for test purposes and are not intended to drive loads less than 50k ohms. An accidental continuous short circuit to FG, SG, or 24 RTN lead on any of these test voltage leads will not affect DS performance.

+24V These leads allow the DS to derive its
24 RTN power from a 24-volt CO battery. Lead 24 RTN is isolated from signal ground and frame ground in the DS. A reversed connection between +24V and 24 RTN will damage the 102A power unit and possibly the data set.

LTRM These leads, which are used outside the
LTRC DS, provide an indication of the state of
LTRB relay LT which is operated when the LT lead is high. The leads and contacts are shown in Fig. 5 and located on AR668B CP.

CP Clear Pulse. An output signal on lead CP is used for CCIS diagnostic testing purposes outside the DS. This tests the ability of the SCR add-delete circuitry to remain in the ***in sync*** mode continuously during a period in which no phase corrections are made to SCR.

TP Test Points. The output signals on these leads represent eight test points from TP7 to TP14. These test points can be used as inputs to external test equipment to evaluate data distortion in the received signal.

OPTIONS

3.25 ▶The transmitter output power, the compromise equalizer, and the facility test loopback amplifier gain are manually switched options (Table E). The switches are designated and located on the front plate of AR668B CP (Fig. 1). The middle screw of the right-hand switch and the top two screws of the left-hand switch are not used. There are no other manual controls and no visual indicators.◀

3.26 The optional output level at tip and ring (T1-R1) of the transmitter when connected to a 600-ohm load is 0 dBm ± 1 dB for TSPS use and -15 dBm ± 1 dB for CCIS use.

3.27 The compromise equalizer (IN) option is used to compensate for nominal telephone line distortion. The equalizer (OUT) option is available if C2-conditioned lines or better are used.

TABLE E

DS OPTIONS

SWITCH (ON AR668)	SWITCH POSITION	FEATURE
S1A	UP DOWN	−15 dB OUTPUT FOR CCIS USE 0 dB OUTPUT FOR TSPS USE
S1B	UP DOWN	0 dB GAIN FOR CCIS USE 16 dB GAIN FOR TSPS USE
S1C	UP DOWN	COMPROMISE EQUALIZER IN COMPROMISE EQUALIZER OUT

3.28 ▶The FT loopback amplifier is optioned for 0 dB of gain when used in CCIS and for 16 dB of gain when used with TSPS.◀

4. TEST FEATURES

4.01 DS 201D provides several test features such as digital loopback, analog loopback, line transfer, and facility test. Figure 6 generally shows these test features but they are more precisely shown in Fig. 5. Refer to Table C throughout this part.

DIGITAL LOOPBACK

4.02 The control inputs establish digital loopback (state 3) by operating the RDL relay. This loops RD to SD and SCR to SCTE and opens the SD and SCTE leads at the terminal interface. A pulse called GIP is allowed to pass to the transmitter to align the transmitter countdown circuitry to the same condition as the receiver countdown circuitry, thus maintaining synchronization.

4.03 The DS is processing data all the time on the SD lead except when in digital loopback. While in digital loopback, the signals on IE, SD, and SCTE are ignored and SCT is phase-locked to SCR.

4.04 In state 3, the line signal is 0 or -15 dBm if COV is high (received signal present) and is off if COV is low (no received signal present). This permits the near-end DS to control the transmitted line signal from the far-end DS if the latter is in digital loopback.

ANALOG LOOPBACK

4.05 There are five analog loopback states (states 4 through 8 of Table C) with each state at a different simulated, received-signal power level. The receiver is not connected to either line A or line B when in any of the analog loopback states (relay RAL is operated). Once relay RAL is operated, switching between the five analog loopbacks is accomplished by a transistor-controlled attenuator with a response time of less than one

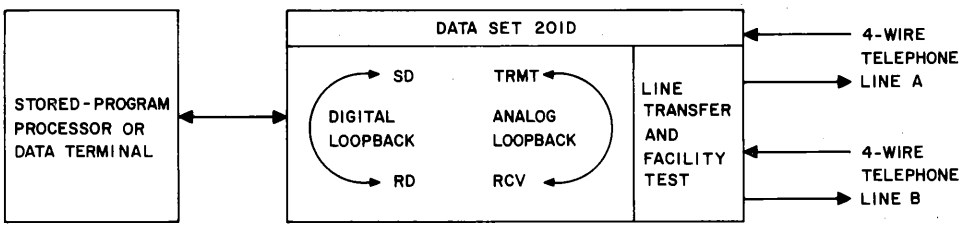


Fig. 6—DS 201D Showing Simplified Test Features

millisecond; thus, is fast enough to test COR response time, sync time, and holdover time.

4.06 In states 1, 4, 5, 6, and 7 (Table C), the transmitter applies the nominal 0 or -15 dBm signal (as optioned) to line A or line B (as selected by LT) at all times such that the near-end testing will not disrupt transmission to the far-end DS.

LINE TRANSFER (LT)

4.07 Line A (AT1, AR1, AT, and AR) and line B (BT1, BR1, BT, and BR) represent two separate 4-wire PLs. The transmitter output and receiver input are normally connected to line B (LT is low). Switching to line A is accomplished by making LT high which activates the LT relay (K3). The DS presents a balanced 600-ohm termination to both lines, except when in the facility test mode. A short circuit between any pairs or a ground fault on any lead will cause no damage to the DS.

FACILITY TEST (FT)

4.08 ▶A low level on FT has no effect on lines A and B. A high level on FT causes the receive pair of the line not selected by LT to be looped back to its transmit pair through the FT loopback amplifier. This permits testing of one line while the other is in use.◀

TESTING AND COMPATIBILITY

4.09 DS 201D ***cannot*** be tested directly with the standard 914B or C data test set (DTS). The 914B or C DTS employs Electronic Industries Association (EIA) negative logic levels (+3 volts equals logical 0 and -3 volts equals logical 1) for SD and RD signals. DS 201D employs positive logic levels (+5 volts equals logical 1 and 0 volts equals logical 0). Thus, the SD and RD signals from the 914B or C DTS (using 511-bit test pattern) must be inverted in logic level and translated in voltage level before being applied to DS 201D. The SCT and SCR clocks from DS 201D; however, they need only be translated (not inverted) in voltage levels before being applied to the 914B or C DTS.

4.10 The DS 201D terminal interface connector does not mate with the 914B or C DTS connector. DS 201D uses a 50-pin connector (KS-16671-L1), whereas the 914B or C DTS uses a 25-pin connector. Other DSs (such as the 201B, 201C, and 205B2) also utilize a 25-pin connector KS-19087-L2).

4.11 Aside from the above-mentioned logic voltage level and connector differences, the DS 201D is compatible with DS 201B, 201C, and 205B2 from both the analog line signal phase shift and the digital logic 1 and 0 standpoints.

4.12 The interface drivers and terminators (AR668B CP) are compatible with WECo 5V TTL (transistor-transistor logic) integrated circuits and WECo 3V 1A integrated circuits. Open-collector drivers are used except for the 460.8-kHz and 1.0368-MHz square waves, which have standard TTL totem-pole outputs.

5. MAINTENANCE POLICY

5.01 The policy depends upon the user diagnostic program for system testing. The program is stored and used by the terminal processor. The program may isolate a fault to a major component of the system such as a terminal, DS, or a voice frequency link including the far-end DS. After a faulty DS is detected, the decision to replace the DS or to isolate a faulty CP depends on the detailed depth of the diagnostic program. The program at TSPS under present planning is to replace the individual CPs. On the other hand, in the CCIS application, program plans are to replace the entire DS with optional replacement of individual CPs. Regardless of the user policy, the faulty component (CP or DS) should be sent to the nearest central maintenance center equipped for DS 201D repair.

6. REFERENCES

6.01 Detailed information for DS 201D may be obtained from the circuit description and schematic drawing (CD- and SD-73090-01). The 102A power unit is described in CD- and SD-82181-01. Additional information may be obtained from the following BSPs.

SECTION	TITLE
592-033-100	Data Set 201D-Type—Identification
592-029-ZZZ	Data Set 201C—Transmitter-Receiver
592-033-180	Data Set 201D-Type—Summarizing Specification