B1 DATA CARRIER TERMINAL SUPERVISORY SIGNALING CIRCUIT

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1. GENERAL

1.01 This section describes the B1 data carrier terminal supervisory signaling circuit, a part of the B1 data carrier terminal described in Section 314-016-150. The supervisory signaling circuit provides a means of transmitting supervisory signals from six trunk circuits (*M* leads) to a distant office via a 150-cps band centered at 350 cps, and for receiving similar signals from a distant office for six trunk circuits (*E* leads). See Fig. 1 for a simplified block diagram.

1.02 A ground placed on an *M* lead of a particular channel will result in an open circuit on the corresponding *E* lead at the distant office, and −48 volts connected to an *M* lead will result in a ground on the corresponding *E* lead (consistent with other *E*- and *M*- type signaling systems).

1.03 The *M* to *E* lead signals from six trunk circuits are transmitted via a single 150-cps bandwidth channel by sequentially sampling each of the six *M* leads and generating a frequency shift keyed signal that changes frequency in accordance with the sample pulses. A sample of an *M* lead that is grounded (on-hook) causes a frequency of 315 cps to be transmitted, and a sample of an *M* lead that is connected to −48 volts (off-hook) causes a frequency of 385 cps to be transmitted.

1.04 Two pulses are added to the *M* lead samples at the end of each sampling cycle or frame to provide synchronization information, and an information pulse (designated trouble pulse) is included to signal the trunk circuits at the distant end to appear busy when a trouble is detected by the local circuits. A frame thus consists of nine bits or pulses. The transmission rate is 95.5 bits per second or one frame every 94.24 milliseconds.

1.05 The transmission delay (not including the transmission facility delay) from an *M* lead to the corresponding *E* lead ranges from a minimum of about 16 milliseconds to a maximum of about 110 milliseconds, depending upon the time difference between the change in *M* lead voltage and the occurrence of the next sampling interval.

1.06 Timing signals for the supervisory signaling circuit are supplied from a separate source, the B1 data carrier terminal carrier supply circuit, in the form of a 477.5-cps square wave for the transmitting circuits and a 3820-cps square wave for the receiving circuits. These frequencies are derived from a common 3820-cps crystal controlled oscillator in the carrier supply circuit.

1.07 Special monitoring and timing circuits are included in the supervisory signaling circuit. If the received signal level is too low or if the demultiplexer loses synchronization, the *E* lead signals to the trunk circuits are frozen until service is restored or, if the trouble persists longer than 3.75 seconds (nominal), until an alarm is activated. The alarm features are discussed in more detail in Part 8.

2. EQUIPMENT FEATURES

2.01 The supervisory signaling circuit uses transistors, diodes, and relays as the active elements and operates from power voltages of +12 and −48 volts. The +12 volts is derived from the −48 volt office supply by the Power Supply Circuit, J87204A (SD-81608-01).

2.02 The circuit components are mounted on 24 separate circuit packages which plug into an aluminum tray. The tray is designed to mount in a standard 23-inch rack and requires about 6 inches of vertical rack space.

2.03 Wherever practical, the logic and gating circuits use simple transistor-resistor logic circuits. More details on the logic circuits are given in CD-73017-01.

2.04 Leads that go to the six trunk circuits, leads to the carrier supply circuit, and the ***AL*** lead (alarm to the testboard) are terminated on three terminal strips mounted along the rear of the mounting tray. The leads that go to the associated channel and line circuits are connected directly to the circuit package connectors.

3. MULTIPLEXER

3.01 It is convenient for the purpose of discussion to divide the supervisory signaling circuit into six functional sections: multiplexer, modulator, supervisory filter, demodulator, demultiplexer, and trouble timer.

3.02 The multiplexer (circuit packages 1 through 4) generates the sequential sampling pulses that gate the ***M*** lead signals onto a common lead (the ***BO*** lead) in the form of +0.2 and +12 voltage levels. A logic diagram is shown in Fig. 2.

3.03 The sampling intervals are generated by combining the outputs of several stages of a binary counter chain into nine transistor "steering gates." When all of the timing signal voltages feeding a steering gate are +0.2 volt, then the output of the gate depends upon the state of the associated ***M*** lead; otherwise the output of the gate is held at +0.2 volt since a positive voltage at any of the inputs will keep the gate transistor saturated. Thus each of the nine gates is "opened" for one of the 9-bit intervals of a frame. Typical wave forms are shown in Fig. 3.

3.04 The two synchronization pulses are arranged to alternate every other frame. This feature makes it easy to distinguish them from the ***M*** lead samples which, generally, repeat for many frames at a time. Fig. 3 illustrates this situation.

4. MODULATOR

4.01 The modulator (circuit package 5) converts the voltage changes on lead ***BO*** (+0.2 or +12 volts) to frequency changes. A voltage on lead ***BO*** of +12 volts causes the modulator to produce an output frequency of 315 cps, and a voltage of +0.2 volt causes an output frequency of 385 cps.

4.02 The nominal output level of the modulator is −13 dbm. This level is reduced to below −42 dbm if the normal +5 volts on the ***CSS*** lead (from the carrier supply circuit) is removed. This signal inhibit feature is included to stop the transmission of any signals if trouble develops in the carrier supply circuit.

4.03 Refer to Fig. 4 for a diagram of the modulator. Transistor Q3 is in an oscillator circuit tuned by the Z2 network. When transistor Q2 is cut off, the oscillator frequency is 315 cps. When Q2 is saturated, the extra inductor in the network, L2, is effectively shunted across the principal inductor L1. This produces an abrupt frequency shift to 385 cps.

4.04 Transistor Q1 inverts and amplifies the input signal (***BO*** lead) from the multiplexer and drives Q2 to saturation or cutoff. When the input voltage is +0.2 volt, Q2 is saturated.

4.05 The output level of the oscillator is stabilized by the two 6-volt zener diodes indicated in Fig. 4. The diodes act to limit the peak-to-peak voltage at the emitter of Q3 to about 12 volts.

4.06 Transistor Q4 is used to isolate the oscillator from the load and to provide the correct 600-ohm output impedance. The input to Q4

is shunted to ground by transistor Q6 when it is saturated. This occurs if the voltage on the *CSS* lead falls to below +0.5 volt. This scheme allows the modulator output level to be reduced to less than −40 dbm by a negative pulse on the *CSS* lead.

5. SUPERVISORY FILTER

5.01 The 620B filter unit contains separate transmitting and receiving filters for the modulator and demodulator, respectively (Fig. 5). Each 620B filter section is connected in parallel with the corresponding filter sections of each of the six data channels.

5.02 Fig. 6 shows the typical response of the two filter sections of the 620B filter. Each section has a nominal bandwidth of 150 cps.

6. DEMODULATOR

6.01 The demodulator detects the frequency changes of the 350-cps signal from the distant end. The nominal input level to the demodulator, from the filter, is −18.7 dbm. However, the demodulator will function properly with any input level between −40 and +10 dbm. The output of the demodulator is +5.2 ±0.6 volts when the input frequency is 385 cps and +0.2 ±0.1 volt when the input frequency is 315 cps. A simplified diagram of the demodulator is shown in Fig. 7.

6.02 The frequency demodulating circuit is shown along the top of Fig. 7 and consists of a limiter, a discriminator network, and an output slicer. Three transistors, Q1, Q2, and Q3, are used as amplifiers in the limiter. The output of each of the amplifiers is limited to about 1.2 volts peak-to-peak by silicon diode limiters. The signal at test point LL is a square wave of fixed amplitude when the input signal is greater than −40 dbm.

6.03 The fourth transistor, Q4, is an amplifier that drives the discriminator network. The discriminator network is a typical Travis-type circuit that uses a pair of stagger-tuned resonant circuits to detect frequency changes. The rectified outputs of the resonant circuits are added to yield a voltage that changes with changes in signal frequency. Fig. 8 shows a typical discriminator response curve. In normal operation the output of the discriminator (at test point DO) is about 4 volts peak-to-peak.

6.04 The output slicer is a circuit that squares the signal from the discriminator. Positive feedback causes the slicer to abruptly switch from one output voltage to the other as the input voltage slowly crosses a threshold. The difference between the input voltage (at test point DO) that causes an output of +5.2 volts and the input that gives an output of +0.2 volt is approximately 0.1 volt.

6.05 The signal loss detector monitors the level of the received signal at the input to the demodulator and generates a warning signal if the input level falls below a critical threshold. The threshold is between −32 dbm and −40 dbm. The warning signal appears on the *CL* lead as +5 volts instead of the normal +0.2 volt.

6.06 The signal loss detector consists of an amplifier that provides about 44 db of voltage gain, a rectifier arrangement to change the amplified signal to a dc voltage, and a slicer to cause the output to switch abruptly if the rectified dc voltage falls too low. An abrupt loss of input signal will be detected by the signal loss detector in about 7 milliseconds.

6.07 The *CL* lead is connected to the output slicer of the demodulator to force the output of the slicer to be held constant (at +0.2 volt) when the input signal is below the critical threshold.

7. DEMULTIPLEXER

7.01 The demultiplexer (circuit packages 12 through 18) accepts the pulses from the demodulator, recovers frame synchronism from the signal, and distributes the *M* lead information to the proper *E* leads. See Fig. 9 and 10 for the logic diagrams of the demultiplexer, and Fig. 11 for the operation sequence.

7.02 A clock signal which corresponds very closely in frequency to the frequency of the sending multiplexer is necessary for the demultiplexer to remain in synchronism. This accurate clock signal is generated by obtaining a 3820-cps signal from the carrier supply circuit,

and dividing the frequency by 40, yielding an output signal of 95.5 cps. The proper phase (to within 260 μsec) is attained by starting the countdown in coincidence with the transition between synchronization pulses.

7.03 Frame synchronism is checked each time the synchronization pulses (described in 3.04) are received. At this time any phase errors are corrected, using the transition between the two synchronization pulses as a reference. Once the countdown circuit has been started, it is allowed to cycle through eight times before being stopped. Since a frame consists of 9 bits (6 carrying ***M*** lead information, 2 carrying synchronizing information, and 1 carrying trouble information), and the clock is stopped after 8 cycles, the next synchronizing transition should occur 1 bit-time after the clock is stopped. Due to distortion and bias in the received signal there will be in general some error in the time of arrival of transitions. In order to maximize the probability of detecting a valid synchronizing transition while rejecting other transitions, a "window" (the T monopulser pulse) is generated. This window is 1-bit interval wide and straddles the expected time of the next transition. If a transition of the correct polarity is detected within this interval the clock is restarted on the transition and the demultiplexer remains in synchronism. If no transition of the correct polarity is detected during this interval, the clock is not started and the K flip-flop, indicating loss of synchronism, is set (at the end of the interval).

7.04 Synchronism is recovered by testing each transition in the frame in sequence until a transition exhibiting the proper alternation of polarity is found. This is accomplished by starting the clock on the first transition detected after loss of synchronism and then checking the polarity of the transition one frame time later. If the polarity is not correct, the next transition is used to start the clock. In this fashion each transition in the frame will be tested for synchronism. In the worst case it requires nine frames, or slightly less than 1 second, to recover synchronism.

8. ALARM FEATURES

8.01 The trouble timer portion of the supervisory signaling circuit provides the various timing and alarm circuits that take action if a trouble is detected in the demultiplexer or the carrier supply circuit, or if the received signal level is too low for reliable signaling.

8.02 If the received signal level is too low, an off-normal signal of +5 volts appears on the ***CL*** lead from the signal loss detector as discussed in 6.05. If the carrier supply circuit is in trouble, an off-normal signal of +0.2 volt appears on the ***CSS*** lead from the carrier supply. If the demultiplexer is not synchronized with the received signal, an off-normal signal of +5 volts appears on the $\overline{K}$ lead from the synchronism recovery circuit of the demultiplexer. These signals are combined in the demultiplexer so that an off-normal signal of +5 volts appears on the $\overline{LU}$ lead if any of the three signals are off-normal (see Fig. 10).

8.03 A pulse detector circuit (see Fig. 12) monitors the bit sampling pulses that occur on the ***SET*** and ***RESET*** leads and the voltage on the $\overline{LU}$ lead. If the pulses fail or if the signal on the $\overline{LU}$ lead is off-normal, an off-normal signal of +5 volts appears on the ***NP*** lead. Any situation that results in an off-normal signal on the ***NP*** lead is treated as a trouble condition.

8.04 As soon as the ***NP*** lead signal indicates that a trouble condition exists the following actions occur:

(a) The red trouble lamp (on CP 11) lights.

(b) The six associated trunk circuits are made busy (by shorting the six B1, B2 pairs).

(c) The seventh information or trouble pulse is transmitted to the distant terminal as a command to make busy the distant trunk circuits.

(d) The 3.75-second timer is started.

(e) The ***E*** lead relays are frozen to prevent false signals from reaching the trunk circuits.

8.05 If the trouble condition exists at the end of the 3.75-second timing interval (nominal) then the following additional actions are taken:

(a) The ***AL*** lead to the toll testboard No. 20A alarm circuit is opened to transmit the alarm condition to the testboard.

(b) The ***E*** leads to the six trunk circuits are opened (to appear as on-hook).

(c) The six ***M*** lead sample pulses and the T (trouble) pulse under the ***Y*** option being transmitted to the distant terminal are forced to appear as on-hook and "in-trouble", respectively. This results in the six ***E*** leads at the distant terminal being opened. When the trouble is cleared service is restored to normal.

8.06 Reception of the trouble pulse from the distant end will cause the six trunk circuits to be made busy, but no other action is taken.

8.07 If either the −48 volts or the +12 volts supplied to the terminal fails, then the six trunk circuits are made busy and the ***AL*** lead is opened without any timed delay interval.

8.08 After the 3.75-second time-out described in 8.05 occurs, followed by the return of good signaling, two modes of behavior are possible, depending on the option provided. Under the ***Z*** option, service is restored immediately upon the appearance of good signaling. Under the ***Y*** option, 2.8 seconds of good signaling must occur before service is restored. The advantage offered by the ***Y*** option is the protection against demodulated line noise briefly resembling good signaling. A momentary return to service induced by these conditions would produce random ***E*** lead closures with the resulting useless occupancy of common central office equipment.

9. MISCELLANEOUS FEATURES

9.01 A test key is provided on circuit package 11 to allow the supervisory signaling circuit to be placed in a test mode. When the test key is operated to the TST position the following actions occur:

(a) The modulator and demodulator circuits are disconnected from the supervisory channel filter and the output of the modulator is connected to the input of the demodulator through a 14-db pad. This allows the transmitted signals to be detected by the demultiplexer.

(b) The trouble timer relays are operated in such a way that the six trunk circuits are made busy, the ***AL*** (alarm) lead is opened, and the six ***E*** leads are opened to prevent false trunk circuit seizures during the testing. The red trouble lamp is allowed to function normally.

9.02 The transmitting and receiving channel filters for the supervisory signaling circuit are mounted on a circuit card similar to the other cards of the circuit. The filter circuit card is coded as 620B filter.

9.03 Test points are provided on all circuit packages to facilitate trouble location and routine tests.

9.04 A special feature of the multiplexer is its ability to generate a 47. 75-cps square-wave output (dotting signal) instead of the usual 9-bit frame signal. Grounding test point DG activates the square-wave generator. This special signal is useful for circuit testing and is also used when the BIAS control on the demodulator is adjusted.

9.05 When fewer than six signaling channels are needed, it is possible to omit certain circuit packages. See SD-73017-01 for the necessary information.

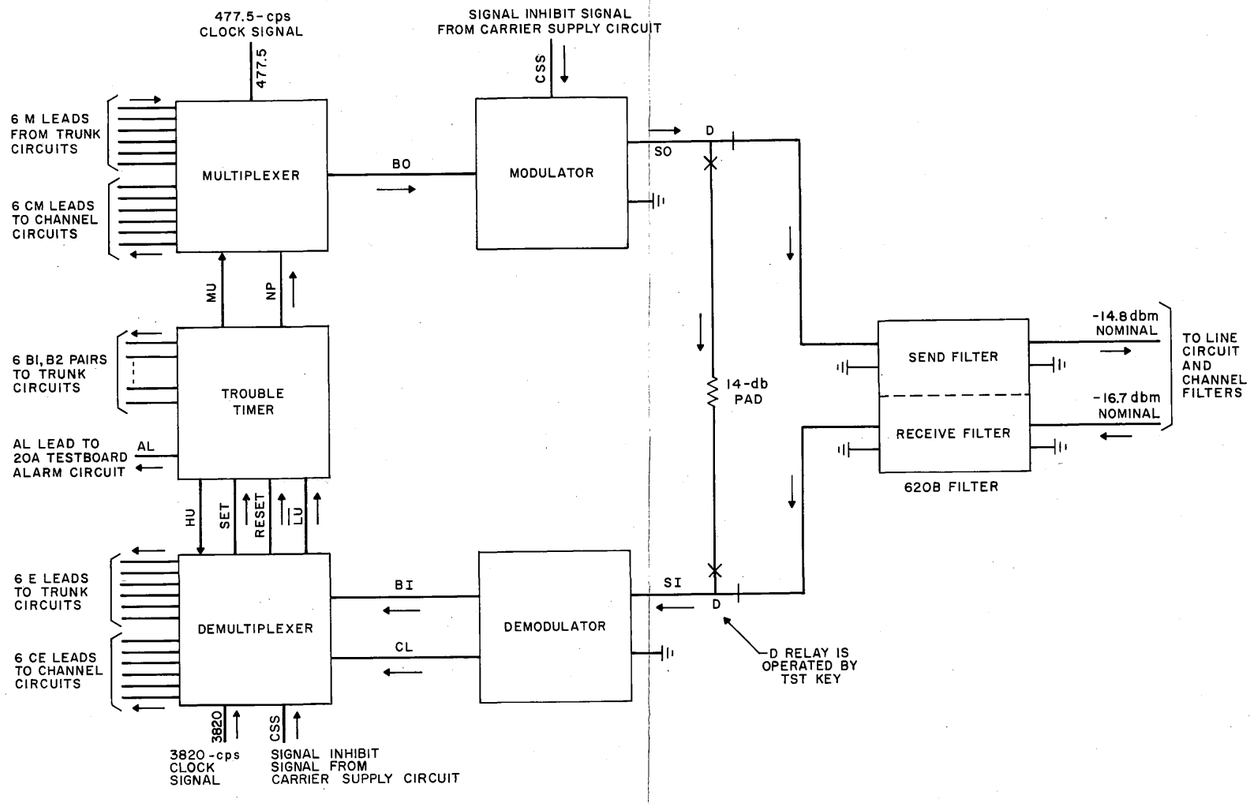


Fig. 1 – Block Diagram Showing Major Signal Leads

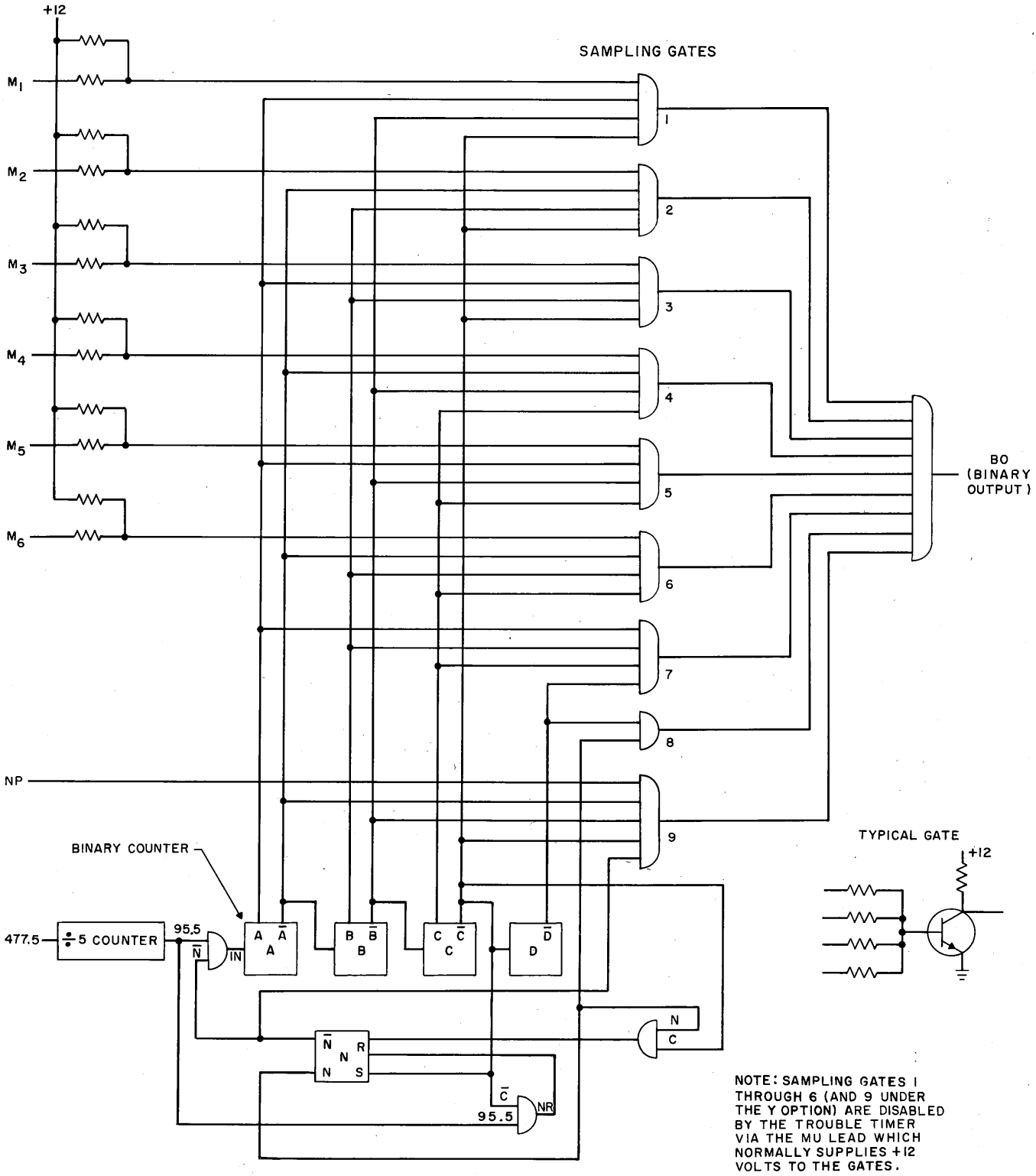
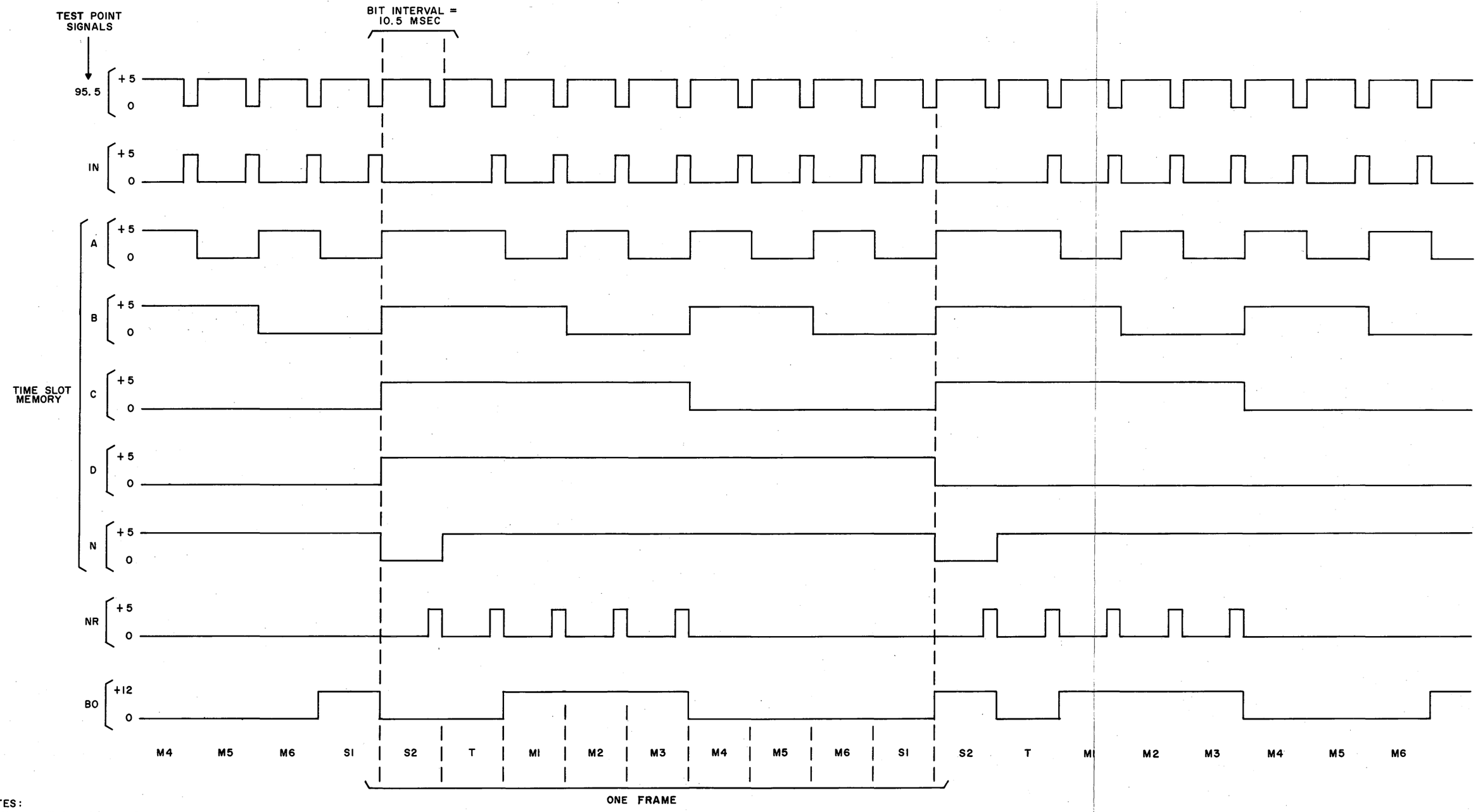


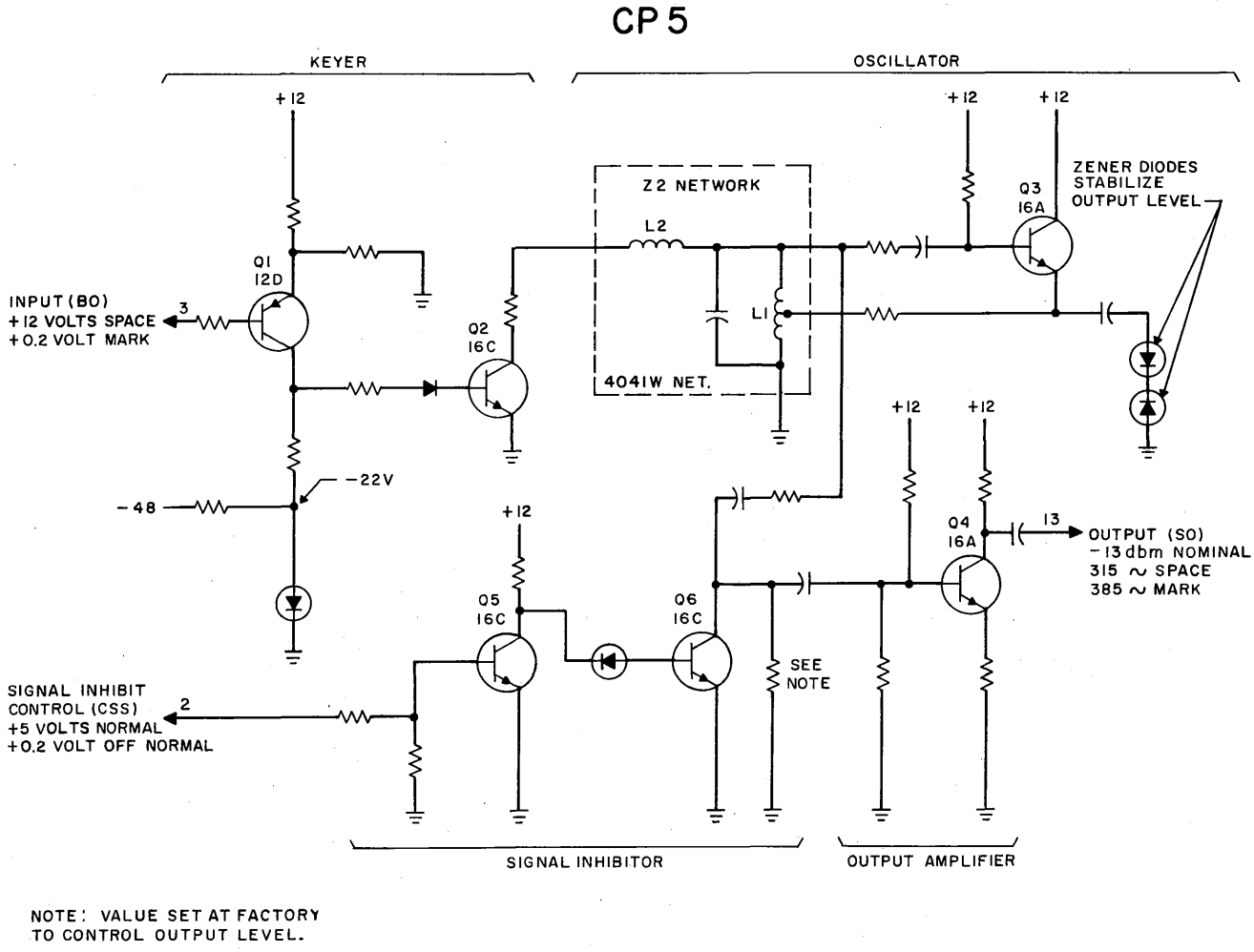
Fig. 2 – Multiplexer Logic Diagram



NOTES:

1. N IS SET BY ACTION OF C RESETTING.
2. N IS RESET BY TRAILING EDGE OF 95.5-CPS PULSES IF C IS AT +5 VOLTS.

Fig. 3 – Multiplexer Operation Sequence



NOTE: VALUE SET AT FACTORY
TO CONTROL OUTPUT LEVEL.

Fig. 4 – Modulator Simplified Diagram

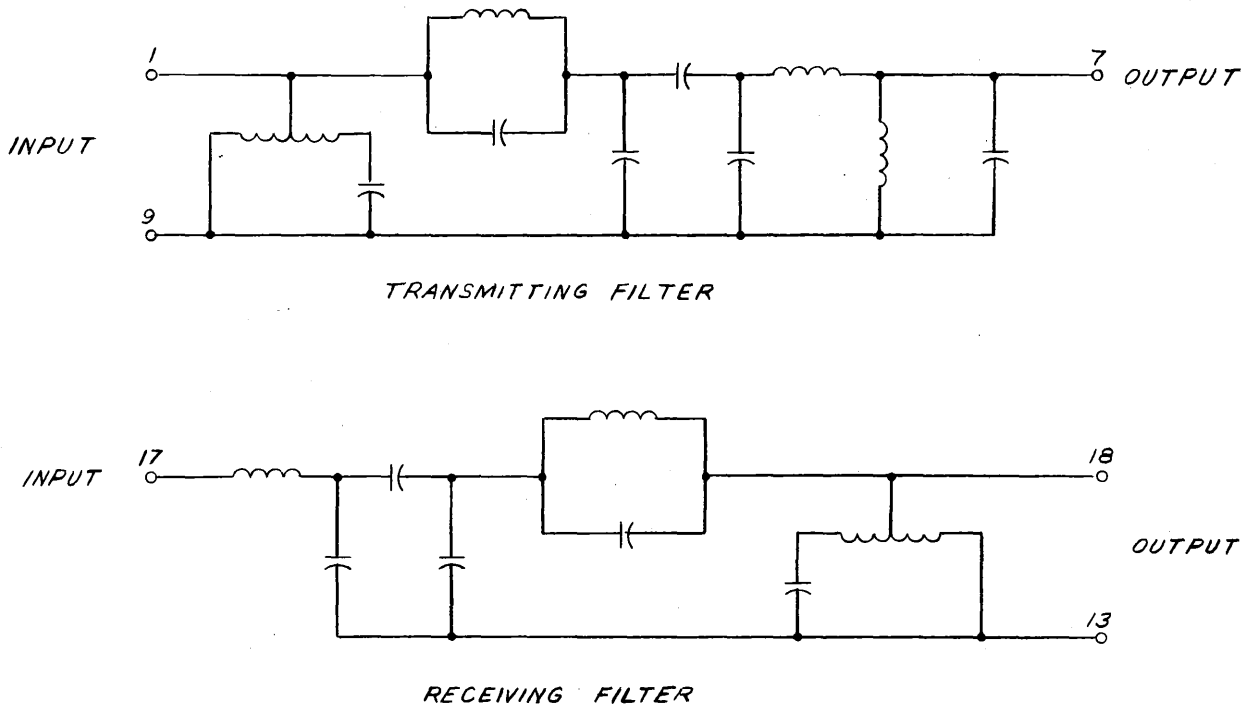


Fig. 5 – 620B Supervisory Filter

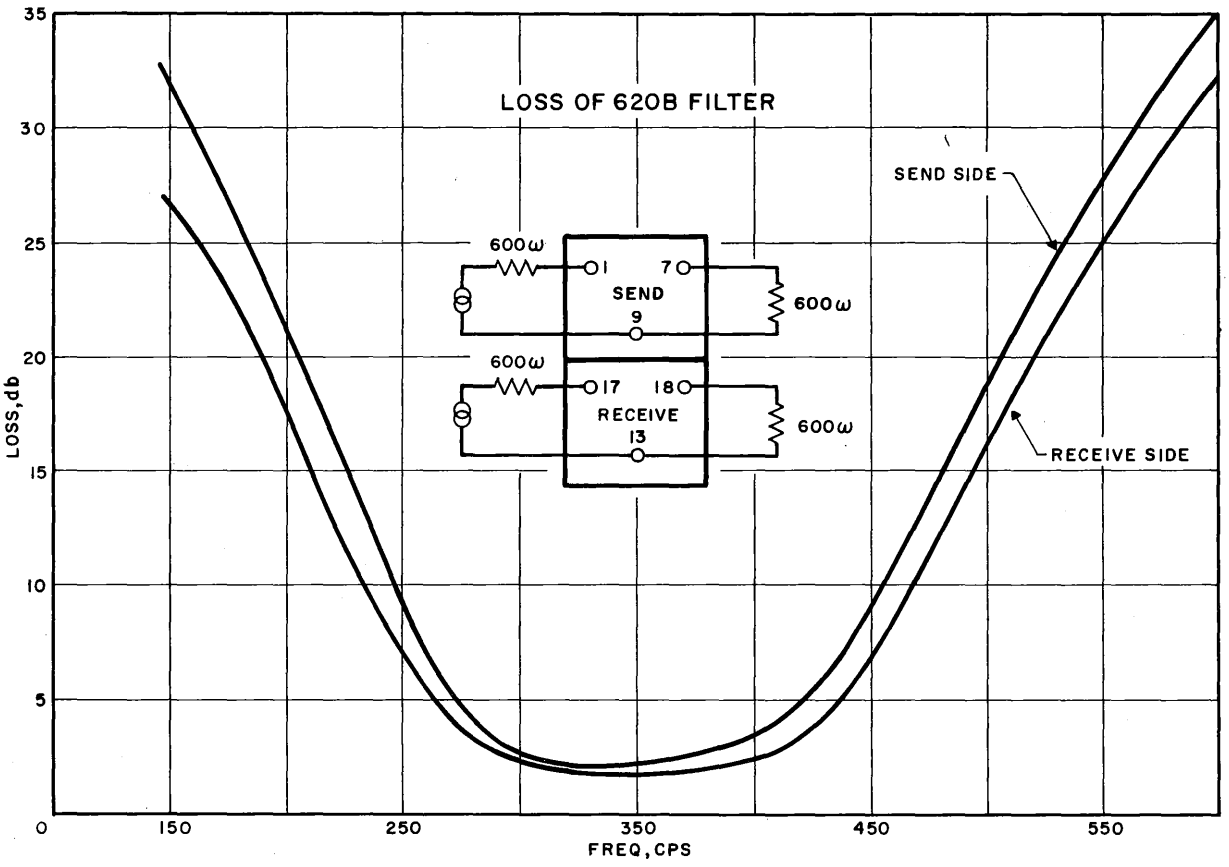
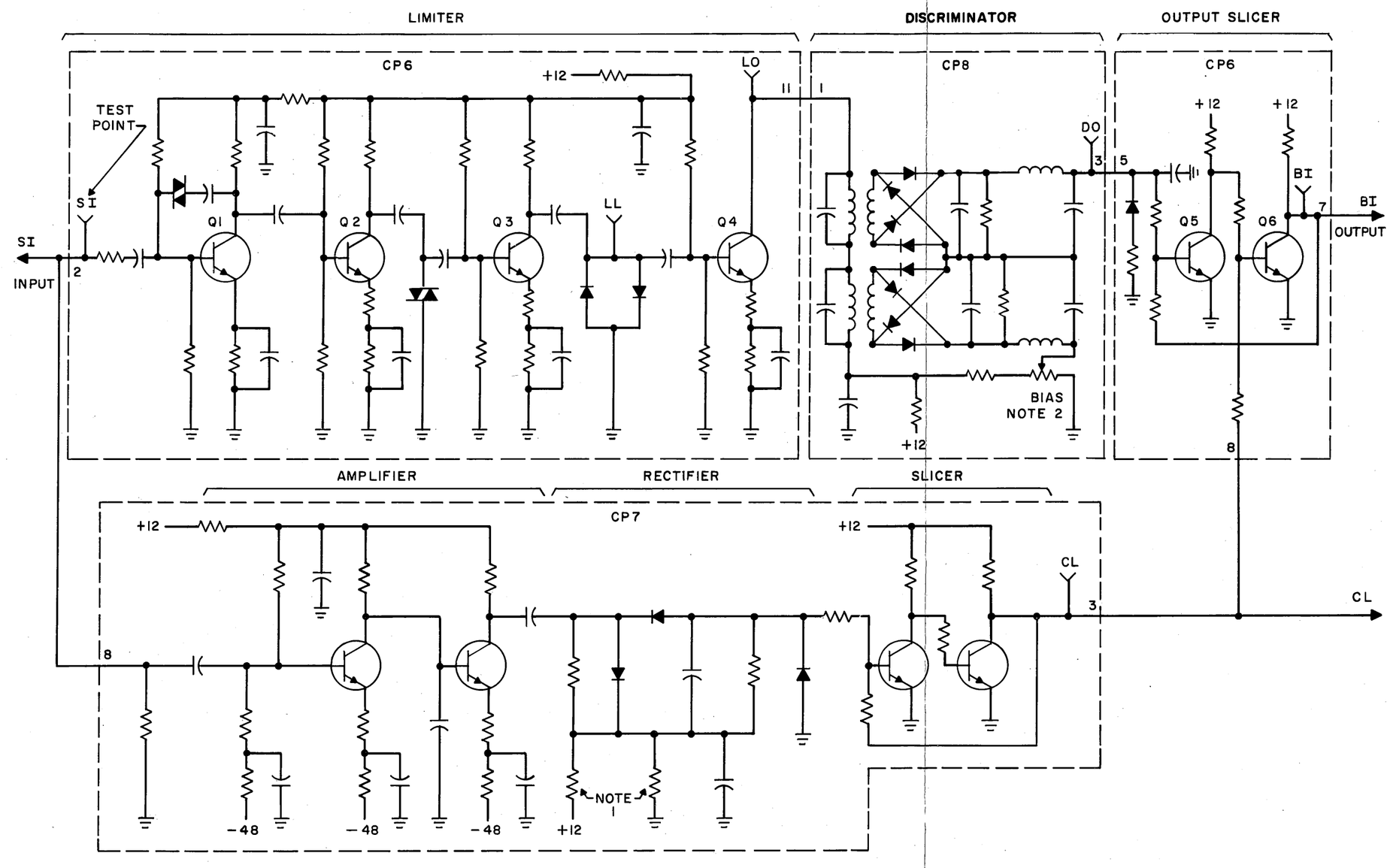


Fig. 6 – Loss-Frequency Characteristics of Supervisory Channel Filter



NOTE 1: VALUES SET AT FACTORY TO GIVE CORRECT SIGNAL LOSS THRESHOLD.

NOTE 2: ADJUSTED IN SERVICE TO GIVE MINIMUM PULSE DISTORTION.

Fig. 7 – Demodulator Simplified Diagram

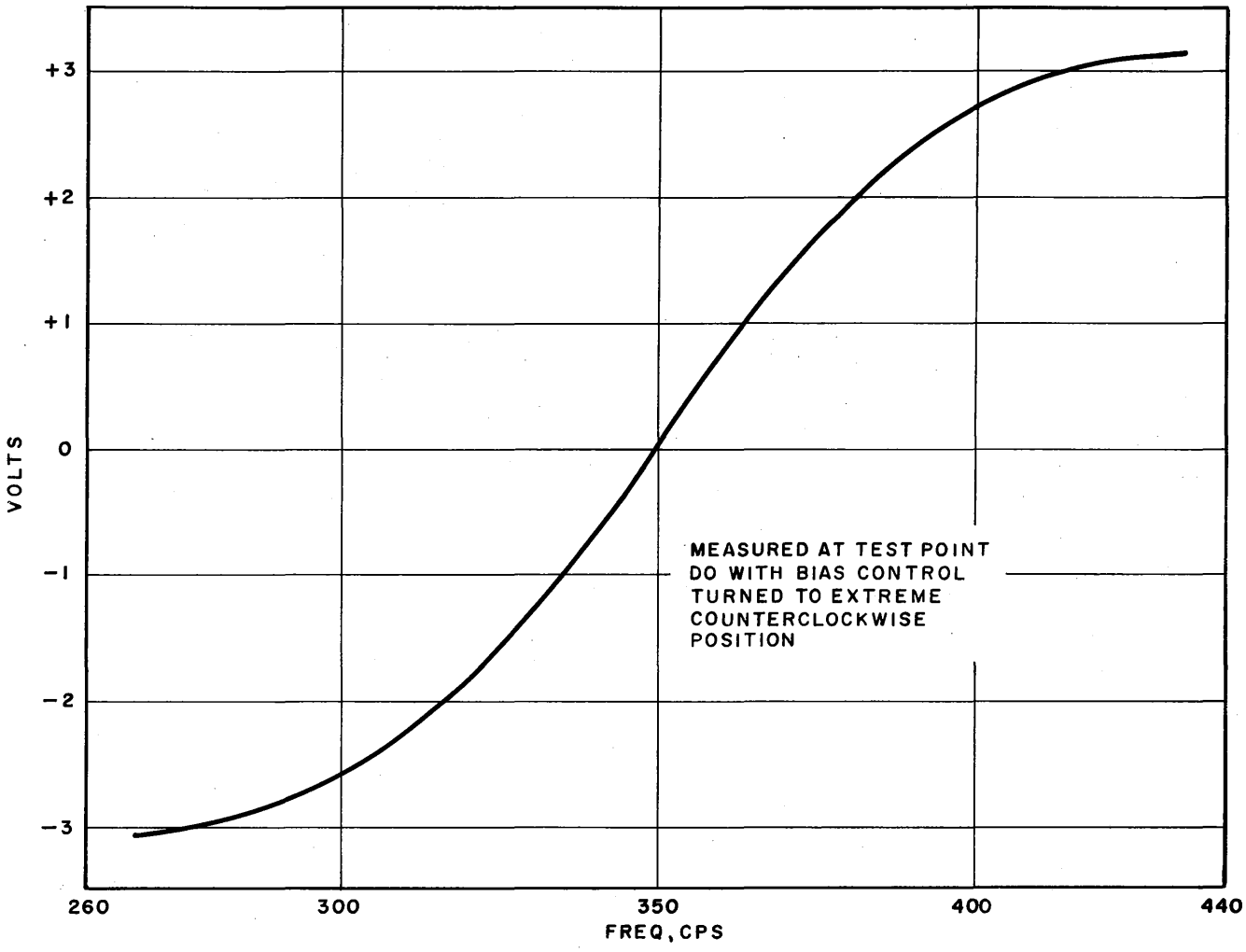


Fig. 8 – Typical Discriminator Response Curve

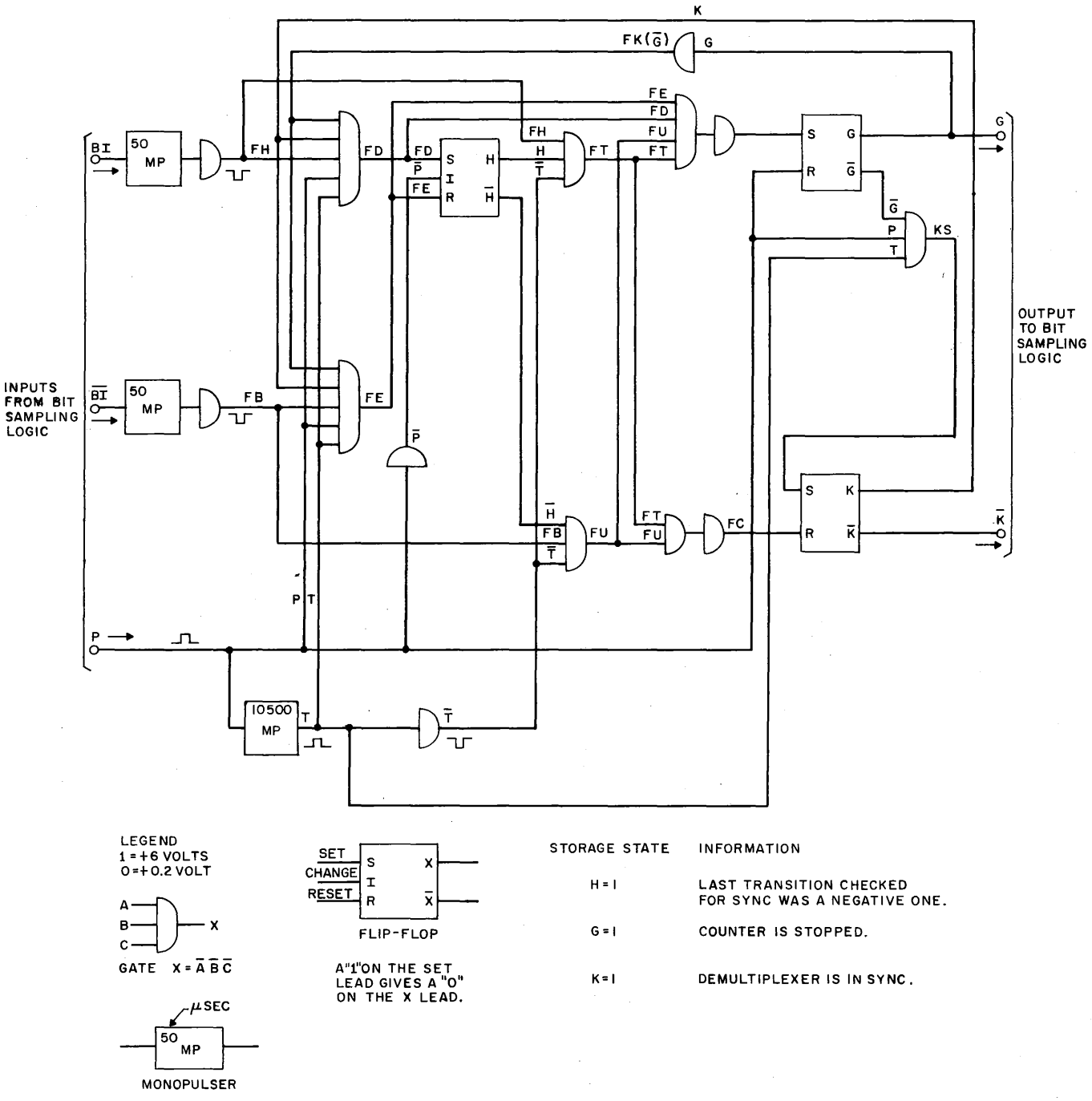


Fig. 9 – Demultiplexer Synchronization Recovery Logic

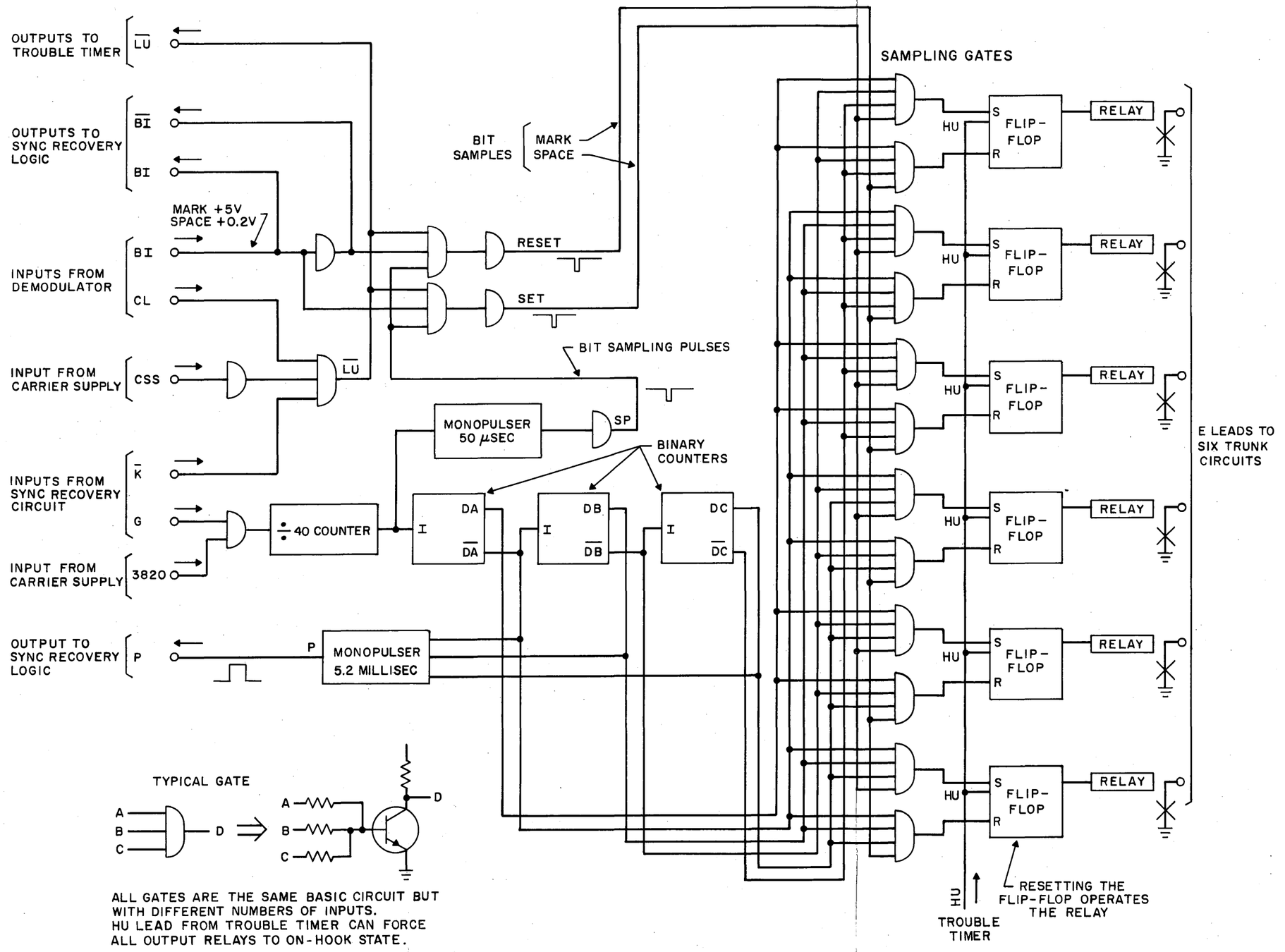


Fig. 10 – Demultiplexer Bit Sampling Logic

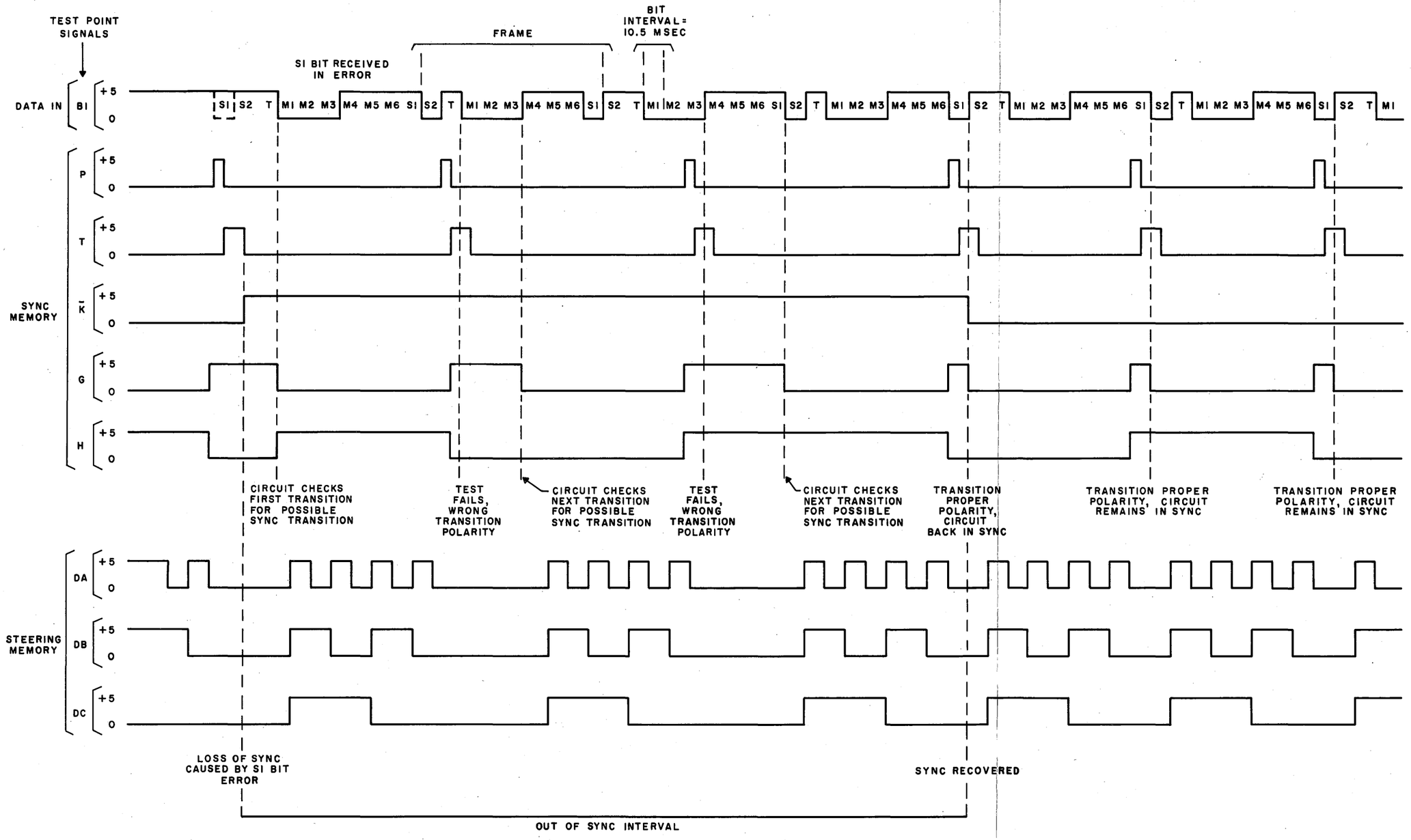


Fig. 11 – Demultiplexer Operation Sequence

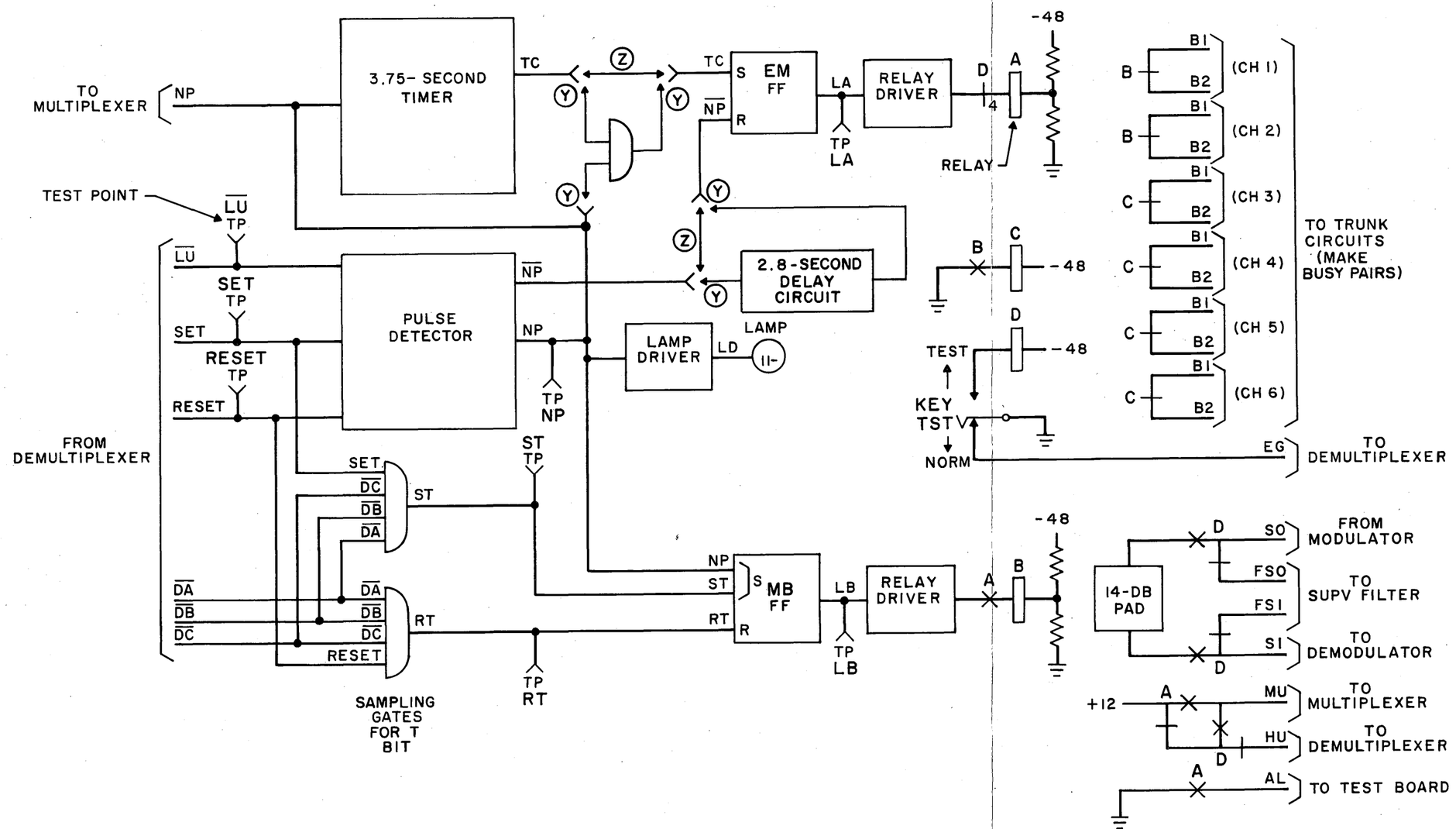


Fig. 12 – Trouble Timer Functional Diagram