DATA SWITCHING NETWORK
ASYNCHRONOUS INTERFACE MODULE (M491)
DESCRIPTION/OPERATION

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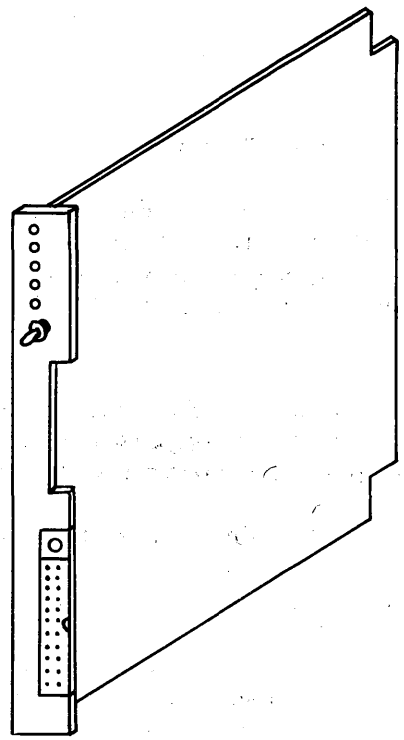


110258 RS232/V.24
Asynchronous Interface Module (M491)
Fig. 1

1. GENERAL

1.01 This section describes the physical and functional characteristics of the 110258 Asynchronous Interface Module (M491).

1.02 (Reserved for future use)

1.03 The M491 Asynchronous Interface Module (Fig. 1) provides a low speed interface between the channel (terminal, data set, etc) and the Real Time Device (RTD) Shuttle Bus in the M3200 System Multiplexer or Switch.

1.04 As a low speed interface, the unit operates in conjuction with a Common Logic Module and interfaces with a Trunk Interface Module when communicating with a remote device. Table A lists the commands and associated functions for this unit.

TABLE A

COMMAND CODE	FUNCTION
E	SENDS STATUS OVER BUS
02	SENDS DATA TO TRUNK INTERFACE MODULE
03	RECEIVES DATA FROM TRUNK INTERFACE MODULE
08	SENDS CONTROL AND DATA TO COMMON LOGIC MODULE
09	RECEIVES CONTROL AND DATA FROM COMMON LOGIC MODULE

1.05 System interface is provided via standard RS232/V.24 Driver/Receivers which convert 12V dc logic level to Transistor Transistor Logic (TTL) levels.

1.06 The module provides serial-to-parallel conversion (data character assembly) from channel to bus and parallel-to-serial conversion (data character disassembly) from bus to channel. It also generates an internal clock 16 times the desired asynchronous data rate and is capable of responding to a remote loop command for diagnostic purposes.

2. PHYSICAL DESCRIPTION

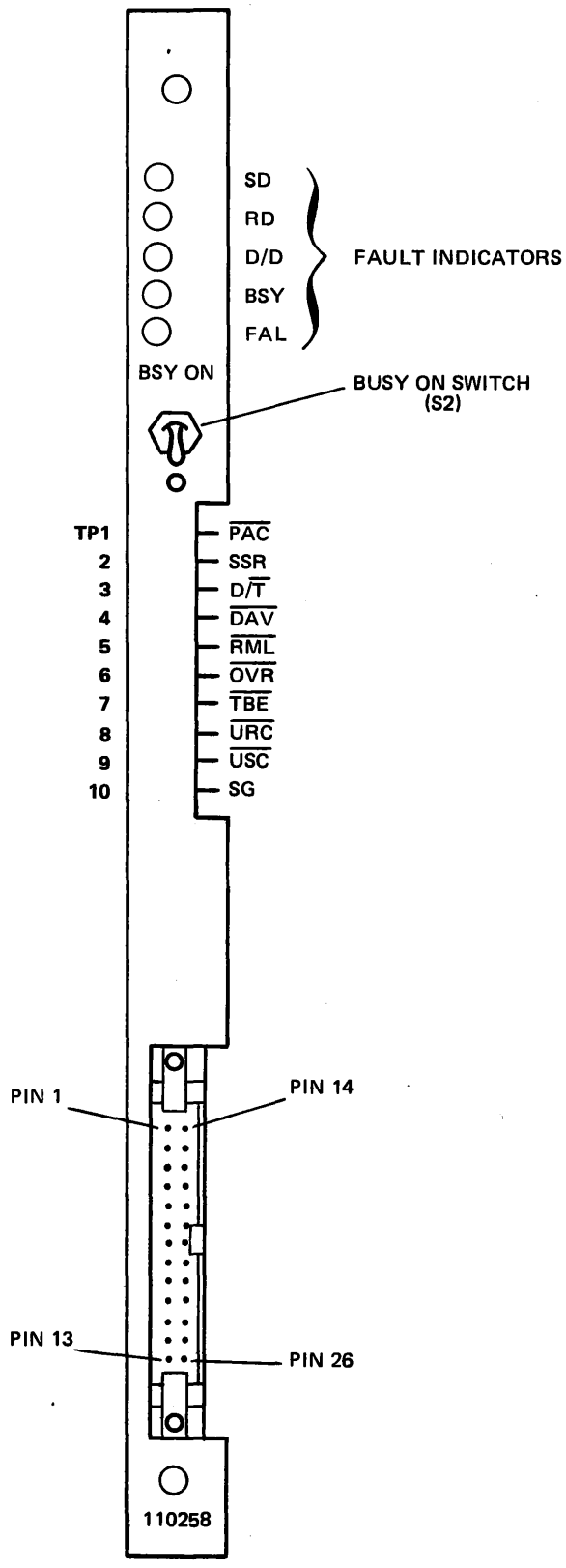
2.01 The unit shown in Fig. 1 is a 7-¾ inch by 13-½ inch Printed Logic Module (PLM). It operates on voltages of +5, +12, and -12V dc at an ambient temperature range of 32° to 122° F (0° to 50° C).

2.02 Provisions on the front panel include 5 fault indicators, one toggle switch, 10 test points, and one 26-pin jack for test access. (See Fig. 2.)

2.03 Table B defines the fault indicators and Table C the test points. Test connector pins and associated signals are listed in Table D.

2.04 Backplane pins on the unit contain 130 contacts that make with the bus. Table E lists these pins and associated signals.

2.05 A slide switch (S1) is located on the right side of the PLM and may be accessed only by removing the module from the chassis.



NOTE: ¯ DENOTES ACTIVE LOGICAL ZERO

Fault Indicators and Test Points
Fig. 2

TABLE B
110258 MODULE FAULT INDICATORS

LAMP	DESCRIPTION
SD	SD (SEND DATA) LAMP IS ON WHEN THE MODULE IS TRANSMITTING A MARK TO A TERMINAL OR DATA SET.
RD	RD (RECEIVE DATA) LAMP IS ON WHEN THE MODULE IS RECEIVING A MARK FROM AN ASSOCIATED TERMINAL OR DATA SET.
D/D	D/D (DATA SET READY/DATA TERMINAL READY) LAMP INDICATES THE STATE OF DSR OR DTR DEPENDING ON THE DEVICE CONNECTED.
BSY	BSY (BUSY) LAMP IS ON WHEN THE RS232/V.24 INTERFACE PIN 25 IS ACTIVE. THIS PIN IS MADE ACTIVE EITHER BY THE CPU (RESOURCE), BY RECEIVING A BUSY CONTROL FROM THE OTHER END OF THE LINK, OR BY THE BSY SWITCH ON THE 0258 MODULE'S FRONT PANEL.
FAL	FAL (FAULT) LAMP IS ON UNDER THE FOLLOWING CONDITONS: THE RTD BUS NOT ACCEPTING DATA FAST ENOUGH (RECEIVER OVERRUN), A LINE DRIVER OR RECEIVER FAULT, OR A REMOTE FAULT.

TABLE C
110258 MODULE TEST POINTS

TEST POINT	DESCRIPTION
TP1	$\overline{\text{PAC}}$ (PHYSICAL ADDRESS COMPARE) IS LOW WHEN THE COMPLEMENT OF THE RTD BUS ADDRESS BITS A00 THROUGH A04 EQUAL THE RTD BUS PA1 THROUGH PA4 LINES.
TP2	SSR (SHUTTLE SLAVE READY) IS HIGH WHEN THE MODULE, A SLAVE DEVICE, IS RESPONDING TO A MASTER DEVICE.
TP3	D/$\overline{\text{T}}$ (DATA SET/TERMINAL*) IS HIGH WITH THE INTERNAL SWITCH (S1) IN THE DATA SET POSITION AND LOW WITH THE SWITCH IN THE TERMINAL POSITION.
TP4	$\overline{\text{DAV}}$ (DATA AVAILABLE) IS LOW WHEN THE MODULE HAS A COMPLETE DATA CHARACTER AVAILABLE FOR THE RTD BUS.
TP5	$\overline{\text{RML}}$ (REMOTE LOOP) IS LOW WHEN THE MODULE IS PERFORMING A REMOTE LOOP.

TABLE C (Contd)

TEST POINT	DESCRIPTION
TP6	$\overline{OVR}$ (OVERRUN) WHEN LOW INDICATES A RECEIVE REGISTER OVERRUN. DATA WAS ENTERED INTO THE RECEIVE REGISTER WHEN IT WAS ALREADY FULL.
TP7	$\overline{TBE}$ (TRANSMIT BUFFER EMPTY) IS LOW WHEN THE MODULE IS READY TO ACCEPT ANOTHER DATA CHARACTER FROM THE RTD BUS.
TP8	$\overline{URC}$ (UART RECEIVE CLOCK) PROVIDES FOR OBSERVATION OF THE INTERNALLY GENERATED RECEIVE CLOCK.
TP9	$\overline{USC}$ (UART SEND CLOCK) PROVIDES FOR OBSERVATION OF THE INTERNALLY GENERATED SEND CLOCK.
TP10	SG (SIGNAL GROUND)

NOTE: * OR $\overline{\quad}$ DENOTES ACTIVE LOGICAL ZERO.

TABLE D
110258 MODULE TEST CONNECTOR SIGNALS

PIN NO.	SIGNAL	PIN NO.	SIGNAL
J1-1	PG (FRAME GRD)	J1-14	
J1-2	SD	J1-15	
J1-3	RD	J1-16	
J1-4	RTS	J1-17	
J1-5	CTS	J1-18	
J1-6	DSR	J1-19	
J1-7	SG	J1-20	DTR
J1-8	CO	J1-21	TEST CONTROL*
J1-9			(INJECT TEST DATA)
J1-10		J1-22	RI
J1-11		J1-23	TEST DATA
J1-12		J1-24	
J1-13	REMOTE LOOP (RL)	J1-25	BO
		J1-26	

NOTE: * DENOTES ACTIVE LOGICAL ZERO.

TABLE E
110258 Module Backplane Signals

PIN NO.	SIGNAL	PIN NO.	SIGNAL
A1	+12 Vdc	B1	+12 Vdc
A2	SG	B2	SG
A3		B3	ENA*
A4	+5 Vdc	B4	+5 Vdc
A5	SMR*	B5	
A6	SSR*	B6	
A7		B7	
A8		B8	
A9		B9	A00*
A10		B10	A01*
A11		B11	A02*
A12		B12	A03*
A13		B13	A04*
A14		B14	
A15		B15	
A16		B16	
A17	D00*	B17	
A18	D01*	B18	
A19	D02*	B19	
A20	D03*	B20	
A21	D04*	B21	A12*
A22	D05*	B22	A13*
A23	D06*	B23	
A24	D07*	B24	
A25	D08*	B25	
A26	D09*	B26	
A27	D10*	B27	
A28	D11*	B28	C00*
A29	D12*	B29	C01*
A30	D13*	B30	C02*
A31		B31	C03*
A32	IOP*	B32	
A33		B33	
A34		B34	
A35		B35	
A36		B36	
A37		B37	
A38		B38	
A39		B39	
A40	PG (J1-1)	B40	F0*
A41	B1	B41	DRDY
A42	B2	B42	SG
A43	B3	B43	SG
A44	B4	B44	SG
A45	AS	B45	SG
A46	DS	B46	TBE*
A47		B47	PA0 (LSB)
A48	PA3	B48	PA1
A49	PG (J1-1)	B49	
A50	SD (J1-2)	B50	
A51	RD (J1-3)	B51	
A52	RTS (J1-4)	B52	
A53	CTS (J1-5)	B53	
A54	DSR (J1-6)	B54	
A55	SG (J1-7)	B55	DTR (J1-20)
A56	CO (J1-8)	B56	
A57		B57	RI (J1-22)
A58		B58	
A59		B59	
A60		B60	B0 (*J1-25)
A61		B61	
A62	+5 Vdc	B62	+5 Vdc
A63	PA4 (MSB)	B63	PA2
A64	SG	B64	SG
A65	-12 Vdc	B65	-12 Vdc

NOTE: * DENOTES ACTIVE LOGICAL ZERO.

3. FUNCTIONAL DESCRIPTION

3.01 This part provides a functional block diagram description of the three basic sections of the 110258 module. These are the Receive, Send, and Common Sections as indicated in Exhibit 1.

A. Receive Section

3.02 The Receive Section consists of the following individual sections of logic: Loop Select, Receive UART, Signature and Status Logic, and Select Logic.

3.03 The Loop Select logic selects input to the Receive UART between incoming data (from RS232/V.24 interface) or outgoing data (from Send UART). Selection is controlled by the remote loop bit during an 09 command word 1. Control signal status input to the RTD bus is also selected between receive controls and send controls.

3.04 The Receive UART consists of an assembly register, a holding register, and control section. The Receive UART controls the DAV (data available) flag for the RTD bus.

(a) The assembly register receives the serial data from the RS232/V.24 interface and assembles it into 8-bit parallel data.

(b) As an 8-bit character is assembled, it is placed in the holding register for subsequent transfer to the RTD bus.

(c) The control section detects the start and stop bits in the serial data stream, checks and verifies correct parity, and determines the specified word length. It also monitors the two registers and when a data character is ready to be placed in the holding register and the holding register is still full, an overrun error is generated.

3.05 The Signature and Status logic places the 02 signature of the module and the status of the control signals on the RTD bus data lines in response to an 08 command word 1.

3.06 The Select logic selects the appropriate data or status to be placed on the RTD bus data lines. The Select logic is controlled by the RTD Address and Command Decode logic.

B. Send Section

3.07 The Send Section consists of the following individual sections of logic: Control Buffers and Send UART.

3.08 Control Buffers provide storage of the status of each control signal for output to the channel.

3.09 The Send UART consists of a holding register, a disassembly register, and a control section.

(a) The holding register accepts one 8-bit parallel character from the RTD bus and holds it until the disassembly register is ready for another character. When the character is placed in the disassembly register, the holding register is now ready to accept another character from the RTD bus.

(b) The disassembly register disassembles the 8-bit parallel character into serial data for output by the RS232/V.24 interface. The start and stop bits along with the correct parity bit are inserted into the serial data stream.

(c) The control section generates the start, stop, and parity bits and determines the word length. The register loading and timing are also handled by the control section.

C. Common Section

3.10 The Common Section contains logic common to both the send and receive sections. This logic consists of the following: RTD Address and Command Decode Logic, Assembly/Disassemble Baud Buffers, and the Assemble/Disassemble Clock Generation logic.

3.11 The RTD Address logic monitors the RTD bus address lines and when the module's address is detected, the RTD Command logic decodes the RTD bus command. This logic then initiates and directs the proper module response.

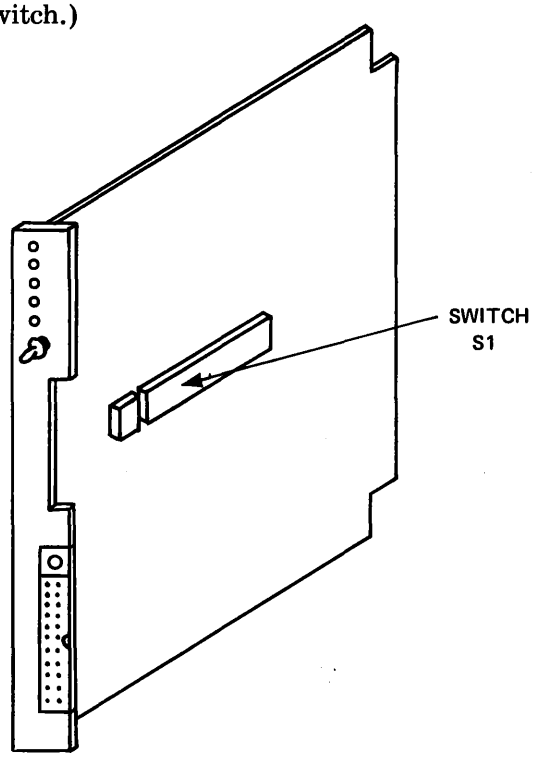
3.12 The Assemble/Disassemble Baud Buffer stores the desired asynchrouous channel data rate (baud) for both the Send and Receive Sections. Both the assemble baud code (for receive) and the disassemble baud code (for send) are stored in these buffers during an 09 command word 2.

3.13 The Assemble/Disassemble Clock Generation logic produces a send clock and a receive clock for internal use by the module. Both the assemble clock and disassemble clock logic receives six clock frequencies from the RTD bus. The assemble clock generator takes the data rate code from the assemble baud buffer. This code is used to select one of the six received frequencies. The selected frequency is then divided down to produce an internal data rate clock which is 16 times the channel data rate. The 16 times receive clock is used by the receive UART for timing. A 16 times send clock, used by the send UART, is generated in identical manner by the disassemble clock generator.

4. OPERATION/PROGRAMMING

4.01 No operating instructions are required for this module other than using the BSY ON (BUSY ON) switch (S2) on the module's front panel. The switch provides the operator with the ability to manually busy-out the channel (RS232/V.24 Pin 25).

4.02 The only hardware programming necessary for this module is a switch (S1) for changing the RS232/V.24 interface between a terminal or data set interface. (Fig. 3 shows the location of the switch.)



Program Switch Location
110258 Module
Fig. 3

5. PROGRAM INSTRUCTION FORMAT

5.01 Commands are issued by the RTD bus master module (ie, the Common Logic module) to specify and control the operation of the slave module (ie, the 110258 module). The 110258 module can respond to the following RTD bus commands:

08 Command, Words 0 and 1

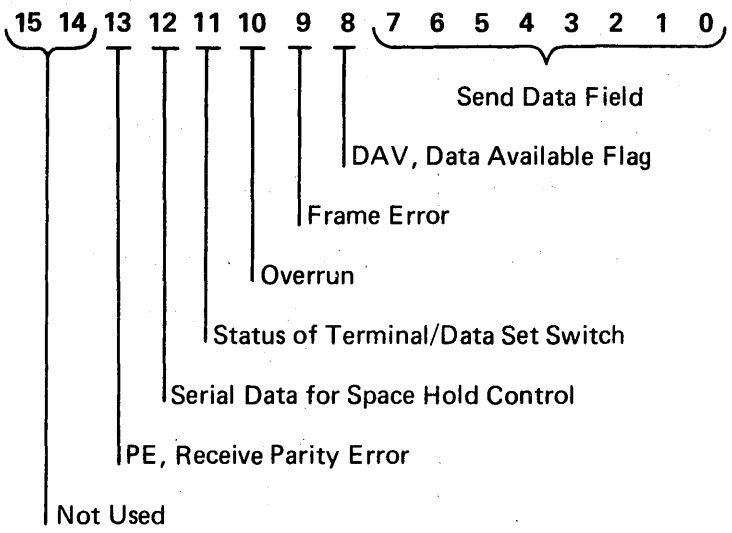
09 Command, Words 0, 1, and 2

Note: From the standpoint of the 110258 module, the 08 Command is a send command and the 09 is a receive command.

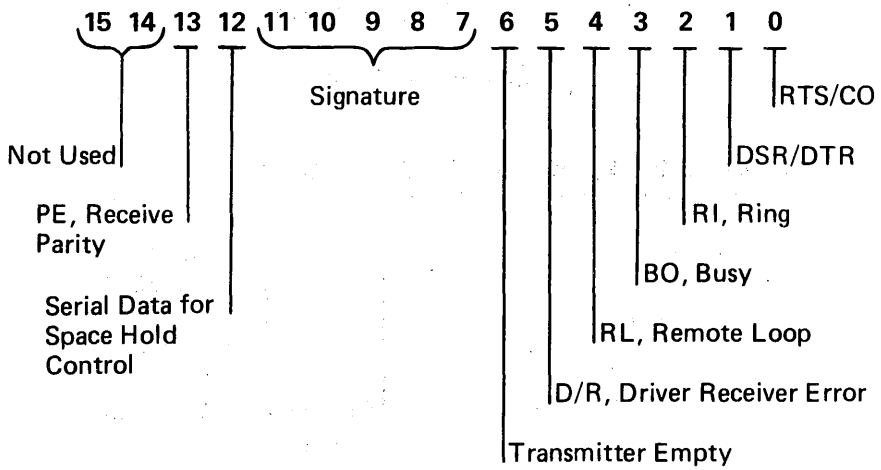
5.02 The 08 Command transfers data (word 0) or controls (word 1) from the slave interface module (110258 module) to the master Common Logic module. (See Fig. 4 for 08 Command formats.)

5.03 The 09 Command transfers data (word 0), controls (word 1), or the data rate (word 2) from the master Common Logic module to the slave interface module (110258 module). (See Fig. 5 for 09 Command formats.)

5.04 Figure 6 shows the RTD Bus Address Line format used by the 110258 module.

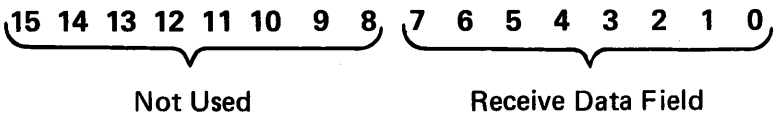


08 Command, Word 0

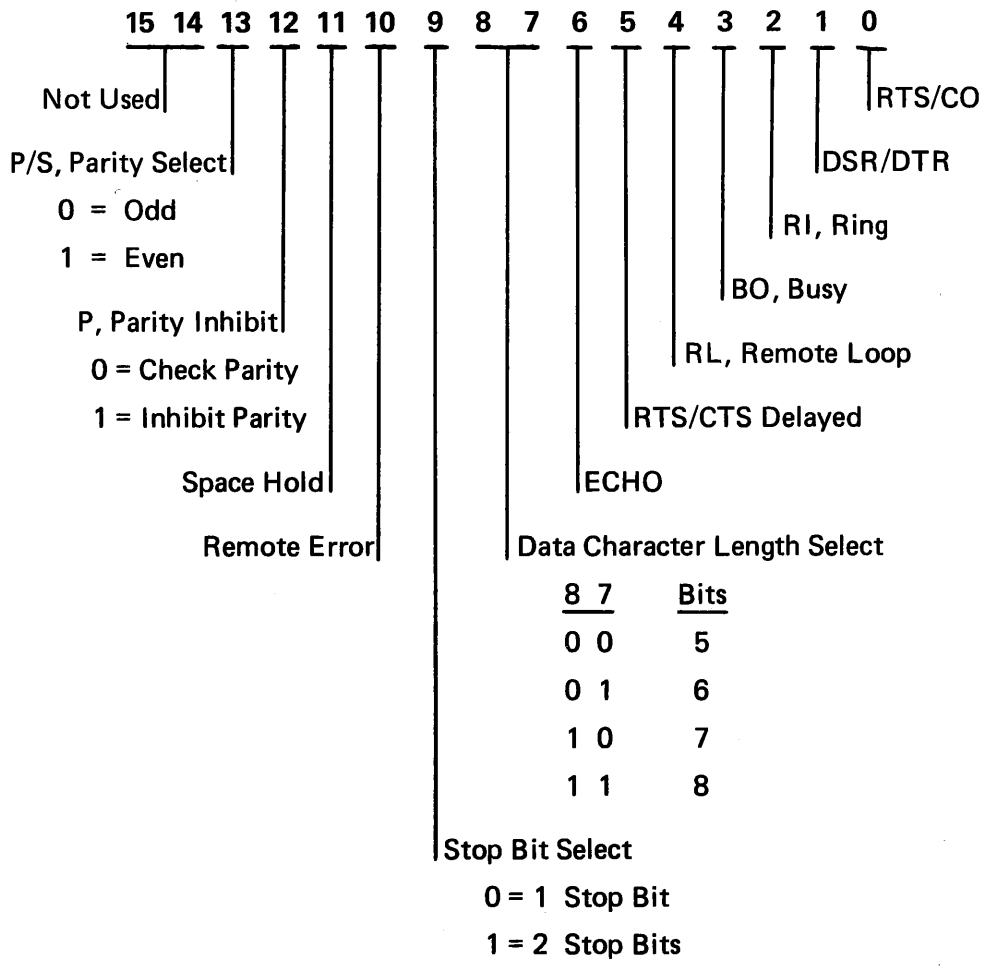


08 Command, Word 1

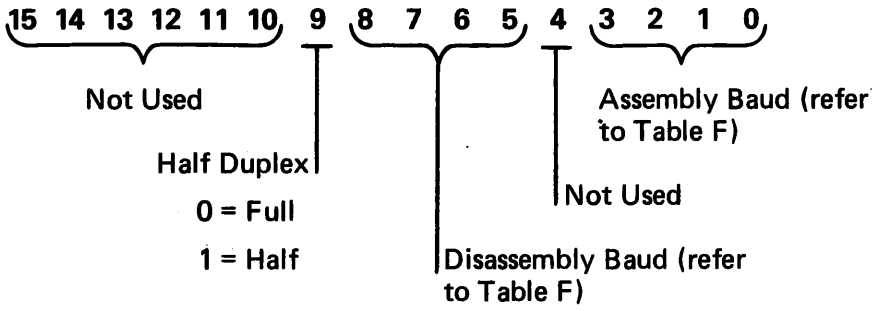
08 Command Formats
Fig. 4



09 Command, Word 0

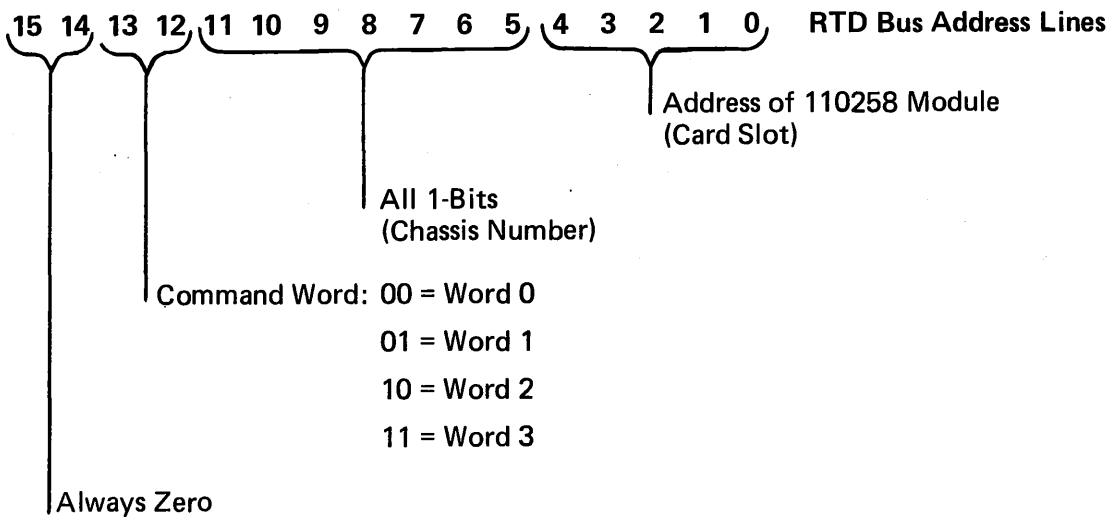


09 Command, Word 1



09 Command, Word 2

09 Command Formats
Fig. 5



RTD Bus Address Line Format
Fig. 6

TABLE F

DATA RATE (BAUD)	CODE HEX	CODE ASSEMBLY/DISASSEMBLY 3/8	2/7	1/6	0/5
50	0	0	0	0	0
75	1	0	0	0	1
110	2	0	0	1	0
134.5	3	0	0	1	1
--	4	0	1	0	0
150	5	0	1	0	1
300	6	0	1	1	0
--	7	0	1	1	1
600	8	1	0	0	0
1200	9	1	0	0	1
2400	A	1	0	1	0
4800	B	1	0	1	1
9600	C	1	1	0	0
--	D	1	1	0	1
--	E	1	1	1	0
--	F	1	1	1	1

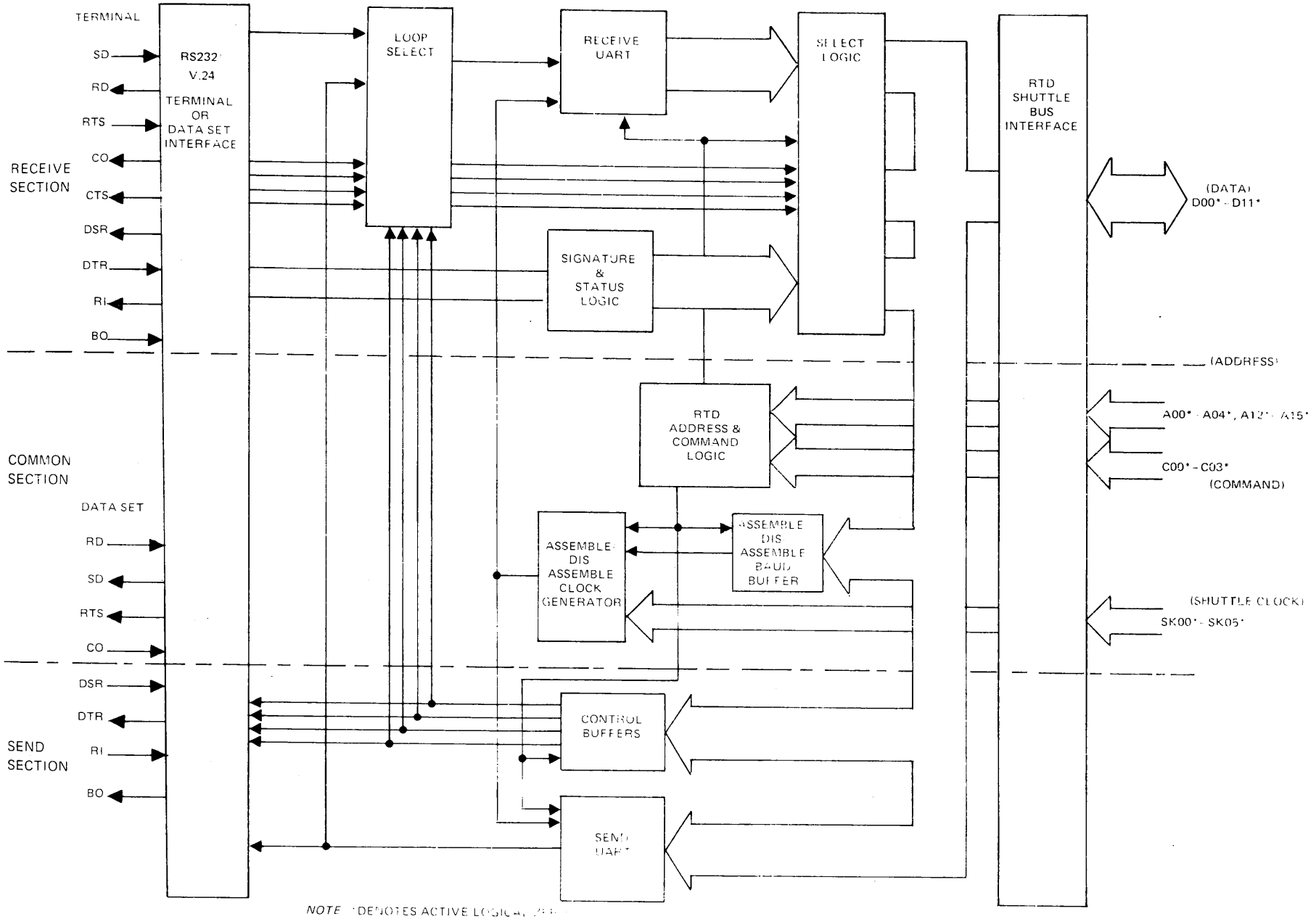
6. MAINTENANCE

6.01 Field repairs that involve replacement of components within this unit are not recommended.

6.02 Troubleshooting is designed to be handled on a push-pull card by card selection under the direction of the Network Control Center (NCC). The NCC computer is designed to provide most of the testing ability on the network.

6.03 All defective units will be processed for repair and return in accordance with the instructions described in Section 314-900-901PT.

6.04 If equipment design and/or manufacturing problems should occur, refer to Section 010-700-010PT for procedures on how to file an Engineering Complaint.



NOTE: * DENOTES ACTIVE LOGICAL ZERO

110258 RS232/V.24 Asynchronous Interface Module (Model M491)
Functional Block Diagram
Exhibit 1