

## SYNCHRONIZATION DISTRIBUTION EXPANDER DESCRIPTION AND OPERATION

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## 1. BACKGROUND INFORMATION

### A. GENERAL

1.01 This practice provides the general description and procedures for the operation of the J98726W-2, J98726W-1, and J98726Y-1 SDE (Synchronization Distribution Expander). Broad schematic coverage is given in application schematic SD-7C389-01 and in SD-7C389-02. The plug-in equipment is coded AHG1, AHG2, AHG2B, AHG3, AHG4, AHG5, AHG10, AHG15, AHG25, and AHG26.

1.02 This practice is reissued to reflect design and operational improvements. The major changes are as follows:

- Additional information on the AHG4 TD (Timing Distributor) circuit pack has been added.
- The AHG5 TD has been added.
- The AHG15 TI (Timing Interface) has been added.
- The J98726Y-1 panel has been added.
- The AHG25 TD has been added.
- The AHG26 TD has been added.

Since this is a general revision, revision arrows are not used.

## 2. DESCRIPTION OF OPERATION

### A. GENERAL

2.01 The synchronization distribution expander (SDE) recovers input timing from either two DS-1, DS-1C, or office clock input signals. A total of 40 composite clock or DS-1 output signals are available from a single, fully equipped SDE shelf. Up to 120 outputs may be made available at a single location by using either the AHG10 or AHG15 auxiliary panel expansion option.

2.02 The SDE consists of a modular construction composed of a shelf assembly and three different classes of circuit packs. The shelf assemblies consist of either the J98726W-1 (fig. 1), J98726W-2 (fig. 2), or J98726Y-1 (fig. 3). The two shelves mainly differ in that the J98726W-1 and J98726W-2 shelves are

mountable in a 23 inch bay and the J98726Y-1, shelf is mountable in a 19 inch bay. The J98726W-2 and J98726Y-1 are both capable of supporting the parallel changeover system (PCS). Each shelf has a fuse and alarm panel which contains dry contact relays for alarm reporting as well as locking alarm cut-off (ACO) switch.

2.03 The SDE is attached to the equipment bay using the brackets on either side of the shelf. These brackets are reversible and allow for both front and rear mounting without additional hardware (fig. 4)

2.04 The three classes of circuit packs (fig. 5) are: timing alarm (TA) timing interface (TI) and timing distributor (TD). One TA is used in each SDE shelf which monitors the alarm information from the TI and TD circuit packs. This information is reported to the fuse and alarm panel. Two TI circuit packs (TI A and TI B) are used in each SDE shelf. Each TI independently recovers and processes input timing information and outputs this information to the TD circuit packs. Up to four TD circuit packs (TD 1, TD 2, TD 3, and TD 4) may be used in each SDE shelf. The TDs select and process the signals output from the TIs and output this information directly to network elements (NE) requiring timing.

2.05 The SDE utilizes full redundancy for both TI and TD circuit packs. Each of the two TI circuit packs recovers timing information independently. This timing information is shared between the two TIs. The TIs share a common input selection circuit that selects only one of the two recovered timing inputs. The selected input is used to derive output signals from both TIs. The input source selection is indicated by the input source (IN SCE) LED on the chosen TI. Each TI outputs a dual-rail unipolar composite clock timing signal to each TD circuit pack. The output signals from each TI are identical.

2.06 The TD circuit packs accept both inputs from the TIs and monitor these signals for continuity. If both signals are good, then a random selection of the input source is made. The TD's input source selection is indicated by the TI INPUT IN USE LED on the TDs faceplate. As long as both TI circuit packs are inserted in the SDE, either LED (TI A or TI B) may be lighted on each TD.

2.07 The TDs output their signals via a backplane harness at the rear of the shelf assembly to the two sets of terminal blocks located above the panel. These blocks are labeled SDE A and SDE B. TD positions 1 and 2 are cabled to the SDE A terminal block and TD positions 3 and 4 are cabled to SDE B terminal block. The output signals may be accessed either directly at the SDE () terminal blocks (direct connect option) or via the adjacent BK A and BK B terminal blocks (cross connect option).

2.08 The output capacity of an SDE installation may be increased by using either distributed or concentrated timing arrangements. Distributed timing arrangements require a master SDE to recover timing from a high stability input source and serve as the office timing master. Other SDE shelves, slaved from the office timing master, are then distributed throughout the office and located where the timing is needed. The benefits of distributed timing are low cabling costs (only two input pairs per distributed panel), reduction of office interference (output cables may be much shorter), flexible growth, and low additional system costs (the low cost AHG10 TI was designed to be used in distributed panels).

2.09 Concentrated timing arrangements allow the direct expansion of a single SDE shelf. The concentrated configuration provides a large number of outputs from a common physical location. Backplane signals from the existing or "main" shelf are carried via cables to physically close additional or "auxiliary" shelves(s). Through the auxiliary shelves act as an extension of the main shelf, they are separately powered and alarmed.

2.10 The signals for the DS-1 or DS-1C input operation mode are obtained either from bridging repeaters or via bridging resistors. If bridging repeaters are used, two separate bridging repeater shelves should be used. One shelf should receive battery from the -48 A feed and the other from the -48 B feed. If only bridging resistors are used, they should be located at the DS-X. Also the TI in the SDE should be equipped with the bridging input option. This option is available on the AHG15 TI. In all cases, the DS-1 or DS-1C inputs should be derived from the receiving ends of two appropriately synchronized, high quality, T1 or T1-C lines. When possible, each line should transverse a different route for best assurance against dual outages.

2.11 The signals for composite clock input operation should be obtained from separate timing sides from the office timing master fig. 6. This arrangement should reduce the risk of common input failures. Examples of office masters are office timing supply (OTS), nodal timing supply (NTS), secondary timing supply (STS), local timing supply (LTS), digital office timing supply (DOTS) and the SDE.

2.12 When the SDE is operating properly, the following indications shall be visible: All lamps on the fuse and alarm panel (F & A Panel) will be extinguished. All LEDs on the AHG1 TA shall extinguish when the MEM button is pressed. Only a single IN SCE LED shall be lighted on one of the two TIs. The TDs should have a single TI OUTPUT IN USE LED lighted (either A or B).

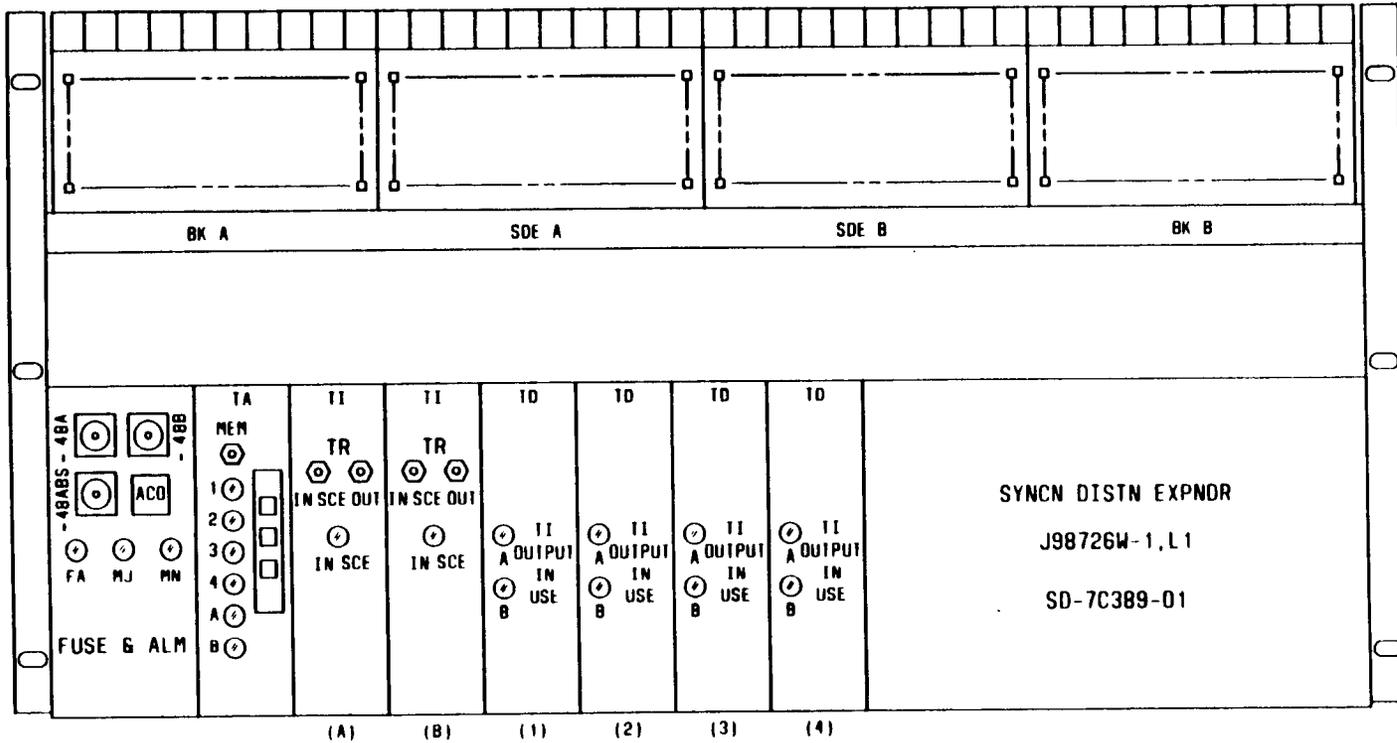


Fig. 1 - Front View of Synchronization Distribution Expander (J98726W-1)

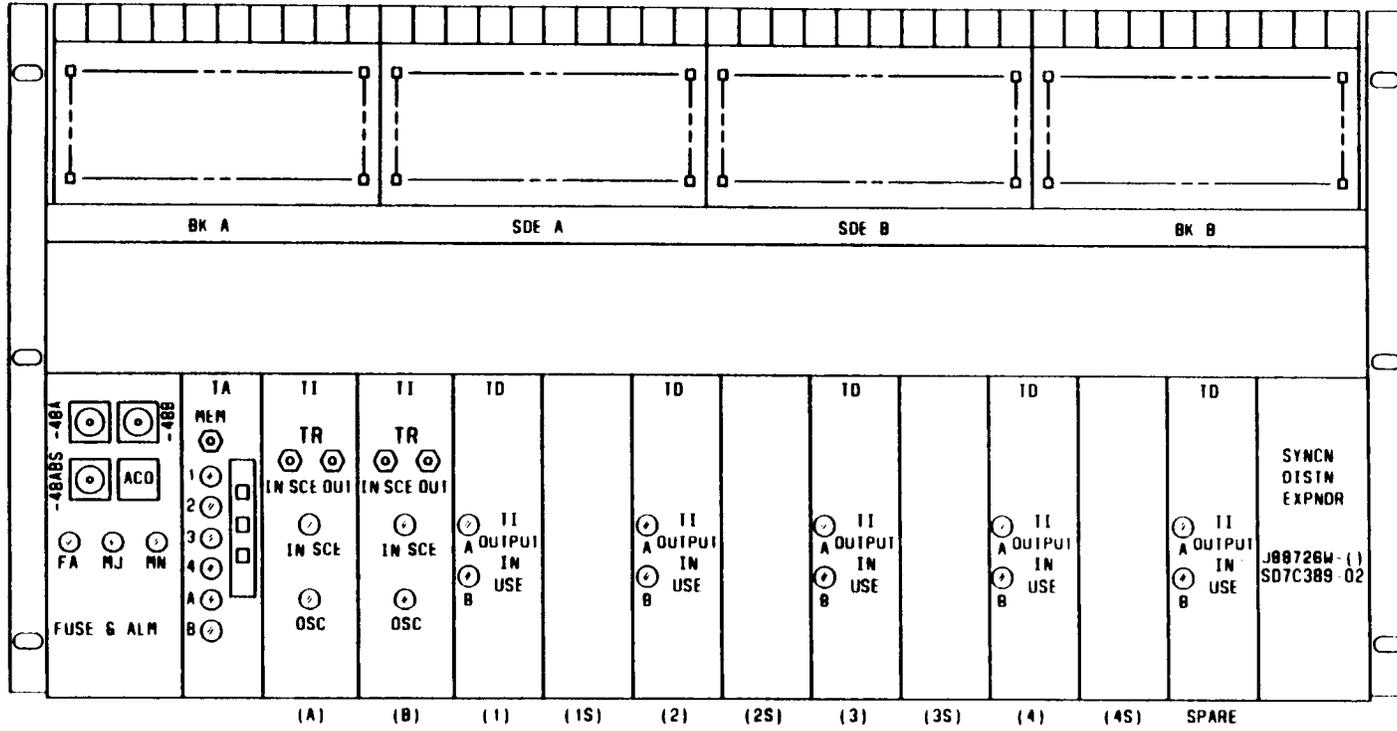


Fig. 2 - Front View of Synchronization Distribution Expander (J98726W-2)

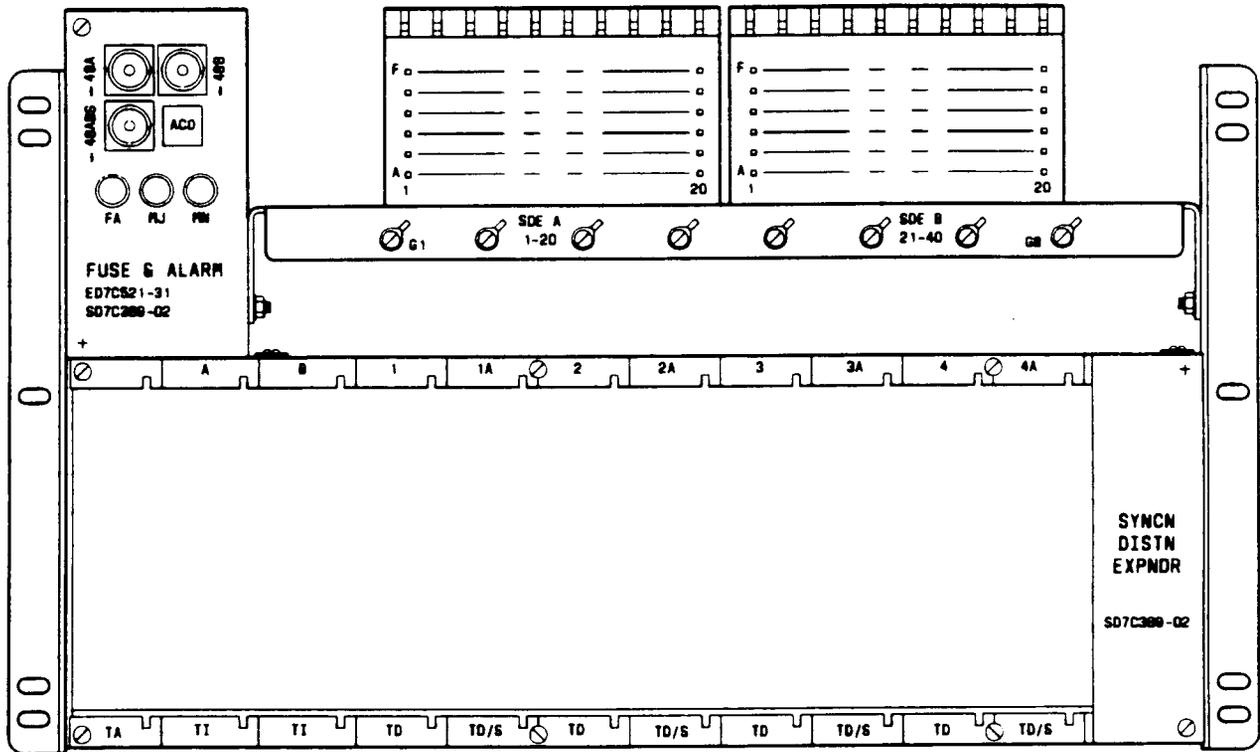


Fig. 3 - Front View of Synchronization Distribution Expander (J98726Y-1)

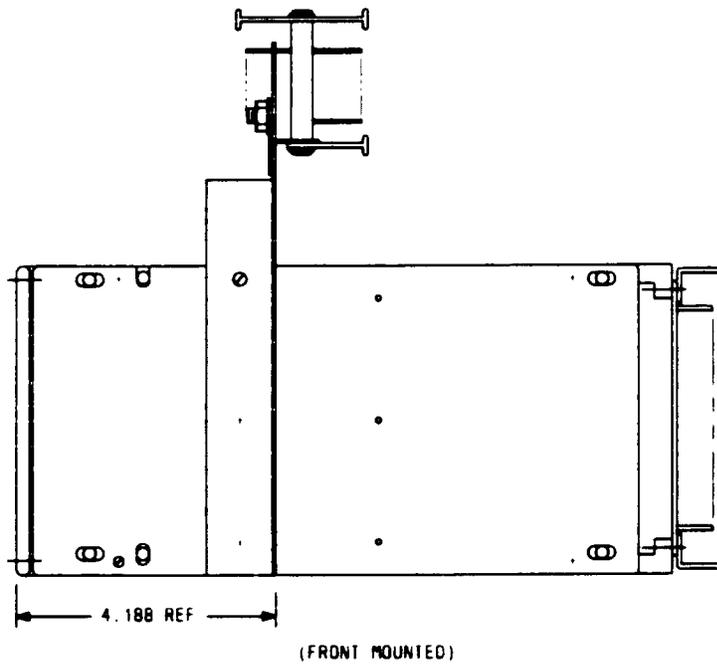
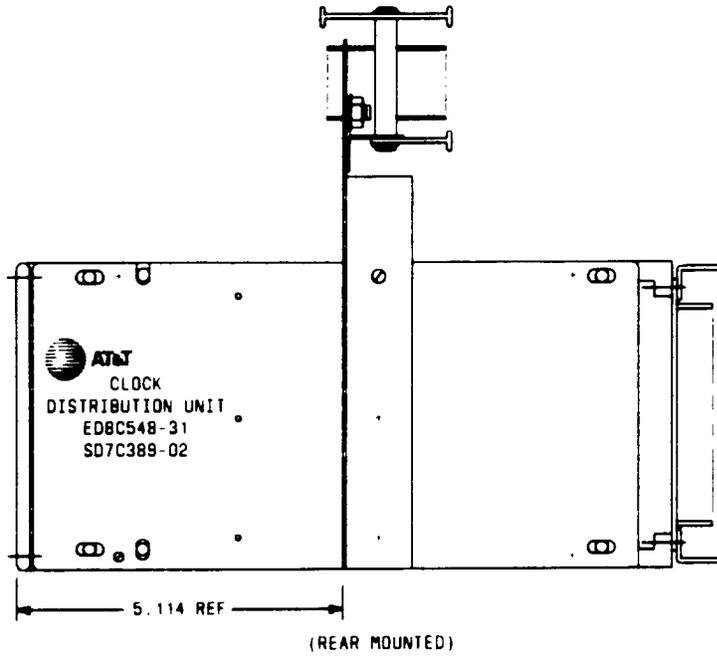


Fig. 4 - Bracket Location for Front and Rear Mounting of SDE

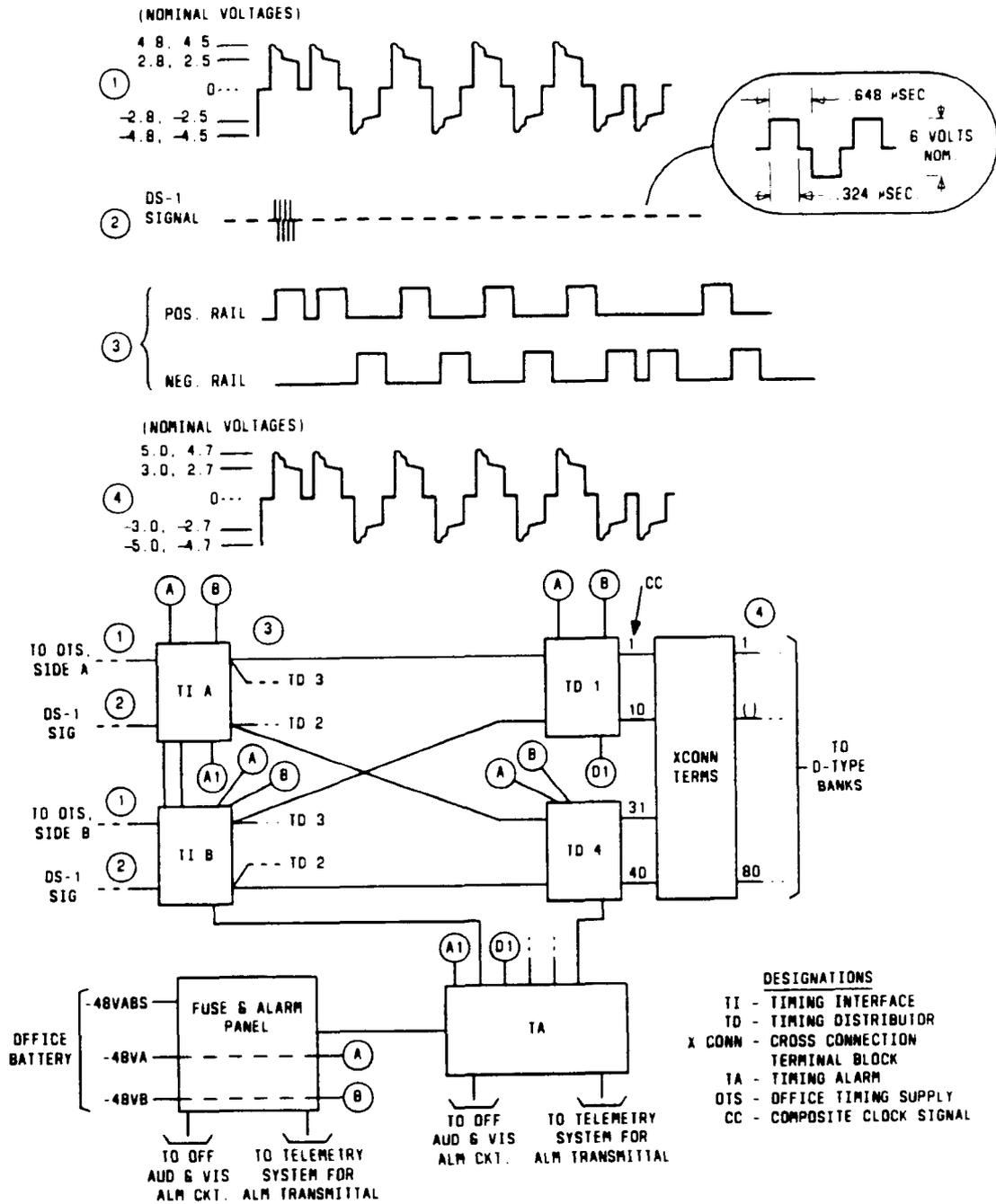


Fig. 5 - Block Diagram of Synchronization Distribution Expander

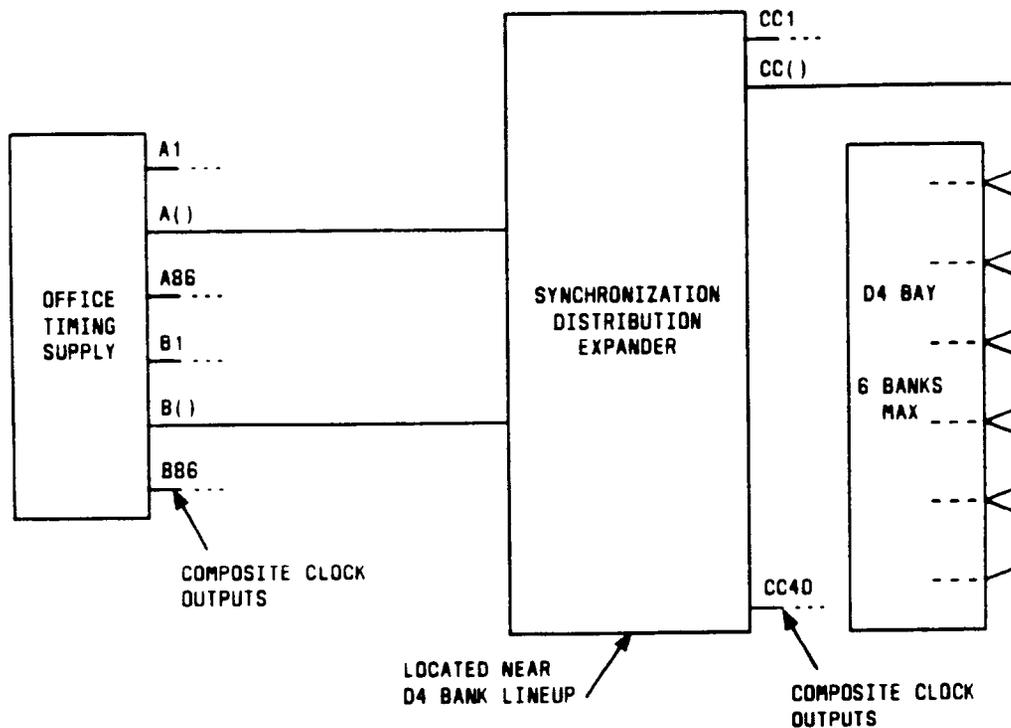


Fig. 6 - Typical Synchronization Distribution Expander Application at Location With Office Timing Supply

3. DETAILED DESCRIPTION

A. GENERAL

Quantity	Name
1	TA
2	TI
1 to 4	TD

3.01 The exterior interface paths to the SDE include power, signal input, signal output, and alarm leads. Several plug-in units form the operational part of the SDE. These units may be readily removed from an out-of-service SDE for easy maintenance. When proper precautions are observed and the parallel changeover system (PCS) is used (SDE only), where necessary, the circuit packs may also be removed from an in-service SDE.

3.02 The plug-in complement of an SDE is as follows:

3.03 The fuse and alarm panel may be removed from the SDE frame by the use of faceplate mounting screws, screw terminals, and a connector. However, because the incoming battery feeds connect directly to the fuse and alarm panel, special care must be exercised on removal from an in-service SDE. If such removal is necessary, information contained in CN8207.1MV, dated 4-12-86, will prove to be most helpful for nondisruptive in-service removal.

3.04 An unwired card slot located on the right end of the frame is provided for the storage of a TD (J98726W-2 only).

## 4. TIMING INTERFACE CIRCUIT PACKS

### A. AHG2 TI

4.01 When the SDE operates with OTS inputs, a composite clock signal from the A-side of the OTS is fed to one AHG2, and a similar signal from the B-side is fed to the other AHG2. Logic elements consisting of small-scale gate array convert the bipolar waveforms of the composite input signals into 2-rail unipolar signals (fig. 7). The unipolar signals of one TI are cross-coupled to the other TI and also feed the output driver gates that deliver two sets of negative logic unipolar signals to the TDs. The durations and repetition rate of the unipolar signals develop from the durations and frequency of the composite clock input pulses without reclocking. The unipolar pulses alternate between the positive and negative rails. Alternately, at an 8-kHz rate a pulse is omitted on one rail, and an extra pulse appears on the other rail to develop the bipolar violation in the composite clock output signals from the TDs.

4.02 When an AHG2 operates with a DS-1 input signal, a hybrid integrated circuit (HIC) containing a phase-locked loop derives a 1.544 MHz clock signal from the DS-1 signal. An integrated circuit counter then obtains a 4 kHz signal that phase locks a 256 kHz oscillator. The oscillator operates logic elements in an integrated circuit to generate the same type of dual-rail clock signal obtained from a composite clock input signal.

4.03 Under normal conditions each AHG2 in an SDE emits the same unipolar signals; however, the polarities may not coincide. In the case of DS-1 inputs, there will also be a phase difference in addition to a possible polarity difference between the two signals. Only one input signal, which enters either the TI A or B, is the originating source of the output signals from both TIs at a given time. The effective input is determined by the state of an S-C flip-flop configured from gates in small-scale integrated circuits. Half of the flip-flop exists in each TI. Backplane wiring between the TIs provides the cross-coupling to complete the circuit. Without manual intervention, the flip-flop may settle in either state to register the selection of either the A or B input for the service signal. The light-emitting

diode (LED) designated IN SCE (input source) on each TI shows whether the A or B source is currently being used by the SDE. A lighted IN SCE LED on TIA indicates use of the A signal source, and a lighted IN SCE LED on TI B indicates use of the B signal source. The input signal selection, A or B, can be changed manually by operating the nonlocking switch TR IN SCE (transfer input source) that has the lighted IN SCE indicator. The IN SCE indicator then lights on the other TI.

4.04 A retriggerable monostable multivibrator in each AHG2 functions as a sensing circuit to monitor the incoming source signal to the TI. If there is an outage of the source signal in service, the multivibrator detects the condition and changes the signal selection flip-flop so as to use the other good input signal. A minor alarm condition is also registered via the TA plug-in unit. If, for example, the A input signal is good and an outage exists on input B, the signal selection flip-flop does not change state if the A signal has an outage simultaneously.

### B. AHG2B TI

4.05 The AHG2B is an upgraded replacement for the AHG2. The AHG2B incorporates the new features of holdover, free run, and frame detection as well as improved operational features common to the AHG2.

4.06 A pair of AHG2Bs may operate with either a redundant pair of composite clock or DS-1 inputs or in a free-run mode for stand-alone applications. The composite clock input option is used in those offices having an NTS, STS, LTS, or a DOTS. If one clock input should fail, the redundant TI will maintain full service. Should both clock inputs fail, both AHG2Bs will switch to a free-run mode of operation to continue to supply its output composite clock. The DS-1 input option is used when it is necessary to synchronize office equipment from incoming T-carrier signals generally traceable to the BSRF. This is accomplished by using bridging repeaters at a DSX-1. Again, continuity of service will be maintained, as described above, if one input source should fail. The SDE will operate in the holdover mode when there has been a failure of both DS-1 inputs. In this case the holdover mode

would "store" the timing information extracted from the last good DS-1 input and continue to allow the SDE to supply its output composite clock. The free-run option would be used in a stand-alone network such as a master in a local data network. This application would require two AHG2Bs set to the free-run mode to provide a redundant source of timing to the SDE.

the DS-1 input by using a dual phase-locked loop (PLL) configuration (fig. 8). The first PLL extracts the 1.544 MHz clock signal from the DS-1 input directly. The second PLL, containing a 12 bit memory circuit and a voltage-controlled crystal oscillator (VCXO), generates a 4.096 MHz signal. This output frequency is then divided to obtain a 256 kHz clock signal that is used to produce the dual-rail clock outputs.

4.07 The AHG2B extracts timing information from

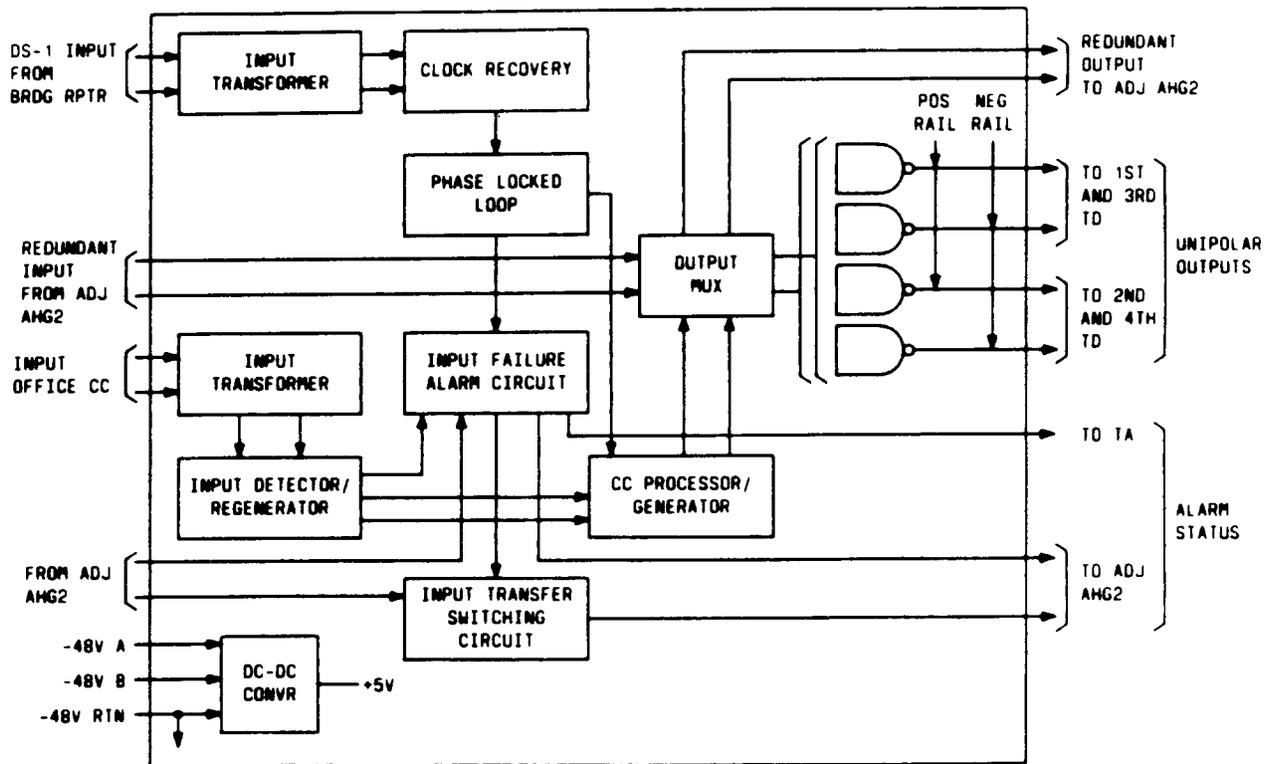


Fig. 7 - Block Diagram of Timing Interface (AHG2)

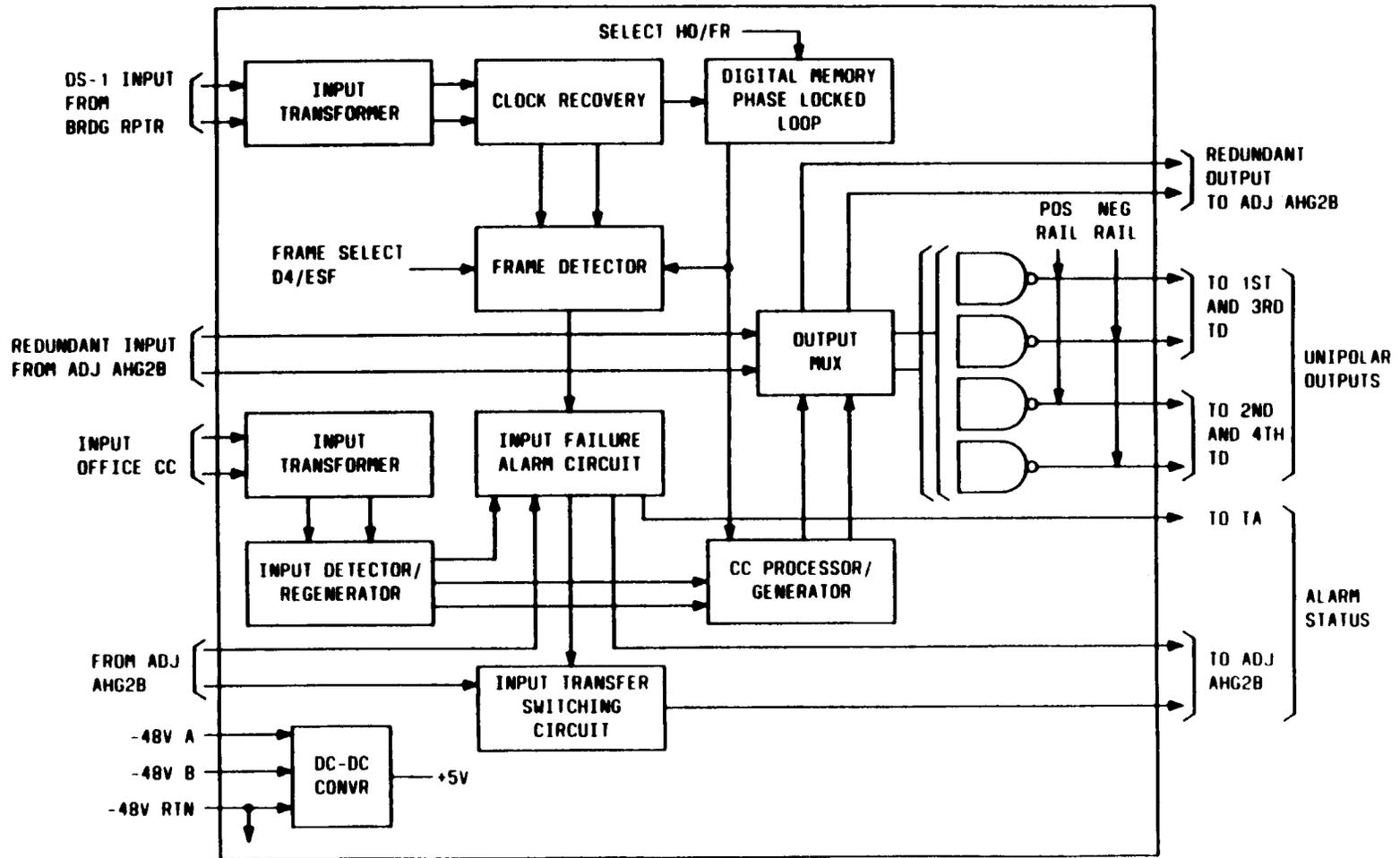


Fig. 8 - Block Diagram of Timing Interface (AHG2B)

4.08 The AHG2B has a frame detection circuit which monitors the framing quality of the DS-1 input for either extended super frame (Fe, ESF) or D4 type framing. A failure of either input source to the AHG2Bs, indicated by a lighted OSC faceplate LED, will cause a source transfer as described above. If both DS-1 input sources to the SDE fail, both AHG2Bs will enter a holdover mode that will provide Stratum III timing for the SDE. The timing reference circuit for the holdover mode contains a 12 bit memory that stores and updates timing information when the DS-1 inputs are good and ceases to update when the DS-1 inputs become bad. In this way the stored timing information becomes the timing reference for a VCXO that will provide frequency synchronous timing in the event of a dual DS-1 failure. Since timing information to the VCXO always comes from the 12 bit memory, no phase hit will occur when switching to the holdover mode. With a VCXO in each AHG2B, the redundant timing configuration is preserved in the holdover mode. When one of the DS-1 inputs is restored, that AHG2B will automatically switch from the holdover mode to the input mode and provide the timing source for the SDE.

4.09 If both composite clock input sources to the SDE fail, both AHG2Bs will enter a free-run mode that will provide timing for the SDE. In this case, the input reference to the VCXO would be a factory preset voltage. Therefore, when switching to the free-run mode, a phase hit in timing could be expected. When one of the composite clock inputs is restored, that AHG2B will automatically switch from the free-run mode to the input mode and provide the timing source for the SDE.

4.10 When the input of a TI is restored, either for a DS-1 or composite clock input, a 1 second recognition delay is employed. The delay provides time for the quality of framing to be checked (DS-1 input) or for the presence to be checked (composite clock input). A 1 second time interval is chosen to guard against bursts of good input that could cause a "false locking" of the TI to the DS-1 input. If the input should become corrupted during this restoration interval, the delay circuitry will reset and

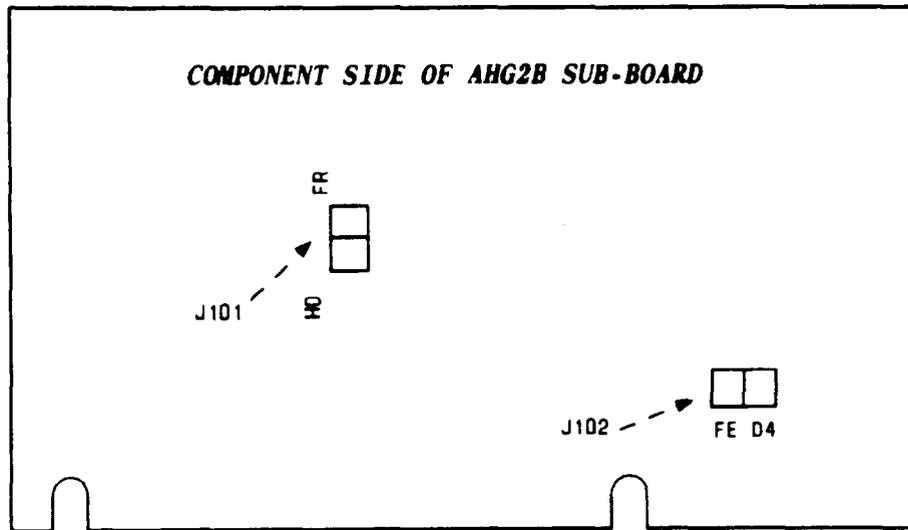
wait for the next indication of a good input signal while still remaining undisturbed in the holdover mode.

4.11 Inter-TI restoration switching is used to minimize the hit time caused by the restoration of a single input to an SDE with two failed inputs. When a good DS-1 input is applied to an AHG2B, a certain amount of time is required for the AHG2B to "lock on." Therefore, a delayed switching protocol is employed. If the input to a AHG2B, supplying the source of timing to the SDE, is restored, then a timing transfer to the adjacent TI will occur for a period of 8 to 12 seconds (lock on time) and then switch back to the now locked-on TI. If the input to the AHG2B, not supplying the source of SDE timing, is restored, then a timing transfer to that TI will occur after the same 8 to 12 second period. If the input signal should fail at any point in the restoration process, the timing transfer will stop.

#### A. AHG2B OPTIONS

4.12 The AHG2B may also be optioned to operate in a free-run mode for which no inputs are used. Visual indication of the free-run mode is provided by the OSC faceplate LEDs on each AHG2B. In this case, the input reference for the VCXO previously described would be a fixed voltage preset at the factory. Two AHG2B circuit packs should be used to preserve the dual-redundancy configuration. Since each VCXO on the two AHG2Bs operates independently, a manual transfer between TIs using the faceplate switches may cause a short burst of errors due to phase or frequency differences.

4.13 Provisioning the AHG2B is dependent upon the type of inputs used. There are two plug and jack assemblies (J101 and J102) located on the sub-board (fig. 9). One assembly, J101, selects either the holdover mode or free-run mode. The other assembly, J102, selects the type of framing to be detected for the DS-1 input when a DS-1 input is used. When DS-1 inputs are used, J101 is set to the HO position and J102 is set to the type of framing being used [D4 or ESF (FE)]. When either composite clock inputs or no inputs are used, J101 is set to the FR position and J102 is a "don't care."



**Fig. 9 - Location of Options for the AHG2B Timing Interface**

### C. AHG10 TI

4.14 The AHG10 timing interface circuit pack allows the SDE to only synchronize from a composite clock input; DS-1 input capability is not provided. The AHG10 is primarily intended for use in distributed timing networks using master-slave SDE arrangements. The AHG10 also provides dedicated output taps for supporting up to two auxiliary SDE panels.

4.15 The input to the circuit pack is a standard composite clock signal. This input is detected by a transformer coupled circuitry and split from a bipolar signal to two unipolar signals. First, these unipolar signals are fed to a buffer stage and finally to the output drivers of the AHG10.

4.16 The composite clock input signal is monitored

by an energy detector (fig. 10) that indicates the disruption of the bipolar input signal. If the input signal is disrupted, the IN FAIL LED on the faceplate of the AHG10 will light. The alarm will be reported to the TA, and the input source will transfer to the adjacent AHG10, provided it has a good input signal. Each pair of unipolar output signals (including auxiliary panel outputs) is also monitored by failure detectors. If one, of all of these pairs of output signals fails (possibly caused by a failed or shorted output driver), the OUT FAIL LED on the faceplate will light and the alarm will be reported to the TA. Output failures will not cause an input source transfer to occur, since an output failure does not mean that the input source is bad. If it is necessary to remove an AHG10 TI with both IN SCE and OUT FAIL LEDs on, the IN TR should be activated first to cause an input transfer to the good AHG10 TI.

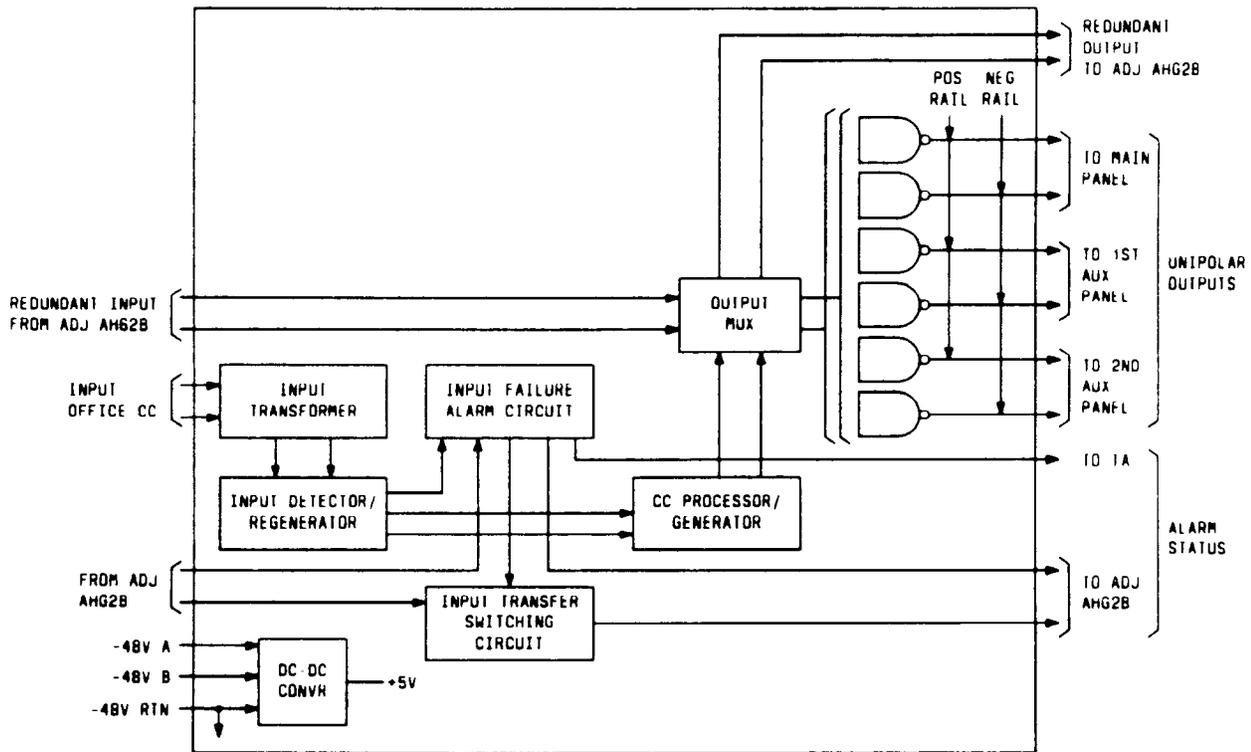


Fig. 10 - Block Diagram of Timing Interface (AHG10)

4.17 Manual input source transfers between a pair of AHG10s are accomplished by actuating the IN SCE TR switch on the faceplate of each AHG10. Since the AHG10 only accepts phase-synchronous composite clock inputs, there will not be any hits during input source transfers.

**D. AHG15 TI**

4.18 The AHG15 TI allows the SDE to recover timing information from either a DS-1C mode 2 input, DS-1 input with ESF or D4 framing, or a composite clock input. In addition, the AHG15 has hitless

input switching capability to allow uninterrupted timing during input reference switching.

4.19 The basic circuit operation is very similar to that of the AHG2B. Differences in the circuit operation are in the areas of input signals, input bridging option, automatic input reference switching, composite clock bipolar violation density checker, and alarm features. Additional features include dedicated output timing taps on each TI to allow connection to two auxiliary SDE panels without requiring TI's for these additional panels.

4.20 The DS-1 and DS-1C inputs are processed by a dual phase-locked circuit with built in jitter suppression (fig. 11). Options on the input circuitry allow various conditions to be monitored (framing and signal continuity) which allow only good inputs to be used as an input source. The recovered

frequency from the DS-1/DS-1C circuitry is then processed by a dual-rail unipolar generator which sends timing signals to the timing distributor (TD) circuit packs. The composite clock inputs are fed directly into the dual-rail unipolar generator which keeps the throughput delay to a minimum.

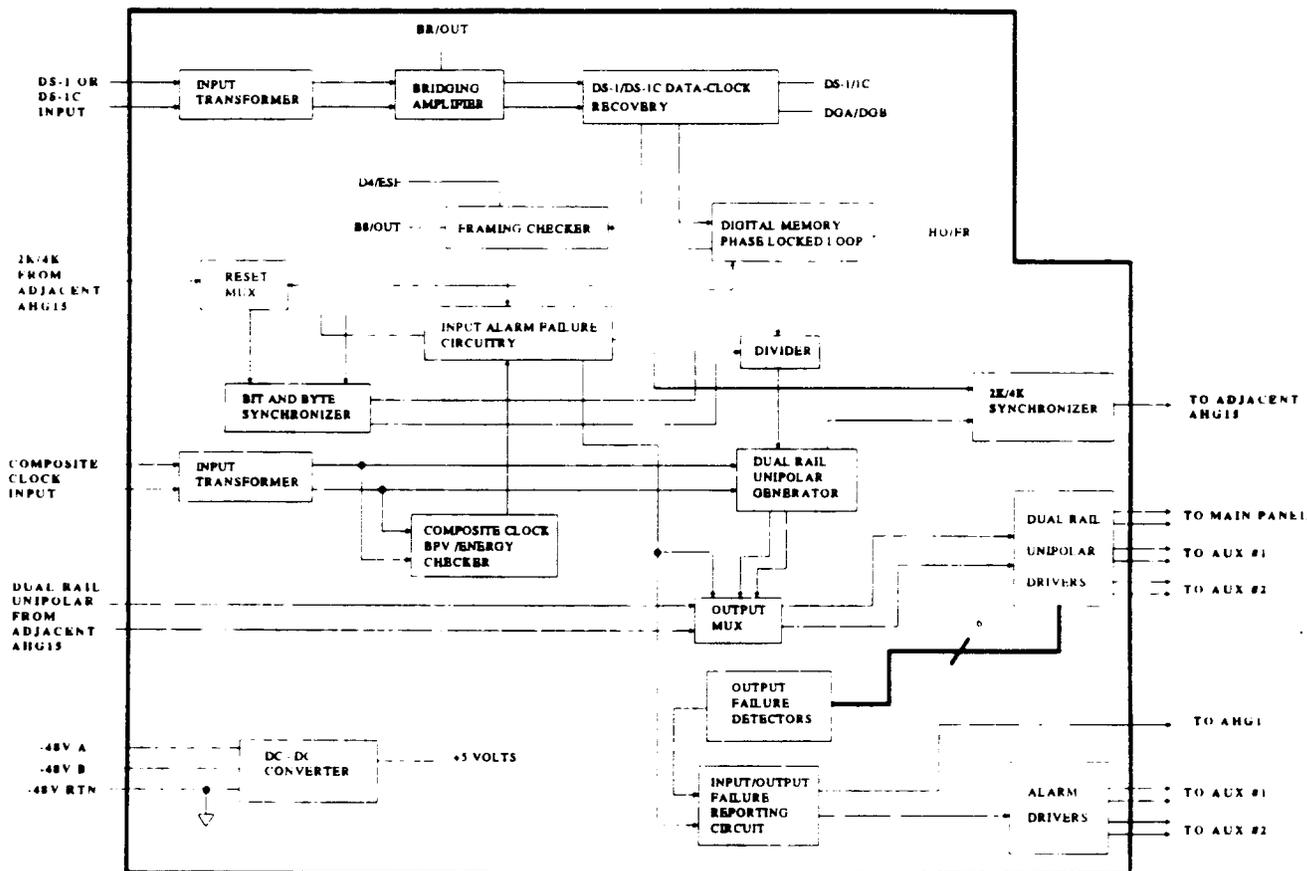


Fig. 11 - Block Diagram of AHG15 Timing Interface

4.21 Upon loss of both inputs to the SDE the AHG15 allows the SDE to enter either a holdover or free-run mode of operation. The holdover mode is for use with DS-1 and DS-1C inputs. The holdover mode sets the TI's oscillator to the frequency equal to that of the last good input and maintains the frequency to within Stratum III accuracy. When at least one of the inputs is restored, the oscillator will lock to the frequency of the restored input and use this to generate the output signals for the SDE. The free-run mode is for use with a composite clock (CC) input or with no input. If both CC inputs fail or the bipolar violation density changes, the oscillator will enter a free-run mode where the oscillator will select a factory set frequency reference to generate the output timing signals for the SDE. When at least one of the inputs is restored, the oscillator reference is disregarded and the CC input is used.

4.22 Hitless input transfer switching is also incorporated in the AHG15. This allows pair of AHG15 TI's to make automatic or manual input reference switches without causing timing discontinuities. Timing discontinuities can cause data hits by the NEs receiving timing. The hitless switching feature also extends to the recovery switching that takes place when an input is restored after a dual input failure. In this case the SDE input mode would switch from the holdover or free-run mode to synchronize to a good input. The hitless switching feature ensures that the SDE will generate error free timing signals during most trouble conditions.

4.23 The AHG15 also has the capability of driving two auxiliary SDE panels. The auxiliary panels contains only a TA and up to four TD circuit packs. The AHG15 has two pairs of dedicated output taps (one pair for each auxiliary panel) which are cabled via the backplane pins on each panel. Both power and alarms for the auxiliary panel is separate to preserve redundancy.

#### E. AHG15 TI OPTIONS

4.24 The AHG15 has three classes of options: those that control the input bridging capability, those which affect input recovery and those for use in input failure conditions.

4.25 The normal AHG15 DS-1 termination is 100 ohms. A working DS-1 line may only have a single 100 ohm termination. When it is desired to have AHG15 be this single termination, set SW101 (fig. 12) to the NORM position. If, however, timing information is to be extracted from a working, terminated DS-1 line, the input bridging option should be used. The bridging option allows the input impedance, presented by the AHG15 and bridging resistors, to be approximately 1000 ohms. This allows the TI to accept the lower input signal level. The bridging option is selected by setting SW101 to the BR position and using two external 432 ohm bridging resistors. The bridging resistors are physically wire-wrapped to the appropriate DS-1 tip and ring terminals on located at the DS-X. Care should be taken to keep unshielded wires a short as possible.

4.26 The options used to modify the input recovery include the input type (DS-1 or DS-1C), input framing format (D4 or ESF), B8ZS coding (IN or OUT) and the choice of di-group timing if DS-1C inputs are used (DGA or DGB). These input options are selected by a four position DIP switch (SW101) (fig. 12). Position 1 controls the input signal type. The OPEN setting is for DS-1C inputs and the other setting is for DS-1 inputs. Position 2 controls the input framing format that is to be detected. The OPEN setting is for ESF framing and the other setting is for D4 framing. Position 3 is for accepting inputs with B8ZS coding. The OPEN setting is for inputs with B8ZS coding and the other setting is for inputs without B8ZS coding. Position 4 is for which di-group in a DS-1C input will be used for timing. The OPEN setting is for di-group B and the other setting is for di-group A.

4.27 The other set of options controls the oscillator mode in case there is a dual-input failure. There are two modes to choose from: holdover and free-run. The holdover and free-run options may be selected by a two position slide switch (SW103). The HO position selects the holdover mode and the FR setting selects the free-run mode.

4.28 The AHG15 is compatible with all SDE panel vintages (J98726W-1, J98726W-2, J98726Y-1) without any additional wiring changes. The AHG15 is not compatible with any other vintages of TI's

and must be used in pairs.

5. TIMING DISTRIBUTOR CIRCUIT PACKS

A. AHG3 TD

5.01 The TD receives the dual-rail unipolar signals from the TIs and converts them to ten composite clock output signals (fig. 13). Up to four TDs may be plugged into positions in the SDE shelf to provide modular growth of composite clock outputs in steps of 10 to a maximum of 40. The outputs of the two TIs each connect to all four TD positions.

When an SDE is first energized, each TD may select the outputs from either TI A or B if both are functioning properly. Timing information from only one of the two input synchronization sources is processed at a given time in the TIs and passed on to the TDs. When desired, the nonlocking switch TR IN SCE (transfer input source) on one of the TIs is operated to effect an input-source selection change. Another nonlocking switch, TR OUT (transfer output), is operated on one of the TIs to cause all TDs to select signals from one particular TI. Only the AHG2 and AHG2B TIs have the TR OUT switch.

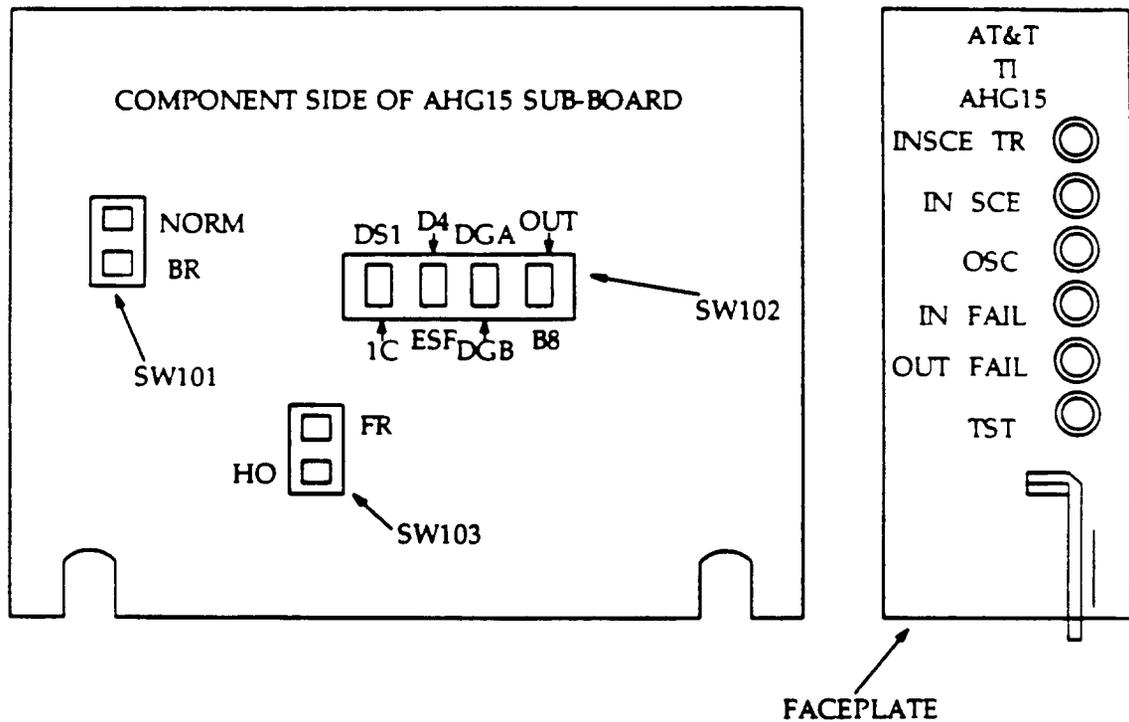


Fig. 12 - Location of Options on the Timing Interface AHG15

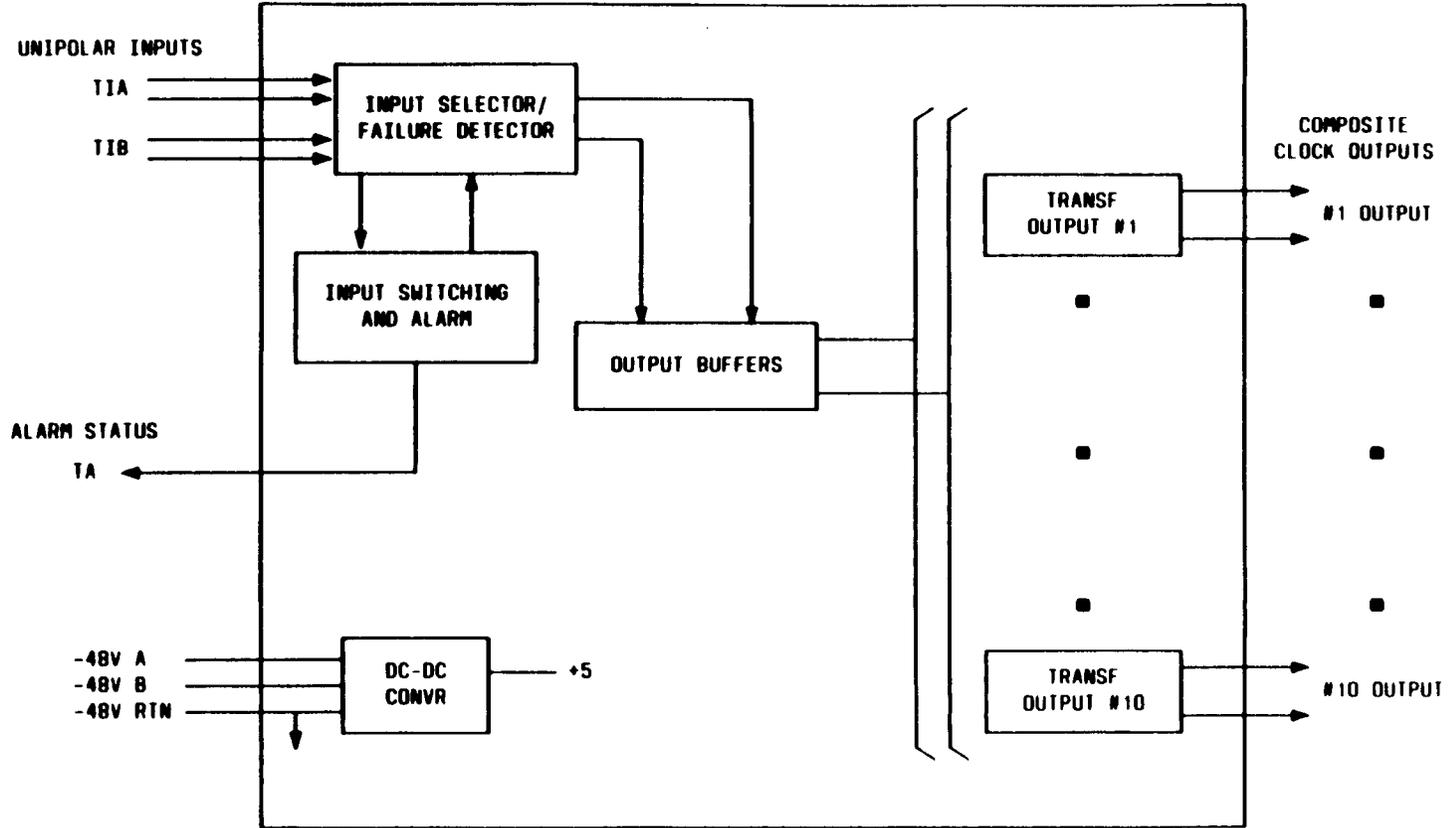


Fig. 13 - Block Diagram of Timing Distributor (AHG3)

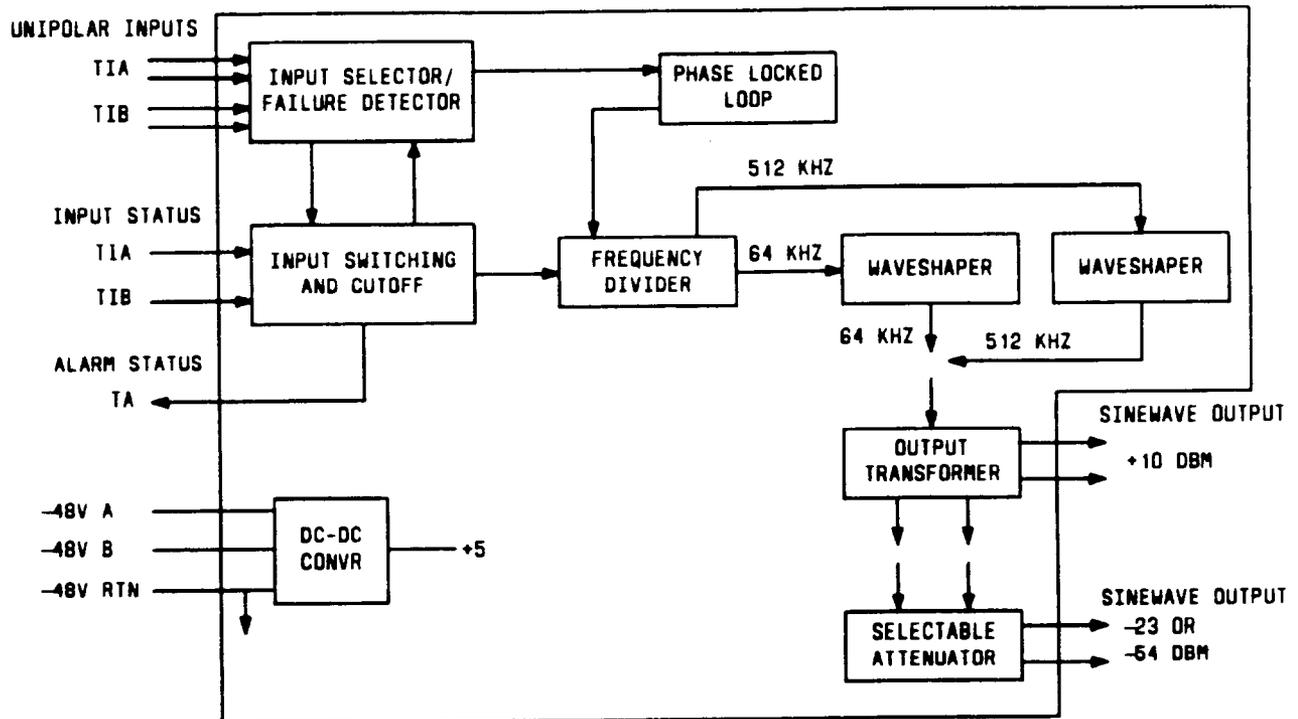


Fig. 14 - Block Diagram of Timing Distributor (AHG4)

## B. AHG4 TD

5.02 The AHG4 timing distributor circuit pack receives dual-rail unipolar signals from the TIs and converts them to a single sine wave output capable of synchronizing the J68857AC primary frequency supply (PFS). The sine wave output is selectable between 64 and 512 kHz frequencies. In addition, the output level is selectable between +10, -23, and -54 dBm. The AHG4 is compatible with all existing backplane connections on the J98726W-1, J98726W-2, and J98726Y-1 panels and is intended to be used in TD slot 4.

5.03 Under normal operating conditions, the AHG4 will supply an output timing signal proportional in frequency to the input of the SDE (fig. 14). The output of the AHG4 will be influenced by both input source and output transfers of the SDE. In the event of a dual-input failure of the SDE, the outputs of the AHG4 would be disabled as indicated by the red LED on the faceplate of the AHG4. Upon restoration of at least one of the inputs to the SDE, the output of the AHG4 would be enabled. When the AHG4 is first inserted into the SDE panel, the red LED will light, indicating that the output is being disabled until the circuitry can synchronize to the input timing signal. After a period of 2 seconds,

the LED will extinguish and the output will enable.

### C. AHG4 TD OPTIONS

5.04 Provisioning the AHG4 for output frequency is done by selecting the proper position of the plug and jack assembly labeled 64 and 512 kHz (fig. 15).

5.05 Provisioning the AHG4 for output level may be done in one of two ways. Typically the output from the AHG4 will come from the attenuated output. The attenuated output has two settings selected by the DIP switch.

- (a) Positions 1 and 2 on the DIP switch need to be set to the ATTEN position. If the 64 kHz frequency is selected, then the -54 dBm output level should be used. The -54 dBm level is selected by setting the DIP switch positions 5 and 6 to the -54 dB position. If the 512 kHz frequency is selected, then the -23 dBm output level should be used.
- (b) The -23 dBm level is selected by setting DIP switch positions 5 and 6 to the -23 dBm position. The attenuated outputs are accessed from TD slot 4 backplane terminals 20 (tip), 47 (ring), and 22 (shield). These signals are carried via a twisted triple to terminals E20, F20, and D20 (respectively) located on SDE B terminal block. Cabling between the SDE and PFS may be done with a 22-gauge twisted, shielded cable.

5.06 If the office environment is noisy so that the low level signals required to synchronize the PFS may not be transmitted from the SDE without interference, then the nonattenuated output provides a sine wave output at a +10 dBm level and may be selected by setting DIP switch positions 1 and 2 to the +10 dB setting. This signal may be accessed at TD slot 4 backplane terminals 21 (tip), 48 (ring), and 22 (shield) via a twisted triple to terminals E20, F20, and D20 on the SDE terminal blocks. Cabling between the SDE and the PFS would require that an external attenuator be placed near the PFS to supply the proper input signal level. A 22 gauge twisted, shielded cable would be used from the SDE to the PFS with a maximum length of 1000 feet.

5.07 Additional backplane wiring is necessary in order to use the AHG4 with the J98726W-1 and J98726W-2,L3 panels. Control wiring is necessary between the timing interface circuit packs and TD slot 4. This wiring shall be 26 gauge (terminal 42 of the TD slot is connected to terminal 16 of TIA, and terminal 43 of the TD slot is connected to terminal 16 of TI B).

### D. AHG5 TD

5.08 The AHG5 TD circuit pack is used in the SDE (J98726W-2 and J98726Y-1) to provide DS-1 level signals for synchronizing digital equipment. The DS-1 signal is an all-ones format with a selectable framing pattern of either D4 or ESF. The TD can be inserted into any TD card slot in any SDE shelf.

5.09 The input to the circuit pack is the standard dual-rail unipolar composite clock (fig. 16) from the backplane as derived by the respective timing interface (TI) circuit pack. The 64 kHz dual-rail signal enters the input selector/failure detector where one of the two input clocks is selected based upon pulse width of the clock. If one of the inputs becomes bad, the input selector will automatically switch to the other input, if not already selected. If both inputs fail, then the output of the TD will cut off and a major alarm will be reported.

5.10 Hysteresis switching is employed upon the restoration of one of the two bad inputs so that the input signal must be good for at least one second before being used as an input. The use of the hysteresis switch prevents false switching and disrupted outputs from the TD. The recovered input signal is then input to a digital phase locked where it is converted into a de-jittered clock of 3.088 MHz. The 3.088 MHz clock is next fed into the DS-1 framing generator where the selected framing format is placed on the all ones DS-1 signal in the appropriate time slots. The output of the framing generator is a unipolar DS-1 signal which is converted to a bipolar signal by the unipolar/dual rail rate converter. The bipolar DS-1 signal is then fed into the output enable buffer where the DS-1 signal is fanned-out before it enters the output driver stage. The buffer also serves to inhibit the DS-1 signal while operating in the "cut off" mode. Each of the ten output drivers is separate and

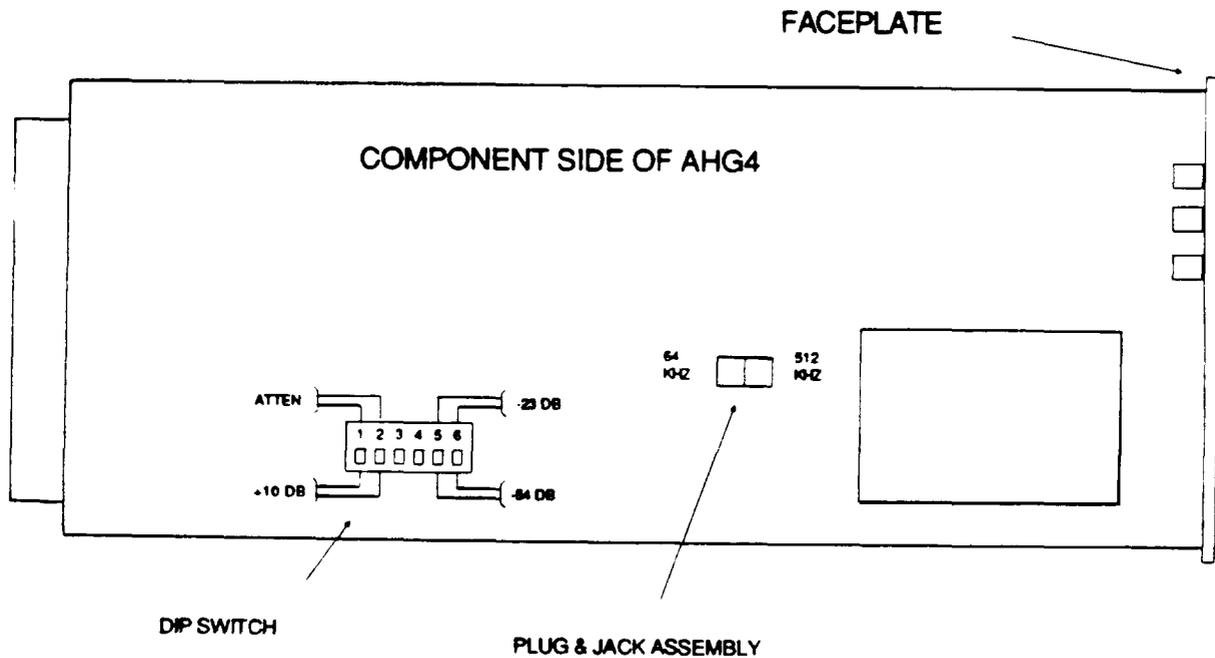
transformer coupled.

5.11 Each DS-1 output is equalized to match the DS-1 template at the DS-X from 0 to 400 feet (Bellcore technical advisory TA-TSY-000378). The maximum distance from the SDE through the DS-X to the far end terminating equipment is 1140 feet (400 + 85 + 655 feet). All outputs are designed to work into a 100 ohm load over 22BF twisted shielded cable. All output signals should be accessed at the SDE A and SDE B terminal blocks directly to reduce the possibility of cross-talk and high frequency emissions. In addition, each unused output should be terminated by a 100 ohm resistor.

**E. AHG5 TD OPTIONS**

5.12 There are two available options on the AHG5 circuit pack. The framing pattern option, mentioned previously, selects a D4 or ESF framing pattern. The

framing pattern is chosen by selecting the proper position of the sub-board switch shown in fig. 17. The switch section labeled "1" is used. The switch in the "D4" position selects the D4 framing format and in the "ESF" position the ESF format is selected. The second option is the "CUTOFF" option which is used when supplying timing signals to equipment of a higher Stratum. The rules for Stratum timing state that equipment may only receive timing from a source of equal or higher Stratum. However, if the "CUTOFF" option is used, then the outputs of the AHG5 will be inhibited if both inputs to the SDE become invalid. In this way, the equipment receiving timing from the SDE will recognize that the input has failed and rely on their own internal clocks for holdover during this outage. Upon restoration of at least one input to the SDE, the outputs of the AHG5 will again be activated and provide a valid output once more.



**Fig. 15 - Location of Options for the AHG4 Timing Distributor**

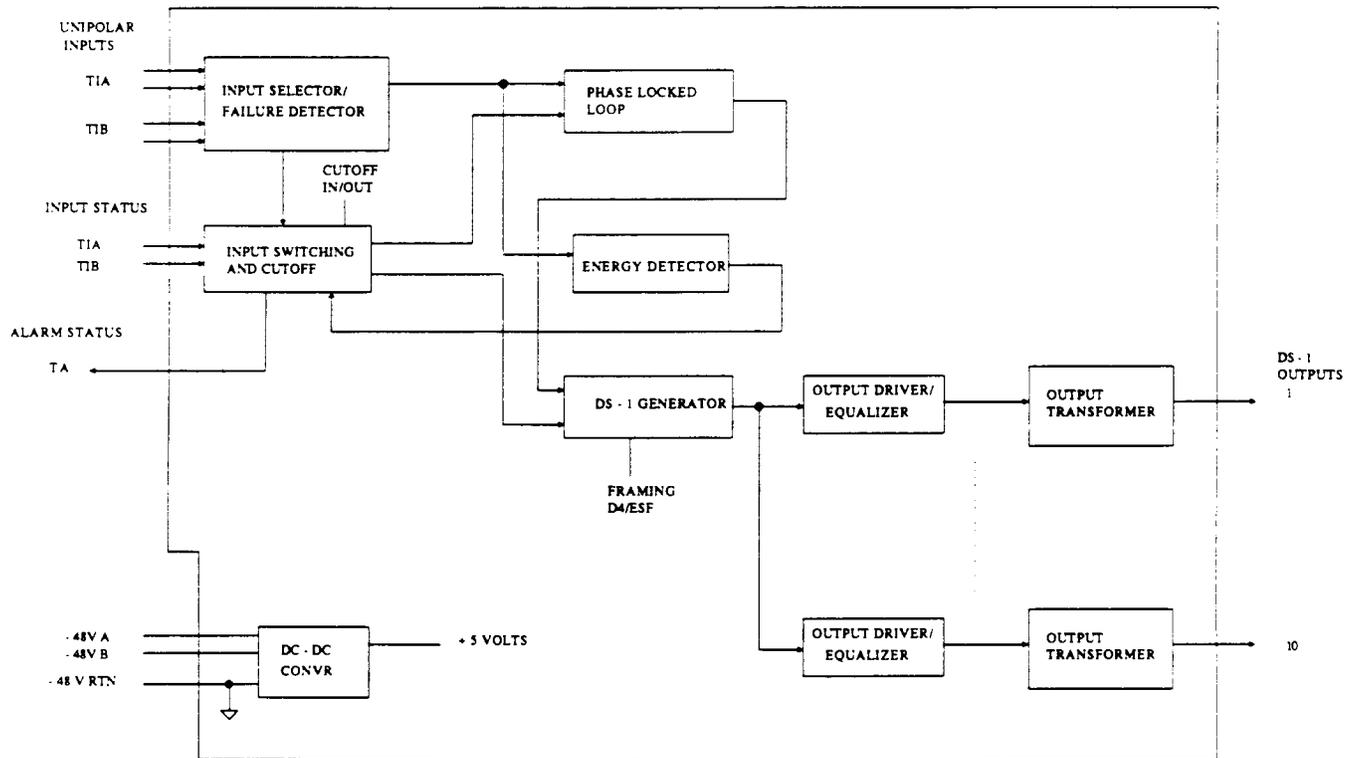


Fig. 16 - Block Diagram of AHG5 Timing Distributor

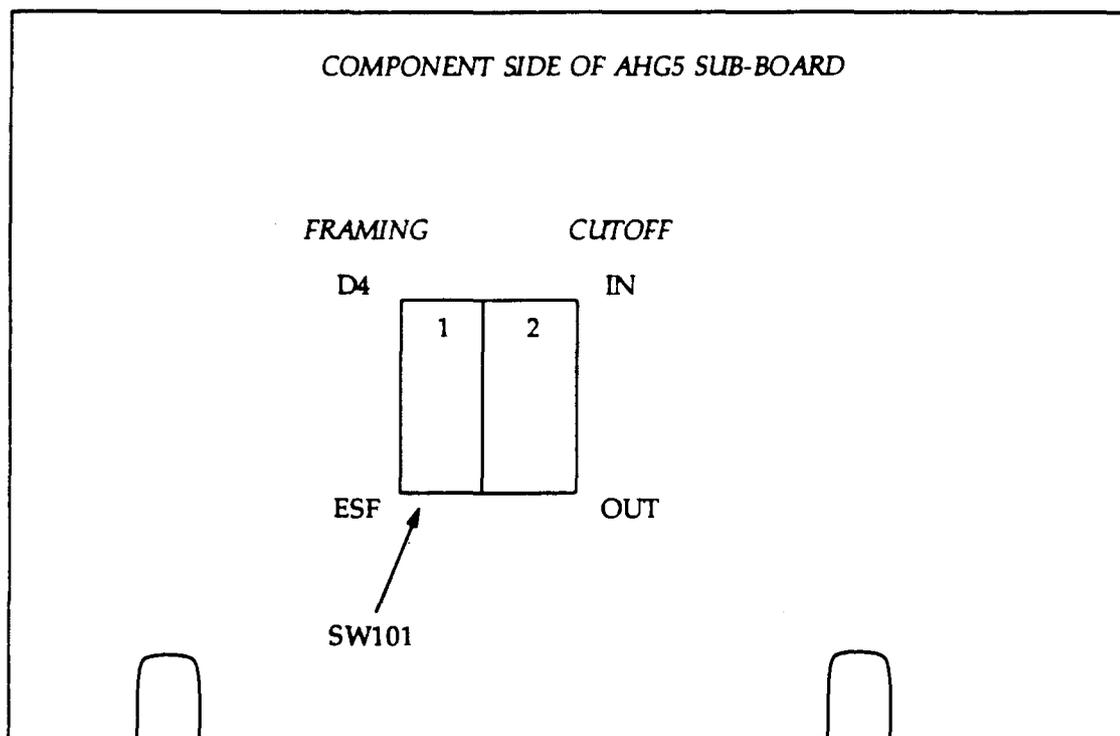


Fig. 17 - Location of Options on the AHG5 Timing Distributor

5.13 If the "CUTOFF" option is not selected then the AHG5 outputs provide a signal as accurate as the inputs from the timing interfaces during a dual input failure. The "CUTOFF" option is selected by choosing the proper position of the switch shown in. The portion of the switch labeled "2" is used. The switch in the "IN" position selects the "CUTOFF" option and in the "OUT" position, inhibits the "CUTOFF" option. Control wiring from the timing interface circuit packs is necessary in order to use the "CUTOFF" option.

5.14 Before the AHG5 may be inserted into the SDE shelf, the proper options must be set as described in the above section. If the "CUTOFF" option is chosen, care must be exercised in installing the necessary backplane wiring (J98726W-2 L3 only) as service may experience minor disruption. Once

the options are set, the AHG5 may be inserted in any primary TD slot (1, 2, 3, 4). Two additional operations must be performed:

- 1 All unused AHG5 outputs must be terminated with a 100 ohm resistor across tip and ring at the appropriate SDE terminal block location.
- 2 A series of grounding wires shall be added connecting the shield row on the SDE terminal blocks to frame ground (J98726W-2 L3 only). These wires are attached to frame ground via the backplane screws with wire-wrap lugs.

5.15 Ensuring output-signal redundancy is most easily done on equipment requiring multiple DS-1 input timing signals. The DS-1 timing signals should be taken from more than one AHG5 located in any TD slot. This arrangement ensures that one

AHG5 may be removed at a time without disrupting service to the equipment receiving timing.

5.16 The AHG5 is intended to be replaced by simply removing the desired circuit pack and inserting the replacement AHG5 in the same slot. The parallel changeover system (PCS) is not intended for AHG5 change out and therefore the adjacent TD\_S slots should not be used in the J98726W-2 panel.

#### F. AHG25 TD

5.17 The AHG25 timing distributor (TD) circuit pack is used in the SDE (J98726W-2 and J98726Y-1) to provide DS-1 level signals for synchronizing digital equipment. The DS-1 signal is an all-ones format with a selectable framing pattern of either D4 or ESF. The TD can be inserted into any timing distributor card slot in any SDE shelf. The AHG25 is also capable of providing phase coherent output signals when used in a CDU.

5.18 The input to the circuit pack is the standard dual-rail unipolar composite clock on the backplane as derived by the respective timing interface (TI) circuit pack (fig. 18). The 64 kHz dual-rail signal enters the input selector/failure detector where one of the two input clocks is selected based upon pulse width of the clock. If one of the inputs becomes bad, the input selector will automatically switch to the other input, if not already selected. If both inputs fail, then the output of the TD will cut off and a major alarm will be reported.

5.19 Hysteresis switching is employed upon the restoration of one of the two bad inputs so that the input signal must be good for at least one second before being used as an input. The use of the hysteresis switch prevents false switching and disrupted outputs from the TD. The recovered input signal is then sent to an edge-triggered digital phase-locked loop where it is converted into a de-jittered clock of 3.088 MHz. The 3.088 MHz clock is next fed into the DS-1 framing generator where the selected framing format is placed on the all ones DS-1 signal in the appropriate time slots. The output of the framing generator is a unipolar DS-1 signal which is converted to a bipolar signal by the unipolar/dual rail rate converter. The bipolar DS-1

signal is then fed into the output enable buffer where the DS-1 signal is fanned-out before it enters the output driver stage. The buffer also serves to inhibit the DS-1 signal while operating in the "CUTOFF" mode.

5.20 Each of the ten output drivers is separate and transformer coupled. Each output is equalized to match the DS-1 template at the DS-X from 0 to 400 feet (Bellcore technical advisory TA-TSY-000378). The maximum distance from the SDE through the DS-X to the far end terminating equipment is 1140 feet (400 + 85 + 655 feet).

5.21 All outputs are designed to work into a 100 ohm load over 22BF twisted shielded cable. All output signals should be accessed at the SDE A and SDE B terminal blocks directly to reduce the possibility of crosstalk and high frequency emissions. In addition, each unused output should be terminated by a 100 ohm resistor.

#### G. AHG25 TD OPTIONS

5.22 There are two available options on the AHG25 circuit pack. The framing pattern option, mentioned previously, selects a D4 or ESF framing pattern. The framing pattern is chosen by selecting the proper position the switch. The switch section labeled "1" is used. The switch in the "D4" position selects the D4 framing format and in the "ESF" position the ESF format is selected.

5.23 The second option is the "CUTOFF" option which is used when supplying timing signals to equipment of a higher Stratum. The rules for Stratum timing state that equipment may only receive timing from a source of equal or higher Stratum. However, if the "CUTOFF" option is used, then the outputs of the AHG25 will be inhibited if both inputs to the SDE become invalid. In this way, the equipment receiving timing from the SDE will recognize that the input has failed and rely on their own internal clocks for holdover during this outage. Upon restoration of at least one input to the SDE, the outputs of the AHG25 will again be activated and provide a valid output once more. If the "CUTOFF" option is not selected then the AHG25 outputs provide a signal as accurate as the inputs from the timing interfaces during a dual input

failure.

5.24 The "CUTOFF" option is selected by choosing the proper position of the sub-board switch (fig. 19). The portion of the switch labeled "2" is used. The switch in the "IN" position selects the "CUTOFF" option and in the "OUT" position, inhibits the "CUTOFF" option. Control wiring from the timing interface circuit packs is necessary in order to use the "CUTOFF" option. This wiring is necessary for the J98726W-2.

5.25 Before the AHG25 may be inserted into the SDE shelf, the proper options must be set as described in the above section. If the "CUTOFF" option is chosen, care must be exercised in installing the necessary backplane wiring as service may experience minor disruption. Once the options are set, the AHG25 may be inserted in any primary TD slot (1, 2, 3, 4). Two additional operations must be performed:

- 1 All unused AHG25 outputs must be terminated with a 100 ohm resistor across tip and ring at the appropriate SDE terminal block location.
- 2 A series of grounding wires shall be added connecting the shield row on the SDE terminal blocks to frame ground on the J98726W-2 panel only. These wires are attached to frame ground via the backplane screws with wire-wrap lugs.

5.26 Ensuring output signal redundancy is most easily done in equipment requiring multiple DS-1 input timing signals. The DS-1 timing signals should be taken from more than one AHG25 located

in any TD slot. This arrangement ensures that one AHG25 may be removed at a time without disrupting service to the equipment receiving timing.

5.27 The AHG25 is intended to be replaced by simply removing the desired circuit pack and inserting the replacement AHG25 in the same slot. The parallel changeover system (PCS) is not intended for AHG25 change-out and therefore the adjacent TD\_S slots should not be used in the J98726W-2 panel.

#### H. AHG26 TD

5.28 The Timing Distributor (TD) plug-in unit, AHG26, is used in the SDE to provide a 2.048 MHz sine wave output. The output provides a -20 dBm or -35 dBm level into 75 ohms to network elements (NE) requiring this input. The TD is intended to be used in the translation of synchronization from the Digital to Analog communications networks.

5.29 The input signal to the TD is a dual-rail unipolar composite clock signal received from the TI (timing interface) plug-in units (fig. 20). This signal is recovered and the signal quality is monitored by single-rail failure detectors. A 64 KHz square wave is derived from the input and then multiplied by a phase locked loop (PLL) to a frequency of 4.096 MHz. The PLL employs a phase coherent phase detector that aligns the edges of the input 64 KHz with the 4.096 MHz output. The PLL also incorporates a slip detector that monitors the phase error between the input and output frequencies of the phase detector. If this error is greater than three cycles of 4.096 MHz, a slip is registered.

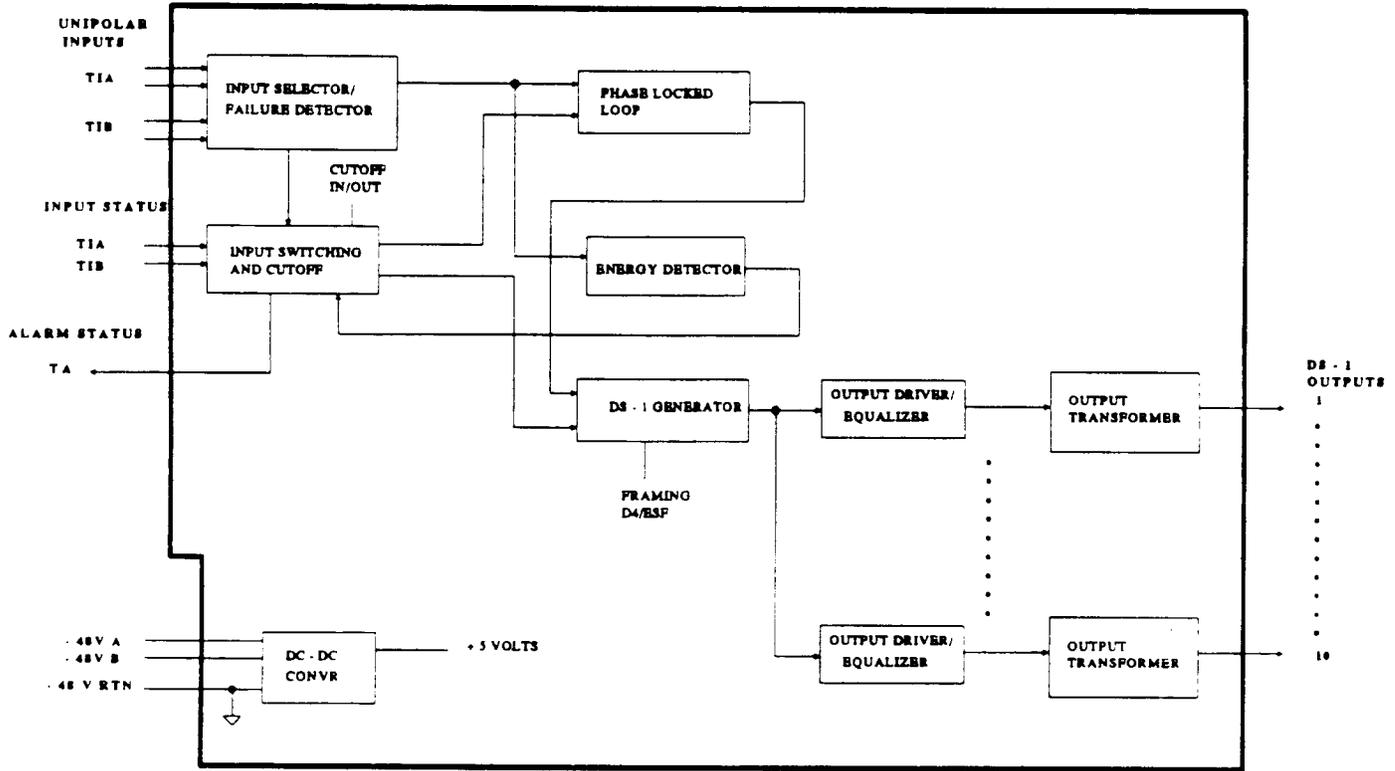
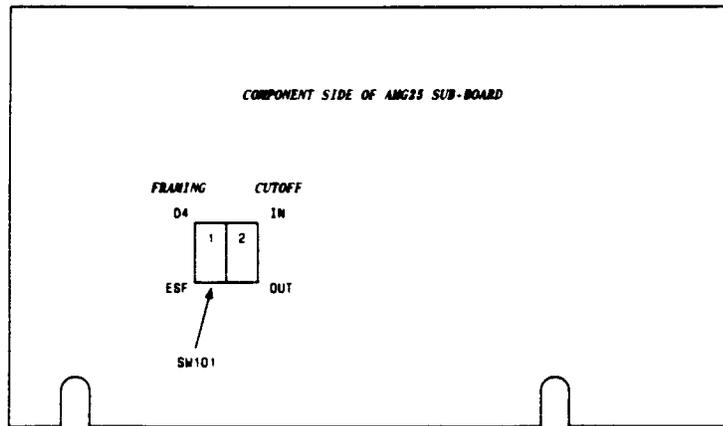


Fig. 18 - Block Diagram of AHG25 Timing Distributor



NOTE: "CUTOFF" SHOULD ALWAYS BE IN THE "IN" POSITION

Fig. 19 - Location of Options on the AHG25 Timing Distributor

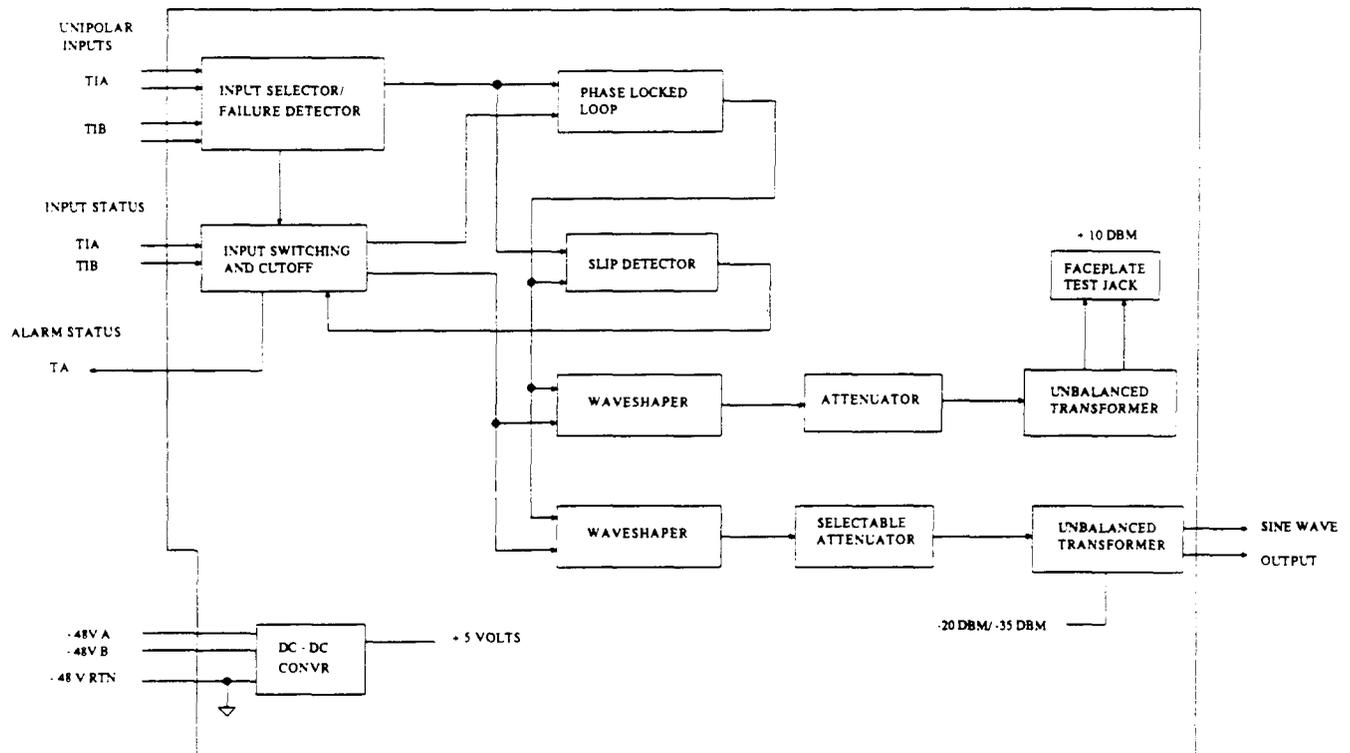


Fig. 20 - Block Diagram of the AHG26 Timing Distributor

5.30 The 4.096 MHz is divided by two to produce the 2.048 MHz base frequency. This frequency is next input to a Class A wave shaper/amplifier that produces the sine wave shape. This signal is fed into an unbalanced output transformer which is impedance matched for a 75 ohm load. Lastly the signal is input to a settable attenuator that allows either a -20 dBm or -35 dBm output level to be output from the TD.

5.31 A faceplate Bantam test jack provides an access port to evaluate the 2.048 MHz sine wave frequency. The test port is separate and buffered from the main output. The test port level is +10 dBm +/- 1 dBm into 75 ohms unbalanced

5.32 The TD also employs an output "cut off" feature. In the event of a dual-TI input failure, the

TD disables its outputs and allows the synchronized equipment to enter a holdover mode at its prescribed Stratum level.

5.33 There are three LED indicators on the TDs faceplate. Two of these indicators (TI OUTPUT IN USE) are green and are used to signify which input source is being used to derive timing (TI A or TI B). If there is a cut off alarm, these LEDs are inhibited as this alarm state prevents any inputs from being used. The last of the LED indicators is the red CUT OFF LED which is used to signify the loss of input, loss of lock, or the external "cut off" command.

#### I. AHG26 TD OPTIONS

5.34 The selection of the output level is the only TD option. The two output levels are -20 dBm and -35 dBm. The two levels are set by a slide switch located at the bottom left of the circuit pack (fig. 21).

5.35 The TD is intended to be used in non-redundant applications and need not be used in pairs. When used in the SDE, the TD is normally placed in slot TD-1 (side A) or slot TD-4 (side B). If, however, there are to be other non-redundant circuit packs used in the panel (i.e., AHG4) then slots TD-1, TD-2, TD-3, or TD-4 may be used.

5.36 An output cable must be run between the TD and the SDE terminal blocks. The cable will be a twisted pair with three twists per inch. The wiring assignments are given per TD slot assignment. Coaxial cable is used to cable from the SDE() terminal blocks to the designated NE. A 728A or equivalent coaxial cable is recommended.

6. TIMING ALARM CIRCUIT PACK

A. ALARMS, AHG1 TA, FUSE AND ALARM PANEL

6.01 The TA receives alarm status information from the TIs and the TDs. The alarm information is stored in a register and visually displayed on the TA faceplate by a series of yellow and red LEDs (fig. 22). The major and minor alarm status associated with the red and yellow LEDs, respectively, are described in Table A. The TAs storage register may be only cleared by the MEM button located on the TA faceplate.

TABLE A

Alarm Responses in the SDE

Timing or Energy Source	Failed Unit	Alarm Sensor Location	OFF ALM & STATUS	ACO	Lamp/LED Location		Backup
					Fuse Panel	TA	
OTS A or DS-1** A	TI A	TI A	MN	Audible	MN	TI A	TI B
OTS B or DS-1** B	TI B	TI B	MN	Audible	MN	TI B	TI A
OTS A & B or DS-1** A & B	TI A and TI B	TDs A, B, C, and D	MJ	Audible	MJ	TI A and TI B	None for AHG2/10; OSC for AHG2B
TI A & B	TD 1	TD 1	MJ	Audible	MJ	TD 1	None
TI A & B	TD 2	TD 2	MJ	Audible	MJ	TD 2	None
TI A & B	TD 3	TD 3	MJ	Audible	MJ	TD 3	None
TI A & B	TD 4	TD 4	MJ	Audible	MJ	TD 4	None
-48ABS	Fuse F1	Fuse panel	MJ		MJ, FA	None	None
-48ABS	-48ABS	Fuse panel	MJ, MN	None	None	None	None
-48A	Fuse F2 or -48A	Fuse panel	MJ	Audible*	MJ, FA	None	F3 (-48B)
-48B	Fuse F3 or -48B	Fuse panel	MJ	Audible*	MJ, FA	None	F2 (-48A)

\* For J98726W-2; otherwise none.

\*\* Or DS-1C.

6.02 There are three settable options (fig. 23) on the faceplate of the TA that allow the alarm information from up to three unequipped TD slots to cut off. These options would be used when operating less than one TD is needed for basic SDE operation. These options are selected by inserting the appropriate plug into the vertical series of sockets. These sockets are labeled on the right-hand side "IN, IN, IN" and on the left-hand side "2, 3, 4" corresponding to TD 2, TD 3, and TD 4. Below each IN position of the socket is an unlabeled OUT position. To defeat the alarm

information from a particular TD, the option plug is placed in the OUT socket corresponding to the appropriately numbered TD. The IN position may be used as a storage position for the unused option plugs. The alarm information is sent from the TA circuit pack to the fuse and alarm panel. Depending on the class of outage, a normally operated relay, MN or MJ, is then released in the fuse and alarm panel. The MN and MJ relays have contacts that activate the regular audible and visual alarms via contact closures to a telemetry system for remote transmittal.

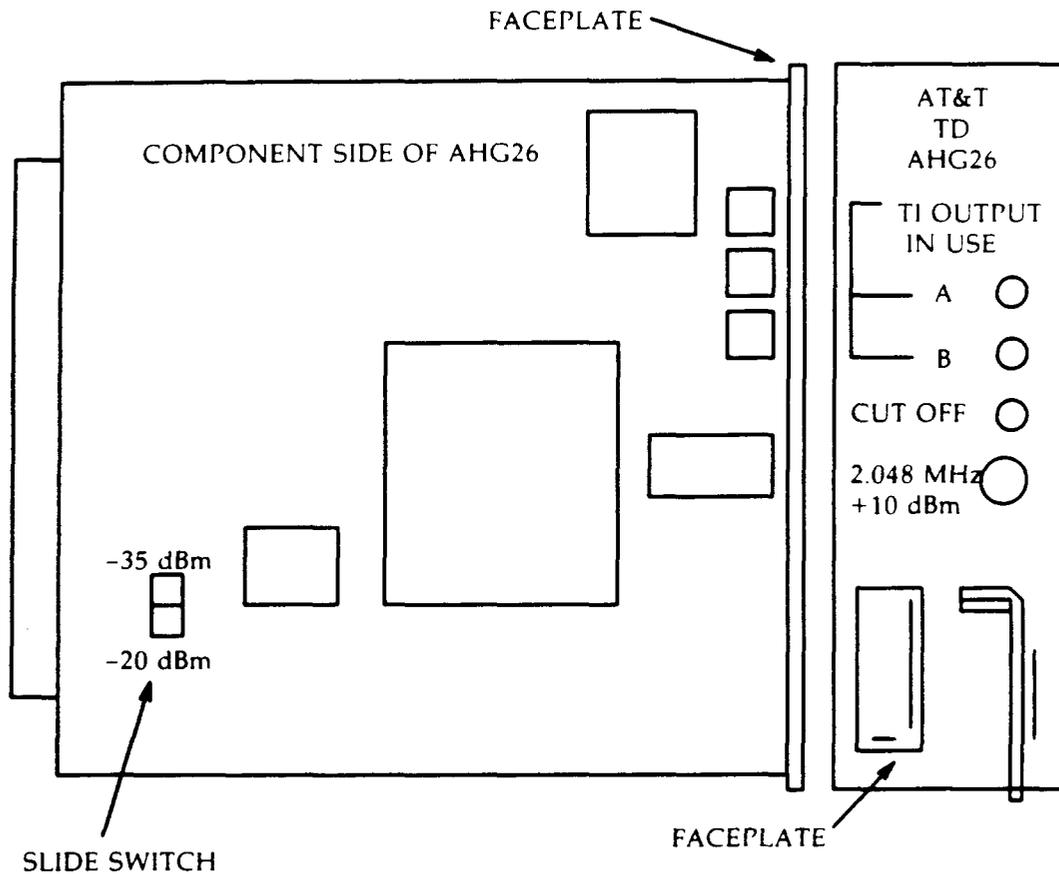


Fig. 21 - Location of Options on the AHG26 Timing Distributor

6.03 Alarm conditions indicated by the fuse and alarm panel include blown fuses and power failure (available on all but the J98726W-1 panel). The occurrence of a blown fuse or loss of power of the -48A and -48B power feeds will cause the FA panel lamp to energize and the (normally operated) MJ relay to release causing a major alarm to be registered. The above events will also happen if the -48ABS has a blown fuse. However, for the case of the -48ABS power feed failing, the FA lamp will not energize. Alarm conditions are registered by the fuse and alarm panel by audible, visual, and status reporting alarms. The audible alarms may be silenced by either depressing the ACO locking switch on the fuse and alarm panel so that it illuminates or by a designated contact closure from a telemetry system. The alarm condition may only be cleared by removing the source of the alarm. Once this has been accomplished, the locking ACO switch, if previously used, shall be depressed a second

time to disengage the ACO mode indicated by the extinguished illumination of the switch. A fault condition registration cannot be released from the memory in the TA until the fault is cleared. The registration is released in the TA by pressing the nonlocking key MEM. Upon successful release, the lighted LED on the TA faceplate darkens.

6.04 Table A summarizes the locations and classes of alarm indications that appear for different types of SDE malfunctions. The term STATUS in the fourth column refers to the relay contacts that connect to a telemetry system for transmitting the alarm information to a remote location.

**B. SIGNAL OUTPUT CONNECTIONS**

6.05 Terminal blocks SDE A, SDE B, BK A (block A), and BK B (block B) are provided as part of the

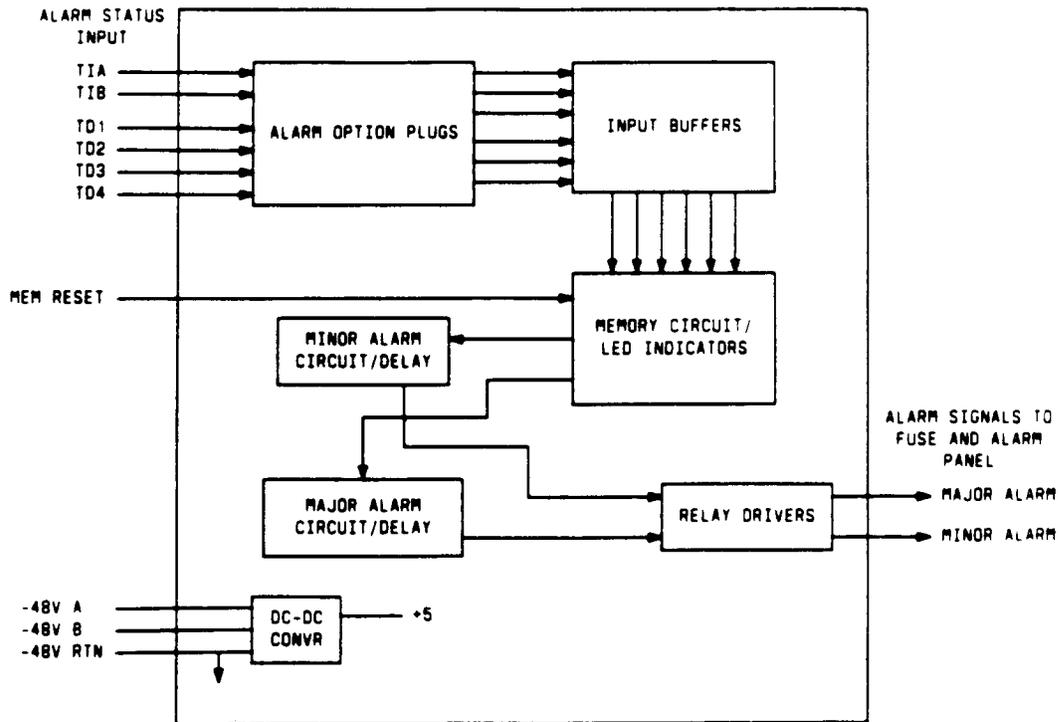


Fig. 22 - Block Diagram of Timing Alarm (AHG1)

SDE for implementing connections between SDE outputs and Network elements requiring synchronization. These terminal blocks may be used either as direct connections or cross connections.

6.06 The direct connect option allows SDE output assignments to be made directly from the SDE A and SDE B terminal blocks to terminal bays. With this wiring option 40 different output assignments of SDE outputs and bays exist. All TD circuit packs may use this option.

6.07 The cross-connect option allows the use of cross-connections between the SDE terminal blocks and BK terminal blocks. This option will yield up to

80 different output assignments with up to 40 fed from the SDE. The AHG3 TD circuit pack may only use this option.

### C. POWER

6.08 The SDE is energized entirely from three redundant -48 volt office battery feeds. Duplicate individually fused feeders run between a nearby miscellaneous fuse panel and the SDE. Within the SDE, duplicate fuse protected paths run to a steering diode arrangement in each plug-in unit. If one path has an outage, the steering diode in the good path carries the operating current. A small dc to dc power converter in each plug-in unit supplies 5 volts for operation of the integrated circuits.

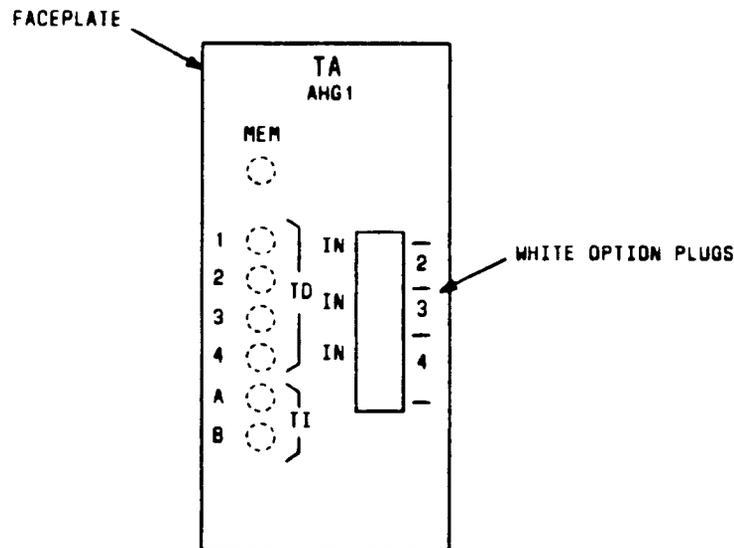


Fig. 23 - Location of Options for the AHG1 Timing Alarm

#### D. PCS (PARALLEL CHANGEOVER SYSTEM)

6.09 The PCS provides a means for removing AHG3 TD(s) from an in-service SDE without disruption of service. Adjacent to each TD is a parallel wired card connector slot that is normally empty. In the event of a failure of one or more output circuits of a single TD, a known working TD may be plugged into the appropriate adjacent TD slot and the failed TD removed. The transfer is initiated by depressing and holding the TR OUT switch located on that TI corresponding to the nonlighted TI OUTPUT IN USE LED on the TD to be changed over. The spare TD is then plugged into the right adjacent TD slot, and the bad TD is removed. Lastly, the replacement TD is inserted into the TD position, and the TR OUT switch is released. Since the input, output, alarm, and power connections are paralleled, there will be no disruption of the good output(s) of the TD, and the formerly bad output(s) if simply TD related will be restored. PCS is available on those SDE panel assemblies labeled J98726W-2 and J98726Y-1.

6.10 If multiple changeovers must be made to a single SDE, the TD(s) should be removed in consecutive order to ease the required battery current.

6.11 The changed-over TD may remain in the adjacent card slot for an indefinite period of time. The above changeover procedure may be performed in reverse to locate a TD back into the primary TD slot.

#### E. AUXILIARY SDE PANEL EXPANSION

6.12 Auxiliary panel expansion allows the output capability of an existing, or main, SDE panel to be increased by a factor of two or three. The auxiliary panel may be either a J98726W-1, J98726W-2, or J98726Y-1 panel with one AHG1 TA circuit pack and up to four TD circuit packs depending upon the number of outputs desired. The auxiliary panel receives its timing information directly from the TI

circuit pack on the main panel. Because the timing signals are fed directly from the TI circuit packs, there is not an additional 300 foot through-put delay (450 ns) for the auxiliary panel as would be the case for a tandem arrangement. The power and alarm connections for the auxiliary panel are separate from the main panel and are wired directly to the auxiliary panel.

6.13 Two auxiliary panel arrangements exist depending upon which pair of TIs is used. The AHG2B TIs can supply timing signals to only a single auxiliary panel. This auxiliary panel can only support the AHG3 TD. The AHG10 and

AHG15 TIs can supply timing signals up to two auxiliary panels. Each of these auxiliary panels can support any code of TD.

6.14 The wiring between the main and auxiliary panels is identical for all panels. The actual wiring is connected between the backplanes of each panel with two separate twisted, shielded, multipaired cables per auxiliary panel. These cables have a length restriction of 4 feet if the AHG2B TIs are used or 6 feet if the AHG10 or AHG15 TIs are used. In all cases, cable shields are connected at the main panel and left open at the auxiliary end. Detailed wiring information is presented in Table B and fig. 24 (AHG2B expansion) and Table C fig. 25 (AHG10 and AHG15 expansion). The wired connections are made between both TI card slots of the main and auxiliary panels such that the TTL timing signals from NR1, PR1, NR2, and PR2 terminals are fed between the two panels. In addition, the AHG10 and AHG15 have an output provision for alarm signals from each TI in the main panel to be output to each auxiliary panel. This alarm information is registered by the TA in the auxiliary panel as a minor alarm failure on the TIA and TIB LEDs. In addition, minor or major office alarms will be reported as a result of these alarm indications. Failures of the TIs on the main panel will be registered on the auxiliary panels as if the auxiliary panels contained TIs.

TABLE B				
Cabling Connections for AHG2B Auxiliary Panel				
From Main Panel		To Auxiliary Panel 1 (Note 3)		
Connector	Terminals	Connector	Terminals	Cable
J2 (TI A)	2	J1 (TA)	2	A
J2 (TI A)	3	J2 (TI A)	3	A
J2 (TI A)	29	J2 (TI A)	29	A
J2 (TI A)	30	J2 (TI A)	30	A
J3 (TI B)	2	J3 (TI B)	2	B
J3 (TI B)	3	J3 (TI B)	3	B
J3 (TI B)	29	J3 (TI B)	29	B
J3 (TI B)	30	J3 (TI B)	30	B
Auxiliary Panel Jumpers (Note 4)				
Connector		From Terminal		To Terminal
J2 (TI A)		16		22
J3 (TI B)		16		22
<p><b>Note 1:</b> Each twisted shielded pair consists of two 26-gauge wires:P1 and P2. The P1 connections are given in this table. All of the P2 connections are tied to the frame ground on each panel. Any unused wires should also be tied to the frame ground at both ends.</p> <p><b>Note 2:</b> The shield connection is tied to the frame ground on the main panel, but not connected on the auxiliary panel.</p> <p><b>Note 3:</b> The maximum overall cable length for each auxiliary panel should not exceed 4 feet.</p> <p><b>Note 4:</b> All jumper wires should be 26-gauge wire.</p>				

TABLE B - Cabling Connections for AHG2B Auxiliary Panel

TABLE C				
Cabling Connections for AHG10 and AHG15 Auxiliary Panels				
From Main Panel		To Auxiliary Panel 1 (Note 3)		
Connector	Terminals	Connector	Terminals	Cable
J2 (TI A)	15	J1 (TA)	2	A1
J2 (TI A)	7	J2 (TI A)	2, 3	A1
J2 (TI A)	34	J2 (TI A)	29, 30	A1
J3 (TI B)	15	J1 (TA)	3	A2
J3 (TI B)	7	J3 (TI B)	2, 3	A2
J3 (TI B)	34	J3 (TI B)	29, 30	A2
From Main Panel		To Auxiliary Panel 2 (Note 3)		
Connector	Terminals	Connector	Terminals	Cable
J2 (TI A)	42	J1 (TA)	2	B1
J2 (TI A)	8	J2 (TI A)	2, 3	B1
J2 (TI A)	35	J2 (TI A)	29, 30	B1
J3 (TA)	42	J1 (TA)	3	B2
J3 (TI B)	8	J3 (TI B)	2, 3	B2
J3 (TI B)	35	J3 (TI B)	29, 30	B2
<p><b>Note 1:</b> Each twisted shielded pair consists of two 26-gauge wires: P1 and P2. The P1 connections are given in this table. All of the P2 connections are tied to frame ground on each panel. Any unused wires should also be tied to frame ground at both ends.</p> <p><b>Note 2:</b> The shield connection is tied to frame ground on the main panel, but not connected on the auxiliary panel.</p> <p><b>Note 3:</b> The maximum overall cable length for each auxiliary panel should not exceed 6 feet.</p>				

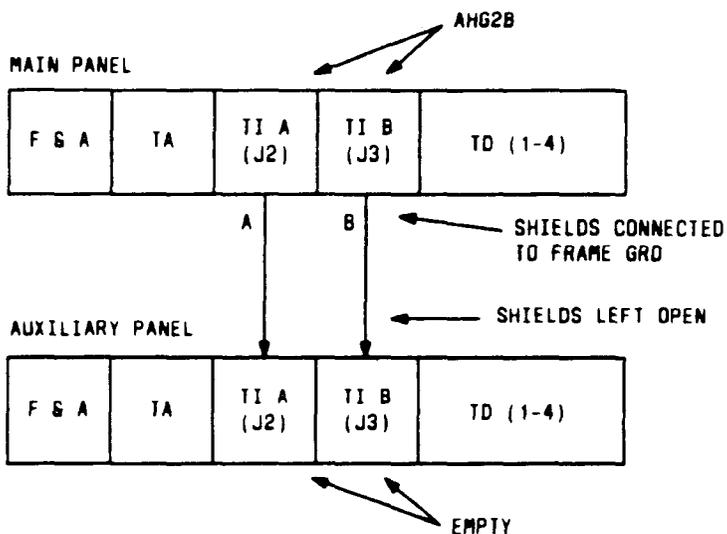


Fig. 24 - Cabling Diagram:Wiring Between Main & Aux Panel Using AHG2B

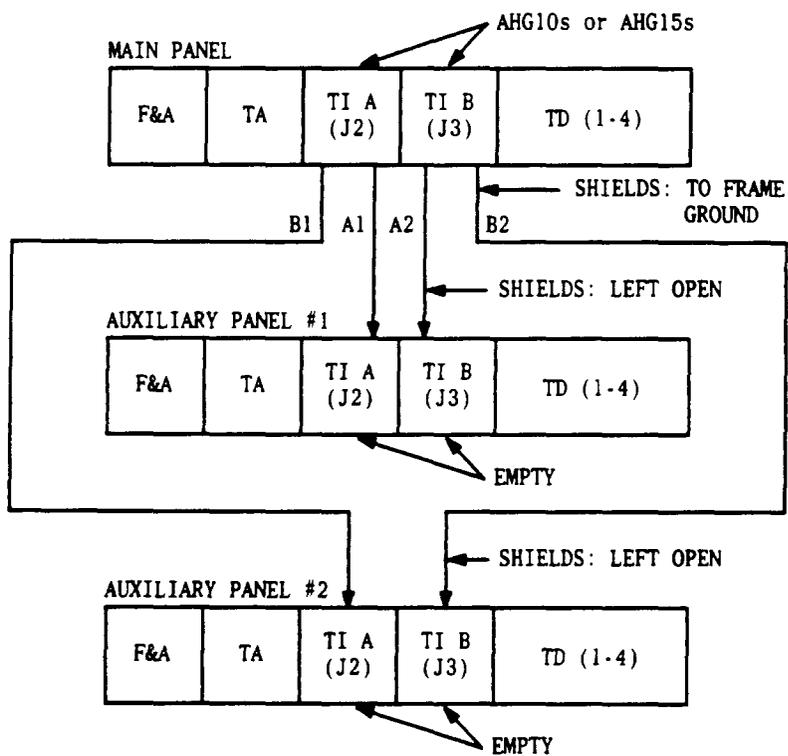


Fig. 25 - Cabling Diagram:Wiring Between Main & Aux Panels Using the AHG10/AHG15

6.15 The operation of the main and auxiliary panels, when properly connected, is much like that of the lone main panel. If an input source transfer is initiated, only the timing interface circuit packs on the main panel will be affected. If an output transfer is initiated, all of the timing distributor circuit packs will switch to the same reference on both the main and auxiliary panels. Alarm information, if present, will be reported separately by the main or auxiliary panels depending on the location of the trouble. It is recommended that separate power and alarm connections be used between the main and auxiliary panels so that redundancy and proper operation are assured. Outputs from the auxiliary panel are available at the SDE terminal block and wired in an identical fashion as the main panel.

6.16 If two J98726W-2 or J98726Y-1 panels are used as the main and auxiliary panels, the PCS will be operational on both panels. If the J98726W-1 panel is used as either the master or auxiliary panel, it will not be capable of supporting PCS.

6.17 As an ESD precaution, it is recommended that the ED8C717 (or equivalent) blank board be placed in the vacant TI slots of the auxiliary panels.

**7. REFERENCE DATA**

**A. WORKING LIMITS**

7.01 The battery supply voltage at the SDE shall be within the range of -41.7 to -52 volts.

**B. FUNCTIONAL DESIGNATIONS**

**a. CIRCUIT PACKS**

Code	Designation	Meaning
AHG1	TA	Timing alarm
AHG2	TI	Timing interface
AHG2B	TI	Timing interface
AHG3	TD	Timing distributor

AHG4	TD	Timing distributor
AHG10	TI	Timing interface
AHG5	TD	Timing distributor
AHG15	TI	Timing interface
AHG16	TI	Timing interface
AHG25	TD	Timing distributor
AHG26	TD	Timing Distributor

**b. FUSES**

Designation	Meaning
F1	Overcurrent protection of power feed to alarm circuit
F2, F3	Overcurrent protection of power feeds to functional units

**c. RELAYS**

Designation	Meaning
FA	Fuse alarm
MJ	Major alarm
MN	Minor alarm
ACO	Alarm Cut-Off

**d. VISUAL INDICATIONS**

Designation	Meaning
FA	Fuse alarm
MJ	Major alarm
MN	Minor alarm
ACO	Alarm Cut-Off
IN SCE	Input source
A TI OUTPUT IN USE	Output of TI A operating TD

B TI OUTPUT IN USE	Output of TI B Operating TD
TI A	Memory in TA registers signal outage or circuit malfunction in TI A
TI B	Memory in TA registers signal voltage or circuit malfunction in TI B
TD 1, TD 2 TD 3, TD 4	Memory in TA register signals outage or circuit malfunction in TDs 1, 2, 3, or 4
OSC	Oscillator LED on AHG2B signifies that the internal oscillator is being used as a result of failure of the input signal; i.e., holdover or free-run modes
CUTOFF	LED on the AHG4 signifies that the output signal has been disabled as a result of a dual-input failure of the timing interface circuit packs

**e. SWITCHES**

Designation	Meaning
ACO	Alarm Cut-Off
MEM	Momentary operation releases alarm condition registered in TA memory if fault is cleared
TR IN SCE	Change input signal source selection
TR OUT	Change TA output that is operating TDs

**C. GLOSSARY**

7.02 Terms used in this document are identified as follows:

TERM	DEFINITION
CDU	Clock Distribution Unit J98726Z-1
CTS	Composite Timing Signal
DACS	Digital Access and Cross Connect System
DDS	Digital Data System
DOTS	Digital Office Timing Supply
ESD	Electro-Static Discharge
F&A Panel	Fuse and Alarm Panel
IN FAIL	Input Failure
IN SCE TR	Input Source Transfer
LED	Light Emitting Diode
LTS	Local Timing Supply
MEM	Memory
NTS	Nodal Timing Supply
OTS	Office Timing Supply
PFS	Primary Frequency Supply
PLL	Phase-Locked Loop
SDE	Synchronization Distribution Expander
STS	Secondary Timing Supply
TA	Timing Alarm
TI	Timing Interface
TD	Timing Distributor
VCXO	Voltage Controlled Crystal Oscillator

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