

**DIGITAL DATA SYSTEM**  
**T1WB4 DATA-VOICE MULTIPLEXER**  
**DESCRIPTION**

CONTENTS	PAGE
<b>1. GENERAL</b> . . . . .	<b>1</b>
<b>2. FUNCTIONAL DESCRIPTION</b> . . . . .	<b>1</b>
<b>A. T1 Line Signal</b> . . . . .	<b>1</b>
<b>B. Operating Modes</b> . . . . .	<b>3</b>
<b>C. Timing</b> . . . . .	<b>4</b>
<b>D. Transmission</b> . . . . .	<b>4</b>
<b>E. Receiving</b> . . . . .	<b>6</b>
<b>F. Power and Alarms</b> . . . . .	<b>6</b>
<b>3. DETAILED DESCRIPTION</b> . . . . .	<b>6</b>
<b>A. Transmitter/Receiver</b> . . . . .	<b>6</b>
<b>B. Channel Unit</b> . . . . .	<b>10</b>
<b>C. Protection Switch I</b> . . . . .	<b>10</b>
<b>D. Protection Switch II</b> . . . . .	<b>11</b>
<b>E. Power</b> . . . . .	<b>11</b>
<b>F. Alarm Control Unit</b> . . . . .	<b>11</b>
<b>G. Clocks</b> . . . . .	<b>13</b>
<b>H. Test Circuit</b> . . . . .	<b>13</b>
<b>4. EQUIPMENT ARRANGEMENT</b> . . . . .	<b>14</b>
<b>5. MAINTENANCE FEATURES</b> . . . . .	<b>14</b>
<b>6. REFERENCES</b> . . . . .	<b>15</b>

**1. GENERAL**

**1.01** This section describes the T1WB4 data-voice multiplexer (T1WB4) which is used in metropolitan area applications of the Digital Data System (DDS).

**1.02** If this section is reissued, the reason for reissue will be given in this paragraph.

**1.03** The T1WB4, shown in Fig. 1, is a 2-shelf, 24-channel, synchronous digital multiplexer capable of combining digital data signals with digital data signals or with digitally encoded voice signals. It time division multiplexes these signals into a 1.544-Mb/s bitstream for transmission over T1 carrier facilities.

**1.04** The T1WB4 can be operated in three separate modes: independent data, chained data, and combined data-voice. These modes (discussed in detail in Part 2B) are easily selected by operating the proper switches.

**2. FUNCTIONAL DESCRIPTION**

**A. T1 Line Signal**

**2.01** The T1WB4 was designed for and is interconnected with the T1 digital transmission line and the D-type channel banks. A sample T1 line format generated by a T1WB4 is shown in Fig. 2. Each T1 line frame contains 192 information bits and 1 framing bit for a total of 193 bits. The 192 information bits are divided into twenty-four 8-bit bytes. Each byte corresponds to a data byte from the DDS or to a digitally encoded voice byte from a D-type channel bank. Data bytes can be inserted into any 12 of the 24 byte positions, and voice bytes occupy the remaining byte positions. Each data byte inserted into the T1 bitstream displaces one voice byte; therefore, each T1WB4

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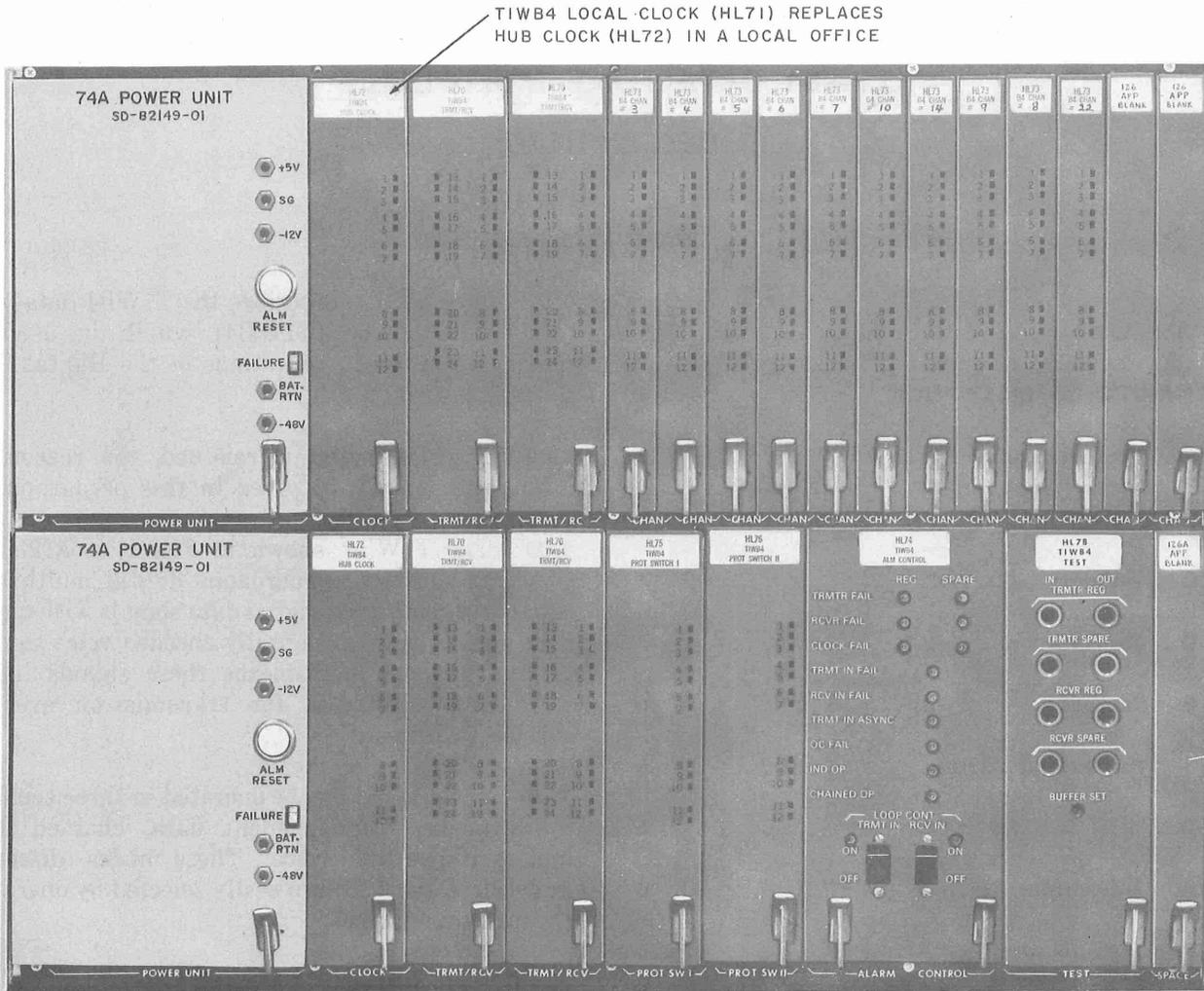


Fig. 1—T1WB4 Data-Voice Multiplexer

channel unit on either end of the connecting T1 line must be conditioned, by properly setting the channel unit selection switches, to accept and to send data in the preempted voice byte position. If the channel unit selection switches of corresponding channel units on the transmit and receive ends of a T1 line are not set to the same channel number, garbled data results.

**2.02** The first seven bits in a data byte can be used to transmit data, resulting in a maximum data rate of 56 kb/s for each data channel (seven bits for each byte times 8000 bytes a second). Since a byte contains eight bits in the T1WB4 format (the eighth bit is discussed in 2.03), the total bitrate of each data channel is 64 kb/s.

**2.03** Bit 8 in the data byte is dedicated to channel status information coding. When the customer data terminal is sending data, the office channel unit (OCU) inserts a logic 1 into bit position 8. When the customer data terminal is idle, the OCU inserts a logic 0 into bit position 8 and logic 1s into bit positions 2 through 7.

**2.04** The 193rd, or framing (F), bit associated with each T1 frame is monitored to synchronize the T1WB4 to the DDS network. It follows a 12-bit sequence, as indicated in Fig. 2, and repeats every 12 frames. The main framing (odd-frame) sequence is a 1010... pattern that occurs every other frame. The F-bit circuitry in the T1WB4 searches for this pattern in order to frame synchronize

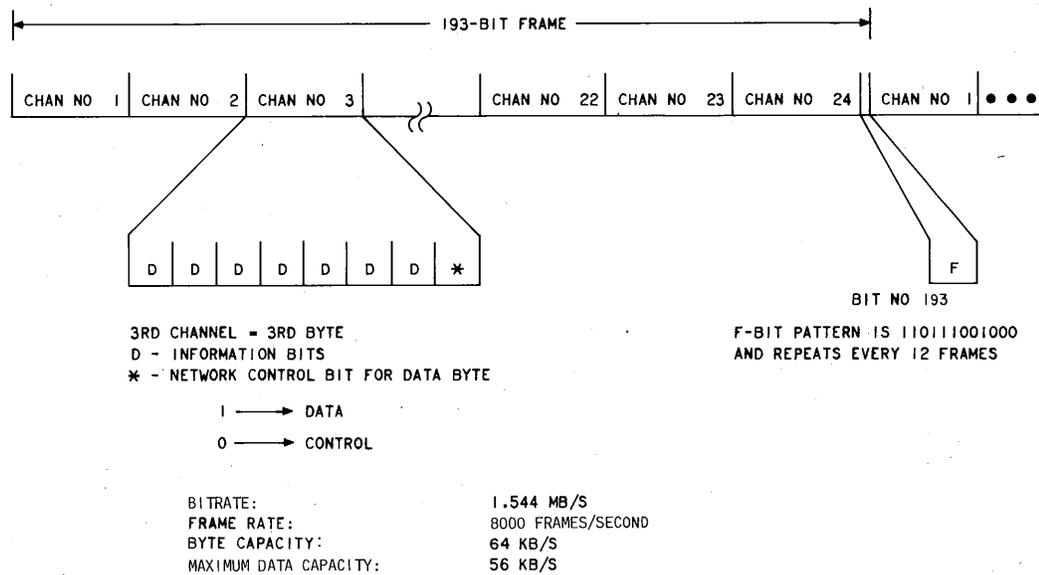


Fig. 2—T1WB4 Line Format

the T1WB4 to the T1 line. The T1WB4 also looks for the D3-type subframing (even-frame) pattern to verify that the 10... pattern to which it is synchronized is really the framing bit and not a data bit sequence that is simulating the 10... pattern.

**2.05** Since cable lengths between the T1WB4 and the 1.544-Mb/s digital system cross-connect (DSX-1) vary, two equalizers and a pad are provided to allow adjustment of the DS-1 line signal to a standard interface level at the DSX-1.

#### B. Operating Modes

**2.06** The three modes of operation—*independent data*, *chained data*, and *combined data-voice* (Fig. 3)—allow the T1WB4 to be used efficiently in the DDS.

**2.07** *Independent data operation* (Fig. 3A or B) is selected by setting the IND OP switch behind the faceplate of protection switch (PS) II to the ON position and the CHAINED OP switch on the alarm control unit (ACU), HL74, to the OFF position. When set for this mode, the T1WB4 is timed by the internally generated 1.544-MHz local clock which is synchronized to the receive T1 line. No digitally coded voice signals are sent through the T1WB4 in this mode; therefore, the T1 line

attached to the T1WB4 carries a maximum of 12 data channels. If any channel unit equipment location is vacant, an out-of-synchronization byte code is placed on the T1 line in the appropriate time slot.

**2.08** *Chained data operation* (Fig. 3C) provides a way to add data customers to a T1 line between a local end office and a hub office. In this mode, no voice channels are present on the T1 line. The first T1WB4 in the chain (local end office) is set for independent data operation and is synchronized to the DDS network by an internal clock signal derived from the receive T1 line. The first T1WB4 generates its own transmit framing pattern and each T1WB4 in the upstream chain then synchronizes on this framing pattern. Each T1WB4 in a chain office is set for chained data operation. This mode is selected by setting the CHAINED OP switch behind the faceplate of the ACU to the ON position and the IND OP switch on PS II to the OFF position.

**2.09** When set for *combined data-voice operation* (Fig. 3D), the T1WB4 at each end of the T1 facility is connected to a D-type channel bank, derives clocking and gating signals from the transmit T1 line, and combines digitally encoded voice channels from the D bank with a recommended maximum of twelve 64-kb/s data channels entering

the T1WB4 channel unit ports. This operation is used in an office anticipating slow digital data growth. It is selected by setting both the IND OP switch on PS II and the CHAINED OP switch behind the faceplate of the ACU to the OFF position.

### **C. Timing**

**2.10** Like all DDS central office equipment, the T1WB4 must use a nodal timing supply (NTS) or a secondary timing supply (STS) as the source of 8- and 64-kHz clock signals when operating in a hub office. Timing is not available at a local office, but the T1WB4 is provided with an integrated local clock circuit pack that derives 8- and 64-kHz clock signals from the recovered 1.544-Mb/s received line signal, converts these signals to a composite bipolar signal, and sends the composite signal to the bay clock, power, and alarms (BCPA) shelf. The BCPA shelf converts the composite bipolar signal to individual unipolar 8- and 64-kHz clock signals and sends these signals to the T1WB4 integrated timing supply for distribution to other T1WB4 circuits. If the received line signal is lost, a holdover circuit is actuated that holds the clock frequency of the T1WB4 stable for approximately 2 seconds at a frequency close to the last frequency setting before the signal loss. This feature is necessary to maintain customer bit integrity during protection switching of the digital line.

**2.11** When the T1WB4 is set for combined data-voice operation, the D-type channel bank must be capable of being loop timed at local offices and externally timed at hub offices. Loop and external timing information for D3, D2, and D1D channel banks is given in Sections 365-150-100, 365-400-100, and 365-116-100, respectively.

### **D. Transmission**

**2.12** Figure 4 shows a functional block diagram of the T1WB4 connected for local timing and set for combined data-voice operation. The following explanation of the overall T1WB4 operation in both the transmitting and receiving directions is based on this figure. Operation of each major block is explained in Part 3.

**2.13** During transmission, the D-type channel bank transmitting equipment generates a 1.544-Mb/s bitstream, synchronized to the DDS network, which contains 24 digitally encoded voice channels and the necessary framing pulses. This

bipolar T1 signal is routed through a DSX-1 to a test access circuit in the T1WB4. From the test access circuit, the transmit 1.544-Mb/s T1 voice signal is paralleled to both the regular and the spare transmitters. The regular transmitter counts the T1 signal bytes, examines framing, and derives selected clock signals from the T1 line. All 12 channel unit transmitting output circuits are multiplied and then paralleled to the inputs of the regular and spare transmitters. The spare transmitter duplicates the functions of the regular transmitter and replaces the regular transmitter if necessary.

**2.14** Each channel unit inserted into the T1WB4 causes one voice byte in the frame to be replaced by a data byte. Which voice byte is replaced is determined from the settings of the channel unit selection switches.

**2.15** The transmitter monitors the T1 voice byte signals from the D-type channel banks and the transmit data byte signals from the channel units. It then places one data byte from each active channel unit in the corresponding voice byte position in the T1 bitstream. The combined data-voice output (transmit voice and data) from the regular transmitter and an identical bitstream from the spare transmitter are connected to a common output in PS I through relay transfer contacts. Either the regular or the spare transmitter drives the T1 line. Normally the regular transmitter drives the line; if it fails, however, it is disconnected from the line and the spare transmitter replaces it. The outputs from the regular and spare transmitters are also connected to transmit out monitor jacks in the test circuit.

**2.16** If no channel units are installed in the T1WB4, all 24 voice channels of the T1 line signal received from the D-type channel banks are transmitted unchanged by the T1WB4. When at least one channel unit is installed, however, the T1WB4 operates as described in 2.12 through 2.14.

**2.17** Data at the 64-kb/s rate is written simultaneously into all channel units by 64-kHz clock signals generated by the local clock. The data is temporarily stored in the channel units. The transmitter, using a 1.544-MHz clock, scans the channel units and enters one data byte from each unit on each frame of the T1 transmit line. The channel selection pulses from the channel units cue the combiner each time a data byte is entered onto the T1 line.

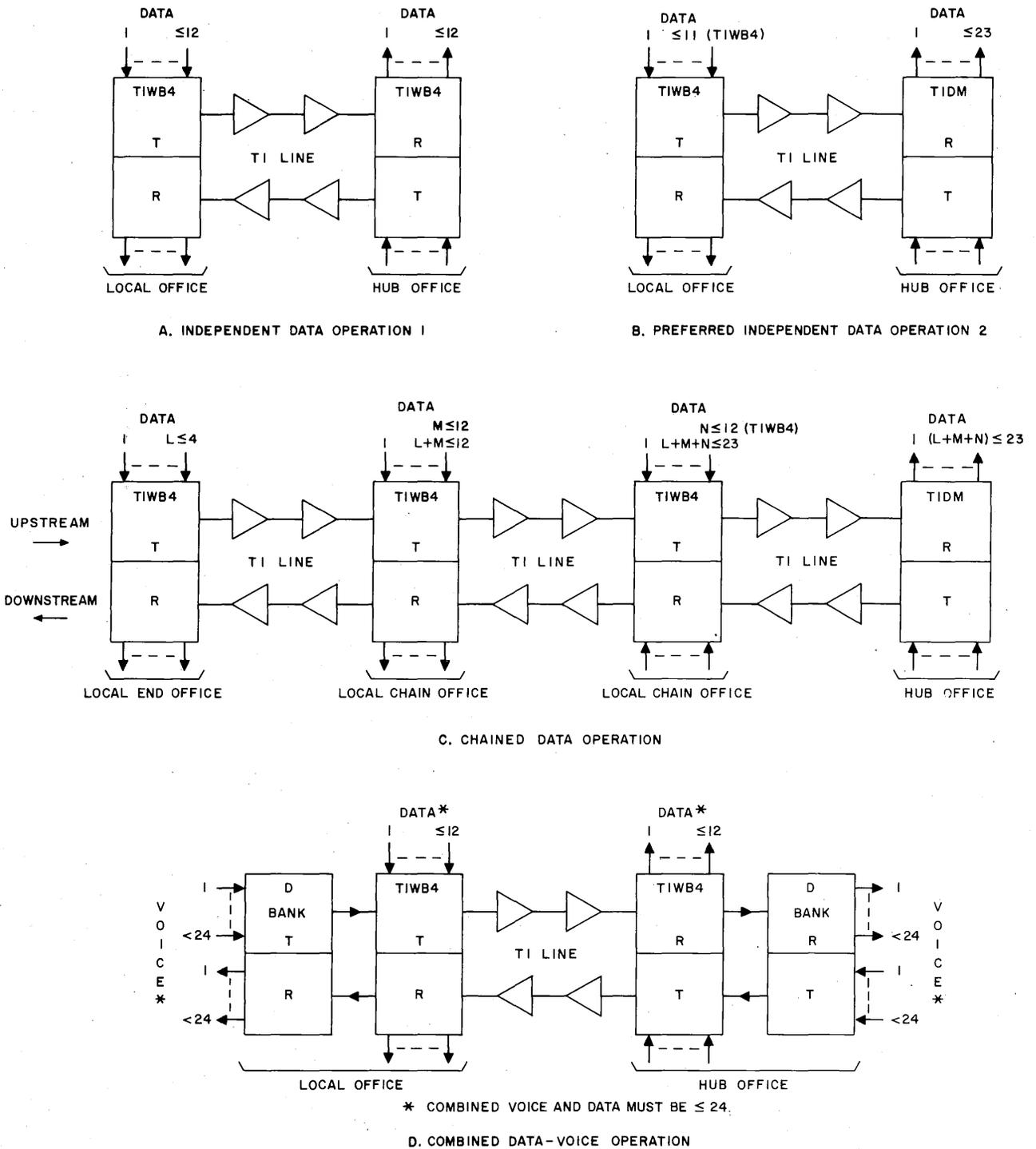


Fig. 3—TIWB4 Modes of Operation

**E. Receiving**

**2.18** The T1 voice and data receive line signal enters the T1WB4 through the test circuit. The signal splits in the test circuit, one input going to the regular receiver and the other input going to the spare receiver. If no channel units are installed in the T1WB4 at the local office end of the T1 line or in the T1WB4 at the hub office end of the T1 line, the receive T1 voice bytes are routed to the D-type channel bank receiving circuits through PS I and the DSX-1.

**2.19** If channel units are installed in the T1WB4s at the ends of the T1 line, the receive T1 line contains data bytes. The receiver extracts the data bytes from the receive T1 line and distributes each to the proper channel unit through relay contacts in PS I. The receive data lead is multiplied to all the channel units. Synchronization provided by gating signals from the active receiver allows the receive data bytes to be sent to the appropriate channel units at the proper time. The byte positions left vacant by the extracted data bytes are stuffed with all ones (1111111) by the receiver, and the stuffed bytes are sent to the D-type channel bank.

**2.20** The receive voice bytes from the regular and spare receivers are routed to PS I, where they are connected to relay contacts. They are then routed through the DSX-1 to the D-type channel bank receiving circuitry. If either active receiver circuit becomes defective, sensing circuits in the ACU switch the functioning receiver through PS I to the D-type channel bank. Also, the individual receive voice outputs of both the regular and the spare receivers are available for monitoring at the receive out jacks of the test circuit.

**F. Power and Alarms**

**2.21** The power source for the T1WB4 is the 74A power unit in a -48 Vdc office or the 78A power unit in a -24 Vdc office. The power unit selected provides +5 and -12 Vdc to all circuits in the T1WB4. A regular and a standby power unit are required, but only one power unit at a time is tied to T1WB4 circuits through PS II. Regular +5 and -12 Vdc power is applied to T1WB4 circuits through the break contacts of PS II and standby +5 and -12 Vdc power is applied through the make contacts. If the +5 or -12 Vdc power fails, a relay in PS II closes the make

contacts and connects the standby power unit to the T1WB4 power bus while opening the break contacts and disconnecting the regular power unit from the bus. Voltage monitoring leads from both the regular and the standby power units connect through contacts on the test circuit to the BCPA shelf to provide centralized alarm indications.

**2.22** The ACU monitors transmit and receive line signals and all the clock and gating signals needed in the T1WB4. It controls all relay drivers in both protection switches, thus controlling all switching of major T1WB4 components.

**3. DETAILED DESCRIPTION****A. Transmitter/Receiver**

**3.01** *The detailed descriptions that follow are based on Fig. 4.* With the exception of the combiner unit, the transmitter/receiver circuit pack performs identical functions for both the transmit and the receive directions of transmission. The shelf back plane wiring and strapping arrangements initiate the receiving or transmitting function. Therefore, the transmitter/receiver circuit pack can be used as a transmitter or receiver depending on whether it is inserted in a transmitter or a receiver equipment location.

**3.02** The transmitter/receiver used as a transmitter receives the bipolar 1.544-Mb/s signal from a D-type channel bank when the T1WB4 is set for combined data-voice operation. The incoming bipolar signal is amplified and converted to a unipolar pulse train by amplifier 1. This unipolar signal is routed to the combiner circuit where it is combined with data signals (transmit data) from the channel units. The combined data and voice signal is amplified by amplifier 2 and converted to bipolar form. In bipolar form, the transmit voice and data signal is routed to PS I and, on monitor voice and data transmit leads, to the test circuit. From PS I the combined voice and data signal is routed through equalizers or pads, and then through a DSX-1 to a T1 line.

**3.03** The recovered 1.544-MHz transmit clock signal is extracted from the transmit T1 line signal at amplifier 1 and is connected to relay contacts in PS II. These relay contacts interconnect with the 1.544-MHz local clock signal. Similarly, the recovered 1.544-MHz transmit clock lead from the spare transmitter connects through relay contacts

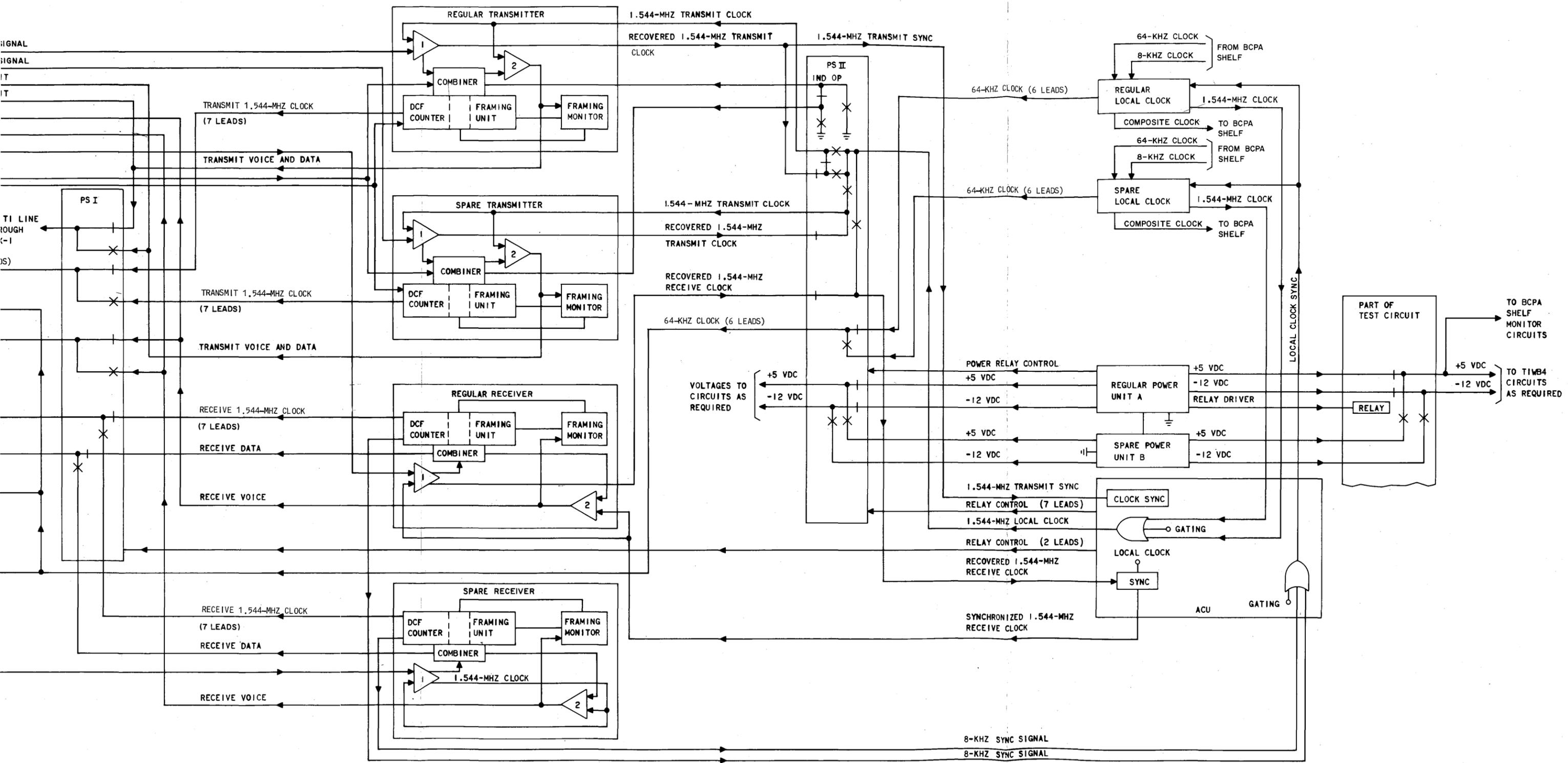
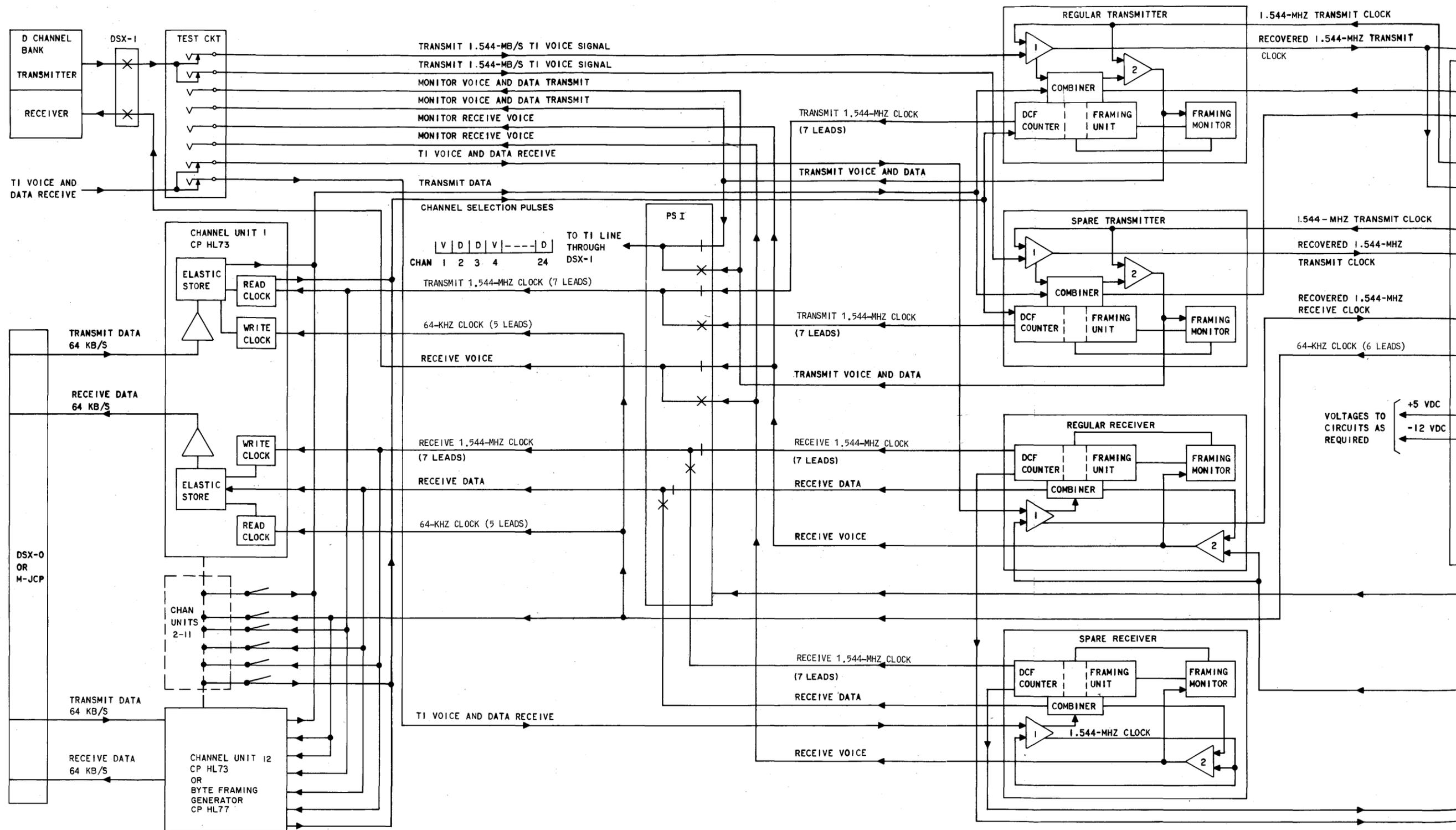


Fig. 4—T1WB4—Functional Block Diagram



to the local 1.544-MHz clock signal. The 1.544-MHz transmit sync lead splits from the recovered 1.544-MHz transmit clock lead and connects to the ACU. In the ACU, the 1.544-MHz transmit sync clock signal is compared with the local 1.544-MHz clock signal. As long as the recovered clock is synchronous with the local clock, the recovered 1.544-MHz transmit clock signal loops through the relay break contacts of PS II to the transmitter. If the recovered clock becomes asynchronous with the local clock, the local clock replaces the recovered transmit clock as the 1.544-MHz signal source.

**3.04** When the T1WB4 is set for independent data or chained data operation, the transmitter has no T1 line input from a D-type channel bank and only data is processed by the T1WB4 and sent out on the outgoing multiplexed T1 line. Timing for independent data or chained data operation (1.544 MHz) is provided through PS II by the hub or local clock. When an office timing supply is available, the hub clock circuit packs are used and are synchronized to the 8-kHz office timing supply. The 1.544-MHz clock signals from the regular and spare clock circuit packs are routed to the ACU, where either the regular or spare clock is selected. The clock signal selected is connected to PS II and then to the transmit converter amplifiers to supply 1.544-MHz clock signals. If an office does not have an office timing supply, a local clock circuit pack arrangement is used to provide timing. Here, the 1.544-MHz synchronized clock feeding the regular receive converter amplifiers is synchronized to the receive T1 line signal instead of to an office clock. The regular and spare transmit converter amplifiers receive 1.544-MHz timing from the local clock through relay contacts on PS II.

**3.05** The digit, channel, and frame (DCF) counter extracts all the necessary synchronizing information from the input DS-1 frame format and furnishes clock signals to all channel units. Each channel unit uses these clock signals to generate a channel selection pulse 1/24th of a frame long corresponding to each channel unit equipment location. Channel selection pulse generation occurs in both the transmitting and receiving sections of the channel units.

**3.06** 1.544-MHz clock signals are generated by both the transmitter and receiver DCF units. The clock signals from the transmitter DCF are multiplied to all channel unit read clock circuits, where they are used to clock data bytes from the

channel unit transmit elastic stores to the transmitter combiner. The clock signals from the receiver DCF are multiplied to all channel unit write clock circuits, where they are used to clock data bytes from the receiver combiner to the channel unit receive elastic stores.

**3.07** The *transmitter combiner* circuitry synchronizes and time division multiplexes transmit data bytes from the channel units with data bytes or digitally encoded voice bytes from the transmit T1 bitstream. The bitstream entering the transmitter combiner contains digitally encoded voice bytes in combined data-voice operation or data bytes in chained data operation. The channel selection pulses from the channel unit transmitters are logically ORed together in the combiner, and the transmit data bytes from the channel units are logically ORed together in the combiner. The outputs from the two OR gates are used in adding data bytes to the T1 bitstream. When a channel unit selection pulse is present, the transmitter combiner logic removes a byte from the transmit T1 bitstream and inserts a data byte from a channel unit in the vacated time slot.

**3.08** In independent data operation, the *receiver combiner* circuitry removes data bytes from the receive T1 bitstream and sends each byte to its appropriate channel unit. In chained data operation, the receiver combiner of each T1WB4 in a chain office removes data bytes from the receive T1 bitstream and replaces each data byte removed with an all 1s stuff byte to maintain the T1 frame format. The stuff bytes and the remaining data bytes of the receive T1 bitstream are sent out to the receiver of the next T1WB4 in the chain. In combined data-voice operation, the receive T1 bitstream coming into the receiver combiner contains both data and voice bytes. The data bytes are extracted and each is sent to its appropriate channel unit. An all 1s stuff byte is inserted in each time slot vacated by a data byte. The stuff bytes and voice bytes of the receive bitstream are sent to the D-type channel bank.

**3.09** A portion of the combiner circuitry is a coding circuit that injects coded alarm information data bytes into the T1 bitstream under certain equipment conditions and DDS network malfunctions.

**3.10** The framing unit synchronizes on the incoming T1 line framing bits (193rd bit in each frame)

from odd-numbered frames. The even-numbered frame framing bits are used to verify a correct T1 line framing pattern in the multiplexing direction because data bytes can simulate the odd-frame pattern. Comparison gates in the framing unit compare the current odd-frame framing bit with that previously stored. If the comparison gates determine that the framing bits are different, good framing is assumed since the odd-frame framing pattern changes from 1 to 0 on every other framing pulse.

**3.11** The framing monitor checks the bipolar T1 output bitstream of the transmitter for proper framing. The framing bits examined are gated through the logic circuitry on every odd-frame framing pulse. These odd-frame framing pulses set and reset a flip-flop that divides the odd-frame repetition rate (4 kHz) by 2, generating a 2-kHz output. This 2-kHz output drives a tuned circuit and threshold detector to give framing status at test point (TP) 24. A logic 0 indicates good framing; a logic 1, an out-of-frame condition.

**3.12** After a minimum of three errors in five odd-frame tests of the main framing sequence, the T1WB4 enters an out-of-sync state. In this state, the sync detector initiates a search for the main framing sequence. Once nine successive good framing bits are detected and the interlaced framing sequence is verified, the T1WB4 can return to the in-sync state.

**3.13** Two distinct out-of-sync states are possible in the T1WB4. If an out-of-sync condition lasts less than 400 milliseconds, garbled data bytes are transmitted from each channel unit of the out-of-sync T1WB4. In data-voice operation, the transmit voice bytes are also garbled. If 400 milliseconds or more elapse, an out-of-sync code is transmitted to all channel unit receivers. This code byte contains logic 1s in bit positions 4, 5, and 7 and logic 0s in the remaining positions. The out-of-sync code is transmitted until synchronization is recovered.

## B. Channel Unit

**3.14** The output of each ISMX, 56-kb/s OCU, or SRDM physically connects to only one channel unit. The channel unit first converts each 64-kb/s bipolar input signal to unipolar and then writes the unipolar signal into its elastic store with a 64-kHz clock synchronized to the DDS network.

Data is written simultaneously into the elastic stores of all channel units installed in the shelf. Elastic stores are necessary in the channel units to compensate for temperature variations of the T1 line which can cause time variations in the data signals. Each elastic store is essentially a pair of shift registers connected in parallel by an OR circuit. Data stored in the shift register is read out by the 1.544-MHz transmit clock which is gated so that one register is read out while the other is having data written into it. Transmit data from all channel units is connected to the combiner circuits of both the regular and spare transmitters by the transmit data signal bus.

**3.15** On the receive side of the channel unit, the data bytes unique to each channel unit are extracted from the receive 1.544-MHz T1 line through the receiver combiner. A channel pulse selected by the channel unit selection switches cues the channel unit when to extract the proper channel unit data byte from the receive T1 line. Each extracted data byte (receive data lead) for a particular channel is written into the receive elastic store by a 1.544-MHz clock signal. Like the transmit elastic store, the receive elastic store is essentially two parallel 8-bit shift registers inputting an OR circuit. Depending on the logic gating signals, either shift register can receive a data byte from the combiner. The data byte is then shifted out of the shift register by a 64-kHz read clock, converted to the bipolar format, and sent to the 64-kb/s digital system cross-connect (DSX-0).

**3.16** Each channel unit contains a channel selection unit made up of logic gates and six slide switches (channel unit selection switches). For proper T1WB4 operation, the channel unit selection switches are set according to Table B, C, or D in Section 314-915-300. Each channel unit is then inserted into a channel unit equipment location of shelf "B". Shelf "B" has 12 channel unit equipment locations numbered from left to right in ascending order beginning with equipment location 36.

## C. Protection Switch I

**3.17** PS I provides switching between the regular and spare transmitters and between the regular and spare receivers. The transmit 1.544-Mb/s T1 voice signal is paralleled to the inputs of both the regular and spare transmitters. The transmit voice and data output line signals are wired to PS I. The output of the regular transmitter is

connected to break contacts; the output of the spare transmitter, to make contacts. If the regular transmitter becomes defective, the ACU causes the relay contacts to switch, replacing the output from the regular transmitter with the output from the spare transmitter. An example of the T1WB4 data-voice multiplexed signal is shown in Fig. 4 at the output of PS I. The transmit 1.544-MHz clock leads from the DCF counters of both the regular and spare transmitters are also switched in PS I by the ACU relay control leads.

**3.18** The T1 voice and data receive line is connected in parallel to the inputs of both the regular and spare receivers. Receive voice and receive data outputs from the regular receiver connect to break contacts in PS I, and the corresponding outputs from the spare receiver connect to make contacts in PS I. If the regular receiver malfunctions, the ACU causes the relay contacts to switch by means of relay control leads and the spare receiver replaces the regular receiver. Receive 1.544-MHz clock signals from DCF counters in both the regular and spare receivers are also switched through PS I under control of the ACU.

#### D. Protection Switch II

**3.19** The local clock provides 4-, 8-, and 64-kb/s clock signals to PS II (64-kHz clock). Regular clock signals connect to the break contacts; spare clock signals, to the make contacts. If the ACU detects a malfunction in the clock, the spare 64-kHz clock signals instead of the regular 64-kHz clock signals are switched through to the channel units.

**3.20** Timing at the 1.544-MHz rate is transferred through PS II contacts for both the regular and spare transmitters and the regular and spare receivers. In normal operation with a local clock, the regular and spare transmitters derive the recovered 1.544-MHz transmit clock signals from the transmit T1 line. The recovered 1.544-MHz transmit clock signals for the regular and spare transmitters are looped through break contacts on PS II and back to each transmitter as 1.544-MHz transmit clock signals. If the transmit T1 line signal becomes asynchronous or if the T1WB4 is set for independent data operation, the ACU causes contacts controlling both the regular and the spare 1.544-MHz clock supplies to switch. Both break contacts for recovered 1.544-MHz transmit clock paths through PS II open, and 1.544-MHz local clock signals from the local clock circuits are routed

through make contacts to the regular and spare transmitters.

**3.21** The regular receiver derives 1.544-MHz timing from the receive T1 line (recovered 1.544-MHz receive clock) and routes it through break contacts on PS II to the ACU, where it is used to synchronize a signal from the local clock circuit. The synchronized 1.544-MHz receive clock signal is returned to the regular receiver for its internal 1.544-MHz timing requirements. If the receive 1.544-MHz clock from the regular receiver becomes asynchronous with the local clock, the ACU causes the relay break contacts in PS II to open, disconnecting the recovered 1.544-MHz receive clock line from PS II. Simultaneously, the make contacts connected to the 1.544-MHz local clock close, providing 1.544-MHz local clock timing to the regular receiver.

**3.22** The IND OP switch on PS II is turned to the ON position to set the T1WB4 for independent data operation because no timing is available from a D-type channel bank. When the IND OP switch is set to the ON position, relay contacts in PS II connect local clock timing to both the regular and spare transmitters.

#### E. Power

**3.23** Regular and standby power units are provided for the T1WB4. The units are dc-to-dc converters that convert -24 or -48 Vdc to +5 or -12 Vdc for distribution to T1WB4 circuits. A sensing circuit in regular power unit A controls the PS II relay driver and causes a switch to standby power unit B if the regular power supply fails. Test points for +5 or -12 Vdc and for -24 or -48 Vdc are brought out to the front panel of each power unit. A red FAILURE lamp and an ALM RESET key are also provided (see Fig. 1).

#### F. Alarm Control Unit

**3.24** The ACU senses transmitter, receiver, and clock malfunctions and generates the appropriate switch signals to relay drivers in PS I and II. Framing information from the regular and spare transmitters and from the regular and spare receivers is connected to the ACU. Logic circuitry in the ACU evaluates the input framing information from the regular transmitter and receiver and causes a switch to a spare unit if either malfunctions.

**3.25** When local clock circuit packs are installed, the regular and spare local clocks are synchronized to the T1 line by an 8-kHz signal from the ACU. Both the regular and spare receivers extract an 8-kHz clock signal from the receive T1 line and send it to logic circuitry in the ACU. The ACU selects either the regular or spare 8-kHz sync signal and routes it (local clock sync) to both the regular and spare local clocks.

**3.26** A recovered 1.544-MHz transmit clock signal is extracted from the transmit T1 line by the regular transmitter and is sent to clock sync logic circuits in the ACU. There, the 1.544-MHz transmit sync signal is compared with the 1.544-MHz signal generated by the local clock. If the 1.544-MHz transmit sync signal is in sync with the local clock, the 1.544-MHz transmit clock is used as the transmit clock for the regular transmitter. If the 1.544-MHz transmit clock signal becomes asynchronous with the 1.544-MHz local clock signal, the ACU energizes a relay in PS II, causing the 1.544-MHz local clock signal to replace the 1.544-MHz transmit clock signal derived from the transmit T1 line.

**3.27** The regular receiver extracts 1.544 MHz from the receive T1 line and routes the recovered 1.544-MHz receive clock signal to logic circuitry in the ACU, where it is used to synchronize a local clock signal. The recovered 1.544-MHz clock signal

is routed back to the regular receiver as its 1.544-MHz timing supply. If both the regular and spare receivers go out of frame, the ACU senses the malfunction as a receive input failure and gives a switch command to a relay in PS II. The synchronized 1.544-MHz receive clock signal is then replaced by the local clock signal from the ACU.

**3.28** The various alarm conditions of the ACU are listed in Table A. These alarms are displayed at the T1WB4 by light-emitting diodes (LEDs) on the faceplate of the ACU. The LEDs are lighted and office alarms are actuated if one or more common equipment circuit packs fail or if there is loss of framing and incoming signals. Some malfunctions in the D-type channel banks can affect the T1 line signal but cause no sustained loss of data in the T1WB4.

**3.29** When the T1WB4 is set for combined data-voice operation, it must not interfere with the D-type channel bank red and yellow alarm system. When a D bank cannot frame on a received T1 signal or when the signal is absent, the D bank displays a red alarm indication. This trouble condition is caused by a defective D bank transmitter at the other end, by a defective incoming T1 line, or by a defective D bank receiver where the alarm is displayed.

TABLE A

LED INDICATIONS PROVIDED ON ALARM CONTROL UNIT

LED LIGHTED	TYPE OF ALARM AND OPERATION					
	NONCHAINED			CHAINED		
	REG	SPARE	BOTH	REG	SPARE	BOTH
TRMTR FAIL	MN	MN	MJ	MN	MN	MJ
RCVR FAIL	MN	MN	MJ	MN	MN	MJ
CLOCK FAIL	MN	MN	MJ	MN	MN	MJ
TRMT IN FAIL		MN			MJ	
RCVR IN FAIL		MN			MJ	
TRMT IN ASYNC		MN			MJ	
OC FAIL		MJ			MJ	
IND OP		None			None	
CHAINED OP		None			None	
LOOP CONT		None			None	

**3.30** When combined data-voice operation is implemented, a T1WB4 or a T1WB5 data-voice multiplexer (T1WB5) is located at the local office and a T1WB4 is located at the hub office. If the D bank transmitter at the local office fails, the T1WB4 or T1WB5 cannot frame on the transmitting side and displays a TRMT IN FAIL alarm. To preserve data transmission, the T1WB4 or T1WB5 breaks away from the D bank and continues to send a DS-1 signal containing data and a through stream consisting of an internally generated red alarm code. This code is an 8-bit code with bit 3 set to logic 0 and the remaining bits set to logic 1s. It is sent in all channel bytes not used for data. The red alarm signal (DS-1 signal) contains an internally generated framing pattern so that the T1WB4 at the hub office can frame on it and continue to receive data. The T1WB4 includes a detector that responds to the absence of bit 3 pulses in the through stream. This response causes the framing pattern to be inhibited at the T1WB4 so that the receive output DS-1 signal to the D bank at the hub office does not have a framing pattern. The D bank cannot frame and displays the red alarm to indicate the failure. If the D bank transmitter at the hub office fails, the T1WB4 breaks away from the D bank and sends the red code to the T1WB4 or T1WB5. The T1WB4 or T1WB5 detects the absence of bit 3 in the through stream and sends a DS-1 signal without framing to the D bank in the local office. The D bank cannot frame and displays the red alarm to indicate the failure. If a D bank red alarm is caused by a bad line or by a defective D bank receiver, the alarm is displayed without help from the T1WB5 and T1WB4.

**3.31** A D-type channel bank displaying a red alarm signals the D bank at the other end with a yellow alarm code. This code is the suppression of the bit 2 pulse in all voice channels. When a D bank receives a T1 signal with bit 2 missing from all channels, it displays a yellow alarm to indicate that there is a red alarm on the D bank at the other end. If the D bank at the hub office is transmitting the yellow alarm code, it is detected at the T1WB4 or T1WB5 at the local office as the absence of a bit 2 pulse in the through stream. The T1WB4 or T1WB5 in turn takes the bit 2 pulse out of the received bytes containing an all 1s stuff code so that the D bank in the local office receives the yellow alarm code in all channels, including those that were preempted for data. If the yellow alarm code is being sent to the hub

office, the T1WB4 there detects the code and takes bit 2 out of the stuff code.

**3.32** The T1WB4 has four alarm interfaces that are compatible with the T Carrier Administration System. Two alarms are used for a combined status of all failure indications on the ACU. Either a major or minor alarm contact closure is actuated depending on whether the failure is service affecting. The other two are used specifically for the TRMT IN FAIL and RCV IN FAIL alarm statuses.

**3.33** Since the T1WB4 can be used to add and drop customers in chained data or combined data-voice operation, it has both input and output DS-1 ports. The four ports are: TRMTR IN, TRMTR OUT, RCVR IN, and RCVR OUT. Jack access to them is available on the test circuit (HL78). The TRMTR IN port receives a DS-1 bitstream, the T1WB4 adds data bytes to the bitstream, and the bitstream is retransmitted; this retransmitted DS-1 bitstream is the TRMTR OUT signal. The RCVR IN port receives a DS-1 bitstream, the T1WB4 extracts data bytes from the bitstream and replaces them with all 1s stuff bytes, and retransmits the bitstream through the RCVR OUT port. In independent data operation, the TRMTR IN and RCVR OUT ports are not used.

## G. Clocks

**3.34** The local clock circuit pack is basically a crystal-controlled oscillator synchronized to the DDS network by signals extracted from an incoming T1 line. It provides 1.544-MHz, 64-kHz, and 8-kHz signals to the T1WB4 and other associated circuits through the BCPA unit. If DDS synchronization is lost, the oscillator may drift out of sync if the outage exceeds 2 seconds. When DDS synchronization is restored, the local clock circuit pack resynchronizes on the receive T1 line. The equipment locations for the regular and spare clock circuit packs are shown in Fig. 1.

## H. Test Circuit

**3.35** The test circuit provides monitor jacks for transmit and receive T1 lines and for the regular and spare transmitters and receivers. It also provides a BUFFER SET key to initialize the elastic stores of channel units and a relay and associated contacts to switch +5 and -12 Vdc to selected T1WB4 circuits. Faceplate nomenclature

and jack configurations for the test circuit are shown in the lower right-hand corner of Fig. 1.

**3.36** The TRMTR REG IN, TRMTR SPARE IN, RCVR REG IN, and RCVR SPARE IN jacks are all line terminating jacks. Therefore, inserting a patch cord into any of them opens the DS-1 signal path to the corresponding circuit. The transmitter input jacks are wired so that the transmit input signal is split between the regular and spare transmitters and the receiver input jacks are wired so that the receive input signal is split between the regular and spare receivers. The TRMTR REG OUT, TRMTR SPARE OUT, RCVR REG OUT, and RCVR SPARE OUT jacks are all bridge jacks. Inserting a patch cord into any of them parallels the patch cord with the DS-1 line and does not open the DS-1 signal path to the corresponding circuit.

#### 4. EQUIPMENT ARRANGEMENT

**4.01** The T1WB4 assembly (J70177AP), shown in Fig. 1, consists of two shop-wired, diecast aluminum shelves 23 inches wide, 8 inches high, and 12 inches deep. The assembly is arranged for front mounting in either 7-foot or 11-foot 6-inch unequal-flange, cable-duct type bays.

**4.02** The top shelf is designed to accept one power unit and 15 HL-coded plug-in circuit packs, three circuit packs associated with the regular common equipment and 12 channel units. The bottom shelf is equipped with a spare power unit, a spare clock circuit pack, two spare common equipment circuit packs, two protection switching circuit packs, an ACU, a test circuit pack, and an apparatus blank. One of two power units (74A or 78A) operating from office battery (-48 or -24 Vdc, respectively) plugs into each shelf.

**4.03** To interconnect a T1WB4 carrying only data with a T1DM, a byte framing generator circuit pack (HL77) is inserted into channel unit equipment location 68, which is the position farthest right in the top shelf (see Fig. 1). The byte framing generator circuit pack allows a T1WB4 to frame synchronize with a T1DM at the far end, but its use limits the number of data channels the T1WB4 can process to 11.

#### 5. MAINTENANCE FEATURES

**5.01** The T1WB4 uses 1-for-1 automatic protection sparing of individual common equipment circuit packs. An ACU indicates the status of each circuit pack and of all incoming and outgoing DS-1 signals. If an individual common equipment circuit pack fails for more than 200 milliseconds, it is automatically spared and a red LED on the ACU is lighted to indicate the failed unit. If the incoming signal to the transmitter from the D-type channel bank fails from loss of either pulses or framing for 400 milliseconds or more, the T1WB4 automatically switches to independent data operation to maintain data service. A red LED is lighted on the ACU to indicate this failure. When the failed external equipment is repaired and the incoming signal is good, combined data-voice operation is automatically restored in approximately 1 second. If the incoming signal to the receiver fails for 400 milliseconds or more, the appropriate red LED on the ACU lights and an out-of-sync signal is sent to the data customers.

**5.02** To guard against incorrect use of the loop control and operation mode switches, the green LEDs on the ACU are lighted whenever these switches are actuated.

**5.03** In the unlikely event that the visual displays on the ACU do not adequately localize a trouble, test points and test jacks are provided for use with portable test equipment to troubleshoot the T1WB4. The test jacks can be used to loop the transmitted DS-1 signals back to their own receivers, thus permitting effective preservice testing and fault isolation. These jacks can also be used to check T1WB4 performance independent of the digital line or D-type channel bank, or both, and the far-end T1WB4 or T1WB5.

**5.04** The loop control (LC) switches are intended for use in loop testing a T1 line. They are inoperative unless there is an incoming alarm condition in the T1WB4. When operational, the LC switches disable the incoming failure office alarm signals and cause an out-of-sync code to be transmitted to each channel unit. There are two LC switches on the ACU, one for the TRMT IN line and one for the RCV IN line. ***Setting the LC switches to the ON position does not loop the T1 line. The T1 line is looped with patch cords at the test circuit (HL78).***

**6. REFERENCES**

314-915-300	Digital Data System—T1WB4 Data-Voice Multiplexer—Initial Installation and Tests	365-150-100	Digital Transmission Systems—D3 Channel Bank—Description
314-915-501	Digital Data System—T1WB4 Data-Voice Multiplexer— Trouble-Locating Procedures	365-400-100	Digital Transmission Systems— D2 Channel Bank—General Description
365-116-100	Digital Transmission Systems— D1D Channel Bank—Description	CD- & SD-73042-01	Digital Data System—Central Office T1WB4 Data-Voice Multiplexer Circuit
		J70177AP	T1WB4 Data-Voice Multiplexer Assembly