

DIGITAL TRANSMISSION SURVEILLANCE SYSTEM

GENERAL DESCRIPTION

DIGITAL DATA SYSTEM

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1. GENERAL

1.01 This section describes the Digital Transmission Surveillance System (DTSS). The DTSS provides the capability of continually gathering performance information on inter-DSA DS-1 facilities of the Digital Data System (DDS). The DTSS remotely monitors, transmits, centrally processes, and retrieves performance data on a digroup basis to identify and localize troubles in each direction of transmission.

1.02 Whenever this section is reissued, the reason(s) for reissue will be given in this paragraph.

1.03 The DTSS, an enhancement to DDS, uses derived 8-kb/s channels for transmitting inter-DSA performance data to a centrally located minicomputer. The data is processed and then dis-

tributed in the form of performance reports over an analog multipoint network.

1.04 The performance reports are automatically transmitted to all DDS centralized test centers (CTC), the Long Lines Network Operating Center (NOC) at Bedminster, New Jersey, Regional Facility Management Centers (RFMC), and appropriate Bell operating company (BOC) locations. The CTCs are responsible for analyzing DTSS performance reports to identify inter-DSA DS-1 performance problems on a real-time basis. Administrative procedures are covered in Section 314-984-101.

2. GLOSSARY OF TERMS

2.01 A listing of some of the more common terms relating to DTSS is presented with a brief description. Refer to Sections 314-900-100 and 660-230-100 for commonly used terms associated with DDS.

8-kb/s SERVICE CHANNEL: The 8-kb/s service channel is derived from the DS-1 signal by using the 191st bit in each 193-bit DS-1 frame. The 191st bit, which is also called the R-bit, is currently unused in the DS-1 signals between T1DMs. Since the DS-1 frame repetition rate is 8000 per second, the derived service channel is 8 kb/s. Also, since the inter-DSA DS-1 facilities are full-duplex, the derived 8-kb/s service channels are also full-duplex.

DIGITAL DATA COMMUNICATIONS MESSAGE PROTOCOL (DDCMP): The DDCMP is the message standard used between the HL95 surveillance unit (SU) and the minicomputer. The DDCMP provides for message synchronization and acknowledgment using message number counters and control messages.

DIGITAL NETWORK ADMINISTRATIVE CENTER (DNAC): The DNAC is the administrative center for DTSS as well as other related digital systems.

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DIGITAL TRANSMISSION SURVEILLANCE SYSTEM (DTSS): An enhancement to the DDS that provides the capability of continually gathering performance information on inter-DSA DS-1 facilities.

MINICOMPUTER: The DTSS minicomputer is a DEC PDP-11/70. Section 314-984-300 covers the software and hardware information related to the DTSS computer operation.

SURVEILLANCE UNIT (HL95 CP): The surveillance unit contains a microprocessor unit that gathers and stores performance data furnished by the HL16B circuit pack (CP). Upon a poll from the minicomputer, the SU transmits the information to the minicomputer. The SU is covered in detail in Part 4.

SU NETWORK ADDRESS: Each SU is assigned an address code. The code allows the minicomputer to identify each SU.

SYNC CIRCUIT (HL16B CP): The sync circuit provides error monitoring of DDS inter-DSA DS-1 facilities and derives an 8-kb/s service channel for the transmission of performance data over existing DS-1 facilities. The HL16B CP is covered in detail in Part 4.

3. FUNCTIONAL DESCRIPTION

A. System Description

3.01 Figure 1 is a typical block diagram of DTSS. The Chicago DSA and DSA #2 each contain an HL95 circuit pack. The incoming DS-1 signal is monitored at each location equipped with an HL95 circuit pack. By having HL95s at the Chicago DSA and DSA #2, the DS-1 signal is monitored in the receive direction by each of the two hub offices. The HL95 in DSA #2 also monitors both directions of the inter-DSA DS-1 facilities between DSA #1 and DSA #2 and DSA #3 and DSA #2.

3.02 There are hub offices not equipped with HL95s, such as DSA #1 and DSA #3 in Fig. 1. Monitoring of the incoming DS-1 signal is provided by equipping these T1DMs with an HL16B in the looped option. This will result in the receive signal (performance data) being looped back to the transmitting T1DMs at DSA #2.

3.03 The performance data for all DS-1 signals received at DSA #2, as well as the performance

data for the looped T1DMs in DSA #1 and DSA #3, are monitored by the HL95 in DSA #2. The performance data for the DS-1 signal received at the Chicago DSA is monitored by the HL95 at the Chicago hub office.

3.04 The performance data is passed between T1DMs and eventually to the minicomputer center via 8-kb/s service channels. The 8-kb/s service channels are an integral part of the inter-DSA DS-1 facilities and are not explicitly shown in Fig. 1. The service channel is derived from the DS-1 signal using the 191st bit in each 193-bit DS-1 frame (see 8-kb/s service channel in Part 2, Glossary of Terms).

3.05 The T1DM uses the DS-1 signal sync word to maintain frame synchronization. It is this basic T1DM process which generates the fundamental signals upon which the performance data is based.

3.06 The 8-kb/s service channels are arranged in the form of multipoint networks emanating from the Chicago hub. Figure 1 would show one such network. The minicomputer polls the HL95s in each performance monitoring location, and the HL95s respond with the performance data. The DDCMP is used for network control (see DDCMP in Part 2, Glossary of Terms).

3.07 The minicomputer processes the performance data and determines the per-route performance levels (see subpart 3B for a description of the performance indications and basic reports that are available). The minicomputer automatically transmits performance reports to designated locations over an analog multipoint network. In addition, the minicomputer has peripheral equipment, such as disc storage and a terminal, for system access and control. Section 314-984-300 covers the minicomputer and associated equipment in detail.

B. Report Capabilities

3.08 The reports generated by DTSS are based on measurements known as DDS performance objectives and DDS performance indicators.

DDS Performance Objectives

3.09 The following inter-DSA DS-1 performance objectives are incorporated into DTSS:

- (1) To experience over each 24-hour day at least 99.75 percent error-free seconds (EFS).
- (2) To experience during each 24-hour day fewer than five 15-minute periods having more than 18 errored seconds.

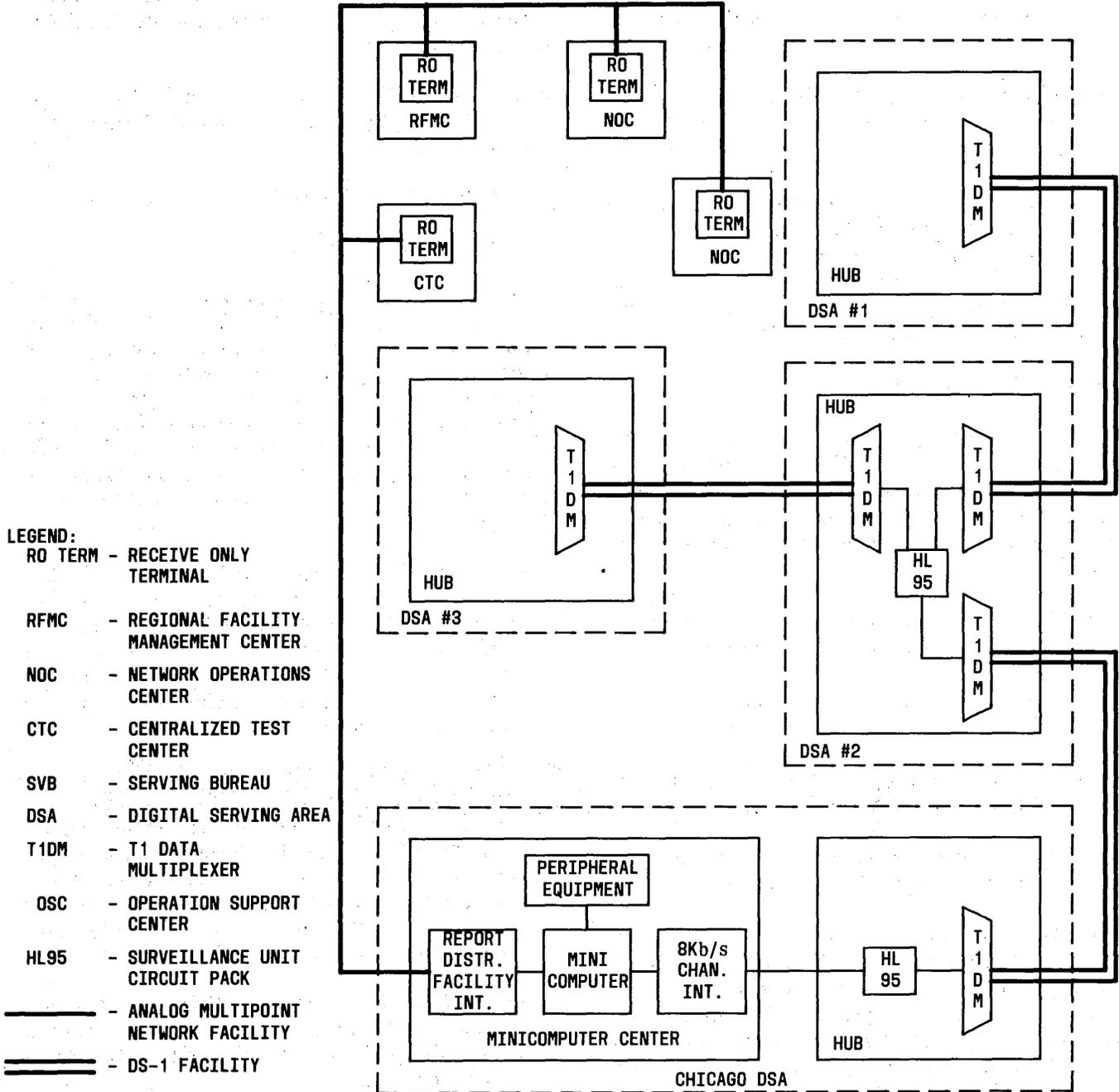


Fig. 1—DTSS Block Diagram

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- (3) To experience during each 24-hour day fewer than two consecutive 15-minute periods with each having more than 90 errored seconds.
- (4) To experience during each 24-hour day fewer than 15 error bursts longer than 100 milliseconds.

The first three objectives were chosen to relate EFS objectives to intervals in which customers have expressed interest and to achieve performance exceeding that which customers describe to be their level of tolerance. The fourth objective was chosen to provide an indication of severe fading activity.

DDS Performance Indicators

3.10 In addition to the DDS performance objectives, performance indicators are generated to alert maintenance forces to potential deficiencies and allow for corrective actions before performance deteriorates to unsatisfactory levels. These indicators are:

- (1) Number of occurrences of more than 18 errored seconds over a 15-minute period
- (2) Number of error bursts longer than 100 milliseconds over a 15-minute period
- (3) Number of error bursts between 2 and 10 milliseconds over a 15-minute period
- (4) Number of error bursts between 11 and 100 milliseconds over a 15-minute period.

3.11 The minicomputer maintains running totals of all performance indicators for each 15-minute period. If more than 18 errored seconds or one or more error bursts longer than 100 milliseconds occur over a DS-1 route during any 15-minute period, the minicomputer will automatically notify the location in control of that route by outputting a summary of performance indicators one through four for that 15-minute period and for each 15-minute period in the previous hour.

Note: These performance measurements are limited to internal Bell System use.

3.12 The DTSS reports are classified as either real-time performance reports or administrative reports. The real-time performance reports are auto-

matically generated whenever a particular limit is reached. Administrative reports are generated either daily, weekly, or monthly.

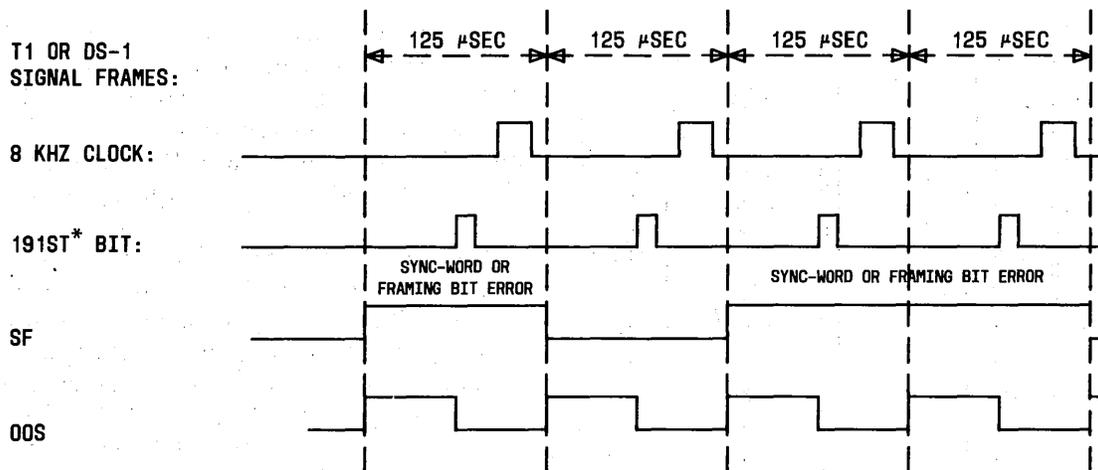
3.13 The DTSS reports are covered in Section 314-984-101. Report distribution and frequency of reports are also covered.

4. HARDWARE DESCRIPTION

A. HL16B Sync Circuit Pack

4.01 The HL16B circuit pack, when substituted for the HL16 circuit pack in the T1DM, derives an 8-kb/s service channel for communicating over the inter-DSA DS-1 facility. It also provides access to a sync circuit which detects an error in the framing pattern to determine that the T1DM is in sync or out of sync. Accordingly, the HL16B is arranged in such a way that the following input and output signals are available. Figure 2 shows the timing for the relevant signals.

- (a) **Output Sync Fail (SF) Signal:** Balanced transmission enables signaling of up to 15 feet in the bay. One polarity denotes the nonerrored condition while the opposite polarity denotes the errored condition. The latter occurs due to a sync-word error. The changes of polarity occur at the boundaries of the 193-bit, DS-1 frames.
- (b) **Output Remote Receive (RR) Signal:** A balanced transmission pair of wires that carries the receiving 8-kb/s service channel signal from the T1DM to the SU. The signal switches polarity at the DS-1 frame boundaries in accordance with the polarity of the 191st bit received during the preceding DS-1 frame. Thus it is the 191st bit held over for one DS-1 frame interval.
- (c) **Output Out-of-Sync (OOS) Signal:** When the T1DM is in the out-of-sync state, a square wave with a period equal to that of the DS-1 frame appears on Test Point 7.
- (d) **Input Remote Transmit (RT) Signal:** A balanced transmission pair of wires that carries the transmitting 8-kb/s service channel signal from the SU to the T1DM. This signal drives the sampling circuit on HL16B which samples the RT signal during the 191st bit for transmission over the DS-1 facility.
- (e) **Input OOS Simulate (OOSS) Signal:** When this input, appearing on Test Point 5, is



* RR LOOPED T1DM → HL-95
 HL95 → MINICOMPUTER
 RT DRIVES SAMPLING FOR HL-16B

Fig. 2—HL16B Timing Signals

grounded at test point 12, a dotting pattern is generated to simulate the out-of-sync state in every other frame. This allows a T1DM to be tested by its associated surveillance unit (HL95) which is described in Paragraph 4.04.

4.02 A switch on the HL16B provides the μ P or the looped mode of operation. In the μ P position, the SF signal is transmitted to the HL95 and the RR and RT (8-kb/s service channel) signals are interconnected to the HL95. The looped position is used when no HL95 is provided locally. Then, the SF signal is interconnected to the RT signal sampling circuit for return transmission over the inter-DSA DS-1 facility.

4.03 Aside from the five input/output signals provided by the HL16B, the operation of the T1DM remains the same as when equipped with an HL16.

B. Surveillance Unit HL95 Circuit Pack

4.04 The HL95 circuit pack is 10.5 inches long by 7.6 inches high by 1.7 inches wide. It consists of component apparatus, mounted on a mother-daughter printed wiring board which is terminated in finger terminals for insertion into three 940A connectors.

4.05 The circuit pack faceplate is shown in Fig. 3.

A solderless terminal cross-connect field is provided on the left side of the faceplate behind a normally-closed metal cover. Access to the cross-connect field is provided by loosening the captive screw located at the top of the cover, thereby allowing cover to pivot downward 180 degrees to its full open position.

4.06 The HL95 surveillance unit circuit pack, as shown in Fig. 4, contains a multiprocessor and the following circuits:

- Twelve access circuits (AC1 through AC4 and AC7 through AC14)
- A broadcast circuit (BR)
- A merging circuit (MG)
- 2 multiplexer circuits (MA and MB)
- 2 demultiplexer circuits (DA and DB)
- A clock circuit (CLC)
- A power circuit (PW).

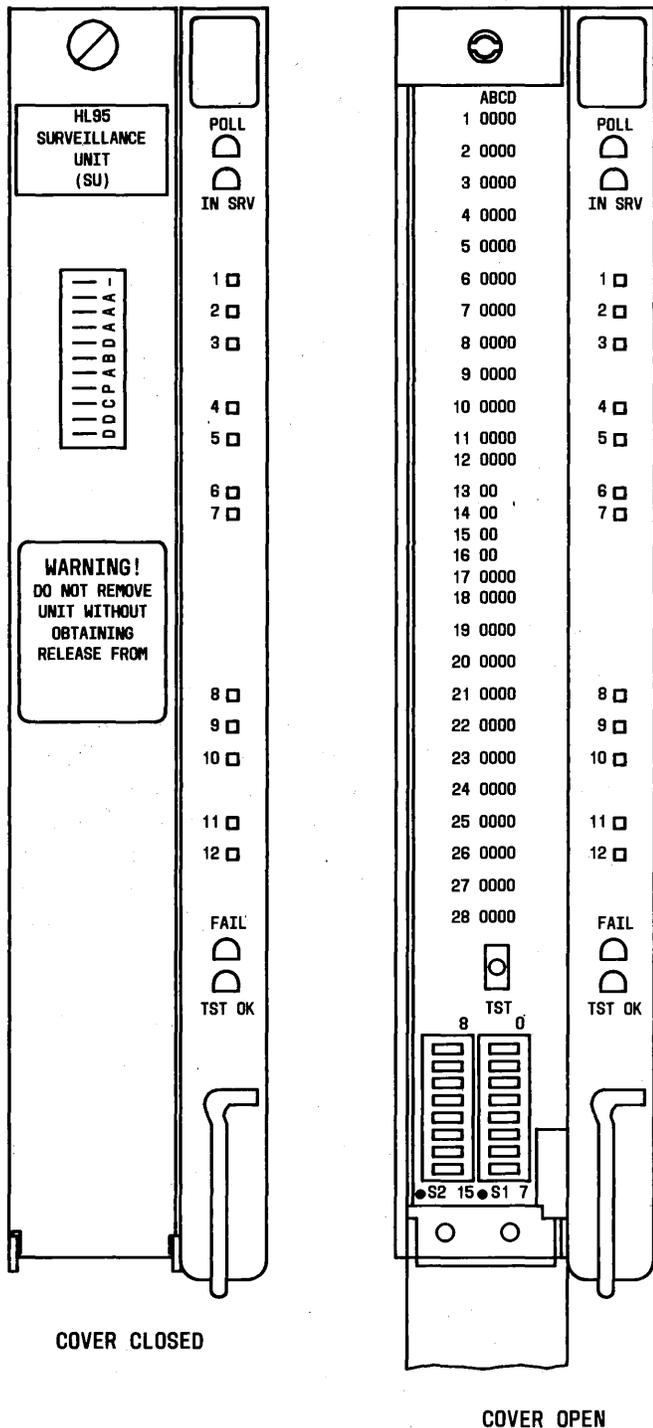


Fig. 3—Front View of CP HL95 Surveillance Unit

Circuits

4.07 Access Circuits (AC): Each of 11 identical access circuits (AC) connect to working T1DMs by four pairs of wires, SF, RR, RT, and SS. The twelfth AC (AC4) connects to the spare T1DM by only three pairs of wires, SF, RR, and RT. The SF, RR, RT, and SS pairs are defined as follows:

- (a) **Sync Fail (SF) Pair:** Each SF pair monitors the state of the incoming sync word signal. After passing through a terminator and switching gates, it is connected permanently to the multiprocessor for analysis. The switching gates are under control of the SS pair. When a working T1DM fails, the spare T1DM takes over and the SF signal from the spare T1DM is routed to the multiprocessor in place of the SF signal originally from the working T1DM.
- (b) **Remote Receive (RR) Pair:** Each RR pair transmits the message carried by the 191st T1 line bit. It may be a DS-1 monitoring signal from a looped T1DM or a message from a distant SU. It passes through a terminator and switching gates (for switching in the spare T1DM, as with the SF signal) and terminates at one of the terminals, R1 through R3 or R7 through R14.
- (c) **Remote Transmit RT Pair:** Each RT pair originates at one of the terminals T1 through T3 or T7 through T14 from which it transmits toward one of the 11 working T1DMs over a balanced pair of wires. In case of a working T1DM failure, the spare T1DM is switched in to accept this signal.
- (d) **Switch Spare (SS) Pair:** Each SS pair originates in a relay on the HL10 (or HL90) circuit pack in one of the working T1DMs. It controls the routing of the SF, RR, and RT signals. In case of working T1DM failure, the relay in HL10 CP causes these signals associated with the protection T1DM to be switched in. For this reason, the SS pair is not needed for the twelfth (protection) T1DM.

4.08 Broadcast Circuit (BR): The broadcast circuit has its input wired to terminal BI, 15 outputs wired to terminals B01 through B015, and the sixteenth output permanently connected to the SI input of the multiprocessor. This circuit broadcasts the messages which come from the minicomputer to

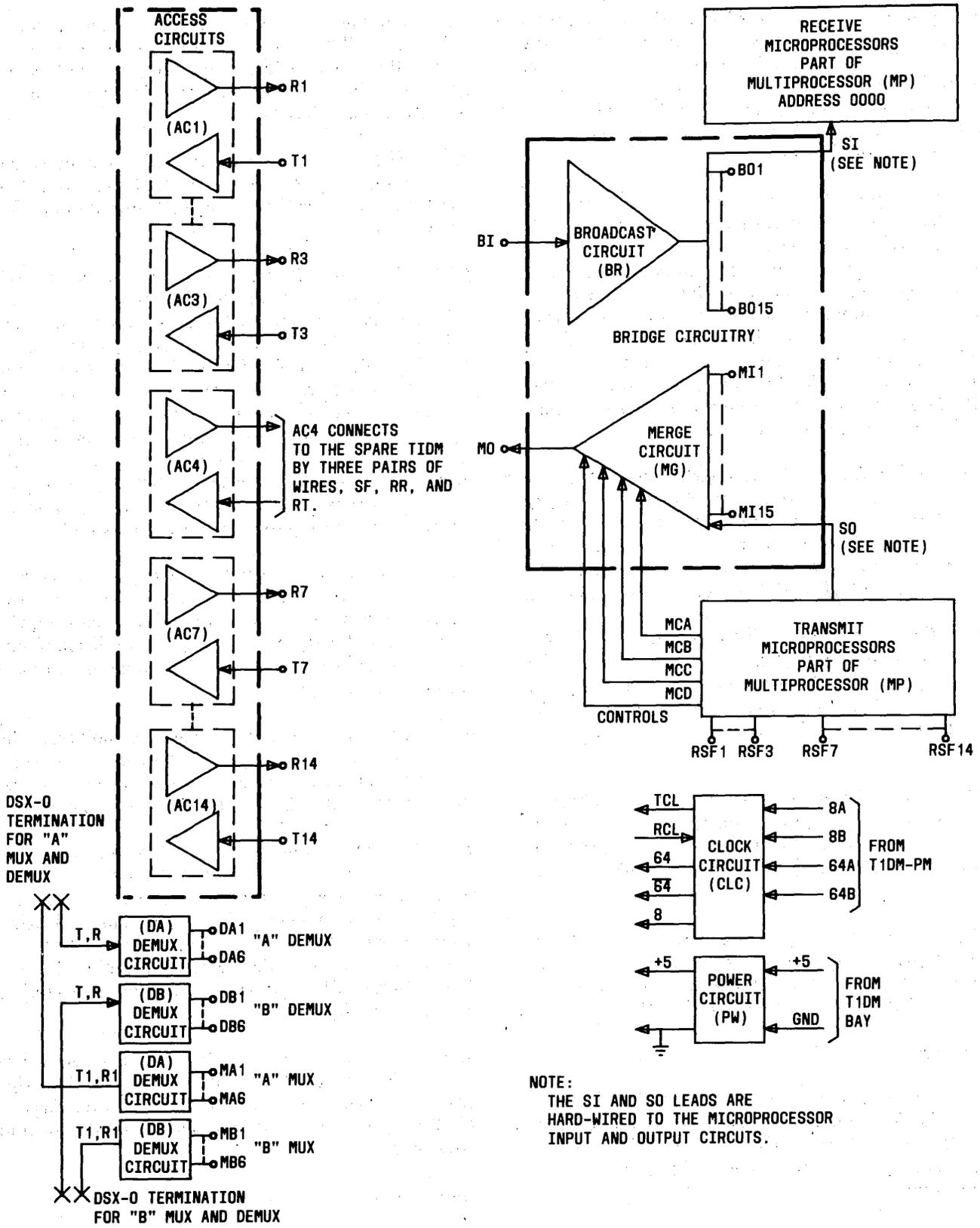


Fig. 4—Simplified Block Diagram of HL95 Surveillance Unit Circuit Pack

the multiprocessors in the system. The BI terminal can be cross-connected to any R terminal or to any DA or DB terminal. B01 through B03 and B07 through B014 are reserved for cross-connection to terminals T1 through T3 and T7 through T14, respectively. B04 through B06 and B015 can be cross-connected to any MA or MB terminal.

4.09 Merging Circuit (MG): The merging circuit provides for transmission in the opposite direction from that of the broadcast circuit. This circuit is under the control of the multiprocessor and allows only one transmission path to be active at any time. This eliminates interference in the event that more than one message is being sent toward the minicomputer at any time or if there is noise on another channel. The MI terminals are always paired with their correspondingly numbered BO terminals and are cross-connected as such.

4.10 Multiplexer Circuits (MA and MB): The 2 multiplexer circuits provide for twelve 8-kb/s channels to be multiplexed onto two 64-kb/s channels for communication with two other bays. The inputs appear on terminals MA1 through MA6 and MB1 through MB6 of the faceplate cross-connect.

4.11 Demultiplexer Circuits (DA and DB): The two demultiplexer circuits provide for demultiplexing two 64-kb/s channels from two other bays. The 12 outputs appear on terminals DA1 through DA6 and DB1 through DB6 of the faceplate cross-connect.

4.12 Clock Circuit (CLC): The clock circuit generates the required timing signals. The SU operation is based on DS0 timing. Therefore, the four timing signals are 8 kHz "A" and "B"; 64 kHz "A" and "B."

4.13 Power Circuit (PW): The power circuit provides the necessary filtering for protection of the HL96. The actual power is supplied by the power unit in the protection T1DM shelf.

Multiprocessor

4.14 The multi-microprocessors circuitry shown in Fig. 5 is a microprocessor circuit arrangement for collecting and analyzing data from DS-1 facilities and handling communications with a centralized minicomputer.

4.15 The multi-microprocessors provide 11 inputs that are permanently connected to the SF sig-

nals from the 11 T1DMs in the bay, LSF1 through LSF3 and LSF7 through LSF14; 11 other inputs are optionally wired to terminals RSF1 through RSF3 and RSF7 through RSF14 to provide monitoring inputs for looped T1DMs.

4.16 The multiprocessor is divided into a main processor portion with attendant peripheral devices and four self-contained SF-event-collection processors.

4.17 The SF-event-collection processors sample the LSF and RSF inputs, determine whether an SF error has occurred within a 1-millisecond interval, and tabulate the total number of SF events for each direction of transmission which have occurred. This data is transferred to the main processor random access memory (RAM) via direct memory access (DMA). The main processor then sorts SF errors into various categories. The messages formed in the main processor are composed of error statistics belonging to the SF inputs. These messages are then transmitted to the minicomputer when the SU is polled.

4.18 Input SI and output SO are the receive and transmit data leads that interconnect the multiprocessor to the communication circuit via the broadcast and merging circuits. Four additional output leads are used to control the transmission path through the merging circuit.

4.19 The main processor decodes each poll from the minicomputer and opens the appropriate transmission paths in the merging circuit for responses from other SUs or for its own response.

4.20 The main processor circuit arrangement has a typical input/output (I/O) bus configuration. Programs are stored in electrically programmable read-only memory (EPROM). Communication protocol with the minicomputer is handled with a communication controller device. A peripheral interface adapter (PIA) is used to control the external merging circuit.

4.21 The four SF-event-collection processors are microprocessor, PROM, RAM, and I/O configurations, all contained on a single integrated circuit. All four processors are identical in hardware and program.

Cross-Connect Terminal Field

4.22 The cross-connect terminal field (see Fig. 3) provides two 8-position switches and an array

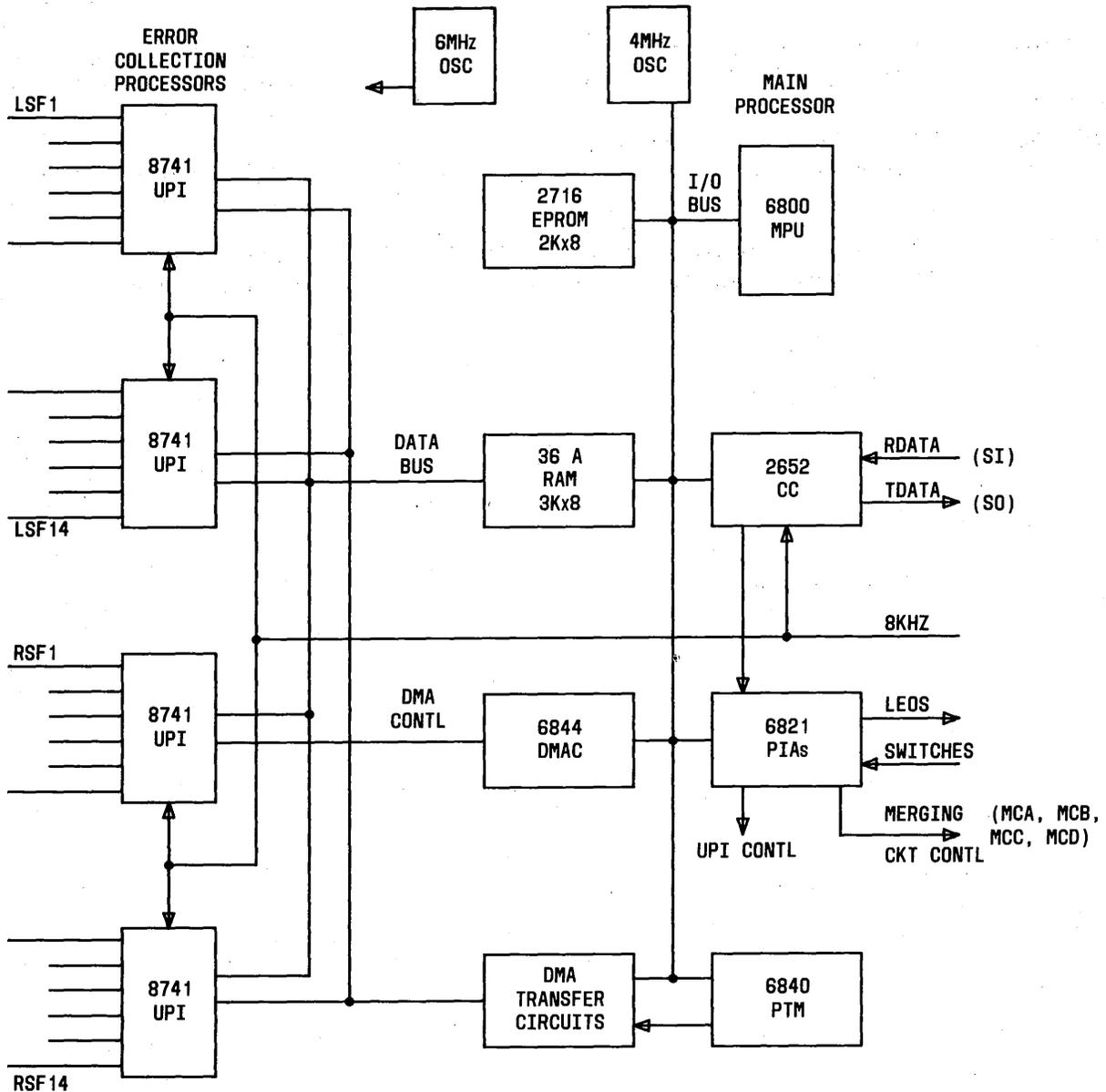


Fig. 5—Multiprocessor Circuitry

of solderless terminals on 0.250-inch centers. The switches are utilized to set the 16-bit hexadecimal coded address associated with the SU. The solderless cross-connect field provides a flexible means of configuring (or reconfiguring) an SU with regard to its particular functional application in the monitoring system. The strapping procedure is covered in Section 314-984-200.

5. REFERENCES

- 5.01 The following sections provide additional information on equipment and functions of DDS and DTSS.

SECTION 314-984-100

SECTION	DESCRIPTION	SECTION	DESCRIPTION
314-900-100	Private Line Service—Overall Description—Digital Data System	314-984-200	DTSS—Circuit Pack Installation and Test Procedures—Digital Data System
314-912-100	T1 Data Multiplexer—Description—Digital Data System	314-984-300	DTSS—Central Processor and Description—Digital Data System
314-984-101	DTSS—Administrative Procedures—Digital Data System	660-230-100	Administrative Procedures—Digital Data System