LMX TERMINALS

LMX-1

CARRIER AND PILOT SUPPLY

PILOT COMBINING CIRCUITS

SIX-FREQUENCY OR TWO-FREQUENCY COMBINING CIRCUIT OUTPUT

This section provides the procedures for measuring and adjusting the pilot combining circuit outputs. The pilot combining circuit is shown in Fig. 1. The tests of Section 356-175-501 should be conducted prior to these tests.

This section is reissued to simplify patching procedures in order to maintain switching capabilities of multiline and expanded multiline systems.

Since this revision is of a general nature, arrows ordinarily used to indicate changes have been omitted. ***Equipment Test Lists are not affected.***

These tests should ***not*** be conducted while a protection line switch is in effect.

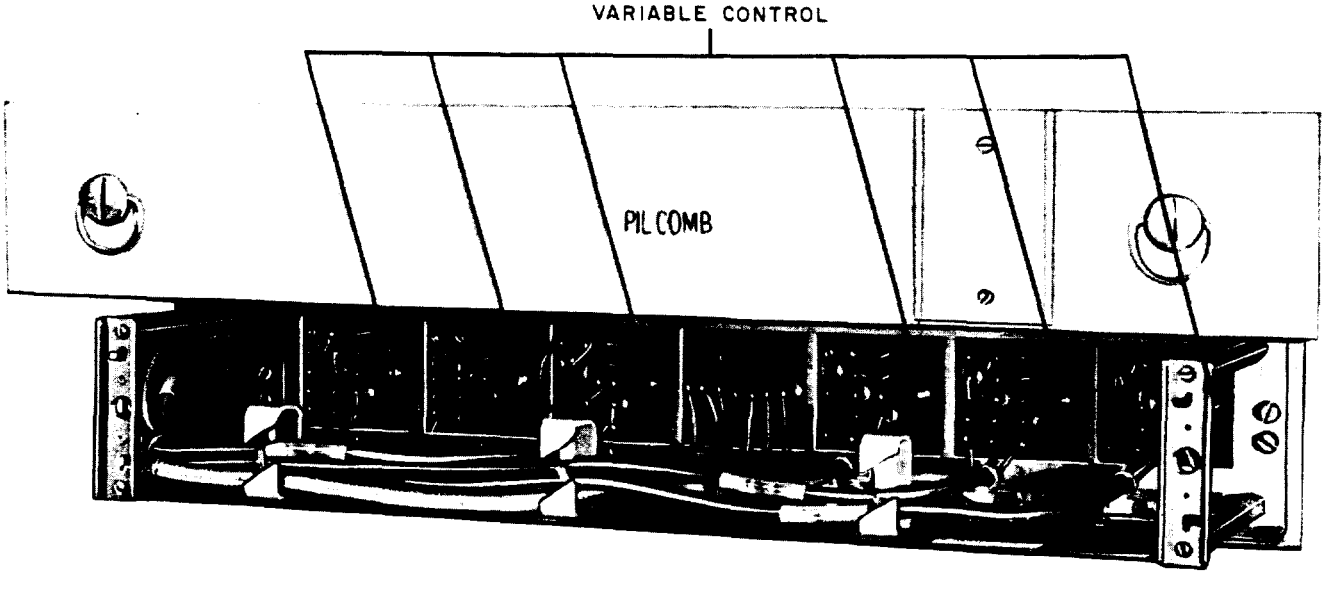


Fig. 1—Pilot Combining Circuit (With and Without Cover)

APPARATUS

Receiving Test Equipment (RTE) (Section 356-010-500) having the following characteristics:

Frequency: 308 to 8320 kHz

Power: −46.80 to −70.00 dBm

Impedance: 75 ohms

2—***P2BJ cords***

STEP	PROCEDURE

Caution: It is important that the number of transfers of the pilot supply and of the combining circuit be kept to a minimum to avoid hits on data and carrier telegraph service.

Note 1: Power readings shall be obtained with all panel covers in place.

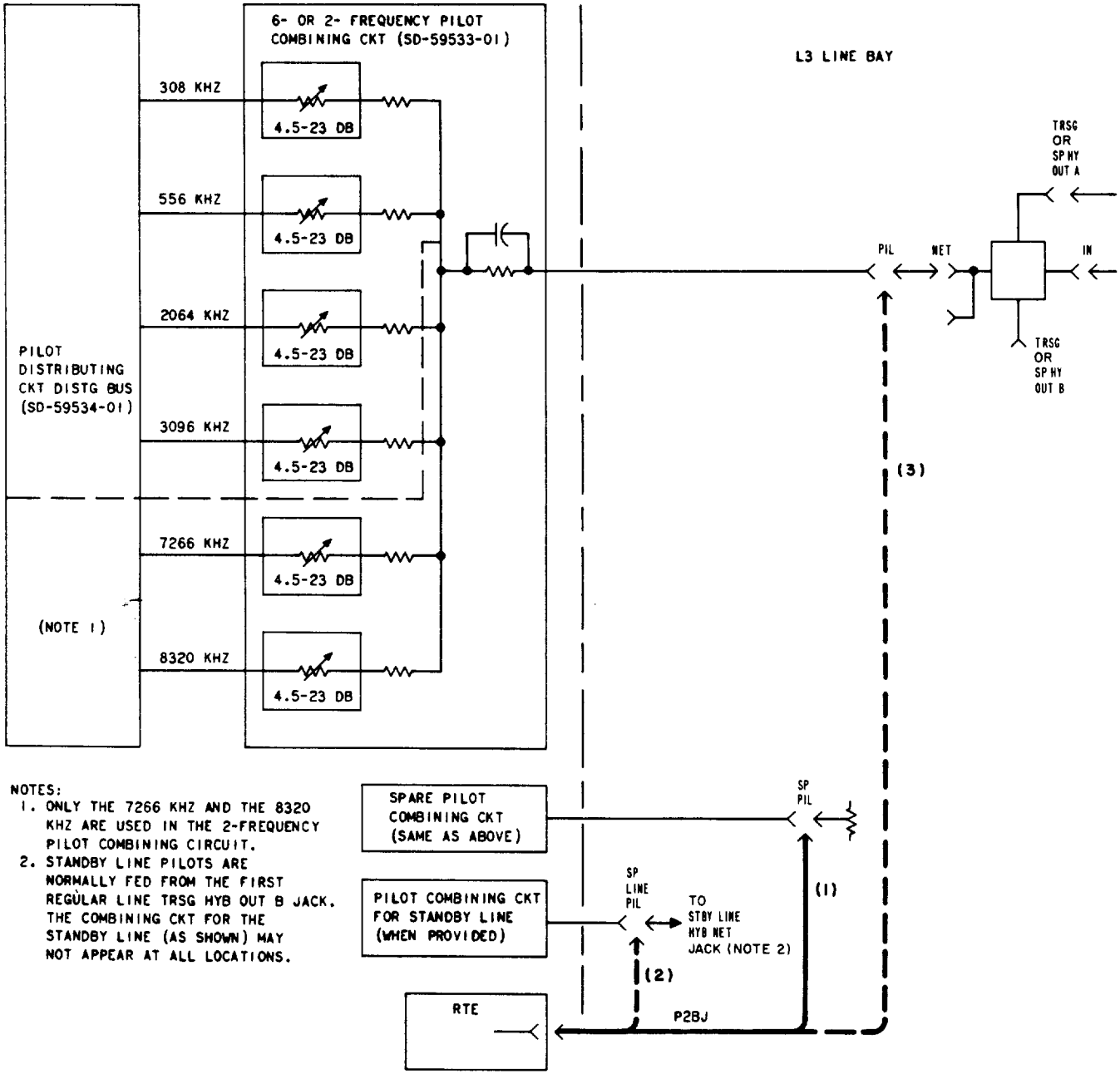
Note 2: Pilots can be measured only at a PIL jack that is not patched to a transmitting hybrid NET jack if protection switching capabilities are to be maintained during the tests and adjustments. Since each transmitting hybrid is fed from a separate pilot combining circuit and the pilots of each combining circuit are adjusted individually, they must ***all*** be adjusted to the proper level or the patching flexibility and the standby line reliability desired may be sacrificed. This test procedure can be performed only at a PIL jack of a spare pilot combining circuit or one which has been taken ***out of service.***

1 Calibrate the RTE for a 75-ohm terminated measurement at the frequency being measured. (See Table A.)

TABLE A

PILOT FREQUENCY (kHz)	POWER AT PIL JACK (dBm)
308	−66.80
556	−66.80
2064	−66.80
3096	−66.80
7266	−46.80
8320	−56.80

STEP	PROCEDURE
2	Where both regular and emergency pilot generators are provided, set the MAN CON switch on all pilot and control panels to REG.
3	Make patch (1), Fig. 2.
4	Measure the level received for each of the frequencies given in Table A. Adjust the variable control (on the pilot combining circuit under test) associated with the frequency being measured, to the power given in Table A.
5	If the requirements of Step 4 are met, proceed to Step 7; if the requirements are ***not*** met, perform the tests outlined in Section 356-175-501 or 356-180-501, as applicable, before proceeding to Step 6.
6	For each frequency ***not*** meeting the requirements of Table A through adjustment, set the variable control of the combining circuit under test to midrange and strap the fixed pads to the value in Table A $\pm$0.12 dB as measured at the PIL jack. (See SD-59533-01 for strapping arrangements.) Then reconduct Steps 3, 4, and 5 before proceeding to Step 7.
7	If both regular and emergency pilot generators are provided, turn all pilot frequency MAN CON switches to EM.
8	Reconduct Step 3 and then proceed to Step 9.
9	Adjust the OUTPUT controls on the various emergency pilot generators until the power output levels are within $\pm$0.01 dB of the values measured in Step 4.
10	Turn the pilot frequency MAN CON switches to NORM.
11	Remove all test connections and restore unit under test to normal. If a separate pilot combining circuit is provided to supply pilots for the standby line, proceed to Step 12. If the standby line receives pilots from the first regular line or in 2-line switching systems, proceed to Step 16.
12	Read this entire step before proceeding with (a) and (b). (a) Patch a P2BJ cord from the SP PIL jack of the spare pilot combining circuit to the TRSG HY NET MULT jack of the standby line. (See Fig. 3.) (b) Remove the 372A plug from between the PIL and TRSG HY NET jacks of the pilot combining circuit normally supplying the standby line pilots. ***Note:*** (a) and (b) should be conducted as simultaneously as possible to reduce "bump" time to a minimum.
13	Conduct Steps 1 through 10, ***omitting Step 3,*** for the combining circuit patched out [patch (2), Fig. 2] and then proceed to Step 14 to restore pilot feed to normal.
14	Read this entire step before proceeding with (a) and (b).



NOTES:
1. ONLY THE 7266 KHZ AND THE 8320 KHZ ARE USED IN THE 2-FREQUENCY PILOT COMBINING CIRCUIT.
2. STANDBY LINE PILOTS ARE NORMALLY FED FROM THE FIRST REGULAR LINE TRSG HYB OUT B JACK. THE COMBINING CKT FOR THE STANDBY LINE (AS SHOWN) MAY NOT APPEAR AT ALL LOCATIONS.

Fig. 2—Pilot Combining Circuit—Output Measurements

STEP	PROCEDURE

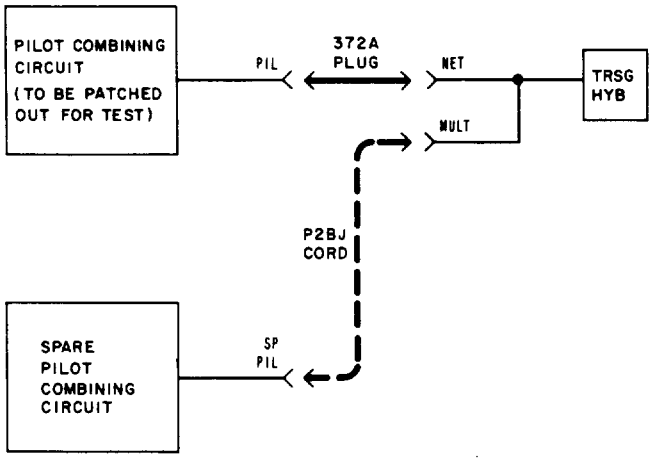


Fig. 3—Patching Procedure to Remove Pilot Combining Circuit from Service

(a) Patch a 372A plug between the PIL and TRSG HY NET jacks of the pilot combining circuit normally supplying the standby line pilots. (See Fig. 3).

(b) Remove the P2BJ cord inserted in Step 12(a).

Note: (a) and (b) should be conducted as simultaneously as possible to reduce "bump" time to a minimum.

15 Remove all test connections and restore unit under test to normal.

16 Read this entire step before proceeding.

(a) Establish a LOCK NORMAL condition for the standby (protection) line.

(b) Patch a P2BJ cord from the SP PIL jack of the spare pilot combining circuit to the TRSG HY NET MULT jack of the regular line under test, pilot combining circuit. (See Fig. 3.)

(c) Remove the 372A plug from between the PIL and TRSG HY NET jacks of the regular line under test.

STEP	PROCEDURE
	Note: (b) and (c) should be conducted as simultaneously as possible to reduce "bump" time to a minimum.
	(d) Release the LOCK NORMAL condition.
17	Conduct Steps 1 through 10, ***omitting Step 3,*** for the regular line pilot combining circuit under test [patch (3), Fig. 2] and then proceed to Step 18 to restore pilot feed to normal.
18	Read this entire step before proceeding.
	(a) Establish a LOCK NORMAL condition for the standby (protection) line.
	(b) Replace the 372A plug removed in Step 16(c). (See Fig. 3.)
	(c) Remove the patch made in Step 16(b).
	Note: (b) and (c) should be conducted as simultaneously as possible to reduce "bump" time to a minimum.
	(d) Release the LOCK NORMAL condition.
19	Remove all test connections and restore unit under test to normal.
20	Repeat Steps 16 through 19 for all regular line pilot combining circuits not tested.