

N3 CARRIER TELEPHONE SYSTEM FREQUENCY CORRECTION UNIT DESCRIPTION

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unit. Since this reissue is a general revision, no revision arrows have been used to denote significant changes. The Equipment Test List is not affected.

A. Function of Frequency Correction Unit (FCU)

1.03 A complete terminal for the N3 Carrier System consists of 24 channels (two channel groups). One FCU is required in each channel group. Both FCUs are identical except for specific filters and inductors and they are not interchangeable between channel groups. Each FCU (Fig. 1) is a single plug-in assembly providing a circuit that corrects the frequency of the received carrier frequency signal of each channel group.

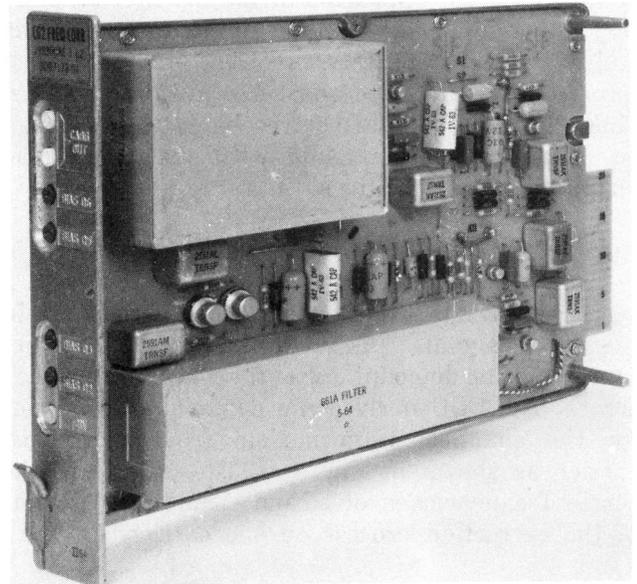


Fig. 1—Frequency Correction Unit (J99300AE)

1. GENERAL

- 1.01 This section describes the J99300AE frequency correction unit (FCU) used in N3 terminals.
- 1.02 This section is reissued to update the procedure for J99300AE frequency correction

NOTICE

Not for use or disclosure outside the
Bell System except under written agreement

1.04 Circuit components are mounted on a printed circuit board that is contained in a die-cast metal frame. All interconnecting wiring to and from the FCU enters the rear of the assembly via a 20-pin plug that is part of the printed circuit board. Seven pin jacks for testing and a mechanical latch for locking the unit in position are located on the front panel.

B. General Characteristics of Circuit

1.05 In the N-type carrier system, "frequency frogging" is used in repeaters in order to provide some self-equalization of signals transmitted over cable and to block crosstalk paths. Frequency frogging is a method whereby low frequencies fed into a repeater are retransmitted as high frequencies by a low-high repeater and vice versa for a high-low repeater. To accomplish this, the N-type repeater is equipped with a local 304-kHz oscillator to provide the modulating carrier for the frogging function.

1.06 As a result of temperature variations and aging effects, the 304-kHz oscillator can be off in frequency. This causes a frequency error in all the signals appearing at the repeater outputs. Depending upon a number of factors, eg, the multiplicity of repeaters involved, this frequency error could accumulate and be as much as 100 Hz. Thus, the line signal at the receiving terminal may be offset by this amount with respect to the terminal bandpass filters.

1.07 To correct this problem, the demodulator in the channel group unit is supplied with a carrier that has the same frequency error as in the input signal. As a result, the two errors cancel and the demodulator output has no frequency error. The FCU derives the demodulating carrier for the channel group modem from a received carrier as shown in Fig. 2. Also shown are the carrier frequencies involved and a sample illustration of the correction process on one carrier.

2. CIRCUITS

A. General

2.01 The frequency correction unit consists of two transistor amplifiers, one narrowband crystal filter, one wideband inductance-capacitance filter, and a double-balanced 2-transistor modulator. The function of this circuitry, a simplified version of which is shown in Fig. 3, is to derive a

demodulating carrier having the frequency error of the received channel group signals. The description of operation is as follows. A narrowband crystal pick-off filter FL1 picks off a selected channel carrier frequency from the input to the channel group modem unit; 112 kHz is channel group 1 and 80 kHz is channel group 2. Both of these frequencies will include the frequency error accumulated due to variations of the 304-kHz oscillators in the N carrier line repeaters.

2.02 This picked off carrier is amplified by the 3-stage amplifier consisting of transistors Q1, Q2, and Q3 and associated circuitry. The amplifier has 50 dB of forward gain and approximately 30 dB of negative feedback. The signal is then fed to the transistor-switch modulator made up of double-unit transistor Q4 and transformers T3 and T4. In this circuit, the carrier is modulated with a signal from the N3 carrier-frequency supply, closely controlled in amplitude and frequency, which is either 168 kHz (for group 1) or 152 kHz (for group 2). The wanted sum product from the modulator is selected by filter FL2. For group 1, this frequency will be 280 kHz plus the line shift error and, for group 2, it will be 232 kHz plus the line shift error.

2.03 The second amplifier, a 2-stage unit with 35 dB of forward gain and approximately 20 dB of negative feedback, amplifies this selected output and feeds it to the carrier leg of the assigned channel group demodulator. The incoming channel group signal (carrier and channel sidebands) feeds into the signal leg of this same channel group demodulator. As previously stated, both the incoming signal and the carrier output from the frequency correction unit derived from it are all shifted in frequency by the same number of Hz. The lower sideband output of the channel group demodulator (the difference between the input signals) is the desired output without frequency error due to cancellation of the line shift error. For example, a channel carrier frequency from the line of 120 kHz plus 8 Hz (error) when demodulated against the output of the frequency correction unit of 280 kHz plus 8 Hz (error) produces a lower sideband (difference) frequency of 160 kHz (280 kHz plus 8 Hz minus 120 kHz plus 8 Hz equals 160 kHz) or an exact corrected carrier frequency. No correction is provided or is necessary in the frequency correction unit for the possible small error introduced by any frequency error in the common carrier

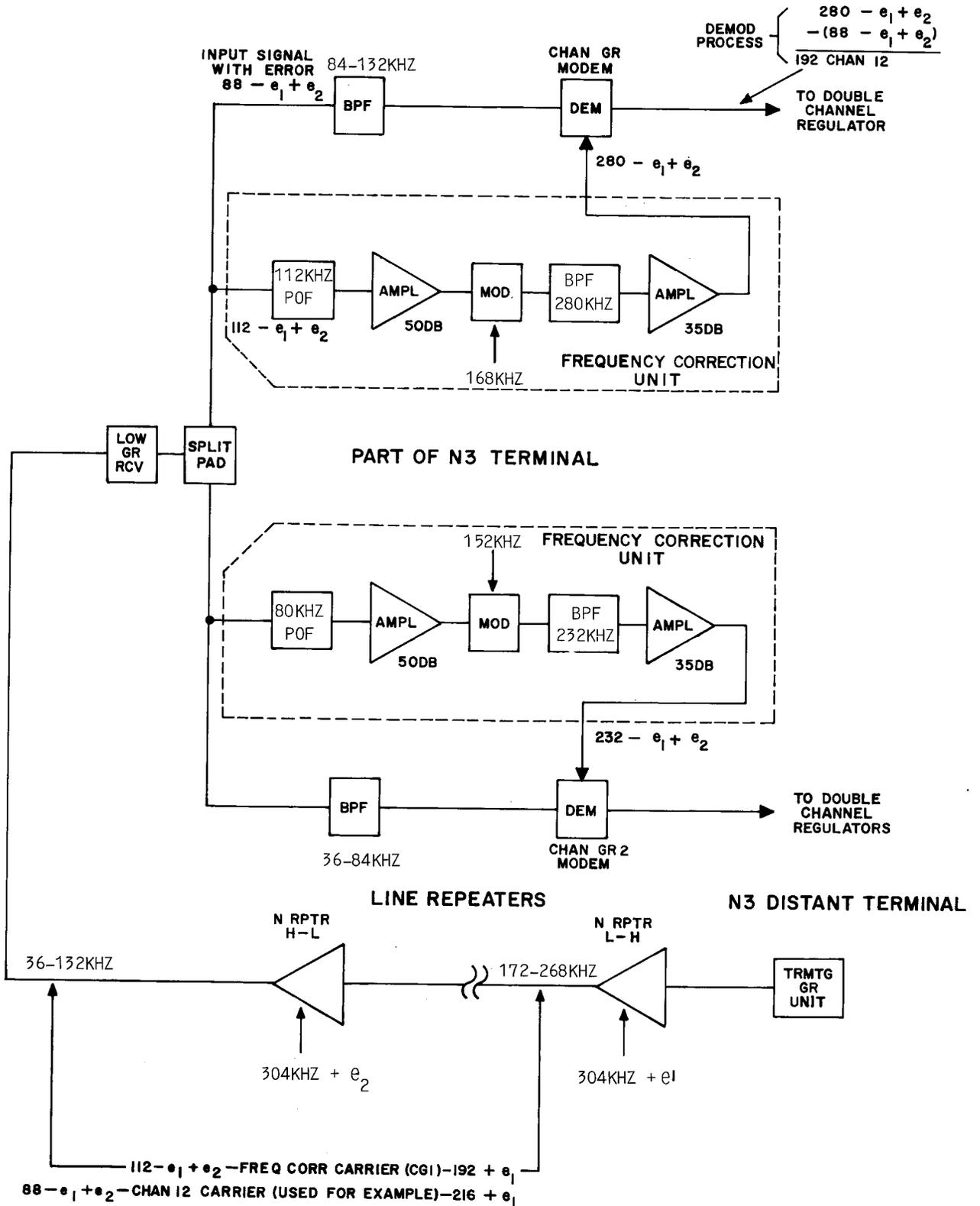


Fig. 2—Application of Frequency Correction Unit (J99300AE)

supply that feeds 168 or 152 kHz to the frequency correction circuit.

2.04 In addition to correcting the frequency error, a degree of amplitude regulation of the demodulating carrier output is provided by feeding the "signal" input to the modulator of the frequency correction unit from the common carrier supply and driving the "carrier" input to the modulator with a picked off signal which has been amplified sufficiently to properly switch the modulator transistors over a wide range of received carrier levels.

3. DETAILED CIRCUIT DESCRIPTION

A. Filters

Input

3.01 In order to generate a frequency shifted demodulating carrier, it is first necessary to select a line carrier that contains the line frequency error. This selection is accomplished by using a narrowband crystal filter. The passband of this filter (FL1 in Fig. 3) is approximately ± 100 Hz from nominal, with discrimination at ± 200 Hz of not less than 30 dB. The balanced input impedance of the filter is 13,000 ohms introducing negligible bridging loss and the output is 135 ohms to match the input impedance of the first amplifier.

3.02 There are two filters, a separate code each channel group, having identical attenuation characteristics, as shown in Fig. 4. The 112-kHz filter is for channel group 1 and the 80-kHz filter is for channel group 2.

Output

3.03 The filter at the output of the modulator must pass the desired upper sideband and reject all other unwanted modulation products. Products from the channel group 1 frequency correction unit modulator fall at 56-kHz intervals and from the group 2 modulator at 8-kHz intervals. Therefore, in each case, maximum filter suppression requirements exist at each of these frequency intervals from the wanted output frequency. As with the input filters, two different passbands are required for this filter centered at 280 kHz for channel group 1 and 232 kHz for channel group 2.

3.04 The basic filter circuit has a 300-ohm unbalanced input and 135-ohm unbalanced output. The internal structure consists of tunable inductors and fixed capacitors arranged to form two full image peak sections and one and one-half constant "k" image sections. The attenuation characteristics for these two filters are shown in Fig. 5 and 6.

B. Amplifiers

Carrier Amplifier

3.05 This amplifier is designed to amplify the low-level carrier received from the line via the input filter and produce a voltage sufficient to drive the transistor modulator.

3.06 The amplifier circuit consists of three common-emitter transistor stages. As shown in Fig. 3, a simplified sketch of the amplifier circuitry, the first two stages are direct coupled and the third is ac coupled. The input transformer T1 provides an impedance match between the 135-ohm midband impedance of pick-off filter FL1 and the nominal input impedance of transistor Q1. In addition to providing part of the dc circuitry, emitter resistors R4 and R9 (see Fig. 3) provide local series feedback in the second and third stages, respectively. In addition to this local feedback in the form of unbypassed emitter resistance, negative feedback is provided by the use of high-side hybrid feedback at both the input and output. This feedback is formed by the feeding back of part of the output voltage to the input via the divider formed by the tapped windings of the output and input transformer. Resistors R14, R15, and R16 plus the hybrid loss of each transformer provide loop feedback circuit loss to establish a nominal amplifier gain of 50 dB for closed loop operation. Fig. 7 shows typical open and closed loop transmission characteristics. Since the same amplifier circuit is used in both channel group frequency correction units, the gain-frequency response should be flat over the 80- through 112-kHz range. For more general application at some possible future date, the amplifier has been designed to have a much wider response characteristic than necessary. As shown in Fig. 7, the gain characteristic is virtually flat over the N carrier band of 36 through 268 kHz.

3.07 Capacitors C1, C3, and C7 and resistor R1 provide high-frequency shaping to ensure

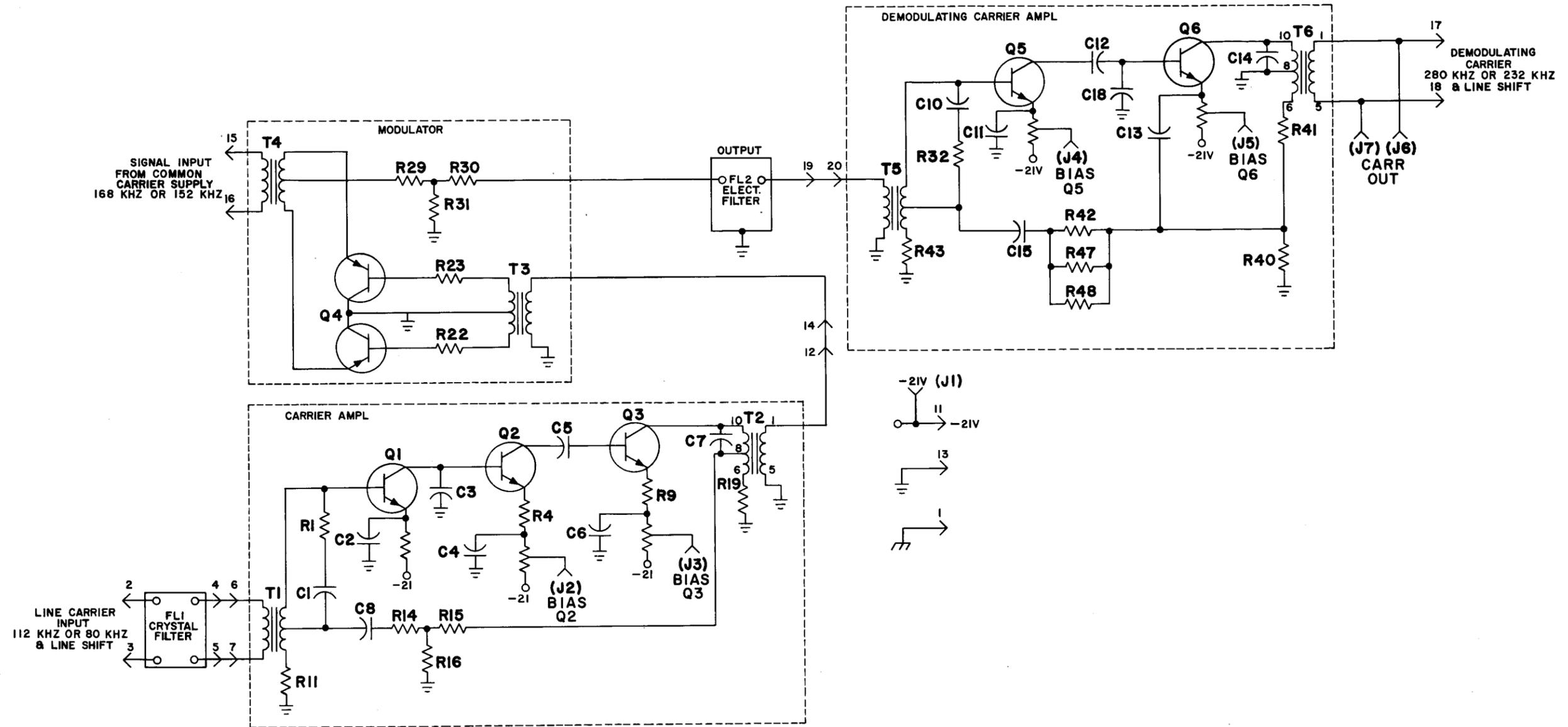


Fig. 3—Frequency Correction Unit (J99300AE)

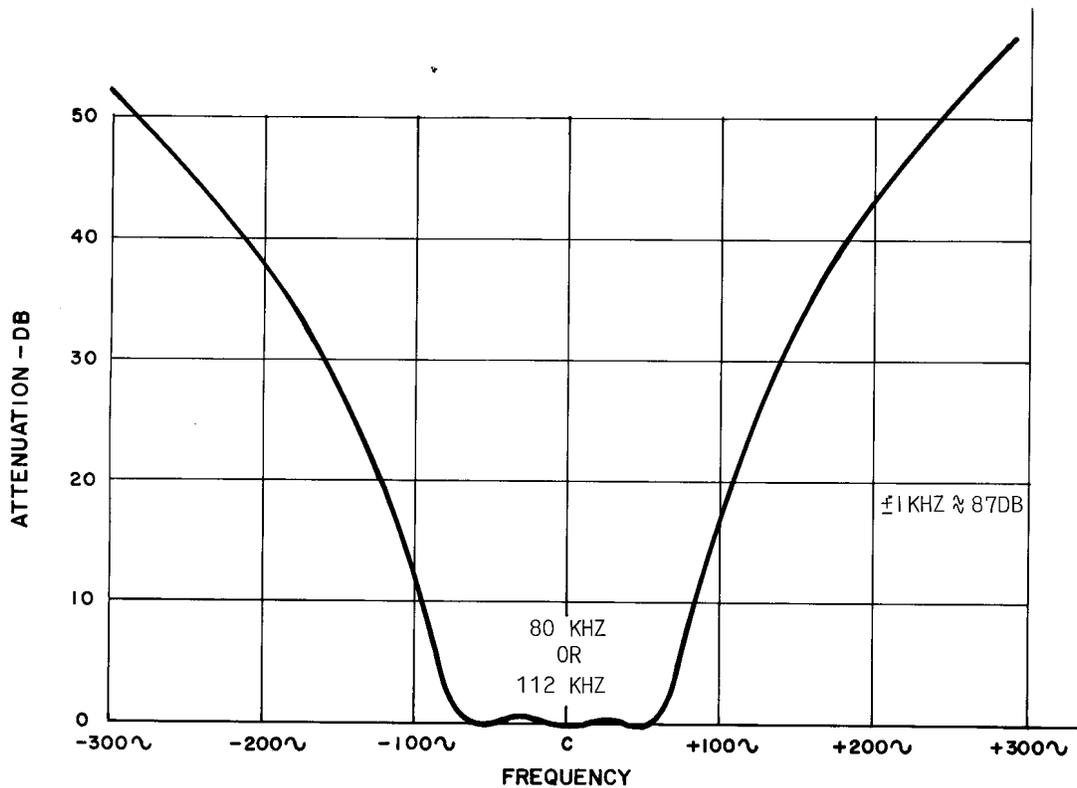


Fig. 4—Attenuation Characteristic of Frequency Correction Circuit (J99300AE) Pick-off Filters

phase and gain margin against singing around the feedback loop. Figures 8A and 8B illustrate the mu-beta phase and gain characteristic above the band for two different terminations. The below band mu-beta gain characteristic is shown in Fig. 9. At gain crossover, there is phase margin of approximately 50 degrees as calculated from the shape of the gain characteristic about the point mu-beta equals zero. Capacitors C2, C4, C5, and C8 and associated circuit resistances, both external and internal to the transistors, are the main contributors to the low-end cutoff.

3.08 The amplifier is designed to have a maximum output power of +15 dBm with the nominal supply voltage of 21 volts. Figure 10 shows the output overload characteristic. Pin jacks on the front panel of the unit designated BIAS Q2 and BIAS Q3 are provided to measure voltages representative of the emitter current of transistors Q2 and Q3. All measurements at bias test points of this circuit are nominally 3 volts for 21-volt supply voltage.

Demodulating Carrier Amplifier

3.09 The demodulating amplifier provides approximately 35 dB of gain to the frequency shifted demodulating carrier received from the modulator output filter. This carrier is delivered to the channel group demodulator at a nominal power of +3.0 dBm. The output may depart from +3.0 dBm as much as +1.2, -1.7 dB due to the adjustment variations in the secondary carrier distribution panel which supplies the "signal" input to the frequency correction unit modulator and allowable tolerances on circuit components.

3.10 The demodulating carrier amplifier, as shown in Fig. 3, consists of two ac coupled common-emitter stages. The primary winding of transformer T5, when the secondary is properly terminated, provides a 135-ohm impedance to match the output impedance of filter FL2; the secondary matches the nominal input impedance of transistor Q5. Two types of feedback are incorporated in this circuit. Local series connected feedback at the output stage reduces the overall amplifier loop

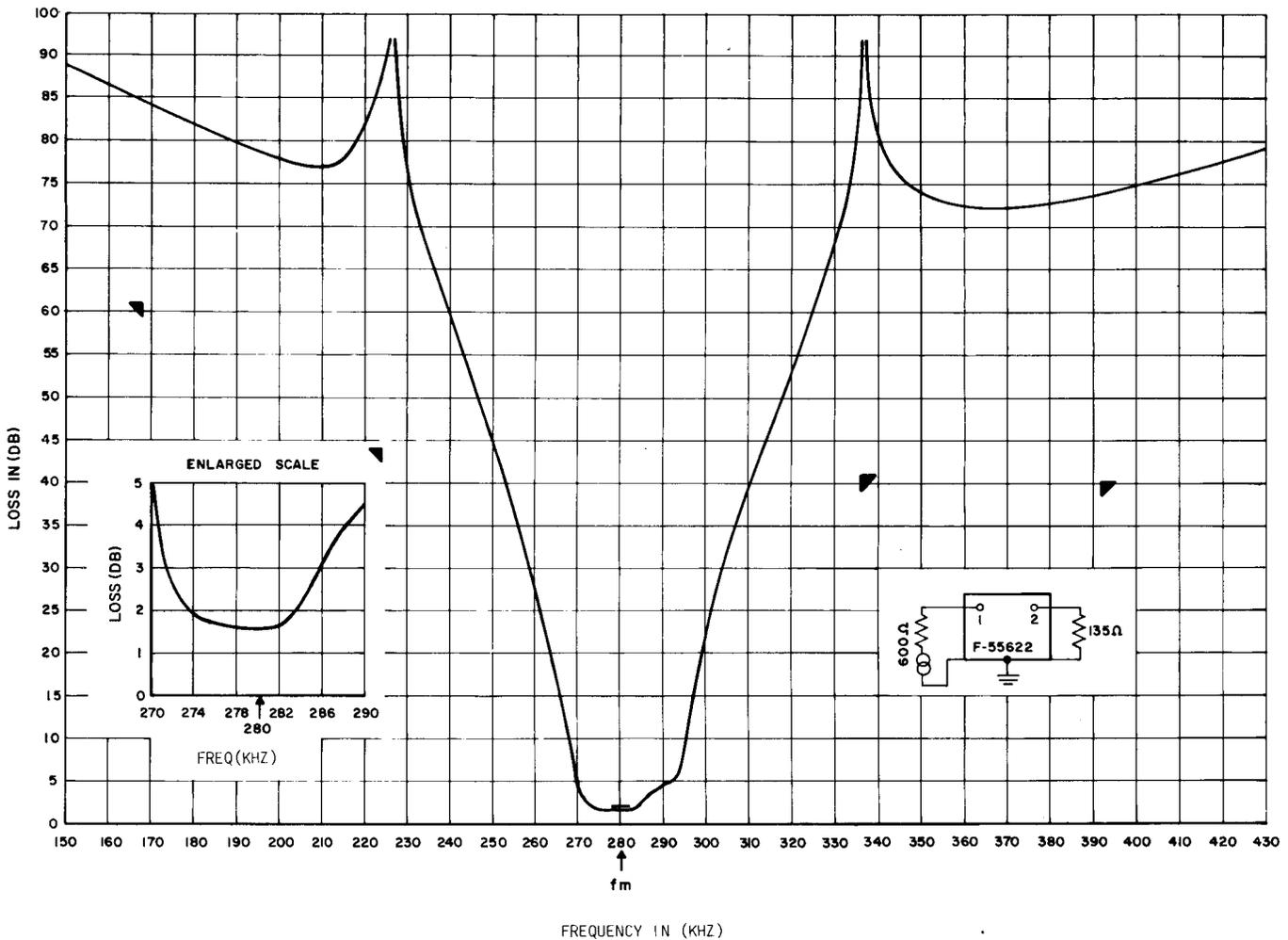


Fig. 5—Frequency Correction Circuit (J99300AE)—Output Filter for Channel Group 1 (280 kHz)

gain which, in turn, reduces the difficulty of controlling the overall mu-beta characteristic. An added advantage of local feedback at the output stage is the retention of the effect of the feedback on the modulation performance of the circuit. The amount of this local feedback is determined by resistors R40, R41, and R42 and winding (6-8) of transformer T6.

3.11 Loop negative feedback is provided through high-side hybrid feedback connections at both input and output transformers. Resistors R42, R47, and R48 also provide beta circuit loss which, added to the hybrid loss, determines the closed-loop amplifier gain. Shaping of the high-frequency end mu-beta characteristic is provided by capacitors C10, C14, and C18 and resistor R32.

Low-frequency end control is primarily due to capacitors C11, C12, and C15. As indicated in Fig. 11A and 11B, sufficient phase and gain margins exist at the high-frequency end with either a resistive termination at the input or the actual modulator and filter termination. For the low-frequency end, only the magnitude of mu-beta is shown in Fig. 12. However, with the slope as shown, approximately 65 degrees of margin is indicated at gain crossover (see Fig. 12).

3.12 The amplifier is designed to operate at 232 and 280 kHz; however, the gain-frequency response with the feedback loop closed, shown in Fig. 13 for this unit, shows capabilities for operation over a much wider range. Figure 13 also shows the open-loop response.

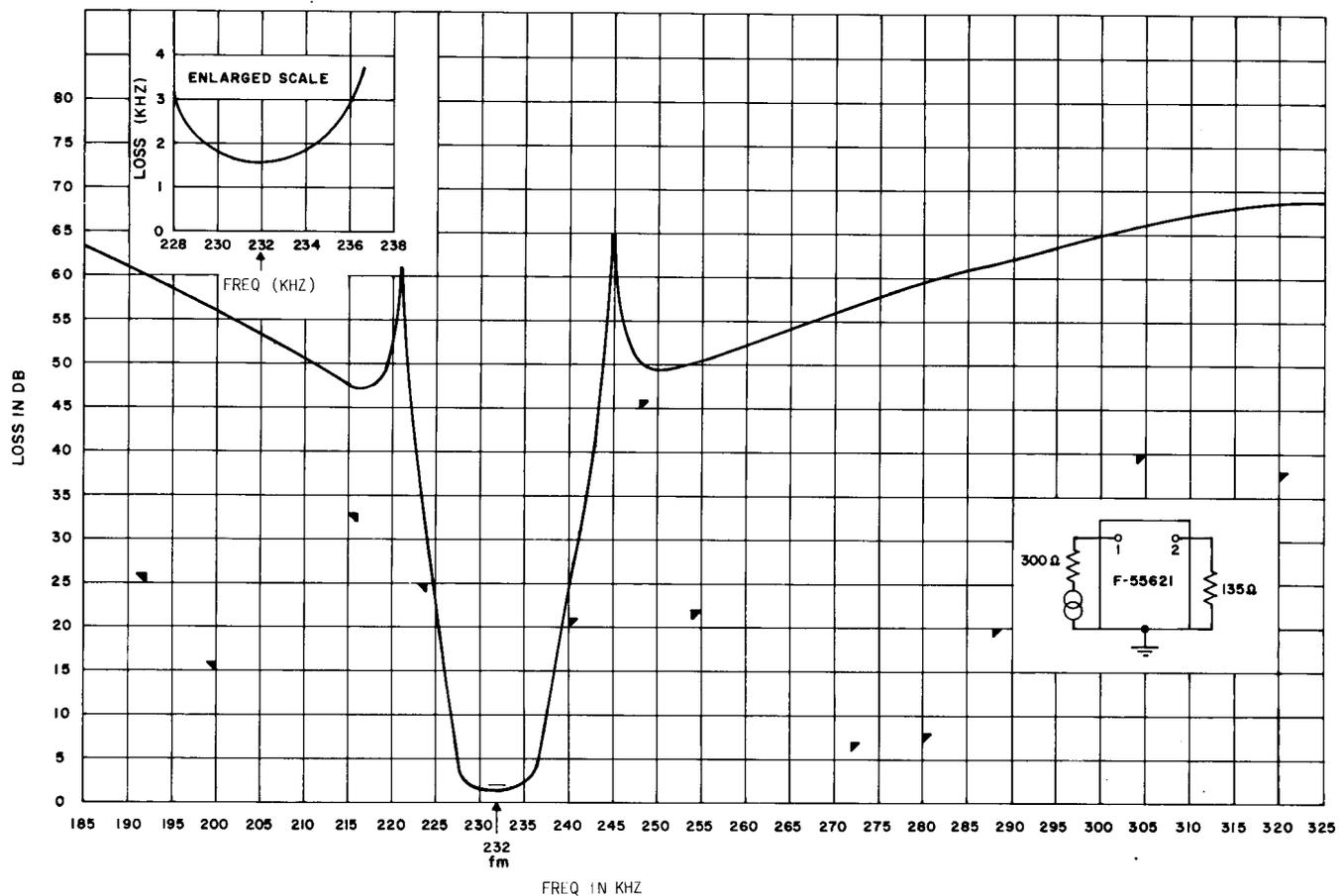


Fig. 6—Frequency Correction Circuit (J99300AE)—Output Filter for Channel Group 2 (232 kHz)

3.13 The output overload characteristic, shown in Fig. 14 for the nominal 21-volt supply voltage, has the gain break at approximately +16 dBm.

3.14 The pin jacks BIAS Q5 and BIAS Q6 on the front panel of the unit are provided to measure voltages representative of the emitter currents of each stage (see Fig. 3). In order to obtain consistent readings on all stages, the emitter resistance is split so that all emitter circuit bias voltage readings are 3 volts when the supply voltage is 21 volts.

3.15 For maintenance purposes, pin jacks CARR OUT permit a voltage measurement of the frequency shifted demodulating carrier that is delivered to the channel group modem demodulator.

C. Modulator

3.16 The modulator shown in Fig. 3 is a double-balanced switch-type transistor modulator. The "signal" is applied to the modulator via transformer T4. The "carrier" input is applied through transformer T3 and resistors R23 and R22 to the base inputs of double transistor Q4. Transistor Q4 consists of a matched pair of transistors specifically selected to maintain a high degree of balance.

3.17 The circuit operation of the modulator is most easily visualized by noting that the carrier controls the transistor switching; one transistor is on and the other off for one polarity of the carrier; the transistor conduction states are reversed with reverse polarity of the carrier. Resistors R22 and R23 in the transistor base leads provide an essentially constant current source and

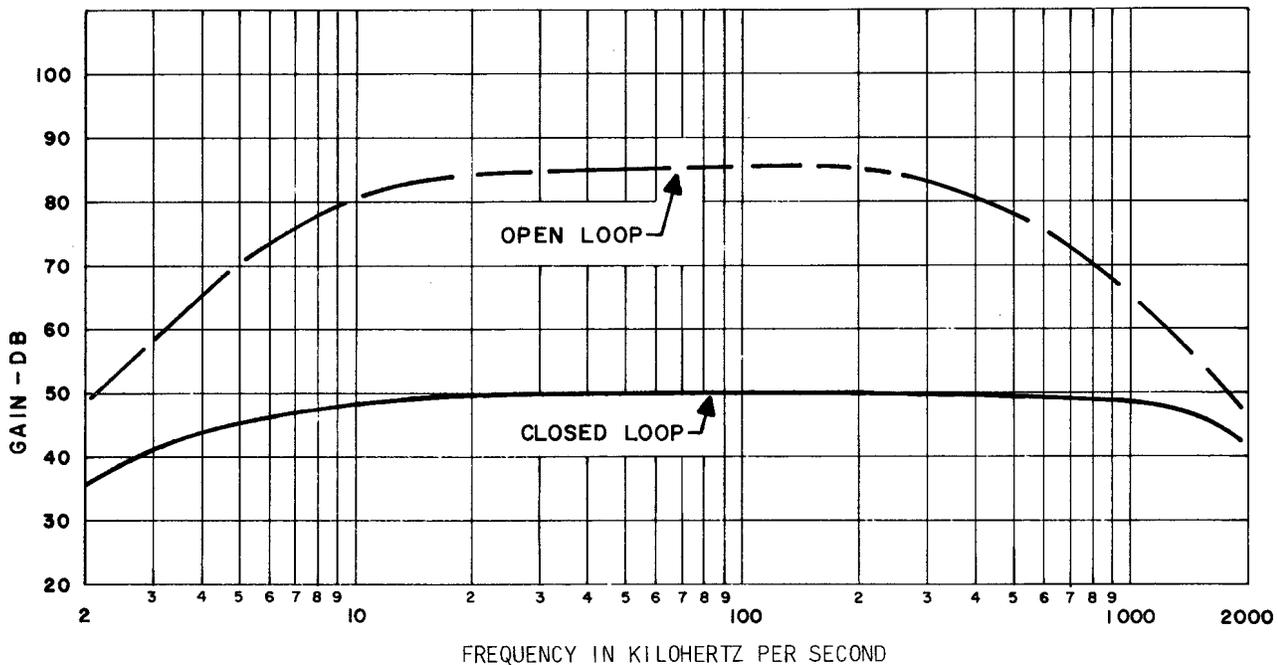


Fig. 7—Carrier Amplifier—Open and Closed Loop Gains

a good carrier input impedance. With the transistors switching on and off in this way, the terminating pad, consisting of resistors R29, R30, and R31 and the associated output circuit, is switched from one half of the secondary winding of transformer T4 to the other and back at the carrier frequency. This operation produces the desired sidebands above and below the carrier frequency at the output of the modulator.

3.18 In the frequency correction unit, the desired output is maintained within ± 0.5 dB of nominal over a 12-dB range of carrier input by providing enough gain in the carrier amplifier to adequately drive the modulator with the lower limit input power. Figure 15 shows the output power plotted as a function of carrier input power.

4. TESTING AND MAINTENANCE FEATURES

A. Terminal Assignments

4.01 In the N3 carrier-frequency correction unit, all connecting wiring to and from the N3 terminal mounting is made through a 20-pin plug at the rear of the unit which is part of the printed wiring board. The plug terminal assignments are shown in Table A.

B. Test Points

4.02 In order to facilitate the in-service detection of component variations in circuits within the frequency correction unit, test points are provided. These test points consist of seven pin jacks located on the front panel. The power of the frequency shifted output is measured at the CARR OUT jacks. Nominally this power is +3.0 dBm. The other pin jacks J2 through J5, in conjunction with the -21V pin jack J1, are used to indicate the emitter bias current of transistors Q2, Q3, Q5, and Q6. The internal measuring circuits are so arranged as to provide a nominal 3-volt reading with respect to -21 volts at all the bias test points located on the unit. Any change in this reading outside the maintenance limits would indicate a transistor gain or biasing component change.

C. Trouble Location

4.03 If it is found that a trouble exists in a frequency correction unit, the defective unit should be removed and replaced by a spare unit.

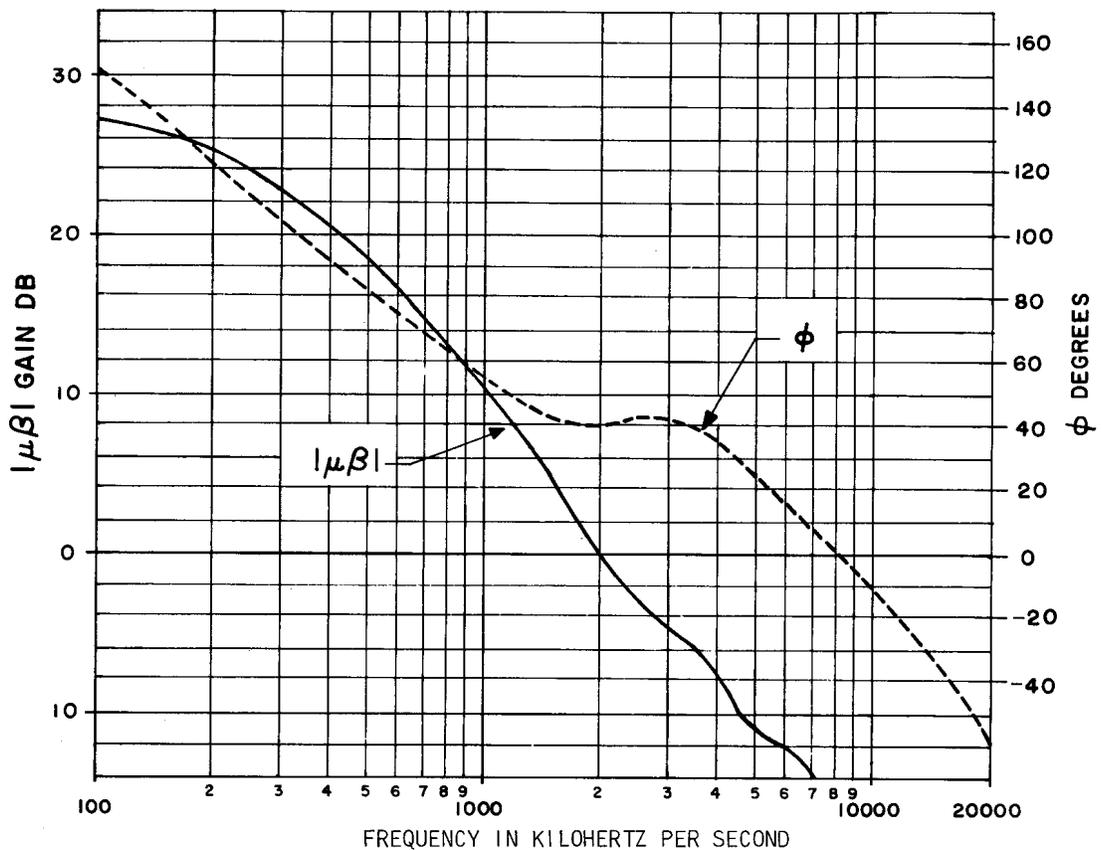


Fig. 8A—Mu-beta Phase and Gain Characteristic of the Carrier Amplifier With Input and Output Terminated in 135 Ohms

5. EQUIPMENT

5.01 The components of the frequency correction unit are mounted on a printed wiring board that is enclosed by a die-cast aluminum unit frame. External connections are made via printed tabs located on the rear of the plug-in assembly.

5.02 Filters for the frequency correction circuit are permanently mounted on the printed board at the factory.

5.03 After tests of the manufactured unit are completed, a prealloy shield is fastened to the bottom of each card holder. This shield

provides protection against undesired interference due to stray electrical or magnetic fields.

6. DRAWINGS

6.01 The following schematic and equipment drawings (not attached) show detailed information on the frequency correction unit.

NUMBER	SUBJECT
J99300AE-()	Frequency Correction Unit
SD-97178-01	Frequency Correction Circuit

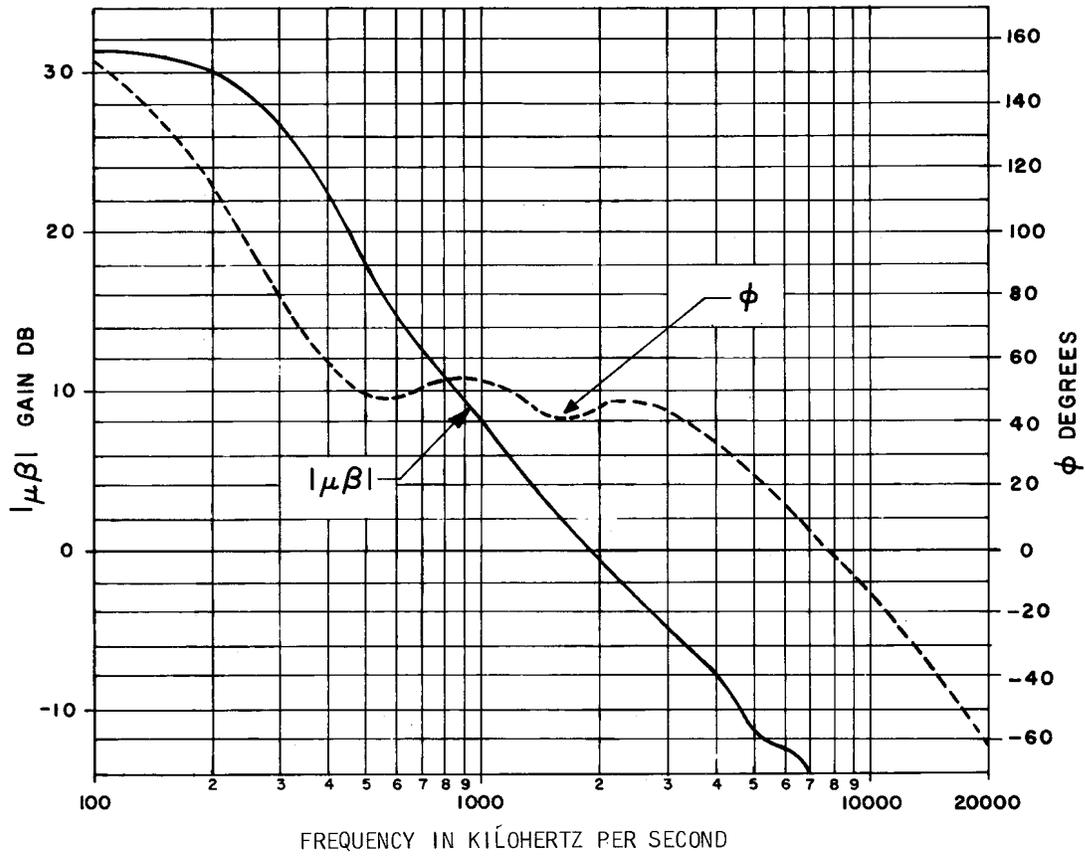


Fig. 8B—Mu-beta Phase and Gain Characteristic of the Carrier Amplifier Input Terminated by 112-kHz Pick-off Filter and Output Terminated in 135 Ohms

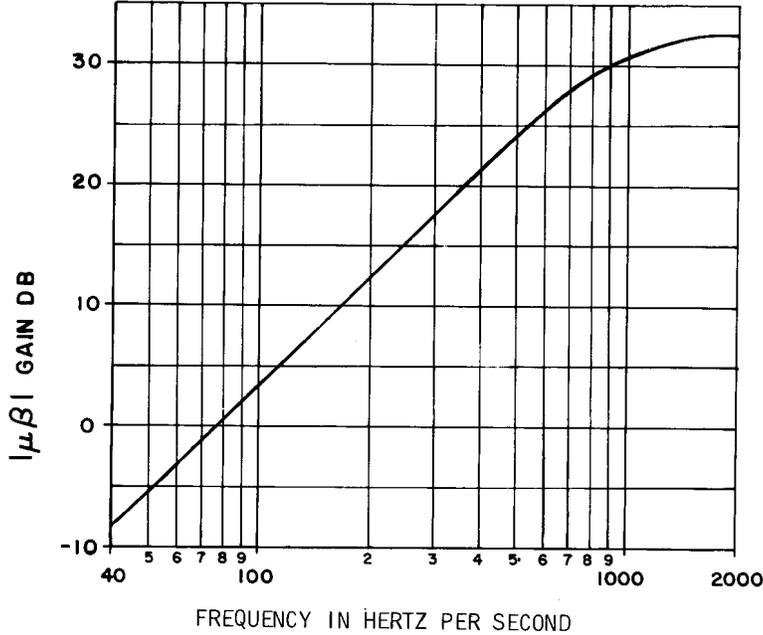


Fig. 9—Low-end Mu-beta Characteristic of the Carrier Amplifier

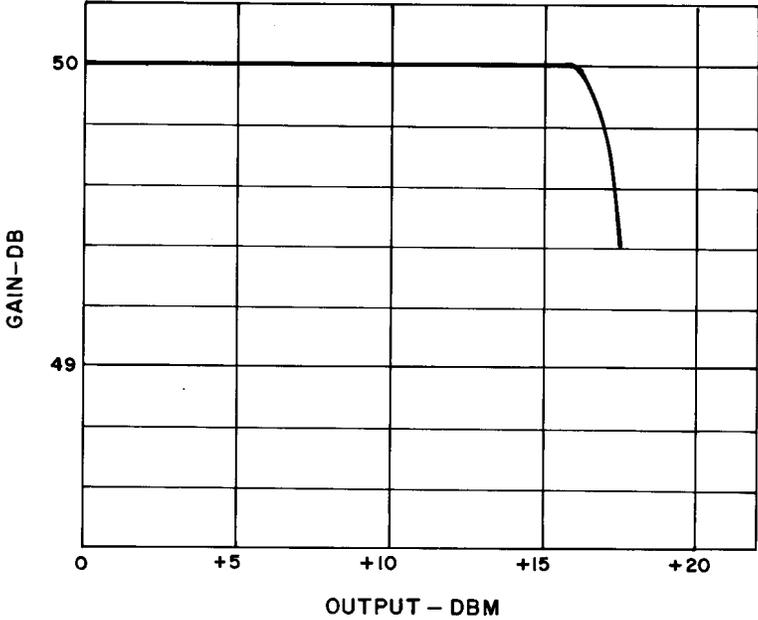


Fig. 10—Gain-Versus-Output Characteristic of the Carrier Amplifier

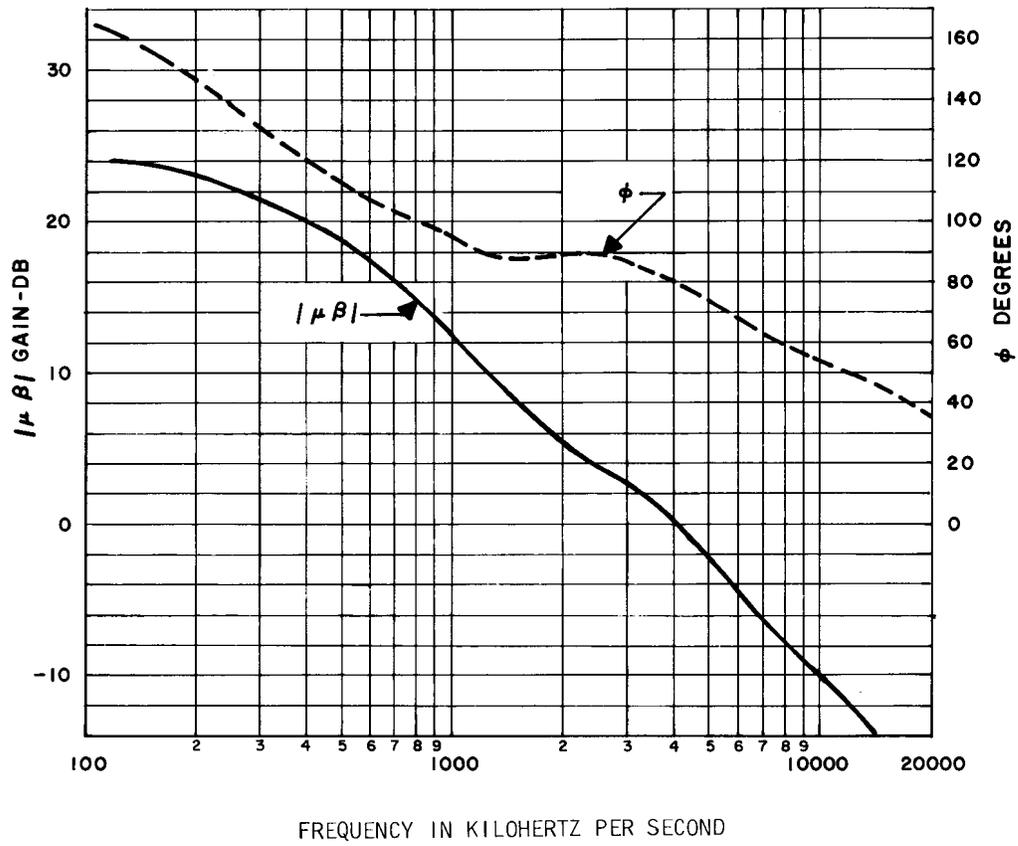


Fig. 11A—Mu-beta Phase and Gain Characteristic of the Demodulating Carrier Amplifier With Resistive 135-Ohm Input and Output Terminations

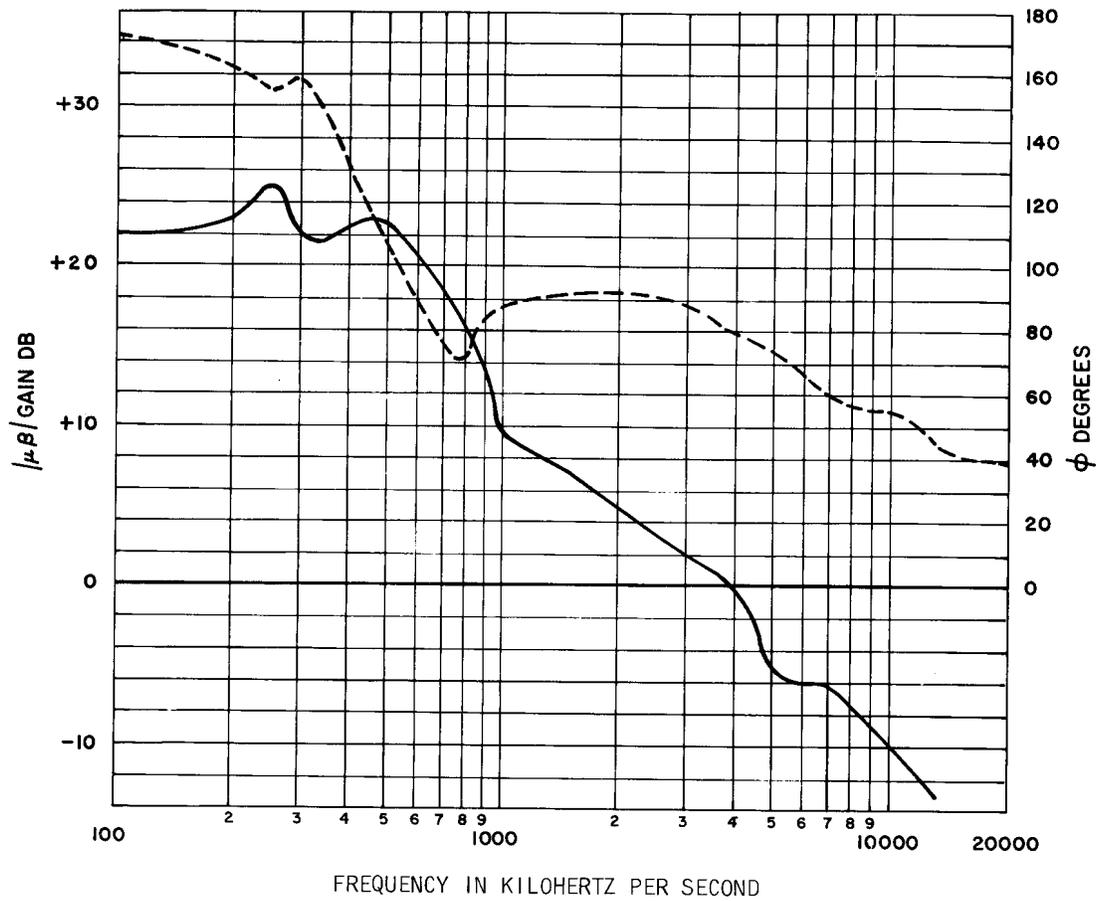


Fig. 11B—Phase and Gain Characteristic of the Demodulating Carrier Amplifier—Input Terminated by 280-kHz Filter, Output Terminated by 135-Ohm Resistor

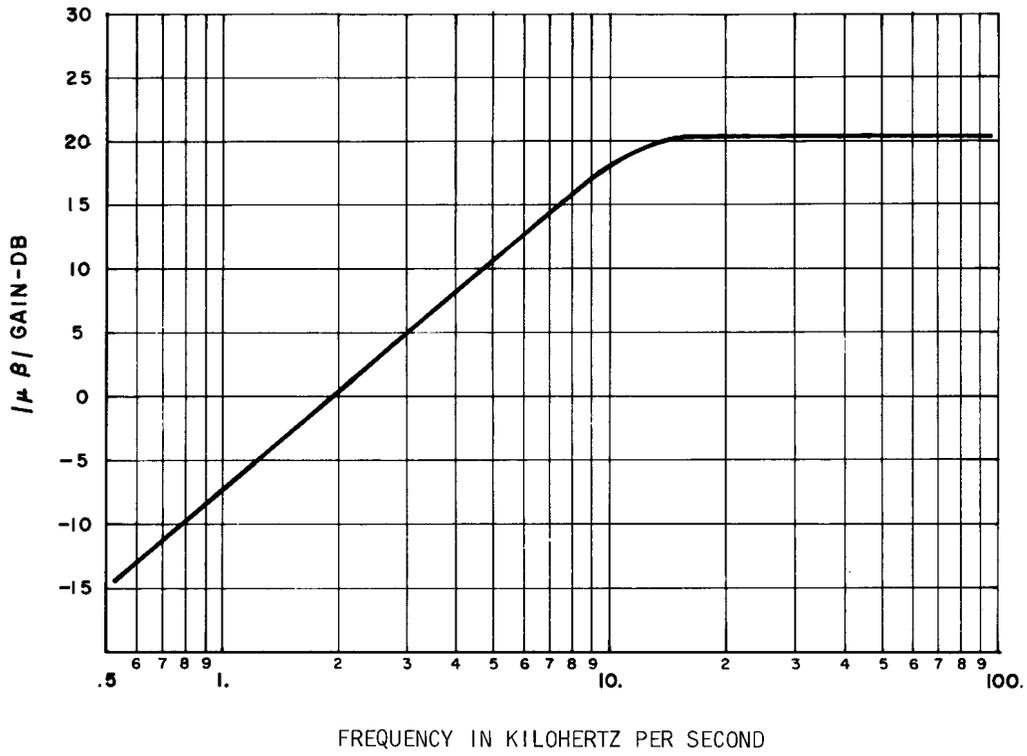


Fig. 12—Low-end Mu-beta Characteristic of the Demodulating Carrier Amplifier

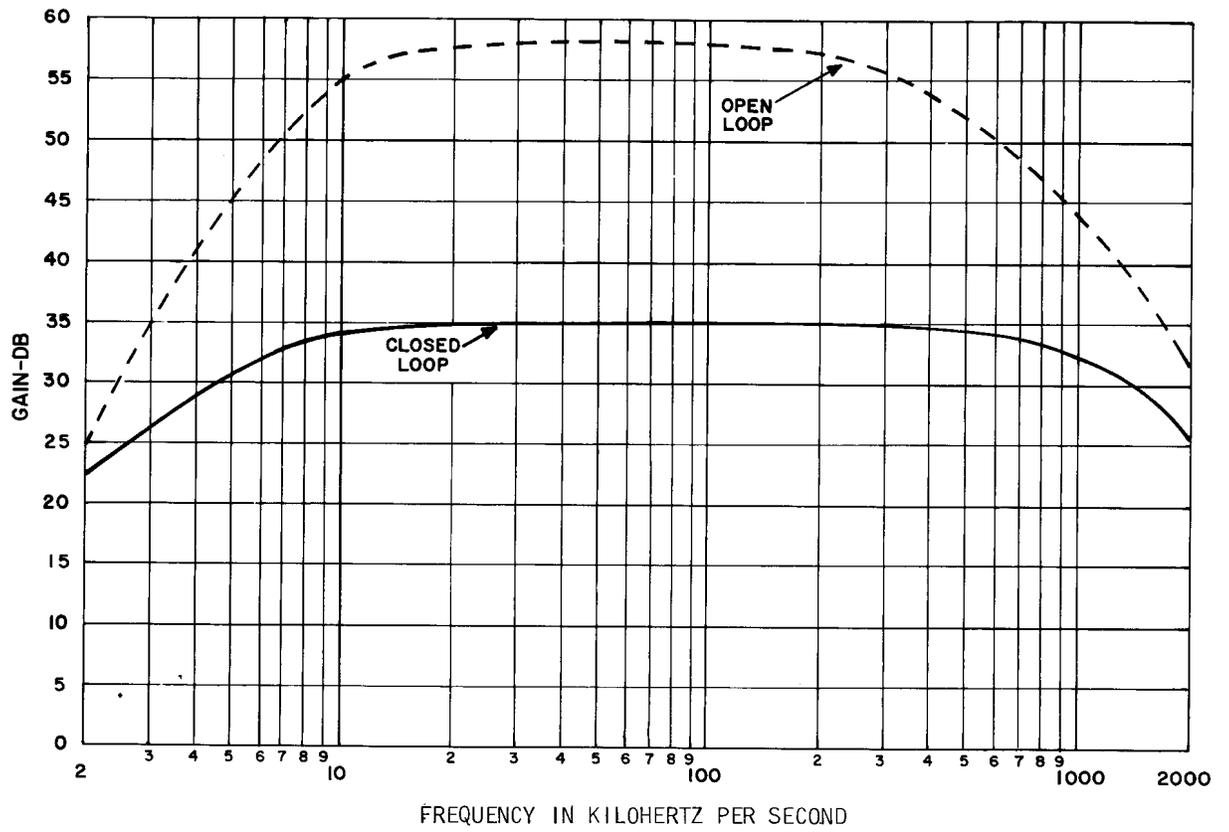


Fig. 13—Demodulating Carrier Amplifier—Open and Closed Loop Gains

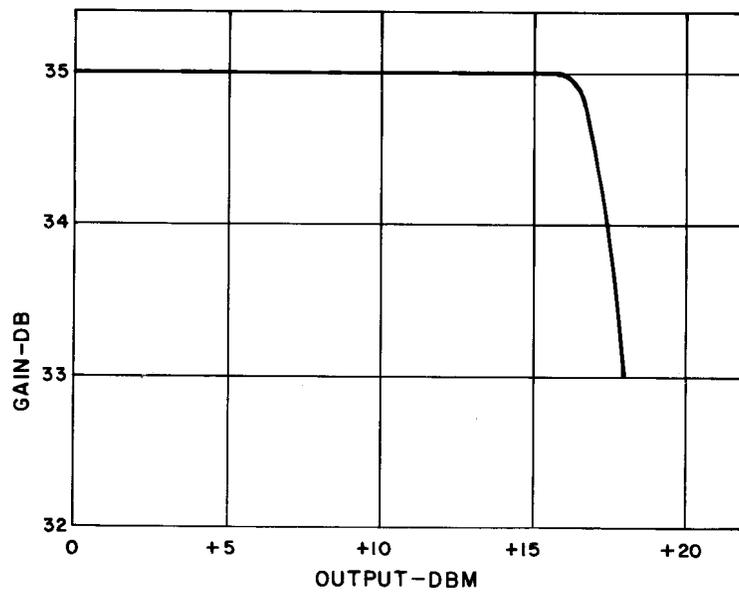


Fig. 14—Gain Versus Output—Demodulating Carrier Amplifier

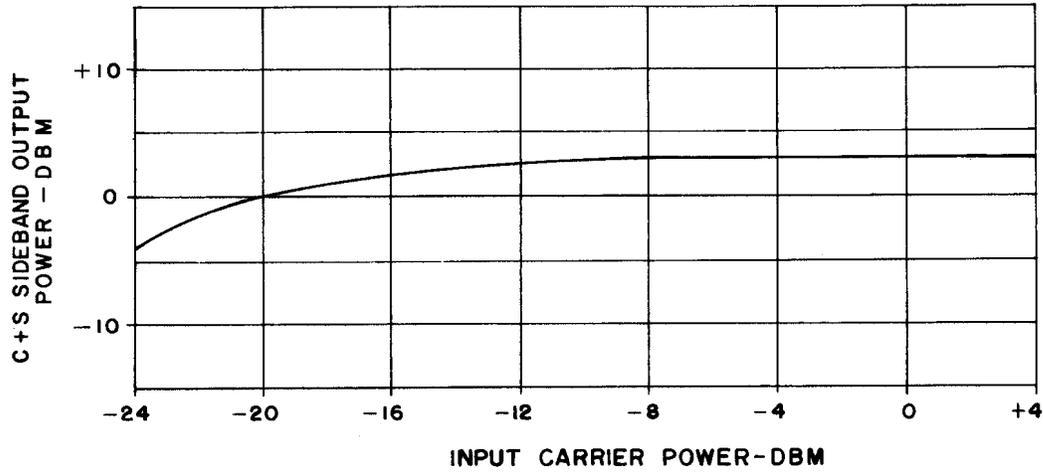


Fig. 15—Demodulating Carrier Output Versus Carrier Drive—Channel Carrier 112 or 80 kHz—Demodulating Carrier Output 280 or 232 kHz—Signal From Carrier Supply 168 or 152 kHz

TABLE A

PIN	ASSIGNMENT
1	Frame ground
2 and 3	Carrier input
4 and 6	Strapped
5 and 7	Strapped
8	No connection
9 and 10	Future circuit use
11	-21 volts
12 and 14	Strapped
13	Circuit ground
15 and 16	"Signal" input from carrier supply
17 and 18	Demodulating carrier output
20 and 19	Strapped