

**N3 CARRIER TELEPHONE SYSTEM
FREQUENCY CORRECTION UNIT**

J99300AS

DESCRIPTION

CONTENTS	PAGE	CONTENTS	PAGE
1. GENERAL	1	5. EQUIPMENT	11
2. FUNCTIONAL DESCRIPTION	2	6. DRAWINGS	11
3. CIRCUIT DESCRIPTION	4	1. GENERAL	
A. Selective Saturation Amplifier	4	1.01 This section describes the J99300AS and J99300AS MOD A frequency correction unit (FCU) used in N3 terminals and N3-L type A junctions.	
B. Alarm Pickoff	4	1.02 This section is reissued to include information on the J99300AS MOD A FCU and to update Fig. 3. Since this is a general revision, change arrows are not used. This reissue does not affect the Equipment Test List.	
C. Phase-Lock Loop Circuits—Narrowband Loop	7	1.03 A complete terminal for the N3 Carrier System consists of 24 channels (2 channel groups). One FCU is required in each channel group. They are identical except for specific filters and inductors and are not interchangeable between channel groups. Each FCU (Fig. 1) is a single plug-in assembly providing a circuit that corrects the frequency of the received carrier-frequency signal of each channel group.	
D. Phase-Lock Loop Circuits—Switching Circuits	7	1.04 Circuit components are mounted on a printed circuit board that is contained in a die-cast metal frame. All interconnecting wiring to and from the FCU enters the rear of the assembly via a 20-pin plug that is part of the printed circuit board. A mechanical latch for locking the unit in position is located on the front panel.	
E. Phase-Lock Loop Circuits—Wideband Loop	8	1.05 In N-Type Carrier System, "frequency frogging" is used in repeaters in order to	
F. Phase Detector Circuit	8		
G. Low-Pass Filter Circuit	8		
H. Varactor Diode	9		
I. Voltage-Controlled Oscillator	9		
J. Frequency Lock Lamp	10		
4. TESTING AND MAINTENANCE FEATURES	10		
A. Terminal Assignments	10		
B. Test Points	10		
C. Trouble Location	10		

NOTICE

Not for use or disclosure outside the Bell System except under written agreement

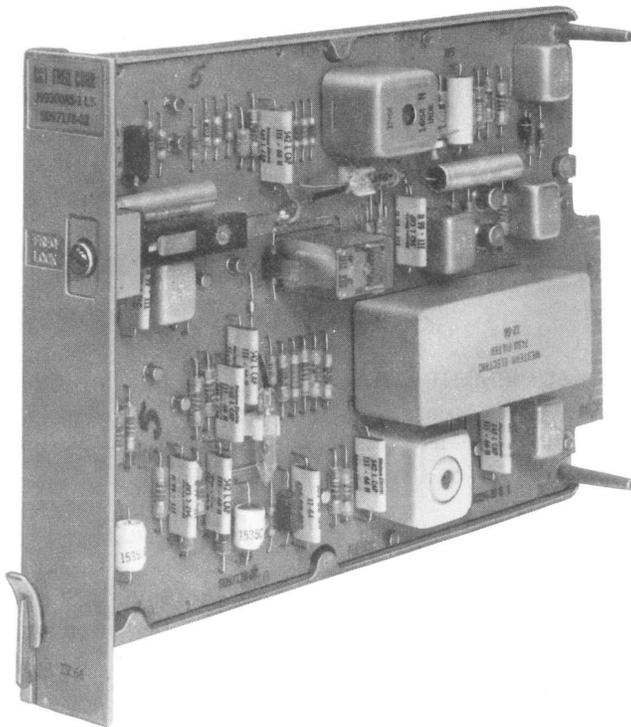


Fig. 1—Frequency Correction Unit

provide some self-equalization of the signals transmitted over cable and to block cross-talk paths. Frequency frogging is a method whereby low frequencies fed into a repeater are retransmitted as high frequencies by a low-high repeater and vice versa for a high-low repeater. To accomplish this, each N-type repeater is equipped with a local 304-kHz oscillator to provide the modulating carrier for the frogging function.

1.06 As a result of temperature variations and aging effects, the 304-kHz oscillator can be off in frequency. This causes a frequency error in all the signals appearing at the repeater outputs. Depending upon a number of factors, eg, the multiplicity of repeaters involved, this frequency error could accumulate and be as much as 150 Hz. Thus, the line signal at the receiving terminal may be offset by this amount with respect to the terminal bandpass filters.

1.07 To correct this problem, the demodulator in the channel group modem unit is supplied with a carrier that has the same frequency error as the input signal. As a result, the two errors

cancel and the demodulator output has no frequency error. The FCU derives the carrier sample from the channel group modem output and injects the corrected demodulating carrier into the channel group modem demodulator. The carrier frequencies involved and a sample illustration of the correction process on one carrier in each channel group are shown in Fig. 2.

2. FUNCTIONAL DESCRIPTION

2.01 The FCU operates on the phase-lock loop principle. In this application, the amount of phase difference between two carriers of the same nominal frequency (because of a slight difference in frequency) yields an error voltage which is used to control the frequency of an oscillator. The oscillator output of the FCU is 232 or 280 kHz (depending upon the assigned channel group) and is modified an amount equal to the frequency error contained in the input signal. This correction signal is then mixed with the input signal in the channel group modem demodulator. As a result, the two errors cancel and the demodulator output has no frequency error.

2.02 The FCU derives its input signal (148 to 196 kHz) from the output of the channel group modem demodulator (Fig. 2). In the FCU, this input is applied to frequency selective amplifier circuits tuned to 152 or 168 kHz (depending upon the assigned channel group). When the signal carrier shift exceeds 30 Hz, it is outside the bandpass of the narrowband loop. Therefore, it is bypassed by the wideband loop to the phase detector which senses the phase shift from a reference carrier of the same nominal frequency. The amount of phase shift is directly related to the frequency shift of the signal carrier. The dc output voltage of the phase detector controls the frequency shift of the voltage-controlled oscillator (VCO) from a quiescent frequency of 232 or 280 kHz (depending upon the assigned channel group). The amount of frequency shift approximates the error in the input signal carrier. The output of the VCO is applied to the channel group modem demodulator where it is mixed with the input signal. This decreases the frequency error of the signal going to the FCU input so that the signal falls within the bandpass of the narrowband loop. When the narrowband circuit senses the signal carrier, the wideband loop is disabled and the signal carrier is applied to the phase detector from the output of the narrowband loop. This operation shifts the

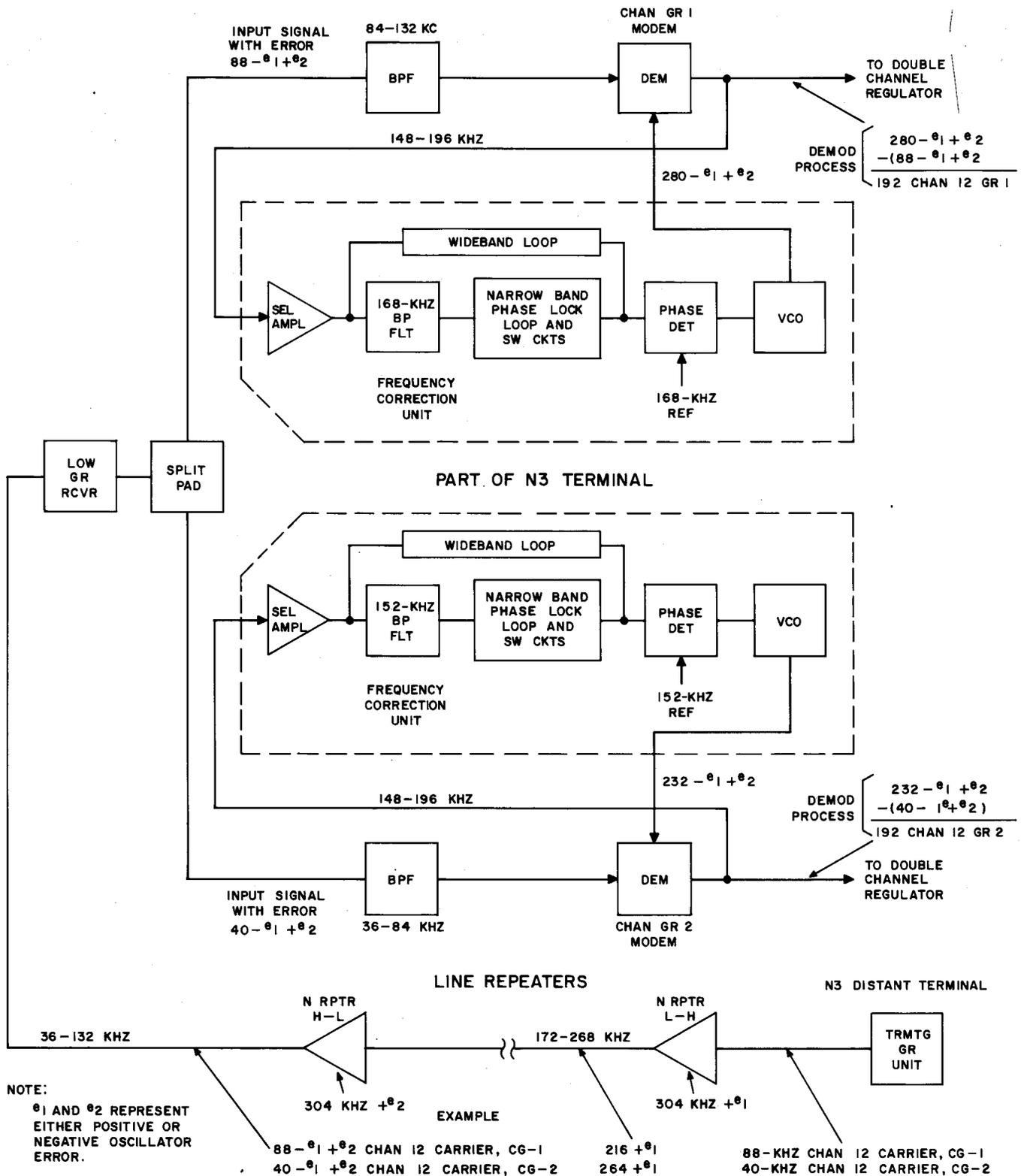


Fig. 2—N3 Terminal Application of Frequency Correction Unit

VCO output frequency to a region where the signal carrier is in phase with the reference carrier, resulting in a line signal at the receiving terminal that has no appreciable frequency error.

3. CIRCUIT DESCRIPTION

A. Selective Saturation Amplifier

3.01 This amplifier is designed to provide broad selectivity in the vicinity of the selected carrier (168 kHz for channel group 1 or 152 kHz for channel group 2).

3.02 The amplifier consists of transformer T1, transistors Q1, Q2, and Q3 connected in the common emitter configuration, and all associated components (Fig. 3).

3.03 Transformer T1 has a relatively high input impedance to prevent loading of the 22.5-ohm channel group demodulator output. The frequency band, 148 to 196 kHz, appearing at the input of the transformer, is applied to the base of transistor Q1. In the emitter circuit of transistor Q1, resistors R3 and R4 provide degenerative feedback. Capacitor C1 and inductor L1 comprise a series resonant circuit in parallel with R4. This combination is resonant at the signal carrier frequency and provides degenerative feedback for all frequencies except those at or near the carrier frequency (152 or 168 kHz). Therefore, frequencies at or near the tuned frequency of the resonant circuit receive more amplification because of the decreased degenerative feedback.

3.04 Two different values of capacitance for capacitor C1 are used. The capacitance for channel group 1 frequency correction circuit enables the series resonant circuit to bypass a 168-kHz carrier signal, and the value for channel group 2 bypasses a 152-kHz carrier signal.

3.05 The selected carrier signal is amplified by the 3-stage saturation amplifier to form a square wave at the collector of transistor Q3. The purpose of saturation is to overcome amplitude changes in the input signal. This results in a constant output level, which is used for both switching and phase comparison.

3.06 Resistor R10 and capacitor C3 provide overall negative feedback for the saturation amplifier. Inductor L2 provides a low-impedance path for

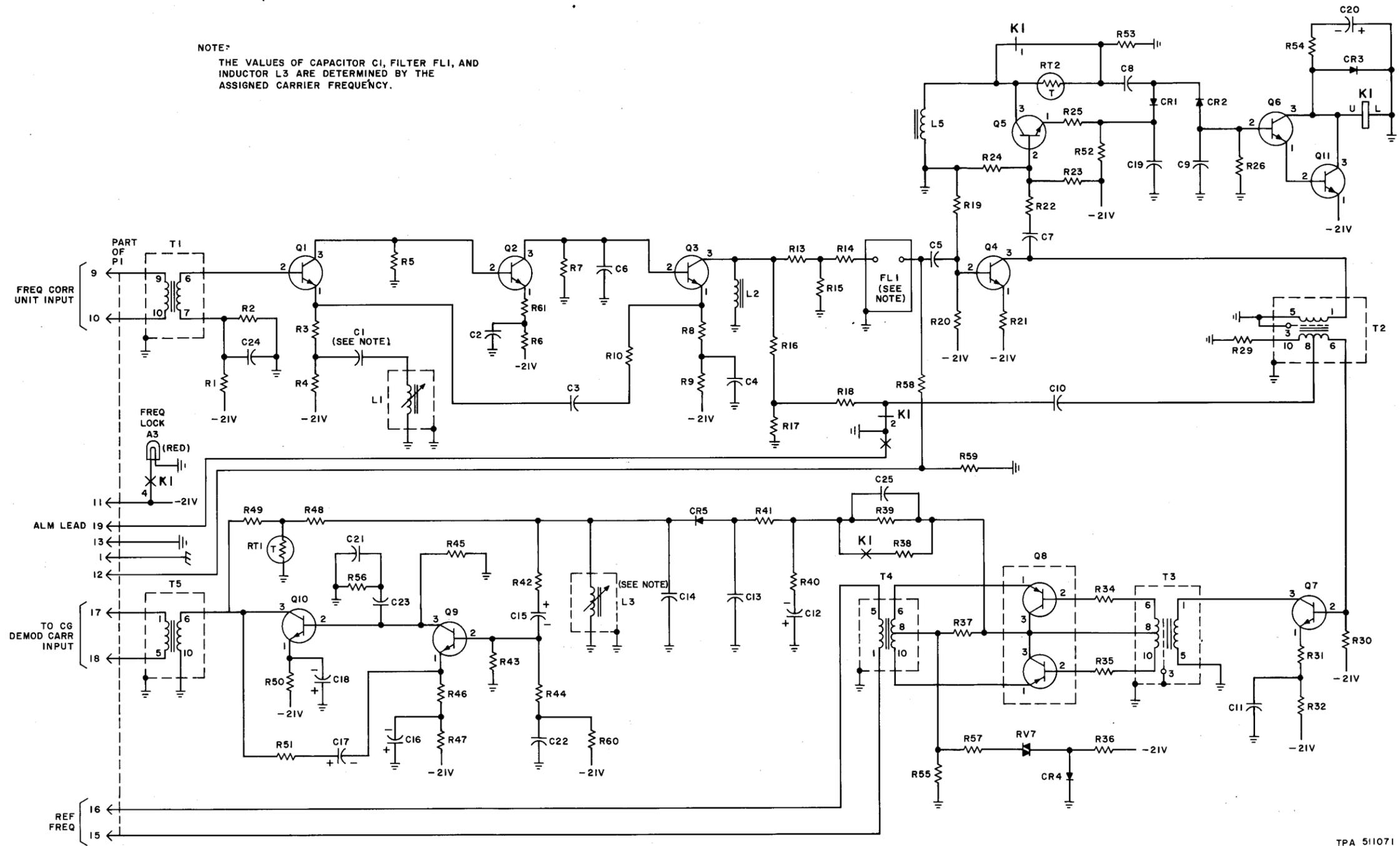
direct current and offers a high reactance to the carrier signal. Capacitor C6 in the base lead of transistor Q3 is a bypass capacitor to prevent high frequency oscillations, thus providing stabilization for the amplifier.

3.07 Base bias on transistor Q1 is obtained by the voltage divider formed by resistors R1 and R2. Capacitor C24 bypasses the signal voltage developed across R2 to eliminate any effect on the base bias established by R1 and R2. Resistor R5 sets the base bias on transistor Q2 and the dc collector voltage of transistor Q1. Resistors R6 and R61 set the emitter current and operating point of transistor Q2, and the series combination of R8 and R9 controls the emitter current and operating point of transistor Q3. Resistor R7 sets the dc collector voltage of transistor Q2 and the base bias on transistor Q3. Capacitors C2, C4, and C24 are bypass capacitors which control the low-end frequency cutoff.

B. Alarm Pickoff

3.08 N3 and N3-L Systems are protected by the alarm and restoral unit located in the receiving path of the N3 terminal. This unit responds to a loss of received carrier by activating trunk-release and make-busy circuits and by halting transmission to the faulty terminal for a few seconds to initiate alarm functions there. The J99300AS FCU provides a single frequency pickoff voltage, either 152 kHz for channel group 2 or 168 kHz for channel group 1, which is applied to the alarm and restoral unit. The single-frequency pickoff removes the susceptibility to spurious tones generated in N3-L Systems which is a problem with the total carrier power alarm method. The single carrier alarm scheme is provided in new universally wired N3 bays which require the use of the J99300AS unit; but the total power method is provided in older N3 bays which may have existing J99300AE units or newer J99300AS units.

3.09 The J99300AS MOD A FCU provides an additional alarm lead for use in an N3-L type A junction. During transmission failure, high noise levels at the input to the FCU may appear momentarily as normal carriers. This condition causes the FCU to switch randomly between its wideband and narrowband loops. To prevent the alarm, squelch, and restoral unit in the junction from restoring in this high noise condition, an alarm lead (Fig. 3, lead 19) is brought in from



TPA 511071

Fig. 3—Frequency Correction Unit, Schematic Diagram

the FCU relay K1. Each time the FCU switches to its wideband loop, the restoral timing sequence is reinitiated, thus avoiding premature restoral. When the carrier failure is cleared, the FCU switches to its narrow band loop and the restoral circuit in the alarm, squelch, and restoral unit is activated. The J99300AS MOD A FCU must be used in the modified type A junction. In N3 terminals, either modified or unmodified FCUs may be used.

C. Phase-Lock Loop Circuits—Narrowband Loop

3.10 The narrowband loop consists of crystal filter FL1, amplifier transistors Q4 and Q5, switching transistors Q6 and Q11, phase detector amplifier transistor Q7, phase detector transistor Q8, resistor R39, switching relay K1, and related circuit components.

3.11 The signal path branches into two directions at the collector of transistor Q3: through crystal filter FL1 to the narrowband loop of the phase-lock loop circuits and through resistor R16 to the wideband loop (Fig. 3). In the narrowband mode, the desired selected carrier signal is present at the output of the selective saturation amplifier and passes through the T pad consisting of resistors R13, R14, and R15 and through crystal filter FL1 and coupling capacitor C5. The bandpass of FL1 at the 1-dB point is approximately 25 Hz wide. See Fig. 4. The carrier signal also passes through resistors R16, R17, and R18 in the wideband loop but is shunted to ground by the normally closed contact of switching relay K1, which is not energized when the narrowband loop is passing the carrier signal. From the crystal filter output, the selected carrier signal is amplified by transistor Q4 and fed to hybrid circuit transformer T2.

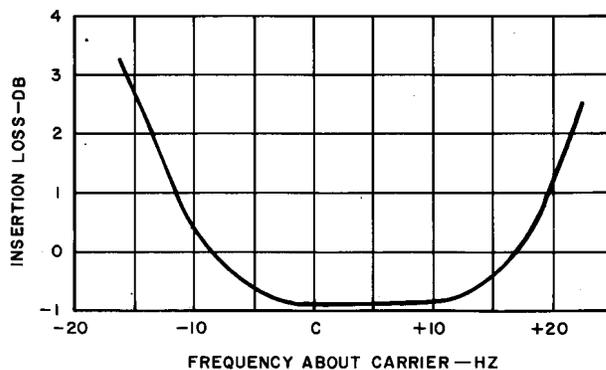


Fig. 4—Typical Passband Performance Curve of 743A and 743B Filters

3.12 Transistor Q4 is operated in the common-emitter configuration with base bias set by the voltage divider consisting of resistors R19 and R20. Resistor R21 provides local degenerative feedback and sets the emitter current and operating point of this stage. Winding 1-5 on transformer T2 supplies a low dc impedance path in the collector circuit of this stage. In addition, this winding, in parallel with the input circuit of transistor Q5, forms the ac load for this circuit.

3.13 The T pad, consisting of resistors R13, R14, and R15, preceding filter FL1 reduces the level of the selected carrier signal to prevent overloading the crystal filter.

D. Phase-Lock Loop Circuits—Switching Circuits

3.14 A switching circuit connected to the collector of transistor Q4 is shunted across the narrowband loop of the phase-lock loop circuit (Fig. 3). The essential parts of this switching circuit are transistor amplifier Q5, delay thermistor RT2, voltage doubler diodes CR1 and CR2, compound-connected switching transistors Q6 and Q11, and switching relay K1. The compound connection of transistors Q6 and Q11 is operated in the common-emitter configuration which provides a high current amplification factor (beta).

3.15 With no carrier signal passing through the narrowband loop, switching transistors Q6 and Q11 are held in conduction by forward bias provided by the -21 volt supply. When conducting, these transistors energize switching relay K1 and open the normally closed contacts shunting thermistor RT2 and the wideband loop. The normally opened contact in series with resistor R38 in the low-pass filter circuit is closed. Also, FREQ LOCK lamp A3 is lighted. The carrier signal that passed through narrowband crystal filter FL1 and was amplified by transistor Q4, is applied to switching circuit amplifier transistor Q5. From the collector of Q5, the signal is fed to delay thermistor RT2. The thermistor is initially cold and its resistance is high with respect to resistor R53, which forms a voltage divider with the thermistor. This condition allows very little carrier signal to be developed across R53. Approximately 30 seconds are required for the carrier signal current to heat the thermistor, reducing its resistance and allowing sufficient carrier signal to be fed to voltage doubler diodes CR1 and CR2. After the 30-second delay, the dc signal voltage at the output of the voltage doubler circuit is large enough to overcome the forward bias of switching transistor Q6. This causes the transistor

to become back biased and to cease conduction. At this time, switching relay K1 is deenergized and the normally closed contact across delay thermistor RT2 shunts the thermistor and allows it to cool, the normally closed contact shunting the wideband loop closes and shunts the wideband loop to ground to prevent carrier signals from passing through this loop, and the normally opened contact in series with resistor R38 opens and removes the wideband loop low-pass filter.

3.16 Inductor L5 provides a low-impedance path for dc currents and a high-impedance path for the signal currents in the collector circuit of transistor amplifier Q5.

3.17 Diode CR3, capacitor C20, and resistor R54 in the collector circuit of switching transistors Q6 and Q11 protect the transistors from inductive transients caused by relay K1.

3.18 Coupling capacitor C7 and series limiting resistor R22 couple the signal from the collector of Q4 to the base of Q5. Voltage divider resistors R23 and R24 set the base bias on transistor Q4. Resistors R25 and R52 control the emitter current and operating point of this stage. In addition, the dc voltage at the junction of resistors R25 and R52 provides a forward bias voltage for voltage doubler diodes CR1 and CR2. Capacitor C19 reduces signal degeneration in amplifier Q5 by bypassing the ac signals at the junction of resistors R25 and R52 to ground.

3.19 Capacitors C8 and C9 are, respectively, the charging and the charged capacitors in the voltage doubler network. Resistor R26 limits the base-bias current of transistor Q6 when it is in the forward biased condition. It also acts as the dc load in the voltage doubler network which furnishes the back bias for transistor Q6.

E. Phase-Lock Loop Circuits—Wideband Loop

3.20 The wideband loop of the phase-lock loop circuits consists of resistors R16, R17, and R18; normally closed contact 2 of relay K1; capacitor C10, hybrid transformer T2; phase detector amplifier transistor Q7; phase detector transistor Q8; resistor R38; and normally open contact 3 of relay K1. (See Fig. 3.)

3.21 This loop provides the initial capture and phase-lock of the carrier signal.

F. Phase Detector Circuit

3.22 The phase detector circuit consists of phase detector amplifier transistor Q7 and phase detector transistor Q8 (Fig. 3).

3.23 The signal carrier coming from either the narrowband or wideband loop is amplified by transistor Q7 and passed through transformer T3 to detector transistor Q8. At the same time, a reference carrier is fed into the low-impedance side of T4 and applied to detector transistor Q8.

3.24 Detector transistor Q8 compares the phase difference of the two carriers. The maximum magnitude of the output developed across resistor R37 can attain a value of ± 0.5 volt. The output is proportional to the phase difference. The output voltage developed across R37 modifies the bias voltage applied to varactor diode CR5.

3.25 The phase detector is a double balanced transistor circuit using the common collector configuration. With this arrangement only one side of transistor Q8 is conducting at a time, depending upon the phase relationship of the two carriers.

3.26 The series combination of resistor R34 or R35 and the low-impedance side of T3 provides a termination for the base collector junctions of Q8. Output load resistor R37 terminates the phase detector and provides the correction voltage that is fed through the low-pass filter to varactor diode CR5.

3.27 The bias voltage applied to the varactor is determined by the network consisting of resistors R36, R57, R55, zener diode CR4, and varistor RV7. Zener diode CR4 establishes a level of -8 volts at the junction of RV7 and R36. Varistor RV7 provides temperature compensation for varactor diode CR5 and inductor L3.

G. Low-Pass Filter Circuit

3.28 There are two low-pass filter circuits, one for the narrowband loop and the other for the wideband loop. The narrowband loop low-pass filter consists of resistors R39, R40, and R41 and capacitors C12 and C13. The wideband loop low-pass filter consists of normally opened contact 3 of relay K1, resistors R38, R40, and R41, and capacitors C12 and C13. See Fig. 3.

3.29 The capture of the incoming signal is controlled by the response of the low-pass filter circuits. The narrowband loop low-pass filter has a cutoff frequency of approximately 25 Hz and will lock in the incoming carrier signal if its frequency shift from nominal does not exceed the frequency cutoff range of the filter. The wideband low-pass filter has a cutoff frequency of approximately 600 Hz. This filter will allow capture of the incoming signal if its frequency shift from nominal does not exceed the 600-Hz range, but does exceed the range of the narrowband loop low-pass filter.

3.30 An inherent problem with the J99300AS (Lists 1, 2, 3, 4, 3A, and 4A) FCU is channel phase jitter caused by cable crosstalk at frequencies in a 16-Hz band centered about the frequency correction carriers. Improved J99300AS FCUs (Lists 3B and 4B) add option W which consists of replacing resistor R39 (56.2k ohms with a value of 100k ohms) and adding capacitor C25 (0.25 μ Fd). This change improves channel phase jitter by improving the stability of the phase-lock loop circuit. List B is added to indicate the inclusion of option W. Section 362-900-507 provides the procedures for testing channels suspected of exhibiting excessive or undesirable phase jitter characteristics.

H. Varactor Diode

3.31 Diode CR5 is a varactor diode, the capacitance of which varies with the applied voltage. This capacitance is part of the frequency determining circuit for the voltage control oscillator. The amount that the oscillator changes in frequency is determined by the amount that the capacitance of this diode changes. See Fig. 3.

3.32 The output voltage from the low-pass filter causes the capacitance of the varactor diode to change in a relationship that is inversely proportional to the frequency shift of the incoming signal carrier. If the frequency of the incoming carrier signal increases, the frequency correcting voltage from the phase detector increases, causing the capacitance of the varactor diode to decrease, and vice versa. See Fig. 5. When the incoming carrier signal is in phase with the reference frequency, the output frequency correcting voltage of the phase detector is zero, and the only voltage applied to the varactor diode is the dc bias voltage.

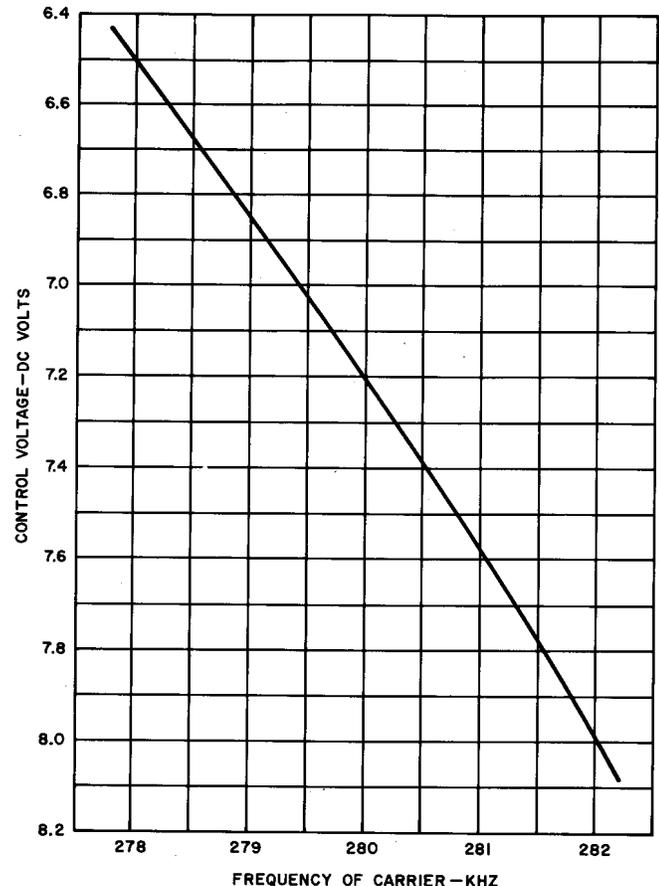


Fig. 5—Frequency of VCO Versus Varactor Bias Curve

I. Voltage-Controlled Oscillator (VCO)

3.33 The VCO consists of transistors Q9 and Q10; the positive feedback loop with resistors R42, R48, R49, capacitor C15, and thermistor RT1; and the negative feedback with resistor R51 and capacitor C17. See Fig. 3. The frequency-determining parallel resonant tank circuit is made up of inductor L3 and the combined capacitance of capacitors C13 and C14 and varactor diode CR5. When the signal carrier is in phase with the reference carrier, the quiescent frequency of the VCO is 280 kHz for the channel group 1 FCU and 232 kHz for the channel group 2 FCU. The value of inductor L3 is dependent upon the assigned channel group and is tuned so that the resonant circuit is operating at the correct frequency. The frequency shift of the resonant tank circuit is controlled by varactor diode CR5 and is directly proportional to the frequency shift of the signal carrier. The output frequency of the VCO is the frequency-correcting

carrier for oscillator is the frequency-correcting carrier for the channel-group demodulator. When the VCO frequency, which has been shifted by an amount equal to the amount of frequency shift of the signal carrier, beats with the incoming carrier signal, the frequency shift of the incoming carrier signal is reduced to zero.

3.34 Limiting in the VCO is performed on a power basis. Feedback via the positive feedback loop is limited by thermistor RT1. The loss in the positive feedback loop incurred by RT1 is equal to the gain of the amplifier. That is, when the power gain of the amplifier increases, the resistive impedance of the thermistor decreases. This causes the thermistor to absorb more power, thereby reducing the amount of positive feedback.

3.35 The negative feedback loop consisting of resistor R51 and capacitor C17 provides gain stability of the amplifiers with respect to variations of the transistor parameters and aging of the components.

3.36 Capacitors C21 and C23 and resistor R56 make up a shaping circuit to prevent the oscillator from singing. Resistors R43, R44, and R60 set the base bias on transistor Q9. Resistor R45 sets the base bias on transistor Q10 and the dc collector voltage of Q9. Capacitor C22 is a decoupling capacitor that prevents interference on the -21 volt supply from reaching the low-level input of transistor Q9. Series-connected resistors R46 and R47 control the emitter current and operating point of transistor Q9. Degenerative feedback is provided by unbypassed resistor R46. Capacitor C16 bypasses the oscillator frequency around resistor R47. Resistor R50 controls the emitter current and operating point of transistor Q10. Capacitor C18 bypasses the oscillator frequency to ground.

J. Frequency Lock Lamp

3.37 The frequency lock lamp (Fig. 3) indicates the operating condition of the FCU, either wideband or narrowband mode.

3.38 This lamp is controlled by relay K1 which is energized in the wideband mode. When the FCU is operating in the wideband mode, the lamp is lighted. If the lamp continues to remain lighted after a period of approximately 30 seconds, this indicates that the frequency shift of the signal

carrier has deviated beyond the range of the frequency correction circuit. The lamp is extinguished when the unit is operating in its narrowband phase-locked loop position.

3.39 Some initially defective J99300AS, List 1 and 2 units always remain in the wideband mode as indicated by the frequency lock lamp. Improved J99300AS, List 3 and 4 units which contain a higher Q resonate circuit are now manufactured instead of List 1 and List 2 units, respectively. SD-97178-02 (not attached) indicates this improvement as option Y. Replacement is necessary only if the trouble is incurred.

4. TESTING AND MAINTENANCE FEATURES

A. Terminal Assignments

4.01 In the N3 carrier FCU, all connecting wiring to and from the N3 terminal mounting is made at the rear of the unit through a 20-pin plug which is part of the printed wiring board. The plug terminal assignments are shown in Table A.

TABLE A

PIN	ASSIGNMENT
1	Frame Ground
9, 10	Signal Carrier Input
11	-21 Volts
12	Alarm Pickoff
13	Circuit Ground
15, 16	Reference Carrier Input
17, 18	Demodulating Carrier Output
19	Type A Junction Alarm Lead

B. Test Points

4.02 No test points are designated at present.

C. Trouble Location

4.03 If trouble exists in a FCU, the defective unit should be removed and replaced by a spare unit assigned to the same channel group.

5. EQUIPMENT

5.01 The components of the FCU are mounted on a printed wiring board that is enclosed by a die-cast aluminum unit frame. External connections are made by printed tabs located on the rear of the plug-in assembly.

5.02 The filter for the FCU is permanently mounted on the printed board at the factory.

5.03 The 35A transistor specified for Q8 consists of a matched pair of transistors. The individual matched transistors of a 35A pair can neither be purchased nor replaced separately.

5.04 The specific value of components C1, L3, and FL1 is dependent upon the assigned carrier frequency of the related channel group.

5.05 After tests of the manufactured unit are completed, a shield is fastened to the bottom of each card holder. This shield provides protection against undesired interference caused by stray electrical and magnetic fields.

6. ASSOCIATED DRAWINGS (Not Attached)

SD-97178-02	Frequency Correction Unit
SD-3C043-01	Type A Junction Circuit (Shop Wired)
SD-3C042-01	N3-L Type A Junction (Application Schematic)
SD-3C049-02	N3-L Alarm, Squelch, and Restoral Unit