AUA71 LBRV TRANSCODER UNIT—5SLI280AXX

DATA SHEET

SLC ® SERIES 5 CARRIER SYSTEM

The AUA71 transcoder unit (TCU) is used in the SLC Series 5 system to provide low bit rate voice (LBRV) treatment of two single digroup pulse code modulation (PCM) signals, serving up to 48 voice frequency (VF) circuits on a single DS1 line.

Figure 1 is a functional block diagram of the unit, and Figure 2 shows the faceplate.

In SLC Series 5 systems, the TCU interfaces with a transmit-receive unit (TRU), a line interface unit (LIU), a line switch unit (LSU), and a Bank Controller (BC).

In the transmit direction, the transcoder transmit device (TTD) receives two single digroup PCM bitstreams (LTPCM-A/C and LTPCM-B/D), a 4.096-MHz clock (CK), and a superframe synchronization signal (NSYNC) from a TRU or two TACs. The TTD monitors PCM parity and the presence of the clock.

The TTD routes the 48 VF channels through TCUs 1-3 and then multiplexes them back together again to form the output ADPCM frame. The TTD passes timeslot 0 through unchanged, inserts all ones into the null timeslots, recalculates parity for each completed timeslot, and transmits one dual digroup bitstream

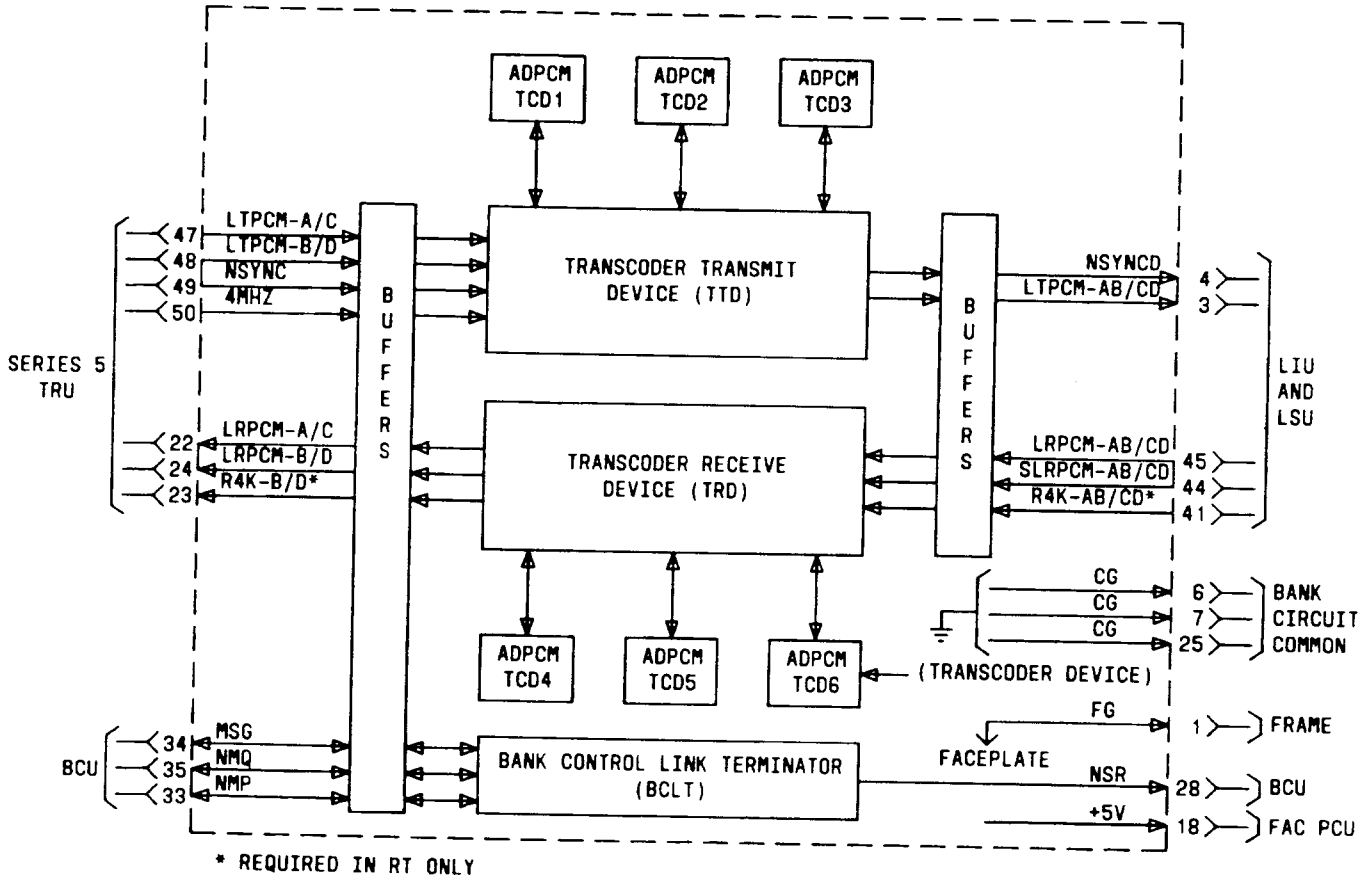

Fig. 1—AUA71 Block Diagram

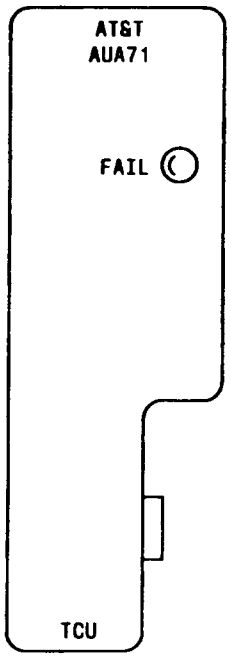

Fig. 2—AUA71 Faceplate

(LTPCM-AB/CD) and a delayed superframe synchronization signal (NSYNCD).

In the receive direction, the transcoder receive device (TRD) receives one dual digroup ADPCM bitstream (SLRPCM-AB/CD) and 4-KHz clock (R4K-AB/CD) from the main LIC, and a dual digroup ADPCM bitstream (SLRPCM-AB/CD) from the LSU. NSYNCD maintains frame synchronization and the tenth-bit of timeslot 0 is used for superframe synchronization. The TRD monitors the two PCM signals for odd parity and, under Bank Controller control, selects one of the ADPCM inputs and enables or disables the R4K.

The TRD routes the 48 VF channels to the output PCM frame. The TRD extracts and outputs the signaling bits of each channel, passes through or sets the E and G bits, and zeros the F bits. The TRD passes through the contents of timeslot 0 and outputs all ones in the null timeslots. Finally, the TRD recalculates odd or even parity for each completed timeslot and transmits two single digroup PCM bitstreams (LRPCM-A/C and LRPCM-B/D), and R4K-B to the TRU or two TACs.

The Bank Controller (BC) and the bank control link terminator (BCLT) communicate via the serial bidirectional data bus MSG in conjunction with NMP and NMQ select leads. The Bank Controller receives service requests from the TTD over the NSR lead, then reads the appropriate registers to determine the reason for the request: PCM or internal parity errors or loss of 4 MHz.

Provisioning parameters received from the BC determine how each equipped voice channel is treated:

Dual-circuit VF channel units: 4-bit ADPCM encode/decode with robbed bit signaling extraction and insertion.

Single-circuit VF channel units: 8-bit PCM pass through with robbed bit signaling.

Dataports: Pass through.

The BC also controls the received E&G bits, the FAIL LED, ouput PCM parity, and loopback test functions.

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