AUA18 DIGITAL TEST UNIT — LEFT 5SCDA00AXX

DATA SHEET

SLC® SERIES 5 CARRIER SYSTEM

The Digital Test Unit (DTU) is composed of two circuit boards, an AUA19 Digital Test Unit-Right (DTU-R) and an AUA18 Digital Test Unit-Left (DTU-L). Thus, the Digital Test Unit-Left, which has been assigned apparatus code AUA18, comprises one half of the Digital Test Unit. However, it is not possible for the DTU-L to provide any DTU functions unless a DTU-R is installed. One DTU pair is installed in the Series 5 Central Office Terminal (COT) or Digital Carrier Line Unit 5 (DCLU 5) Transmission Facility Interface Unit (TFIU), and another pair is installed in the Series 5 Remote Terminal (RT). The DTU is used by the Extended Test Controller (XTC) (AT&T Practice 363-205-300) and the Series 5 Craft Interface Unit (CIU) (AT&T Practice 306-205-201) for channel testing functions. The DTU provides the interface for the XTC and the CIU to obtain bit stream access on a channel. For a full description of the DTU functions, see the DTU-R (AUA19) Data Sheet (AT&T Practice 363-005-207).

This practice has been reissued to add the use of the AUA18 in the DCLU 5.

Figure 1 is a functional block diagram of the AUA18 DTU-L unit. Figure 2 shows the faceplate. The following description refers to the block diagram of Fig. 1. All of the following functions require control signals from the DTU-R.

Input MUX: This circuit selects one of the four Series 5 Transmit/Receive units (TRUs) or DCLU 5 Timeslot Access Circuits (TACs) to provide the 4-MHz data (from the XRPCM and YTPCM leads), 4-MHz clock, and nsync, the synchronization signal.

Receive Path Processor: [Named receive by convention, since in the normal access mode the signal path is from the line interface unit (LIU) output to the channel unit input.] These circuits provide 64-KHz to 4-MHz rate conversion on the data received from the extended test controller or the craft interface unit via the YR lead. Signalling bit recovery and parity bit generation is performed on the 8-bit, 64-KHz, DS0 formatted data received. After rate conversion, the 16 bits of 4-MHz data are transmitted to a channel unit via the XTYRP leads of the TRU.

A 4-MHz to 64-KHz rate conversion is performed on the data received from the LIU, via the TRU or the DCLU 5 TACs XRPCM lead. The 16-bit 4-MHz data is converted into 8-bit, 64-KHz, DS0 formatted data, and transmitted to either the XTC or CIU via the XR lead. Robbed-bit signalling bits are generated and transmitted in frames 6, 12, 18, and 24, if desired. Otherwise, the first 8 bits of the 4-MHz data are reproduced and transmitted as the 8 DS0 bits.

Transmit Path Processor: (Named transmit by convention, since in the normal access mode the signal path is from the channel unit output to the line interface unit input.) These circuits provide 64-KHz to 4-MHz rate conversion on the data received from the extended test controller or the craft interface unit via the XT lead. Signalling bit recovery and parity bit generation is performed on the 8-bit, 64-KHz, DS0 formatted data received. After rate conversion, the 16 bits of 4-MHz data are transmitted to a line interface unit via the XTYRP leads of the TRU or DCLU 5 TAC.

A 4-MHz to 64-KHz rate conversion is performed on the data received from the channel units, via the TRU or TACs YTPCM lead. The 16-bit 4-MHz data is converted into 8-bit, 64-KHz, DS0 formatted data, and transmitted to either the XTC or CIU via the YT lead. Robbed-bit signalling bits are generated and transmitted in frames 6, 12, 18, and 24, if desired. Otherwise, the first 8 bits of the 4-MHz data are reproduced and transmitted as the 8 DS0 bits.

Output Select: This circuit selects the particular TRU in the Series 5 dual bank or TAC in DCLU 5 which is to receive the 4-MHz XTYRP outputs. It also controls the multiplexing of data onto the XTYRP outputs for the transmit and receive path processors.

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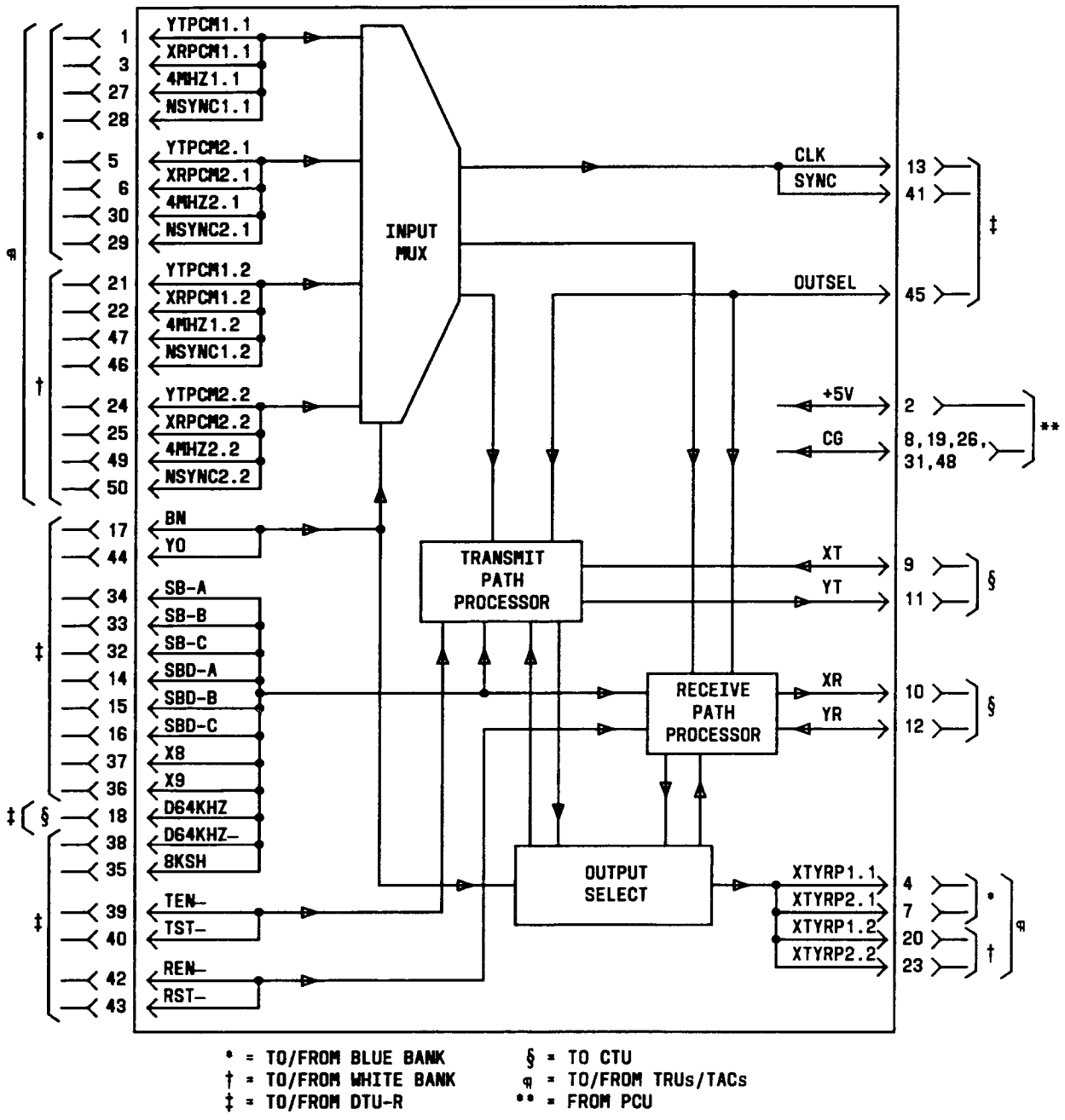

Fig. 1—AUA18 DTU-L Block Diagram

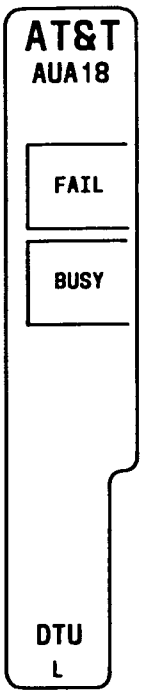

Fig. 2—AUA18 DTU-L Faceplate Diagram