

## AUA19 DIGITAL TEST UNIT — RIGHT 5SCDB00AXX

### DATA SHEET

### SLC® SERIES 5 CARRIER SYSTEM

The Digital Test Unit (DTU) is composed of two circuit boards, an AUA19 Digital Test Unit-Right (DTU-R) and an AUA18 Digital Test Unit-Left (DTU-L). One DTU pair is installed in the Series 5 Central Office Terminal (COT) or Digital Carrier Line Unit 5 (DCLU 5), and another pair is installed in the Series 5 Remote Terminal (RT). For a full description of the DTU functions, see DTU-L (AUA18) Data Sheet (AT&T Practice 363-005-206). The DTU is used by the Extended Test Controller (XTC) (AT&T Practice 363-205-300) and the Series 5 Craft Interface Unit (CIU) (AT&T Practice 306-205-201) for channel testing functions. The DTU provides the interface for the XTC and the CIU to obtain bitstream access on a channel.

This practice has been reissued to add the use of the AUA19 in the DCLU 5.

The DTU provides access to the 4-MHz bit streams of a SLC Series 5 Carrier System between the Transmit/Receive Units (TRUs) and the Channel Units (CUs) or, with DCLU 5, at the Data Link Interface (DLI). There are two normal access modes of operation, both of which allow either the Extended Test Controller (XTC) or the Craft Interface Unit (CIU), via the Channel Test Unit (CTU), to insert data into and receive data from the 4-MHz bit streams. There is no XTC at the RT; therefore, only the CIU has access to the 4-MHz bit streams.

In Series 5, one of the four TRUs in a dual bank is selected by the DTU. In conjunction with that TRU, the DTU selects one of the 32 time slots of that particular TRU's 4-MHz bit streams, which corresponds to a particular customer's line. In both normal access modes of operation, the selected 4-MHz time slot is converted into an 8-bit, 64-KHz, DS0 format for transmission to the XTC or CIU. However, in the first mode, the eight DS0 bits represent the first eight 4-MHz bits. Thus a 64-KHz clear data channel is provided to the XTC or CIU.

In the second normal access mode of operation, the DTU can also provide XTC or CIU access to the signaling bits of the 4-MHz time slot. Of the 16 bits received from the 4-MHz time slot, the first 7 bits are transmitted intact; and the A, B, C, and D bits are "bit stuffed" into the eighth bit of frames 6, 12, 18, and 24, respectively. The 8 bits are then transmitted at the 64-KHz rate.

The 16 bits that are injected back into the 4-MHz bit stream from the DTU, in either of the normal access modes, are derived as follows:

Bits 1 through 8 come from the 8 DS0 bits received from the XTC or CIU.

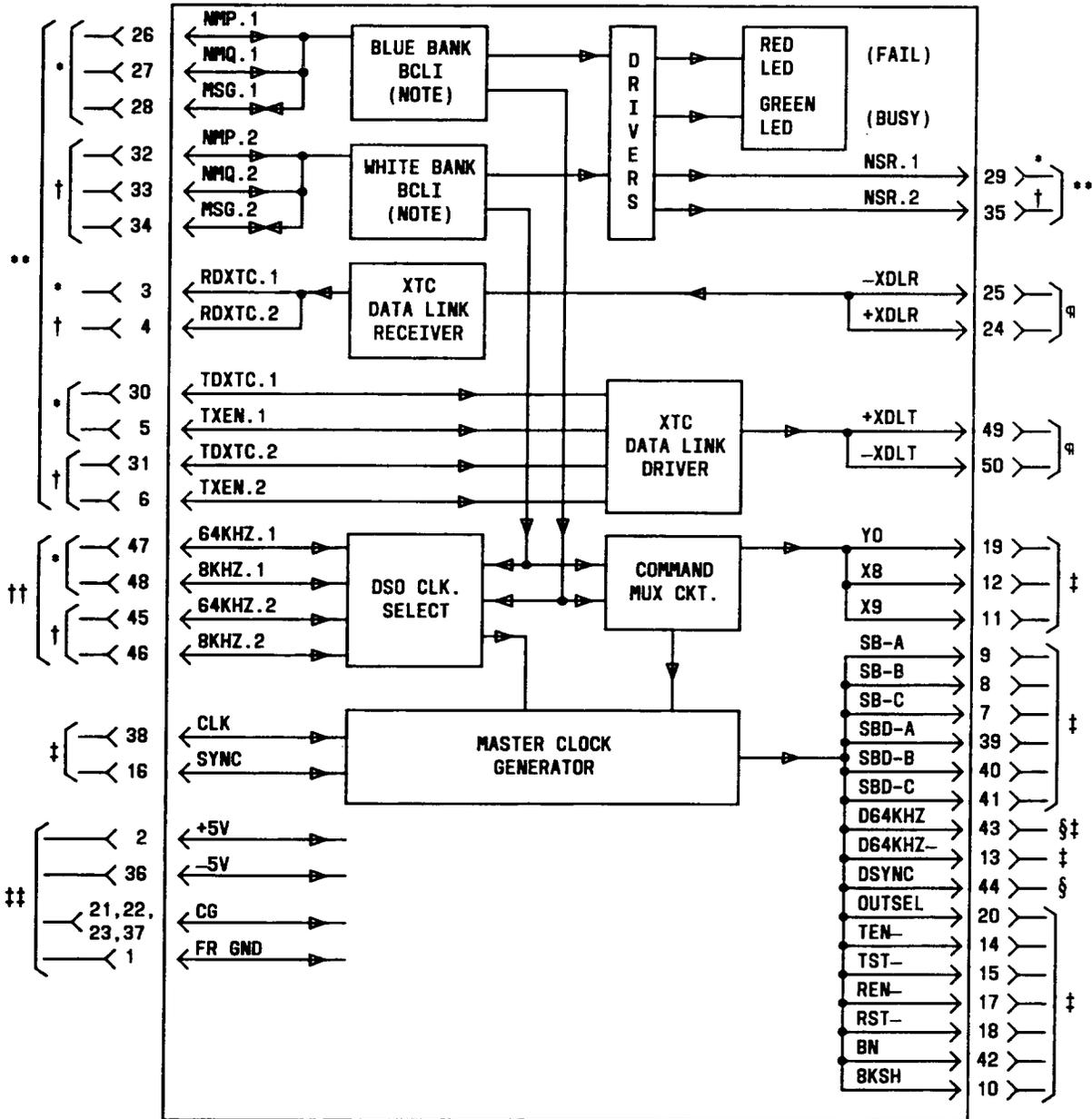
Bits 9 through 12 are the A, B, C, and D bits derived from the robbed eighth bit.

Bits 13 through 15 are passed as received from the 4-MHz input.

Bit 16 is the parity bit and is generated by the DTU to send odd parity.

The DTU also has two special modes of operation, the monitor mode and the DS0 loopback mode.

In the monitor mode, the 4-MHz bit streams received on the XRPCM and YTPCM leads are passed to the 4-MHz output, XTYP, with no modifications. The XRPCM lead carries data from the Line Interface Unit (LIU), the YTPCM lead carries data from the channel unit, and the XTYP lead transmits multiplexed data to both LIU and CU. All three leads come from the TRU, which diverts the normal paths of the 4-MHz bit streams to these leads. The DS0 outputs still transmit to the XTC or CIU as in a normal access mode of operation. The DS0 inputs from the XTC or CIU are ignored. Therefore, this mode allows a customer's line to be monitored by the XTC or CIU, while not affecting the customer's communication.



NOTE: BCLI - Bank Control Link Interface

- \* = TO/FROM BLUE BANK
- † = TO/FROM WHITE BANK
- ‡ = TO/FROM DTU-L
- § = TO CTU
- ¶ = TO/FROM XTC
- \*\* = TO/FROM BANK CONTROLLERS
- †† = FROM OTU'S
- ‡‡ = FROM PCU

Fig. 1—AUA19 DTU-R Block Diagram

In the DS0 loopback mode of operation, the DS0 inputs, XT and YR, are looped back to the DS0 outputs, XR and YT, respectively. The 4-MHz output injects the received data back into the bit stream as in the normal access modes. The 4-MHz inputs are ignored. This mode provides a functional check of the DTU circuitry.

Figure 1 is a functional block diagram of a Series 5 AUA19 DTU-R unit. Figure 2 shows the faceplate.

The following description refers to the block diagram of Fig. 1.

**Blue/White BCLI (Bank Control Link Interface) Integrated Circuits:** These devices allow either of the bank controllers in the dual bank to communicate with the DTU.

**FAIL LED:** This red LED allows either bank controller to mark the DTU as "failed". If this occurs, both of the DTU circuit cards should be replaced.

**BUSY LED:** This green LED indicates that the DTU is currently in use.

**NSR Leads:** These service request leads are used to get DTU initialization from the bank controllers.

**XTC Data Link Driver/Receiver:** This circuit merely provides the interface between the bank controllers and the XTC. It is totally separate from the other DTU functions. This is the only DTU function that will continue to operate if a DTU-L is not installed.

**DS0 Clock Select:** This circuit selects the appropriate clock source from the Office Timing Unit (OTU) according to which bank is currently using the DTU. If an OTU is not needed, this circuit selects the internal clocks provided by the master clock generator.

**Master Clock Generator:** This circuit provides all of the timing signals and clocks for the DTU based on the incoming sync and clock from the selected TRU or clocks from the OTU. The OTU clocks are used for access to the Dataport Channel Units (AUA34 and AUA52); otherwise, the necessary clocks are generated by counting down the 4-MHz clock input from the selected TRU.

**Command MUX Circuit:** This circuit allows either bank controller to gain full control over the DTU. It also provides protection in case both should try to gain control at the same time.

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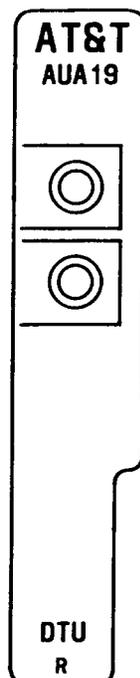


Fig. 2—AUA19 DTU-R Faceplate Diagram