TECHNICAL DESCRIPTION

AT&T

Transmission Systems

DIGITAL ACCESS AND CROSS-CONNECT SYSTEM II (DACS II) RELEASE 6.0

General

This document provides an overview of the AT&T DACS II Release 6.0 features and capabilities. In addition to supporting the extensive set of features available in the preceeding DACS II Releases, Release 6.0 provides global (U.S. and international) Electromagnetic Compatibility (EMC) compliance, 1.544 Mbit/s ANSI/Bellcore compliant Performance Monitoring, in-service roll of DS1/DS0, Nx64 Kbit/s Test Access, and numerous CCITT compliant 2 Mbit/s interface enhancements.

Organization

This Customer Information Release (CIR) – Technical Description consists of a cover sheet and an attachment which contains the detailed information for the DACS II Release 6.0 features and capabilities.

DACS II Documentation

Additional documentation on DACS II may be ordered from the AT&T Customer Information Center by calling 1-800-432-6600 (1-800-432-8432 for CIRs).

Distribution

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ATTACHMENT
Digital Access and Cross-Connect System II Release 6.0 Technical Description

CONTENTS

List of Figures

ATTACHMENT
Digital Access and Cross-Connect System II Release 6.0 Technical Description

1. INTRODUCTION

This document provides an overview of the AT&T DACS II Release 6.0 features and capabilities. In addition to supporting the extensive set of features available in the preceeding DACS II releases, Release 6.0 provides global (24 and 30 channel) Electromagnetic Compatibility (EMC) compliance, ANSI/Bellcore compliant Performance Monitoring, in-service roll of DS1/DS0, Nx64 Kbit/s Test Access, and numerous 2 Mbit/s interface enhancements.

2. PRE-RELEASE 6.0 FEATURES

All of the DACS II features provided in releases prior to Release 6.0 are listed in Appendix 1.

3. Electromagnetic Compatibility (EMC) Compliance

Beginning with Release 6.0, DACS II will be offered in two additional frame configurations, an EMC compliant Enclosed Capacity Expansion Frame (ECEF) and an EMC compliant Enclosed Single Bay Frame (ESBF). These frames are cabinetized versions of the DACS II Capacity Expansion Frame (CEF) and Single Bay Frame (SBF) measuring 600mm X 600mm X 2200mm (23.6"x23.6"x86.6") per bay. Frame extensions will be available to increase the height of the frame to 2600mm (102.3"). See Figure 1 for ECEF Bay Dimensions.
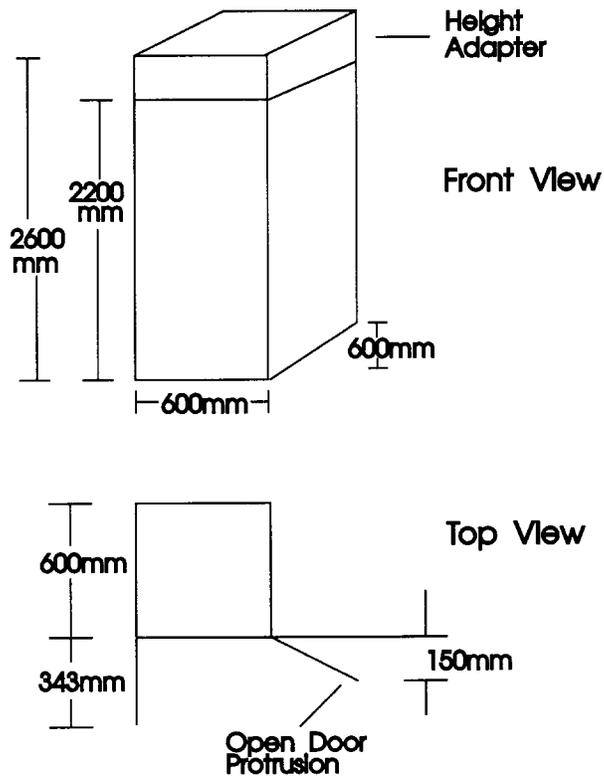
Figure 1 — ECEF Bay Dimensions

In general, frame layout (i.e. Unit and Circuit Pack locations) in the ECEF are the same as for a similarly equipped CEF. Some differences exist, however, between the switch bay layouts of the ECEF and CEF. Switch bay layout for the ECEF is shown in Figure 2.

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┌─────────────────┐
│                 │
│     ECCN 1      │
│                 │
├─────────────────┤
│   TTY & STATUS  │
├─────────────────┤
│                 │
│     ECCN 0      │
│                 │
├─────────────────┤
│                 │
│   F&A PANEL     │
├────────┬────────┤
│        │  SYNC  │
├────────┴────────┤
│                 │
│      MAIN       │
│   CONTROLLER    │
├─────────────────┤
│    MISC. T.S.   │
└─────────────────┘
```
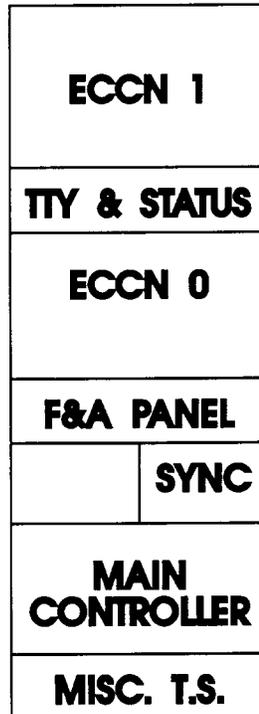
Figure 2 — Switch Bay for ECEF

Cabinet doors are provided on the front and rear of each bay to provide access to the circuit packs and cabling. Doors are removable without tools if more open access is required. Since the Status and Alarm Panel on the Switch Bay is not visible when the cabinet doors are closed, visual indication of power and alarms is provided by a series of indicator lamps mounted at the top of the Switch Bay. These indicators include power, critical alarm, major alarm, minor alarm, and Main Controller major alarm.

The main controller for the ESBF will utilize the same Expanded Frame Controller as the CEF and ECEF. ECEFs and ESBFs will comply with the following standards:

1. FCC, Part 15 of Chapter 1 of Title 47 of the Code of Federal Regulations for Class B equipment.

2. International Electrotechnical Commission (IEC): Electromagnetics Compatibility for Industrial Process Measurement and control Equipment, Publication 801

3. IEC C.I.S.P.R.[1] Publication 22

4. European standard EN 55022

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1. C.I.S.P.R. - International Special Committee on Radio Interference

5. American National Standards Institute (ANSI) T1.308-1990

6. Bell Communications Research (Bellcore) EMC requirements, TA-NWT-001089

Where standards differ in allowable interference criteria, DACS II is designed to be compliant with the more stringent requirement, regardless of which standard they are derived from.

4. ENHANCED DS1 INTERFACE

4.1 Description

An enhanced DS1 interface is provided in a new, software downloadable Enhanced Dual Digroup Card (EDDC) circuit pack (TG-191) that supports ANSI T1.403 and Bellcore TR-TSY-000820 Performance Monitoring (PM). This capability is also provided for DS1s embedded within DS3s through the use of the new Enhanced Multiplexer (EMXR) and Enhanced Multiplexer Interface Units (EMIU) circuit packs.

In addition to the enhancements provided by the EDDC, EMXR and EMIU, these circuit packs will support many of the Pre-Release 6.0 Network Processing Circuit (NPC) types. Those NPC types which will be supported are described in Table 1.

Circuit Pack	NPC Type							
	DE/TE	DE/TE Unframed Clear-DS1	DE ZBTSI	DS SLC 96 w/DL	DS SLC 96 w/o DL	DS SLC 5	DA/TA Framed Clear-DS1	DA/TA
TG191 (EDDC)	Yes	Yes	Yes	No	Yes	No	Yes	Yes
KCR5/ KCR6 (EMXR/ EMIU)	Yes	Yes	No	No	No	No	Yes	Yes
KCR5 (EMXR)	Yes	Yes	No	No	Yes	No	No	No

Table 1. DACS II Release 6.0 DS1 Signal Processing Hardware and NPC Type Summary

4.2 DS1 Performance Monitoring

Performance monitoring, data storage and retrieval is compliant with Bellcore TR-TSY-000820. This specification identifies the Near End and Far End DS1 PM parameters to be monitored as well as the data collection intervals for these PM data. ANSI T1.403 defines the requirements for broadcast and receipt of PM data as well as the initiation of loopbacks.

DACS II Release 6.0 support of ANSI T1.403 includes:

• Generating/Terminating the ANSI T1.403 ESF data link DS1 performance reports

• Calculation and storage of Far End performance data

• Initiation of ANSI T1.403 compliant Far End loopbacks

Using the EDDC and EMXR/EMIU, DACS II provides line and path performance monitoring on directly terminated 1.5 Mbit/s facility lines, and path performance monitoring on 1.5 Mbit/s signals embedded within 45 Mbit/s signals. The performance data are stored in 15 minute and 24 hour intervals, and may be retrieved for analysis by an external user or operations system.

The following performance parameters are monitored and stored by the new circuit packs:

- Near End 1.5 Mbit/s Line Performance Parameters

    — Coding Violations (CV)
    This parameter is a count of the line coding violations (e.g., bipolar violation).

    — Errored Seconds (ES)
    This parameter is a count of seconds during which at least one line CV has occurred.

    — Severely Errored Seconds (SES)
    This parameter is a count of seconds during which 1544 or more line CVs have occurred. This number corresponds to an approximate BER of 10^{-3}.

- Far End 1.5 Mbit/s Line Performance Parameters[2]

    — Errored Seconds (ES)
    This parameter is a count of seconds during which at least one far end line CV has occurred. The far end CV data are communicated to the near end via the Extended Superframe data link.

- Near End 1.5 Mbit/s Path Performance Parameters

    — Coding (CRC-6) Violations (CV)
    This parameter is a count of detected CRC-6 CVs (or a count of detected framing errors for non-Extended Superframe formats).

    — Errored Seconds (ES)
    This parameter is a count of seconds during which at least one of the following has occurred: a path CV, a controlled slip, or a severely errored framing event.

    — Severely Errored Seconds (SES)
    This parameter is a count of seconds during which at least one of the following has occurred: 320 or more CRC-6 CVs or a severely errored framing event. For non-Extended Superframe formats, the occurrence of 8 or more framing errors may be substituted for the 320 CRC-6 CVs.

    — Severely Errored Framing Seconds (SEFS)
    This parameter is a count of seconds during which at least one severely errored framing event has occurred. A severely errored framing event is defined as: 2 or more framing bit errors within a 3 millisecond period (often referred to as an out of frame condition).

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2. The far end performance parameters are communicated to the near end via the Extended Superframe data link as defined in ANSI T1.403.

— Controlled Slip Seconds (CSS)
This parameter is a count of seconds during which a controlled slip has occurred.

— Unavailable Seconds (UAS)
This parameter is a count of seconds during which the 1.5 Mbit/s signal is deemed unavailable (e.g., during a loss of frame condition).

• Far End 1.5 Mbit/s Path Performance Parameters

The far end path performance parameters are based on far end CRC-6 CV counts that are communicated to the near end via the Extended Superframe data link. The CVs are not communicated as exact counts but rather as a range of counts in compliance with ANSI T1.403. For example, if 40 far end CRC-6 errors were detected in a 1 second interval, the far end would indicate (via the data link) that between 11 and 100 CRC-6 errors were detected. The near end would, therefore, always have the worst case assessment of the far end performance (e.g., DACS II would assume 100 CRC-6 errors in the above example). The following far end path performance parameters are monitored and stored by DACS II.

— Coding Violations (CV)
This is a count of Path Coding Violations (i.e., Bipolar Violation).

— Errored Seconds (ES)
This parameter is a count of seconds during which a far end path CV is reported.

— Severely Errored Seconds (SES)
This parameter is a count of seconds during which the far end reports 320 or more CRC-6 CVs.

— Severely Errored Framing Seconds (SEFS)
This parameter is a count of seconds during which at least 1 far end severely errored framing event is reported.

— Controlled Slip Seconds (CSS)
This parameter is a count of seconds during which a far end controlled slip is reported.

— Unavailable Seconds (UAS)
This parameter is a count of seconds during which the far end 1.5 Mbit/s signal is deemed unavailable.

4.3 1.5 Mbit/s Performance Data Storage

DACS II monitors the above performance parameters and stores their counts for future retrieval as required by Bellcore TR-TSY-000820. These data storage intervals are listed below.

• 15 minute intervals:

— Current 15 minute interval,

— Previous 15 minute interval,

— Additional 95 most recent 15 minute intervals.
Note that this exceeds Bellcore requirement of additional 31 most recent 15 minute intervals (i.e. 8 hours of historical data).

- 24 hour intervals:
  - — Current 24 hour interval,
  - — Previous 24 hour interval,
  - — 6 most recent 24 hour intervals.

Each of the performance parameters has thresholds for the current 15 minute interval and the current 24 hour interval. When a threshold is exceeded, an autonomous message is broadcast over the DACS II administrative link. Each performance parameter may be assigned one of 4 software settable threshold values for generating the autonomous message. When provisioning a 1.5 Mbit/s interface, the user can select one of the four threshold options for each performance parameter on that particular 1.5 Mbit/s interface.

DACS II provides the following capabilities to retrieve and maintain the 1.5 Mbit/s performance data.

- Display the current count for all performance parameters for selected transmission links

- Display the current count of a particular parameter for selected or all transmission links

- Display the desired history of counts for a particular parameter of selected transmission links

- Clear the count of a particular parameter for selected or all transmission links

- Clear the count of all parameters for a selected transmission link.

The display of counts and alarm state of selected transmission links can also be scheduled for time of day execution. In addition, a status command is also available that gives a summary of the status of a specified 1.5 Mbit/s signal, including the alarm state, all parameter counts, options selected, and performance threshold settings.

4.4 1.5 Mbit/s Loop Back

In compliance with ANSI T1.403, DACS II provides the ability to initiate and terminate the following far end 1.5 Mbit/s loop backs.

1. Line Loop Back (LLB)
2. Network Loop Back (NLB)
3. Payload Loop Back (PLB)

The far end loop back commands are initiated and terminated via the standard DACS II administrative interface (i.e., PDS or MML commands). Upon receiving a request to initiate a far end loop back, DACS II uses the Extended Superframe data link and/or inband signaling to direct the identified far end equipment to execute/terminate the loopback.

In addition to requesting far end loop backs, DACS II can also perform a near end payload loop back in compliance with ANSI T1.403. That is, upon receiving a data link payload loop back command from the far end equipment or via a local administrative command, DACS II will loop the received payload back onto the facility. When the loop back is terminated, DACS II automatically returns the existing connections to their

previous states.

NOTE: Both near end and far end loop backs are service affecting and should only be used for out of service maintenance.

4.5 1.5 Mbit/s Test Signal Injection

The new DACS II EDDC and EMIU circuit packs provide the ability to inject 1.5 Mbit/s test signals onto existing, provisioned 1.5 Mbit/s facilities. The test signals may be used in conjunction with the far end loop back features to perform single ended facility maintenance.

The four 1.5 Mbit/s test signals that DACS II can inject are:

1. Yellow Signal:
   Since this signal is transmitted in the Extended Superframe data link, it may be used in conjunction with the remaining test signals. However, when using the Superframe or T1DM framing formats, the yellow signal is actually passed via the data channels. Consequently, users may not use other 1.5 Mbit/s test signals with the Superframe or T1DM yellow signal.

2. High Ones Density Test Signal:
   This signal consists of all ones in the payload bits with valid 1.5 Mbit/s framing.

3. Low Ones Density Test Signal:
   This signal consists of a repeating eight bit pattern of (00000001) with valid 1.5 Mbit/s framing.

4. Quasi-Random Test Signal:
   A 1,048,575 bit sequence generated by a 20 stage shift register as defined in ANSI T1.403, with valid 1.5 Mbit/s framing.

In addition to the test signals, the new EDDC and EMIU circuit packs enable DACS II to send the following in-band signals to control far end loopbacks:

1. In-band Loop Back Activate Signal:
   This signal consists of a repeating bit pattern of (00001) lasting for 5 to 8 seconds with valid 1.5 Mbit/s framing.

2. In-band Loop Back Deactivate Signal:
   This signal consists of a repeating bit pattern of (001) lasting for 5 to 8 seconds with valid 1.5 Mbit/s framing.

Once the test signal activation command is received and executed by DACS II, the test signal remains on the line until it is deactivated by a subsequent user command.

DACS II always applies downstream trunk conditioning before it begins transmitting the requested test signal.

5. DS1/DS0 In-Service Roll

5.1 Description

DACS II Release 6.0 DS0 and DS1 Roll features provide a means to roll live service from one DS1 facility to another. The standard procedure for performing these rolls is as follows:

1. Bridge the existing service onto the new facility at each DACS II.

2. Switch the received signal from the old facility to the new facility at both DACS IIs. This step does not need to be coordinated between the two DACS IIs.(i.e., no need for coordinated "1-2-3 Switch!")

3. Remove the remaining bridge to the old facility.

Figure 3 displays the Roll procedure.
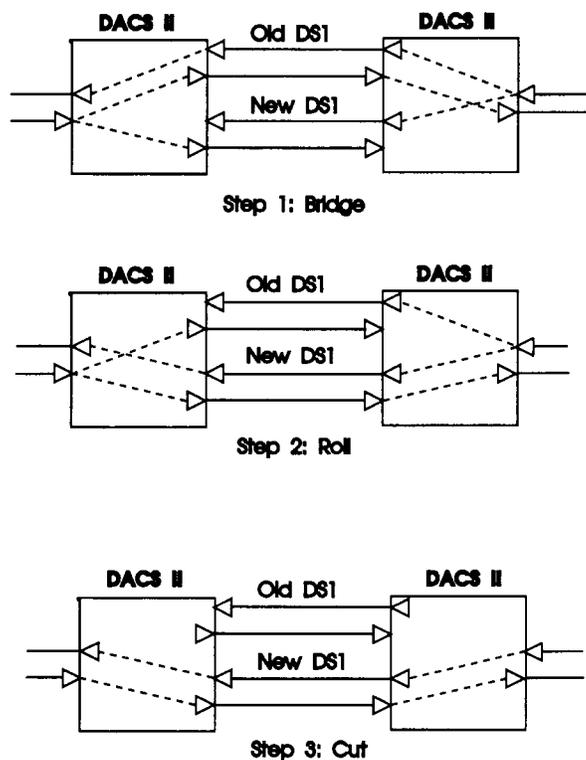
Figure 3 — DS1 Roll Procedure

For DS1 rolls, steps 1 and 2 may be combined in a single step. This capability would be useful in restoring DS1 service that has already been lost.

5.2 Benefits

5.2.1 DS0 Roll

Rearrangement of customer's networks can generate numerous service orders each

month which frequently involve grooming of DS0s to maximize DS1 facility fill. The present method of moving DS0s (i.e. Disconnect command followed by Crossconnect to the new circuit) causes an outage in the customer application. Consequently, the network provider must generally obtain a release from the customer before the circuit can be moved. This results in lost time waiting for the customer release, and then waiting again for the scheduled time. The DS0 Roll feature allows rearrangement of DS0s or groups of DS0s with service "hits" of less than one millisecond per DS0. (If the new and old service paths are different lengths, additional application degradation may result due to changes in delay. The period of potential degradation starts when one end of the facility is Rolled and ends when the other end is Rolled). This frees network providers to schedule service order work during off-peak hours, at their convenience.

5.2.2 DS1 Roll

The two major applications for the DS1 Roll are rolls due to Facility and Hardware provisioning or maintenance activity. The two applications are discussed below.

5.2.2.1 Facility Rearrangement
Like DS0 Roll, DS1 Roll allows rapid rearrangement of 24 DS0s or a Clear DS1 with service outages less than 24 milliseconds per DS1. (If the new and old service paths are different lengths, additional application degradation may result due to changes in delay. The period of potential degradation starts when one end of the facility is rolled and ends when the other end is rolled.) This feature is a logical extension of the DS0 Roll feature, providing the same capability for 24 Channels or Clear DS1 circuits terminating on the DACS II.

A 24 DS0 channel version of the DS1 Roll feature would also be useful in converting facilities from one framing format to another (i.e. from D4 or T1DM framing formats to ESF with B8ZS).

Further, DS1 Roll can be used to quickly restore a channelized DS1 (24 DS0 channels) to full service in the event of facility degradation or failure.

5.2.2.2 Hardware Upgrades and Failures

The second major benefit derived from the DS1 Roll feature consists of the ability to more easily perform in-service replacement of a faulty Dual Digroup Card (DDC) or upgrade the DDC for a new release. The present operating procedure for upgrading or maintaining DDCs involves removing the circuit from service while the card is being changed. The DS1 Roll feature would allow the in-service facility to be rolled to another NPC while the service NPC is being changed. Once the original card is replaced and returned to service, the facility can be rolled back to its assigned port. Service interruptions lasting less than 24 milliseconds would occur during the facility roll to the temporary card and during the roll back to the new card. This feature could be used by any service using facilities that terminate on DS1 interface cards on the DACS II.

6. Nx64 Kbit/s Test Access (for 1.544 Mbit/s and 2.048 Mbit/s

6.1 Description

The DACS II Release 6.0 Nx64 Kbit/s test access feature will allow customers to grow and reconfigure up to 400 Nx64 Kbit/s Test Groups (TGs) on DACS II. A TG is composed of two separate bundles of N 64 Kbit/s channels. These bundles are referred to as the East bundle and the West bundle of the TG and allow an Nx64 Kbit/s circuit to be tested simultaneously in both directions of transmission. Once the TGs are

grown, test access sessions will operate in a manner similar to current 64 Kbit/s test access on DACS II (i.e., circuit monitor, split, etc. will operate as with current 64 Kbit/s test access). Customers will be able to gain Nx64 Kbit/s test access regardless of the service channel arrangement within the facility (i.e., the service channels may be contiguous, alternate, or random within the facility).

The Nx64 Kbit/s test access feature will allow customers to test Nx64 Kbit/s services with value of N ranging between 1 and 24 for DS1s and 1 and 31 for 2 Mbit/s interfaces.

In addition to the maximum of 400 TGs, DACS II Release 6.0 will continue to support creation of Test Ports (TPs) and Test Access Digroups (TADs or NPCTPs). The maximum number of NPCTPs has been increased to 8 in Release 6.0 (up from the maximum of 4 provided for in previous releases) yielding a total of up to 96 TPs.

6.2 Benefits

Prior to Release 6.0, DACS II test access capabilities for a testable Nx64 Kbit/s service could be no greater than 768 Kbit/s (12 64 Kbit/s channels). This limit was due to the previous configuration limits of DACS II Test Access Digroups (TADs)[3]. Previously, DACS II only provided for TADs (i.e., NPCTPs) which were "hardcoded" to support at most 12 64 Kbit/s test ports per NPCTP. Because service providers may offer Nx64 Kbit/s services where N can be as high as 24 (DS1) or 31 (2 Mbit/s), DACS II Release 6.0 with NxDS0 test access capability can meet those needs also.

Since Nx64 Kbit/s services require multiple 64 Kbit/s Test Ports (there are a total of 48 64 Kbit/s TPs available on a Pre-Release 6.0 DACS II frame), DACS II test access capacity can be depleted very quickly when testing Nx64 Kbit/s services.

Previously, subject to the 768 Kbit/s maximum, NxDS0 test access would require N different commands for each test mode (monitor, split, etc.). test access session would require time consuming and error prone user input and coordination. The Release 6.0 NxDS0 test access feature eliminates the need for time consuming and detailed coordination and streamlines the NxDS0 test set up when compared to previous methods.

7. 2 Mbit/s Interface Enhancements

7.1 Enhanced 2 Mbit/s Performance Monitoring

DACS II Release 6.0 provides enhanced 2 Mbit/s performance monitoring similar to the DS1 PM enhancements described above. This feature requires the Enhanced Dual Primary Card (EDPC) circuit pack.

The 2 Mbit/s line interfaces measure a large number of performance parameters of the digital signal. DACS II performance monitoring principally complies with the recommendations in the CCITT "Blue book". However, adaptations on the "blue book" have been made in the meanwhile which required deviation from the recommendations as laid down in the "blue book". As an example, G.821 is expected to disappear in favor of a new G.82X (number yet unknown). Development of the PM feature has followed the new CCITT initiatives. The following parameters are accumulated/calculated per 2

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3. The term TAD is used here in a generic sense and covers both 64 Kbit/s and Nx64 Kbit/s test access. The terms Network Processing Circuit Test Port (NPCTP) and NPC Test Group (NPCTG) are used to differentiate between 64 Kbit/s TADs and Nx64 Kbit/s TADs respectively.

Mbit/s facility.

7.1.1 Error Count Parameters

- Code violations (CV)
  The CV count is incremented every time a code violation is detected. DACS II monitors and accumulates the CV in addition to converting it into an error rate estimate for alarm reporting.

- Framing error count (FRER)
  The FRER count is incremented every time a framing error is detected. The FRER is also used to provide an error rate estimate for alarm reports.

- Unavailable time count (UATC)
  A period of unavailable time (UAT) begins when the bit error ratio in each second is worse than 10E-3 for a period of 10 consecutive seconds. These 10 seconds are considered unavailable time. A new period of available time begins at the first second of a period of 10 consecutive seconds each having an error rate better than 10E-3. The UATC count is incremented every time a period of unavailable time is entered.

- CRC4 block error count (CRC)
  The CRC count is incremented every time a CRC block error is detected.

7.1.2 Errored Interval Parameters

- Controlled Slip Seconds (CSS)
  The CSS is incremented for every 1-second interval with one or more slip defects.

- Out of Frame Seconds (OFS)
  The OFS is incremented for every 1-second interval with one or more Loss of frame defect. Continuous Loss of frame defects are counted as one defect, in this case the OFS count is incremented for each 1-second of continuous Loss of Frame.

- Errored Seconds (ES)
  The ES is incremented for every 1-second interval with one or more of the following conditions: CV, slip, LOS, LOF, AIS framing error, or CRC4 block error.

- Severely Errored Seconds (SES)
  The SES is incremented for every 1-second interval with one or more of the following conditions: 2048 CVs, slip, LOS, LOF, AIS, 100 distributed (or a user defined number) FAS or CRC-4 block errors.

- Unavailable Seconds (UAS)
  The UAS count is incremented for every 1 second interval in an UAT period.

- Multiframe Alignment Errored Second (MER)
  The MER count is incremented for every 1-second interval with 1 or more CTS16 multiframe alignment errors.

7.1.3 Remote (Far end) Performance Parameters

For framed 2 Mbit/s facilities it is also possible to accumulate some far-end performance parameters by using the received E-bits (or international bits) in the CRC-4 multiframe word. The following parameters are stored:

- Far End Block Error Count (FEBE)
  FEBE is incremented whenever an E-bit is recieved in the "0" state.

- Far End Errored Seconds (FES)
  The FES count is incremented every time one or more FEBE occur in a one second interval.

- Far End Severely Errored Seconds (FSES)
  The FSES count is incremented every time a user provisionable number of FEBEs occur in a one second interval.

- Far End Unavailable Seconds (FUAS)
  FUAS is similar to UAS only it is calculated using FSES rather than SES.

7.1.4 2 Mbit/s Performance Data Management

DACS II collects and stores the performance parameters in 15 minute and daily intervals as required per CCITT rec. G.784. For each collection interval, current and previous registers are kept to provide a history of the parameter. As an example, the following registers are kept for coding violations:

Current 15 minute interval, previous 96 15 minute intervals, current day and 7 previous days.

All current parameters have associated thresholds that, when exceeded, result in an autonomous alarm message. Message thresholds can be specified on a per-2 Mbit/s link basis from one of four values, either locally or remotely over the administrative links. One of the four values is the system default value while the remaining three values are defined by the user. The daily counts and alarm state of all transmission links are also displayed automatically as part of a daily report. By default the daily report is issued at midnight and all daily parameter counts and alarm state are reported. The time of day for the daily report and the parameters and alarm state to be included in the report are user definable. A status command is also available that gives a summary of the status of a specified port including the alarm state, all parameter counts, options selected, and performance threshold settings.

7.1.5 2 Mbit/s Loopback

The DACS II Enhanced Dual Primary Card (EDPC) circuit packs support the following 2 Mbit/s loop backs.

1. Facility Loop Back

2. Equipment Loop Back

The 2 Mbit/s loop backs are initiated and terminated by user commands entered via the DACS II administrative links. The facility loop back loops the received 2 Mbit/s signal from the incoming facility back onto the facility. The received signal line coding and line timing are both preserved during the facility loop back. This loop back is useful for sectionalizing 2 Mbit/s facility troubles between the DACS II and far end network element.

The equipment loop back loops the transmitted 2 Mbit/s signal from the EDPC pack DACS II back into the EDPC pack. (i.e., the EDPC receives its own transmitted 2 Mbit/s). This loop back includes the line coding and line timing produced by the EDPC and is useful in performing continuity tests through the entire DACS II system.

For both loop backs, the user specifies whether the direction being looped should be transmitted through DACS II (for facility loop back), transmitted onto the 2 Mbit/s facility (for equipment loop back) or be terminated, with AIS transmitted downstream (for both loop backs). Users also specify whether DACS II is to provide 2 Mbit/s performance monitoring on the received signal.

7.1.6 2 Mbit/s Monitor Points

Each 2 Mbit/s output and input signals can be monitored at a monitor point on the front of the Enhanced Dual Primary Card. The signals for both the 75 and 120 Ohm versions of the EDPC are attenuated by 20db +/- 20%. The monitor point is protected against short circuits which will not affect regular transmission on the monitored port.

7.2 Clear 2 Mbit/s Crossconnect and Test Access

DACS II Release 6 supports the following types of clear
2 Mbit/s functions :

- One-way, two point cross-connection

- Two-way, two point cross-connection

- One way broadcast connection

- Two way broadcast connection with switched or looped return

The 2 Mbit/s signal can be either framed or unframed. Two-way and one-way point to point 2 Mbit/s cross-connections are established in the same manner as 64 Kbit/s cross-connections. A two-way, two point connection can be converted to a two-way broadcast circuit by just adding tributaries. A similar process as with 64 Kbit/s broadcasts exists to loop back the input or use a switched return for the return leg. The number of legs in a broadcast is unlimited but only 8 legs can be added at a time.

The Alarm Indication Signal (AIS) for a 2 Mbit/s is standard all '1's and therefore not user programmable as with the 64 Kbit/s idle and alarm patterns.

The difference in performance monitoring between a framed and unframed 2 Mbit/s signal are caused by the absence of time slot 0 and 16 in the unframed signal. This permits, for instance, CRC-4 to be used in a framed signal which provides a number of performance parameters both locally and from the far end. In an unframed signal only code violations, loss of incoming signal and slips will be counted. In addition, framing errors, loss of frame and reception of AIS will be monitored in framed 2 Mbit/s connections.

7.3 2 Mbit/s Time-Slot Zero (TS0) Cross-connect

Prior to Release 6.0, DACS II customers could only crossconnect TS0 spare bits between TS0 channels. When equipped with the EDPC pack, the DACS II Release 6.0 TS0 crossconnect feature allows customers to crossconnect the TS0 spare bits to non-TS0 channels (e.g. TS 1-TS31) on 2 Mbit/s interfaces. This ability enables network management systems to connect to a DACS II 2 Mbit/s port to exchange provisioning and maintenance information with far end network elements. This information is embedded in the TS0 National (Sn) and International (Si) spare bits. The following describes these bits in the TS0 format.

- International bits (Bit 1 of Frame Word and Bit 1 of Non Frame Word).
- National Bits (Bits 4 - 8 of Non Frame word).

Alternate Frames	Bit Number							
	1	2	3	4	5	6	7	8
Frame containing frame alignment signal (FW)	S_i	0	0	1	1	0	1	1
	Note 1	Frame Alignment Signal						
Frame not containing the frame alignment signal (NFW)	S_i	1	RAI	S_n	S_n	S_n	S_n	S_n
	Note 1			Note 2				

Table 2. Allocation of TS0 Bits 1-8

A primary interface can be provisioned for Cyclic Redundancy Check-4 (CRC) or non-CRC.

Note 1: When the primary is provisioned for CRC, the S_i bit positions will contain the encoded CRC word, a CRC multiframe alignment signal, and international bits, as described in CCITT G.704. The international bits are located in frames 13 and 15.

Note 2: S_n are the national bits. In some applications some of these bits may have special uses which make them unavailable for cross-connection. For example, Bit 4 may be used for Remote AIS (RAIS) or Remote Bit Error Rate (RBER) indication, and Bit 5 may be used for for Synchronization Failure Indication (SFI).

A. Cross-connections from TS0 to TS0

    i. When CRC-4 is not used in the "to" (outgoing) TS0 direction : Only bits 1 (S_i) and 4-8 (S_n) of the non frame word (NFW) and bit 1 of the frame word (FW) can be cross-connected. The other bits of TS0 are sourced as indicated in Table 2. In order to keep a proper FW/NFW integrity when cross-connecting the S_i bits, both S_i bits are treated independently.

    ii. When CRC-4 is used in the "to" TS0 : Only bits 4-8 (S_n) of the NFW and bit 1 (S_i) of frames 13 and 15 of the CRC multiframe can be cross-connected. The other bits in TS0 are sourced as indicated in Table 2. CRC multiframe integrity is maintained by cross- connecting the S_i bits independently.

It is not possible to cross-connect the S_i bits in TS0 between a primary that is using CRC and one that is not.

B. Cross-connections from TS0 to any other time slot except TS0.
    When passing TS0 from an incoming facility to an outgoing one, DACS II provides the following necessary functions:

1. Transformation of Frame Alignment Signal

   To prevent false framing at the far end network element, DACS II will allow the user to enter a programmable pseudo framing signal to replace the standard Frame Alignment Signal contained in the Frame Word (Bits 2 - 8, value 0011011). As an option, the Frame Alignment Signal may be overwritten by the Non Frame Word.

2. Manipulation of Cross-Connected Bits

   The TS0 bits which are not part of the Frame Alignment Signal (Bit 1 of the Frame Word and all 8 bits of the Non Frame Word) can be cross-connected to the outgoing channel. For each of these bits the following bit manipulation choices are available to the user:

   a. Pass the bit through as received

   b. Invert the bit

   c. Set the bit to '0', regardless of received value

   d. Set the bit to '1', regardless of received value

C. Cross-connections from any time slot except TS0 to TS0
   When cross-connecting a channel to an outgoing TS0, DACS II provides the following functions:

   1. Frame Alignment Signal Substitution

      In order to generate a proper frame alignment pattern in the outgoing TS0, DACS II must receive a "pseudo frame word" in the channel that is to be connected to a TS0. DACS II can be programmed to recognize the pseudo framing signal generated by the far end equipment and substitute the pseudo framing signal with the real Frame Alignment Signal (Bits 2 - 8 in the Frame Word, value 0011011) before transmitting it to the network element. As an option, the Frame Alignment Signal may be overwritten by the Non Frame Word.

   2. Manipulation of Cross-Connected Bits

      The recognition of the pseudo framing signal received from the network management system enables DACS II to identify the spare bits in the Non Frame Word. The international bits (Bit 1 of the Frame Word and Bit 1 of the Non Frame Word) and the national bits (bits 4 - 8 of the Non Frame Word) can all be cross-connected unless they are used for other specific purposes (i.e. RAIS in bit 4 or SFI in bit 5). For each of the cross-connected bits the following bit manipulation choices are available to the user:

      a. Pass the bit through as received

      b. Invert the bit

      c. Set the bit to '0', regardless of received value

      d. Set the bit to '1', regardless of received value

7.3.1 2 Mbit/s Alarms and Fault Conditions

DACS II detects the following fault conditions for each 2 Mbit/s link, consistent with CCITT Recommendations:

- Loss of incoming 2 Mbit/s signal
- Loss of 2 Mbit/s frame alignment
- Alarm Indication Signal (AIS) received
- Remote Alarm Indication received from remote end
- High Error Rate (10E-3 and 10E-5)
- Synchronization Alarm (Bit 5 of TS0 non-frame word)
- Remote AIS
- Remote High Error Rate (10E-5)
- Loss of CRC multiframe alignment (Auto CRC only)
- Far-end loss of CRC multiframe alignment (Auto CRC only)
- Pseudo Frame Word out of Frame

If TS16 is used to carry channel associated signaling information, then the following additional alarm conditions are detected, consistent with CCITT Recommendations:

- Loss of multiframe alignment
- Alarm indication received from remote time slot 16 equipment
- Remote multiframe alarm

7.3.2 2 Mbit/s Consequent Actions

The consequent actions for each of the fault conditions listed above comply with the relevant clauses of CCITT Recommendations. Per CCITT Recommendations, AIS is inserted and the Remote Alarm Indication is activated where necessary. Reporting of alarm conditions is based on a 48 millisecond scan time within the 2 Mbit/s port interface equipment and is generally available for activation of station alarms and reporting over administrative links 144 milliseconds after detection.

8. GLOSSARY

Term	Definition
AIS	Alarm Indication Signal
ANSI	American National Standards Institute
BER	Bit Error Rate
CCITT	Comite Consultatif International Telegraphique et Telephonique
CEF	Capacity Expansion Frame
CEPT	Conference Europene des Postes Telecommunications
CRC	Cyclic Redundancy Check
CSS	Controlled Slip Seconds
CV	Coding Violation
DACS	Digital Access and Cross-Connect System
DDC	Dual Digroup Circuit
DL	Data Link
DPC	Dual Primary Circuit
DSP	Digital Signal Processor
DSPU	Digital Signal Processing Unit
ECEF	Enclosed Capacity Expansion Frame
EDDC	Enhanced Dual Digroup Circuit
EDPC	Enhanced Dual Primary Circuit
EFC	Expanded Frame Controller
EMC	ElectroMagnetic Compatibility
EMIU	Enhanced Multiplexer Interface Unit
EMXR	Enhanced Multiplexer
ES	Errored Seconds
ESBF	Enclosed Single Bay Frame
ESD	ElectroStatic Discharge
ESF	Extended SuperFrame
FAS	Frame Alignment Signal
FCC	Federal Communications Commission
FDL	Facility Data Link
FEBE	Far End Block Error
FES	Far end Errored Seconds
FRER	Framing (bit) Error
FS	Failed Seconds
FSES	Far end Severely Errored Seconds
FUAS	Far end Unavailable Seconds
FW	Frame Word
IEC	International Electrotechnical Commission
LLB	Line Loop Back
MC	Main Controller
MIU	Multiplexer Interface Unit
MML	Man Machine Language
MXR	Multiplexer
NFW	Non Frame Word
NLB	Network Loop Back
NPC	Network Processing Circuit

NPCTG	NPC Test Group
NPCTP	NPC Test Port
OFS	Out of Frame Seconds
PDS	Program Documentation Standards
PLB	Payload Loop Back
PM	Performance Monitoring
RAIS	Remote Alarm Indication Signal
RBER	Remote Bit Error Rate
SBF	Single Bay Frame
SEFS	Severely Errored Framing Seconds
SES	Severely Errored Seconds
SFI	Synchronization Failure Indication
SLC®	Subscriber Loop Carrier®
SRDC	Subrate Data Cross-connect Capability
TAD	Test Access Digroup
TD	Technical Description
TG	Test Group
TP	Test Port
TS0	Time Slot Zero
UAS	UnAvailable Seconds
UAT	UnAvailable Time
UATC	UnAvailable Time Count

Appendix I. DACS II Pre-Release 6.0 Features

RELEASE 2 FEATURES

The features in DACS II Release 2 are listed here. For a description of these features refer to DACS II Release 2 TD (CIR 365-099-055 TD, May 1988, Issue 1).

- Enhanced Administrative Features
  1. X.25 Protocol over the Data Link Interface
  2. CCITT Human-Machine Language (TL1 based)
  3. I/O Screening, Command Prioritization, and Security via Login Passwords
  4. Macro Commands
  5. Alternate Maps for Rapid Configuration of 2-Way-2-Point Cross-Connections

RELEASE 3 FEATURES

The features in DACS II Release 3 are provided in multiple releases and are listed below. For a description of these features refer to DACS II Release 3 TD (CIR 365-099-093 TD, September 1989, Issue 1).

- Digital Signal Processing Features
  1. Subrate and 56 Kb/s Multipoint Processing
  2. Subrate Multiplexing
  3. Subrate and 56 Kb/s Error Correction
  4. Subrate and 56 Kb/s Cross-connection
  5. Subrate and 56 Kb/s Secondary Channel Processing
  6. Subrate and 56 Kb/s Test Access
  7. C-bit Processing For CEPT Terminations
- Facility Types
  1. SLC® 96 Mode III
  2. CEPT Interface
  3. SLC® 96 Mode I Pass Through to TR-08 Digital Switch (5ESS™ Switch, DMS 100)
  4. SLC® Series 5 FPC Specials Only
  5. Zero Byte Time Slot Interchange (ZBTSI)
- General Features
  1. Feature Packaging
  2. Interface to SLC® Series 5 CIU (Provisioning)

3. Enhanced CEPT Features

4. CEPT (2.048 Mb/s)/DS1 (1.544 Mb/s) Gateway

RELEASE 4.0 FEATURES

The DACS II Release 4.0 features are listed here. For a description of these features refer to Release 4.0 TD (CIR 365-099-105TD, March 1990, Issue 1).

*   Asynchronous DS3 Termination

*   DACS II Interface Unit Capability

*   Flexible Bay Configurations

*   Clear DS1 Cross-Connection

*   DS1 Test Access

RELEASE 4.1 FEATURES

The DACS II Release 4.1 features are listed here. For a description of these features refer to Release 4.1 TD (CIR 365-099-112TD, December 1990, Issue 1).

*   Integrated Facility Terminating Unit (IFTU)

*   Fully Flexible Frame Configuration

*   5:4 SLC® System Interface

*   SLC® System Mode 1 "Standalone" Operation Programmable Alarm Indication Signal (AIS) Alarm

*   Eight-Character User Identifier Enhancement

RELEASE 5.0 FEATURES

The DACS II Release 5.0 features are listed here. For a description of these features refer to Release 5.0 TD (CIR 365-099-111TD, November 1990, Issue 1).

*   DACS II Capacity Expansion Frame (CEF)

*   Fully Flexible Configuration [With Integrated Facility Terminating Unit (IFTU)]

*   Internal Cable and Backplane Testing

*   CEF Retrofit

RELEASE 5.1 FEATURES

The DACS II Release 5.1 features are listed here. For a description of these features refer to Release 5.1 TD (CIR 365-099-124TD, November 1991, Issue 1).

*   Software Convergence for CEF and Non-CEF Hardware

*   High-speed Enhanced Communications Interface

- Provisionable XON/XOFF Snider Links
- Provisionable ENQ/ACK Snider Links
- X.25 Feature Enhancements
- Tape Use Counter
- Tape Cleaning Enhancement