D1D CHANNEL BANK
DESCRIPTION
DIGITAL TRANSMISSION SYSTEMS

CONTENTS PAGE

CONTENTS PAGE

1. GENERAL

1.01 This section describes the D1D channel bank on a block diagram level and provides functional descriptions of the plug-in units for the channel bank. The alarm features of the channel bank and the bays used to mount the channel banks are also described.

1.02 This section is reissued for the following reasons:

(a) To correct the part number for the D1A channel bank label.

(b) To include the caution label for the J86498A power supply when used with a No. 4 ESS power plant.

(c) To add a figure for the J86498A power supply caution label.

Revision arrows are used to emphasize the more significant changes. Equipment Test List are not affected.

1.03 The D1D channel bank (Fig. 1) is a carrier terminal used for processing 24 voice-frequency channels into a 1.544-Mb/s bitstream, using pulse code modulation (PCM). PCM is described in Section 365-010-100. Transmission between terminals is over a digital transmission facility such as the T1 digital line (Section 365-200-100).

1.04 The D1D channel bank provides direct, tandem, and toll-connecting trunk facilities on an end-to-end basis with any terminal equipment that has a compatible DS1 interface as well as with another D1D channel bank. In addition, an existing D1-type facility can be converted for use with a D3 or D4 facility, rather than installing new terminal equipment. The D1D channel bank can be formed at an unequipped bay or a D1A or D1B channel bank can be converted to a D1D channel bank. The only essential requirement is that the bay be equipped with the K (or D1B-type) wiring option, (paragraph 5.03). The conversion (Section 365-116-501) is done by substituting 12 common plug-in units, which are distinguished from units common to other D1-type channel banks by the overall blue color of the faceplates (Fig. 2). In the text which follows, reference is made to the D1B channel bank only rather than the D1A/B channel bank.

1.05 There are two categories of plug-in units in the D1D channel bank: channel units and common units. Channel units serve individual channels and are peculiar to the type of trunk application. Common units serve many channels and do not depend on the types of assigned trunks.

1.06 The D1D channel banks are mounted in J98711A, B, and C bays which are also employed for D1B channel banks.

1.07 The -48 volt office battery is the source for the dc-to-dc power converter in the D1D channel bank. Undervoltage, overvoltage, and interlock protective arrangements are provided. Normal operation is obtained over an office battery range of -42.75 to -52.5 volts.

1.08 The 1.544-Mb/s clock is usually generated internally in the D1-type channel bank. Certain applications of the D1D channel bank require that the clock be supplied externally. Other applications require that the terminal be loop-timed; that is, the outgoing clock is derived from the incoming bitstream. Either of these arrangements requires additional modifications to the channel bank as described in paragraph 2.08.

2. DESCRIPTION

2.01 Although the D1D channel bank is similar to the D1B channel bank, the two are not compatible because of the difference in encoding and in the line format produced by these channel banks. The D1D channel bank uses a nonlinear encoder whereas the D1B channel bank does not. The line format transmitted by these channel banks can be compared on the basis of the recurring frames, which consist of digital bits containing information for 24 channels in a fixed period of time (125μ seconds). The frame format, which is formed by time division multiplexing in the D1D channel bank, can be seen in Fig. 3. In the D1D channel bank, five consecutive frames are used to transmit message information, and the sixth frame is used for message and signaling information. In this way eight bits are available to transmit the message information for 5/6 of the time and seven bits are available 1/6 of the time. In the D1B channel bank, only seven bits of each frame are available for message information, since one of the bits (D1) is always dedicated to signaling. Because of the extra bit available for encoding, the D1D channel bank offers improved transmission quality over the D1B channel bank.

2.02 The description of the D1D channel bank can be divided into descriptions of the timing section, the transmitting section, and the receiving section.

A. Timing Section

2.03 To obtain accurate sampling, multiplexing, coding, and unipolar-to-bipolar conversion in the D1D transmitter and accurate bipolar-to-unipolar conversion, decoding, and demultiplexing in the receiver, accurate timing circuits based on PCM requirements are used. Timing is based on the number of channels per channel bank (24), the channel sampling rate (8000 per second), the number of PCM digits per channel sample (8), and the framing digit rate (8000 per second). Thus, the basic pulse repetition rate is obtained by taking 24 x 8000 x 8 + 8000 = 1,544,000.

2.04 The transmitting timing circuits (Fig. 4) consist of a transmit clock, a digit generator, and a channel counter. These circuits generate all timing signals required by the voice and signaling transmitting circuits; they also generated a series of framing pulses that are used by the distant-end receiver to maintain synchronism with the local transmitter.

2.05 A 6.176-MHz crystal oscillator in the transmit clock circuit is used as the source of precise timing signals. This stable frequency is reduced by a frequency divider to 1.544 MHz, the frequency required for the D1D channel bank. The output from the transmit clock is used for accurate timing of the transmitting converter and the digit generator. The digit generator is used for generating the eight digits (D1 through D8) used by the encoder to form the PCM code groups that represent pulse amplitude samples and signaling plus the framing digit (D9) for each 24-channel frame; thus, the digit generator operates at 1.544 MHz. The digit generator also provides pulses for timing the transmitting converter and common signaling circuit at 1.544 MHz for triggering the channel counter at the channel rate of 192,000 (24 x 8000) Hz, and for triggering each transmitting clamp, alternately, at the group rate of 96,000 Hz. The channel counter supplies channel pulses to the signaling scanning gates and the channel gates.

2.06 The receiving timing circuits (Fig. 5) consist of a clock extraction circuit in the receiving converter, a digit generator, a framing detector and a channel counter. These circuits use the basic rate of the incoming PCM train for the generation of all timing pulses required by the voice and signaling circuits. In addition, they use the framing pulses in the incoming PCM train to synchronize the local receiver with the distant-end transmitter.

2.07 The receiving converter contains a clock extraction circuit for recovering the basic PCM rate (1.544 MHz) from the incoming PCM train. This reclaimed 1.544-MHz clock signal is used to determine the operating rate of the digit generator and thus, to ensure that the receiving timing circuits operate at the same rate as the distant-end transmitting timing circuits. The framing detector is used to compare the timing train generated by the receiving digit generator against the incoming PCM train. If the receiver timing is not synchronized with the incoming PCM train, the framing detector initiates action to bring the digit generator into correct synchronization. When framing is correct, the digit generator supplies timing for the channel counter, the receiving converter, and the decoder at the 1.544-MHz rate. The correctly synchronized channel counter supplies timing for both the channel gates and the signaling receiver.

2.08 In addition to the standard internal timing supplied in the D1D channel bank, two other timing options are available. Both require the use of specialized interface units and additional bay wiring. The loop timing feature, for use with No. 4 ESS and the Digital Data System, permits the 6.176-MHz crystal oscillator to be synchronized with the recovered 1.544-MHz clock of the receiver. To implement this feature, the standard D1D interface (INT-4019CN) must be replaced with the loop timing interface (INT LOOP TMG-4019 CW), and the appropriate bay wiring in SD-97060-01 must be provided. The external timing feature, for use in the Digital Data System, allows synchronization to an 8-kHz timing signal derived from the external 64-kHz/8-kHz composite office clock (Fig. 6). Here the external timing interface (INT EXT TMG-4019 CU) replaces the standard D1D interface and the appropriate bay wiring in SD-97060-01 must be provided.

B. Transmitting Section

2.09 The production of the bipolar PCM signal in the transmitting section can be seen from the block diagram (Fig. 7). The 2-wire channel unit, which contains a hybrid, is shown in the block diagram as the interface between a supposed 2-wire trunk circuit and the 4-wire circuits inside the channel bank. A 4-wire channel unit used for a 4-wire trunk does not have a hybrid. The channel units have scanning gates which are operated sequentially at the rate of 8000 times per second. These gates send sampled information for signaling to the transmitting converter and common signaling circuit. The 24 channel gates, which are preceded by 3200-Hz cutoff filters (channel gates and filters), are operated sequentially at the same time the associated scanning gates are sampled to extract a stream of 5.2-microsecond amplitude samples of the message signals at the 24 channel units. This operation is called pulse amplitude modulation (PAM) because the amplitude of each pulse depends on the instantaneous amplitude of the voice-frequency input. The 24 channels are divided into two groups: channels 1 through 12 comprise group 1 and channels 13 through 24 comprise group 2. The channel sampling sequence is 1, 13, 2, 14, 3, 15, ... 11, 23, 12, 24 to provide 12-channel separation between adjacent samples and a maximum protection against interchannel crosstalk. The high-speed encoder produces a digital code comprised of the presence or absence of constant amplitude pulses called bits. This operation is called PCM. The encoder operates nonlinearly to encode low PAM pulses at a higher resolution than higher PAM pulses. This accomplishes the signal compression necessary for end-to-end compandoring. Because of this compression technique, the encoder produces a unipolar PCM output from the 256 possible code combinations with a higher signal to noise ratio. The transmitting converter and common signaling unit produces the PCM framing code for synchronization and inserts PCM signaling bits into the outgoing signal. This unit also converts the unipolar PCM signal to a bipolar signal for transmission over the digital line.

C. Receiving Section

2.10 The receiving converter and common signaling unit converts the incoming bipolar signal to a unipolar signal, extracts the information for receiving timing, and produces signaling trigger pulses from the incoming signaling bits. The nonlinear decoder produces PAM pulses from the PCM code groups representing the message signal. These PAM pulses have the same amplitude relationship as those at the transmitter since the nonlinear action of the decoder is matched to that of the encoder to accomplish end-to-end compandoring. The 24 channel gates, which are operated in sequence by the timing circuits, separate the PAM pulses for each channel. A channel filter associated with each of the 24 channel gates reconstructs the speech signal and eliminates frequencies above 3200 Hz to avoid crossover distortion. The channel units provide the interconnection between the channel bank and the trunk circuits and contain a signaling receiver to activate trunk processing equipment from the signaling trigger pulses.

3. PLUG-IN UNITS

A. Channel Units

3.01 The channel units in the D1D channel bank Fig. 4 and 7) serve as an interface between the central office trunk circuits and the multiplexing and demultiplexing circuits in the channel bank. Each channel unit consists of a transmitting section and a receiving section. The transmitting section accepts outgoing voice and signaling information from the associated trunk and applies the voice information to the multiplexing circuits and the signaling information to the transmitting common signaling circuits. The receiving section accepts incoming voice information from the demultiplexing circuits and signaling information from the receiving common signaling circuits and applies both types of information to the associated trunk.

3.02 The following channel units are used in the D1D channel banks. Physical and functional description of these channel units are contained in Section 365-100-110.

(a) 2-Wire Dial Pulse, Originating End (DP ORIG)

(b) 3-Wire Dial Pulse, Originating End, Sleeve Ground (SDP ORIG)

(c) 2-Wire Dial Pulse, Terminating End (DP TERM)

(d) 2-Wire E & M (2W-EM)

(e) 4-Wire E & M (E & M)

(f) 2-Wire Foreign Exchange, Office End (FX OFF)

(g) 2-Wire Foreign Exchange, Subscriber End (FX SUB)

(h) 2-Wire Revertive Pulse, Originating End (RP ORIG)

Note: Use only J98711G-3, L3 or J98711G-3 L2, L4 (RP ORIG) units in D1D channel banks.

(i) 2-Wire Revertive Pulse, Terminating End (RP TERM)

Note: Use only J98711H-2, L3 or J98711H-2, L2, L4 (RP TERM) units in D1D channel banks.

(j) 4-Wire Foreign Exchange, Subscriber End (FX-SUB)

(k) 2-Wire Duplex (2W DX)

(l) 4-Wire Duplex (4W DX)

(m) 4-Wire Tandem (4W TDM)

(n) 2-Wire Transmission Only (2-W TO)

(o) 4-Wire Transmission Only (4-W TO)

(p) 4-Wire Pulse Link Repeater (PLR)

(q) 4-Wire Equalized Transmission Only (4-W ETO)

B. Transmitting Channel Gates and Filters (XMTG GTS)

3.03 Four plug-in boards containing 24 channel gates and 24 corresponding channel filters are used in the transmitting section of the D1D channel bank for extracting a continuous series of PAM samples from the 24 voice-frequency input signals and for sequentially combining these samples into two continuous streams of PAM pulses corresponding to two 12-channel groups.

3.04 The 24 voice-frequency signals from the 24 channel units are applied to the 24 transmitting channel filters. These are notched low-pass filters having a resonant rejection frequency at 150 Hz and a sharp cutoff above 3000 Hz in order to remove any information outside the frequency range of 200 to 3200 Hz or 180 to 3400 Hz with improved filters. This arrangement removes most low-frequency noise and commercial power ripple. In addition, it prevents any voice-frequency components of greater than half the sampling rate from reaching the sampling circuit and thus, prevents a form of distortion (foldover distortion) in the reconstructed voice-frequency signal at the distant-end receiver.

3.05 Channel pulses from the channel counter sequentially operate each of the 24 transmitting channel gates for 5.2 microseconds during each 125-microsecond frame to allow a portion of the corresponding voice-frequency signal to pass through. During the time that one gate is conducting, the other 23 gates are nonconducting to prevent sampling from more than one channel during any one sampling period.

C. Transmitting Clamp (XMTG CLAMP)

3.06 The transmitting clamp consists of a clamp gate circuit driven by a blocking oscillator. Two transmitting clamps are provided in the D1D channel bank; one for group 1 and one for group 2. The clamp gate discharges an associated group PAM pulse storage capacitor in the encoder network after approximately six microseconds to prevent interference with the next PAM sample coming from the other group. The blocking oscillator under the control of clock drive pulses from the transmit clock produces a spike voltage which operates the clamp gate circuit.

D. Nonlinear Encoder (ENC)

3.07 The nonlinear encoder converts the amplitudes of PAM pulses into a PCM signal. The PCM signal for each pulse consists of an 8-bit code with pulses either present (1) or absent (0) in the eight time slots. The encoder has a nonlinear characteristic to provide the signal compression necessary for end-to-end compandoring.

3.08 The encoder is composed of four networks: a regulated power supply, a code translator, a weighting network, and the encoding network. The code translator produces eight timing pulses for the weighting network from ten pulses supplied by the digit generator. The weighting network develops precisely controlled currents that are referenced to the local voltage regulator. The currents are switched and attenuated in a resistive ladder network to produce a nonuniform ($\mu = 255$) coding characteristic output voltage. This voltage is compared to the PAM pulse in a summing amplifier. The difference between these voltages determines whether or not a PCM bit is produced. This process continues until the PAM pulse has been encoded into the presence or absence of eight

PCM bits corresponding in time with the eight timing pulses from the code translator. The weighting network operates nonlinearly so that a low PAM pulse is encoded with greater resolution than a higher pulse (compression). Thus, the 8-digit PCM code, representing a PAM pulse, is produced by eight successive comparisons between the PAM pulse and nonlinear increments of reference voltage.

3.09 An inhibit circuit and a zero code suppression circuit are included in the encoder board. The inhibit logic circuit prevents the use of certain digits during the encoding. These digits occur at the appropriate time because of the action of the transmitting converter and common signaling circuit. The zero code suppression circuit prevents the loss of line synchronization by inserting digit D7 when an all-zero PCM code occurs at the encoder network.

E. Transmitting Converter and Common Signaling Unit (XMTG CONV SIG)

3.10 The transmitting converter and common signaling unit consists of two circuits on one circuit board. The common signaling circuit is used to convert the signaling information (presence or absence of signaling pulses) received from the transmitting section of the 24 channel units into the presence or absence of PCM bits in time slot D8, every sixth frame. The common signaling circuit also produces the PCM framing code with the presence or absence of a bit in alternate D9 time slots of each frame for synchronizing the distant-end receiver. The other use of alternate D9 time slots is for signaling synchronization which is accomplished by sending a repetitive 111000 subframing pattern. The transmitting converter multiplexes the message, signaling, framing, and signaling synchronization PCM bits into a unipolar train and converts this train into a bipolar PCM train. This conversion to bipolar form reduces the principal energy component on the line from 1.544 MHz to 0.772 MHz, which in turn reduces bandwidth requirements of the digital line, reduces crosstalk, and permits the use of transformer coupling in the digital line repeaters.

3.11 The common signaling circuit processes the regular (2-state) D1D signaling information (supervision) and the additional information (2-state) for 2-way dialing on foreign exchange channels. Since additional information is required for foreign exchange channels, it is necessary to alternate between regular and additional signaling every sixth frame. A 111000 pattern of PCM framing bits, produced by the common signaling circuit from the D9 pulses supplied by the digit generator board, directs this operation. Thus, every sixth frame, the common signaling circuits convert the regular or additional signaling pulses from the channel units into the presence or absence of PCM bits in time slots D8 of 24 channels. For other than foreign exchange channels, only regular signaling is transmitted every sixth frame. Whenever PCM bits are produced at time slot D8 in the common signaling circuit, an inhibit pulse (DINH in Fig. 7) is sent to the encoder to prevent the use of digit D8 there.

3.12 The transmitting converter multiplexes the PCM voice code from the encoder with the PCM signaling (D8) and framing (D9) bits from the common signaling circuit to produce a unipolar bit stream. Figure 8 shows the framing pattern that synchronizes the terminals and the subframing pattern which identifies which frame contains signaling and what signaling information (A1 or A) is being transmitted. Both of these patterns of framing bits are multiplexed into the bit stream. The unipolar stream is then applied to two accurately timed blocking oscillators, which operate alternately producing a bipolar output.

F. Receiving Converter and Common Signaling Unit (RCVG CONV SIG)

3.13 The RCVG CONV SIG unit consists of two circuits on one board. The receiving converter portion converts the incoming bipolar PCM train into a unipolar PCM train sent to the decoder and extracts the base frequency (1.544 MHz) of the received signal for timing in the receiver. The common signaling circuit extracts the signaling bits from the unipolar PCM train and converts these bits into 2.6-microsecond signaling trigger pulses for the channel units.

3.14 A full-wave rectifier in the receiving converter circuit produces a unipolar bit stream applied to a tuned amplifier which recovers the base frequency (1.544-MHz sine wave) for receiver timing. This recovered frequency drives the clock pulse generator circuits which supply the receiving digit generator. The unipolar bit stream from the full-wave rectifier is applied to the nonlinear decoder and the framing detector.

3.15 The logic circuitry in the common signaling circuit extracts the signaling bits from the unipolar PCM train and applies them to two blocking oscillators which produce signaling trigger pulses for regular and foreign exchange signaling. The subframing pattern (paragraphs 3.10 and 3.11) in the received signal synchronizes the signaling in the receiver by alternately activating (every sixth frame) the blocking oscillator for the regular signaling and the blocking oscillator for foreign exchange signaling.

G. Nonlinear Decoder (DEC)

3.16 The nonlinear decoder is used to convert the received PCM code groups into PAM pulses which are reconstructed into voice-frequency signals for 24 channels. The decoder has a nonlinear characteristic which matches that of the encoder at the transmitting terminal to achieve end-to-end compandoring.

3.17 The decoder drive, code translator, and weighting network in the decoder board operate together to convert the PCM code groups into PAM pulses. The decoder drive has logic circuitry to accumulate an 8-bit PCM code group from the receiving converter for application to the code translator. The code translator produces eight digital pulses from the incoming 8-bit code group which concurrently operate the eight switch circuits in the weighting network. These switch circuits simultaneously apply portions of current from the decoder reference supply to a common output resistor to produce an amplitude pulse (PAM pulse). The weighting network operates nonlinearly so that PCM code groups for weak PAM pulses are decoded with more resolution than PCM code groups for strong PAM pulses. This expansion technique provides for end-to-end compandoring.

H. Receiver Common Amplifier (RCVR COM AMP)

3.18 The receiver common amplifier is used to develop sufficient PAM pulse power for driving the channel gate circuit. A negative feedback circuit is used in this amplifier for improved frequency response, phase shift, and stability.

I. Receiving Channel Gates and Filters (RCVG GTS)

3.19 The receiving channel gate and filter circuit consists of 24 gates and filters that are used to extract sequentially the 24 channels of voice-frequency information from the two 12-channel PAM trains received from the common decoder circuit. This extracted information is then used to reconstruct 24 voice-frequency signals for application to the 24 associated channel units.

3.20 The receiving channel gates are similar to the transmitting gates except that a transistor gate driver stage is required because of the low impedance of the low-pass channel filter into which the gate operates. When the channel pulse which activated the gate driver stage for that channel ends, the transistor reverse biases the gate diodes to prevent any further PAM pulses from passing through until the next channel pulse occurs for this channel; that is, until after the other 23 channel gates have been operated.

3.21 The PAM samples from the 24 channel gates are applied to the corresponding channel filters where all pulse components above the upper cut-off frequency are removed and all lower-frequency components are retained to form an accurate duplicate of the bank-limited voice-frequency signal applied to the sampling circuits at the distant-end transmitter.

J. Transmit Clock (XMT CLK)

3.22 The transmit clock common unit consists of two independent circuits mounted on a single board; a clock generator and a group generator (Fig. 9).

3.23 The clock generator supplies the basic timing for the transmitting section of the local D1D channel bank and thus, for the outgoing digital line and the receiving section of the distant-end D1D channel bank. A crystal oscillator in the voltage-controlled oscillator (VCO) network generates the sine wave (6.176 MHz) from which the basic 1.544 Mb/s is obtained by a frequency divider. The phase comparator network produces a small dc control voltage proportional to the amount that the loop timing input (if provided) differs in frequency from 6.176 MHz, the natural rate of the crystal oscillator in the transmit clock. This loop timing feature allows the crystal oscillator to be driven at the frequency applied to the phase comparator for precise timing of D1D channel banks. The phase 1 output of the phase shift network, which is applied to the transmitting converter, leads the phase 2 output, which is applied to the encoder and digit generator, by approximately

25° for correct timing throughout the D1D channel bank.

3.24 The group generator is triggered by timing pulses from the transmitting digit generator. Each timing pulse causes the group generator to change state and thus to alternately generate group 1 and group 2 enable pulses concurrently with group 2 and group 1 inhibit pulses. The resultant pulse trains are composed of symmetrical square-wave pulses having a repetition rate of 1.544 Mb/s. This circuit simultaneously supplies an enable pulse to one channel group with an inhibit pulse to the other channel group in order to permit group 1 (or group 2) circuits to sample and to multiplex one voice channel while group 2 (or group 1) circuits are encoding the PAM sample from the preceding voice channel.

K. Digit Generator (DIG GEN)

3.25 The digit generator produces separate timing pulses (digits) approximately 0.3 microsecond wide for each of the 8-pulse positions (D1 through D8) used for encoding and for one pulse position (D9) in the framing code. Identical digit generators are used in both transmitting and receiving sections of the bank.

3.26 The digit generator consists of nine blocking oscillators connected in tandem so that the operation of one will prepare the following one for operation. Negative feedback to the first blocking oscillator prevents its operation while another blocking oscillator is operated. Timing pulses from the transmitting common signaling circuit or the framing detector (receiving section) are necessary to trigger the operation of the ninth blocking oscillator. Because of the tandem connection, the first eight blocking oscillators are operated in sequence to produce eight identical digits and, when the enable pulses for the ninth oscillator occur, the ninth digit is generated. A square wave from the master clock or receiving converter (1.544 MHz) times the operation of the nine blocking oscillators.

L. Transmitting Channel Counter (XMTG CTR)

3.27 The four transmitting channel counter units in the D1D channel bank generate a series of 24 pulses which direct the sampling sequence of the 24 channels. These pulses trigger the transmitting channel gates and the scanning gates in the channel units. One pair of channel counter units is used for group 1 and the other pair is used for group 2.

3.28 The transmitting channel counter consists of 27 blocking oscillators, 24 of which are channel pulse generators, 2 are drivers, and 1 is an inhibitor. The two drivers receive clock drive pulses from the group generator of the transmit clock to alternately switch between the first group of 12-channel pulse generators and the second group of 12. The channel pulse generators in each group are connected in tandem so that the operation of one will prepare the next one for operation. The inhibitor restricts the operation of the channel pulse generator for channel 1 to the first operation in the first group. This first operation starts the alternating progression down the groups of channel pulse generators, producing a series of 24 pulses in the sequence 1, 13, 2, 14, ... 11, 23, 12, 24.

M. Receiving Channel Counter (RCVG CTR)

3.29 The four receiving channel counters are very similar to the transmitting channel counter (paragraphs 3.27 and 3.28) except that the timing pulses for switching between group 1 and group 2 are developed in the receiving counter instead of by the group generator. The two driver blocking oscillators in these common units are initiated by a timing pulse from the receiving digit generator and produce self-inhibiting pulses after each operation to allow alternation between both groups of 12 channel counters. This circuit generates a series of 24 channel pulses in the sequence 1, 13, 2, 14, ... 11, 23, 14, 24, which are synchronized to the 24 channel pulses generated in the distant-end transmitting channel counter.

N. Framing Detector (FR DET)

3.30 The framing detector is used to initiate receiving digit generator action for inserting framing digits in the pulse train that is used to synchronize the receiving timing circuits. In the event that the digit generator becomes desynchronized with the incoming PCM pulse train or the PCM pulse train contains excessive framing code errors, the framing detector initiates action to resynchronize the digit generator. A visual indicator, which has a reset button associated with it, is located on the face of the unit to indicate a single framing error.

3.31 The framing detector is composed of three circuits: the reframer, the framer, and the alarm detector circuit. The phase comparator in the reframer detects the desynchronized condition in the receiver and activates the framer to correct the condition. The reference flip-flop in the reframer changes state (0 or 1) in the middle of a frame period for a comparison at the phase comparator with the next framing bit in the incoming PCM train. When the presence or absence of a pulse occurs simultaneously, the output of the phase comparator is zero; but, with a mismatch, the output is a pulse in position D9. If two more pulses occur during the next ten frames because of errors in the framing pattern (Fig. 8), the framer will operate. The framer causes the receiving digit generator to insert a framing pulse for resynchronization. The alarm detector circuit produces a dc voltage which is abnormally low during incorrect framing. At a certain low level the receiving alarm unit will indicate trouble.

4. ALARM EQUIPMENT

A. Receiving Alarm

4.01 The receiving alarm common unit in the D1D channel bank (Fig. 10) is used to detect a power supply failure, a receiver failure, improper framing of the receiver, and alarm indications from the distant end. Trouble can be localized by observing the red (AR) and yellow (AY) alarm lamps on the alarm control unit. In addition, this unit has an alarm cutoff (ACO) button, a loop terminal (LT) key, and a loop control (LC) key. The ACO button silences the office alarms and the LT key allows the bank to be looped during an alarm condition for trouble-shooting or for out-of-service maintenance. The LC key manually controls the transmission of a yellow (AY) alarm over the digital line. This feature is used to locate a faulty span line section between a terminal with a red (AR) alarm and the intermediate office(s). The line is looped by patching at an intermediate office, and the terminal alarm indication should change from red to yellow if the line section under test is good (Table A).

4.02 The AR lamp indicates an alarm condition in the receiving direction and the AY lamp indicates that the distant terminal is not receiving. The AR alarm is caused by a faulty receiver, no received signal, or loss of receiver synchronization. The AR alarm causes control signals to be sent to the encoder and the transmitting common signaling unit, activates the carrier group alarm (CGA) and the office alarms, and inhibits an AY alarm if the terminal had not previously received an AY alarm. These control signals cause the deletion of PCM digit D2 from the transmitted signal to force an AY alarm at the distant terminal. The AY alarm activates the CGA and the office alarms.

B. Carrier Group Alarm (CGA) Circuit

4.03 The CGA circuit (refer to Section 365-108-102) is used with the D1D channel bank to:

(a) Recognize the presence of an alarm condition in the channel bank caused by loss of synchronization or dc power in the system,

(b) Isolate the associated trunk circuits and stop service charges,

(c) Make all trunks busy,

(d) Introduce a brief time delay during which subscribers may disconnect,

(e) Automatically disconnect any subscriber remaining on a trunk after the disconnect period,

(f) Remove all trunks from service,

(g) Automatically restore all trunks to service after the trouble condition has been corrected.

5. EQUIPMENT DESCRIPTION

A. Equipment Bays

5.01 The J98711A, B, and C standard bays are used to mount D1D channel banks. These shop-wired bays are 23 inches wide and have die-cast aluminum shelves for plug-in units. The J98711A bay is 11-1/2 feet high and mounts three channel banks. The J98711B bay is 9 feet high and mounts two channel banks. The J98711C double bay mounts three channel banks and is intended for offices such as ESS where the bay height is limited to 7 feet.

5.02 As discussed in paragraph 2.08, a D1D channel bank is specialized by its mode of timing which can be identified by the type of interface unit in the channel bank. When other than the standard internal timing is required for a channel bank, additional bay wiring is done for that channel bank and the appropriate interface unit is used. The additional bay wiring (rear of bay) for the loop timing option and the external timing option is shown in Fig. 11 and 12, respectively. The interface unit can be changed to revert back to internal timing even with the additional wiring in place. Providing the additional wiring for both the loop timing and external timing options allows selection of any of the three options by changing interface units.

5.03 As discussed in paragraph 1.04, a D1D channel bank can be formed in an unequipped bay or a D1B channel bank can be converted to a D1D channel bank. One essential requirement is that the bay be equipped with the K wiring option per Fig. 13. The K wiring option may be installed at the factory or it may be provided in the field by adding four wires as shown in Fig. 13.

5.04 D1 channel bank labels are provided to identify D1A, D1B, and D1D channel banks because the plug-in boards are not factory stenciled. Labels are also provided to identify channel banks which are equipped with hardened boards. The color codes and location of these labels is shown in Fig. 14.

5.05 The channel banks are connected to the digital line at the office repeater bay or DSX-1 cross-connected bay. All external connections (such as to the digital line, DSX-1, the office battery, and the 1000-Hz milliwatt generator) are made at the terminating panel. Connections to the external office clock for timing of a channel bank are also made at this panel. The 20-Hz ringing voltage and equalizer panel provides for the mounting of an equalizer or pad which builds out the cabling loss to 6 dB between the channel bank and the repeater bay or DSX-1 and brings 20-Hz ringing voltage into the bay for subscriber-end foreign exchange channels.

5.06 The common plug-in units for the D1D channel bank are die-cast metal frames supporting printed wiring boards. Connections to other circuits are made through a 20-pin plug on the rear of the metal frame. The common plug-in units are either 1 or 2 inches wide, 8-1/2 inches high, and 9 inches deep. The channel units are 11/16 inch wide, 5-7/8 inches high, and 10 inches deep.

B. Power Supplies

5.07 The J86498A power supply provides +24, -24, -42, and +48 volts to the bay. This power supply consists of a dc-to-dc converter; +24, -24, and +48 volt regulators; and an over/under voltage alarm circuit. The J86498A, +24/-24 volt regulators are hinged to the associated connecting panel and wired to the dc-to-dc converter with flexible cords so that the regulators can be swung out for access to all apparatus. When the D1D channel bank operates with an ESS power plant, office battery is -52 volts. In this case, a caution label for the J86498A power supply is needed to warn of the adjustment to the ±24 volt regulators. The caution label (Fig. 15) must be attached to the regulators when they are adjusted for 25-volt output. The other power supplies do not need adjustment. The newer J87331A power supply is used for the standard bays. This power supply has built-in regulators and provides +24, -24, -42, and +48 volts to the bay through a connecting panel which is also used with the J86498A power supply.

C. Fuse, Alarm, and Filter Panel

5.08 The fuse, alarm, and filter panel provides filtering, fusing, and distribution of primary power for the D1D channel bank bay. It also provides blown-fuse indications for the power distribution circuits. This circuit distributes -48 volts to the channel banks and to the carrier group alarm circuit (CGA). Filtering is provided to minimize noise transfer, in both directions, between the -48 volt office battery and the bay. Lamps designated FA and ABS in the fuse, alarm, and filter panel are provided for local indication of blown fuses; relay contacts provide control signals to the CGA circuit and to the office audible and visual alarm circuits during fuse or transmission alarm conditions. The fuse, alarm, and filter panel connections are illustrated in Fig. 16.

6. TEST EQUIPMENT

6.01 Lineup and testing procedures for the D1D channel bank require a 1-kHz code generator testboard and a 1-kHz rejection filter testboard, which are described in Sections 365-116-101 and 365-103-104, respectively. The 1-kHz code generator is placed in position E of the channel bank under test. The 1-kHz rejection filter testboard is placed in position S or Y of the channel bank under test.

A matching network, which is permanently mounted at the left side of the bay, is used to make test connections from the testboards to the external test equipment. The 4019CS 1-kHz code generator serves three functions: to generate digital signals which are equivalent to 1-kHz test tones for the 24 channels; or to generate a coded zero signal with a random polarity bit; or to generate a coded zero signal. The first function mentioned is used in aligning the receiver, the second is used in measuring crossover distortion in the decoder, and the third is used in measuring idle circuit noise in the receiver.

7. REFERENCES

7.01 The following is a list of the plug-in units and drawings associated with the D1D channel bank.

DESCRIPTION	CODE	DRAWING
Through Connecting Circuit	4019AA (Note 1)	SD-97060-01
Transmitting Channel Gates and Filter	4019BD (Note 2)	SD-97062-02
Digit Pulse Generator	4019BH	SD-97067-02
Transmit (Master) Clock	4019CL	SD-3C142-01
Transmitting Converter and Common Signaling Unit	4019CM	SD-3C143-01
D1D Interface (INT)	4019CN	SD-3C145-01
Receiving Framing Detector	4019CP	SD-3C147-01
Receiving Converter and Common Signaling Unit	4019CR	SD-3C148-01
1kHz Code Generator	4019CS	SD-3C151-01
Through Connecting Circuit	4019CT (Note 1)	SD-152-01
External Timing Interface (INT EXT TMG)	4019CU	SD-3C153-01
Loop Timing Interface (INT LOOP TMG)	4019CW	SD-3C154-01
Transmitting Clamp	4020S	SD-3C141-01
Encoder	4020T	SD-3C144-01
Receiver Common Amplifier	4020U	SD-1C146-01
Decoder	4020W	SD-3C149-01
Receiving Alarm (RCVG ALM)	J98711Y-1 or J98711Y-2	SD-3C150-01

Note 1: In the D1D channel banks, the 4019CT through connector circuit is used in position J and the 4019AA is used in position E and L.

Note 2: A 4019D channel gates and filters unit may be used in the D1D channel bank. The 40198D has a greater bandwidth than the 4019D.

TABLE A

TERMINAL ALARM INTERPRETATION

LAMP INDICATIONS	CAUSE	LAMP INDICATIONS IF BANK IS LOOPED	PROBABLE TROUBLE
Red (AR)	Incoming alarm	Red remains	Local Receiver or Local Power Supply
		Red clears	Far End Transmitter or Incoming Line
Yellow (AY)	Far end not receiving	Yellow clears Red appears	Local Transmitter
		Yellow clears	Outgoing Line or Far End Receiver
Red and Yellow	Far end has red and has bank looped	Red remains	Local Transmitter
		Red and yellow clear	Outgoing Line or Far End Receiver
Looped line test: Red clears Yellow appears	Looped line returning AY alarm (LC key in horizontal position)	Bank not looped	Looped section of line not at fault
Looped Line Test: Red remains	Looped line does not return AY alarm (LC key in horizontal position)	Bank not looped	Looped section of faulty line

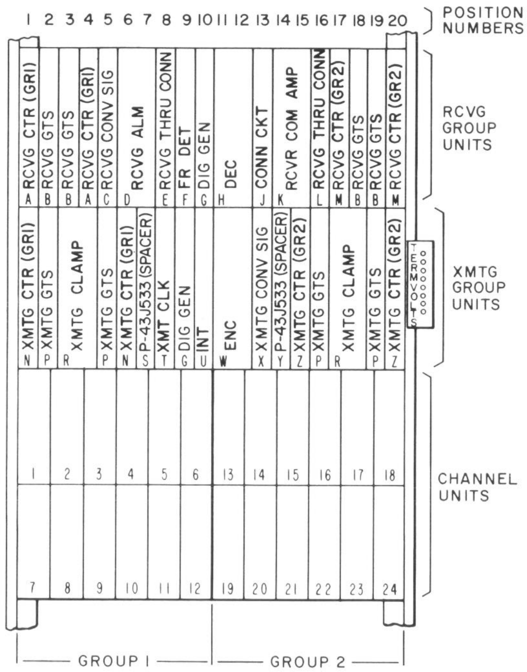


Fig. 1—D1D Channel Bank

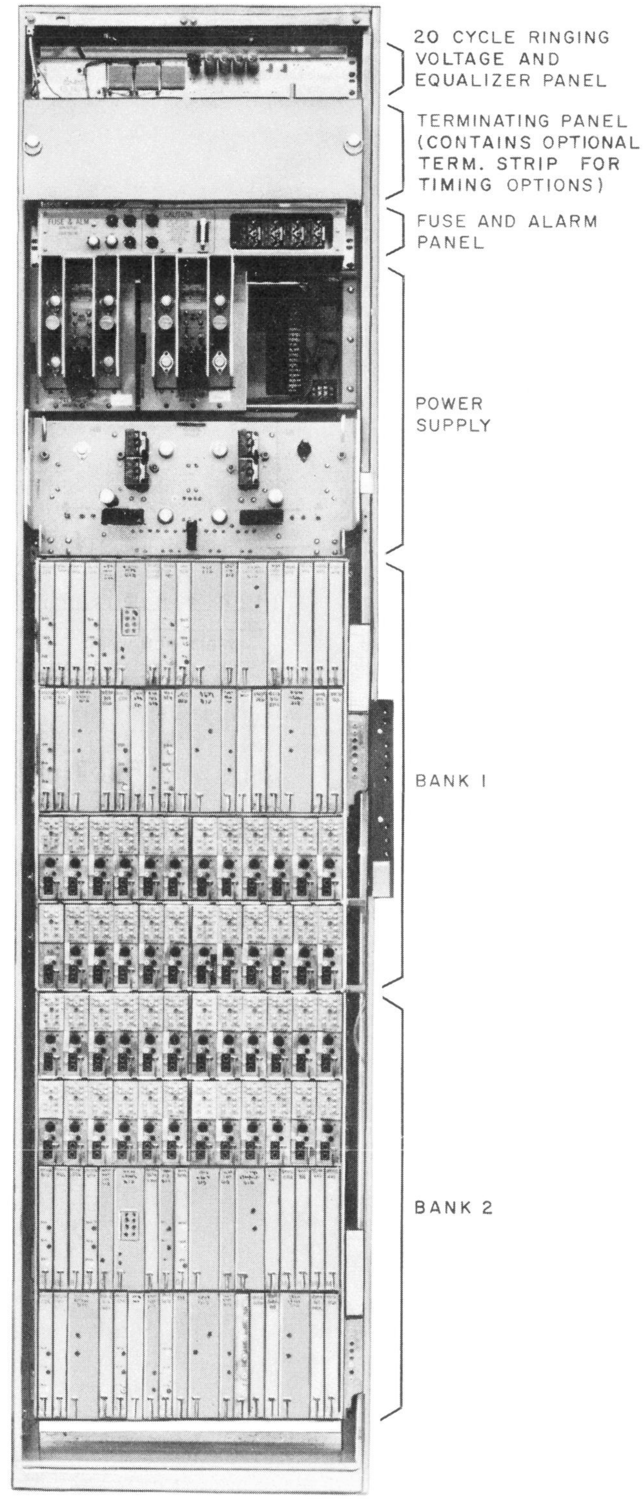


Fig. 2—D1D Channel Bank—9-Foot Bay

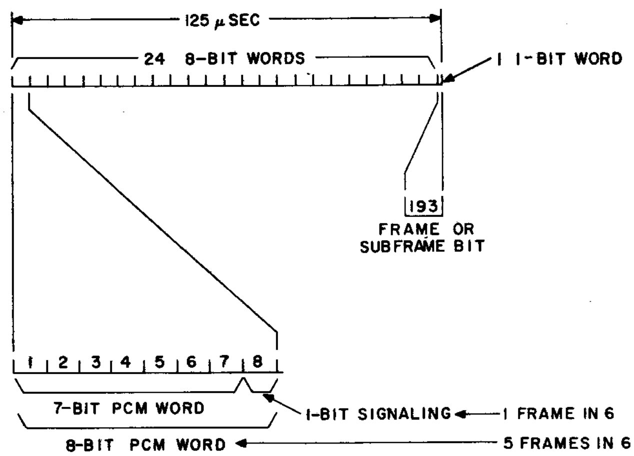


Fig. 3—D1D Frame Format

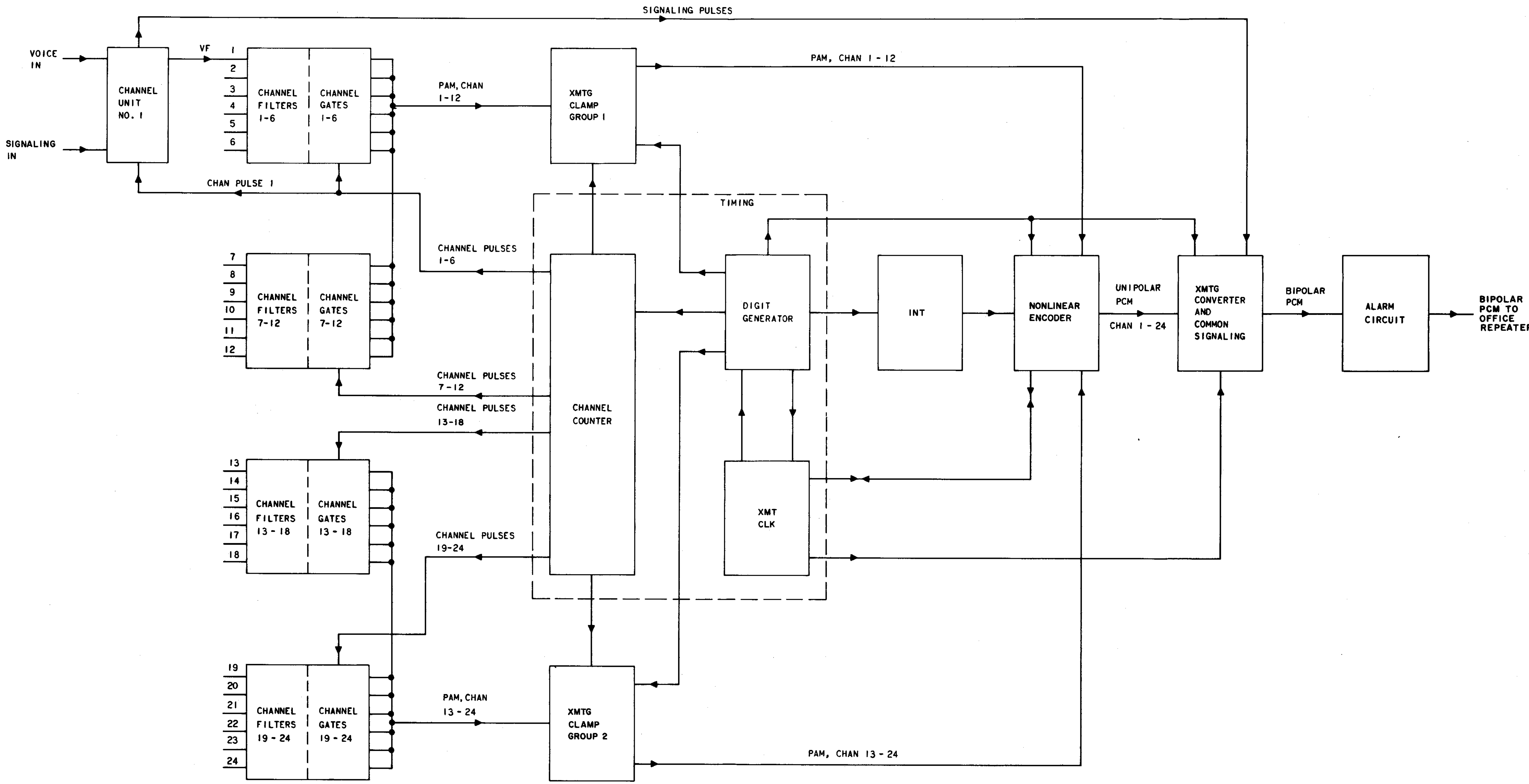


Fig. 4—Timing Circuits, Transmitting Section

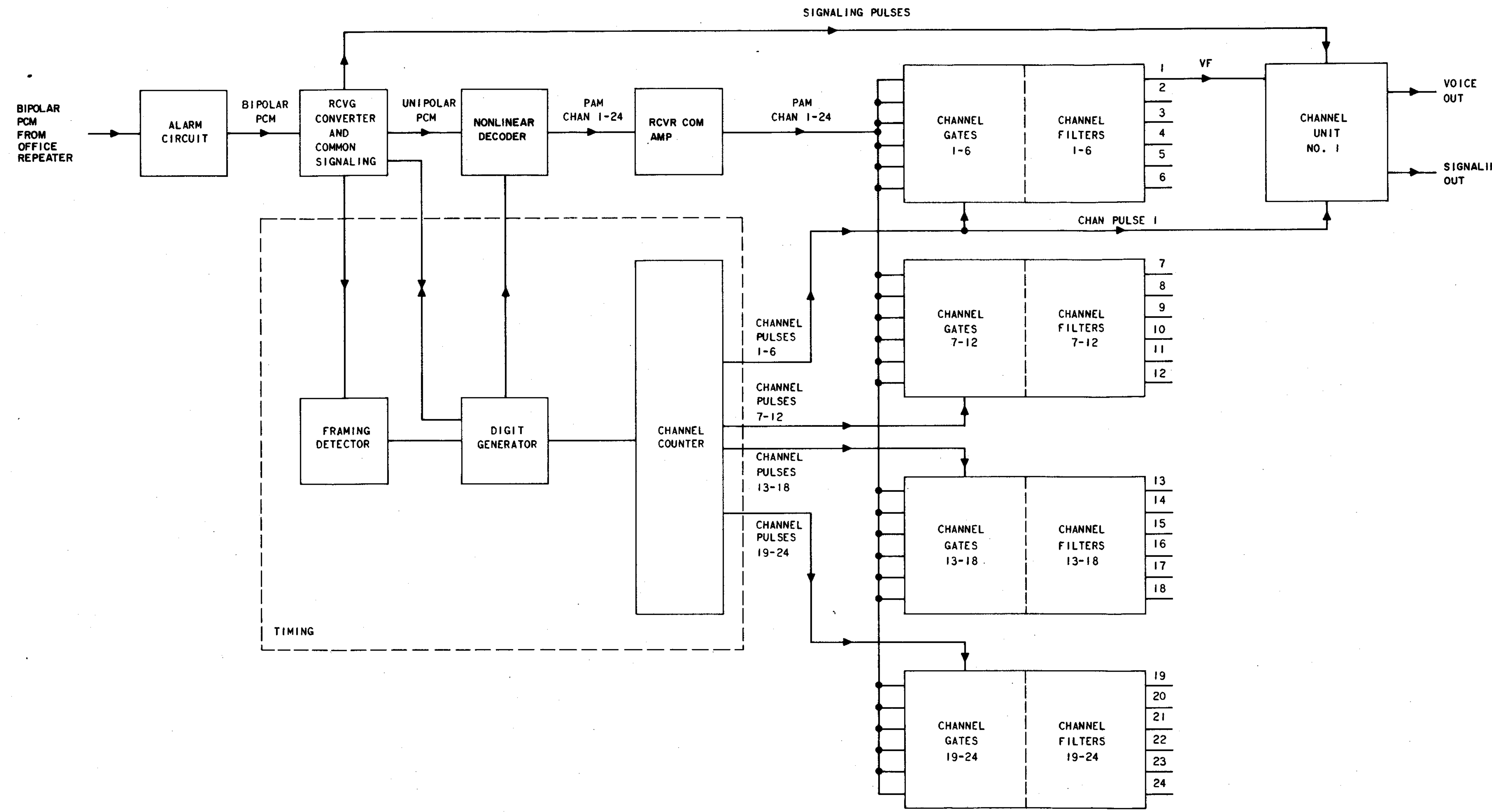


Fig. 5—Timing Circuits, Receiving Section

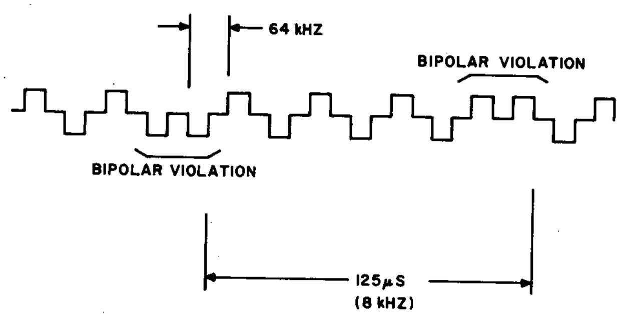


Fig. 6—64-kHz/8-kHz Composite Office Clock Signal

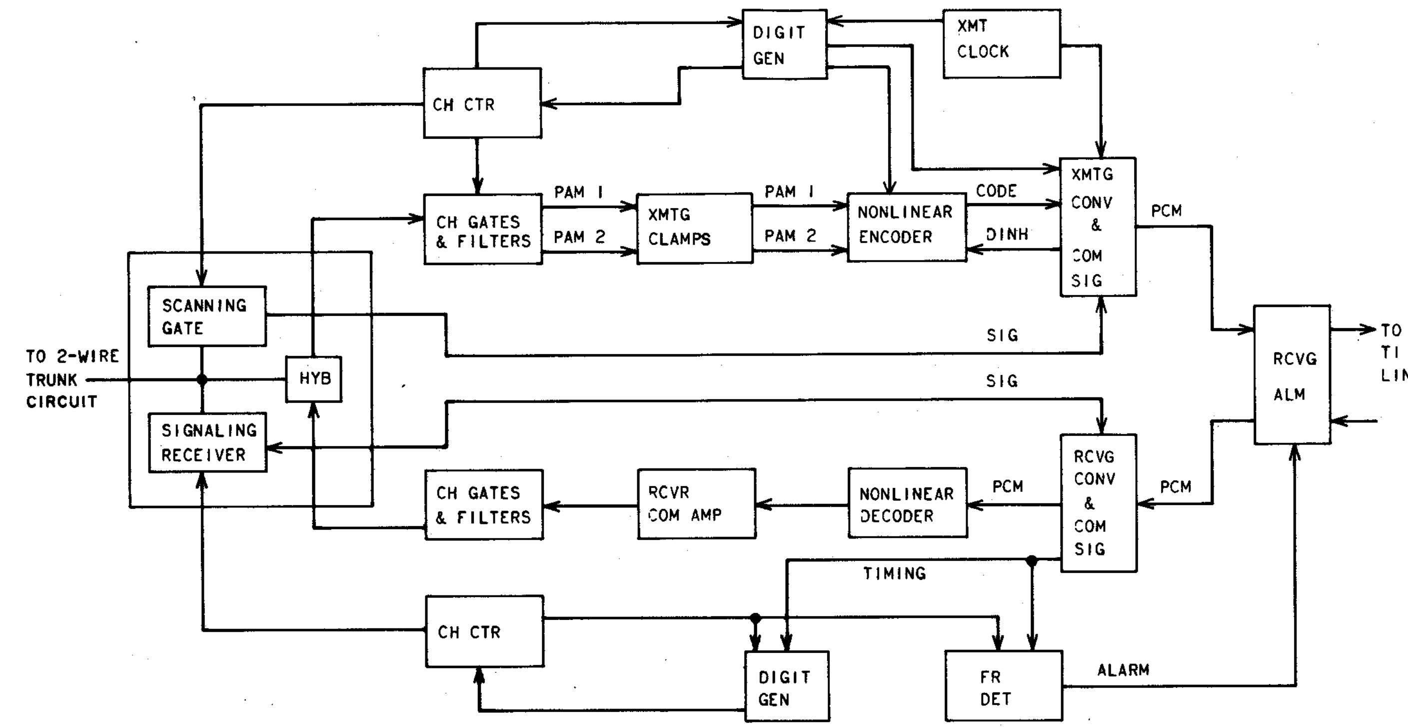


Fig. 7—D1D Channel Bank Block Diagram

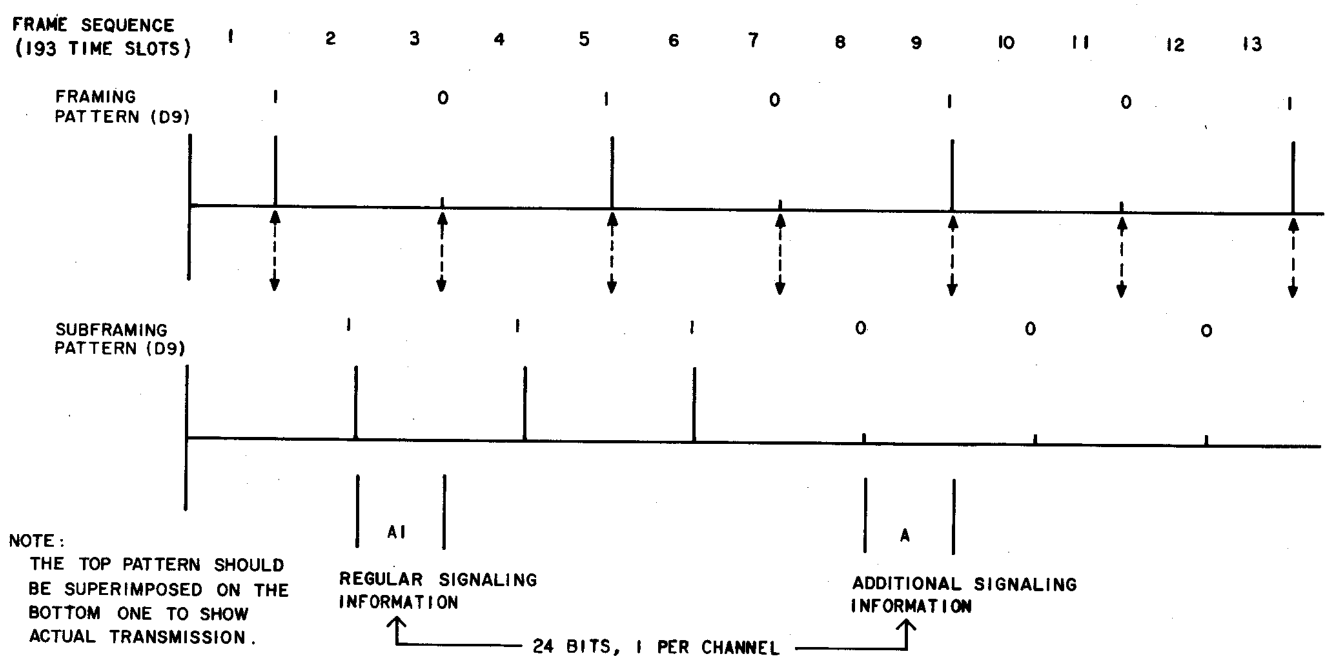


Fig. 8—D1D Channel Bank Signaling Format

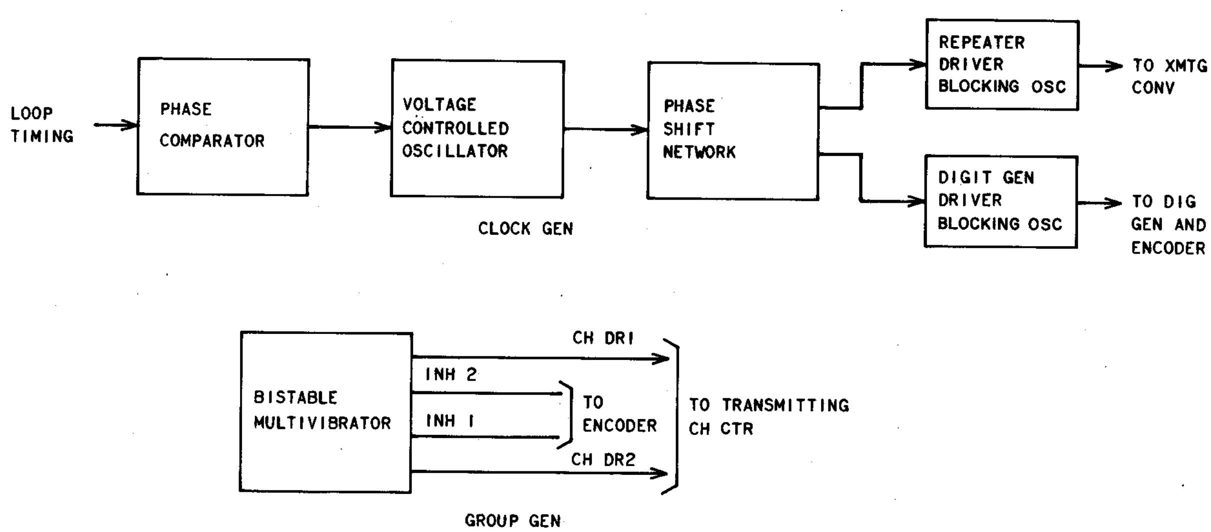


Fig. 9—Transmit Clock

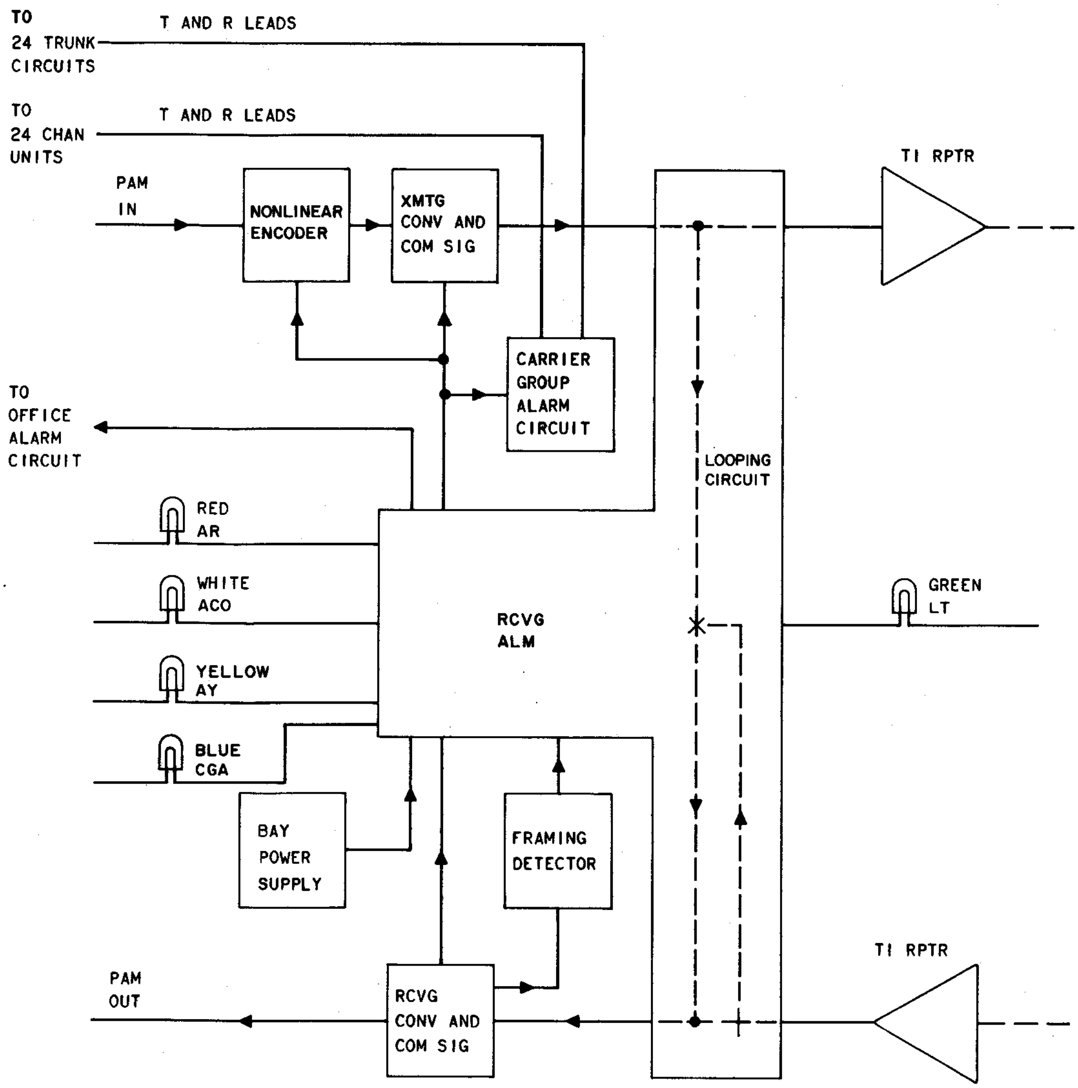


Fig. 10—Receiving Alarm

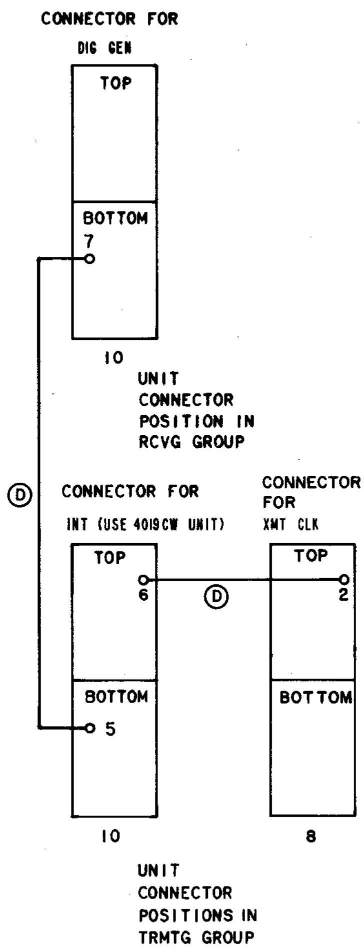
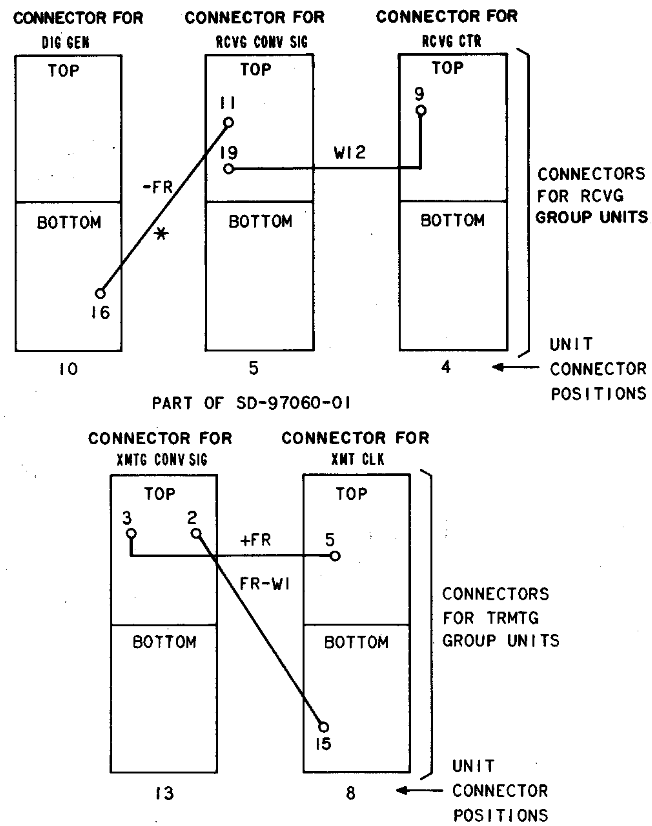


Fig. 11—Bay Wiring for Loop Timing Option



*IF K WIRING WAS INSTALLED AT THE FACTORY, THE WIRING WILL RUN FROM PIN 11 TOP OF CONNECTOR 5 TO PIN 15 BOTTOM OF CONNECTOR 8 THEN TO PIN 16 BOTTOM OF CONNECTOR 10.

Fig. 13—Bay Wiring for K Wiring Option

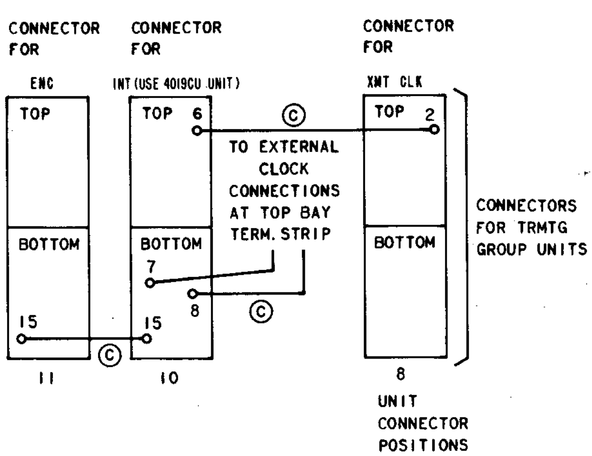


Fig. 12—Bay Wiring for External Timing Option

NOTES:

1. CHANNEL BANK LABELS SHOULD BE PROVIDED AS AN AID IN THE MAINTENANCE OF D1-TYPE CHANNEL BANKS AND LOCATED ON THE VOLTS TEST STRIP AS SHOWN.

2. THESE LABELS SHOULD BE ORDERED AS REQUIRED PER CHANNEL BANK AS FOLLOWS:

PART NUMBER	CHANNEL BANK	COLOR
842113599	D1A	GRAY
842113607	D1B	RED
842113615	D1D	BLUE
* 842432858	D1AH	GRAY
* 842432866	D1BH	RED

* D1AH AND D1BH CHANNEL BANK LABELS ARE USED WHERE D1A AND D1B CHANNEL BANKS ARE EQUIPPED WITH HARDENED COMPRESSORS.

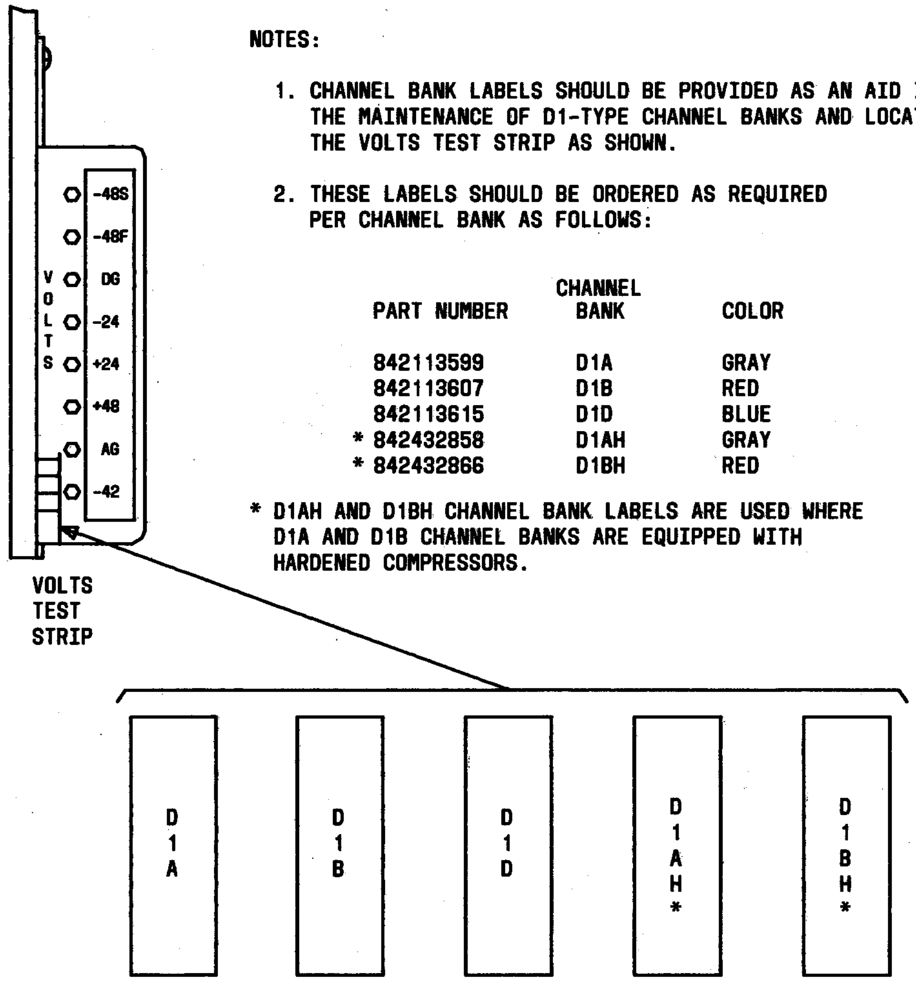


Fig. 14—Bank Labels and Location

J86498A

CAUTION

THIS BAY POWERED BY 52 VOLT SUPPLY

24 VOLT REGULATORS MUST BE ADJUSTED TO 25 VOLTS

ADJ ±24V REGS FOR .285 VOLTS AT TST JACKS

DIB REQUIRES 4019 BT SERIES 11 OR HIGHER -RCV CONV SIG

DID REQUIRES 4019 CR SERIES 10 OR HIGHER -RCV CONV SIG

B.S.P 365-101-500

NOTE:

±24 VOLT REGULATORS ARE ADJUSTED FOR .285 VOLTS WHEN USING A KS-14510 VOM. IF A KS-20599 DMM IS USED, THESE REGULATORS ARE ADJUSTED FOR .295 VOLTS.

Fig. 15—♦Caution Label For J86498A Power Supply♦

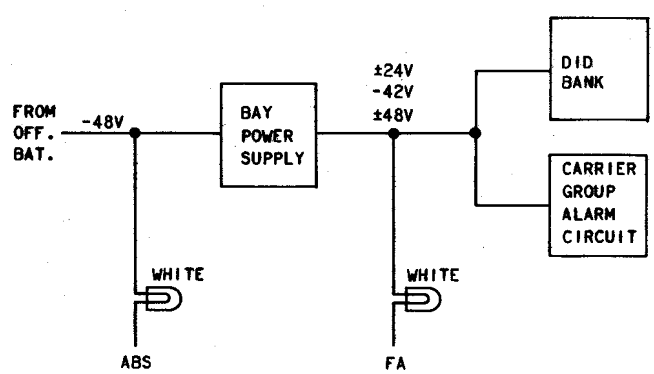


Fig. 16—Fuse, Alarm, and Filter Circuit—Alarm Connections