

365-340-403

**DACS IV-2000 Quick Reference Job Aids - Release 3.0 - 365-340-403**

## 1. Functional Block Diagram

See Figure 1.

## 2. Unit Numbering

Figures 2, 3, and 4 illustrates the physical association of bays, units (the shelf positions of interface modules), and interbay cables in a fully-equipped system with all DS1 interfaces, DS3 interfaces, and STS-1 interfaces, respectively. For example, using Figure 2, look at Unit 11, located in the third column of the second row. The first label in Unit 11 is *SWIO 7*. This represents the Switch Input/Output (SWIO) circuit pack in the Switch Module that is associated with Unit 11. The designation *N-Rate D* indicates half of an N-rate cable (labeled *D*) that connects this interface module to the Switch Module. The number *9* indicates the DS1 Interface-Protection Module (located in Unit 9) responsible for protection this interface module. Finally, the number *J-7* shows the control cable for this interface module in the bay lineup. Each unit shown in this sample configuration is labeled with the same information.

The unit numbers and control cable numbers shown in Figures 2, 3, and 4 are the same for any DACS IV-2000 system configuration. The examples pictured are based on a maximum configurations, but the same numbers are used for other configurations.

### 3. Commands and Messages

Command	Command	Command	Command
ABT-CMD	ED-T1	RLS-TSTPT-VT1	RTRV-NE
ACT-ECHO-LINK	ED-T3	RMV-EQPT	RTRV-PATH-STS1
ACT-USER	ED-VT1	RMV-LINK	RTRV-PATH-T1
ACT-LPBK-EC1	ENT-AUTOCMPN-T1	RST-EQPT	RTRV-PATH-VT1
ALW-LPBK-T1	ENT-CONF-STS1	RST-LINK	RTRV-PM-EC1
ALW-LPBK-T3	ENT-CONF-T1	RTRV-ALM-ALL	RTRV-PM-T1
ACT-LPBK-VT1	ENT-CONF-VT1	RTRV-ALM-COM	RTRV-PM-T3
ALW-MSG-EC1	ENT-CRS-STS1	RTRV-ALM-EC1	RTRV-PM-VT1
ALW-MSG-VT1	ENT-CRS-T1	RTRV-ALM-EQPT	RTRV-PMCENFRN-T1
ALW-PMREPT-EC1	ENT-CRS-VT1	RTRV-ALM-LINK	RTRV-PMMODE-EC1
ALW-PMREPT-T1	ENT-EQPT	RTRV-ALM-T1	RTRV-PMMODE-VT1
ALW-PMREPT-T3	ENT-FAN-FILTER	RTRV-ALM-T2	RTRV-PMSCHED-EC1
ALW-PMREPT-VT1	ENT-ROLL-STS1	RTRV-ALM-T3	RTRV-PMSCHED-T1
ALW-SW-EQPT	ENT-ROLL-T1	RTRV-ALM-VT1	RTRV-PMSCHED-T3
CANC-ECHO-LINK	ENT-ROLL-VT1	RTRV-ATTR-EC1	RTRV-PMSCHED-VT1
CANC-USER	ENT-SECU-USER	RTRV-ATTR-EQPT	RTRV-PORT
CHG-ACCMD-T1	ENT-SYSID	RTRV-ATTR-T1	RTRV-PRMTR-LINK
CHG-ACCMD-T1	ENT-TSTPT-EC1	RTRV-ATTR-T2	RTRV-SCANTH-NE
CHG-ACMD-VT1	ENT-TSTPT-T1	RTRV-ATTR-T3	RTRV-SECU-AUD
CHG-TACC-EC1	ENT-TSTPT-VT1	RTRV-ATTR-VT1	RTRV-SECU-LINK
CHG-TACC-T1	EX-EQPT	RTRV-CMD-STAT	RTRV-SECU-USER
CHG-TACC-VT1	INH-LPBK-EC1	RTRV-COND-EC1	RTRV-STATE-EC1
CONN-PM-T1	INH-LPBK-T1	RTRV-COND-EQPT	RTRV-STATE-EQPT
CONN-TACC-EC1	INH-LPBK-T3	RTRV-COND-LINK	RTRV-STATE-T1
CONN-TACC-T1	INH-LPBK-VT1	RTRV-COND-T1	RTRV-STATE-VT1
CONN-TACC-VT1	INH-MSG-EC1	RTRV-COND-T2	RTRV-SYCN
CPY-MEM	INH-MSG-VT1	RTRV-COND-T3	RTRV-SYSID
DGN-DET-EQPT	INH-PMREPT-EC1	RTRV-COND-VT1	RTRV-T1
DISC-PM-T1	INH-PMREPT-T1	RTRV-CONF-STS1	RTRV-T3
DISC-TACC	INH-PMREPT-T3	RTRV-CONF-T1	RTRV-TACC-EC1
DLT-CONF-STS1	INH-PMREPT-VT1	RTRV-CONF-VT1	RTRV-TACC-T1
DLT-CONF-T1	INH-SW-EQPT	RTRV-CRS	RTRV-TACC-VT1
DLT-CONF-VT1	INIT-REG-EC1	RTRV-CRS-STS1	RTRV-TH-EC1
DLT-CRS-STS1	INIT-REG-T	RTRV-CRS-T1	RTRV-TH-T1
DLT-CRS-T1	INIT-REG-T3	RTRV-CRS-VT1	RTRV-TH-T3
DLT-CRS-VT1	INIT-REG-VT1	RTRV-DROPCRS-STS1	RTRV-TH-VT1
DLT-EQPT	INIT-SYS	RTRV-DROPCRS-T1	RTRV-TH-NE
DLT-SECU-AUD	OPR-ACO-ALL	RTRV-DROPCRS-VT1	RTRV-VT1
DLT-SECU-USER	OPR-LPBK-EC1	RTRV-EC1	SCHED-PMREPT-EC1
ED-DATE	OPR-LPBK-T1	RTRV-ECHO-LINK	SCHED-PMREPT-T1
ED-EC1	OPR-LPBK-T3	RTRV-EQPT	SCHED-PMREPT-T3
ED-EQPT	OPR-LPBK-VT1	RTRV-HDR	SCHED-PMREPT-VT1
ED-NE	RLS-LPBK-EC1	RTRV-LPBK-EC1	SET-ATTR-EC1
ED-PRMTR-LINK	RLS-LPBK-T1	RTRV-LPBK-T1	SET-ATTR-EQPT
ED-SECU-LINK	RLS-LPBK-T3	RTRV-LPBK-T3	SET-ATTR-T1
ED-SECU-PID	RLS-LPBK-VT1	RTRV-LPBK-VT1	SET-ATTR-T2
ED-SECU-USER	RLS-TSTPT-EC1	RTRV-MSG-EC1	SET-ATTR-T3

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ED-STATE-EQPT	RLS-TSTPT-T1	RTRV-MSG-VT1	SET-ATTR-VT1
Command	Autonomous Message	Autonomous Message	Autonomous Message
SET-PMODE-EC1	REPT ALM COM	REPT DROPCRS T1	REPT RSTCRS STS1
SET-PMODE-VT1	REPT ALM EC1	REPT DROPCRS VT1	REPT RSTCRS T1
SET-SCANTH-NE	REPT ALM EQPT	REPT EVT EC1	REPT RSTCRS VT1
SET-SID	REPT ALM LINK	REPT EVT T1	REPT SW
SET-TH-EC1	REPT ALM T1	REPT EVT T3	REPT TRMSN T1
SET-TH-T1	REPT ALM T2	REPT EVT VT1	
SET-TH-T3	REPT ALM T3	REPT EXCPTN SYS	
SET-TH-VT1	REPT ALM VT1	REPT FAN FILTER	
STA-SCANPM-T1	REPT BKUP	REPT LOCL IN	
STP-SCANPM-T1	REPT CMPR MEM	REPT PM EC1	
SW-DX-EQPT	REPT DBCHG	REPT PM T1	
SW-TOPROTN-EQPT	REPT DGNDT EQPT	REPT PM T3	
SW-TOWKG-EQPT	REPT DISC TACC	REPT PM VT1	
TEST-CABLE	REPT DLTCRS STS1	REPT RMV EQPT	
TEST-SW-CONTROL	REPT DLTCRS T1	REPT RMV LINK	
TEST-TRMSN-T1	REPT DLTCRS VT1	REPT RST EQPT	
TEST-UNIT-CABLE	REPT DROPCRS STS1	REPT RST LINK	

## 4. Facility Address (EID)

### 4.1 STS-1 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{port number} (Unit-STS-1 Port) for the STS-1 ports must be addressed as follows:

- o Individually or as a range:
  - For STS1 Interface-16 Modules, only: {1-32}-{1-15}**
- o As all ports in an STS1 Interface Module: **UNIT-{1-32}**

### 4.2 VT1.5 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{slot number}-{port number} (Unit-STS-1 Equivalent-VT1.5 Port) for the VT1.5 ports must be addressed as follows:

- o Individually or as a range:
  - For STS1 Interface-16 Modules, only: {1-32}-{1-15}-{1-28}**
- o As an individual or a range of VT1GRPs (group of 28 VT1.5 tributaries):
  - For STS1 Interface-16 Modules: {1-32}-{1-15}**
- o As all ports in an STS1 Interface Module: **UNIT-{1-32}**

### 4.3 DS1 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{slot number}-{port number} (Unit-DS3 Equivalent-DS1 Port) for the DS1 ports must be addressed as follows:

- o Individually or as a range:
  - For STS1 Interface-16 Modules: {1-32}-{1-15}-{1-28}**
  - For DS3 Interface-32 Modules: {1-32}-{1-31}-{1-28}**
  - For DS3 Interface-16 Modules: {1-32}-{1-15}-{1-28}**
  - For DS1 Interface Modules: {1-32}-{1-8}-{1-28}**
  - For DS1 Interface-P Modules: {1-32}-{1-7}-{1-28}**
- o As an individual or a range of DS1GRPs (group of 28 DS1 ports functioning as a DS3 equivalent):
  - For STS1 Interface-16 Modules: {1-32}-{1-15}**
  - For DS3 Interface-32 Modules: {1-32}-{1-31}**
  - For DS3 Interface-16 Modules: {1-32}-{1-15}**
  - For DS1 Interface Modules: {1-32}-{1-8}**

**For DS1 Interface-P Modules: {1-32}-{1-7}**

- o As all ports in a interface module: **UNIT-{1-32}**

## 5. Allowable Commands for Various Main Controller States

Most system functions are not allowed when the main controller (MC) is not in service. Certain functions, however, either can be performed with the MC out of service, or require the MC to be out of service to be performed. The following lists the allowable commands for the given state of the MC:

### o OOS-FLT state:

**DGN-DET-EQPT** (on MC, and MC subentities\* in the IS state)  
**INIT-SYS** (Initialization Level 9)  
**RTRV-CMD-STAT**  
**RTRV-STATE-EQPT** (on MC)  
**RST-EQPT** (on MC)

\* MC subentities include: CPU-0, CPU-1, UI, MTC-0, MTC-1, SSC-0, SSC-1, PRI-1, PRI-2, SEC, ECI-1, ECI-2, SCI-1, SCI-2, CC-0, and CC-1

### o OOS-MTCE state:

**DGN-DET-EQPT** (on MC, and MC subentities\* in the IS state)  
**INIT-SYS** (Initialization Level 9)  
**RTRV-CMD-STAT**  
**RTRV-STATE-EQPT** (on the MC)  
**RST-EQPT** (on the MC, PRI, and SEC)  
**RMV-EQPT** (on SEC)  
**CPY-MEM**

\* MC subentities include: CPU-0, CPU-1, UI, MTC-0, MTC-1, SSC-0, SSC-1, PRI-1, PRI-2, SEC, ECI-1, ECI-2, SCI-1, SCI-2, CC-0, and CC-1

\*\* See **CPY-MEM** command early in the DACS IV-2000 Release 3.0 Commands and Messages manual (AT&T 365-340-402) for details.

### o OOS-MCOND state:

**DGN-DET-EQPT** (on MC, and MC subentities\* in the IS state)  
**INIT-SYS** (Initialization Level 9)  
**RTRV-CMD-STAT**  
**RTRV-STATE-EQPT** (on the MC)  
**RST-EQPT** (on the MC, PRI, and SEC)  
**RMV-EQPT** (on the PRI and SEC)  
**RTRV-SYSID**  
**ENT-SYSID**  
**CPY-MEM**

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\* MC subentities include: CPU-0, CPU-1, UI, MTC-0, MTC-1, SSC-0, SSC-1, PRI-1, PRI-2, SEC, ECI-1, ECI-2, SCI-1, SCI-2, CC-0, and CC-1

\*\* See **CPY-MEM** command early in the DACS IV-2000 Release 3.0 Commands and Messages manual (AT&T 365-340-402) for details.

o **IS state** the following commands are **not** allowed:

**RMV-EQPT** (on the only in-service PRI)

**CPY-MEM\*\***

\*\* See **CPY-MEM** command early in the DACS IV-2000 Release 3.0 Commands and Messages manual (AT&T 365-340-402) for details.

## 6. Error Codes

Error Code	Error Condition
EHNS	Equipment hierarchy not satisfied
ENEQ	Equipage, not equipped
ENMB	Equipage, not a multipoint bridge
ENRD	Equipage, not redlined
ENRE	Equipage, not recognized equipage
ERLC	Equipage, a redlined circuit
IBEX	Input, extra block
IBNC	Input, block not consistent
IDMS	Input, data missing
IDNC	Input, data not consistent
IDNV	Input, data not valid
IDRG	Input, data, range error
IICT	Input, invalid CTAG
IISP	Input, invalid syntax or punctuation
IITA	Input, invalid target identifier (TID)
ISCH	Input, syntax character error in input command
ISPC	Input, syntax punctuation error in input command
PICC	Privilege, illegal command code
PIOC	Privilege, illegal operations channel
PIPW	Privilege, illegal password/user id code
PIRC	Privilege, illegal record control
PIUI	Privilege, illegal user identity
PKOR	Circuit pack out of range
PLNA	Privilege, login not active
SAAL	Status, already allowed
SAAS	Status, already assigned
SABT	Status, execution stopped abruptly before completion
SACC	Status, already cross-connected
SADC	Status, already disconnected
SAIN	Status, already inhibited
SAIS	Status, already in-service
SAOP	Status, already operated
SAOS	Status, already out-of-service
SAPS	Status, already in protection state
SAPV	Status, already provisioned

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SARB	Status, all resources busy
SARL	Status, already released
SASW	Status, already in switched state
SAWS	Status, already in working state
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SCAT	Status, circuit is already connected to another TAP
SDNC	Status, data in input message is not consistent with the provisioned object entity
SEIP	Status, entity is protected
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SNAS	Status, not assigned
SNCC	Status, not cross-connected
SNDA	Status, no data available
SNDB	Status, no database on the device
SNIS	Status, not in-service
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SNML	Status, no monitor line established
SNOS	Status, not out-of-service
SNPV	Status, not provisioned
SNST	Status, execution could not be started
SNVS	Status, not in valid state
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SOSF	Status, out-of-service, failed
SOST	Status, out-of-service testing
SPFA	Status, protection entity failed
SRIP	Status, request inconsistent with provisioning
SROF	Status, requested operation failed
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SSTP	Status, execution stopped gracefully before completion
SVTF	Status, validation of tape failed
SWFA	Status, working entity failed
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## 7. Main Fuse Panel and Charts

Tables 1, 2, and 3 relate DACS IV-2000 system fuses for bays, interface modules, and interface module shelves to their physical location on the fuse and alarm panel (see Figure 5) at the top of the Switch Bay.

**Note:** Fuses for power buses A, B, C, and D come in pairs with the load fuse labeled with -1 and the indicator fuse labeled with -2. Fuses for power bus E do not have dual fuses (one load and one indicator), they are all indicator fuses.

## 8. Secondary Fuses

See Figure 6 and Table 4.

## 9. Redundant Controller Power Module Fuses

(See Figure 7.)

## **10. Equipment Module Diagrams**

### **10.1 Switch Power Module**

See Figure 8.

### **10.2 Auxiliary and Redundant Controller Power and Synchronizer Modules**

See Figure 9

### **10.3 Redundant Controller Module**

See Figure 10.

### **10.4 Switch Module**

See Figure 11.

### **10.5 DS1 Interface/Interface-Protection Module**

See Figure 12.

For provisioned DS1 Interface and DS1 Interface- Protection Modules, see minimum equipage tables on next page. For unprovisioned DS1 Interface Modules within a DS1 interface protection group associated with a provisioned DS1 Interface-Protection Module, all DS1IF circuit pack slots must be equipped with either BXA or DS1IF circuit packs and all SWIF circuit packs slots must be equipped with either BXA or SWIF circuit packs if the DS1 Interface Module has been cabled (that is, an DS1 Interface Module that is not cabled can be left empty). If the DS1 Interface-Protection Module within an DS1 interface protection group is unprovisioned, no circuit packs are required in any of the interface modules associated with the DS1 Interface-Protection Module; but, are recommended to keep out dust and other foreign matter.

See Tables 5 and 6.

### **10.6 DS3 Interface-32 Module**

See Figure 13 and Table 7.

### **10.7 DS3 Interface-16 Module**

See Figure 14 and Table 8.

### **10.8 STS1 Interface-16 Module**

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See Figure 15 and Table 9.

## 11. Circuit Pack Cross- Reference

Module	Circuit Pack	Code	System Address
RC Module	CPU2	AWP6	CPU- {0,1}
	ECI3	AWP8	ECI- {1,2}
	MTC3	AWR10	MTC- {0,1}
	PRI2	ED-9C046	PRI- {1,2}
	SCI3	AWR2C	SCI- {1,2}
	SEC2	ED-9C050	SECSSC- {0,1}
	SSC2	AWP7	STPNL
	STPNL UI2	ED-9C046 AWR12	UI
SYNC Module	DPLL1	AWP9	DPLL- {0,1}
	DS1TX1	AWS5	TX- {0,1} /TXPT- {0,1}- {1,2}
	TBS31	AWS3	TB- {0,1}
RC Power Module	PWRF	427AA	PWRF- {1,2}
	PWRG	428AA	PWRG- {1,2}
	FBF	ED-9C051	-
	FBG	ED-9C052	-
	FBH	ED-9C053,G2	-
	FBI	ED-9C055	-
SW Module	SWIO1	AWR6	SWIO- {1-32}
	SWCS1	AWS1B	SWCS- {1-32}
	CLKGN2	AWR7	CLKGN- {0,1}
SW Power Module	PWRA	552A	PWRA- {1-4}
	FBA	ED-2C962-30,G1	-
	FBB	ED-2C960-30,G1	-
	FBC	ED-2C963-30,G1	-
	FBD	ED-2C961-30,G1	-
AUX Power Module	PWRE3	556C	PWRE2-SW- {1,2}
DS1 Interface Modules	CLKDR1	AKM56	CLKDR- {1-32}- {1-4}
	DS1IF1	AKM46/AKM46B	DS1IF- {1-32}- {1A-8B}
	DS1IP1	AKM47	DS1IP- {1-32}- {PA,PB}
	DS1RY1	AKM48	DS1RY- {1-32}- {1-4}
	PMGR1	AKM66	SWIF- {1-32}- {1-8}
	SWIF1/SWIF2	AKM49/AKM50	SWIF- {1-32}- {1-8,P}
	UC/UC2	AKM59/AKM59B	UC- {1-32}
	PWRE3	556C	PWRE- {1-32}- {1,2}
	BXA1	AKM64	-
DS3 Interface Modules	CLKDR1	AKM56	CLKDR- {1-32}- {1-4}
	DS3PM1	AKM62	DS3PM- {1-32}
	MUX1/MUX2	AKM52/AKM68B	MUX- {1-32}- {1-31}
	MUXP1/MUXP2	AKM55/AKM70B	MUXP- {1-32}

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	MUXPS1	AKM53	MUXPS- {1-32}
	PMGR1	AKM66	MUX- {1-32} - {1-31}
	UC/UC2	AKM59/ AKM59B	UC- {1-32}
	PWRE3	/556C	PWRE- {1-32} - {1, 2}
	BXA1	AKM64	-
STS1 Interface Modules	CLKDR1	AKM56	CLKDR- {1-32} - {1-4}
	SMUX1	AKM84	SMUX- {1-32} - {1-15}
	SMUXP1	AKM85	SMUXP- {1-32}
	MUXPS1	AKM53	MUXPS- {1-32}
	UC/UC2	AKM59/ AKM59B	UC- {1-32}
	PWRE3	556C	PWRE- {1-32} - {1, 2}
	BXA1	AKM64	-

## 12. Expendable Equipment Cross-Reference

Equipment (Location)	Part Number	Expected Life
Tape Drive Cleaning Kit	406646844	N/A
Cleaning Kit Refill	406646851	N/A
Fan Filter:		
Fan Assembly ED2C816-30,G1 (SW Bay)	405056078	3 -6 Months
Fan Assembly ED2C906-30 (SW Bay)	405470808	3-6 Months
Fan Assembly ED-9C130, G1 (SW Bay)	WP-92310,L100	3-6 Months
Fan Assembly ED-9C130,G2 (STS1/DS3 Bay)	WP-92310,L100	3-6 Months
Database Backup System Tape	J9878650-4,L3	90 Backups
Fuse Extractor Tool	WP-90247,L201	N/A
Fuses:		
12 A Main Fuse (Main Fuse Panel)	KS19780,L8	N/A
10 A Main Fuse (Main Fuse Panel)	KS19780,L2	N/A
5 A 70D Indication Fuse (Main Fuse Panel)	100203355	N/A
2 A 70B Indication Fuse (Main Fuse Panel)	100203330	N/A
0.5 A 70G Indication Fuse (Main Fuse Panel)	100203389	N/A
10 A SW PWR MOD 77D Fuse (FBA and FBB)	KS-23543L77D	N/A
7.5 A SW PWR MOD 78J Fuse (FBC and FBD)	KS-23543L78J	N/A
7.5 A RC PWR MOD Fuse (FBI)	WP-90247L314	N/A
5 A RC PWR MOD Fuse (FBF, FBG, and FBH)	WP-90247L313	N/A
2 A RC PWR MOD Fuse (FBH and FBI)	WP-90247L309	N/A
1 A RC PWR MOD Fuse (FBF and FBG)	WP-90247L306	N/A
0.5 A RC PWR MOD Fuse (FBI)	WP-90247L303	N/A

### 13. Provisioning Sequence

Entity	Supporting Entities Required To Provision
SWIO [1] (provisioned in pairs)	None
UNIT	None (DS1 Interface Module requires supporting DS1 Interface-Protection Module)
DS3PM (optional) [4]	UC
CLKDR [2] (provisioned in pairs)	UNIT, SWIO
MUXP [3]	CLKDR
MUX [3]	MUXP
DS1RY [5]	UNIT
SWIF [5]	CLKDR
DS1IP [5]	SWIF, DS1RY
DS1IF**	SWIF, DS1RY, DS1IP (supporting DS1IP circuit pack can be in another UNIT)
TX (provisioned in pairs)	DPLL
TB (provisioned in pairs)	DPLL
CLKGN3	DPLL, TB
SMUXP [6]	CLKDR
SMUX [6]	SMUXP
PMGR1 (optional)	UC, CLKDR

[1] Provisioned as a result of entering the **ENT-EQPT** and **RST-EQPT** commands. SWIO circuit packs are automatically provisioned when the software release is downloaded and/or by initialization via the **INIT-SYS:::9** command.

[2] Provisioned automatically when a interface module is provisioned with the **RST-EQPT** command.

[3] Provisioned automatically when an DS3 Interface Module is provisioned with the **RST-EQPT** command.

[4] DS3PM circuit packs are not supported in STS1 Interface-16

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Modules.

- [5] Provisioned automatically when a DS1 Interface or DS1 Interface-Protection Module is provisioned with the **RST-EQPT** command.
- [6] Provisioned automatically when an STS1 Interface Module is provisioned with the **RST-EQPT** command.

## 14. Loopbacks

The DACS IV-2000 system provides DS1 signal loopback, DS3 line loopback, STS-1 signal loopback, and VT1.5 wideband (terminal) loopback features that can be used to facilitate testing and trouble isolation. DS1 facilities and DS1 tributaries on DS3 facilities and EC-1 facilities can be looped back. STS-1 and VT1.5 loopbacks are performed through EC-1 facilities only. Figure 16 shows examples of the possible loopback features available in the DACS IV-2000 system. The following is a list of the different loopback types available:

- o DS1 Loopbacks - can be operated on a specified DS1 port or range of DS1 ports, either towards the facility, towards the switch, or through the switch fabric of a DS1 Interface, a DS3 Interface (tributary of a DS3), or an STS1 Interface (as a VT1.5 tributary) Module within the system. DS1 loopbacks can be one of the following four types:
  - LPBKL (Line Loopback) - loops the signal from the input port to the output port (towards the facility) at the DS1 Interface Module.
  - LPBKT (Terminal Loopback) - loops the signal from the input port to the output port (through the switch fabric) in the switch module. DS1 terminal loopbacks are valid for near-end on either DS1 interface (DS1IF), DS3 interface (MUX or MUX2), or SONET interface (SMUX) circuit packs.
  - LPBKI (Internal Loopback) - loops the signal from the output port to the input port (towards the switch) at the DS1 Interface Module.
  - LPBKM (DS1 Tributary Loopback) - loops a DS1 tributary signal, within a DS3 interface circuit pack from the input port to the output port (towards the facility) at the DS3 Interface Module. DS1 tributary loopbacks are valid for either near-end or far-end on MUX2 circuit packs only.
- o DS3 Line Loopbacks - connect (or loopback) incoming DS3 signals directly to the outgoing direction of the same port. This loopback happens directly in the MUX2 circuit pack. This keeps the signal from entering the switch matrix and thus keeps the amount of hardware encountered to a minimum. Because the signal is not demultiplexed, it retains all its control bits, overhead bits, and bipolar violations; and preserves the timing

of the looped back signal. The only modification of the DS3 signal occurs when the system regenerates the signal to meet the specifications for an outgoing DS3 signal.

- o STS-1 Loopbacks - can be operated on a specified STS-1 port or range of STS-1 ports, either towards the facility or through the switch fabric of an STS1 Interface Module. STS-1 loopbacks can be one of the following two types:
  - LPBKL (Line Loopback) - loops the signal from the input port to the output port (towards the facility) at the STS1 Interface Module.
  - LPBKT (Terminal Loopback) - loops the signal from the input port to the output port through the switch fabric in the switch module. STS-1 terminal loopbacks are valid for near-end on SMUX circuit packs.
- o VT1.5 Wideband (Terminal) Loopbacks - can be operated on a specified VT tributary of an STS-1 signal as a terminal loopback (LPBKT), which loops the VT1.5 signal from the input port to the output port through the switch fabric in the switch module.

## 15. Test Access

### 15.1 General

When working with test access connections, you need to be familiar with terms such as E-END, F-END, and A and B direction (see Figure 17). The E-END and F-END are arbitrarily designated as Near-End (E-END) and Far- End (F-END) of a one-way or a two-way cross-connection, as a signal travels through the DACS IV-2000 frame. These signals are terminated at DS1, DS3, or STS1 Interface Modules. Test access can be established at either the E-END or the F-END through a FAD. As signals travel through the frame, the path through the frame from the E-END to the F-END is referred to as the A direction and the path from the F-END to the E-END is the B direction. In a one-way cross-connection, the signal travels in the A direction. The In and Out designations indicate the direction to/from the E-End and F-End. Once you designate the Near-End (E-END) and Far-End (F-END), the designations must not change during the test access session.

There are ten modes of test access in the DACS IV-2000 system. These modes are:

MONE	SPLTE
MONF	SPLTF
MONEF	SPLTEF
SPLTA	LOOPE
SPLTB	LOOPF

Each mode is described in the following sections.

### 15.2 Monitor Test Access Connections

#### 15.2.1 MONE Mode

The MONE mode of test access monitors the E-END of an idle port, a one-way cross-connection, or a two-way cross-connection. It reads the incoming signal in direction A. A MONE test access connection is established with one of the following commands

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,:::MONE; (Figure 18) VT1.5:
CONN-TACC-VT1::15-1-1,15-1-3,:::MONE; STS-1: CONN-TACC-EC1::15-
1,15-3,:::MONE;
```

In Figure 18, a monitor test access connection is established from a testport located at port 1 of DS1GRP-15-1 to an idle port located at port 3 of DS1GRP-15-1. If the E-END is idle, the connections shown by the dotted and dashed lines are not present. If there is a one-way cross-connection from the E-END to the F-END, the connection shown by the dashed line is not present.

## 15.2.2 MONF Mode

The MONF mode of test access monitors the F-END of a two-way cross-connection. It reads the incoming signal in direction B. A MONF test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::MONF; (Figure 19)
VT1.5: CONN-TACC-VT1::15-1,15-3,15-4::MONF; STS-1: CONN-TACC-
EC1::15-1-1,15-1-3,15-1-4::MONF;
```

In Figure 19, a monitor test access connection is established on the F-END of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport.

## 15.2.3 MONEF Mode

The MONEF mode of test access monitors both directions of a two-way cross-connection. This mode of test access requires two FADs. It reads the incoming signals in directions A and B. A MONEF test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::MONEF; (Figure 20)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4::MONEF; STS-1:
CONN-TACC-EC1::15-1,15-3,15-4::MONEF;
```

In Figure 20, a monitor test access connection is established on both the E-END and the F-END of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Ports 1 and 2 of DS1GRP-15-1 as the testports. Only the odd numbered port of the testport pair is specified in the test access command and the MONEF mode of test access can only be established on a two-way cross-connection.

## 15.3 Split Test Access Connections

### 15.3.1 SPLTA Mode

The SPLTA mode of test access splits the E-END (to FAD) to F-END (from FAD) connection of a one-way or two-way cross-connection to allow testing in the A direction. A SPLTA test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::SPLTA; (Figure 21)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4::SPLTA; STS-1:
CONN-TACC-EC1::15-1,15-3,15-4::SPLTA;
```

In Figure 21, a split test access connection is established in the A direction on a one-way cross-connection from Port 3 of

DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. On a one-way cross-connection from the E-END to the F-END, the connection shown by the dashed line is not present.

### **15.3.2 SPLTB Mode**

The SPLTB mode of test access splits the F-END (to FAD) to E-END (from FAD) connection of a two-way cross-connection to allow testing in the B direction. A SPLTB test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::SPLTB; (Figure 22)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4::SPLTB;
STS-1: CONN-TACC-EC1::15-1,15-3,15-4::SPLTB;
```

In Figure 22, a split test access connection is established in the B direction on a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport.

### **15.3.3 SPLTE Mode**

The SPLTE mode of test access splits the E-END to F-END of an idle port, a one-way cross-connection, or a two-way cross-connection to allow testing at the E-END. The incoming signal in the A direction goes to the input of the FAD and the output of the FAD is sent in the B direction. A SPLTE test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::SPLTE; (Figure 23)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4::SPLTE; STS-1:
CONN-TACC-EC1::15-1,15-3,15-4::SPLTE;
```

In Figure 23, a split test access connection is established at the E-END of a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a quasi-random (QRSS) or IDLE signal is sent to the F-END output port and to any other ports tied to the E-END input port. For a two-way cross-connection, the F-END input port is disconnected from the E-END output port during the test session. If there is a bridge tied to the F-END input port, it is not affected. If the E-END port is idle, the dotted and dashed connections are not present. If there is a one-way cross-connection from the E-END to the F-END, the connection shown by the dashed line is not present.

For DS1 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 SPLTE test access, the output mode of the

F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending path AIS.

#### **15.3.4 SPLTF Mode**

The SPLTF mode of test access splits the F-END to E-END of a two-way cross-connection to allow testing at the F-END. The incoming signal in the B direction goes to the input of the FAD and the output of the FAD is sent in the A direction. A SPLTF test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::SPLTF; (Figure 24)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4::SPLTF; STS-1:
CONN-TACC-EC1::15-1,15-3,15-4::SPLTF;)
```

In Figure 24, a split test access connection is established at the F-END of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a quasi-random (QRSS) or IDLE signal is sent to the E-END output port and to any other ports tied to the F-END input port unless the F-END port is idle. The E-END input port is disconnected from the F-END output port during the test session. If there is a bridge tied to the E-END input port, it is not affected.

For DS1 SPLTF test access, the output mode of the E- End output port, along with any other output ports the F- End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending path AIS.

#### **15.3.5 SPLTEF Mode**

The SPLTEF mode of test access splits both directions of a two-way cross-connection to allow testing at both the E-END and the F-END. This mode of test access requires two FADs. The incoming signal in the A direction goes to the input of FAD-1 and the output of FAD-1 is sent in the B direction. The incoming signal in the B direction goes to the input of FAD-2 and the output of FAD-2 is sent in the A direction. A SPLTEF test access connection is established with one of the following command:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4::SPLTEF; (Figure 25)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4::SPLTEF; STS-1:
CONN-TACC-EC1::15-1,15-3,15-4::SPLTEF;
```

In Figure 25, a split test access connection is established on

both the E-END and the F-END of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Ports 1 and 2 of DS1GRP-15-1 as the testports.

Only the odd numbered port of the testport pair is specified in the test access command and the SPLTEF mode of test access can only be established on a two-way cross-connection.

## 15.4 Loopback Test Access Connections

### 15.4.1 LOOPE Mode

The LOOPE mode of test access establishes a terminal loopback on the E-END port and monitors the loopback signal. It reads the incoming signal in the A direction. A LOOPE test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::LOOPE; (Figure 26)
VT1.5: CONN-TACC-VT1::15-1-1,15-1-3,15-1-4:::LOOPE; STS-1:
CONN-TACC-EC1::15-1,15-3,15-4:::LOOPE;
```

In Figure 26, a loopback test access connection is established on a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a quasi-random (QRSS) or IDLE signal is sent to the F-END output port. The LOOPE mode can be established on either a one-way or a two-way cross-connection. For a two-way cross-connection, the F-END input port is disconnected from the E-END output port during the test session. If there is a bridge tied to the F-END input port, it is not affected. If the E-END port is idle, the dotted and dashed connections are not present. If there is a one-way cross-connection from the E-END to the F-END, the connection shown by the dashed line is not present.

For DS1 LOOPE test access, the output mode of the F- End output port, along with any other output ports the E- End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending path AIS.

### 15.4.2 LOOPF Mode

The LOOPF mode of test access establishes a terminal loopback on the F-END port and monitors the loopback signal. It reads the incoming signal in the B direction. A LOOPF test access connection is established with one of the following commands:

```
DS1: CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::LOOPF; (Figure 27)
```

VT1.5: **CONN-TACC-VT1::15-1-1,15-1-3,15-1-4:::LOOPF;** STS-1:  
**CONN-TACC-EC1::15-1,15-3,15-4:::LOOPF;**

In Figure 27, a loopback test access connection is established on a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a quasi-random (QRSS) or IDLE signal is sent to the E-END output port. The E-END input port is disconnected from the F-END output port during the test session. If there is a bridge tied to the F-END input port, it is not affected.

For DS1 LOOPF test access, the output mode of the E- End output port, along with any other output ports the F- End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending path AIS.

## **16. Performance Monitoring**

### **16.1 DS1 Performance Monitoring Parameters**

See Tables 10, 11, 12, 13, 14, and 15.

### **16.2 Maximum Allowable PMGR Circuit Packs**

See Table 16.

### **16.3 DS3 Performance Monitoring Parameters**

See Table 17.

### **16.4 SONET Performance Monitoring Parameters**

See Tables 18 and 19.

**List of Tables**

**Table 1: Fuse Chart for Switch Bay (Bay 5 Excluding Fan Assembly)**

Auxiliary Power PWRA		Switch Power PWRA			
1	2	1	2	3	4
B14	D8	A2	B2	C2	D2

Note: Fuses A2-1, B2-1, C2-1, and D2-1 are 12 A and fuses B14-1 and D8-1 are 10 A. Fuses A2-2, B2-2, B14-2, C2- 2, D2-2, and D8-2 (indicator fuses) are 0.5 A.

**Table 2: Fuse Chart for Interface Bays**

Shelf	PWR Circuit Pack	Bay 1	Bay 2	Bay 3	Bay 4	Bay 6	Bay 7	Bay 8	Bay 9
4	PWRE-2	C17	D14	D4	D10	C12	D6	B15	C19
	PWRE-1	A17	C15	B4	C10	B12	B6	C8	A19
3	PWRE-2	D16	D13	C4	B10	D12	C6	B8	D18
	PWRE-1	A16	A14	A4	A10	A12	A6	A8	C18
2	PWRE-2	B18	C14	D3	C9	D11	D5	C7	D19
	PWRE-1	A15	B17	C3	B9	B11	C5	B7	A18
1	PWRE-2	D15	C13	B3	D9	C11	B5	D7	D17
	PWRE-1	C16	A13	A3	A9	A11	A5	A7	B19

Note: All load fuses (labeled with -1) are 10 A and all indicator fuses (labeled with -2) are 0.5 A.

**Table 3: Fuse Chart for Fan Assemblies (Switch and Interface Bays)**

Power Source	Bay 2	Bay 3	Bay 4	SW Bay	Bay 6	Bay 7	Bay 8
Main	A16	B18	A17	E6-1	A19	B19	A18
Auxiliary	D16	D15	C17	B13-2	C19	D17	D19

Note: All load fuses (labeled with -1) for bays 2, 3, 4, 6, 7, and 8 are 10 A and all indicator fuses (labeled with -2) are 0.5 A. The switch bay fan assembly fuses E6 and B13-2 are indicator fuses rated at 5 A.

Table 4: Secondary Fuse Chart for the DACS IV-2000 System

Location	Type 77D Fuse (10 A) for +5 V Supply				
	FBA	FBB-1	FBB-2	FBB-3	FBB-4
P	SWIO-11	SWCS-9	SWCS-23	SWIO-21	NC
N	SWIO-10	SWCS-8	SWCS-22	SWIO-20	NC
M	SWIO-9	SWCS-7	SWCS-21	SWIO-19	SWIO-32
-					
L	CLKGN-0	SWCS-6	SWCS-20	SWIO-18	SWIO-31
K	SWIO-8	SWCS-5	SWCS-19	SWIO-17	SWIO-30
J	SWIO-7	SWCS-4	SWCS-18	SWCS-32	SWIO-29
H	SWIO-6	SWCS-3	SWCS-17	SWCS-31	SWIO-28
-					
G	SWIO-5	SWCS-2	SWCS-16	SWCS-30	SWIO-27
F	SWIO-4	SWCS-1	SWCS-15	SWCS-29	SWIO-26
E	SWIO-3	SWIO-16	SWCS-14	SWCS-28	SWIO-25
D	SWIO-2	SWIO-15	SWCS-13	SWCS-27	SWIO-24
-					
C	SWIO-1	SWIO-14	SWCS-12	SWCS-26	SWIO-24
B	-	SWIO-13	SWCS-11	SWCS-25	SWIO-23
A	-	SWIO-12	SWCS-10	SWCS-24	SWIO-22
Location	Type 78J Fuse (7.5A) for -5 V Supply				
	FBC	FBD-1	FBD-2	FBD-3	FBD-4
P	SWIO-11	SWCS-9	SWCS-23	SWIO-21	NC
N	SWIO-10	SWCS-8	SWCS-22	SWIO-20	NC
M	SWIO-9	SWCS-7	SWCS-21	SWIO-19	SWIO-32
-					
L	CLKGN-0	SWCS-6	SWCS-20	SWIO-18	SWIO-31
K	SWIO-8	SWCS-5	SWCS-19	SWIO-17	SWIO-30
J	SWIO-7	SWCS-4	SWCS-18	SWCS-32	SWIO-29
H	SWIO-6	SWCS-3	SWCS-17	SWCS-31	SWIO-28
-					
G	SWIO-5	SWCS-2	SWCS-16	SWCS-30	SWIO-27
F	SWIO-4	SWCS-1	SWCS-15	SWCS-29	SWIO-26
E	SWIO-3	SWIO-16	SWCS-14	SWCS-28	SWIO-25
D	SWIO-2	SWIO-15	SWCS-13	SWCS-27	SWIO-24
-					
C	SWIO-1	SWIO-14	SWCS-12	SWCS-26	SWIO-24
B	-	SWIO-13	SWCS-11	SWCS-25	SWIO-23
A	-	SWIO-12	SWCS-10	SWCS-24	SWIO-22

NC - Not Connected.

**Table 5: DS1 Interface-Protection Module Minimum Equipage**

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
DS1RY1	AKM48	4
DS1IP1	AKM47	2
DS1IF1	AKM46	2
SWIF1/SWIF2	AKM49/AKM50	2
BXA1	AKM64	19
SWIO1	AWR6	2

Note: PMGR circuit packs (AKM66), when used, replace SWIF circuit packs associated with interface groups (not the protection group). Refer to Table [REF. 1] for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused interface group circuit pack (DS1IF and SWIF) slots and the slot between CLKDR-1 and SWIF-2 only, and must not be inserted in any other circuit pack slot (for example, DS1RY slots must never contain BXA circuit packs).

[REF. 1] 16

**Table 6: DS1 Interface Module Minimum Equipage**

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
DS1RY1	AKM48	4
DS1IF1	AKM46	2
SWIF1/SWIF2	AKM49/AKM50	1
BXA1	AKM64	22
SWIO1	AWR6	2

Note: PMGR circuit packs (AKM66), when used, replace SWIF circuit packs. Refer to Table [REF. 1] for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused interface group circuit pack (DS1IF and SWIF) slots and the slot between CLKDR-1 and SWIF-2 only, and must not be inserted in any other circuit pack slot (for example, DS1RY slots must never contain BXA circuit packs).

[REF. 1] 16

**Table 7: DS3 Interface-32 Module Minimum Equipage**

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	4
MUXPS1	AKM53	1
MUXP1/MUXP2	AKM55/AKM70	1
MUX1/MUX2	AKM52/AKM68	1
BXA1	AKM64	31
SWIO1	AWR6	4

Note: PMGR circuit packs (AKM66), when used, replace MUX1/MUX2 circuit packs. Refer to Table [REF. 1] for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused MUX or DS3PM circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs). An optional DS3PM circuit pack (AKM62) can be used in any DS3 Interface-32 Module. Interface modules ordered without the DS3PM circuit pack come with a BXA circuit pack in the DS3PM slot.

[REF. 1] 16

**Table 8: DS3 Interface-16 Module Minimum Equipage**

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
MUXPS1	AKM53	1
MUXP1/MUXP2	AKM55/AKM70	1
MUX1/MUX2	AKM52/AKM68	1
BXA1	AKM64	15
SWIO1	AWR6	2

Note: PMGR circuit packs (AKM66), when used, replace MUX1/MUX2 circuit packs. Refer to Table [REF. 1] for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused MUX or DS3PM circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs). An optional DS3PM circuit pack (AKM62) can be used in any DS3 Interface-16 Module. Interface modules ordered without the DS3PM circuit pack come with a BXA circuit pack in the DS3PM slot.

[REF. 1] 16

**Table 9: STS1 Interface-16 Module Minimum Equipage**

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
MUXPS1	AKM53	1
SMUXP1	AKM85	1
SMUX1	AKM84	1
BXA1	AKM64	14
SWIO1	AWR6	2

Note: BXA circuit packs must be inserted into unused SMUX circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs).

**Table 10: DS1 Performance Parameters**

Parameter	Definition	Parameter	
CVP	Path Code Violation	DM	Degraded Minute
OOFs	Out-of-Frame Second	CVL	Line Code Violations
ESP	Path Errored Seconds	ESL	Line Errored Seconds
BESP	Path Bursty Errored Seconds	SESL	Line Severely Errored Seconds
SESP	Path Severely Errored Seconds	SEFS	Severely Errored Frame Seconds
UAS	Unavailable Seconds	SLS	Slipped Seconds

Table 11: DS1 Performance Monitored Parameters

Location	Monitored Parameter	Full-Time			Camp-On			Scan		
		ESF	SF	UNF	ESF	SF	UNF	ESF	SF	UNF
Near-End	CVL	M	M	M	M	M	M	M	M	-
	ESL	M	M	M	M	M	M	M	M	-
	SESL	M	M	M	M	M	M	M	M	-
	CVP	M	M	-	M	M	-	M	M	-
	ESP	M	M	-	M	M	-	M	M	-
	BESP	M	M	-	M	M	-	-	-	-
	SESP	M	M	-	M	M	-	M	M	-
	OOFs	M	M	-	M	M	-	M	M	-
	DM	M	-	-	M	-	-	-	-	-
UAS	M	M	-	M	M	-	-	-	-	
Far-End	SEFS	M	-	-	M	-	-	M	-	-
	SLS	M	-	-	M	-	-	-	-	-
	ESP	M	-	-	M	-	-	M	-	-
	SESP	M	-	-	M	-	-	M	-	-
	CVP	M	-	-	M	-	-	-	-	-
	BESP	M	-	-	M	-	-	-	-	-
	DM	M	-	-	M	-	-	-	-	-
UAS	M	-	-	M	-	-	-	-	-	

**Table 12: Default Thresholds for Full-Time and Camp-On DS1 Performance Monitoring**

Monitored Parameter		DS1 Framing Format							
		Extended Super Frame				Super Frame		Unframed	
		Far-End		Near-End					
		15 Min and Hourly	Daily	15 Min and Hourly	Daily	15 Min and Hourly	Daily	15 Min and Hourly	Daily
CVP	-	-	53184	132960	6616	16540	-	-	
ESP	-	-	259	648	38	95	-	-	
BESP	-	-	100	600	19	90	-	-	
SESP	-	-	40	100	11	27	-	-	
OOFs	-	-	7	17	7	17	-	-	
DM	-	-	15	360	-	-	-	-	
UAS	-	-	10	10	10	10	-	-	
CVP	53184	132960	-	-	-	-	-	-	
ES	259	648	-	-	-	-	-	-	
BES	100	600	-	-	-	-	-	-	
SES	40	100	-	-	-	-	-	-	
SEFS	7	17	-	-	-	-	-	-	
SLS	7	17	-	-	-	-	-	-	
DM	15	360	-	-	-	-	-	-	
UAS	10	10	-	-	-	-	-	-	
CVL*	-	-	53360	133400	53360	133400	53360	133400	
ESL*	-	-	259	648	259	648	259	648	
SESL*	-	-	40	100	40	100	40	100	

\* Only applicable for DS1 signals terminating on DS1Interface Modules.

Table 13: Default Thresholds for Scan Performance Monitoring

Monitored Parameter	DS1 Framing Format					
	Extended Super Frame				Super Frame	
	Far-End		Near-End			
	15 Min and Hourly	Daily	15 Min and Hourly	Daily	15 Min and Hourly	Daily
CVP	-	-	1772	4432	177	443
ESP	-	-	8	21	1	3
SESP	-	-	1	3	1	3
OOFs	-	-	1	2	1	2
ES	8	21	-	-	-	-
SES	1	3	-	-	-	-
SEFS	1	2	-	-	-	-
CVL*	-	-	53360	133400	53360	133400
ESL*	-	-	259	648	259	648
SESL*	-	-	40	100	40	100

\* Only applicable for DS1 signals terminating on DS1 interface circuit packs.

**Table 14: Thresholds Values for Full-Time and Camp-On DS1 Performance Monitoring**

Monitored Parameter	Far-End			Near-End		
	15 Min	Hourly	Daily	15 Min	Hourly	Daily
CVP	0-2097152	0-8388608	0-134217728	0-2097152	0-8388608	0-134217728
ESP	-	-	-	0-900	0-3600	0-65535
BESP	-	-	-	0-900	0-3600	0-65535
SESP	-	-	-	0-900	0-3600	0-65535
OOF5	-	-	-	0-900	0-3600	0-65535
DM	0-15	0-60	0-1440	0-15	0-60	0-1440
UAS	0-900	0-3600	0-65535	0-900	0-3600	0-65535
ES	0-900	0-3600	0-65535	-	-	-
BES	0-900	0-3600	0-65535	-	-	-
SES	0-900	0-3600	0-65535	-	-	-
SEFS	0-900	0-3600	0-65535	-	-	-
SLS	0-900	0-3600	0-65535	-	-	-
CVL*	-	-	-	0-58981500	0-235926000	0-4294967295
ESL*	-	-	-	0-900	0-3600	0-65535
SESL*	-	-	-	0-900	0-3600	0-65535

\* Only applicable for DS1 signals terminating on DS1 Interface Modules.

**Table 15: Thresholds Values for Scan Performance Monitoring**

Monitored Parameter	Far-End			Near-End		
	15 Min	Hourly	Daily	15 Min	Hourly	Daily
CVP	-	-	-	0-65535	0-65535	0-65535
ESP	-	-	-	0-900	0-3600	0-65535
SESP	-	-	-	0-900	0-3600	0-65535
OOF5	-	-	-	0-900	0-3600	0-65535
ES	0-900	0-3600	0-65535	-	-	-
SES	0-900	0-3600	0-65535	-	-	-
SEFS	0-900	0-3600	0-65535	-	-	-
CVL*	-	-	-	0-2097152	0-8388608	0-134217728
ESL*	-	-	-	0-900	0-3600	0-65535
SESL*	-	-	-	0-900	0-3600	0-65535

\* Only applicable for DS1 signals terminating on DS1 interface circuit packs.

**Table 16: Maximum Allowable PMGR Circuit Packs per Interface Module**

Interface Module Type	Performance Monitoring Mode	
	Full-Time/Camp-On	Scan
DS3 Interface-32	16	0
	8	1
	2	2
DS3 Interface-16	15	0
	8	1
DS1 Interface	8	0
	7	1/0*
DS1 Interface-Protection	7	0
	6	1/0**

\* Zero if there is a SCAN performance monitoring PMGR circuit pack in the associated DS1 Interface-Protection Module.

\*\* Zero if there is a SCAN performance monitoring PMGR circuit pack in the associated DS1 Interface Module.

Table 17: Threshold Values for DS3 Performance Monitoring

Parameter	Interval					
	15 Minutes		1 Hour		24 Hours	
	Default	Range	Default	Range	Default	Range
PSET#1 (CB149)						
Number of Block Errors (BEC)	4000	0-8458200	-	-	386500	0-81198720
0						
Errored Seconds A (ESA)	30	0-900	-	-	90	0-65535
Errored Seconds B (ESB)	30	0-900	-	-	90	0-65535
Errored Seconds C (ESC)	20	0-900	-	-	60	0-65535
Out-of-Frame Seconds (OOFs)	10	0-900	-	-	30	0-65535
Unavailable Seconds (UAS)	30	0-900	-	-	90	0-65535
PSET#2 (TR820)						
Coding Violations (CV)	4000	0-8458200	16100	0-33832800	386500	0-
Errored Seconds (ES)	40	0-900	40	0-3600	90	811987200
Severely Errored Seconds (SES)	20	0-900	20	0-3600	60	0-65535
Out-of-Frame Seconds (OOFs)	10	0-900	10	0-3600	30	0-65535
Unavailable Seconds (UAS)	30	0-900	30	0-3600	90	0-65535

**Table 18: STS-1 and VT1.5 Performance Monitored Parameters**

Monitored Parameter		STS-1			VT1.5
		Section	Line	Path	Path
Near-End	Severely Errored Frame Seconds(SEFS)	M	-	-	-
	Loss-of-Signal Seconds (LOSS)	M	-	-	-
	Coding Violations (CV)	-	M	M	M
	Errored Seconds (ES)	-	M	M	M
	Errored Seconds A (ESA)	-	M	M	M
	Errored Seconds B (ESB)	-	M	M	M
	Severely Errored Seconds (SES)	-	M	M	M
	AIS Seconds (AISS)	-	M	-	M
	AIS/Loss-of-Pointer Seconds (ALS)	-	-	M	M
	Unavailable Seconds (UA)S	-	M	M	M
Far-End	Coding Violations (CV)	-	-	M	-
	Errored Seconds (ES)	-	-	M	-
	Errored Seconds A (ESA)	-	-	M	-
	Errored Seconds B (ESB)	-	-	M	-
	Severely Errored Seconds (SES)	-	-	M	-
	Unavailable Seconds (UAS)	-	-	M	-

Note: M means monitoring is available for the parameter specified.

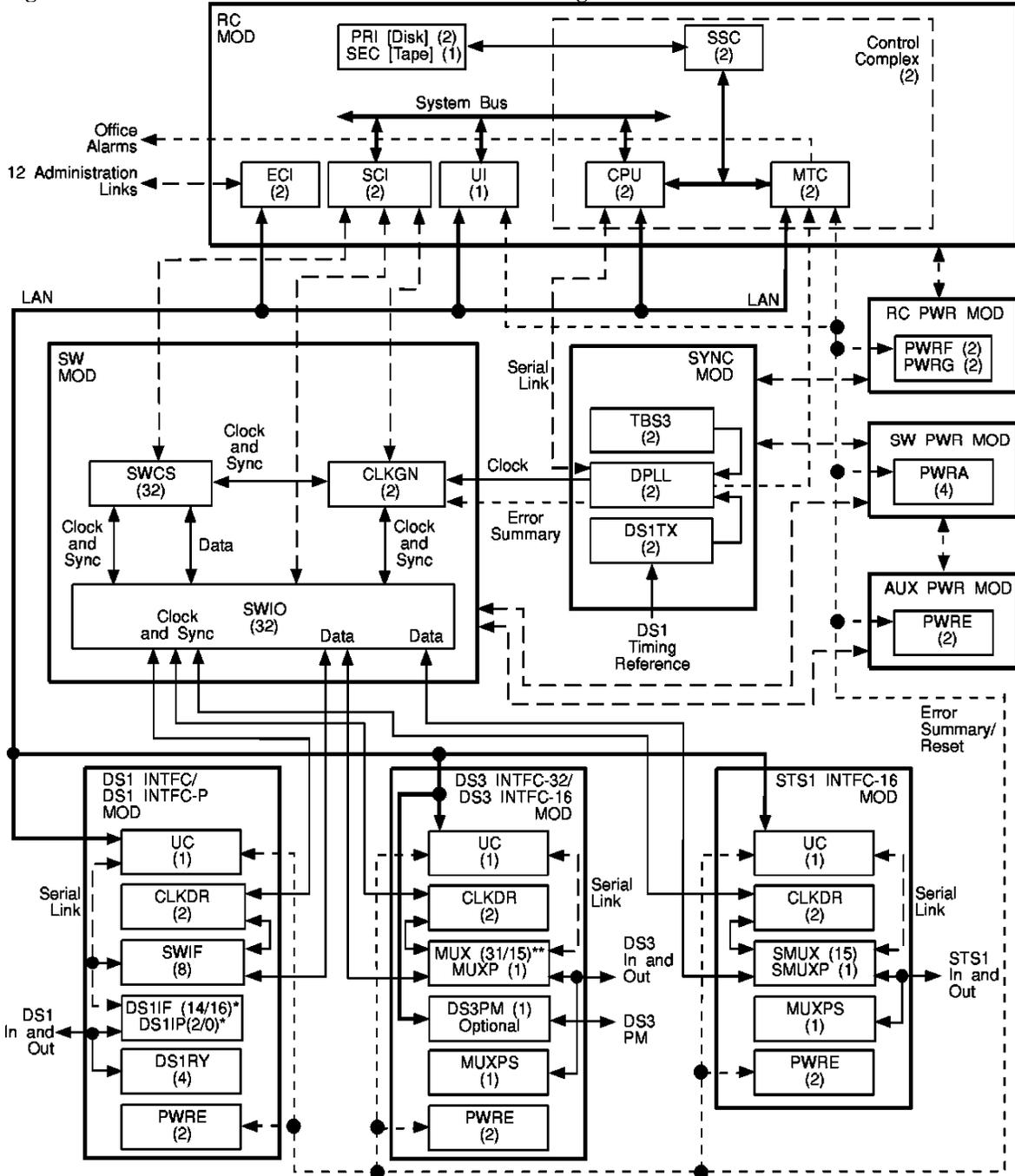
**Table 19: Threshold Values for STS-1 and VT1.5 Performance Monitoring**

Parameter Name	Accumulation Interval			
	15 Min		Day	
	Default	Range	Default	Range
STS-1 Section Performance Monitoring Parameters (Near-End)				
SEFS	10	0-900	100	0-86400
LOSS	10	0-900	100	0-86400
STS-1 Path and Line Performance Monitoring Parameters (Near-End)				
CV	4666	0-46660	447900	0-447900
ES	65	0-900	648	0-86400
ESA	65	0-900	648	0-86400
ESB	65	0-900	648	0-86400
SES	10	0-900	100	0-86400
AISS (line only)	10	0-900	100	0-86400
ALS (path only)	10	0-900	100	0-86400
UAS	10	0-900	100	0-86400
STS-1 Path Performance Monitoring Parameters (Far-End)				
CV	4666	0-46660	447900	0-447900
ES	65	0-900	648	0-86400
ESA	65	0-900	648	0-86400
ESB	65	0-900	648	0-86400
SES	10	0-900	100	0-86400
UAS	10	0-900	100	0-86400
VT1.5 Path Performance Monitoring (Near-End)				
CV	156	0-16383	14930	0-1048575
ES	65	0-900	648	0-86400
ESA	65	0-900	648	0-86400
ESB	65	0-900	648	0-86400
SES	10	0-900	100	0-86400
ALS	10	0-900	100	0-86400
UAS	10	0-900	10	0-86400



# List of Figures

Figure 1: DACS IV-2000 Release 3.0 Functional Block Diagram



**Notes:**

Numbers in parentheses indicate the quantity of the specified entity.

\* X/Y (X = DS1 INTFC, Y = DS1 INTFC-P)

\*\* X/Y (X = DS3 INTFC-32, Y = DS3 INTFC-16)

**Legend:**

- Transmission/Data
- - - Control
- - - Alarm/Reset/Error

Figure 2: Physical Associations of Bays, Units, and Interbay Cables in a Maximum Configuration of DS1 Interface Modules

4	SWIO 16 N-Rate H 1 J-16	8	SWIO 12 N-Rate F 5 J-12	12	SWIO 8 N-Rate D 9 J-8	16	SWIO 4 N-Rate B 13 J-4	External Misc T/S			20	SWIO 20 N-Rate K 17 J-20	24	SWIO 24 N-Rate M 21 J-24	28	SWIO 28 N-Rate P 25 J-28	32	SWIO 32 N-Rate T 29 J-32
								Fuse & Alarm										
								Switch Power Module										
3	SWIO 15 N-Rate H 1 J-15	7	SWIO 11 N-Rate F 5 J-11	11	SWIO 7 N-Rate D 9 J-7	15	SWIO 3 N-Rate B 13 J-3	Sync Mod	RC Pwr Mod	Aux Pwr Mod	19	SWIO 19 N-Rate K 17 J-19	23	SWIO 23 N-Rate M 21 J-23	27	SWIO 27 N-Rate P 25 J-27	31	SWIO 31 N-Rate T 29 J-31
								Redundant Controller Module										
2	SWIO 14 N-Rate G 1 J-14	6	SWIO 10 N-Rate E 5 J-10	10	SWIO 6 N-Rate C 9 J-6	14	SWIO 2 N-Rate A 13 J-2	Switch Module			18	SWIO 18 N-Rate J 17 J-18	22	SWIO 22 N-Rate L 21 J-22	26	SWIO 26 N-Rate N 25 J-26	30	SWIO 30 N-Rate R 29 J-30
1	SWIO 13 N-Rate G J-13	5	SWIO 9 N-Rate E J-9	9	SWIO 5 N-Rate C J-5	13	SWIO 1 N-Rate A J-1				17	SWIO 17 N-Rate J J-17	21	SWIO 21 N-Rate L J-21	25	SWIO 25 N-Rate N J-25	29	SWIO 29 N-Rate R J-29
1		2		3		4		5			6		7		8		9	
Bay Position																		

Note: Units 1, 5, 9, 13, 17, 21, 25, and 29 are all DS1 Interface-Protection Modules. All other units are DS1 Interface Modules.

**Figure 3: Physical Associations of Bays, Units, and Interbay Cables in a Maximum Configuration of DS3 Interface-32 Modules**

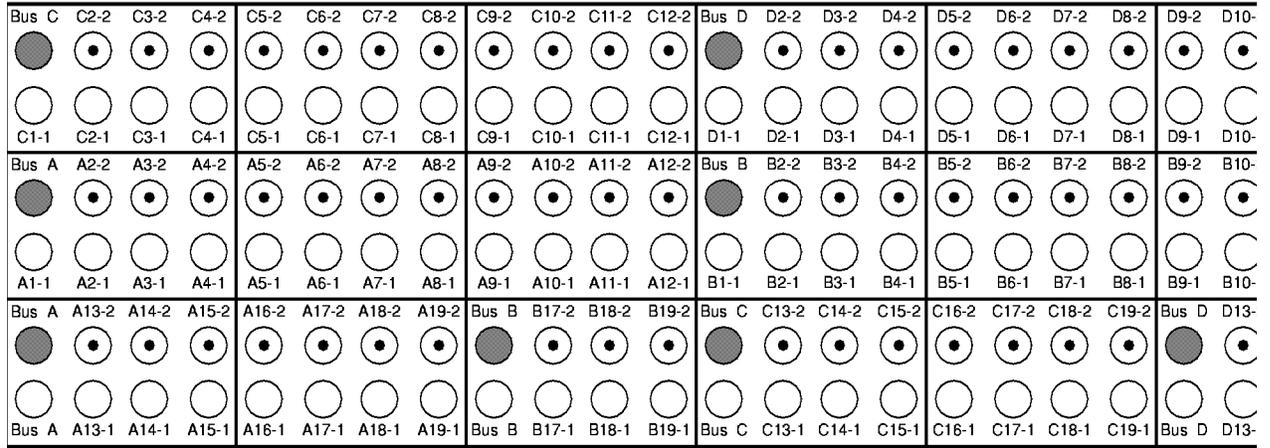
12	16	External Misc T/S			20	24
		Fuse & Alarm				
		Switch Power Module				
11	15	Sync Mod	RC Pwr Mod	Aux Pwr Mod	19	23
SWIO 13-16 N-Rate G/H (J16) J-7	SWIO 5-8 N-Rate C/D (J14) J-3	Redundant Controller Module			SWIO 21-24 N-Rate L/M (J30) J-19	SWIO 29-32 N-Rate R/T (J32) J-23
10	14	Switch Module			18	22
SWIO 9-12 N-Rate E/F (J15) J-6	SWIO 1-4 N-Rate A/B (J13) J-2				SWIO 17-20 N-Rate J/K (J29) J-18	SWIO 25-28 N-Rate N/P (J31) J-22
9	13	Fan Assembly			17	21
3	4	5	6	7		
Bay Position						

Note: The J-cable ID shown in parentheses indicate the control cable for the optional DS3PM circuit pack. In the above figure, it is assumed each DS3 Interface-32 Module contains a DS3PM circuit pack.

Figure 4: Physical Associations of Bays, Units, and Interbay Cables in a Maximum Configuration of STS1 Interface-16 Modules

12 SWIO 15/16 N-Rate H  J-8	16 SWIO 7/8 N-Rate D  J-4	External Misc T/S			20 SWIO 23/24 N-Rate M  J-20	24 SWIO 31/32 N-Rate T  J-24
		Fuse & Alarm				
		Switch Power Module				
11 SWIO 13/14 N-Rate G  J-7	15 SWIO 5/6 N-Rate C  J-3	Sync Mod	RC Pwr Mod	Aux Pwr Mod	19 SWIO 21/22 N-Rate L  J-19	23 SWIO 29/30 N-Rate R  J-23
		Redundant Controller Module				
10 SWIO 11/12 N-Rate F  J-6	14 SWIO 3/4 N-Rate B  J-2	Switch Module			18 SWIO 19/20 N-Rate K  J-18	22 SWIO 27/28 N-Rate P  J-22
9 SWIO 9/10 N-Rate E  J-5	13 SWIO 1/2 N-Rate A  J-1				17 SWIO 17/18 N-Rate J  J-17	21 SWIO 25/26 N-Rate N  J-21
3	4	5			6	7
Bay Position						

**Figure 5: Main Fuse Panel (on Alarm and Fuse Panel)**



Note: Fuses for power buses A, B, C, and D come in pairs with the load fuse labeled with -1 and the indicator fuse labeled with -2. Fuses for power bus E do not have dual fuses (one load and one indicator), they are all indicator fuses.



**Figure 7: Redundant Controller Power Module Fuses (FBF, FBG, FBH, and FBI)**

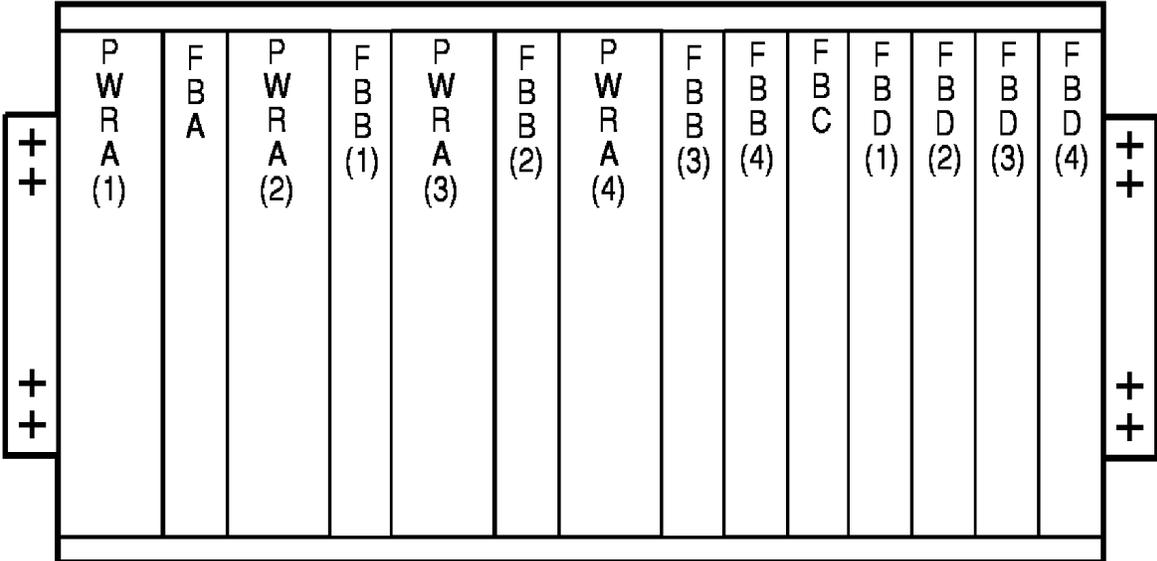
FBF	FBG	FBH	FBI
○ ALM	○ ALM	○ ALM	○ ALM
□ ECI (1) 5A	□ ECI (2) 5A	□ UI 5A	□ PWRPF (1) 7.5A
□ CPU (0) 5A	□ CPU (1) 5A	□ SCI (1) 5A	□ PWRG (1) 7.5A
□ MTC (0) 5A	□ MTC (1) 5A	□ SCI (2) 5A	□ SPRPF 2 0.5A
□ SSC (0) 5A	□ SSC (1) 5A	□ STPNL 2A	□ SYNCF 2A
□ PRI (1) 5A	□ PRI (2) 5A	□ SECC 5A	□ PWRPF (2) 7.5A
□ ECI (1) 1A	□ ECI (2) 1A	□ SECC 5A	□ PWRG (2) 7.5A
□ PRI (1) 5A	□ PRI (2) 5A	□ SPR 5A	□ SPRG 0.5A
□ ECI (1) 1A	□ ECI (2) 1A	□ SPR 5A	□ SYNCG 2A

**Notes:**

- Numbers in parentheses are circuit pack position numbers in the Redundant Controller Module. Fuse ratings are listed below the circuit pack identifier.
- The 7.5A fuses are the load fuses to the PWRF and PWRG power circuit packs.
- The 5A (2A for the Status Panel) fuses are the secondary fuses (or the +5V supply) to the circuit packs contained in the Redundant Controller Module.
- The 1A fuses associated with the ECI circuit packs are for +12V and -12V supplied to the CILINKs. When these fuses blow, communication with the CILINKs can be interrupted.
- The 5A fuses for the optical disk drive (SEC) is for the +5V and +12V supply.
- The 5A fuses for the hard disk drives (PRI) are for the +5V and +12V supply.
- The 2A fuses for SYNCF (TBS3-0) and SYNCG (TBS3-1) are for the -48V supply to the TBS3 circuit packs.
- The labels SPR, SPRF, and SPRG denote spare fuses that are not connected to any circuit pack.

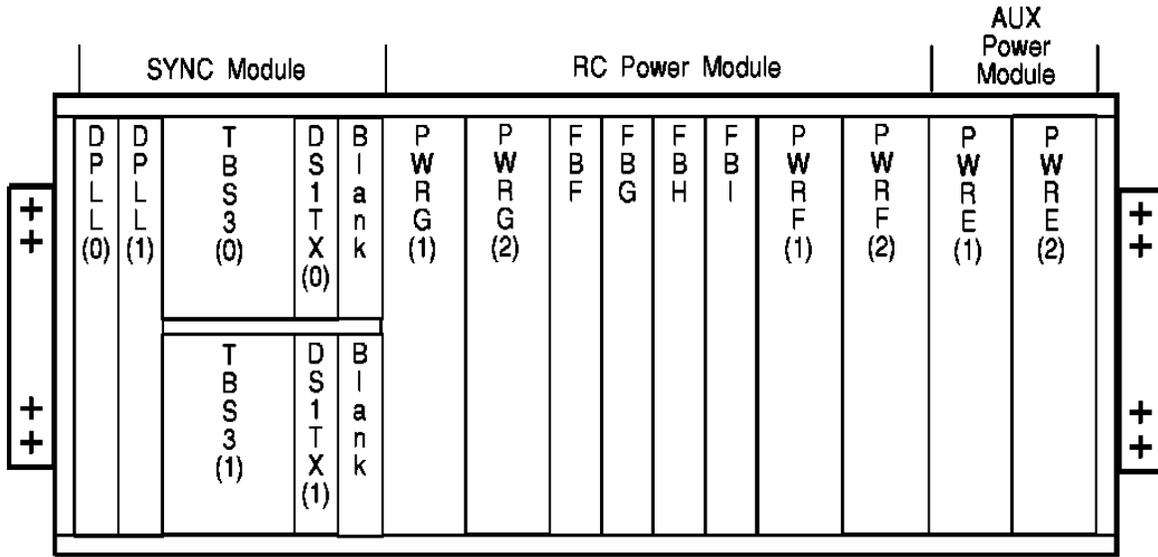


Figure 8: Switch Power Module



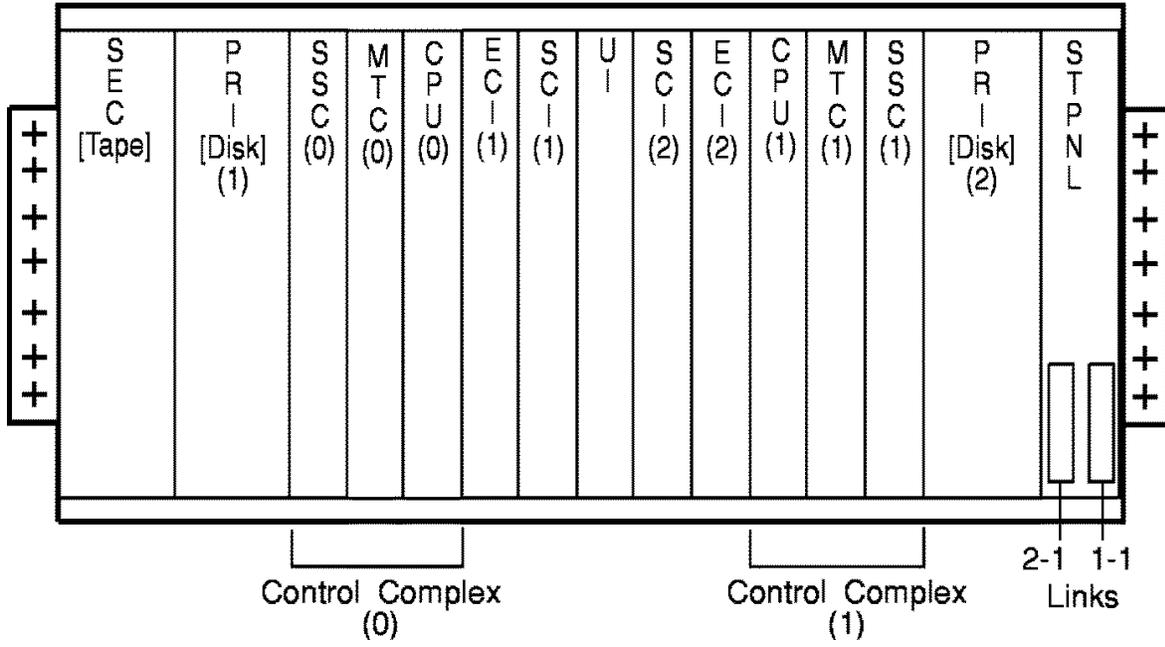
Note: Number in parentheses is circuit pack position number in module.

Figure 9: Auxiliary and Redundant Controller Power and Synchronizer Modules



Note: Number in parentheses is circuit pack position in module.

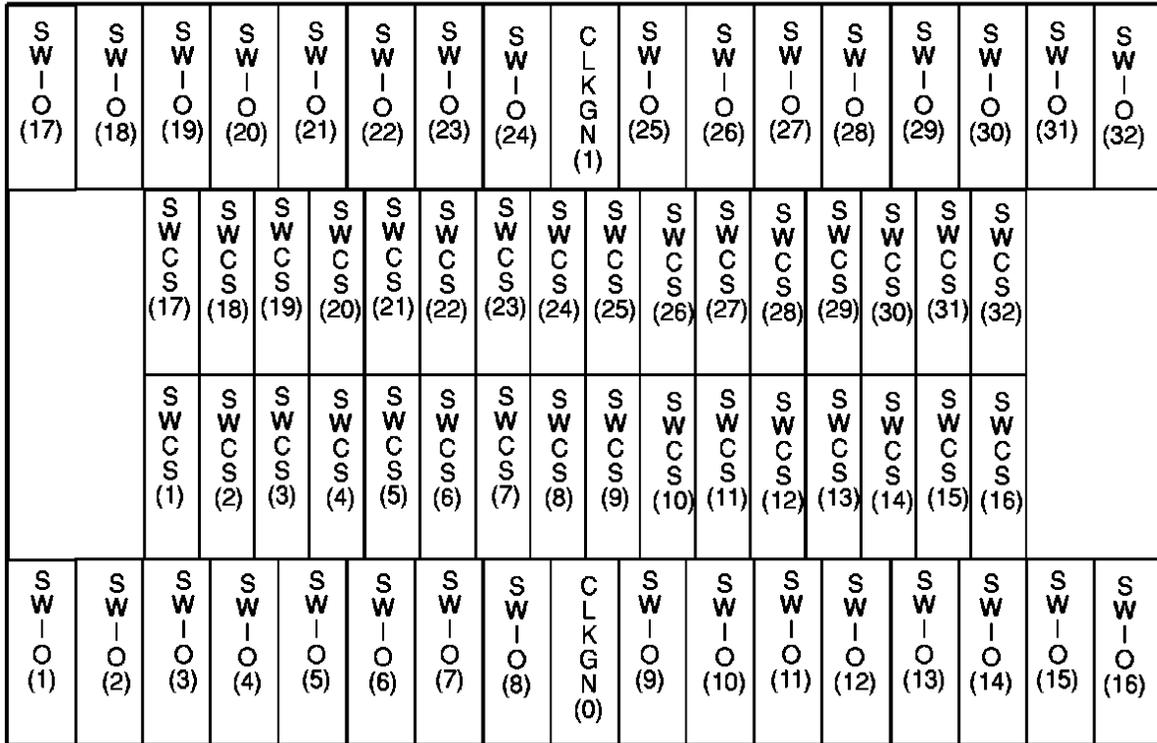
Figure 10: Redundant Controller Module



Note: Number in parentheses is circuit pack position in module.

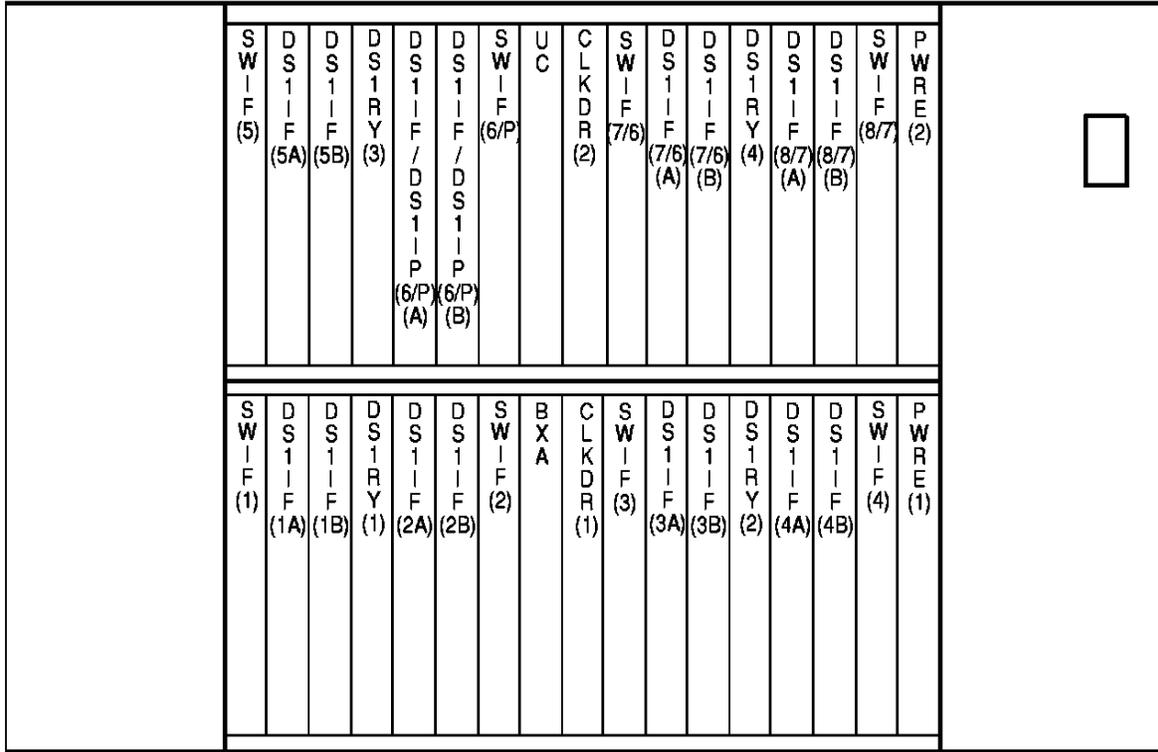
Figure 11: Switch Module

Front View



Note: Number in parentheses is circuit pack position in module.

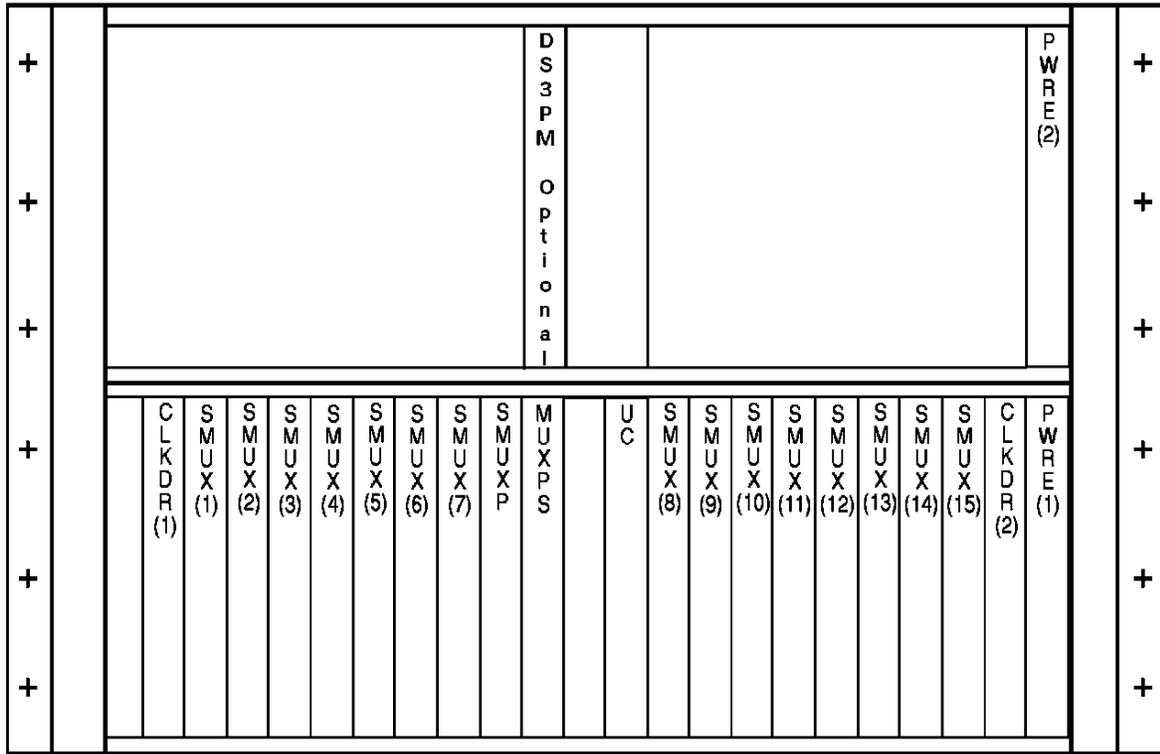
Figure 12: DS1 Interface/Interface-Protection Module



Note: Number in parentheses is circuit pack position number on module. For entries with slashes (/), the entry before the slash corresponds to the DS1 interface module and the entry after the slash corresponds to the DS1 interface-protection module.



Figure 14: DS3 Interface-16 Module



Notes:

Numbers in parentheses is circuit pack position number on module.

To implement DS1 performance monitoring features, one to fourteen MUX circuit packs are replaced with PMGR circuit packs. For more information on DS1 performance monitoring configurations, refer to the section titled "DS1 PM Hardware" later in this chapter.



Figure 16: DS1, DS3, STS-1, and VT1.5 Loopbacks

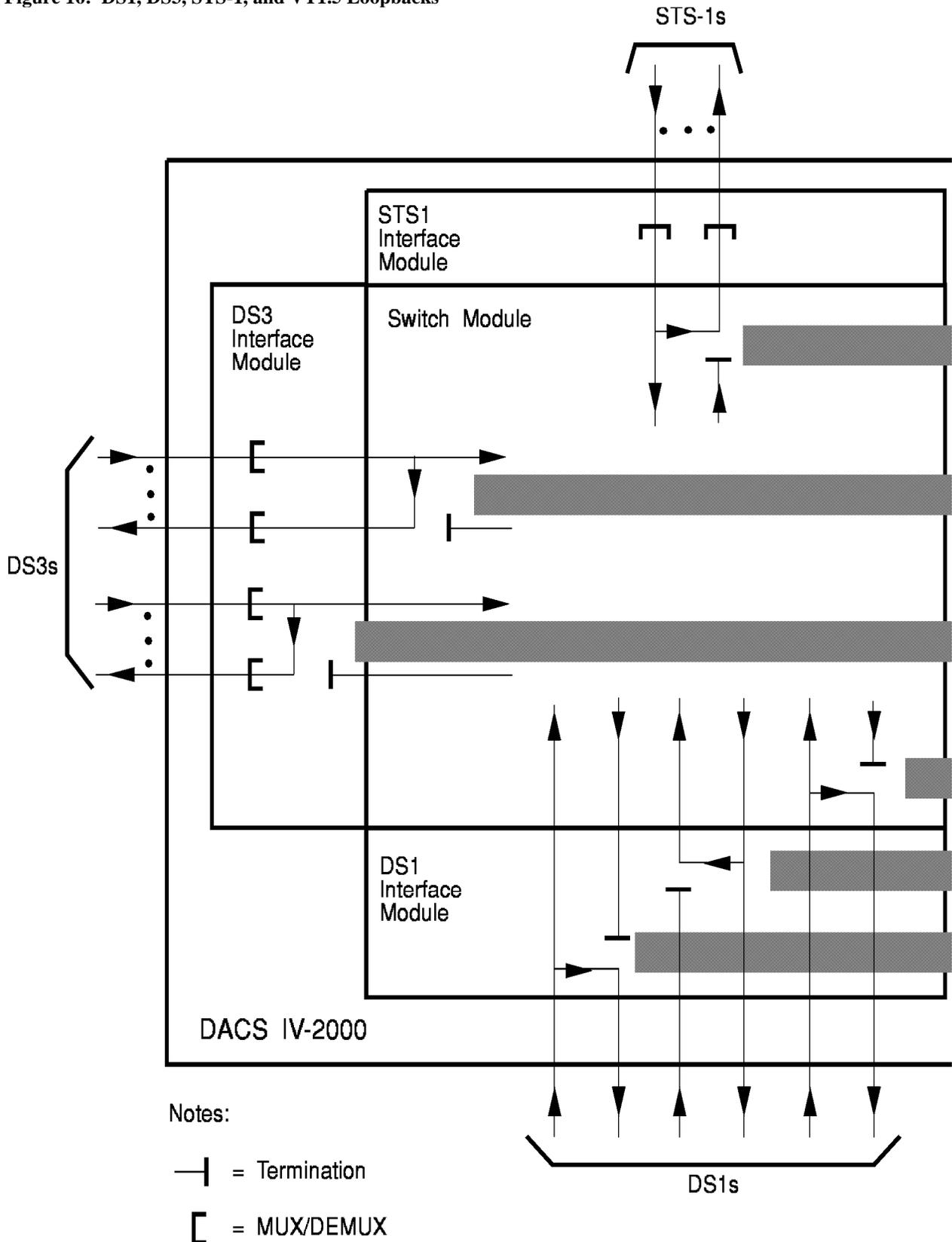




Figure 17: Test Access Conventions

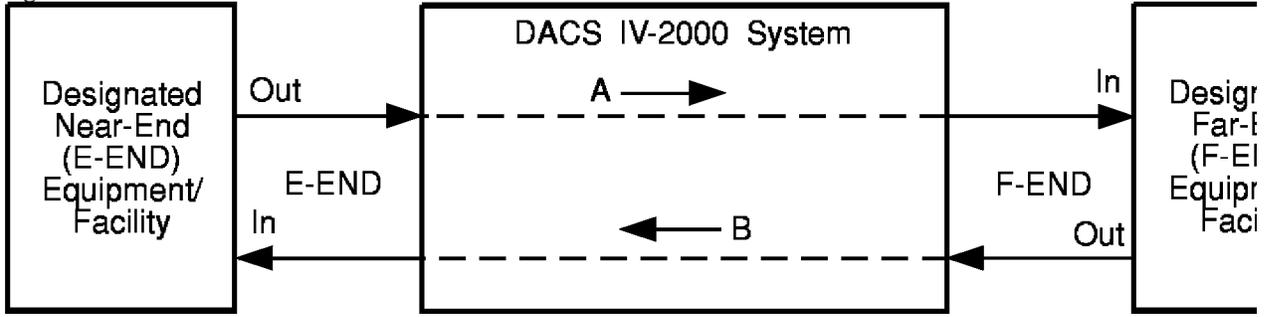


Figure 18: MONE Mode of Test Access

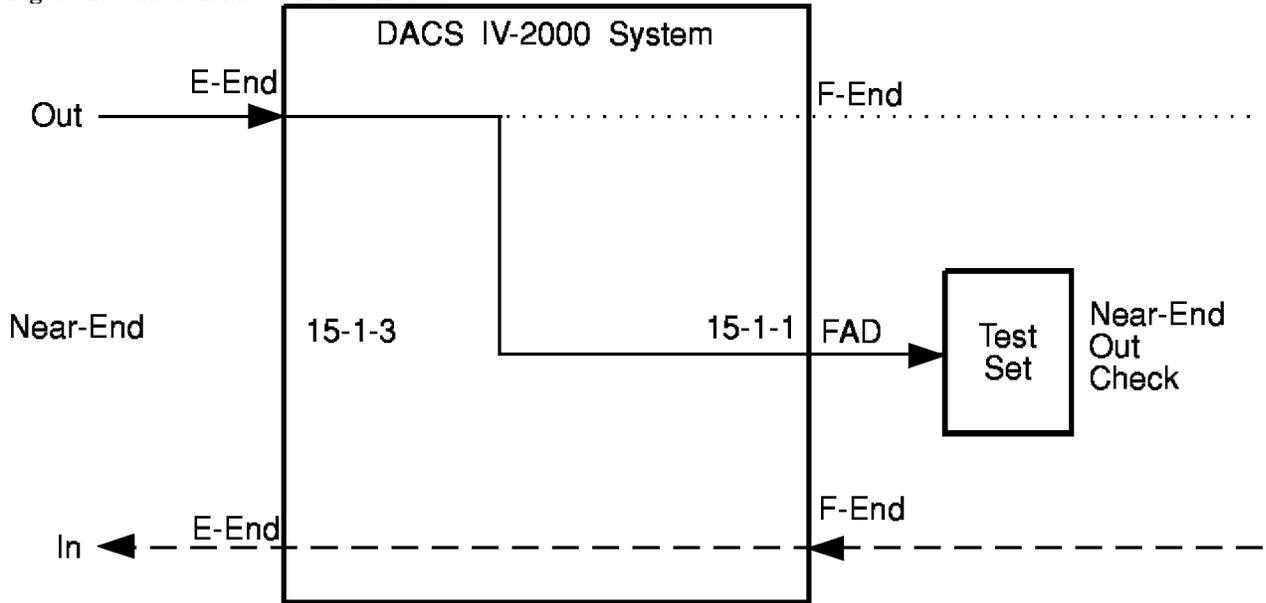


Figure 19: MONF Mode of Test Access

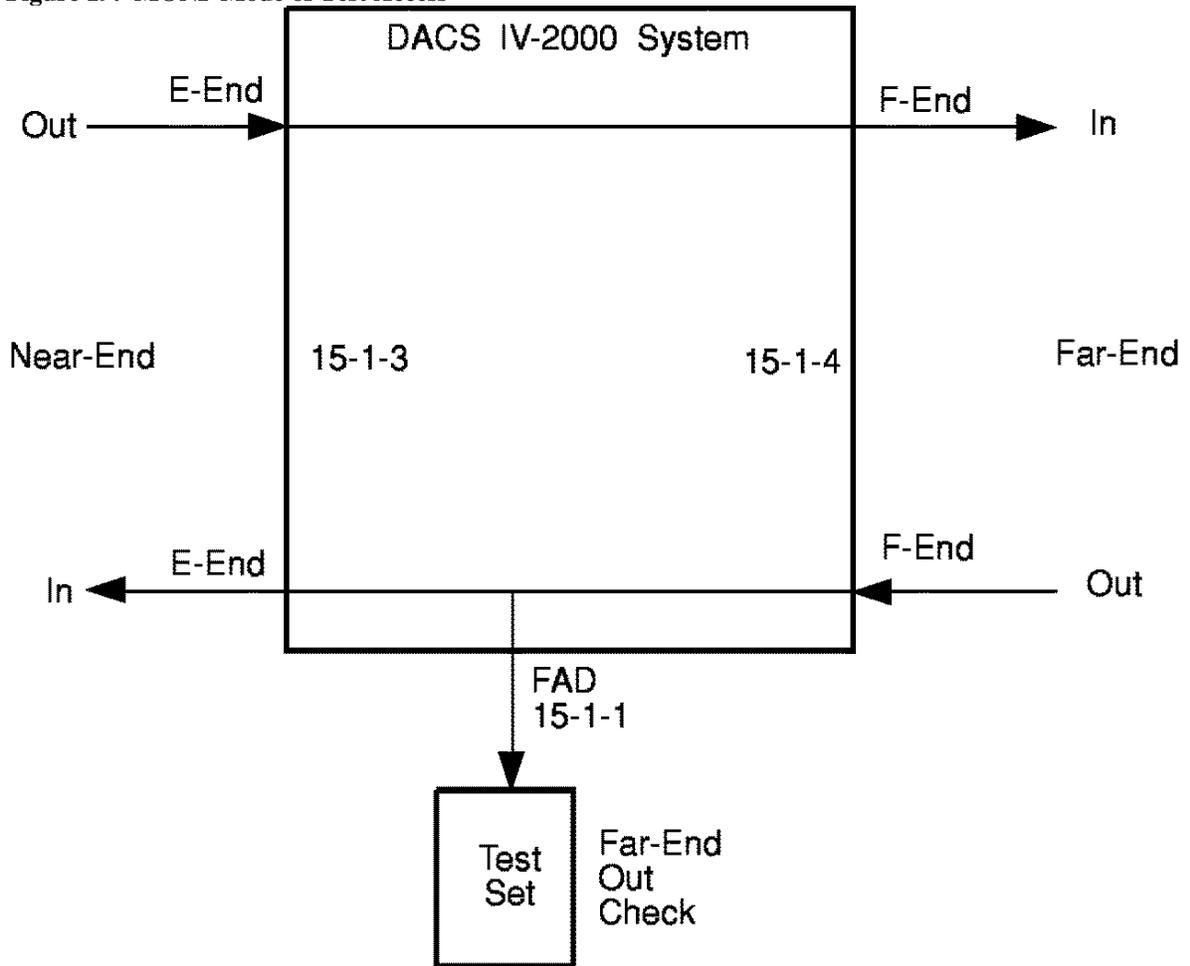


Figure 20: MONEF Mode of Test Access

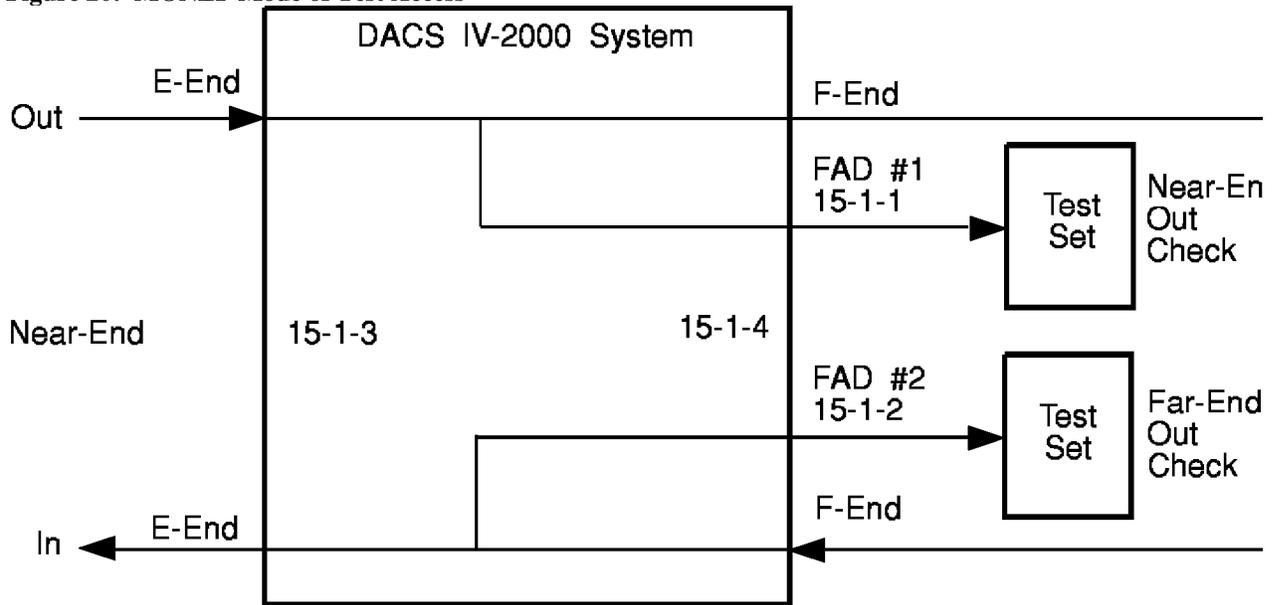


Figure 21: SPLTA Mode of Test Access

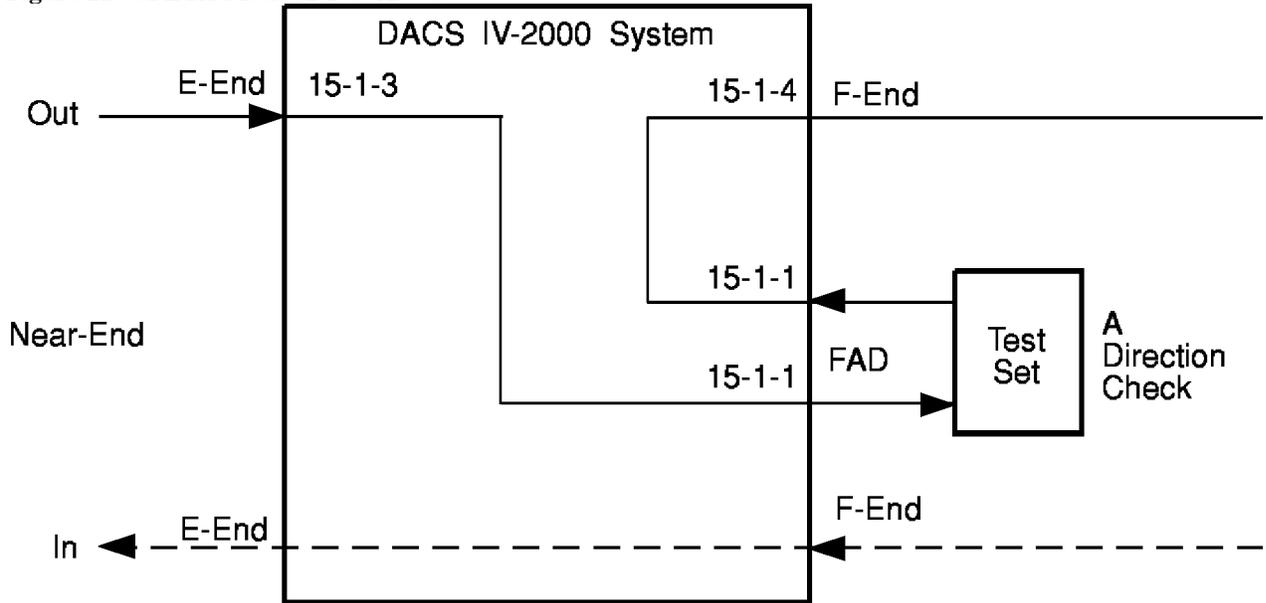


Figure 22: SPLTB Mode of Test Access

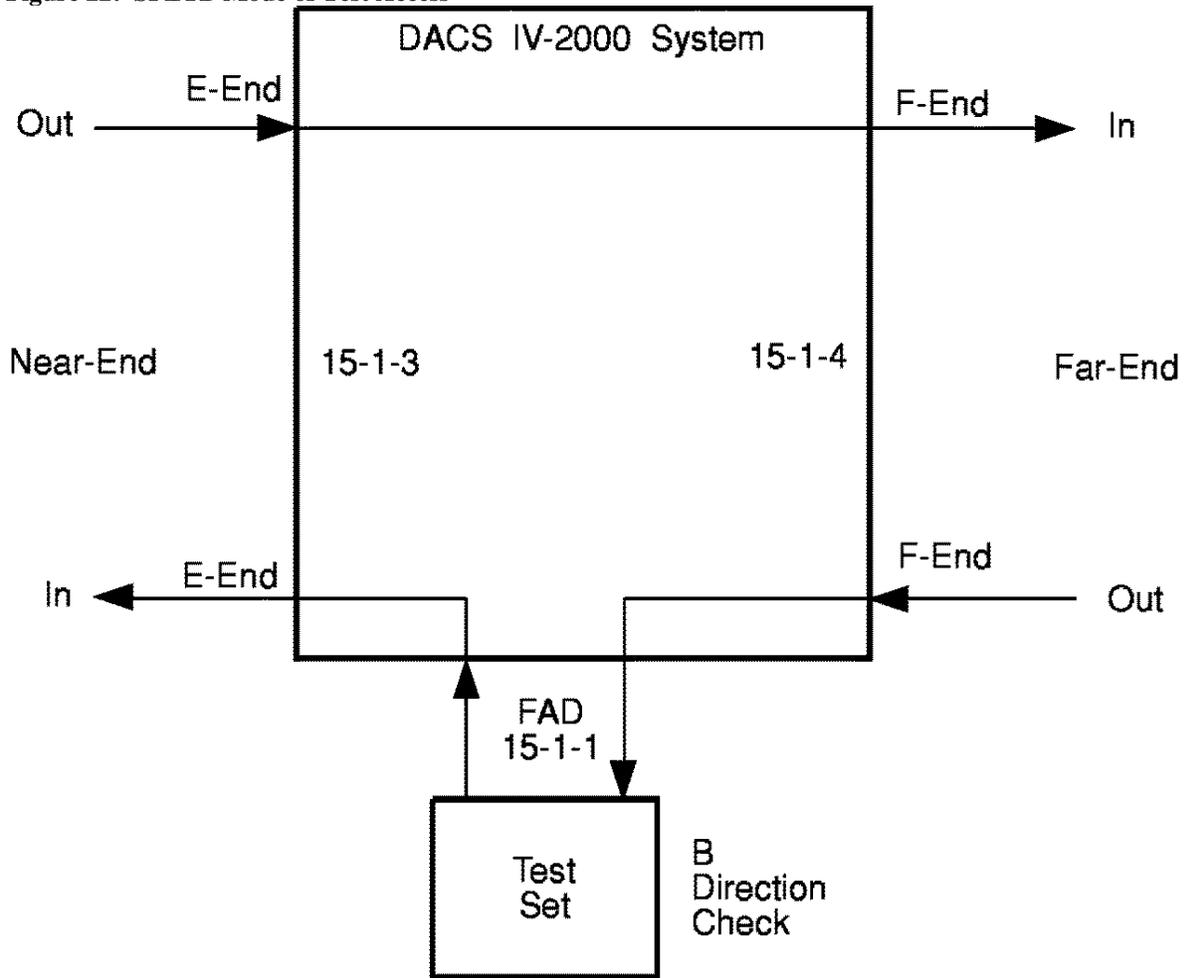


Figure 23: SPLTE Mode of Test Access

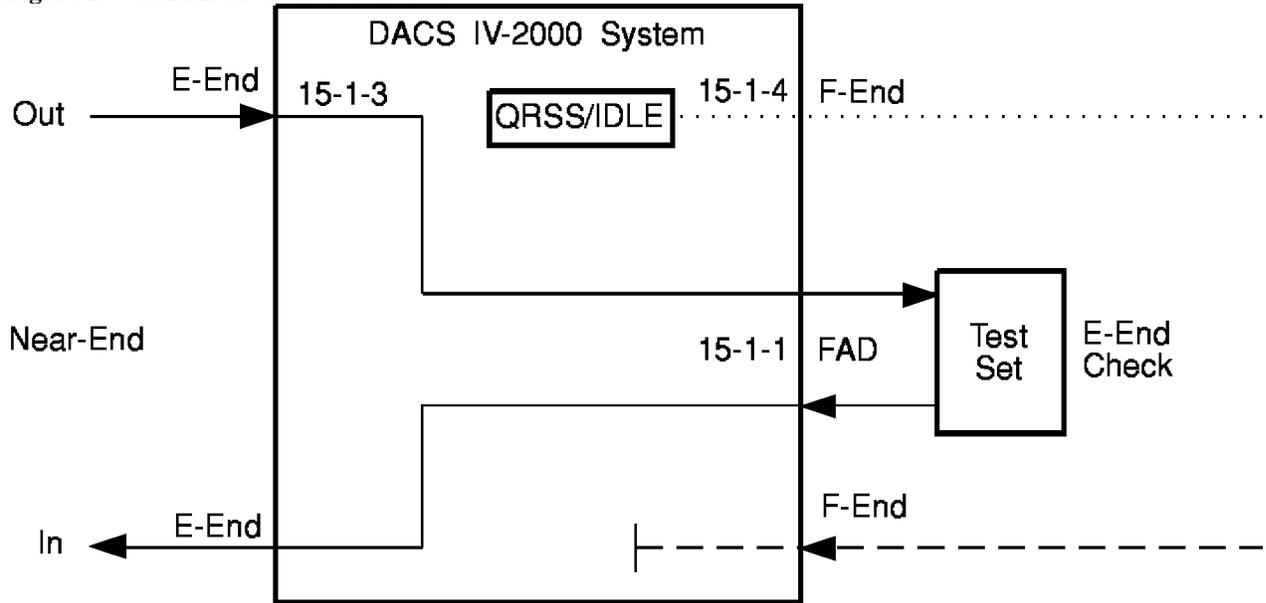


Figure 24: SPLTF Mode of Test Access

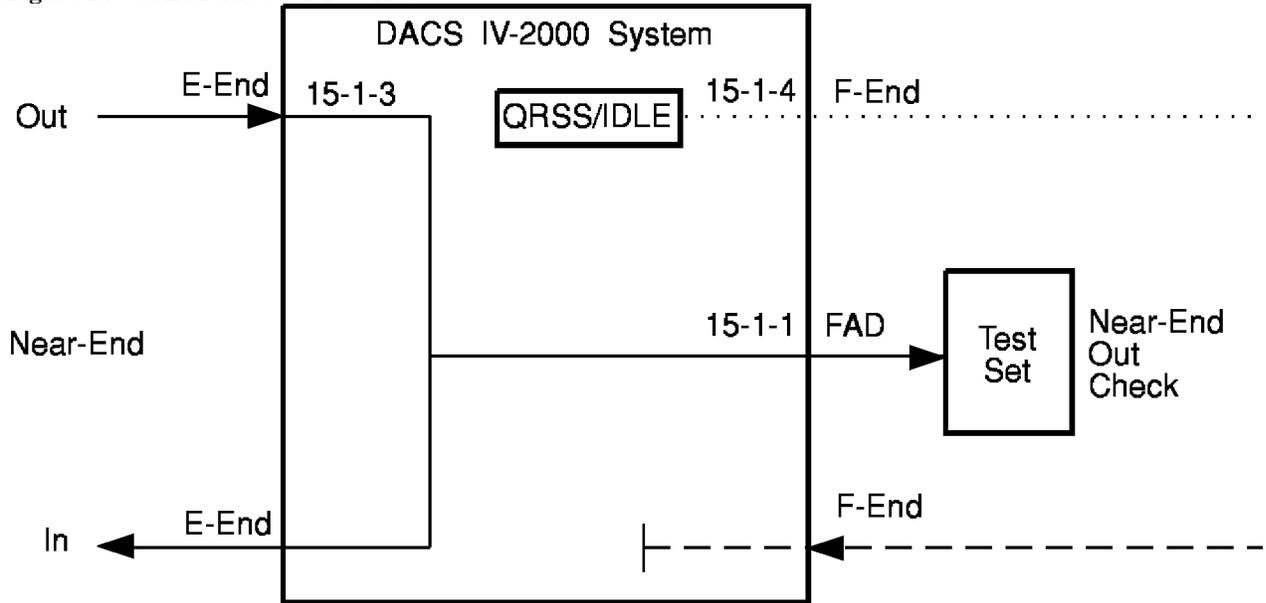


Figure 25: SPLTEF Mode of Test Access

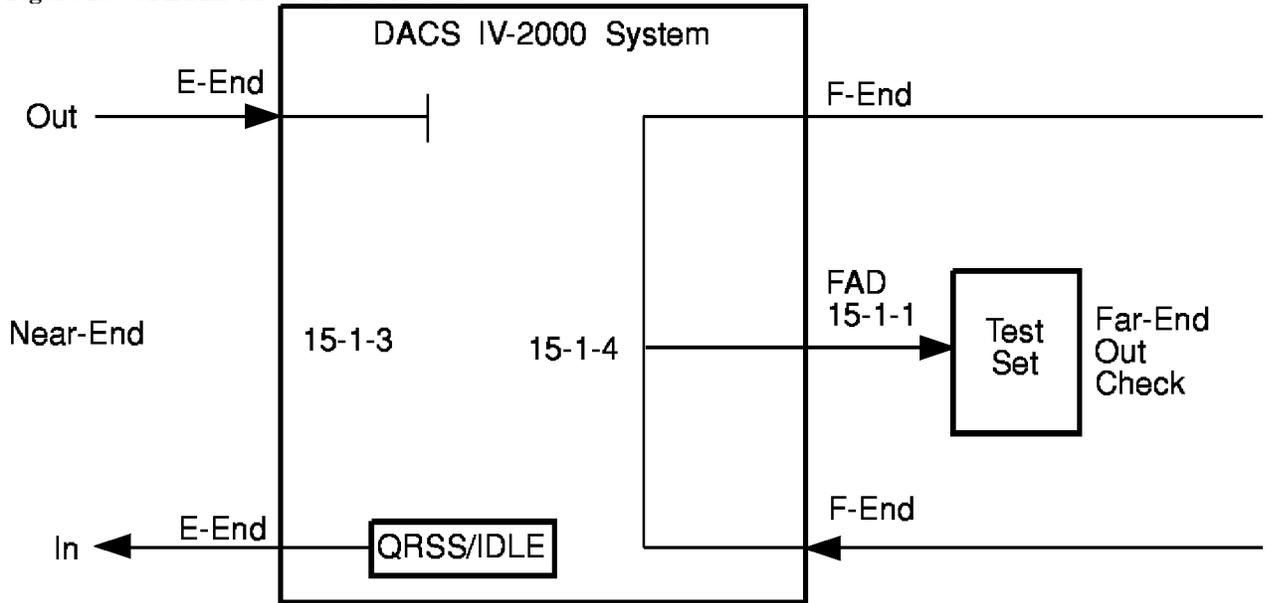


Figure 26: LOOPE Mode of Test Access

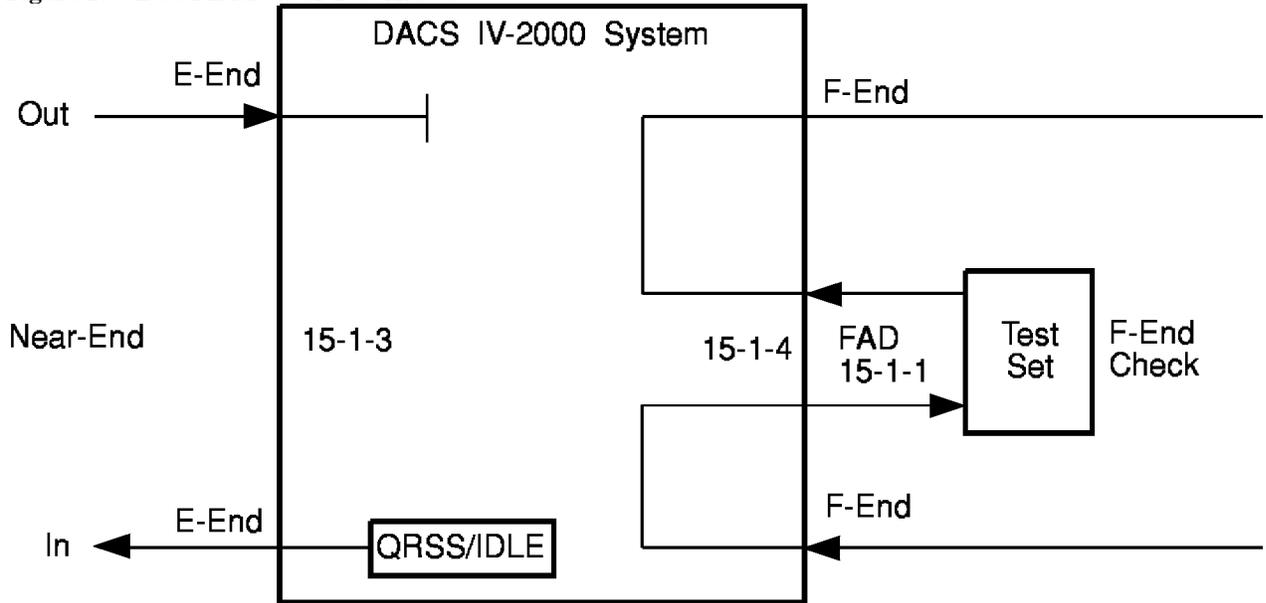


Figure 27: LOOPF Mode of Test Access

