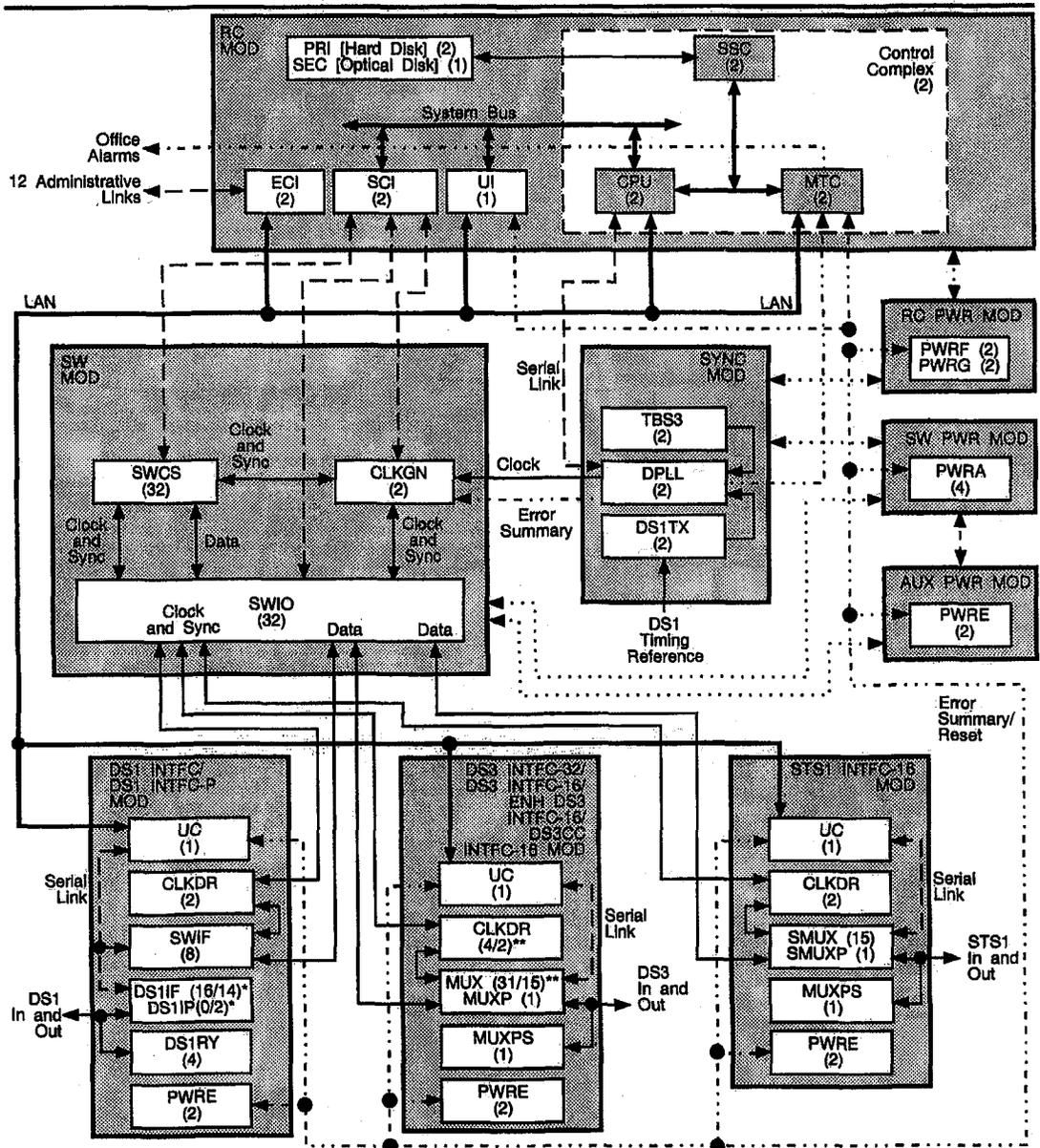# Functional Block Diagram

Notes:

Numbers in parentheses indicate the
quantity of the specified entity.

* X/Y (X = DS1 INTFC, Y = DS1 INTFC-P)

** X/Y (X = DS3 INTFC-32, Y = DS3 INTFC-16)

Legend:

——————— Transmission/Data
— — — — Control
············ Inter-Module Power
·· — ·· — Alarm/Reset/Error

Figure 1. **DACS IV-2000 (256) Release 5.0 Functional Block Diagram**

Unit Numbering

Figures 2, 3, and 4 illustrate the physical association of bays, units (the shelf positions of interface modules), and interbay cables in a fully-equipped system with all DS1 interfaces, DS3 interfaces, and STS-1 interfaces, respectively. For example, using Figure 2, look at Unit 11, located in the third column of the second row. The first label in Unit 11 is *SWIO 7*. This represents the Switch Input/Output (SWIO) circuit pack in the Switch Module that is associated with Unit 11. The designation *N-Rate D* indicates half of an N-rate cable (labeled *D*) that connects this interface module to the Switch Module. The number *9* indicates the DS1 Interface-Protection Module (located in Unit 9) responsible for providing protection for this interface module. Finally, the number *J-7* shows the control cable for this interface module in the bay lineup. Each unit shown in this sample configuration is labeled with the same information.

The unit numbers and control cable numbers shown in Figures 2, 3, and 4 are the same for any DACS IV-2000 configuration. The examples pictured are based on maximum configurations, but the same numbers are used for other configurations.

4 SWIO 16 N-Rate H 1 J-16	8 SWIO 12 N-Rate F 5 J-12	12 SWIO 8 N-Rate D 9 J-8	16 SWIO 4 N-Rate B 13 J-4	External Misc T/S			20 SWIO 20 N-Rate K 17 J-20	24 SWIO 24 N-Rate M 21 J-24	28 SWIO 28 N-Rate P 25 J-28	32 SWIO 32 N-Rate T 29 J-32
				Fuse & Alarm						
				Switch Power Module						
3 SWIO 15 N-Rate H 1 J-15	7 SWIO 11 N-Rate F 5 J-11	11 SWIO 7 N-Rate D 9 J-7	15 SWIO 3 N-Rate B 13 J-3	Sync Mod	RC Pwr Mod	Aux Pwr Mod	19 SWIO 19 N-Rate K 17 J-19	23 SWIO 23 N-Rate M 21 J-23	27 SWIO 27 N-Rate P 25 J-27	31 SWIO 31 N-Rate T 29 J-31
				Redundant Controller Module						
2 SWIO 14 N-Rate G 1 J-14	6 SWIO 10 N-Rate E 5 J-10	10 SWIO 6 N-Rate C 9 J-6	14 SWIO 2 N-Rate A 13 J-2	Switch Module			18 SWIO 18 N-Rate J 17 J-18	22 SWIO 22 N-Rate L 21 J-22	26 SWIO 26 N-Rate N 25 J-26	30 SWIO 30 N-Rate R 29 J-30
1 SWIO 13 N-Rate G J-13	5 SWIO 9 N-Rate E J-9	9 SWIO 5 N-Rate C J-5	13 SWIO 1 N-Rate A J-1	Fan Assembly			17 SWIO 17 N-Rate J J-17	21 SWIO 21 N-Rate L J-21	25 SWIO 25 N-Rate N J-25	29 SWIO 29 N-Rate R J-29
1	2	3	4	5			6	7	8	9

Bay Position

Note: Units 1, 5, 9, 13, 17, 21, 25, and 29 are all DS1 Interface-Protection Modules. All other units are DS1 Interface Modules.

Figure 2. **Physical Associations of Bays, Units, and Interbay Cables in a Maximum Configuration of DS1 Interface Modules**

12	16	External Misc T/S			20	24
		Fuse & Alarm				
		Switch Power Module				
11 SWIO 13-16 N-Rate G/H J-7	15 SWIO 5-8 N-Rate C/D J-3	Sync Mod	RC Pwr Mod	Aux Pwr Mod	19 SWIO 21-24 N-Rate L/M J-19	23 SWIO 29-32 N-Rate R/T J-23
		Redundant Controller Module				
10 SWIO 9-12 N-Rate E/F J-6	14 SWIO 1-4 N-Rate A/B J-2	Switch Module			18 SWIO 17-20 N-Rate J/K J-18	22 SWIO 25-28 N-Rate N/P J-22
9	13				17	21
		Fan Assembly				

3　　　4　　　　5　　　　6　　　7

Bay Position

Figure 3. Physical Associations of Bays, Units, and Interbay Cables in a
Maximum Configuration of DS3 Interface-32 Modules

12 SWIO 15/16 N-Rate H J-8	16 SWIO 7/8 N-Rate D J-4	External Misc T/S			20 SWIO 23/24 N-Rate M J-20	24 SWIO 31/32 N-Rate T J-24
		Fuse & Alarm				
		Switch Power Module				
11 SWIO 13/14 N-Rate G J-7	15 SWIO 5/6 N-Rate C J-3	Sync Mod	RC Pwr Mod	Aux Pwr Mod	19 SWIO 21/22 N-Rate L J-19	23 SWIO 29/30 N-Rate R J-23
		Redundant Controller Module				
10 SWIO 11/12 N-Rate F J-6	14 SWIO 3/4 N-Rate B J-2	Switch Module			18 SWIO 19/20 N-Rate K J-18	22 SWIO 27/28 N-Rate P J-22
9 SWIO 9/10 N-Rate E J-5	13 SWIO 1/2 N-Rate A J-1	Fan Assembly			17 SWIO 17/18 N-Rate J J-17	21 SWIO 25/26 N-Rate N J-21

3　　　4　　　　5　　　　6　　　7

Bay Position

Figure 4. Physical Associations of Bays, Units, and Interbay Cables in a
Maximum Configuration of STS1 Interface-16 Modules

Commands and Messages

Command	Command	Command	Command
ABT-CMD	ED-PORT	OPR-LPBK-EC1	RTRV-DROPCRS-T1
ACT-ECHO-LINK	ED-PRMTR-LINK	OPR-LPBK-T1	RTRV-DROPCRS-T3
ACT-USER	ED-SECU-LINK	OPR-LPBK-T3	RTRV-DROPCRS-VT1
ALW-LPBK-EC1	ED-SECU-PID	OPR-LPBK-VT1	RTRV-EC1
ALW-LPBK-T1	ED-SECU-USER	RLS-LPBK-EC1	RTRV-ECHO-LINK
ALW-LPBK-T3	ED-STATE-EQPT	RLS-LPBK-T1	RTRV-EQPT
ALW-LPBK-VT1	ED-T1	RLS-LPBK-T3	RTRV-FWID
ALW-MSG-EC1	ED-T3	RLS-LPBK-VT1	RTRV-HDR
ALW-MSG-VT1	ED-VT1	RLS-TSTPT-EC1	RTRV-LPBK-EC1
ALW-PMREPT-EC1	ENT-AUTOCMPN-T1	RLS-TSTPT-T1	RTRV-LPBK-T1
ALW-PMREPT-T1	ENT-CONF-STS1	RLS-TSTPT-T3	RTRV-LPBK-T3
ALW-PMREPT-T3	ENT-CONF-T1	RLS-TSTPT-VT1	RTRV-LPBK-VT1
ALW-PMREPT-VT1	ENT-CONF-T3	RMV-EQPT	RTRV-MSG-EC1
ALW-SW-EQPT	ENT-CONF-VT1	RMV-LINK	RTRV-MSG-VT1
CANC-ECHO-LINK	ENT-CRS-STS1	RST-EQPT	RTRV-NE
CANC-USER	ENT-CRS-T1	RST-LINK	RTRV-PATH-STS1
CHG-ACCMD-EC1	ENT-CRS-T3	RTRV-ALM-ALL	RTRV-PATH-T1
CHG-ACCMD-T1	ENT-CRS-VT1	RTRV-ALM-COM	RTRV-PATH-T3
CHG-ACCMD-T3	ENT-EQPT	RTRV-ALM-EC1	RTRV-PATH-VT1
CHG-ACMD-VT1	ENT-FAN-FILTER	RTRV-ALM-EQPT	RTRV-PM-EC1
CHG-TACC-EC1	ENT-ROLL-STS1	RTRV-ALM-LINK	RTRV-PM-T1
CHG-TACC-T1	ENT-ROLL-T1	RTRV-ALM-T1	RTRV-PM-T3
CHG-TACC-T3	ENT-ROLL-T3	RTRV-ALM-T2	RTRV-PM-VT1
CHG-TACC-VT1	ENT-ROLL-VT1	RTRV-ALM-T3	RTRV-PMCNFGRN-T1
CONN-PM-T1	ENT-SECU-USER	RTRV-ALM-VT1	RTRV-PMMODE-EC1
CONN-TACC-EC1	ENT-TSTPT-EC1	RTRV-ATTR-EC1	RTRV-PMMODE-VT1
CONN-TACC-T1	ENT-TSTPT-T1	RTRV-ATTR-EQPT	RTRV-PMSCHED-EC1
CONN-TACC-T3	ENT-TSTPT-T3	RTRV-ATTR-T1	RTRV-PMSCHED-T1
CONN-TACC-VT1	ENT-TSTPT-VT1	RTRV-ATTR-T2	RTRV-PMSCHED-T3
CPY-MEM	EX-EQPT	RTRV-ATTR-T3	RTRV-PMSCHED-VT1
CPY-TH-T1	INH-LPBK-EC1	RTRV-ATTR-VT1	RTRV-PORT
DGN-DET-EQPT	INH-LPBK-T1	RTRV-CMD-STAT	RTRV-PRMTR-LINK
DISC-PM-T1	INH-LPBK-T3	RTRV-COND-EC1	RTRV-PRMTR-SFTWR
DISC-TACC	INH-LPBK-VT1	RTRV-COND-EQPT	RTRV-SCANTH-NE
DLT-CONF-STS1	INH-MSG-EC1	RTRV-COND-LINK	RTRV-SECU-AUD
DLT-CONF-T1	INH-MSG-VT1	RTRV-COND-T1	RTRV-SECU-LINK
DLT-CONF-T3	INH-PMREPT-EC1	RTRV-COND-T2	RTRV-SECU-USER
DLT-CONF-VT1	INH-PMREPT-T1	RTRV-COND-T3	RTRV-STATE-EC1
DLT-CRS-STS1	INH-PMREPT-T3	RTRV-COND-VT1	RTRV-STATE-EQPT
DLT-CRS-T1	INH-PMREPT-VT1	RTRV-CONF-STS1	RTRV-STATE-T1
DLT-CRS-T3	INH-SW-EQPT	RTRV-CONF-T1	RTRV-STATE-T3
DLT-CRS-VT1	INIT-REG-EC1	RTRV-CONF-T3	RTRV-STATE-VT1
DLT-EQPT	INIT-REG-T1	RTRV-CONF-VT1	RTRV-SYNCN
DLT-SECU-AUD	INIT-REG-T3	RTRV-CRS	RTRV-SYSID
DLT-SECU-USER	INIT-REG-VT1	RTRV-CRS-STS1	RTRV-T1
ED-DATE	INIT-SYS	RTRV-CRS-T1	RTRV-T3
ED-EC1	LGN-USER	RTRV-CRS-T3	RTRV-TACC-EC1
ED-EQPT	LGT-USER	RTRV-CRS-VT1	RTRV-TACC-T1
ED-NE	OPR-ACO-ALL	RTRV-DROPCRS-STS1	RTRV-TACC-T3

Table continued on next page.

Command	Command	Autonomous Message	Autonomous Message
RTRV-TACC-VT1	SET-PMMODE-EC1	REPT ALM COM	REPT EVT EC1
RTRV-TH-EC1	SET-PMMODE-VT1	REPT ALM EC1	REPT EVT T1
RTRV-TH-NE	SET-SCANTH-NE	REPT ALM EQPT	REPT EVT T3
RTRV-TH-T1	SET-SID	REPT ALM LINK	REPT EVT VT1
RTRV-TH-T3	SET-TH-EC1	REPT ALM T1	REPT EXCPTN SYS
RTRV-TH-VT1	SET-TH-NE	REPT ALM T2	REPT FAN FILTER
RTRV-VT1	SET-TH-T1	REPT ALM T3	REPT LOCL IN
SCHED-PMREPT-EC1	SET-TH-T3 SET-TH-VT1	REPT ALM VT1	REPT PM EC1
SCHED-PMREPT-T1	STA-SCANPM-T1	REPT BKUP	REPT PM T1
SCHED-PMREPT-T3	STP-SCANPM-T1	REPT CMPR MEM	REPT PM T3
SCHED-PMREPT-VT1	SW-DX-EQPT	REPT DBCHG	REPT PM VT1
SET-ATTR-EC1	SW-TOPROTN-EQPT	REPT DGNDET EQPT	REPT RMV EQPT
SET-ATTR-EQPT	SW-TOWKG-EQPT	REPT DISC TACC	REPT RMV LINK
SET-ATTR-T1	TEST-CABLE	REPT DLTCRS STS1	REPT RST EQPT
SET-ATTR-T2	TEST-SW-CONTROL	REPT DLTCRS T1	REPT RST LINK
SET-ATTR-T3	TEST-TRMSN-T1	REPT DLTCRS T3	REPT RSTCRS STS1
SET-ATTR-VT1	TEST-UNIT-CABLE	REPT DLTCRS VT1	REPT RSTCRS T1
		REPT DROPCRS STS1	REPT RSTCRS T3
		REPT DROPCRS T3	REPT RSTCRS VT1
		REPT DROPCRS T1	REPT SW
		REPT DROPCRS VT1	REPT TRMSN T1

Facility Address (EID)

STS-1 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{port number} (Unit-STS-1 Port) for the STS-1 ports must be addressed as follows:

■ Individually or as a range:
   For STS1 Interface-16 Modules, only: [1-32]-[1-15]

■ As all ports in an STS1 Interface Module: UNIT-[1-32]

DS3 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{port number} (Unit-DS3 Port) for the DS3 ports must be addressed as follows:

■ Individually or as a range:
   For DS3 Interface-32 Modules, only: [1-32]-[1-31]
   For DS3 Interface-16 Modules, only: [1-32]-[1-15]

■ As all ports in an DS3 Interface Module: UNIT-[1-32]

DS1 and VT1.5 Mappings

Asynchronous DACS IV-2000 to DDM-1000		Synchronous			
		DACS IV-2000		DDM-2000	
DS1 Within DS3	DS2, DS1	VT1.5 Within STS-1	VT Group, VT	VT Group, VT	VT1.5 Within STS-1
1	1,1	1	1,1	1,1	1
2	1,2	2	2,1	1,2	8
3	1,3	3	3,1	1,3	15
4	1,4	4	4,1	1,4	22
5	2,1	5	5,1	2,1	2
6	2,2	6	6,1	2,2	9
7	2,3	7	7,1	2,3	16
8	2,4	8	1,2	2,4	23
9	3,1	9	2,2	3,1	3
10	3,2	10	3,2	3,2	10
11	3,3	11	4,2	3,3	17
12	3,4	12	5,2	3,4	24
13	4,1	13	6,2	4,1	4
14	4,2	14	7,2	4,2	11
15	4,3	15	1,3	4,3	18
16	4,4	16	2,3	4,4	25
17	5,1	17	3,3	5,1	5
18	5,2	18	4,3	5,2	12
19	5,3	19	5,3	5,3	19
20	5,4	20	6,3	5,4	26
21	6,1	21	7,3	6,1	6
22	6,2	22	1,4	6,2	13
23	6,3	23	2,4	6,3	20
24	6,4	24	3,4	6,4	27
25	7,1	25	4,4	7,1	7
26	7,2	26	5,4	7,2	14
27	7,3	27	6,4	7,3	21
28	7,4	28	7,4	7,4	28

For more information on DS1 and VT1.5 mappings, refer to the "Cross Connections" section in Chapter 2 of the *DACS IV-2000 (256) Release 4.0 Reference Manual* (AT&T 365-340-700).

VT1.5 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{slot number}-{port number} (Unit-STS-1 Equivalent-VT1.5 Port) for VT1.5 port numbering or {unit number}-{slot number}-{group number}-{port number} for VT1.5 group numbering must be addressed as follows:

- Individually or as a range:
  For STS1 Interface-16 Modules, only:
  VT1.5 port number: {1-32}-{1-15}-{1-28}
  VT1.5 group number: {1-32}-{1-15}-{1-7}-{1-4}

- As an individual or a range of VT1GRPs (group of 28 VT1.5 tributaries):
  For STS1 Interface-16 Modules, only:
  VT1.5 port number (only): VT1GRP-{1-32}-{1-15}

- As all ports in an STS1 Interface Module: UNIT-{1-32}

DS1 Ports

The port EID (Equipment Identification) code, expressed as: {unit number}-{slot number}-{port number} (Unit-DS3 Equivalent-DS1 Port) for the DS1 ports must be addressed as follows:

- Individually or as a range:
  For STS1 Interface-16 Modules:
  DS1 port number: {1-32}-{1-15}-{1-28}
  VT1.5 group number: {1-32}-{1-15}-{1-7}-{1-4}

  For DS3 Interface-32 Modules: {1-32}-{1-31}-{1-28}
  For DS3 Interface-16 Modules: {1-32}-{1-15}-{1-28}

  For DS1 Interface Modules: {1-32}-{1-8}-{1-28}
  For DS1 Interface-P Modules: {1-32}-{1-7}-{1-28}

- As an individual or a range of DS1GRPs (group of 28 DS1 ports functioning as a DS3 equivalent):
  For STS1 Interface-16 Modules:
  DS1 port number (only): DS1GRP-{1-32}-{1-15}

  For DS3 Interface-32 Modules: DS1GRP-{1-32}-{1-31}
  For DS3 Interface-16 Modules: DS1GRP-{1-32}-{1-15}

  For DS1 Interface Modules: DS1GRP-{1-32}-{1-8}
  For DS1 Interface-P Modules: DS1GRP-{1-32}-{1-7}

- As all ports in an interface module: UNIT-{1-32}

Allowable Commands for Various Main Controller States

Most system functions are not allowed when the main controller (MC) is not in service. Certain functions, however, either can be performed with the MC out of service, or require the MC to be out of service to be performed. The following lists the allowable commands for the given state of the MC:

- **OOS-FLT state:**
  ABT-CMD
  DGN-DET-EQPT (on MC, and MC subentities* in the IS state)
  INIT-SYS (Initialization Level 9)
  RTRV-CMD-STAT
  RTRV-PRMTR-SFTWR
  RTRV-STATE-EQPT (on MC)
  RST-EQPT (on MC)

- **OOS-MTCE state:**
  ABT-CMD
  DGN-DET-EQPT (on MC, and MC subentities* in the IS state)
  ED-EQPT (on MC, and MC subentities[†] in the IS state)
  INIT-SYS (Initialization Level 9)
  RTRV-CMD-STAT
  RTRV-PRMTR-SFTWR
  RTRV-STATE-EQPT (on the MC)
  RST-EQPT (on the MC, PRI, and SEC)
  RMV-EQPT (on SEC)
  CPY-MEM[‡]

- **OOS-MCOND state:**
  ABT-CMD
  DGN-DET-EQPT (on MC, and MC subentities* in the IS state)
  ED-EQPT (on MC, and MC subentities[†] in the IS state)
  INIT-SYS (Initialization Level 9)
  RTRV-CMD-STAT
  RTRV-PRMTR-SFTWR
  RTRV-STATE-EQPT (on the MC)
  RST-EQPT (on the MC, PRI, and SEC)
  RMV-EQPT (on the PRI and SEC)
  RTRV-SYSID
  CPY-MEM[‡]
  SET-SID

- **IS state** the following commands are **not** allowed:
  RMV-EQPT (on the only in-service PRI)
  CPY-MEM[‡]

---

* MC subentities include: CPU-0, CPU-1, UI, MTC-0, MTC-1, SSC-0, SSC-1, PRI-1, PRI-2, SEC, ECI-1, ECI-2, SCI-1, SCI-2, CC-0, and CC-1
† MC subentities include: MTC-0, MTC-1, SSC-0, SSC-1, PRI-1, PRI-2, SEC
‡ See CPY-MEM command entry in the *DACS IV-2000 (256) Release 5.0 Commands and Messages* manual (AT&T 365-340-802) for details.

Error Codes

| Error Code	Error Condition	Error Code	Error Condition
EHNS	Equipment hierarchy not satisfied	SAIN	Status, already inhibited
ENEQ	Equipage, not equipped	SAIS	Status, already in-service
ENMB	Equipage, not a multipoint bridge	SAOP	Status, already operated
ENMD	Equipage, no media present	SAOS	Status, already out-of-service
ENRD	Equipage, not red-lined	SAPS	Status, already in protection state
ENRE	Equipage, not recognized equipage	SAPV	Status, already provisioned
ENRI	Equipage, not equipped for retrieving specified information	SARB	Status, all resources busy
		SARL	Status, already released
ERLC	Equipage, a red-lined circuit	SASW	Status, already in switched state
IBEX	Input, extra block	SAWS	Status, already in working state
IBNC	Input, block not consistent	SCAT	Status, circuit is already connected to another TAP
IDMS	Input, data missing		
IDNC	Input, data not consistent	SCCF	Status, SEC cartridge checksum failure
IDNV	Input, data not valid	SDNC	Status, data in input message is not consistent with the provisioned object entity
IDRG	Input, data, range error		
IICT	Input, invalid CTAG	SEIP	Status, entity is protected
IISP	Input, invalid syntax or punctuation	SIOM	Status, invalid output mode
IITA	Input, invalid target identifier (TID)	SMVF	Status, media validation failed
IPAI	Input, port address inconsistent	SNAS	Status, not assigned
ISCH	Input, syntax character error in input command	SNCC	Status, not cross-connected
		SNDA	Status, no data available
ISPC	Input, syntax punctuation error in input command	SNDB	Status, no database on the device
		SNIS	Status, not in-service
MRAS	Maximum reports already scheduled	SNML	Status, no monitor line established
PICC	Privilege, illegal command code	SNOS	Status, not out-of-service
PIOC	Privilege, illegal operations channel	SNPV	Status, not provisioned
PIPW	Privilege, illegal password/user id code	SNST	Status, execution could not be started
PIRC	Privilege, illegal record control	SNVS	Status, not in valid state
PIUI	Privilege, illegal user identity	SOSF	Status, out-of-service, failed
PKOR	Pack out of range	SOST	Status, out-of-service, testing
PLNA	Privilege, login not active	SPFA	Status, protection entity failed
SAAL	Status, already allowed	SRIP	Status, request inconsistent with provisioning
SAAS	Status, already assigned		
SABT	Status, execution stopped abruptly before completion	SROF	Status, requested operation failed
		SSTP	Status, execution stopped gracefully before completion
SACC	Status, already cross-connected		
SADC	Status, already disconnected	SWFA	Status, working entity failed

Main Fuse Panels and Charts

Tables 1 (Interface Bays) and 2 (Switch Bay) relate DACS IV-2000 (256) fuses for bays, interface modules, and fan assemblies to their physical location on the fuse and alarm panel (see Figure 5 [ED-2C940-30 Fuse and Alarm Panel] or Figure 6 [ED-9C114-30 Fuse and Alarm Panel]) at the top of the Switch Bay.

Bus C	C2-2	C3-2	C4-2	C5-2	C6-2	C7-2	C8-2	C9-2	C10-2	C11-2	C12-2	Bus D	D2-2	D3-2	D4-2	D5-2	D6-2	D7-2	D8-2	D9-2	D10-2	D11-2	D12-2	Bus E	E6	E7	E8
C1-1	C2-1	C3-1	C4-1	C5-1	C6-1	C7-1	C8-1	C9-1	C10-1	C11-1	C12-1	D1-1	D2-1	D3-1	D4-1	D5-1	D6-1	D7-1	D8-1	D9-1	D10-1	D11-1	D12-1	E1	E2	E3	E4
Bus A	A2-2	A3-2	A4-2	A5-2	A6-2	A7-2	A8-2	A9-2	A10-2	A11-2	A12-2	Bus B	B2-2	B3-2	B4-2	B5-2	B6-2	B7-2	B8-2	B9-2	B10-2	B11-2	B12-2	B13-2	B14-2	B15-2	B16-2
A1-1	A2-1	A3-1	A4-1	A5-1	A6-1	A7-1	A8-1	A9-1	A10-1	A11-1	A12-1	B1-1	B2-1	B3-1	B4-1	B5-1	B6-1	B7-1	B8-1	B9-1	B10-1	B11-1	B12-1	B13-1	B14-1	B15-1	B16-1
Bus A	A13-2	A14-2	A15-2	A16-2	A17-2	A18-2	A19-2	Bus B	B17-2	B18-2	B19-2	Bus C	C13-2	C14-2	C15-2	C16-2	C17-2	C18-2	C19-2	Bus D	D13-2	D14-2	D15-2	D16-2	D17-2	D18-2	D19-2
Bus A	A13-1	A14-1	A15-1	A16-1	A17-1	A18-1	A19-1	Bus B	B17-1	B18-1	B19-1	Bus C	C13-1	C14-1	C15-1	C16-1	C17-1	C18-1	C19-1	Bus D	D13-1	D14-1	D15-1	D16-1	D17-1	D18-1	D19-1

Note: Fuses for power buses A, B, C, and D come in pairs with the load fuse labeled with -1 and the indicator fuse labeled with -2. Fuses for power bus E do not have dual fuses (one load and one indicator), they are all indicator fuses.

Figure 5. Main Fuse Panel (ED-2C940-30 Fuse Panel)
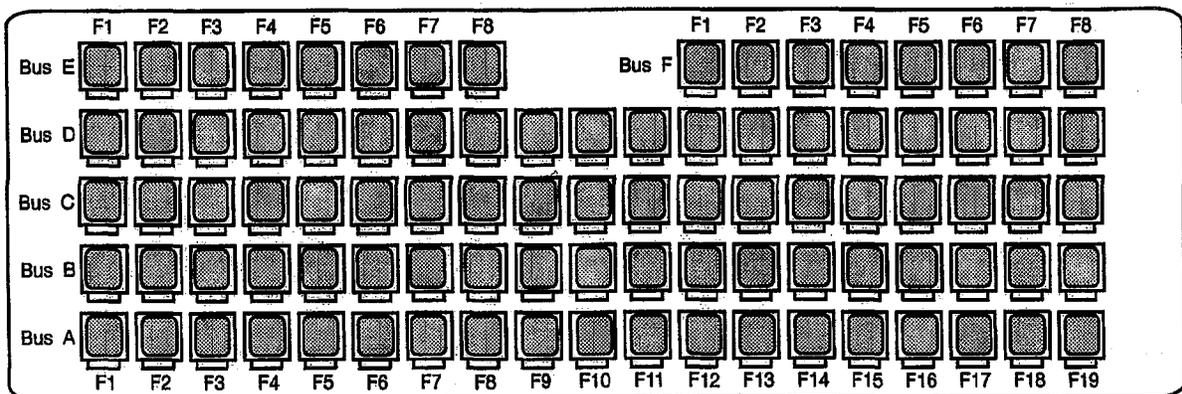
Note: Fuse location B1 is not connected. Fuses A1, A2, B2, C1, C2, and D2 are 12A, fuse D1 is 2A, all other fuses are 10A. All fuses have a red alarm lamp to indicate failure.

Figure 6. Main Fuse Panel (ED-9C114-30 Fuse Panel)

Table 1. Fuse Chart Interface Bays (Bay 1-4 and 6-9)

Shelf	PWR Circuit Pack	Bay 1	Bay 2	Bay 3	Bay 4	Bay 6	Bay 7	Bay 8	Bay 9
Standard Power (ED-2C940-30 Fuse Panel)									
4	PWRE-2	C17	D14	D4	D10	C12	D6	B15	C19
	PWRE-1	A17	C15	B4	C10	B12	B6	C8	A19
3	PWRE-2	D16	D13	C4	B10	D12	C6	B8	D18
	PWRE-1	A16	A14	A4	A10	A12	A6	A8	C18
2	PWRE-2	B18	C14	D3	C9	D11	D5	C7	D19
	PWRE-1	A15	B17	C3	B9	B11	C5	B7	A18
1	PWRE-2	D15	C13	B3	D9	C11	B5	D7	D17
	PWRE-1	C16	A13	A3	A9	A11	A5	A7	B19
Fan	Main	—	A16	B18	A17	A19	B19	A18	—
	Auxiliary	—	D16	D15	C17	C19	D17	D19	—

Note: All load fuses are 10A and all indicator fuses are 0.5A.

Shelf	PWR Circuit Pack	Bay 1	Bay 2	Bay 3	Bay 4	Bay 6	Bay 7	Bay 8	Bay 9
Duplex Power (ED-2C940-30 Fuse Panel)									
4	PWRE-2	D16	D14	D4	D10	D12	D6	B17	D19
	PWRE-1	B16	B17	B4	B10	B12	B6	B8	B19
3	PWRE-2	C16	C14	C4	C10	C12	C6	C8	C19
	PWRE-1	A16	A14	A4	A10	A12	A6	A8	A19
2	PWRE-2	D15	D13	D3	D9	D11	D5	D7	D18
	PWRE-1	B15	B13	B3	B9	B11	B5	B7	B18
1	PWRE-2	C15	C13	C3	C9	C11	C5	C7	C18
	PWRE-1	A15	A13	A3	A9	A11	A5	A7	A18
Fan	Main	—	A15	A16	B16	B19	A19	A18	—
	Auxiliary	—	C15	C16	D16	D19	C19	C18	—

Note: All load fuses are 10A and all indicator fuses are 0.5A.

Table 1. Fuse Chart Interface Bays (Bay 1-4 and 6-9) (Continued)

Shelf	PWR Circuit Pack	Bay 1	Bay 2	Bay 3	Bay 4	Bay 6	Bay 7	Bay 8	Bay 9
Duplex Power (ED-9C114-30 Fuse Panel)									
4	PWRE-2	F4	D14	D4	D10	D12	D6	D8	F8
4	PWRE-1	E4	B14	B4	B10	B12	B6	B8	E8
3	PWRE-2	F3	C14	C4	C10	C12	C6	C8	F7
3	PWRE-1	E3	A14	A4	A10	A12	A6	A8	E7
2	PWRE-2	D15	D13	D3	D9	D11	D5	D7	D18
2	PWRE-1	B15	B13	B3	B9	B11	B5	B7	B18
1	PWRE-2	F2	C13	C3	C9	C11	C5	C7	F6
1	PWRE-1	E2	A13	A3	A9	A11	A5	A7	E6
Fan	Main	E1	A15	A16	B16	B19	A19	A18	E5
Fan	Auxiliary	F1	C15	C16	D16	D19	C19	C18	F5

Note: All fuses are rated at 10A and contain a red alarm lamp to indicate failure.

Table 2. Fuse Chart Switch Bay (Bay 5)

Auxiliary Power PWRE		Switch Power PWRA				Fan Assembly	
1	2	1	2	3	4	Main	Auxiliary
Standard Power (ED-2C940-30 Fuse Panel)							
B14	D8	A2	B2	C2	D2	E6	B13-2

Note: Fuses A2-1, B2-1, C2-1, and D2-1 are 12 A and fuses B14-1 and D8-1 are 10 A. Fuses A2-2, B2-2, B14-2, C2-2, D2-2, and D8-2 (indicator fuses) are 0.5 A.

Duplex Power (ED-2C940-30 Fuse Panel)							
B14	D8	A2	B2	C2	D2	A17	C17

Note: Fuses A2-1, B2-1, C2-1, and D2-1 are 12A and fuses B14-1, D8-1, A17-1, and C17-1 are 10A. Fuses A2-2, B2-2, B14-2, C2-2, D2-2, D8-2, A17-2, and C17-2 (indicator fuses) are 0.5A.

Duplex Power (ED-9C114-30 Fuse Panel)

B14	D8	A2	B2	C2	D2	A17	C17
PWRF-1, PWRG-1, TBS3-0 (SYNC-0)			PWRF-2, PWRG-2, TBS3-1 (SYNC-1)			Header Designation Assembly	
A1			C1			D1	

Note: Fuses A1, A2, B2, C1, C2, and D2 are 12A, fuses B14 and D8 are 10A, and fuse D1 is 2A. All fuses have a red alarm lamp to indicate failure.
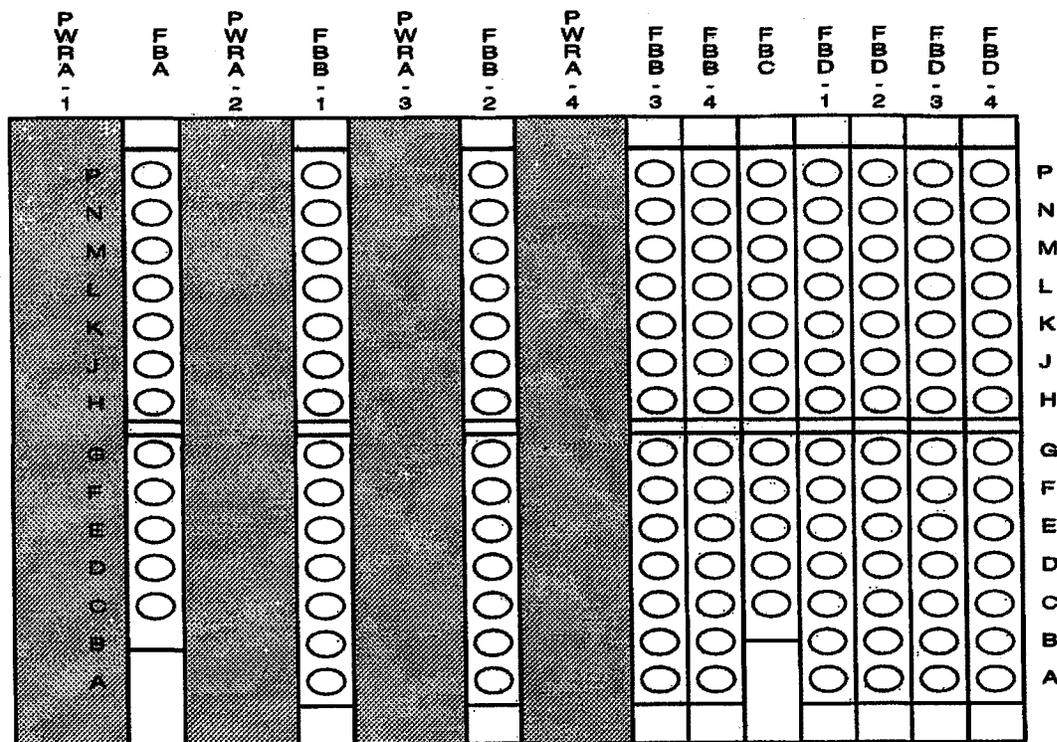
Secondary Fuses

Figure 7. Secondary Fuses (FBA, FBB, FBC, and FBD)

Table 3. Secondary Fuse Chart for the DACS IV-2000 (256)

Location	Type 77D (10A) Fuse for +5V Supply				
	FBA	FBB-1	FBB-2	FBB-3	FBB-4
P N M	SWIO-11 SWIO-10 SWIO-9	SWCS-9 SWCS-8 SWCS-7	SWCS-23 SWCS-22 SWCS-21	SWIO-21 SWIO-20 SWIO-19	SYNC-1*† SYNC-0* SWIO-32
L K J H	CLKGN-0 SWIO-8 SWIO-7 SWIO-6	SWCS-6 SWCS-5 SWCS-4 SWCS-3	SWCS-20 SWCS-19 SWCS-18 SWCS-17	SWIO-18 SWIO-17 SWCS-32 SWCS-31	SWIO-31 SWIO-30 SWIO-29 SWIO-28
G F E D	SWIO-5 SWIO-4 SWIO-3 SWIO-2	SWCS-2 SWCS-1 SWIO-16 SWIO-15	SWCS-16 SWCS-15 SWCS-14 SWCS-13	SWCS-30 SWCS-29 SWCS-28 SWCS-27	SWIO-27 SWIO-26 SWIO-25 CLKGN-1
C B A	SWIO-1 - -	SWIO-14 SWIO-13 SWIO-12	SWCS-12 SWCS-11 SWCS-10	SWCS-26 SWCS-25 SWCS-24	SWIO-24 SWIO-23 SWIO-22
Location	Type 78J (7.5A) Fuse for -5V Supply				
	FBC	FBD-1	FBD-2	FBD-3	FBD-4
P N M	SWIO-11 SWIO-10 SWIO-9	SWCS-9 SWCS-8 SWCS-7	SWCS-23 SWCS-22 SWCS-21	SWIO-21 SWIO-20 SWIO-19	SYNC-1* SYNC-0* SWIO-32
L K J H	CLKGN-0 SWIO-8 SWIO-7 SWIO-6	SWCS-6 SWCS-5 SWCS-4 SWCS-3	SWCS-20 SWCS-19 SWCS-18 SWCS-17	SWIO-18 SWIO-17 SWCS-32 SWCS-31	SWIO-31 SWIO-30 SWIO-29 SWIO-28
G F E D	SWIO-5 SWIO-4 SWIO-3 SWIO-2	SWCS-2 SWCS-1 SWIO-16 SWIO-15	SWCS-16 SWCS-15 SWCS-14 SWCS-13	SWCS-30 SWCS-29 SWCS-28 SWCS-27	SWIO-27 SWIO-26 SWIO-25 CLKGN-1
C B A	SWIO-1 - -	SWIO-14 SWIO-13 SWIO-12	SWCS-12 SWCS-11 SWCS-10	SWCS-26 SWCS-25 SWCS-24	SWIO-24 SWIO-23 SWIO-22

* SYNC fuses provide fuse protection for all three circuit packs (DPLL, TBS3, and DS1TX) associated with a synchronizer side.

† Also provides fuse protection for the Auxiliary Power Module.
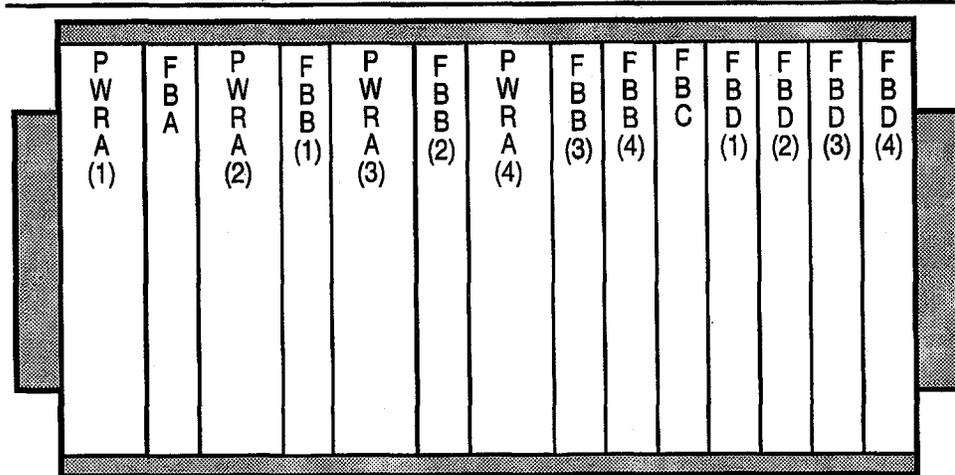
Redundant Controller Power Module Fuses

Notes:

- Numbers in parentheses are circuit pack position numbers in the Redundant Controller Module. Fuse ratings are listed below the circuit pack identifier.

- The 7.5A fuses are the load fuses to the PWRF and PWRG power circuit packs.

- The 5A (2A for the Status Panel) fuses are the secondary fuses (or the +5V supply) to the circuit packs contained in the Redundant Controller Module.

- The 1A fuses associated with the ECI circuit packs are for +12V and -12V supplied to the CILINKs. When these fuses blow, communication with the CILINKs can be interrupted.

- The 5A fuses for the optical disk drive (SEC) is for the +5V and +12V supply.

- The 5A fuses for the hard disk drives (PRI) are for the +5V and +12V supply.

- The 2A fuses for SYNCF (TBS3-0) and SYNCG (TBS3-1) are for the -48V supply to the TBS3 circuit packs.

- The labels SPR, SPRF, and SPRG denote spare fuses that are not connected to any circuit pack.

Figure 8. Redundant Controller Power Module Fuses (FBF, FBG, FBH, and FBI)
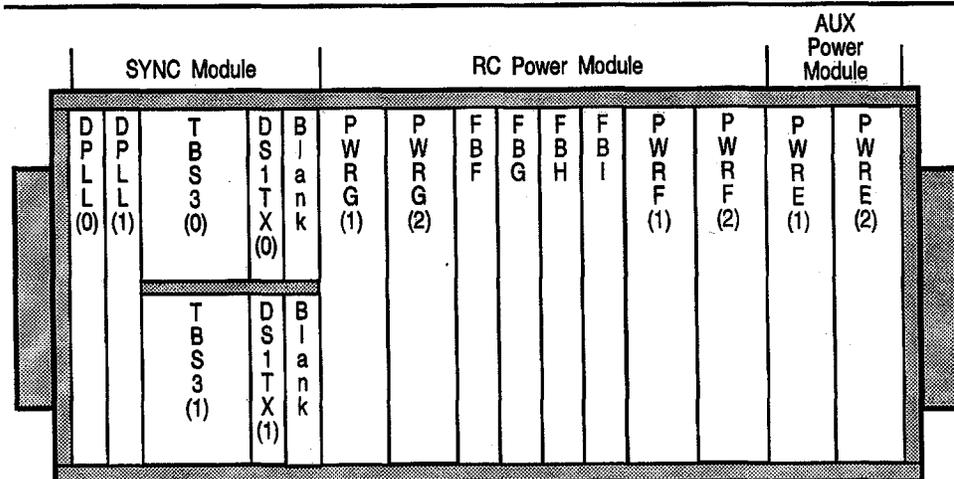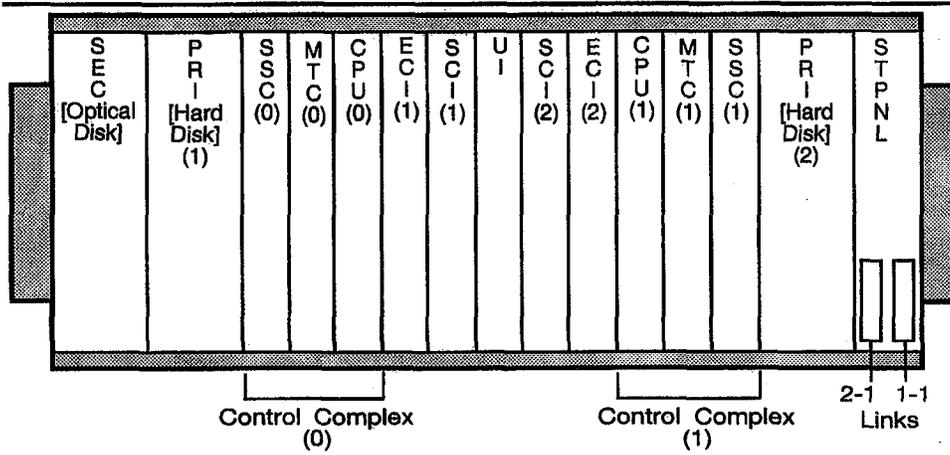
Equipment Module Diagrams

Switch Power Module

PWRA (1)	FBA	PWRA (2)	FBB (1)	PWRA (3)	FBB (2)	PWRA (4)	FBB (3)	FBB (4)	FBC	FBD (1)	FBD (2)	FBD (3)	FBD (4)

Note: Number in parentheses is circuit pack position in module.

Auxiliary and Redundant Controller Power and Synchronizer Modules

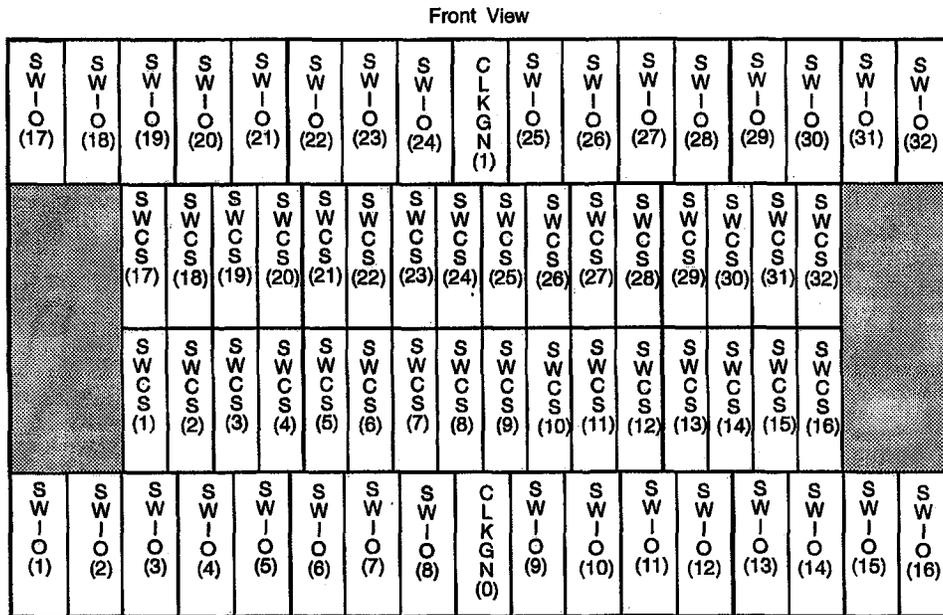| SYNC Module					RC Power Module								AUX Power Module	
DPLL (0)	DPLL (1)	TBS3 (0)	DS1TX (0)	Blank	PWRG (1)	PWRG (2)	FBF	FBG	FBH	FBI	PWRF (1)	PWRF (2)	PWRE (1)	PWRE (2)
		TBS3 (1)	DS1TX (1)	Blank										

Note: Number in parentheses is circuit pack position in module.

Redundant Controller Module

SEC [Optical Disk]	PRI [Hard Disk] (1)	SSC (0)	MTC (0)	CPU (0)	ECI (1)	SCI (1)	UI	SCI (2)	ECI (2)	CPU (1)	MTC (1)	SSC (1)	PRI [Hard Disk] (2)	STPNL

Control Complex (0)   Control Complex (1)   2-1 1-1 Links

Note: Number in parentheses is circuit pack position in module.

Switch Module

Front View

SWIO (17)	SWIO (18)	SWIO (19)	SWIO (20)	SWIO (21)	SWIO (22)	SWIO (23)	SWIO (24)	CLKGN (1)	SWIO (25)	SWIO (26)	SWIO (27)	SWIO (28)	SWIO (29)	SWIO (30)	SWIO (31)	SWIO (32)
		SWCS (17)	SWCS (18)	SWCS (19)	SWCS (20)	SWCS (21)	SWCS (22)	SWCS (23)	SWCS (24)	SWCS (25)	SWCS (26)	SWCS (27)	SWCS (28)	SWCS (29)	SWCS (30)	SWCS (31)	SWCS (32)
		SWCS (1)	SWCS (2)	SWCS (3)	SWCS (4)	SWCS (5)	SWCS (6)	SWCS (7)	SWCS (8)	SWCS (9)	SWCS (10)	SWCS (11)	SWCS (12)	SWCS (13)	SWCS (14)	SWCS (15)	SWCS (16)
SWIO (1)	SWIO (2)	SWIO (3)	SWIO (4)	SWIO (5)	SWIO (6)	SWIO (7)	SWIO (8)	CLKGN (0)	SWIO (9)	SWIO (10)	SWIO (11)	SWIO (12)	SWIO (13)	SWIO (14)	SWIO (15)	SWIO (16)

Note: Number in parentheses is circuit pack position in module.

DS1 Interface/Interface-Protection Module

SWIF (5)	DS1IF (5A)	DS1IF (5B)	DS1RY (3)	DS1IF/DS1IP (6/P)(A)	DS1IF/DS1IP (6/P)(B)	SWIF (6/P)	UC	CLKDR (2)	SWIF (7/6)	DS1IF (7/6)(A)	DS1IF (7/6)(B)	DS1RY (4)	DS1IF (8/7)(A)	DS1IF (8/7)(B)	SWIF (8/7)	PWRE (2)
SWIF (1)	DS1IF (1A)	DS1IF (1B)	DS1RY (1)	DS1IF (2A)	DS1IF (2B)	SWIF (2)	BXA	CLKDR (1)	SWIF (3)	DS1IF (3A)	DS1IF (3B)	DS1RY (2)	DS1IF (4A)	DS1IF (4B)	SWIF (4)	PWRE (1)

Note: Number in parentheses is circuit pack position in module. For entries with slashes (/), the entry before the slash corresponds to the DS1 Interface Module and the entry after the slash corresponds to the DS1 Interface-Protection Module.

For provisioned DS1 Interface and DS1 Interface-Protection Modules, see minimum equipage tables on next page. For unprovisioned DS1 Interface Modules within a DS1 Interface protection group associated with a provisioned DS1 Interface-Protection Module, all DS1IF circuit pack slots must be equipped with either BXA or DS1IF circuit packs and all SWIF circuit packs slots must be equipped with either BXA or SWIF circuit packs if the DS1 Interface Module has been cabled (that is, an DS1 Interface Module that is not cabled can be left empty). If the DS1 Interface-Protection Module within an DS1 interface protection group is unprovisioned, no circuit packs are required in any of the interface modules associated with the DS1 Interface-Protection Module. However, interface or BXA circuit packs are recommended to keep out dust and other foreign matter.

Table 4. DS1 Interface-Protection Module Minimum Equipage

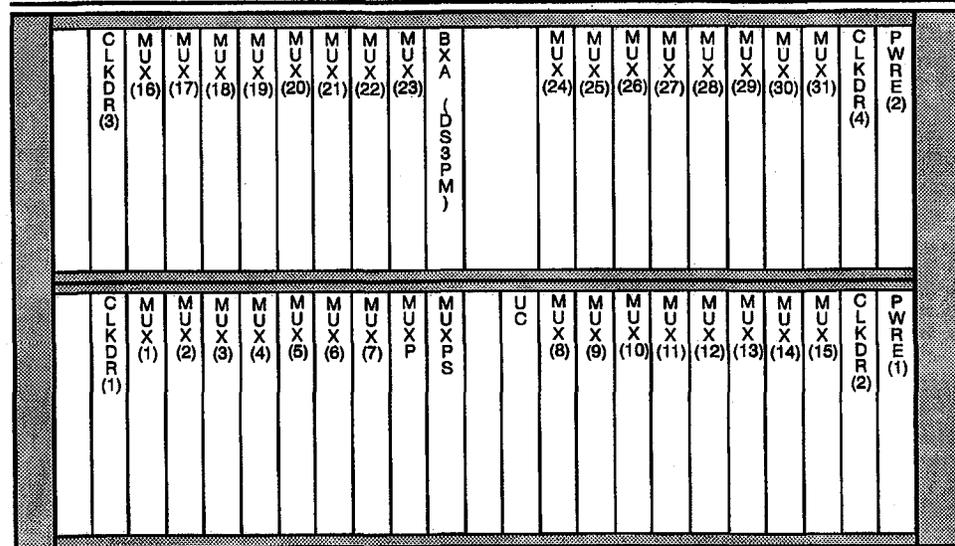| Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
DS1RY1	AKM48	4
DS1IP1	AKM47	2
DS1IF1	AKM46	2
SWIF1/SWIF2	AKM49/AKM50	2
BXA1	AKM64	19
SWIO1	AWR6	2
PWRE3	556C	2

Note: PMGR circuit packs (AKM66), when used, replace SWIF circuit packs associated with inter-face groups (not the protection group). Refer to Table 17 for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused interface group circuit pack (DS1IF and SWIF) slots and the slot between CLKDR-1 and SWIF-2 only, and must not be inserted in any other circuit pack slot (for example, DS1RY slots must never contain BXA circuit packs).

Table 5. DS1 Interface Module Minimum Equipage

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
DS1RY1	AKM48	4
DS1IF1	AKM46	2
SWIF1/SWIF2	AKM49/AKM50	1
BXA1	AKM64	22
SWIO1	AWR6	2
PWRE3	556C	2

Note: PMGR circuit packs (AKM66), when used, replace SWIF circuit packs. Refer to Table 17 for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused interface group circuit pack (DS1IF and SWIF) slots and the slot between CLKDR-1 and SWIF-2 only, and must not be inserted in any other circuit pack slot (for example, DS1RY slots must never contain BXA circuit packs).
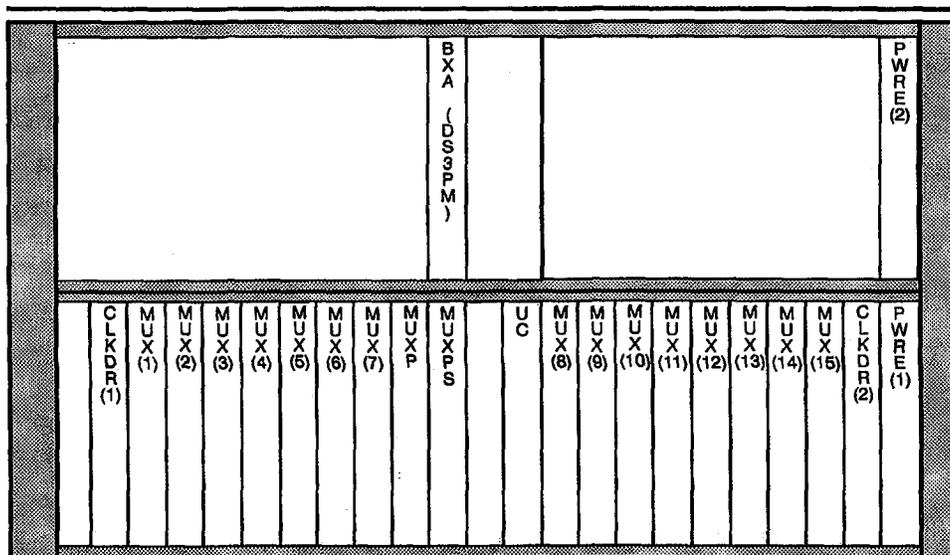
DS3 Interface-32 Module

| C
L
K
D
R
(3) | M
U
X
(16) | M
U
X
(17) | M
U
X
(18) | M
U
X
(19) | M
U
X
(20) | M
U
X
(21) | M
U
X
(22) | M
U
X
(23) | B
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(24) | M
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X
(25) | M
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X
(26) | M
U
X
(27) | M
U
X
(28) | M
U
X
(29) | M
U
X
(30) | M
U
X
(31) | C
L
K
D
R
(4) | P
W
R
E
(2) |
| C
L
K
D
R
(1) | M
U
X
(1) | M
U
X
(2) | M
U
X
(3) | M
U
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(4) | M
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(5) | M
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(6) | M
U
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(7) | M
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(8) | M
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(9) | M
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(10) | M
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(12) | M
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(13) | M
U
X
(14) | M
U
X
(15) | C
L
K
D
R
(2) | P
W
R
E
(1) |

Note: Number in parentheses is circuit pack position in module.

Table 6. DS3 Interface-32 Module Minimum Equipage

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	4
MUXPS1	AKM53	1
MUXP1/MUXP2	AKM55/AKM70	1
MUX1/MUX2	AKM52/AKM68	1
BXA1	AKM64	31
SWIO1	AWR6	4
PWRE3	556C	2

**Note:** PMGR circuit packs (AKM66), when used, replace MUX1/MUX2 circuit packs. Refer to Table 17 for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused MUX and the DS3PM circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs).

DS3 Interface-16 Module

Note: Number in parentheses is circuit pack position in module.

Table 7. DS3 Interface-16 Module Minimum Equipage

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
MUXPS1	AKM53	1
MUXP1/MUXP2	AKM55/AKM70	1
MUX1/MUX2	AKM52/AKM68B	1
BXA1	AKM64	15
SWIO1	AWR6	2
PWRE3	556C	2

Note: PMGR circuit packs (AKM66), when used, replace MUX1/MUX2 circuit packs. Refer to Table 17 for maximum allowable PMGR circuit packs. BXA circuit packs must be inserted into unused MUX and DS3PM circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs).

Table 8. Enhanced DS3 Interface-16 Module Minimum Equipage

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
MUXPS1	AKM53	1
MUXP3	AKM92	1
MUX2/MUX3	AKM68B/AKM91	1
BXA1	AKM64	15
SWIO1	AWR6	2
PWRE3	556C	2

Note: BXA circuit packs must be inserted into unused MUX and DS3PM circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs). PMGR circuit packs are not allowed in Enhanced DS3 Interface-16 Modules.

Table 9. DS3 Clear-Channel Interface-16 Module Minimum Equipage

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
MUXPS1	AKM53	1
MUXP3	AKM92	1
MUX3	AKM91	1
BXA1	AKM64	15
SWIO1	AWR6	2
PWRE3	556C	2

Note: BXA circuit packs must be inserted into unused MUX and DS3PM circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs). PMGR circuit packs are not allowed in DS3 Clear-Channel Interface-16 Modules.

STS1 Interface-16 Module
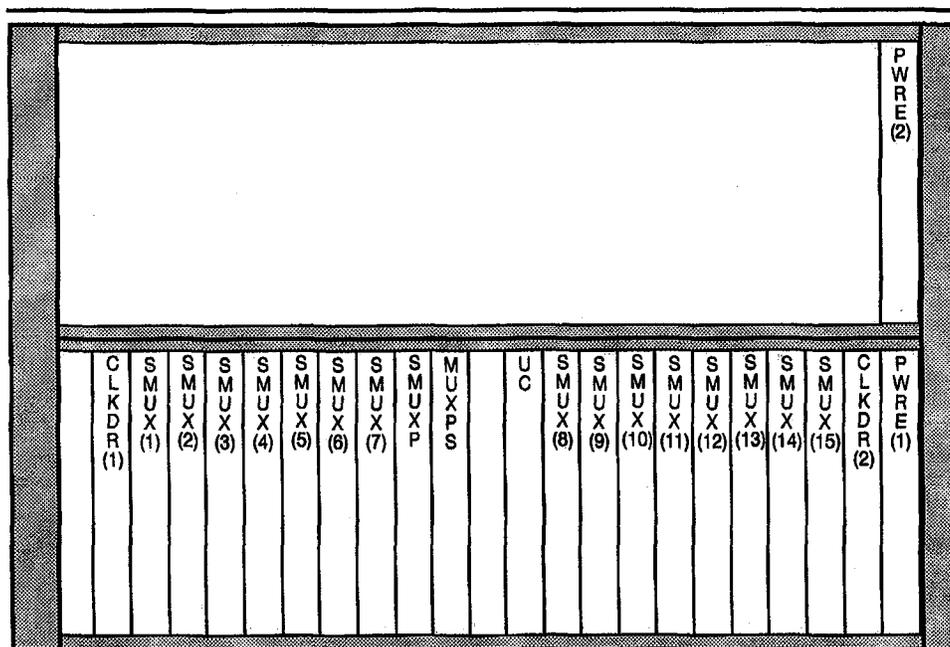
Note: Number in parentheses is circuit pack position in module.

Table 10. STS1 Interface-16 Module Minimum Equipage

Functional Name	Circuit Pack Code	Minimum Quantity
UC2	AKM59B	1
CLKDR1	AKM56	2
MUXPS1	AKM53	1
SMUXP1	AKM85	1
SMUX1	AKM84	1
BXA1	AKM64	14
SWIO1	AWR6	2
PWRE3	556C	2

Note: BXA circuit packs must be inserted into unused SMUX circuit pack slots only, and must not be inserted in any other circuit pack slot (for example, MUXPS slots must never contain BXA circuit packs).

Circuit Pack Cross-Reference

Module	Circuit Pack	Code	System Address
RC Module	CPU2 ECI3 MTC3 PRI5 SCI3 SEC5 SSC5 STPNL UI2	AWP6 AWP8 AWR10 ERB5 AWR2C ERB6 AWP14 ED-9C046 AWR12	CPU-{0,1} ECI-{1,2} MTC-{0,1} PRI-{1,2} SCI-{1,2} SEC SSC-{0,1} STPNL UI
SYNC Module	DPLL1/DPLL2 DS1TX1/DS1TX2 TBS31/TBS32	AWP9/AWP15 AWS5/AWS9 AWS3AWS8	DPLL-{0,1} TX-{0,1} TB-{0,1}
RC Power Module	PWRF PWRG FBF FBG FBH FBI	427AA 428AA ED-9C051 ED-9C052 ED-9C053,G2 ED-9C055	PWRF-{1,2} PWRG-{1,2} — — — —
SW Module	SWIO1 SWCS1 CLKGN2	AWR6 AWS1B AWR7	SWIO-{1-32} SWCS-{1-32} CLKGN-{0,1}
SW Power Module	PWRA1/PWRA2 FBA FBB FBC FBD	552A/566A ED-2C962-30,G1 ED-2C960-30,G1 ED-2C963-30,G1 ED-2C961-30,G1	PWRA-{1-4} — — — —
AUX Power Module	PWRE3	556C	POWERE-SW-{1,2}
DS1 Interface Modules	CLKDR1 DS1IF1 DS1IP1 DS1RY1 PMGR1 SWIF1/SWIF2 UC1/UC2 PWRE3 BXA1	AKM56 AKM46/AKM46B AKM47 AKM48 AKM66 AKM49/AKM50 AKM59/AKM59B 556C AKM64	CLKDR-{1-32}-{1-4} DS1IF-{1-32}-{1A-8B} DS1IP-{1-32}-{PA,PB} DS1RY-{1-32}-{1-4} SWIF-{1-32}-{1-8} SWIF-{1-32}-{1-8,P} UC-{1-32} PWRE-{1-32}-{1,2} —

Table continued on next page.

Module	Circuit Pack	Code	System Address
DS3 Interface Modules	CLKDR1 DS3PM1 MUX1/MUX2/MUX3 MUXP1/MUXP2/MUXP3 MUXPS1 PMGR1 UC1/UC2 PWRE3 BXA1	AKM56 AKM62 AKM52/AKM68B/AKM91 AKM55/AKM70B/AKM92 AKM53 AKM66 AKM59/AKM59B 556C AKM64	CLKDR-{1-32}-{1-4} DS3PM-{1-32} MUX-{1-32}-{1-31} MUXP-{1-32} MUXPS-{1-32} MUX-{1-32}-{1-31} UC-{1-32} PWRE-{1-32}-{1,2} —
STS1 Interface Modules	CLKDR1 SMUX1 SMUXP1 MUXPS1 UC1/UC2 PWRE3 BXA1	AKM56 AKM84 AKM85 AKM53 AKM59/AKM59B 556C AKM64	CLKDR-{1-32}-{1-4} SMUX-{1-32}-{1-15} SMUXP-{1-32} MUXPS-{1-32} UC-{1-32} PWRE-{1-32}-{1,2} —

Expendable Equipment Cross-Reference

Equipment (Location)	Part Number	Expected Life
Optical Drive Lens Cleaning Kit	406935346	N/A
Optical Cartridge Emergency Eject Tool	406923292	N/A
Cleaning Kit Refill	406646851	N/A
Filter, Fan Assembly ED2C816-30,G1 (SW Bay)	405056078	3 -6 Months
Filter, Fan Assembly ED2C906-30 (SW Bay)	405470808	3-6 Months
Filter, Fan Assembly ED-9C130, G1/G2	WP-92310,L4A	3-6 Months
LEDs, Fan Assembly ED-9C130,G1/G2 (Order from McLean Engineering, Inc., Princeton-Junction, NJ)	N/A	N/A
Blank Optical Disk Cartridge	J98786SD-5,List 3	N/A
Fuse Extractor Tool	WP-90247,L201	N/A

Fuses:
    2 A Main Fuse (ED-9C114-30 Fuse Panel)
    10 A Main Fuse (ED-9C114-30 Fuse Panel)
    12 A Main Fuse (ED-9C114-30 Fuse Panel)
    12 A Main Fuse (ED-2C940-30 Fuse Panel)
    10 A Main Fuse (ED-2C940-30 Fuse Panel)
    5 A 70D Indicator Fuse (ED-2C940-30 Fuse Panel)
    2 A 70B Indicator Fuse (ED-2C940-30 Fuse Panel)
    0.5 A 70G Indicator Fuse (ED-2C940-30 Fuse Panel)
    10 A SW PWR MOD 77D Fuse (FBA and FBB)
    7.5 A SW PWR MOD 78J Fuse (FBC and FBD)
    7.5 A RC PWR MOD Fuse (FBI)
    5 A RC PWR MOD Fuse (FBF, FBG, and FBH)
    2 A RC PWR MOD Fuse (FBH and FBI)
    1 A RC PWR MOD Fuse (FBF and FBG)
    0.5 A RC PWR MOD Fuse (FBI)
	
	WP91768.L107
	WP91768,L114
	WP91768,L115
	KS19780,L8
	KS19780,L2
	100203355
	100203330
	100203389
	KS-23543L77D
	KS-23543L78J
	WP-90247L314
	WP-90247L313
	WP-90247L309
	WP-90247L306
	WP-90247L303
		
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A
		N/A

Provisioning Sequence

Entity	Number oF Circuit Packs Required	Supporting Entity
CC *	(9)	none
PRI †	(2)	none
SEC	(1)	none
SYNC ‡	(6)	none
CLKGN	(2)	none
ECI †	(2)	CC
SWCS	(32)	CLKGN, CC
SWIO **	(2)	SWCS
UNIT ‡‡	(1)	SWIO
CLKDR **	(2) or (4)††	UNIT, SWIO
PMGR	(1)	CLKDR
MUXP	(1)	CLKDR
MUX	(1)	MUXP
SMUXP	(1)	CLKDR
SMUX	(1)	SMUXP
DS1RY	(1)	UNIT
SWIF	(1)	CLKDR
DS1IP	(1)	SWIF, DS1RY
DS1IF	(2)	SWIF, DS1IP §§

*   Must be provisioned as a group (CPU, MTC, SCI1, SCI2, SSC, UI). If both controller sides are not provisioned, an alarm is raised.

†   If one or both ECI circuit packs or one or both PRI disk drives are not provisioned, one or more alarms are raised.

‡   SYNC is provisioned as a group (DPLL, DS1TX [TX], TBS3 [TB]). If all circuit packs on both SYNC sides are not present, alarms are raised.

§   SYNC is required if CLKGN3 circuit packs are present (to support SONET or DS3cc).

**   Must be provisioned in pairs.

††   Depending on the type of interface module

‡‡   DS1 Interface Module requires supporting DS1 Interface-Protection Module.

§§   The supporting DS1IP circuit pack can be in another DS1 Interface Module.

Loopbacks

The DACS IV-2000 provides DS1 signal loopback, DS3 line loopback, STS-1 signal loopback, and VT1.5 wideband (terminal) loopback features that can be used to facilitate testing and trouble isolation. DS1 facilities and DS1 tributaries on DS3 facilities and EC-1 facilities can be looped back. STS-1 and VT1.5 loopbacks are performed through EC-1 facilities only. Figure 9 shows examples of the possible loopback features available in the DACS IV-2000. The following is a list of the different loopback types available:

■ DS1 Loopbacks — can be operated on a specified DS1 port or range of DS1 ports, towards the facility, towards the switch, or through the switch fabric of a DS1 Interface, a DS3 Interface (tributary of a DS3), or an STS1 Interface (as a VT1.5 tributary) Module within the system. DS1 loopbacks can be one of the following four types:

— LPBKL (Line Loopback) — loops the signal from the input port to the output port (towards the facility) at the DS1 Interface Module.

— LPBKT (Terminal Loopback) — loops the signal from the input port to the output port (through the switch matrix) in the Switch Module. DS1 terminal loopbacks are valid for near-end on DS1 interface (DS1IF), DS3 interface (MUX, MUX2, or MUX3), or SONET interface (SMUX) circuit packs.

— LPBKI (Internal Loopback) — loops the signal from the output port to the input port (towards the switch) at the DS1 Interface Module.

— LPBKM (DS1 Tributary Loopback) — loops a DS1 tributary signal within a DS3 interface (MUX2 or MUX3) circuit pack from the input port to the output port (towards the facility) at the DS3 Interface Module. DS1 tributary loopbacks are valid for either near-end or far-end on MUX2 or MUX3 circuit packs only.

■ DS3 Loopbacks — can be operated on a specified DS3 port or range of DS3 ports, towards the facility (MUX2 or MUX3 circuit pack only) or through the switch matrix (MUX3 circuit pack only) of a DS3 Interface Module within the system. DS3 loopbacks can be one of the following two types:

— LPBKL (Line Loopback) — loops the incoming DS3 signals directly to the outgoing direction of the same port. This loopback happens directly in the MUX2 or MUX3 circuit pack. The DS3 line loopback is supported in both clear-channel and DS1 modes for MUX3 circuit packs. This keeps the signal from entering the switch matrix and thus keeps the amount of hardware encountered to a minimum. Because the signal is not demultiplexed, it retains all its control bits, overhead bits, and bipolar violations, and preserves the timing of the looped back signal. The only modification of the DS3 signal occurs when the system regenerates the signal to meet the specifications for an outgoing DS3 signal.

— LPBKT (Terminal Loopback) [MUX3 circuit pack only] — loops the DS3 signal from the input port to the output port (through the switch fabric) in the Switch Module when the MUX3 circuit pack is provisioned for clear-channel mode. Bipolar violations are not preserved for DS3 terminal loopbacks.

■ STS-1 Loopbacks — can be operated on a specified STS-1 port or range of STS-1 ports, either towards the facility or through the switch fabric of an STS1 Interface Module. STS-1 loopbacks can be one of the following two types:

— LPBKL (Line Loopback) — loops the signal from the input port to the output port (towards the facility) at the STS1 Interface Module.

— LPBKT (Terminal Loopback) — loops the signal from the input port to the output port through the switch fabric in the Switch Module. STS-1 terminal loopbacks are valid for near-end on SMUX circuit packs.

■ VT1.5 Wideband (Terminal) Loopbacks — can be operated on a specified VT tributary of an STS-1 signal as a terminal loopback (LPBKT), which loops the VT1.5 signal from the input port to the output port through the switch fabric in the Switch Module.
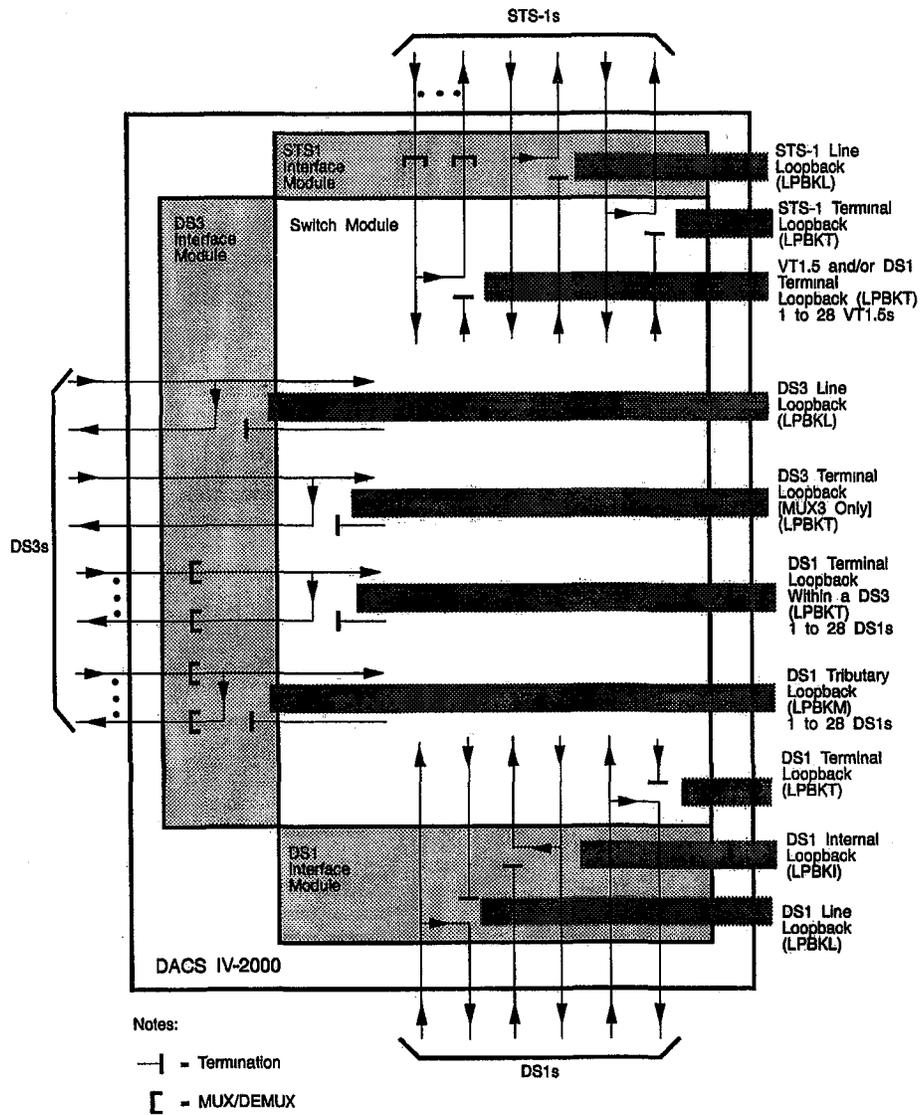
Figure 9. DS1, DS3, STS-1, and VT1.5 Loopbacks

Test Access

When working with test access connections, you need to be familiar with terms such as E-End, F-End, and A and B direction (see Figure 10). The E-End and F-End are arbitrarily designated for a one-way or a two-way cross-connection. For example, the E-End can be designated to correspond to a *short haul* transmission path to a piece of equipment (for example, a DACS III-2000) within the same Central Office and the F-End can be designated to correspond to a *long haul* transmission path to another Central Office[1]. The E-End and F-End signals are terminated at DS1, DS3, or STS1 Interface Modules. Test access can be established at either the E-End or the F-End through a test access port (TAP). As signals travel through the frame, the path through the frame from the E-End to the F-End is referred to as the *A direction* and the path from the F-End to the E-End is the *B direction*. In a one-way cross-connection, the signal travels in the A direction. The In and Out designations indicate the direction to/from the E-End and F-End. After selecting designations of E-End and F-End, these designations must not change during the test access session.
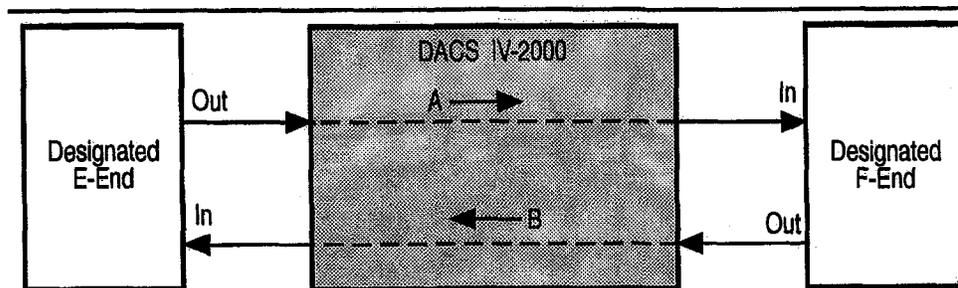

Figure 10. **Test Access Conventions**

There are ten modes of test access in the DACS IV-2000. These modes are:

MONE	SPLTE
MONF	SPLTF
MONEF	SPLTEF
SPLTA	LOOPE
SPLTB	LOOPF

Each mode is described in the following sections.

---

1. Traditionally E-End and F-End mean equipment and facility end, respectively. However, you can designate any port as E-End or F-End.

Monitor Test Access Connections

MONE Mode

The MONE mode (Figure 11) of test access monitors the E-End of an idle port, a one-way cross-connection, or a two-way cross-connection. It reads the incoming signal in direction A.
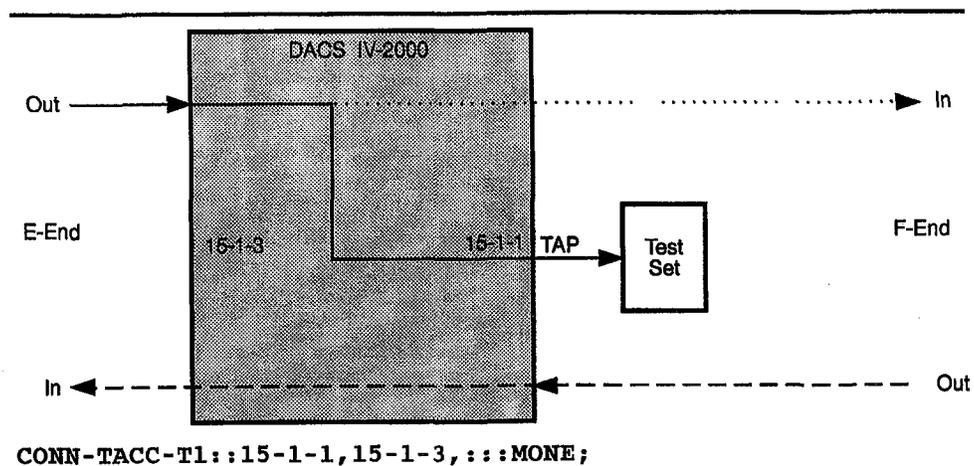


```
CONN-TACC-T1::15-1-1,15-1-3,:::MONE;
```

Figure 11. MONE Mode of Test Access

MONF Mode

The MONF mode (Figure 12) of test access monitors the F-End of a two-way cross-connection. It reads the incoming signal in direction B.
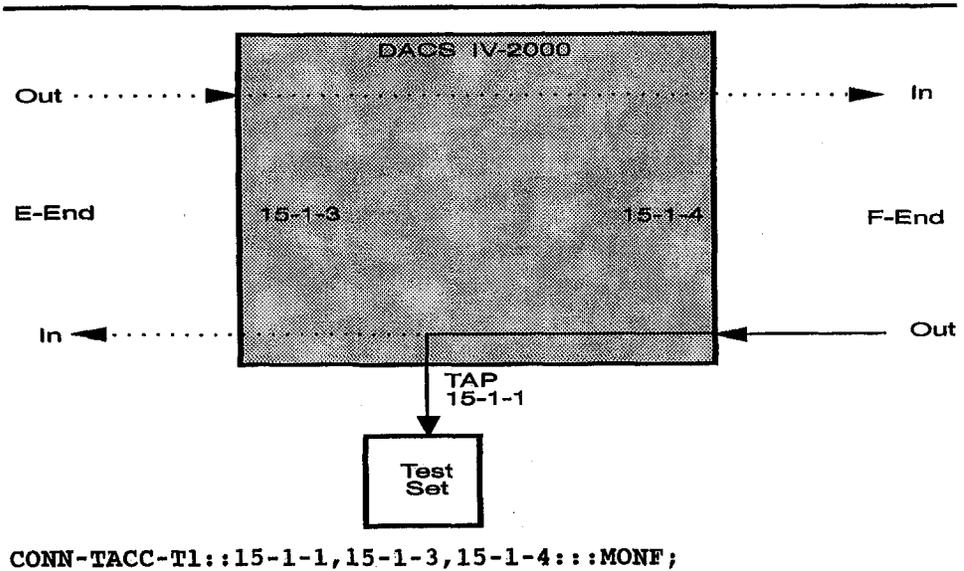
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::MONF;

Figure 12. MONF Mode of Test Access

MONEF Mode

The MONEF mode (Figure 13) of test access monitors both directions of a two-way cross-connection. This mode of test access requires two TAPs. It reads the incoming signals in directions A and B.
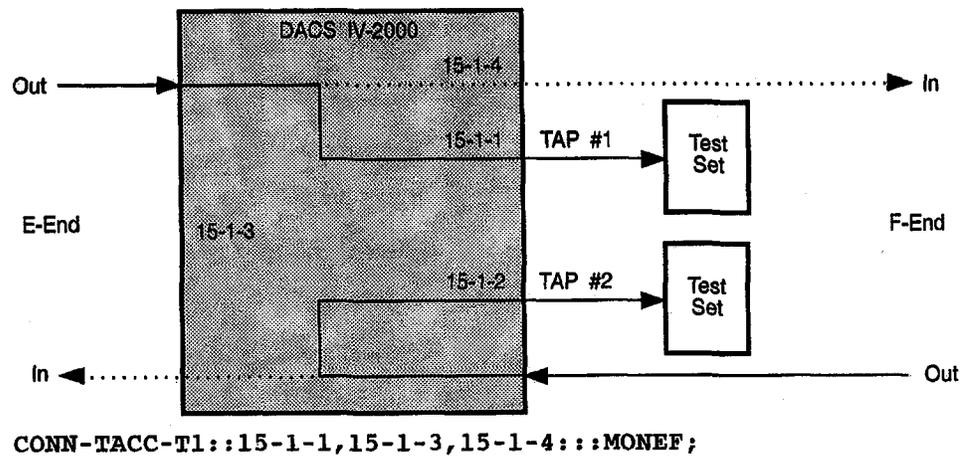

CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::MONEF;

Figure 13. MONEF Mode of Test Access

Split Test Access Connections

SPLTA Mode

The SPLTA mode (Figure 14) of test access splits the E-End (to TAP) to F-End (from TAP) connection of a one-way or two-way cross-connection to allow testing in the A direction.
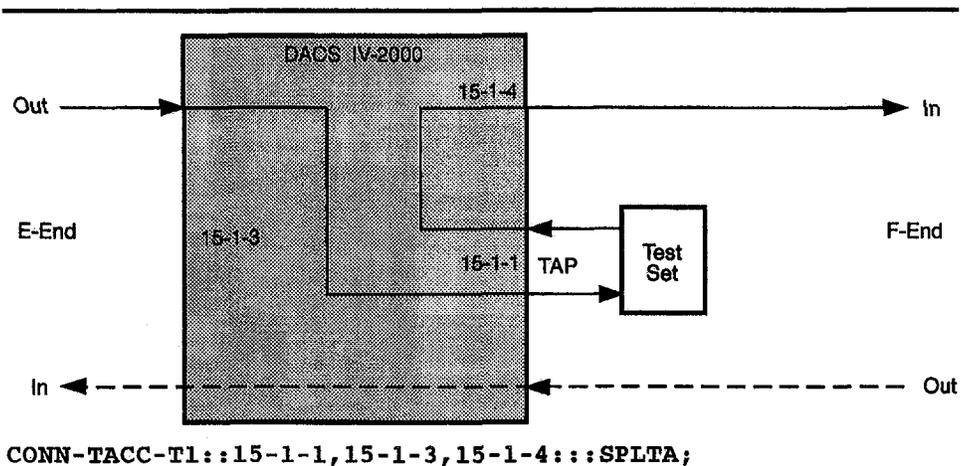

CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTA;

Figure 14. SPLTA Mode of Test Access

SPLTB Mode

The SPLTB mode (Figure 15) of test access splits the F-End (to TAP) to E-End (from TAP) connection of a two-way cross-connection to allow testing in the B direction.
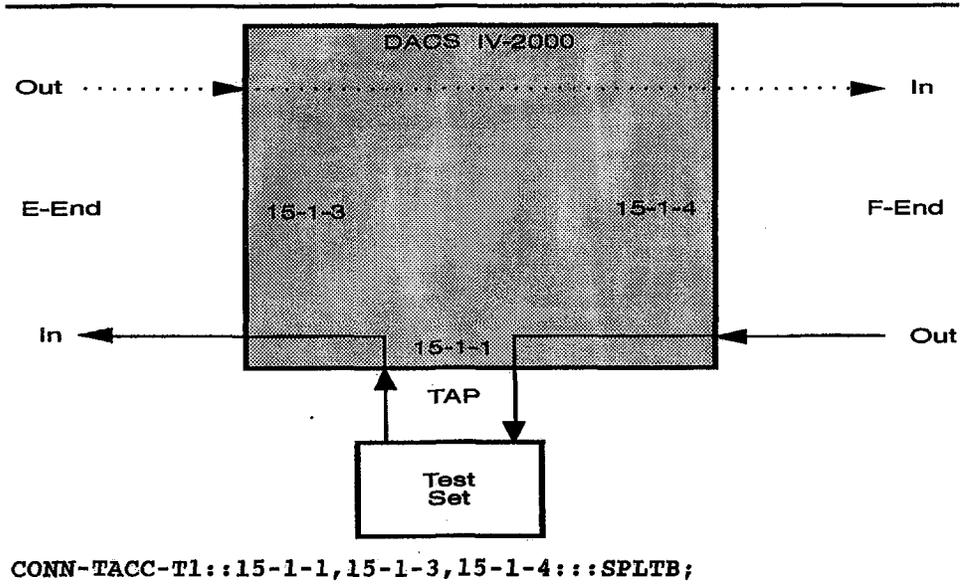
```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTB;
```

Figure 15. SPLTB Mode of Test Access

SPLTE Mode

The SPLTE mode (Figure 16) of test access splits the E-End to F-End of an idle port, a one-way cross-connection, or a two-way cross-connection to allow testing at the E-End. The incoming signal in the A direction goes to the input of the TAP, and the output of the TAP is sent in the B direction.


```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTE;
```
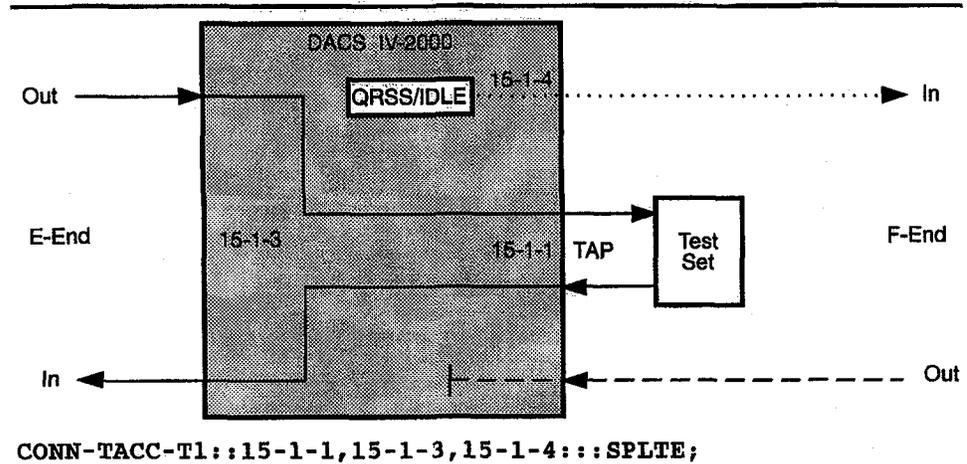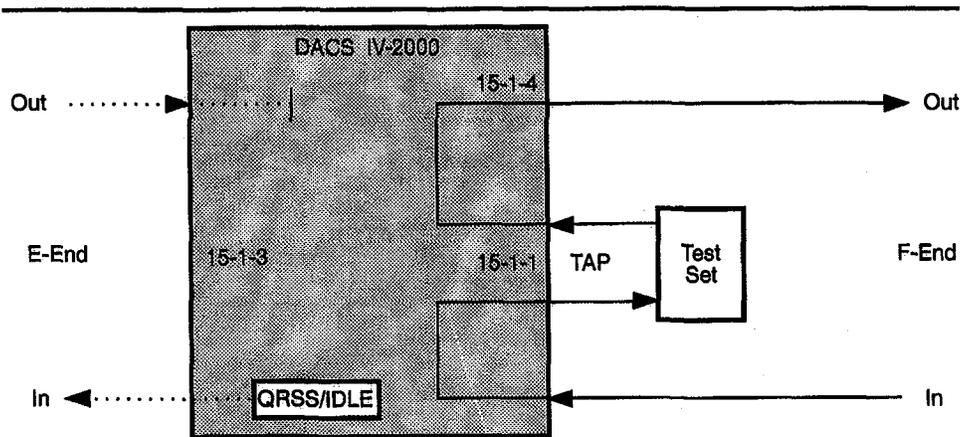
Figure 16. SPLTE Mode of Test Access

For DS1 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

SPLTF Mode

The SPLTF mode (Figure 17) of test access splits the F-End to E-End of a two-way cross-connection to allow testing at the F-End. The incoming signal in the B direction goes to the input of the TAP and the output of the TAP is sent in the A direction.

For DS1 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTF;

Figure 17. SPLTF Mode of Test Access

SPLTEF Mode

The SPLTEF mode (Figure 18) of test access splits both directions of a two-way cross-connection to allow testing at both the E-End and the F-End. This mode of test access requires two TAPs. The incoming signal in the A direction goes to the input of TAP-1 and the output of TAP-1 is sent in the B direction. The incoming signal in the B direction goes to the input of TAP-2 and the output of TAP-2 is sent in the A direction.


```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTEF;
```
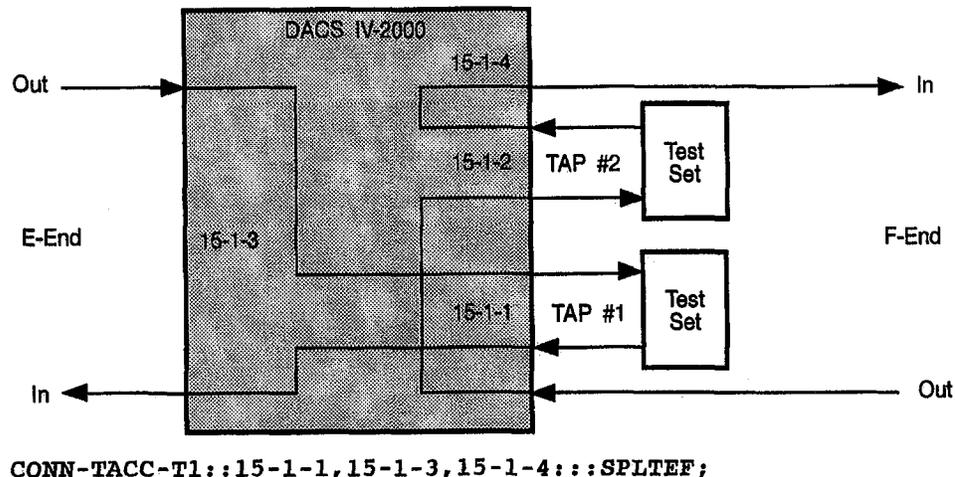
Figure 18. SPLTEF Mode of Test Access

Loopback Test Access Connections

LOOPE Mode

The LOOPE mode (Figure 19) of test access establishes a terminal loopback on the E-End port and monitors the loopback signal. It reads the incoming signal in the A direction.

For DS1 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::LOOPE;
```
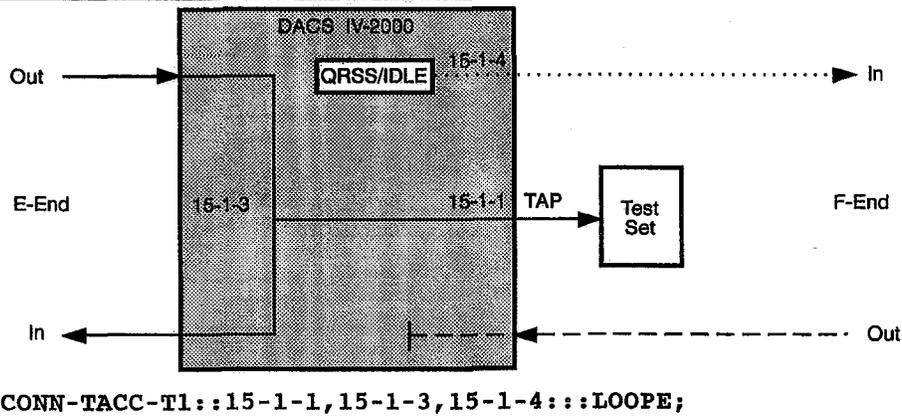
Figure 19. LOOPE Mode of Test Access

LOOPF Mode

The LOOPF mode (Figure 20) of test access establishes a terminal loopback on the F-End port and monitors the loopback signal. It reads the incoming signal in the B direction.

For DS1 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.
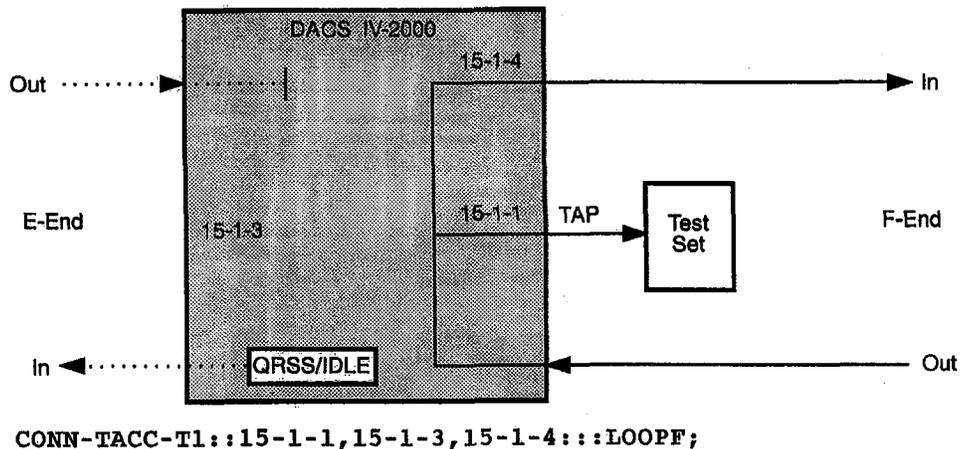


```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::LOOPF;
```

Figure 20. LOOPF Mode of Test Access

Performance Monitoring

DS1 Performance Monitoring Parameters

Table 11. DS1 Performance Parameters

Parameter	Definition	Parameter	Definition
CVP	Path Code Violation	CVL	Line Code Violations
OOFS	Out-of-Frame Second	ESL	Line Errored Seconds
ESP	Path Errored Seconds	SESL	Line Severely Errored Seconds
BESP	Path Bursty Errored Seconds	SEFS	Severely Errored Frame Seconds
SESP	Path Severely Errored Seconds	CSS	Controlled Slipped Seconds
UAS	Unavailable Seconds		

Table 12. DS1 Performance Monitored Parameters

Location	Monitored Parameter	Full-Time			Camp-On			Scan		
		ESF	SF	UNF	ESF	SF	UNF	ESF	SF	UNF
Near-End	CVL	✓	✓	✓	✓	✓	✓	✓	✓	-
	ESL	✓	✓	✓	✓	✓	✓	✓	✓	-
	SESL	✓	✓	✓	✓	✓	✓	✓	✓	-
	CVP	✓	✓	-	✓	✓	-	✓	✓	-
	ESP	✓	✓	-	✓	✓	-	✓	✓	-
	BESP	✓	✓	-	✓	✓	-	-	-	-
	SESP	✓	✓	-	✓	✓	-	✓	✓	-
	OOFS	✓	✓	-	✓	✓	-	✓	✓	-
	UAS	✓	-	-	✓	-	-	-	-	-
	CSS	✓	-	-	-	-	-	-	-	-
Far-End	SEFS	✓	-	-	✓	-	-	✓	-	-
	ESP	✓	-	-	✓	-	-	✓	-	-
	SESP	✓	-	-	✓	-	-	✓	-	-
	CVP	✓	-	-	✓	-	-	-	-	-
	BESP	✓	-	-	✓	-	-	-	-	-
	UAS	✓	-	-	✓	-	-	-	-	-
	CSS	✓	-	-	-	-	-	-	-	-

Note: ✓ denotes parameter being monitored for the given performance monitoring option and line format.

Table 13. Default Thresholds for Full-Time, Camp-On, and Line DS1 Performance Monitoring

Monitored Parameter	DS1 Framing Format							
	Extended Super Frame				Super Frame		Unframed	
	Far-End*		Near-End					
	15 Min and Hourly	Daily	15 Min and Hourly	Daily	15 Min and Hourly	Daily	15 Min and Hourly	Daily
Full Time (SWIF2/MUX3 Based) and Camp-on (PMGR Based)								
CVP	53184	132960	53184	132960	6615	16540	-	-
ESP	259	648	259	648	38	95	-	-
BESP	100	600	100	600	19	90	-	-
SESP	40	100	40	100	11	27	-	-
OOFS	-	-	7	17	7	17	-	-
UAS	10	10	10	10	10	10	-	-
SEFS	7	17	-	-	-	-	-	-
CSS‡	7	17	7	17	-	-	-	-
Line (DS1IF Based)								
CVL†	-	-	53360	133400	53360	133400	53360	133400
ESL†	-	-	259	648	259	648	259	648
SESL†	-	-	40	100	40	100	40	100

DM (degraded minutes) is no longer supported as of DACS IV-2000 (256) Release 5.0.

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

† Only applicable for DS1 signals terminating on DS1 Interface Modules.

‡ CSS (Controlled Slipped Seconds) was formerly known as SLS (Slipped Seconds).

Table 14. Default Thresholds for Scan (PMGR Based) DS1 Performance Monitoring

Monitored Parameter	DS1 Framing Format					
	Extended Super Frame				Super Frame	
	Far-End*		Near-End			
	15 Min and Hourly	Daily	15 Min and Hourly	Daily	15 Min and Hourly	Daily
CVP	-	-	1772	4432	177	443
ESP	8	21	8	21	1	3
SESP	1	3	1	3	1	3
OOFS	-	-	1	2	1	2
SEFS	1	2	-	-	-	-

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

Table 15. Threshold Value Ranges for Full-Time, Camp-On, and Line DS1 Performance Monitoring

Monitored Parameter	Far-End*			Near-End		
	15 Min	Hourly	Daily	15 Min	Hourly	Daily
Full Time (SWIF2 Based) and Camp-on (PMGR Based)						
CVP	0-2097152	0-8388608	0-134217728	0-2097152	0-8388608	0-134217728
ESP	0-900	0-3600	0-65535	0-900	0-3600	0-65535
BESP	0-900	0-3600	0-65535	0-900	0-3600	0-65535
SESP	0-900	0-3600	0-65535	0-900	0-3600	0-65535
OOFS	-	-	-	0-900	0-3600	0-65535
UAS	0-900	0-3600	0-65535	0-900	0-3600	0-65535
SEFS	0-900	0-3600	0-65535	-	-	-
CSS[‡]	0-900	0-3600	0-65535	0-900	0-3600	0-65535
Line (DS1IF Based)						
CVL[†]	-	-	-	0-58981500	0-235926000	0-4294967295
ESL[†]	-	-	-	0-900	0-3600	0-65535
SESL[†]	-	-	-	0-900	0-3600	0-65535

DM (degraded minutes) is no longer supported as of DACS IV-2000 (256) Release 5.0.

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

† Only applicable for DS1 signals terminating on DS1Interface Modules.

‡ CSS (Controlled Slipped Seconds) was formerly known as SLS (Slipped Seconds).

Table 16. Threshold Value Ranges for Scan (PMGR Based) DS1 Performance Monitoring

Monitored Parameter	Far-End*			Near-End		
	15 Min	Hourly	Daily	15 Min	Hourly	Daily
CVP *	-	-	-	0-65535	0-65535	0-65535
ESP	0-900	0-3600	0-65535	0-900	0-3600	0-65535
SESP	0-900	0-3600	0-65535	0-900	0-3600	0-65535
OOFS	-	-	-	0-900	0-3600	0-65535
SEFS *	0-900	0-3600	0-65535	-	-	-

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

Maximum Allowable PMGR Circuit Packs

Table 17. Maximum Allowable PMGR Circuit Packs per Interface Module

Interface Module Type	Performance Monitoring Mode	
	Full-Time/Camp-On	Scan
DS3 Interface-32	16	0
	8	1
	2	2
DS3 Interface-16	15	0
	8	1
DS1 Interface	8	0
	7	1/0*
DS1 Interface-Protection	7	0
	6	1/0†

* Zero if there is a SCAN performance monitoring PMGR circuit pack in the associated DS1 Interface-Protection Module.

† Zero if there is a SCAN performance monitoring PMGR circuit pack in the associated DS1 Interface Module.

DS3 Performance Monitoring Parameters

Table 18. Threshold Values for DS3 Performance Monitoring

Parameter	Interval					
	Current 15 Minutes		Current 1 Hour* and Last 24 1-Hour Intervals		Current Day* and Last 7 Days of Daily Totals	
	Default	Range	Default	Range	Default	Range
PSET#1 (CB149)						
Number of Block Errors (BEC)*	4000	0-8458200	-	-	386500	0-811987200
Errored Seconds A (TPA)	30	0-900	-	-	90	0-65535
Errored Seconds B (TPB)	30	0-900	-	-	90	0-65535
Errored Seconds C (TPC)	20	0-900	-	-	60	0-65535
Out-of-Frame Seconds (OOFS)	10	0-900	-	-	30	0-65535
Unavailable Seconds (UAS)	30	0-900	-	-	90	0-65535
PSET#2 (TR820)						
Coding Violations (CVL/CVP)	4000	0-8458200	16100	0-33832800	386500	0-811987200
Errored Seconds (ESL/ESP)	40	0-900	40	0-3600	90	0-65535
Severely Errored Seconds (SESL/SESP)	20	0-900	20	0-3600	60	0-65535
Out-of-Frame Seconds (OOFS)	10	0-900	10	0-3600	30	0-65535
Unavailable Seconds (UAS)	30	0-900	30	0-3600	90	0-65535

* Current hour is the sum of 15-minute intervals beginning on the hour and current day is the sum of hourly intervals beginning at midnight.

SONET Performance Monitoring Parameters

Table 19. STS-1 and VT1.5 Performance Monitored Parameters

Monitored Parameter		STS-1			VT1.5
		Section	Line	Path	Path
Near-End	Severely Errored Frame Seconds (SEFS)	✓	–	–	–
	Loss-of-Signal Seconds (LOSS)	✓	–	–	–
	Coding Violations (CV)	–	✓	✓	✓
	Errored Seconds (ES)	–	✓	✓	✓
	Errored Seconds A (ESA)	–	✓	✓	✓
	Errored Seconds B (ESB)	–	✓	✓	✓
	Severely Errored Seconds (SES)	–	✓	✓	✓
	AIS Seconds (AISS)	–	✓	–	–
	AIS/Loss-of-Pointer Seconds (ALS)	–	–	✓	✓
	Unavailable Seconds (UAS)	–	✓	✓	✓
Far-End	Coding Violations (CV)	–	–	✓	–
	Errored Seconds (ES)	–	–	✓	–
	Errored Seconds A (ESA)	–	–	✓	–
	Errored Seconds B (ESB)	–	–	✓	–
	Severely Errored Seconds (SES)	–	–	✓	–
	Unavailable Seconds (UAS)	–	–	✓	–

Note: ✓ means monitoring is available for the parameter specified.

Table 20. Threshold Values for STS-1 and VT1.5 Performance Monitoring

Parameter Name	Accumulation Interval			
	15 Min		Day	
	Default	Range	Default	Range
STS-1 Section Performance Monitoring Parameters (Near-End)				
SEFS	10	0-900	100	0-86400
LOSS	10	0-900	100	0-86400
STS-1 Path and Line Performance Monitoring Parameters (Near-End)				
CV	4666	0-46660	447900	0-447900
ES	65	0-900	648	0-86400
ESA	65	0-900	648	0-86400
ESB	65	0-900	648	0-86400
SES	10	0-900	100	0-86400
AISS (line only)	10	0-900	100	0-86400
ALS (path only)	10	0-900	100	0-86400
UAS	10	0-900	100	0-86400
STS-1 Path Performance Monitoring Parameters (Far-End)				
CV	4666	0-46660	447900	0-447900
ES	65	0-900	648	0-86400
ESA	65	0-900	648	0-86400
ESB	65	0-900	648	0-86400
SES	10	0-900	100	0-86400
UAS	10	0-900	100	0-86400
VT1.5 Path Performance Monitoring (Near-End)				
CV	156	0-16383	14930	0-1048575
ES	65	0-900	648	0-86400
ESA	65	0-900	648	0-86400
ESB	65	0-900	648	0-86400
SES	10	0-900	100	0-86400
ALS	10	0-900	100	0-86400
UAS	10	0-900	10	0-86400