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1. DIGITAL DATA SYSTEM - GENERAL

This document describes the Bell System Digital Data System (DDS) and the interface between the channel termination equipment of the DDS, contained in a Channel Service Unit (CSU) and the customer's data terminal equipment. There are two sections:

Section 1 - Briefly describes the DDS, introduces the CSU and covers performance objectives, testing and maintenance considerations.

Section 2 - Covers technical details on the channel interface specifications.

1.1 Service Provided

Initially DDS provides two-point*, duplex, private line data transmission at synchronous data rates of 2.4, 4.8, 9.6, or 56 kilobits per second (kb/s). The data rate must be specified in the request for service. No alternate voice or voice coordination is provided. Data transfer to and from the customer must be synchronized with the network clocking system.

1.2 System Description

The DDS shown schematically in Figure 1 is functionally discrete from but physically integrated into the existing Bell System network. This concept allows DDS to share the Bell System's extensive routing flexibility and 24-hour maintenance coverage.

DDS uses the existing and planned hierarchy of digital transmission systems. Cable routes and T1 digital systems are currently deployed in many metropolitan areas. They provide a basic means of distributing service within the network's metropolitan serving areas. In addition, radio and coaxial systems are used to interconnect the various metropolitan areas into a nationwide network.

The end-to-end transmission delay depends largely on the propagation time of signals on these intercity facilities. The delay will generally not exceed 50 ms.

1.2.1 Channel Service Unit (CSU) Interface

The basic customer interface unit for a DDS channel is the CSU. The unit, pictured in Figure 2, provides the ability to quickly and decisively test (remotely from a Telephone Company test center) a DDS channel up to the point of interface with the customer. The CSU is essential for this purpose and contains the minimum amount of hardware required.

A six-wire interface permits the customer to connect his data communication equipment to a DDS channel. When interfaced with the CSU, the cus-

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* A multipoint service is also planned to be available using the same interface arrangements as two-point service. This Technical Reference will be modified as required to describe multipoint service.

tomer's equipment must perform the following functions:

1. Proper coding and decoding of signals
2. Timing recovery
3. Synchronous sampling
4. Formatting
5. Generation and recognition of control signals

The specifications for these functions are contained in Section 2 of this Technical Reference.

1.2.2 Data Service Unit (DSU) Interface

The Bell System also provides a unit that performs the functions listed above. This Data Service Unit (DSU) is described in the Technical Reference, "Digital Data System - Data Service Unit Interface Specifications" (PUB 41450). The DSU includes the functions of the CSU along with the additional circuitry to provide an EIA RS-232-C interface at the subrate speeds of 2.4, 4.8 and 9.6 kb/s. At the 56 kb/s rate, the interface conforms with CCITT Recommendation V.35.

1.2.3 Office Channel Unit (OCU)

The DSU (or CSU working in conjunction with customer-provided equipment) transmits data over cable pairs to a DDS office. In the office, this local loop is terminated by an Office Channel Unit (OCU). Four OCU speeds are available to match the four customer speeds. The functions of the OCU are to

1. Transmit outgoing loop signals to the station
2. Reshape, retime and regenerate incoming loop signals
3. Assemble the data into a format suitable for multiplexing
4. Transmit and detect control signals with bipolar violations (see Section 2)

1.2.4 Time-Division Multiplexers

The DDS uses synchronous time-division multiplexing to pack the data for efficient transmission between DDS offices. Figure 1 shows two stages of multiplexing.

One multiplexing stage combines channels at the subrate speeds of 9.6, 4.8 and 2.4 kb/s.

The 56 kb/s speed is fed directly to another synchronous time-division multiplexing stage. This multiplexing stage can combine data streams from customers and/or the subrate multiplexer mentioned above.

The same structure as described above is used to demultiplex the streams, with each of the equipment pieces performing the reverse of the function it performs in the multiplexing process. Since this is a duplex system, (it has independent paths for both directions of transmission) multiplexing and demultiplexing take place simultaneously.

1.2.5 Network Synchronization

A timing control network is employed in the DDS to ensure that data signals are synchronous. This means that sampling takes place at the same frequency throughout the network.

The synchronous timing control for the network is derived from a single master supply. The timing is distributed to each digital equipment location through a treelike timing network. This network is an important part of the Digital Data System. The timing supplies provide timing for the data multiplexers, office channel units, and other office terminals. Timing is transmitted to the station by means of the bipolar bit stream which has a sufficient number of pulses to permit timing recovery.

The timing system is designed so that phase jitter and phase hits do not propagate through the network. If branches of the timing tree become severed, the individual timing supplies continue without interruption.

1.3 Design Objectives, System Tests and Maintenance Considerations

The Digital Data System is intended to provide an excellent communications medium for the transfer of digital data between customer terminals. This leads to a set of design objectives which are aimed at the primary concerns that a data customer has about the communications channel which he uses.

Overall performance will depend on the characteristics of data communications equipment that is provided and maintained by the customer as well as those of the DDS. The quantitative objectives listed below apply to the DDS exclusively.

1.3.1 Design Objectives

The following are <u>preliminary design objectives only</u> and are <u>not</u> to be construed as minimum performance guarantees. The objectives are subject to change as experience with the DDS dictates.

Quality - To average at least 99.5% error-free seconds at 56 kb/s and better performance at the lower rates of 9.6, 4.8, and 2.4 kb/s.

Availability - To average at least 99.96% channel availability, i.e., annual downtime less than 0.04%. It should be noted that this average is that value which would be observed over a period of several years. Some of the causes of downtime are failures which occur infrequently but which may have long outages associated with them when they do occur. While these infrequent long outages represent small contributions to the long-term average, they may significantly affect the downtime seen in a shorter period of time (even as long as a year.)

1.3.2 Testing and Maintenance

Testing and maintenance features are an integral part of the DDS. Centralized test centers, as shown in Figure 3, can conduct tests with both ends of each circuit in their area. These features permit rapid isolation and correction of trouble conditions. The Telephone Company will be aware of most trouble conditions that occur in the DDS, and repair will be undertaken prior to reports from customers. If the customer suspects an undetected trouble condition in his DDS channel, he should call the number for trouble reporting that is furnished when the channel is installed. A customer operating procedure that provides indications of specific problems (e.g., no signal, first bit in error, etc.) on the communications channel is a great aid in expediting repairs. It is expected that the reporting customer will assist in analysis of the trouble. It is also expected that the customer will check his terminal equipment for proper operation prior to calling the Telephone Company.

In the event of trouble the Telephone Company will test the DDS channel. Such tests require the brief removal of customer data. These tests should be infrequent and short, but it is essential to good service that the DDS user be willing to release his channel when testing is required. Of course, the Telephone Company will not intentionally disturb the channel without first receiving permission to test from the user.

1.3.3 Remote Testing

Most tests of a DDS channel will not require a visit to the user's premises. Remote tests of the DDS channel are under the control of a test center. They can remotely loop back the channel at the user's premises permitting the Telephone Company to evaluate overall operation.

1.3.4 Trouble Conditions

Where there is a failure in the higher order digital facilities, a repetitive Out-of-Service sequence (see Part 2.2.2) is sent to the customer equipment. A failure on the local cable pair that carries signals from the OCU to the customer's location is not detected by the DDS. However, the customer's equipment can detect local loop failure by an absence or distortion of digital signals. If there is a failure on the cable pair that is carrying signals to the OCU, the DDS equipment at the central office detects this condition and transmits the repetitive Idle sequence (see Part 2.2.1) to the far-end terminal. This same sequence results when no pulses are being transmitted. Therefore, if a terminal receives this Idle sequence when it expects to receive data, the user should check his far-end transmitting equipment. If the Idle sequence is received when the far-end is transmitting data, the user should report this to the Telephone Company.

2. INTERFACE DESIGN CONSIDERATIONS

This section is directed to those who use the channel interface provided by the CSU described in Part 1.2.1. For the DSU interface described in Part 1.2.2, refer to the Technical Reference, "Digital Data System - Data Service Unit Interface Specifications" (PUB 41450).

Detailed specifications for transmission using the DDS are discussed in this section. Included are the encoding and decoding requirements that the customer's equipment must observe in order to operate over a DDS channel equipped with CSUs. If a customer chooses to use DSUs, these requirements are met by circuitry within the DSU. In such cases the following material merely provides background information about the DDS.

2.1 Transmission Plan

Baseband, bipolar return-to-zero signaling is used for transmission over the local loop and is described by the following coding rules: A binary 0 is transmitted as zero volts. A binary 1 is transmitted as either a positive or negative pulse, opposite in polarity to the previous 1. An example of bipolar signaling is shown in Figure 4.

Through the use of bipolar violations, additional information capacity is achieved to provide a convenient way of transmitting network control information. A bipolar violation occurs when the alternate polarity rule is violated. For example, the bipolar rule is violated if the last 1 was transmitted as a positive pulse, and the next 1 is also transmitted as a positive pulse. Using the following notations, Figure 5 shows a typical bipolar sequence containing bipolar violations.

- 0 - denotes zero volts transmitted
- B - denotes $\pm$E volts (polarity determined by bipolar rule)
- V - denotes $\pm$E volts (polarity in violation of bipolar rule)

2.2 Encoding and Decoding Rules

To be compatible with the DDS, the transmit and receive data signals must use bipolar violations to indicate control information (Idle and Out-of-Service) and Zero Suppression. The Zero Suppression sequence is necessary since long sequences of zeros do not provide the transitions necessary to maintain timing recovery. The encoding and decoding rules that the customer must follow are outlined below. The notation is the same as in Part 2.1 with the following addition.

Unrestricted insertion of violations in the pulse stream would produce an undesirable dc component. A means of solving this problem is to reserve a time slot prior to a violation for application of a binary pulse or no-pulse in such a way that successive violations (V) alternate in polarity. The reserved time slot is designated by the symbol X. The desired polarity alternation of Vs is achieved by assigning a value 0 or B to the X such that the total number of Bs since the last V is odd.

If pulses of the same polarity were adjacent, performance would have been degraded. Therefore, X and V bits are separated by a ZERO, resulting in an XOV pattern in each bipolar violation sequence.

2.2.1 Transmitting Sequences Containing Bipolar Violations

1. Idle Sequence - This sequence may be used as a supervisory signal. For example, it could indicate that the terminal

does not have data to transmit. Such usage is analogous to the Request-to-Send OFF indication in EIA Standard RS-232-C. The Idle sequence consists of one or more repetitions of the sequence BBBXOV at 2.4, 4.8, or 9.6 kb/s or BBBBXOV at 56 kb/s. (See Figure 6.)

2. Zero Suppression Sequence - At 2.4, 4.8, or 9.6 kb/s any sequence of 6 consecutive 0s must be encoded as 000XOV; at 56 kb/s, any sequence of 7 consecutive 0s must be encoded as 0000XOV. (See Figure 7.)

2.2.2 Receiving Sequences Containing Bipolar Violations

1. Idle Sequence - This is the same as the transmitting Idle sequence described above. (See Figure 6.)

2. Zero Suppression Sequence - Reception of 000XOV for any speed must be decoded as 6 0s. (See Figure 7.)

3. Out-of-Service Sequence - This sequence is an indication of trouble in the DDS. It consists of one or more repetitions of the sequence 00BXOV at 2.4, 4.8, or 9.6 kb/s or 000BXOV at 56 kb/s. (See Figure 8.)

2.2.3 System Response to Bipolar Violation Sequences

A single bit transmission error could change a data sequence into a bipolar violation sequence. This would not be particularly serious if data were changed to the Zero Suppression sequence. One or two errors would be the result. However, if data were changed to the Idle sequence or Out-of-Service sequence, it could seriously affect the operation of data terminal equipment unless spurious occurances of these sequences are ignored.

The design of the logic circuitry associated with the coding and decoding functions in the data communication equipment can reduce the effect of short bursts of errors. For example, the Bell System Data Service Unit (DSU) requires three repetitions of the Idle or Out-of-Service sequences before detecting these conditions and turning OFF the Received Line Signal Detector (CF) lead. To turn ON this lead the DSU must receive 12 bits (2.4, 4.8, or 9.6 kb/s) or 14 bits (56 kb/s) of data containing neither Idle nor Out-of-Service sequences.

The customer's data terminal may transmit Idle sequences through a DDS channel for supervisory signaling purposes. The transmission delay will not necessarily be the same for Idle sequences as for data. This difference in delay may cause signals to be modified when going between the Idle and data modes. The transition from data to Idle adds a number of pulses between the last data bit and the first pulse of the Idle sequence. The transition from Idle to data will replace the same number of the initial data bits with the bits of the Idle sequence. The additional delay for Idle sequences will be less than six bits at 2.4, 4.8 and 9.6 kb/s. At 56 kb/s the additional delay will be less than seven bits.

It is important to note that a Zero Suppression sequence may not be received when one was transmitted and vice versa. If a Zero Suppression sequence follows a B00000 data sequence, then the received data could have ten consecutive zeros.

2.2.4 Other Bipolar Violation Sequences

The Idle and Zero Suppression sequences from the data communication equipment at the customer's location are detected at the Telephone Company central office and are transmitted to the distant central office with a signal format that does not involve bipolar violations. At the distant central office the bipolar violations are inserted in the pulse train that is transmitted to the customer's location in accordance with the data alignment within the time-division multiplexer bit stream which does not necessarily correspond to their original placement. Bipolar violation sequences other than those specified will reach the distant end as bipolar pulses (B) rather than bipolar violations (V).

2.3 CSU Block Diagram

A simplified block diagram of the CSU is shown in Figure 9. Nominal 50 percent duty-cycle, bipolar pulses are accepted from the customer on the Transmitted Data leads DT and DR. These pulses must be synchronous with the DDS and must comply with the specifications listed in Section 2.7. The input bipolar pulses are amplified, filtered, and passed through the transmit repeat coil to the transmit pair.

The signal on the receive pair is amplified, equalized and sliced by the line receiver. The resultant bipolar pulses are then passed to the customer over the DT1 and DR1 Received Data leads. From these pulses the customer must recover the synchronous clock used for timing the transmitted data and sampling the received data.

2.4 CSU Physical Description

The CSU, shown in Figure 2, is designed for wall mounting. It measures approximately five inches high, 2-3/4 inches deep, and eight inches wide. Visible through the face of the housing are two lights to indicate

1. PWR - when ac power is applied to the unit.

2. TST - when the unit is being remotely tested from the test center.

The CSU will operate over a temperature range of +40°F to +120°F with a relative humidity less than 95 percent. The CSU weighs approximately 3 pounds.

Power is furnished to the CSU from a customer-provided 105-129 volt, 60 ±3 Hz, nonswitched source by means of a 3-foot cord with a U-ground type 3-conductor plug. The CSU consumes approximately 10 watts of ac power. The CSU should be located so that the customer-provided interface cable from the CSU to the data terminal will not exceed 100 feet. (See Part 2.5.2).

2.5 CSU Interface Circuits

The interface discussed in this Technical Reference is the point of connection between the CSU of the DDS and the customer-provided terminal equipment. The interface that is provided consists of six leads: two pairs for data, a ground (normally connected to the power ground but may be optionally disconnected), and a Status Indicator lead.

As shown in Figure 9, leads DT and DR are the Transmitted Data pair, and leads DT1 and DR1 are the Received Data pair. The electrical characteristics of these leads are significantly different from those described in RS-232-C. For this reason, Parts 2.7.1 through 2.7.13 in this Technical Reference cover the standards for the data interchange signals. This is the first time these interface characteristics have been used. The parameters and specifications will be reexamined as user experience is acquired. In this light, the specifications should be considered as preliminary.

The Status Indicator (SI) lead conforms electrically to EIA Standard RS-232-C. It is analogous to Data Set Ready (CC) described in RS-232-C. When Circuit SI is ON, (voltage to ground between +3 and +25 volts), the local CSU is connected to ac power and is not in a test mode. Ground return for this circuit is normally connected within the CSU to the power plug ground. It may be disconnected at the customer's request. The short circuit current on the SI lead is limited to 20 mA. The ON condition should not be interpreted as either an indication that a communication channel has been established to a remote data station or the status of any remote station equipment. The OFF condition (voltage between -3 and -25 volts) is an indication that the data terminal equipment should disregard signals appearing on the Received Data Circuit and should not attempt to transmit data over the Transmitted Data Circuit.

2.5.1 Interface Connector

The six leads are provided on a 15-pin female connector. The customer-provided plug must be a male 15-pin connector such as the DAMA-15-P plug manufactured by Cinch, or the equivalent. The pin assignments for the connector are given below.

Pin Number	Function	Signal Direction
1	Ground (GRD)	-
2	Status Indicator (SI)	From CSU to Customer
3	Received Data (DT1)	From CSU to Customer
4	Received Data (DR1)	
5	Transmitted Data (DT)	From Customer to CSU
6	Transmitted Data (DR)	
7-15	Not Used	-

2.5.2 Interface Cable Requirements

The cable from the data terminal equipment to the CSU requires three twisted pairs. One twisted pair should be used for DT and DR, one pair for DT1 and DR1 and one pair for SI and GRD. To reduce the possibility of crosstalk between the various leads and assure proper operations, the following recommendations are made regarding the cable parameters.

Gauge	24 AWG
Characteristic Impedance of Pair	120 ohms ± 10% at 150 kHz 100 ohms ± 10% above 400 kHz
Mutual Capacitance of Pair	1600 pF/100 feet ± 20%
Capacitance of Single Lead to Ground - all other leads grounded	4000 pF/100 feet maximum
Crosstalk Loss - Pair-to-Pair	40 dB minimum at 150 kHz

2.6 Data Interchange Circuits - Introduction

The CSU is transformer coupled to the data interface leads. This interface is designed to be compatible with a wide variety of drivers and terminators in the user's equipment. Transformer coupling causes the CSU input and output impedances to be frequency dependent. It also means that the CSU neither responds to nor transmits dc voltages.

The interface specifications describe pulse characteristics when the drivers in the CSU and in the customer equipment are terminated with a 135-ohm resistance. To describe the opposite direction of transmission, the characteristics of pulses from a source having an internal impedance of 135-ohms, resistive, are used. That is, the terminators in the CSU and in the customer equipment are described by specifying the shape of pulses from a 135-ohm resistive source of pulses. Figure 10 shows two possible schematic diagrams for interface cable terminators in the customers data equipment. Figure 11 shows two possible interface cable drivers.

2.7 Definitions and Limiting Specifications

In this Part, various terms and parameters used to specify the data interchange circuits are introduced, defined and illustrated. Following the definition, the limiting specification is stated along with any explanatory comments.

2.7.1 Output Voltage (V_{out})

Definition: Figure 12 shows the output voltage measured between leads A and B (V_{out}).

Specification: The transmission of a binary ONE or ZERO shall be indicated by the following differential ac output voltages measured across a 135-ohm resistive termination.

1. Customer Generator

   ONE $1.4 \text{ volts} \leq |V_{out}| \leq 2.1 \text{ volts}$

   ZERO $|V_{out}| \leq 0.14 \text{ volts}$

2. CSU Generator

   ONE $1.33 \text{ volts} \leq |V_{out}| \leq 2.1 \text{ volts}$

   ZERO $|V_{out}| \leq 0.21 \text{ volts}$

   Where $|V_{out}|$ denotes the absolute value.

These requirements are illustrated in Figure 13.

The differential dc output voltage of the customer generator shall not exceed 25% of the peak-to-peak ac signal. The differential dc output voltage of the CSU will be zero.

Comment: Greater tolerance on the CSU output voltage limits reflects the fact that data signals are not retimed in the CSU. Some conversion of time to amplitude distortion may be expected.

2.7.2 Terminator Threshold Voltage (V_{in})

Definition: Figure 14 shows the differential ac input pulse amplitudes (V_{in}) that a terminating system will interpret as a binary ONE or ZERO when driven by a generator meeting the specifications in this Section.

The threshold levels are said to be normalized when referred to the equivalent amplitude obtained at the input of a terminator having a 135-ohm resistive input impedance.

Specification: The following normalized input voltages apply to both the customer terminator and the CSU.

ONE	$\lvert V_{in} \rvert \geq$ 1.05 volts
Undefined	0.35 volts $< \lvert V_{in} \rvert <$ 1.05 volts
ZERO	$\lvert V_{in} \rvert \leq$ 0.35 volts

Where $\lvert V_{in} \rvert$ denotes the absolute value.

These requirements are illustrated in Figure 14.

2.7.3 Rise and Fall Times (T_R, T_F)

Definition: Figure 15 shows the rise and fall times of the leading and trailing edges of a pulse.

Specification: The time (T_R, T_F) required for a generator to indicate a change in its binary state shall not exceed 5% of a bit interval. This is measured when the generator is terminated with a 135-ohm resistive load.

Comment: The rise and fall times shown on Figure 15 are exaggerated for additional clarity.

2.7.4 Pulse Width (W)

Definition: Figure 15 shows the pulse width at the nominal threshold level.

Specification:

1. Customer to CSU - The pulse width, measured across a 135-ohm resistance at the generator terminals, shall be 50% ± 2.5% of the bit interval at the nominal terminator threshold levels of ± 0.7 volts.

2. CSU to Customer - The average pulse width, measured across a 135-ohm resistance at the generator terminals, will be greater than 45% and less than 90% of the bit interval at the nominal terminator threshold levels of ± 0.7 volts.

Comment: The CSU to customer specification reflects the fact that data signals are not retimed in the CSU. Random noise introduced in the cable pairs could cause data transitions anywhere within the bit interval. The specification covers pulse widths in the absence of random noise or when the received signal is averaged over many bit intervals.

2.7.5 Differential Impedance (Z_{in}, Z_{out})

Definition: Figure 12 shows the points where the effective impedances (Z_{in}, Z_{out}) are measured. Figure 16 outlines a method for determining the impedance.

Specification: The following impedances apply to interface generators and terminators that are operating at the given bit rate and with the nominal signal levels and duty-cycle specified in this Section. As shown in Figure 16, the impedance during the rise and fall intervals is not specified.

1. Generator - When transmitting a bipolar pulse train into a resistive load, Z_{out} shall be 135 ohms ±20%.

2. Terminator - When receiving a bipolar pulse train transmitted by a resistive source, Z_{in} shall be 135 ohms ±50%.

Comment: When the CSU is in the test mode (see Part 1.3.3), interface leads DT, DR, DT1 and DR1 will be open-circuited and disconnected from the DDS channel.

2.7.6 Longitudinal (Common Mode) Noise

Definition: Noise currents and voltages may be introduced along the interface cable. If they cause an equal change in the potential of terminal A and of terminal B (Figure 17) with respect to ground, they are called longitudinal noise sources.

2.7.7 Common Mode Impedance (Z_{CM})

Definition: Refer to Figure 17 for common mode impedance and voltage illustrations. The impedance to ground with the A and B terminals shorted together is the common mode impedance, Z_{CM}.

Specification: None

Comment: Since the CSU is coupled to the interface cable through a balanced, ungrounded transformer, it is expected that longitudinal noise current effects will be negligible. Consequently, Z_{CM} of the customer generator or terminator may be chosen relatively low (about 135/4 or 34 ohms) to minimize interference caused by capacitive coupling of stray signals.

2.7.8 Common Mode Voltage (V_{CM})

Definition: As shown in Figure 17(b), this is the arithmetic mean of the voltage on terminals A and B measured with respect to ground.

Specification: These specifications are based on measurements between ground and the midpoint of a 135-ohm resistive termination. The common mode output voltage must satisfy the following limits:

1. Customer generator or terminator to CSU

   (a) The dc component of V_{CM} shall be between +5.5 volts and -5.5 volts.

   (b) The peak ac component of V_{CM} shall not exceed the limits shown on Figure 17(c).

2. CSU to customer generator or terminator

   Not specified

Comment: The CSU may impress a common mode signal at the interface during instants of transition between binary states as a result of nonideal characteristics in the interface transformers. However, this signal is associated with the high common mode impedance of an ungrounded transformer and will be negligible relative to the differential signal power.

2.7.9 V_{CM} Input Voltage Range

Definition: This characteristic describes the voltage range through which V_{CM} may be varied without causing improper operation of a generator or terminator. That is, no change in binary state is caused, and the driver or terminator continues to meet all interface specifications.

Specification: A generator or terminator shall continue to operate satisfactorily when connected to the test source illustrated in Figure 18(a). This source has the pulse amplitude and impedance characteristics indicated in Figure 18(c). It produces a pulse train at the given bit rate.

Comment: This specification permits a comparison of generators and terminators that is independent of their common mode impedances. Comparison is on the basis of their ability to withstand longitudinal noise of equal available power.

2.7.10 Impedance Balance

Definitions: As shown in Figure 19, this quantity is an expression of the difference in the impedance from terminal A to ground (Z_A) and the impedance from terminal B to ground (Z_B). The balance is measured indirectly by means of the test shown in Figure 19.

Specification: When driven by a sinusoidal test source, the ratio of applied common mode voltage (V_T) to differential voltage (V) shall not be greater than the values shown on Figure 19. For example at 4.8 kb/s, the impedance balance must be greater than 40 dB at 9.6 kHz and greater than 20 dB at 96 kHz.

2.7.11 Terminator Bias Current

Definition: This is the short-circuit dc current flow when the terminator leads are connected together.

Specification:

1. CSU generator to customer terminator - 0.1 mA

2. Customer generator to CSU terminator - Not specified

Comment: Since a transformer is used as the output device from the CSU, dc current flow from DT1 to DR1 must be limited to avoid distortion of the data signals. The input transformer in the CSU has a series capacitor at the midpoint of its primary winding. This blocks any bias current from flowing.

2.7.12 Protection

Specification: The difference in ground potential between the CSU and the customer's terminal equipment shall not exceed a peak value of 1.0 volt. Under conditions of worst-case ground potential difference, the short-circuit current to ground from the customer's generator or terminator shall not exceed 120 mA.

The circuits used in this interface shall not be damaged by a short circuit between the balanced data leads or by a short circuit from either lead to ground or to the Status Indicator lead. The circuits shall not be damaged under open-circuit conditions.

Comment: Protection under conditions of accidental contact with other voltages or circuits is not specified, and circuit damage may result. The user is cautioned not to mix the interface leads with other circuits in the same cable.

2.7.13 Timing Accuracy

Definition: This term describes the difference between the frequency of the received pulses and the nominal data rate.

Specification:

1. Customer to CSU - The transmitted data shall be synchronous with the received data.

2. CSU to Customer - Under normal conditions, the frequency of the received data will agree with the nominal data rate to within ±2 parts in 10^9. Some trouble conditions will allow the frequency difference to vary ±0.005% of the nominal data rate.

2.7.14 Minimum Average Pulse Density

Definition: The average pulse density of a sequence is the total number of non-zero pulses (Bs or Vs) divided by the sequence length.

Specification:

1. Customer to CSU: The Zero Suppression encoding rule given in Part 2.2.1 guarantees that the customer will deliver to the CSU a minimum average pulse density of 1 in 6 (at 2.4, 4.8 and 9.6 kb/s) or 1 in 7 (at 56 kb/s.)

2. CSU to Customer: The rule controlling the generation of Zero Suppression codes in the pulse stream from the CSU to the customer differs somewhat from that given in Part 2.2.1. Specifically, the Zero Suppression sequences are always generated in alignment with blocks of 6 (at 2.4, 4.8 and 9.6 kb/s) or 7 (at 56 kb/s) bits of data passed from the multiplexer to the OCU. The effect of this is to increase the maximum number of successive zeros which may appear to 10 (at 2.4, 4.8 and 9.6 kb/s) or 11 (at 56 kb/s) bits, but to maintain a minimum average pulse density of 1 in 6 (or 7.)

Comment: The problems of timing, phase detection and received level control are strongly dependent on the minimum average pulse density. The rule for customer to CSU Zero Suppression given in Part 2.2.1 provides a simple method for meeting this requirement.

2.7.15 Isochronous and Peak Individual Distortion (Jitter)

Definition: (See Appendix)

1. Customer to CSU:

   Specification: The peak individual distortion of the data signals from the customer to the CSU shall not exceed 5% of a bit interval relative to a reference clock in phase with the mean of the significant transitions when receiving random data from a CSU having the distortion characteristics shown in Figure 20 (d).

   The isochronous distortion of data signals from the customer to the CSU shall not exceed 10% of a bit interval when receiving random data or periodic patterns from the CSU.

   Comment: A maximum jitter bandwidth for the customer's timing recovery circuit is estimated conservatively at 0.01% to 0.05% of the signaling frequency* (bit rate).

*See Appendix

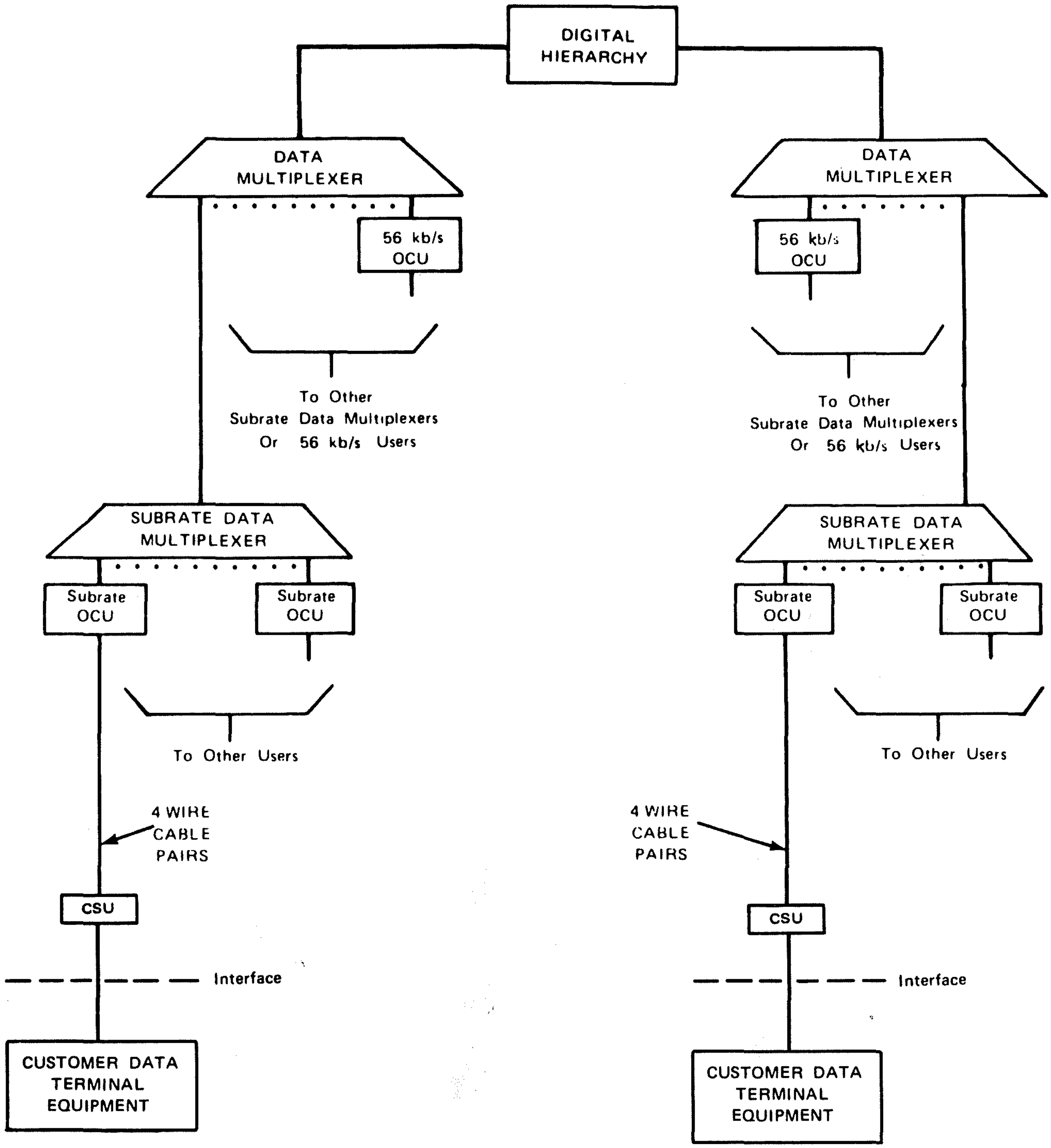
2. DSU to Customer:

Comment: Signals transmitted from the central office to the customer location are not retimed in the CSU. Consequently, the effects of random noise, intersymbol interference and data pattern variations may cause data transitions to occur anywhere within the unit signaling interval. However, it is expected that intersymbol interference and pattern variations will be dominant in establishing the average statistics of the received data signal.

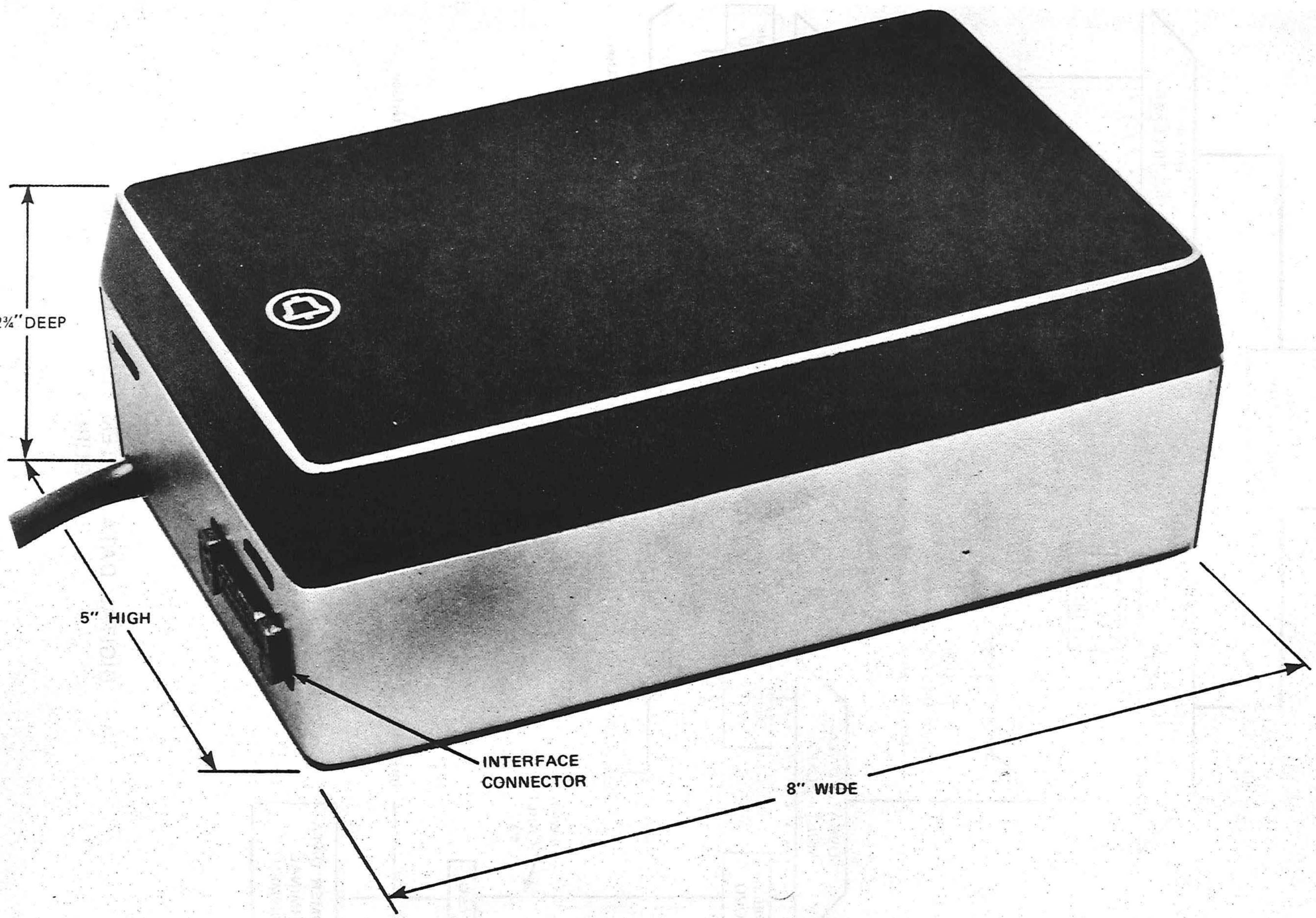
Measurements in the absence of noise indicate that a bipolar eye diagram as shown in Figure 20 (d) may be obtained under worst-case conditions. This corresponds to 27.5% isochronous distortion (also called peak-to-peak jitter) of the leading and trailing pulse edges. This measurement would be taken at the nominal threshold levels of ±0.7 volts with a 135-ohm resistive termination.

The phase difference between the average pulse centers (midpoint of the ±0.7-volt transitions) of any two repetitive patterns is not expected to exceed 7.5% of a bit interval.*

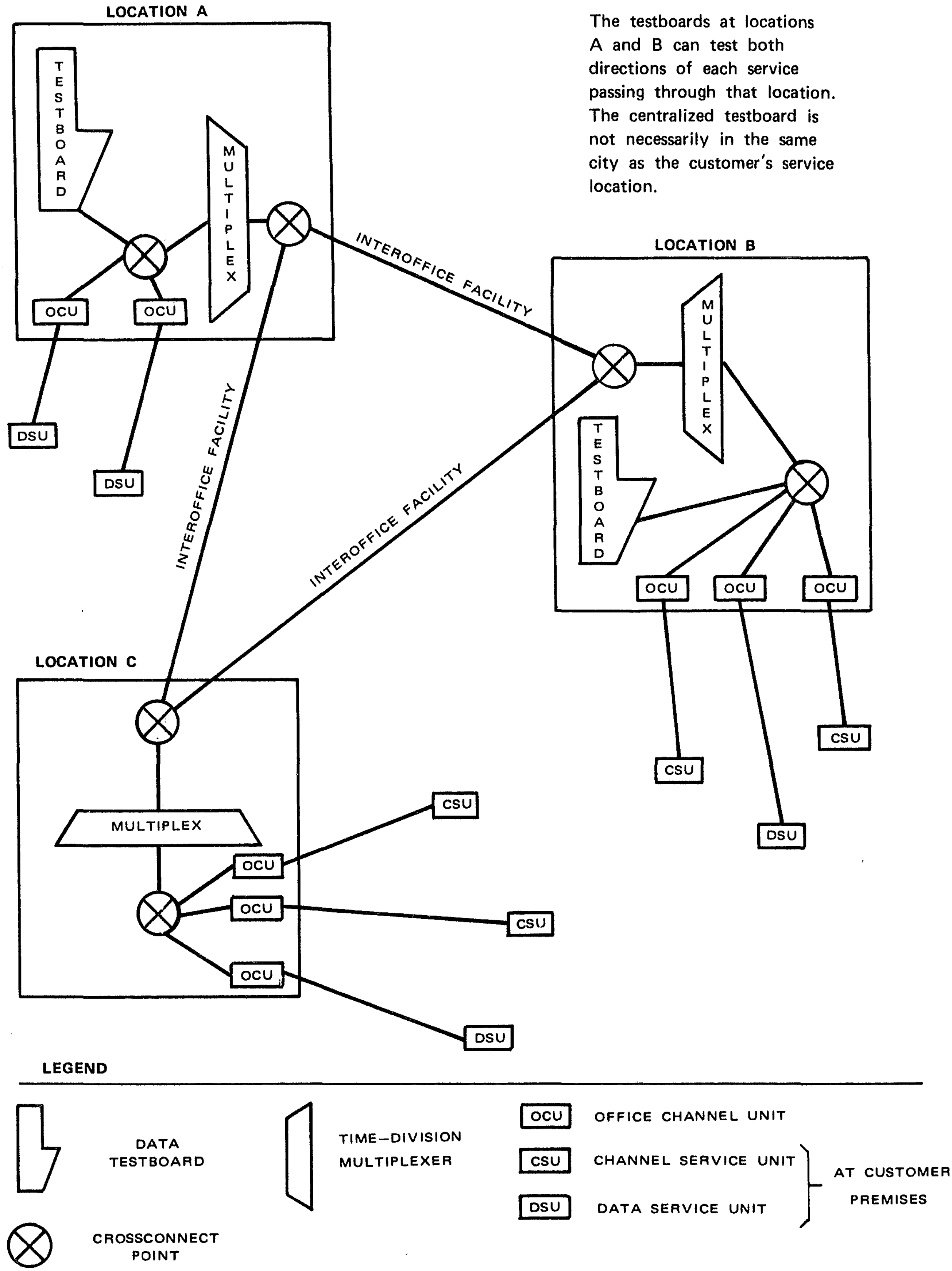
*See Appendix



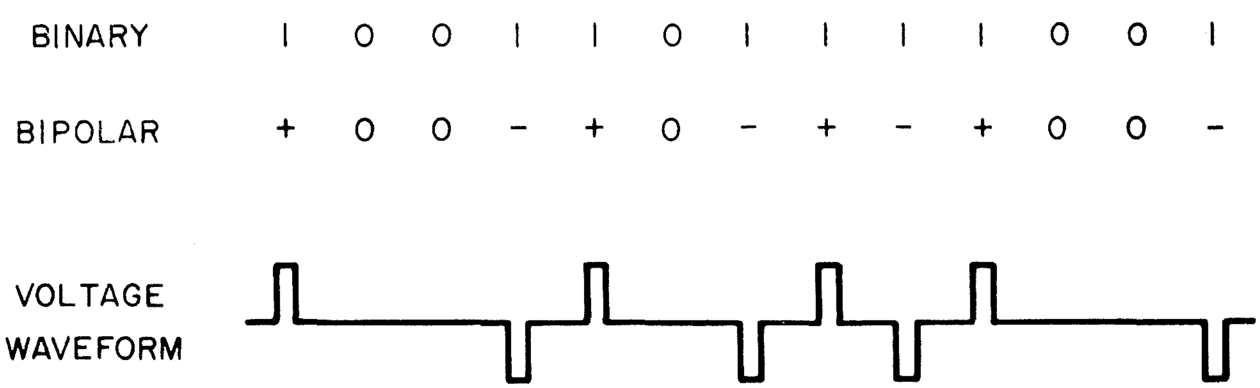
DIGITAL DATA SYSTEM BLOCK DIAGRAM
FIGURE 1



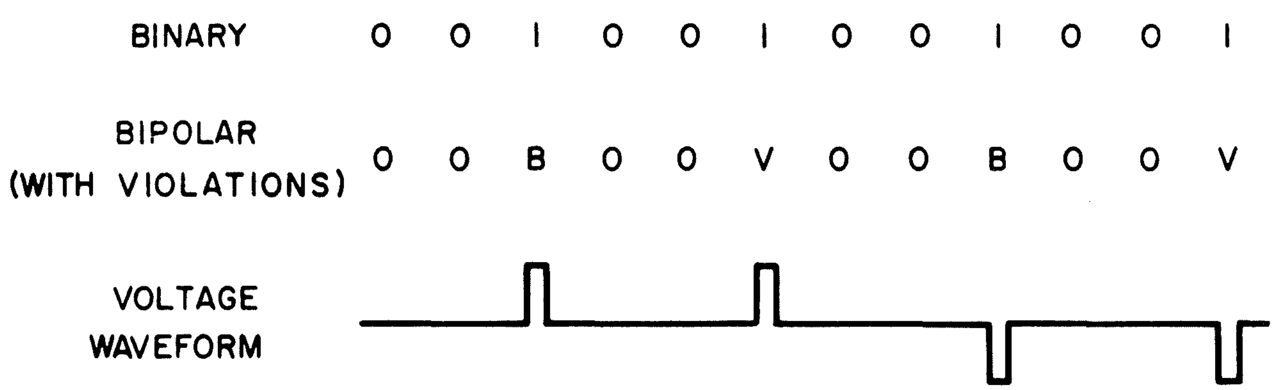
CHANNEL SERVICE UNIT
FIGURE 2



CENTRALIZED TEST CENTERS
FIGURE 3

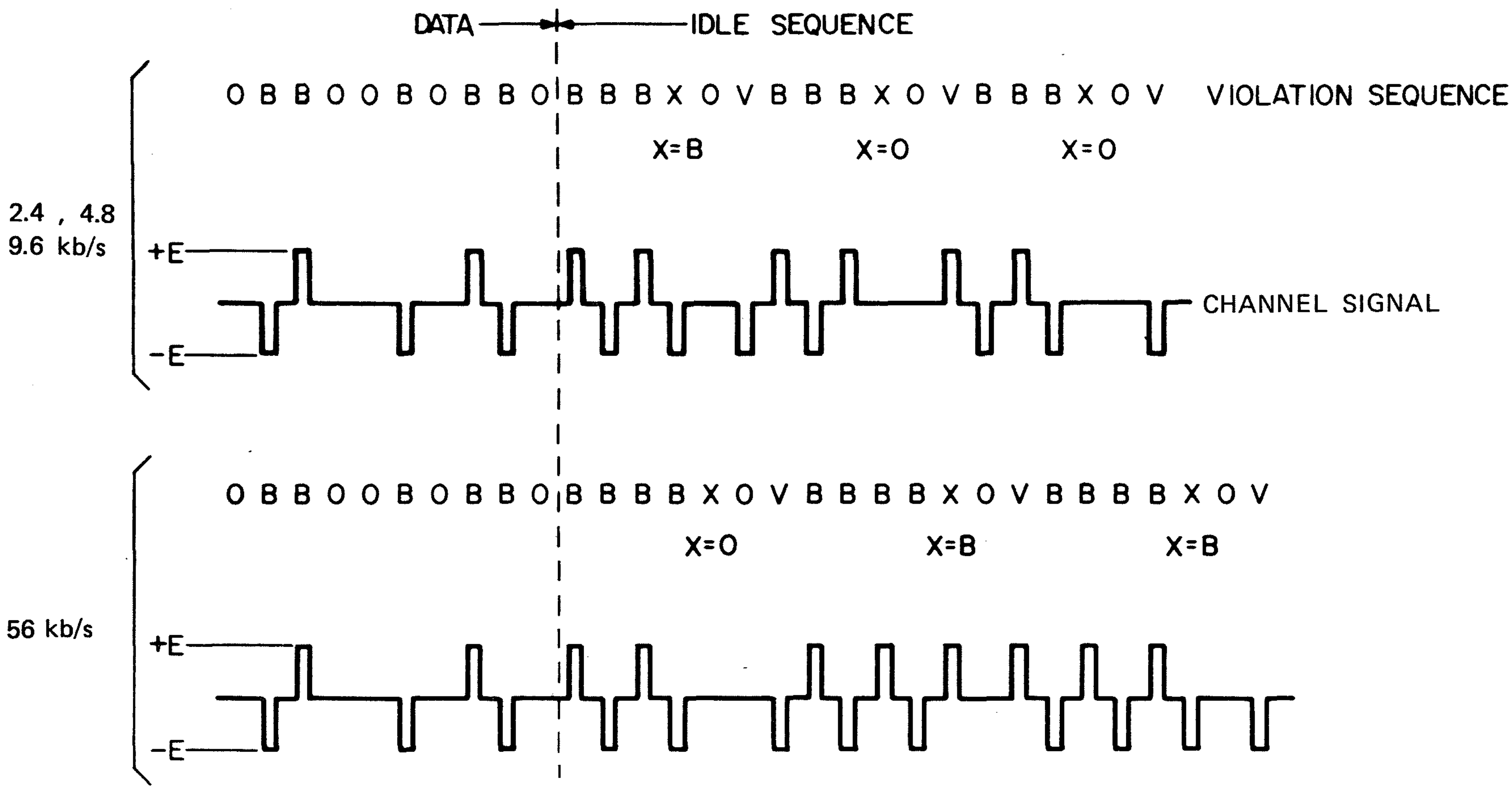


BIPOLAR SEQUENCES
FIGURE 4



BIPOLAR VIOLATION SEQUENCES

FIGURE 5

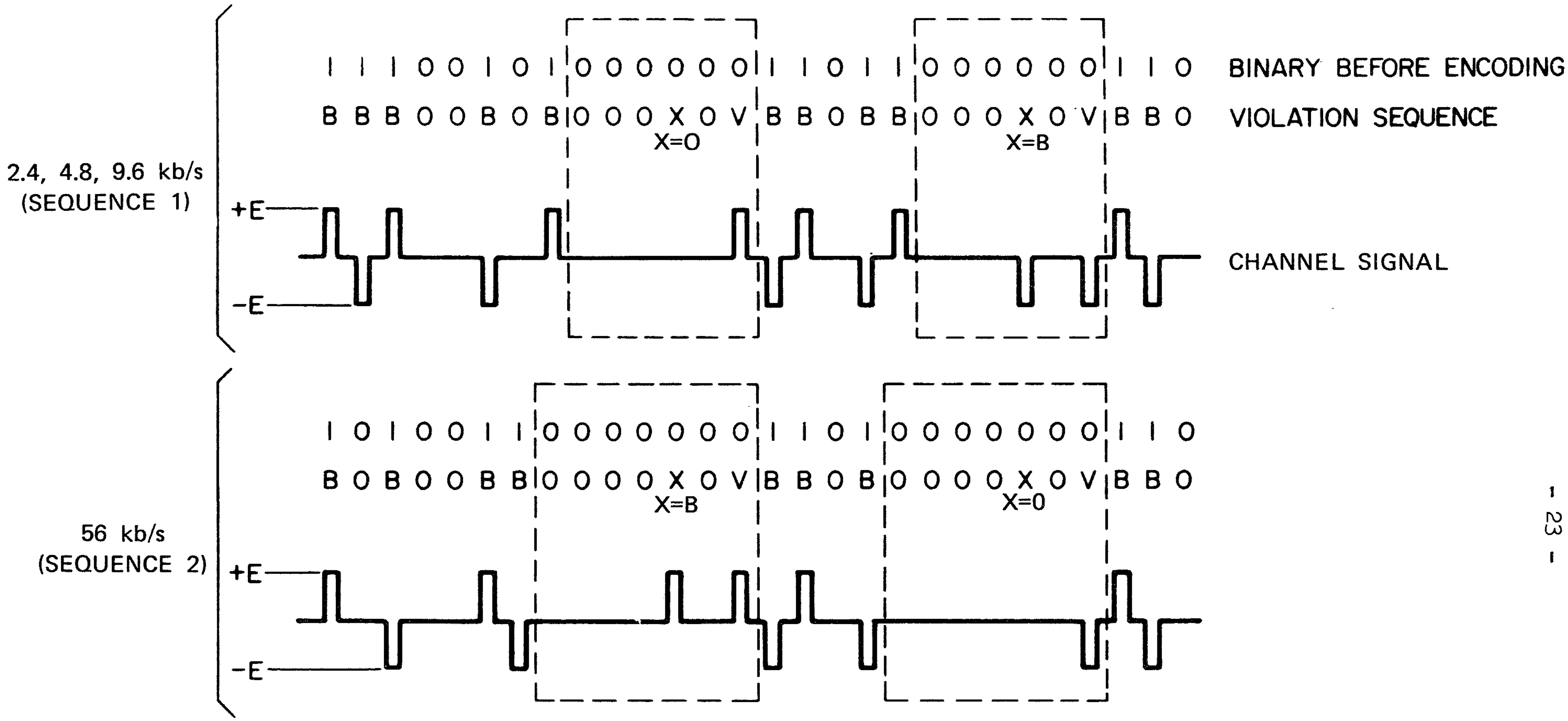


NOTE:

O	Denotes Zero Volts Transmitted — Binary Zero
B	Denotes ±E Volts Transmitted (Polarity Determined by Bipolar Rule) —Binary One
V	Denotes ±E Volts Transmitted (Polarity in Violation of Bipolar Rule) —Binary One
X	Equals O or B if Number of Bs Since Last V is Odd or Even, Respectively in Above Example the First X Equals O or B and the Remaining Xs Equal 0 for 2.4, 4.8 and 9.6 kb/s and B for 56 kb/s.

IDLE SEQUENCE

FIGURE 6

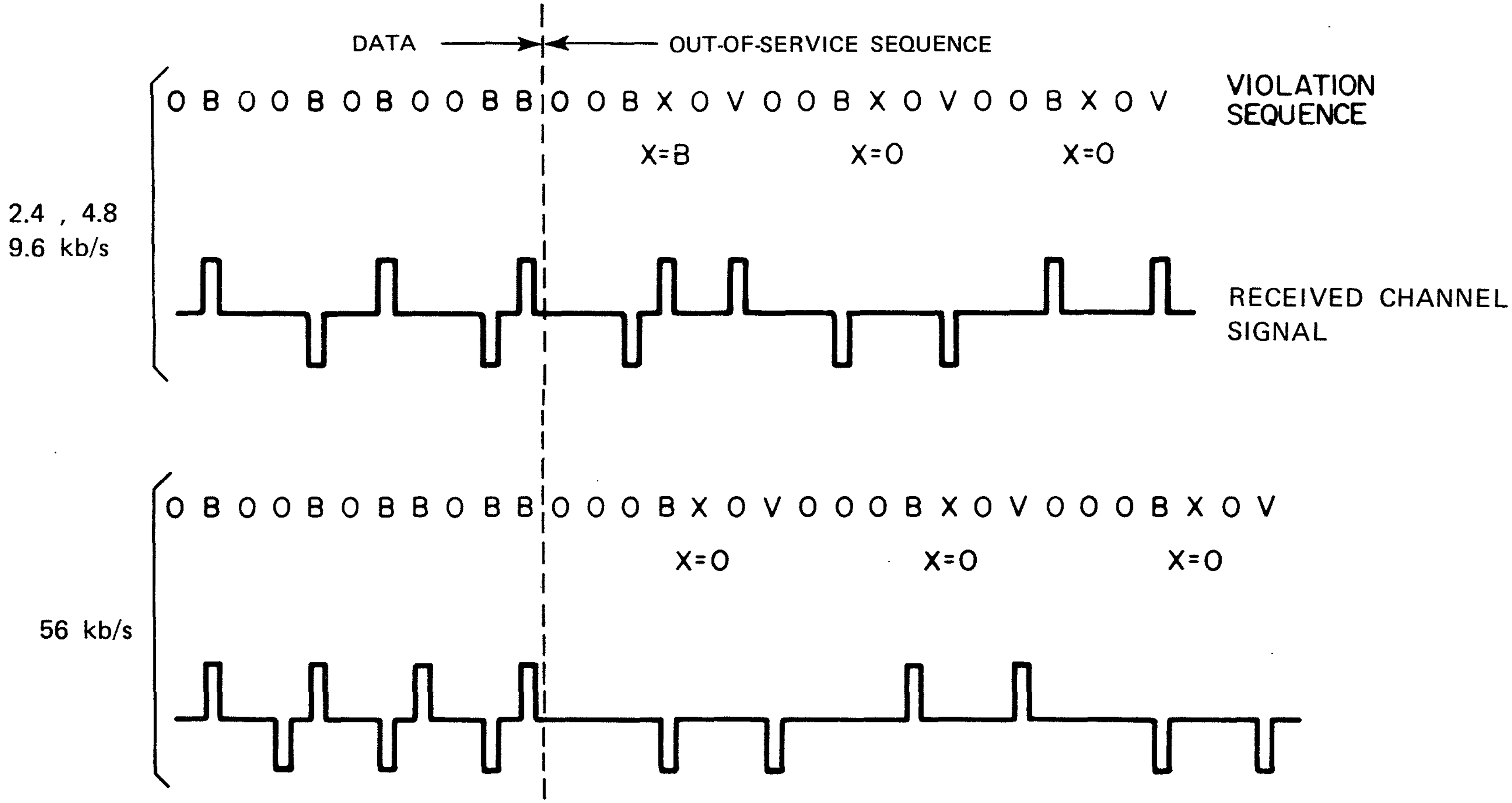


NOTE:

ZERO SUPPRESSION SEQUENCE WITHIN DOTTED LINES

FOR SEQUENCES I AND 2 IT IS ASSUMED THAT FOR THE FIRST X THE NUMBER OF B'S SINCE LAST V IS ODD AND EVEN, RESPECTIVELY

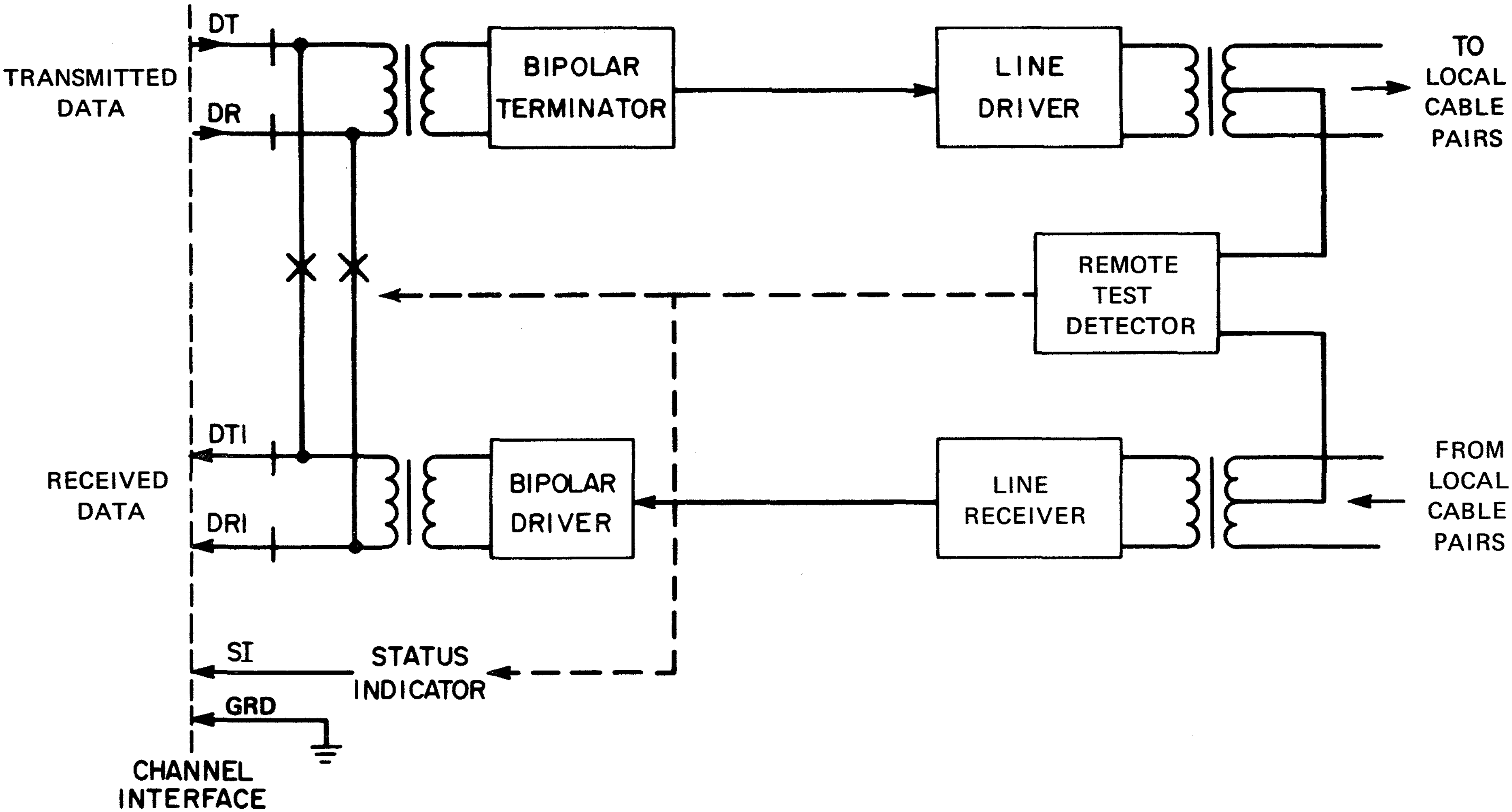
ZERO SUPPRESSION SEQUENCE
FIGURE 7



Note:
First X may be O or B depending on number of Bs since last V. The remaining Xs in Out-of-Service sequence are Os.

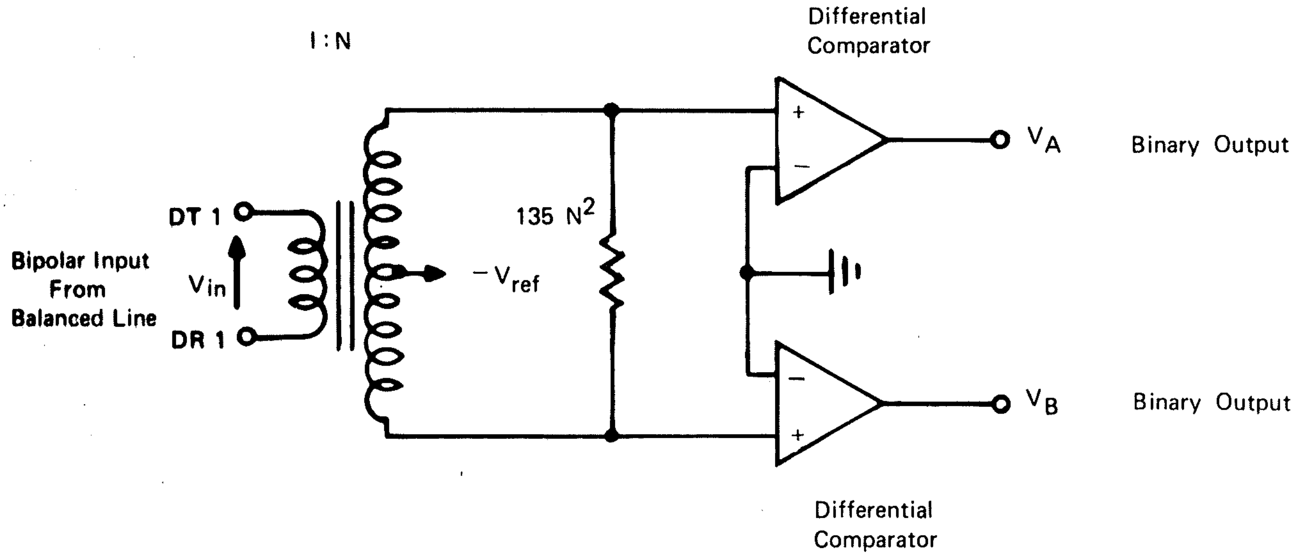
OUT-OF-SERVICE SEQUENCE

FIGURE 8

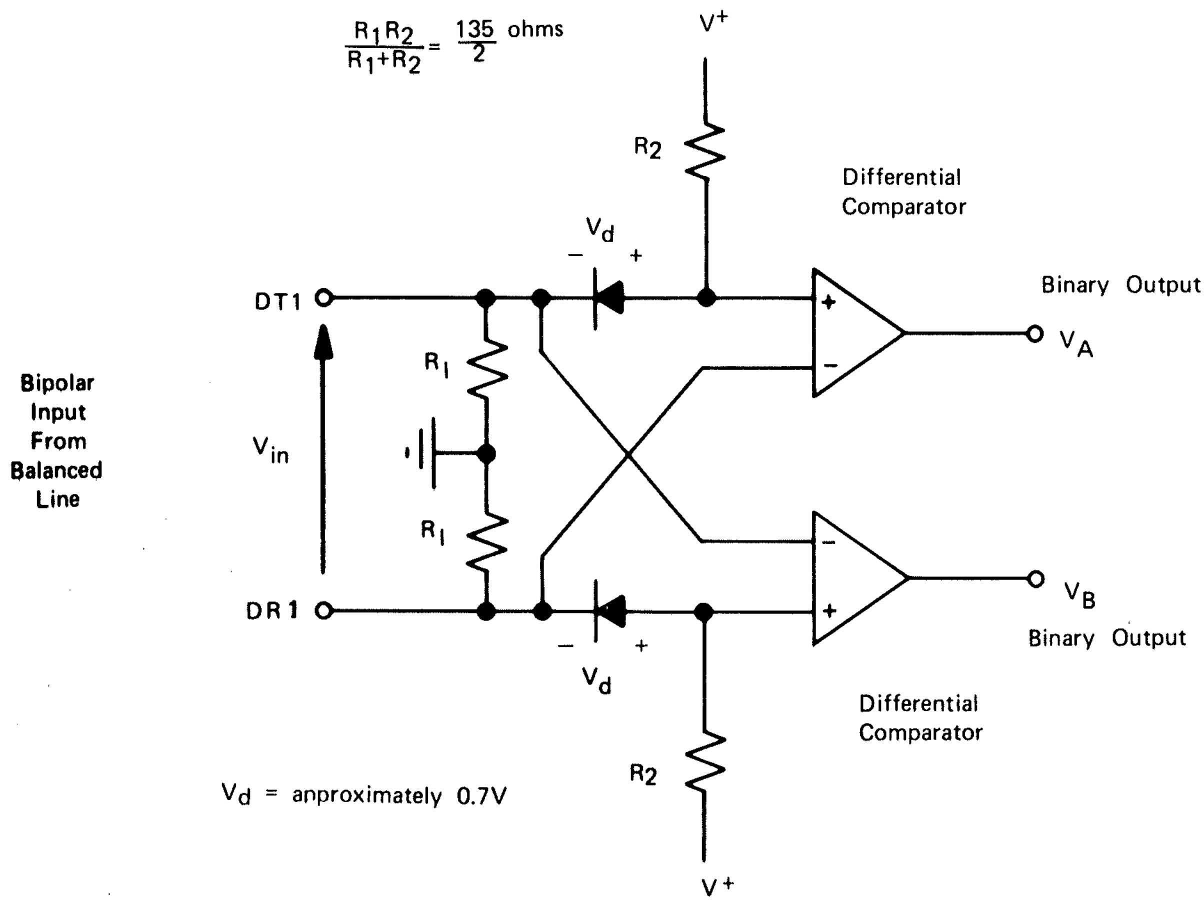


BLOCK DIAGRAM OF CHANNEL SERVICE UNIT

FIGURE 9

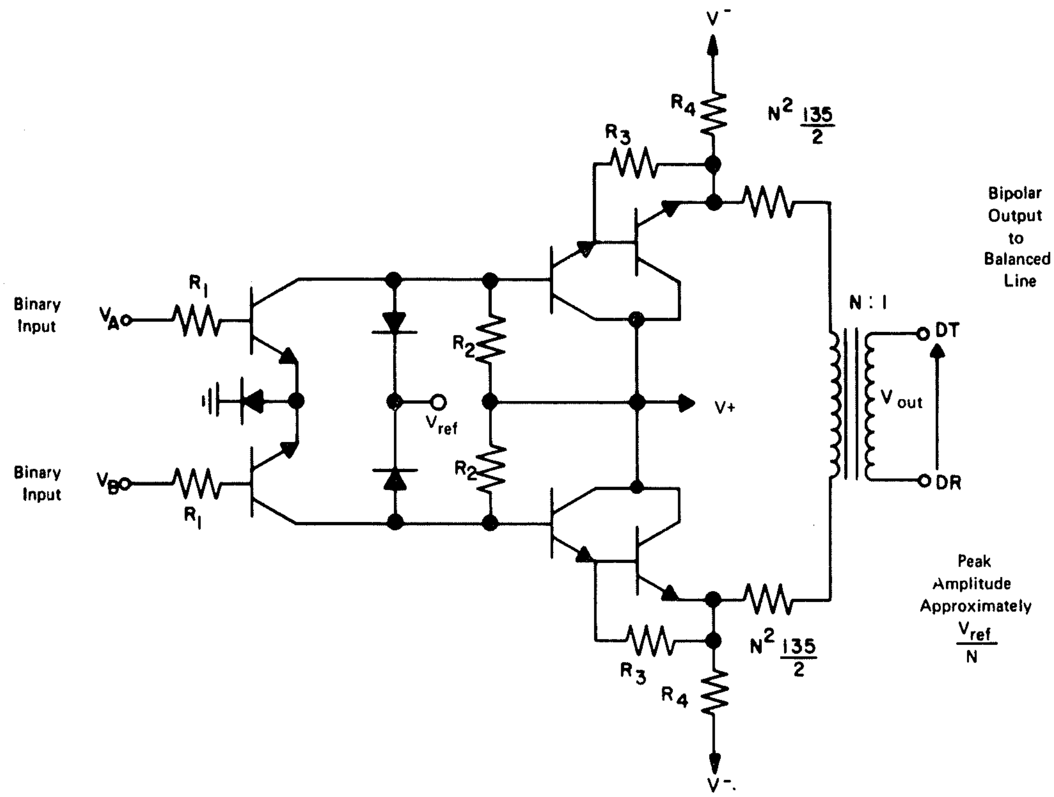


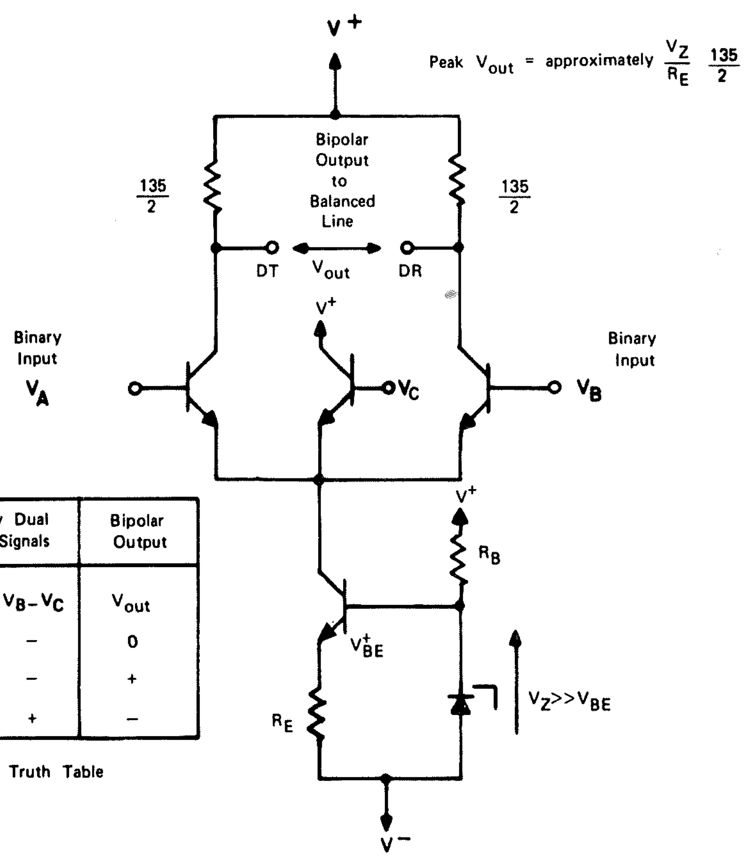
V_{ref} = approximately $0.7\,(\frac{N}{2})\,V$



BALANCED BIPOLAR INTERFACE CABLE TERMINATOR

FIGURE 10



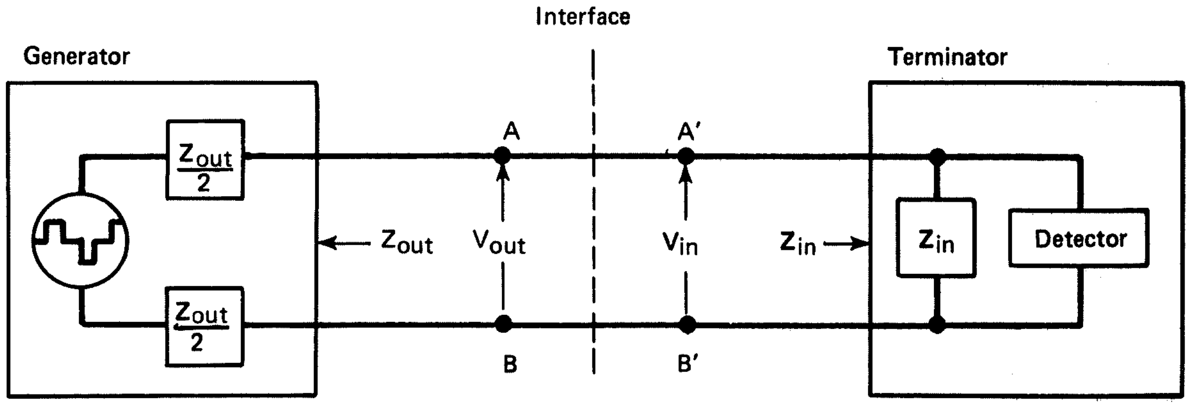


Binary Dual Rail Signals		Bipolar Output
V_A-V_C	V_B-V_C	V_{out}
–	–	0
+	–	+
–	+	–

Truth Table

BALANCED BIPOLAR INTERFACE CABLE DRIVER

FIGURE 11



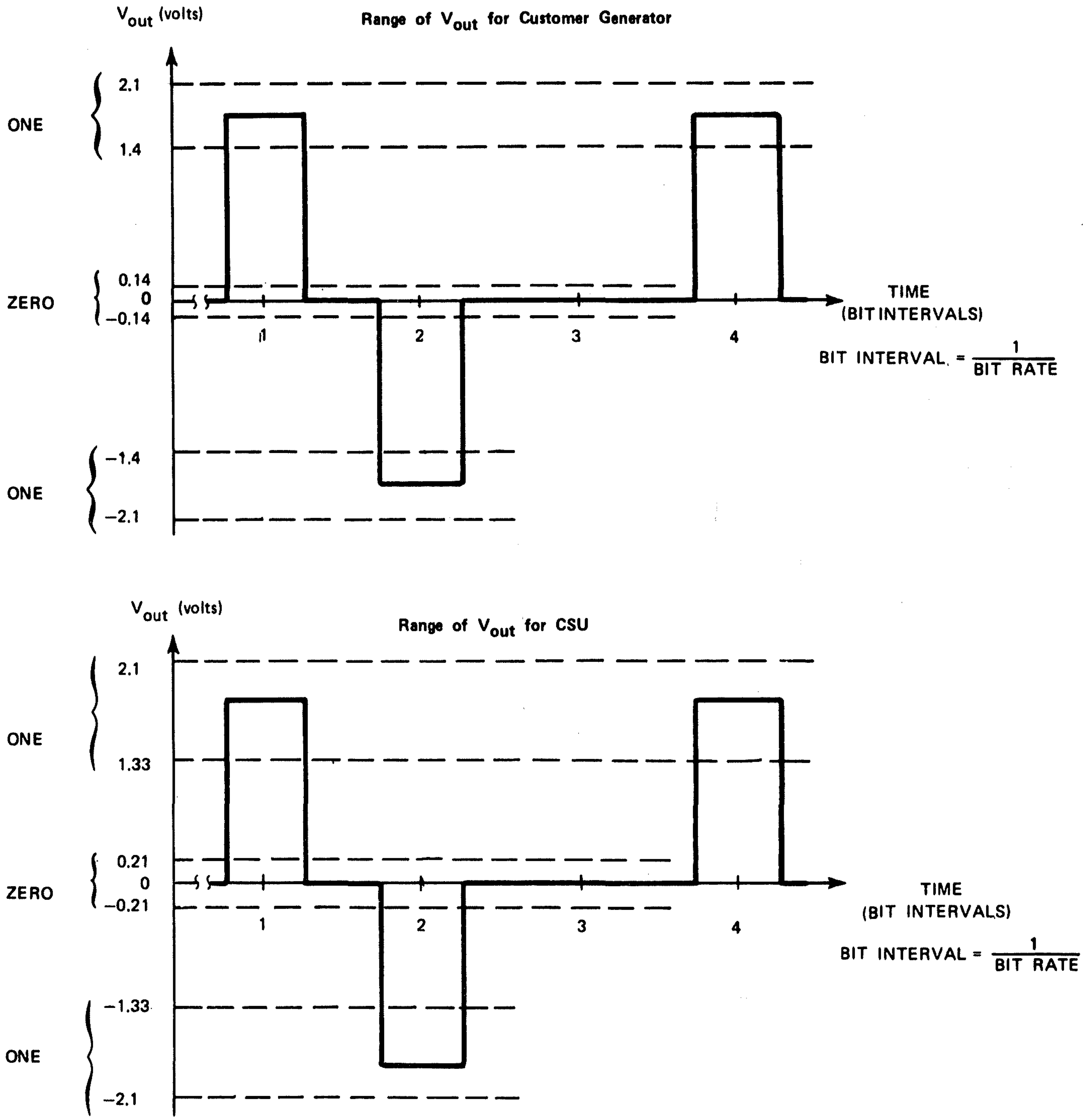
Notes:

1. For signals on the Transmitted Data leads (DT, DR)
   - the generator is in the customer's equipment
   - the terminator is in the CSU

2. For signals on the Received Data leads (DT1, DR1)
   - the generator is in the CSU
   - the terminator is in the customer's equipment

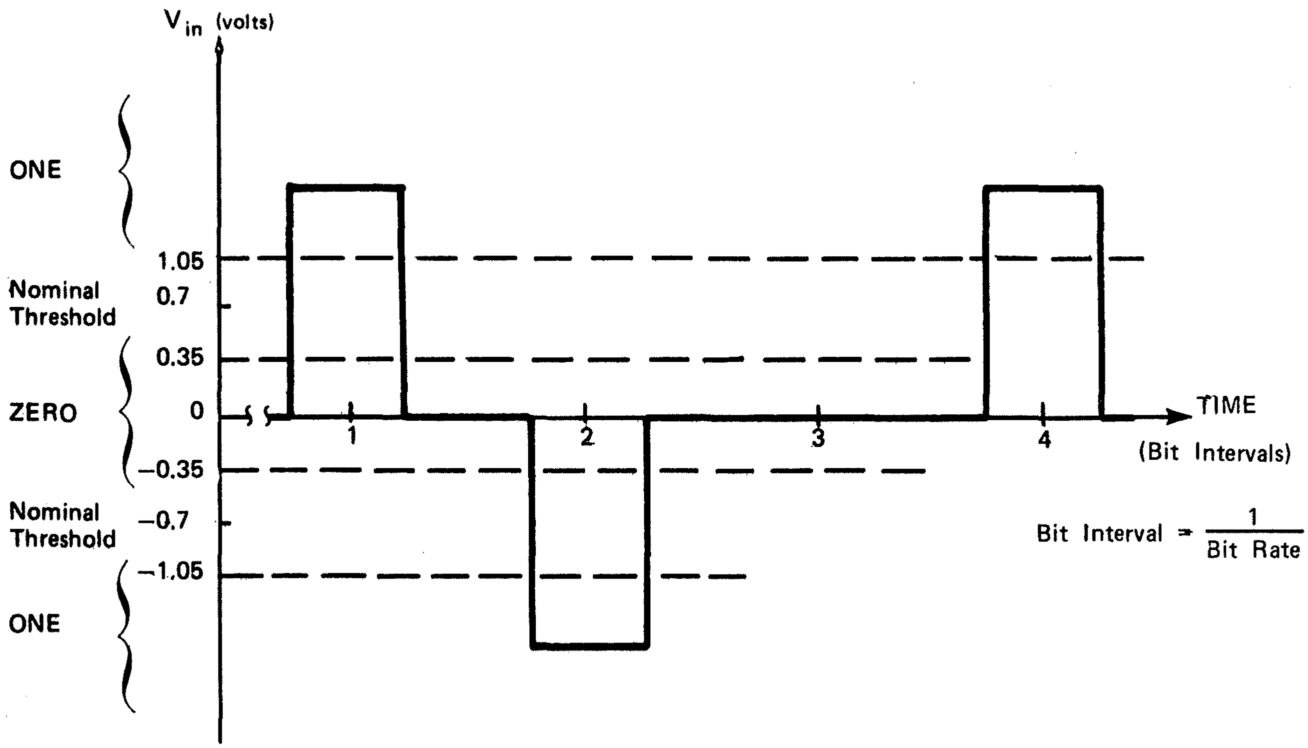
3. The differential impedances, Z_{out} and Z_{in} are defined with respect to pulse-type signals rather than sinusoidal ones. The impedances are measured when transmitting or receiving a bipolar pulse train at the nominal bit rate, signal level and duty-cycle with a 135-ohm resistive load or source respectively.

DIFFERENTIAL VOLTAGES
FIGURE 12



Note: V_{out} is a differential ac Voltage across a 135-ohm resistive termination.

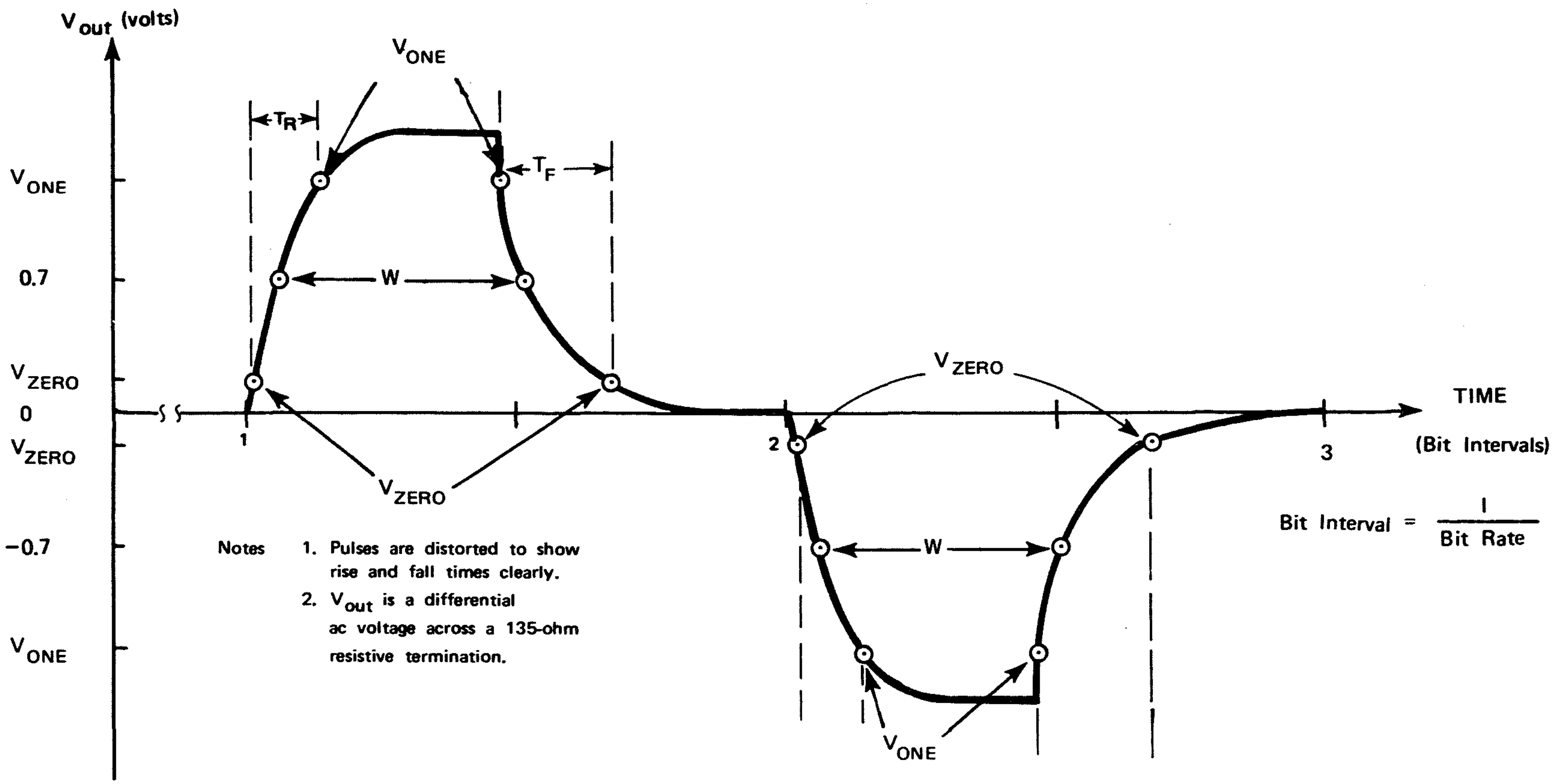
OUTPUT VOLTAGE RANGE
FIGURE 13



Notes: V_{in} is the normalized input voltage that is applied to a customer's terminator or the CSU terminator. V_{in} is said to be normalized when it is the voltage obtained when the source of test pulses has a 135-ohm resistive termination.

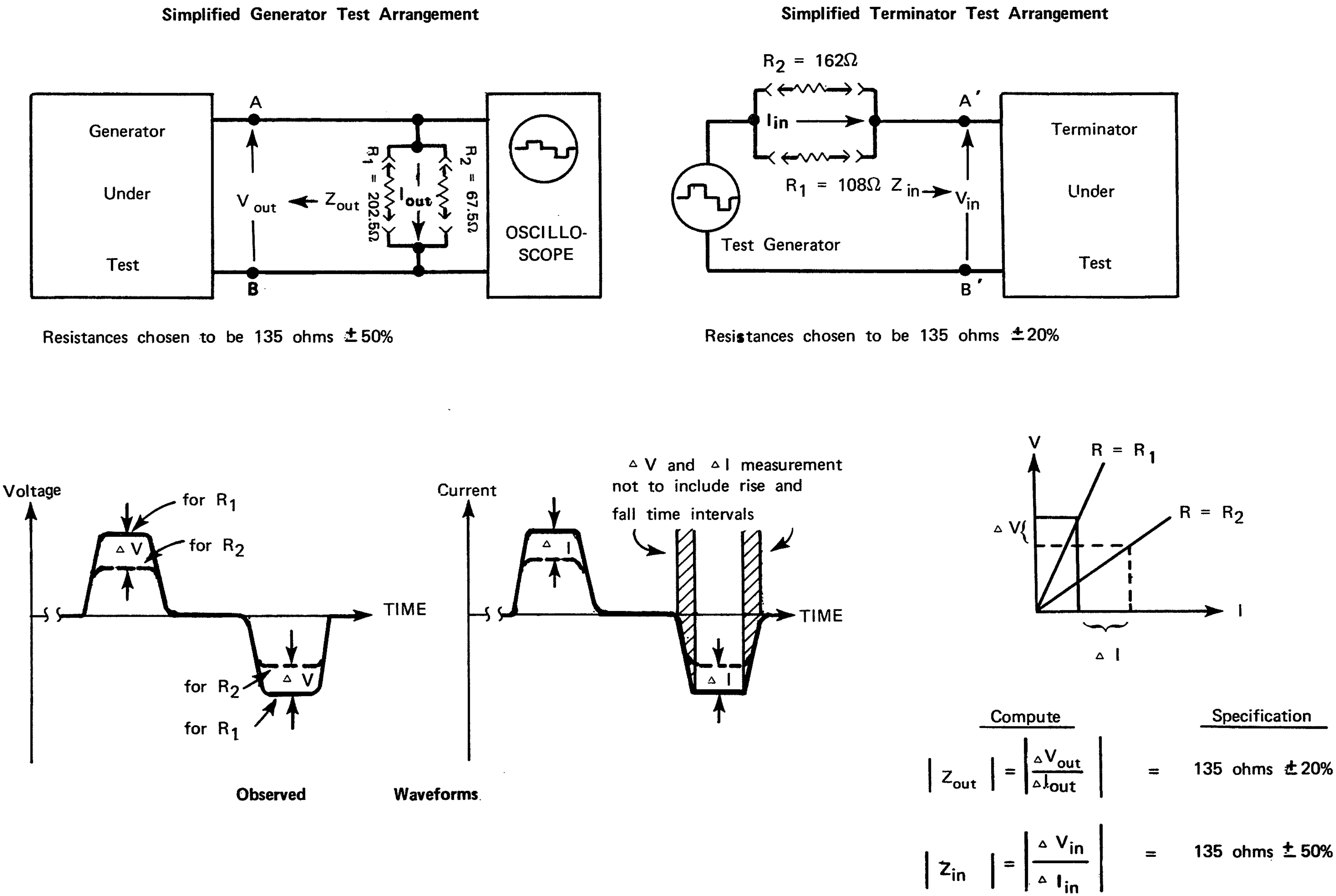
TERMINATOR THRESHOLD VOLTAGES

FIGURE 14

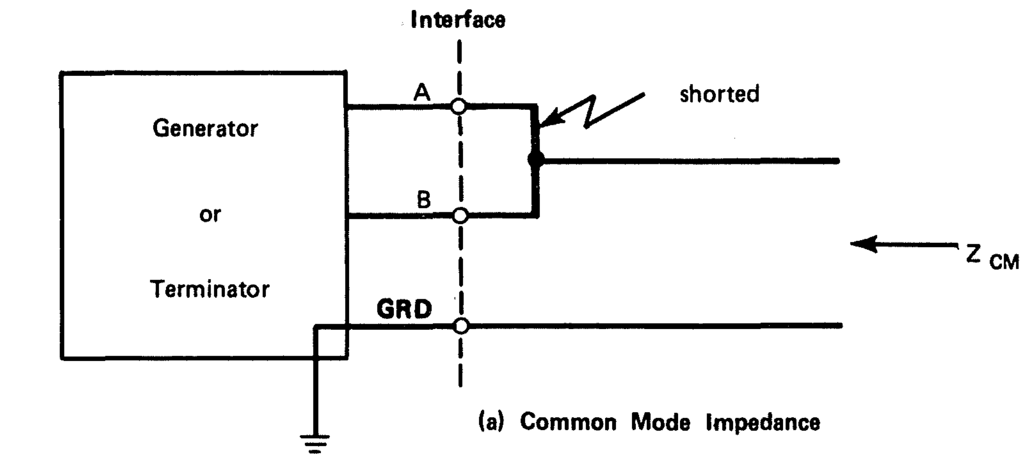


Symbol	Definition	Specification	
T_R	Rise Time	Not to exceed 5% of a Bit Interval	
T_F	Fall Time	Not to exceed 5% of a Bit Interval	
W	Pulse Width	Customer to CSU	– 47.5% to 52.5% of a Bit Interval
		CSU to Customer	– 45% to 90% of a Bit Interval
V_{ONE}	Minimum ac voltage for a binary one	Customer Generator	– 1.4 volts
		CSU Generator	– 1.33 volts
V_{ZERO}	Maximum ac voltage for a binary zero	Customer Generator	– 0.14 volts
		CSU Generator	– 0.21 volts

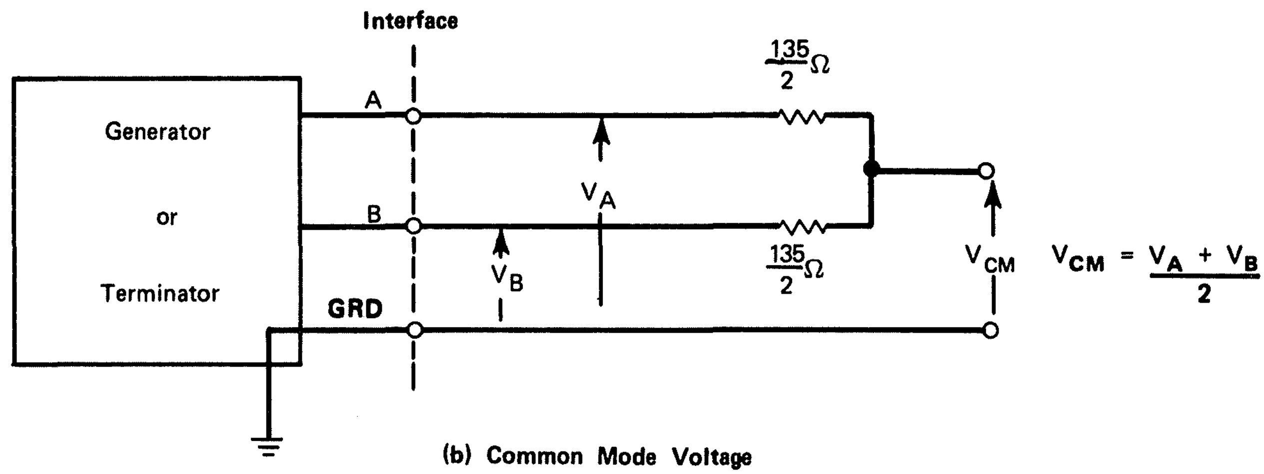
BIPOLAR PULSE CHARACTERISTICS
FIGURE 15



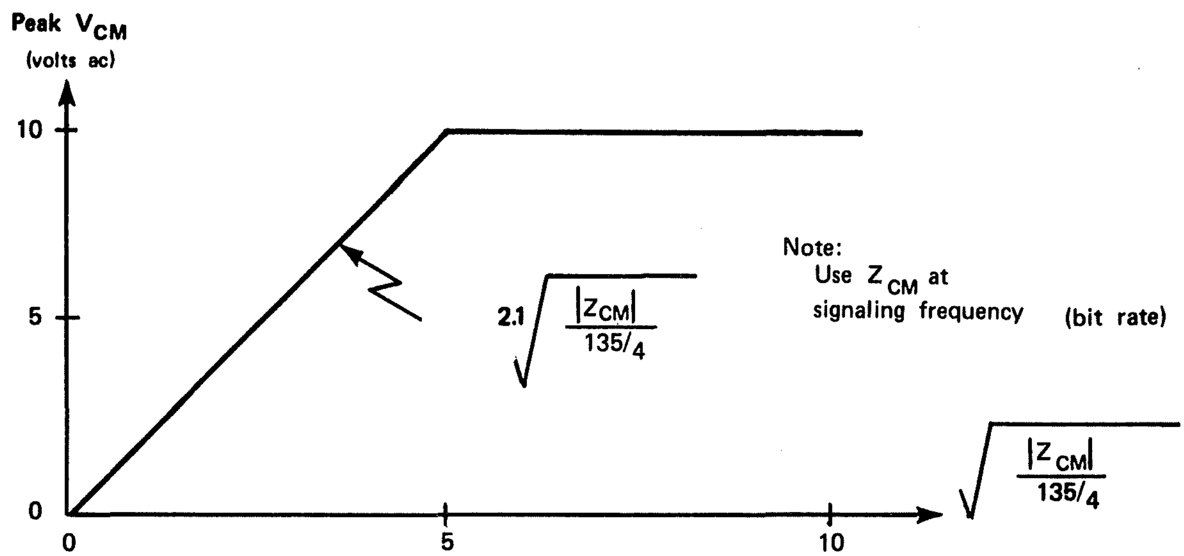
DIFFERENTIAL IMPEDANCE
FIGURE 16



(a) Common Mode Impedance

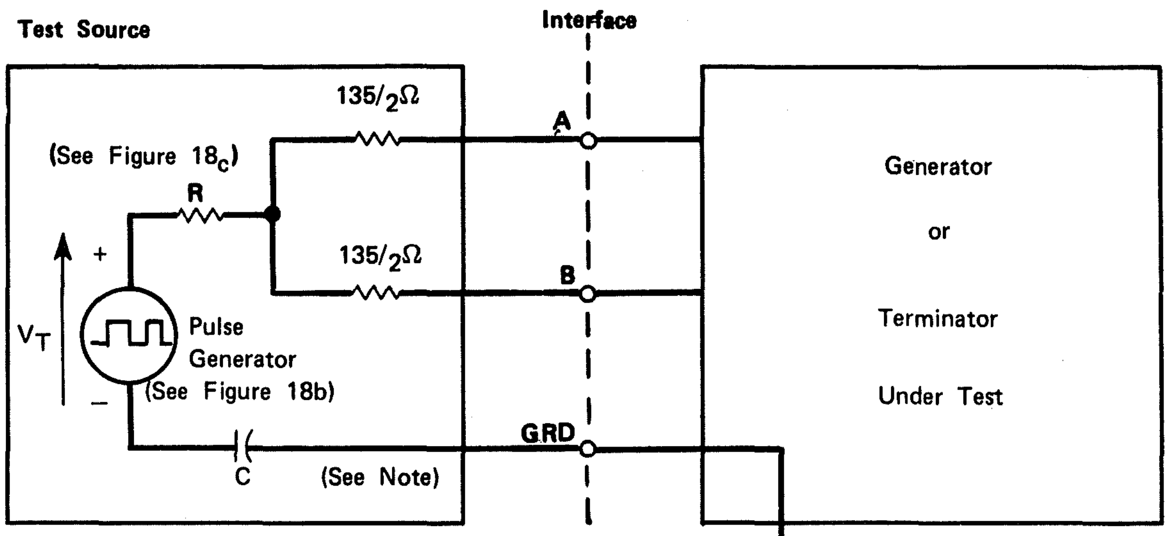


(b) Common Mode Voltage



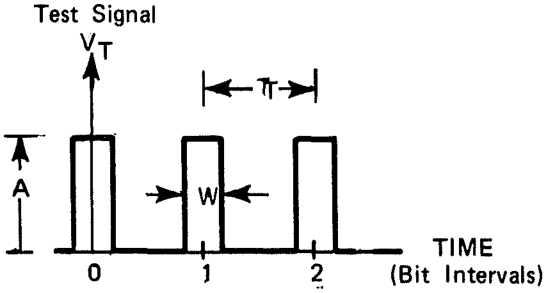
(c) Peak V_{CM} (ac) as a Function of Z_{CM} (output from generator or terminator)

COMMON MODE IMPEDANCE AND VOLTAGE
FIGURE 17



Note: The capacitor C allows tests on equipment having a dc common mode voltage present. The value of C is chosen so its impedance will be negligible at all significant frequencies.

(a) Test Arrangement

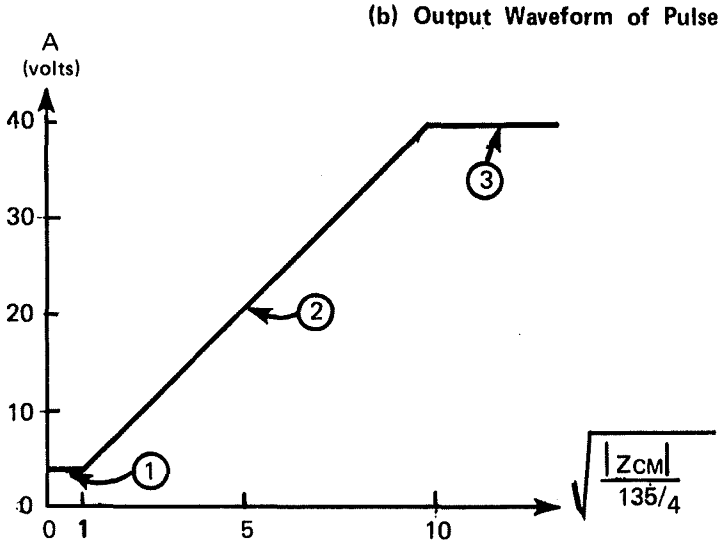


A = Pulse Amplitude
(determined from Figure 18c)

T = Bit Interval = $\frac{1}{\text{Bit Rate}}$

W = Pulse Width
$0.1T \leq W \leq 0.9T$
Rise and fall times $\leq 0.01T$

(b) Output Waveform of Pulse Generator

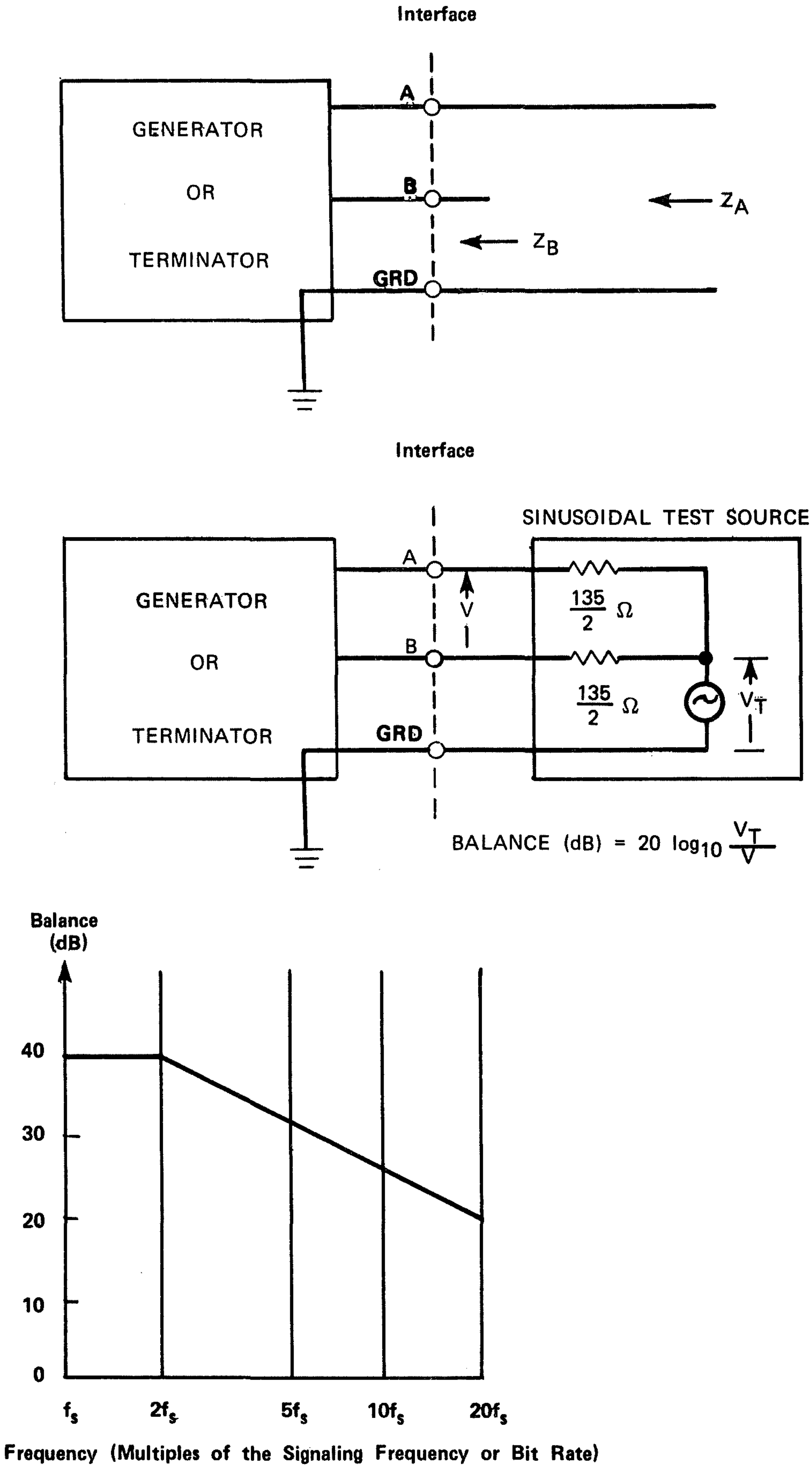


Region	R_T (ohms)
1	0
2	$\left\lvert Z_{CM} - \frac{135}{4} \right\rvert$
3	$10\left(\frac{135}{4}\right)^2$ or 11400

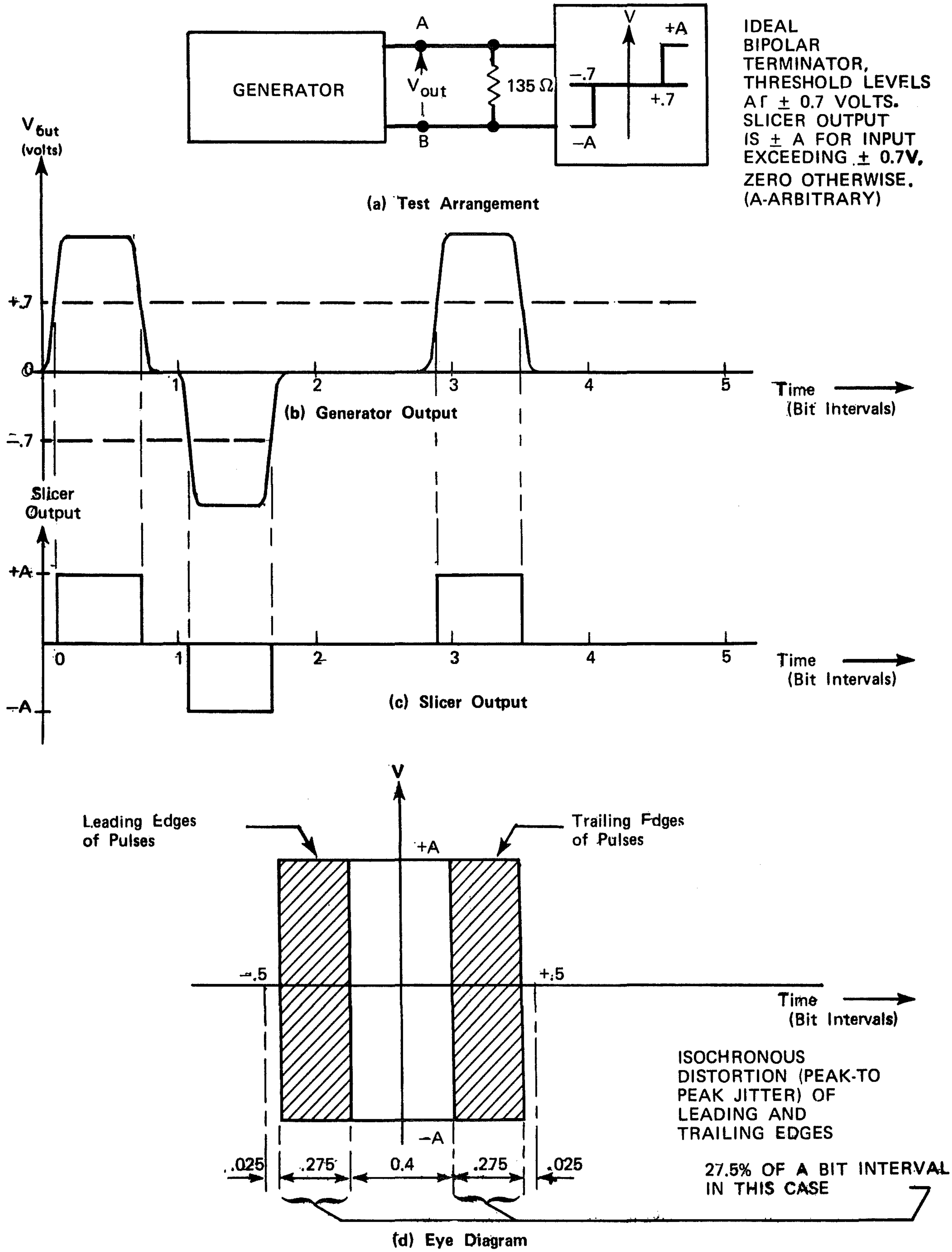
Note: Use Z_{CM} at signaling frequency (bit rate)

(c) Pulse Amplitude as a Function of Z_{CM}

COMMON MODE INPUT VOLTAGE RANGE
FIGURE 18



IMPEDANCE BALANCE
FIGURE 19



ISOCHRONOUS DISTORTION
FIGURE 20

APPENDIX

Timing Recovery Definitions

This appendix is included to provide a convenient reference for the definition of isochronous and peak individual distortion of data signal transitions. These terms are also used and discussed in two publications:

EIA Standard RS-334, "Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission."

EIA Industrial Electronics Bulletin No. 5, March, 1956, "Tutorial Paper on Signal Quality at a Digital Interface."

Definitions

In the following discussion, the term "unit interval" means the reciprocal of the data rate. The term "significant instant of modulation" with reference to a bipolar data signal, means the instant the signal crosses a preset threshold level. In the case of the CSU interface, the levels are ±0.7 volts, measured across a 135-ohm resistance at the generator terminals.

Degree of Individual Distortion of a Particular Significant Instant (from Bulletin No. 5):

"The ratio to the unit interval of the displacement, expressed algebraically, of this significant instant from an ideal instant. This displacement is considered positive when the significant instant occurs after the ideal instant. The degree of individual distortion is usually expressed as a percentage."

Degree of Peak Individual Distortion (from RS-334):

"The maximum individual distortion, irrespective of sign, of all significant instants occurring during a particular measuring period."

Degree of Isochronous Distortion (from RS-334):

1. "Ratio to the unit interval of the maximum measured difference, irrespective of sign, between the actual and the theoretical intervals separating any two significant instants . . . , these instants being not necessarily consecutive."

2. "Algebraical difference between the highest and lowest value of individual distortion affecting the significant instants of an isochronous modulation. (This difference is independent of the choice of the reference ideal instant.)"

In the case of both isochronous and peak individual distortion, the length of observation is also important. In the case of a prolonged observation, it is appropriate to consider the probability that a given degree of distortion will be exceeded.

Applications

To apply these definitions to the CSU interface, the expected nature of the data signals must be considered. The Transmitted Data (DT, DR) from the customer data terminal to the CSU is expected to be synchronous with the DDS, relatively noise-free, and well-controlled in width (nominal 50% duty-cycle.)

The requirement of synchronism implies that the theoretical instants of transition are related to the average of the transitions of the received data. For example, a clock would have its negative-going transitions occurring midway between the average of the positive and negative-going transitions of the received data.

The measurement of peak individual distortion then proceeds as illustrated in Figure A. Since the signals on DT and DR are relatively noise-free, fairly large measuring intervals may be used.

The distortion of signals transmitted from the CSU to the customer is largely determined by the characteristics of the cable pair from the Telephone Company office to the customer location. The duty-cycle is not controlled here. Noise bursts may cause data transitions to occur anywhere within the unit interval. In the theoretical noise-free case, the dispersion of the transitions from an ideal instant will be due to intersymbol interference and data pattern variations.

Timing Recovery

Timing recovery in data transmission commonly involves applying the received signal, or a processed version thereof, to a high-selectivity circuit, such as an LC tank or a phase-locked loop, to extract the fundamental bit frequency. The equivalent circuit for these schemes usually reduces to a low-pass filter acting on the input jitter of the received data transitions.

The data signal is then sampled at clock transitions in phase with the nominal center of the received pulses.

Since the low-pass character of the timing circuit attenuates high-frequency jitter, attention is focussed on the low-frequency input and output jitter. An empirically verified theory, discussed below, leads to a useful figure of merit for the quality of the received signal transitions and establishes performance limits for the synchronous sampling circuits described above.*

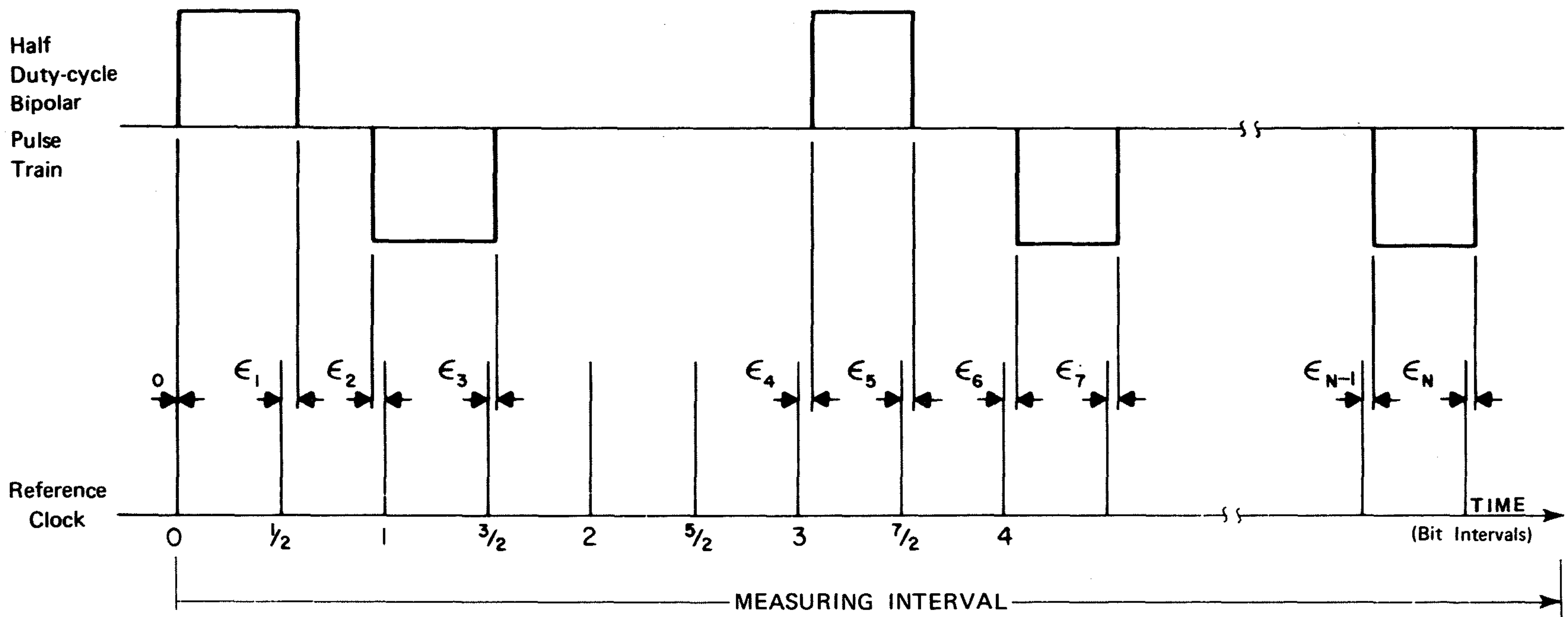
* Byrne, C.J., Karafin, B. J., and Robinson, D. B., Jr., "Systematic Jitter in a Chain of Digital Regenerators," Bell System Technical Journal, November, 1963, pp. 2679-2714.

We suppose that the input jitter depends only on the last few bits transmitted, and consider a repetitive pattern with period much less than the reciprocal of the bandwidth, B. Associated with this periodic pattern is an average or dc phase shift, θ_1, corresponding to the location of the average of the pulse centers; the phase is measured with respect to the transitions of an appropriate ideal clock signal. Now suppose the pattern is suddenly switched to one with average phase, θ_2. The data transitions adjust their phase to θ_2 in a few bit's time, the assumed memory span of the jitter mechanism. The recovered clock phase, however, changes at a rate $B(\theta_2-\theta_1)$, and thus requires a time 1/B to adjust to the new phase (See Figure B.)

Evidently, the recovered timing signal has an irreducible phase jitter of $\theta_1-\theta_2$; moreover, the data sampling instant is offset from the nominal pulse center by $\theta_2-\theta_1$ immediately following the change in pattern.

Thus, the worst-case peak-to-peak dc phase shift between any two repetitive patterns represents a figure of merit for the quality of the received data transitions.

It is independent of the particular realization in this class of timing and sampling circuits.



LEGEND:

$100.0 \times \epsilon_i$ = Individual Distortion of i^{th} significant instant (%) (i = 1, 2, . . . N)

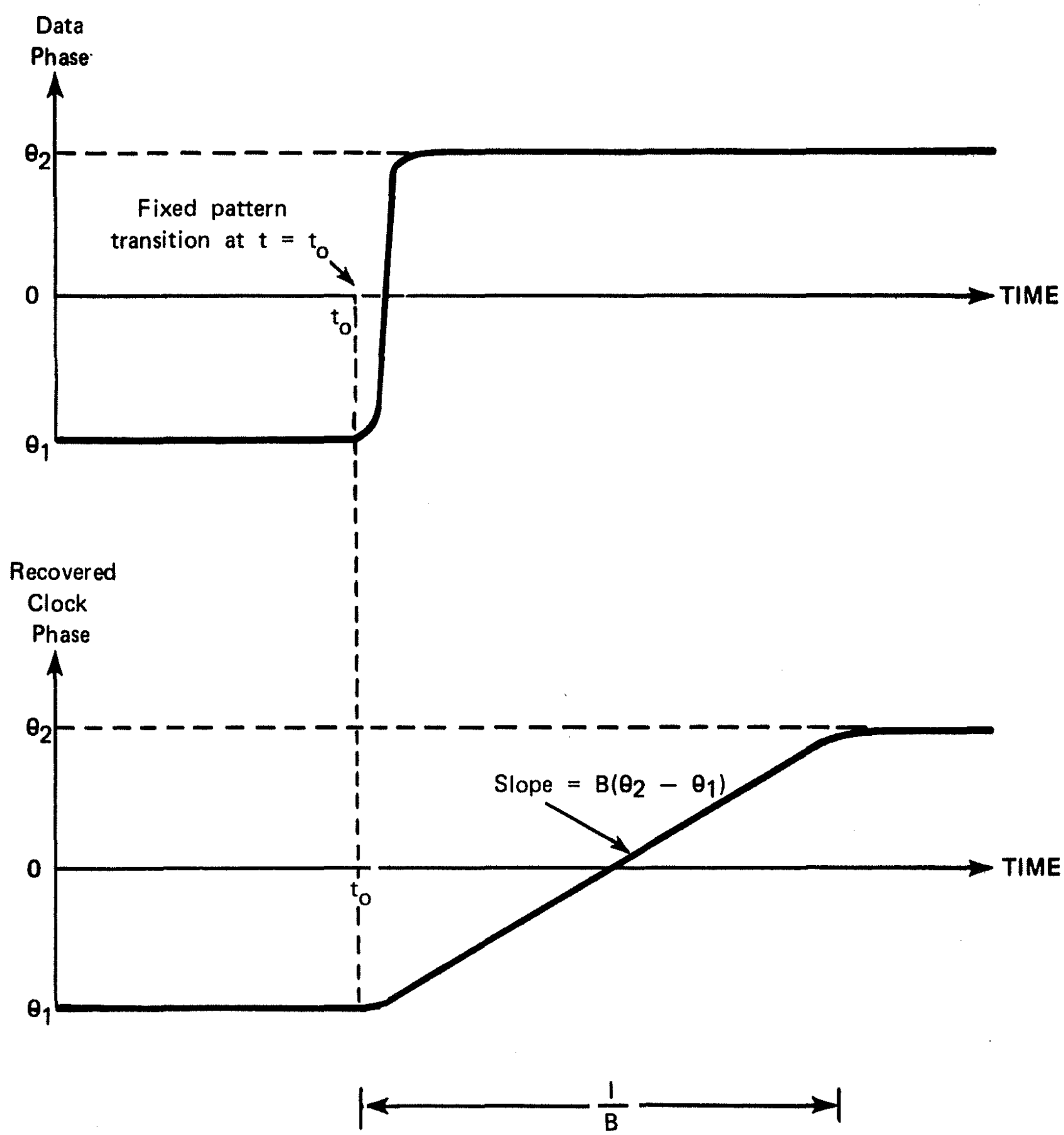
ϵ_{max} = Maximum $|\epsilon_i|$ observed in measuring interval (i = 1, 2, . . . N)

$100.0 \times \epsilon_{max}$ = Peak Individual Distortion

δ_{max} = Maximum $|\epsilon_i - \epsilon_j|$ between any two Individual Distortions observed in measuring interval. (i, j = 1, 2, . . . N) not necessarily consecutive pulses.

$100.0 \times \delta_{max}$ = Isochronous Distortion (%)

TIMING DISTORTION
FIGURE A



B = Timing circuit bandwidth

EFFECT OF FIXED PATTERN TRANSITIONS
ON RECEIVED CLOCK PHASE

FIGURE B

INDEX